RD-V3-R1 Fixed Virtual Platform

Revision 1129

User Guide

Non-Confidential

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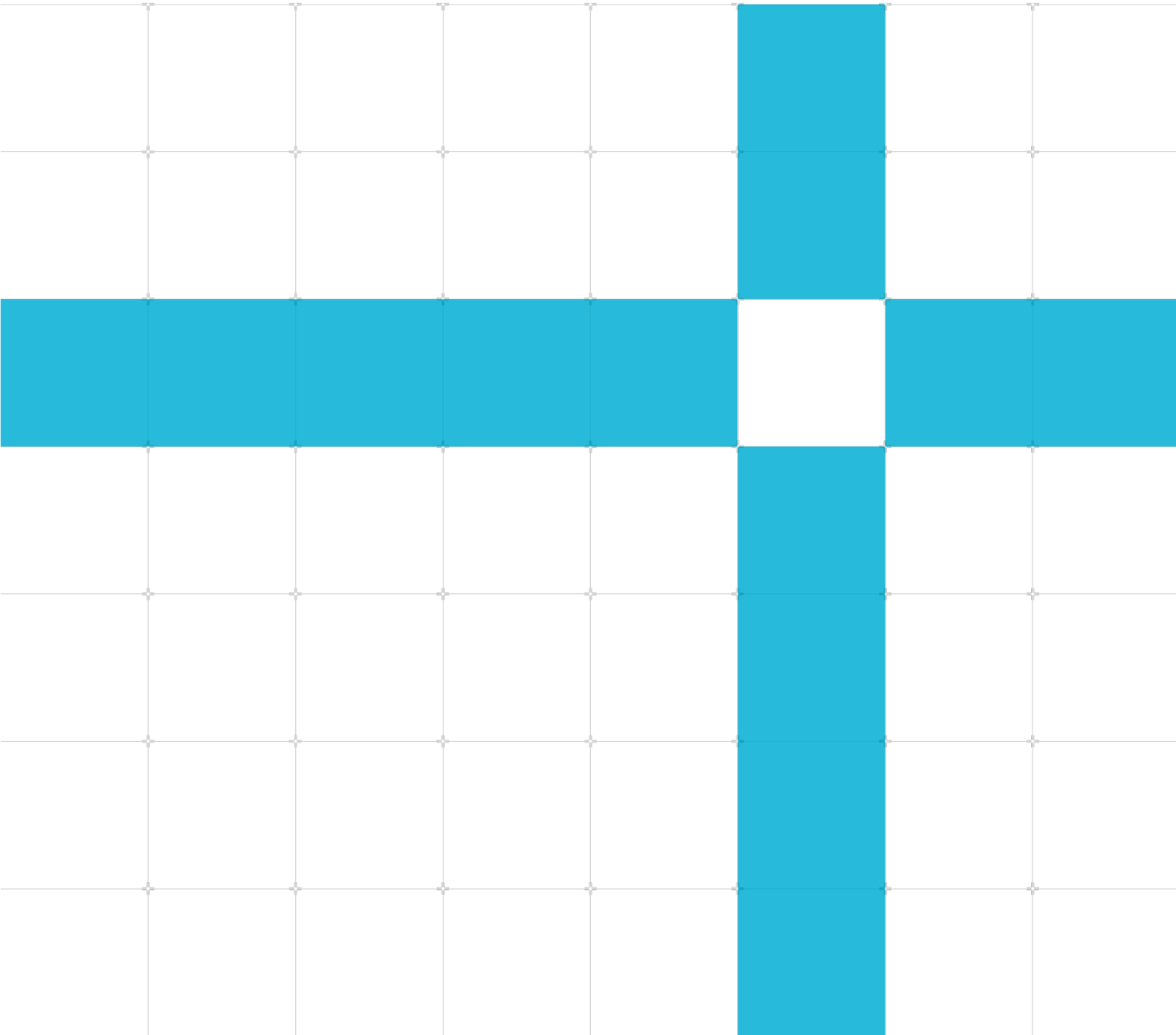

RD-V3-R1 Fixed Virtual Platform User Guide

This document (110024_1129_00_en) was issued on 26 September 2025. There might be a later issue at http://developer.arm.com/documentation/110024

The product revision is 1129.

See also: Product and document information | Useful Resources

Start reading

If you prefer, you can skip to the start of the content.

Intended audience

This book is written for hardware or software engineers who want an overview of the non-CSS components and functionality in the RD-V3-R1 Fixed Virtual Platform.

Inclusive language commitment

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We believe that this document contains no offensive language. To report offensive language in this document, email terms@arm.com.

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To provide feedback on the document, fill the following survey: https://developer.arm.com/documentation-feedback-survey.

Contents

1. Fixed Virtual Platforms

You can use a Fixed Virtual Platform (FVP) to develop software without prototype hardware. Arm FVP models use binary translation technology to deliver fast simulations of Arm-based systems.

The RD-V3-R1 Reference Design FVP supports system architecture and software standardization. It enables early and efficient software and firmware development, reducing the amount of work needed to bring up a complete system.

2. FVP configurations

The RD-V3-R1 FVP models the following configurations:

- RD-V3-R1-Cfg1 implements a homogeneous quad-chiplet configuration, which supports:
  - 32xMP1 Arm® Neoverse™ V3 cores
  - Arm Neoverse CMN S3 interconnect with a 3x4 mesh network
  - 8 IOMACRO blocks
  - 8 shared LCP groups. Each group integrates 4xMP1 Arm Neoverse V3 cores.
- RD-V3-R1 implements a homogeneous dual-chiplet configuration, which supports:
  - 28xMP1 Arm Neoverse V3 cores
  - Arm Neoverse CMN S3 interconnect with a 9x8 mesh network
  - 6 IOMACRO blocks
  - 14 shared LCP groups. Each group integrates 2xMP1 Arm Neoverse V3 cores.

3. FVP components

The FVP models the following IP components:

- Arm Neoverse V3 cores
- Arm Neoverse CMN-S3 Coherent Mesh Network interconnect
- Arm CoreLink™ NOC S3 Non-Coherent Interconnect
- Arm CoreLink GIC-700 Generic Interrupt Controller
- Arm CoreLink MMU S3 System Memory Management Unit
- System Control Processor (SCP) based on the Arm Cortex®-M7 processor
- Manageability Control Processor (MCP) based on the Arm Cortex-M7 processor
- Local Control Processor (LCP) based on the Arm Cortex-M55 processor
- Runtime Security Engine (RSE) based on the Arm Cortex-M55 processor
- On-Chip ROM, RAM, and other peripherals
- Multiple AXI expansion ports for I/O Coherent PCIe (IOMACRO).
- Clock generators

The FVP does not model the following IP components that RD-V3-R1 describes:

- Arm CoreSight™ System-on-Chip SoC-600
- Third-party DDR5 controller configured for memory

4. Prerequisites

This FVP supports the following host architectures, operating systems, and compilers.

4.1. Disk space required

The FVP bundle requires approximately 4 GB to download and approximately 500 MB to unpack and install.

4.2. Architecture

The FVP supports x86-64 and Arm® AArch64 host platforms.

4.3. Recommended specification

The FVP requires at least 32 GB of RAM, but we recommend 48 GB.

Fast Models and associated FVPs benefit most from high single-threaded performance. For example, a host CPU with a high frequency (4 GHz - 5 GHz) such as Intel Core i9 or i7 or AMD Ryzen 9 or 7, can improve performance by 30-60% over lower-frequency Intel Xeon cores (2 GHz -3 GHz).

For more information, see Optimizing runtime performance of Fast Models.

4.4. Operating system

- Red Hat Enterprise Linux 7 or 8 (for 64-bit architectures)
- Ubuntu 22.04 or 24.04 Long Term Support (LTS)
- Microsoft Windows 10 64-bit

4.5. Compiler

This FVP was built using Visual Studio 2019 and GCC 9.3.0.

5. Downloading and installing the FVP

Arm delivers the FVP through Arm Developer.

5.1. Download the FVP bundle

1. Go to Arm Ecosystem FVPs.
2. Select the section titled Infrastructure FVPs.
3. To download the FVP bundle, in the section Neoverse V3 r1 Reference Design FVP, choose the appropriate package for your target platform:
   - Linux
   - Linux Arm Host
   - Windows

The FVP bundle contains the following components:

- FVP installer
- Release notes
- Fast Models FVP Reference Guide

5.2. Unpack the FVP Linux bundle

1. Copy the `.tgz` file to your chosen installation directory.
2. Extract the `.tar` file contents using the UNIX `tar` utility. For example:

```
tar -xzvf FVP_RD_V3_R1_11.29_35_Linux64.tgz
```

3. Extracting the `.tar` file creates `FVP_RD_V3_R1.sh`, which is the FVP installer. Run this file to install the FVP:

```
./FVP_RD_V3_R1.sh
```

The FVP installer includes a `license_terms` directory, which contains the licenses under which the FVP is distributed.

5.3. Software bundle

The FVP is used with the RD-V3-R1 software package. See the RD-V3-R1 software bundle readme on GitLab for setup and usage instructions.

6. FVP peripherals

The RD-V3-R1 Reference Design FVP has two main parts:

- Reference subsystem or Compute Subsystem (CSS)
- Rest of the System (RoS) with expansion peripherals

The RoS contains components that are not defined in the RD-V3-R1 Reference Design subsystem. These components create the necessary environment for running and developing a reference software stack.

The RoS components connect to the CSS through its expansion interfaces. This setup reflects how the CSS is integrated in a SoC and board.

The peripherals in the RD-V3-R1 RoS are required for the software payload to run. They represent peripherals that might be added to a CSS in a SoC design. The RD-V3-R1 SoC model is based on the Juno Arm Development Platform (ADP).

The RoS peripherals region in the RD-V3-R1 memory map is mapped to a customer expansion region (AMBA® AXI) memory space. Therefore, these mappings are not defined in the Reference Design. They are shown in the following table:

6.1. FVP RoS peripherals memory map

The following table shows the memory map for the RoS peripherals region:

Name	Base address	Size	Description
NOR flash 0	0x00_0800_0000	64 MB	-
NOR flash 1	0x06_5000_0000	64 MB	-
NOR flash 2	0x06_5400_0000	64 MB	-
NOR flash 3	0x06_5800_0000	64 MB	-
Ethernet	0x06_5C00_0000	64 MB	Non-PCIe Ethernet controller (SMSC 91C111)
System registers	0xC010000	64 KB	-
PL180 MCI	0xC050000	64 KB	Arm PrimeCell Multimedia Card Interface (PL180)
KMI 0	0xC060000	64 KB	Arm PrimeCell PS2 Keyboard/Mouse Interface (PL050)
KMI 1	0xC070000	64 KB	Arm PrimeCell PS2 Keyboard/Mouse Interface (PL050)
UART2	0xC090000	64 KB	Arm PrimeCell UART (PL011)
UART3	0xC0A0000	64 KB	Arm PrimeCell UART (PL011)
Watchdog SP805	0xC0F0000	64 KB	Arm Watchdog Module (SP805)
Virtio block device	0xC130000	64 KB	-

Name	Base address	Size	Description
Virtio RNG	0xC140000	64 KB	-
Virtio net	0xC150000	64 KB	-
GPIO 2Wire (DVI)	0xC160000	64 KB	Arm PrimeCell General Purpose Input/Output (PL061)
RTC0 PL031	0xC170000	64 KB	Arm PrimeCell Real Time Clock (PL031)
RTC1 PL031	0xC180000	64 KB	Arm PrimeCell Real Time Clock (PL031)
Virtio_P9	0xC190000	64 KB	-
GPIO0	0xC1D0000	64 KB	Arm PrimeCell General Purpose Input/Output (PL061)
GPIO1	0xC1E0000	64 KB	Arm PrimeCell General Purpose Input/Output (PL061)
PCIe config space	0x100_0000_0000	1 GB	ECAM0/1/2/3 PCIe NCI Memory space2
PCIe 32-bit memory	0x00_6000_0000	512 MB	PCIe MMIO
PCIe 64-bit memory	0x101_0000_0000	0.966 TB	PCIe MMIO
Non PCIe devices	0x07_C000_0000	256 MB	Non-PCIe devices connected to IOMACRO
SoC temperature sensor	0x00_0E03_0000	1 KB	-
SoC Interconnect NIC-400 GPV	0x00_0ED0_0000	1 MB	-
TRNG	0x00_0EE6_0000	4 KB	-
Trusted Non-volatile counters	0x00_0EE7_0000	4 KB	-
DDR3 PHY 0-31	0x00_0EB0_0000	2 MB	Dummy APB
HDLCD0	0x00_0EF6_0000	4 KB	-
UART 0	0x00_0EF7_0000	4 KB	-
UART 1	0x00_0EF8_0000	4 KB	-
System override registers	0x00_0EFF_0000	4 KB	-
AP configuration	0x00_0EFE_0000	64 KB	Granular Power Requester (GPR)
DRAM	0x00_8000_0000	2 GB	-
DRAM	0x200_8000_0000	190 TB	By default, 6 GB implemented in the FVP

6.2. FVP RoS peripherals interrupt map

The following table lists the interrupt IDs and their corresponding sources:

Interrupt ID	Source
131	RTC1
132	RTC0
133	UART0
134	UART1

Interrupt ID	Source
135	KMI1
136	GPIO0
137	GPIO1
138	I2C GPIO
139	MCIINTR0
140	MCIINTR1
141	SMSC 91C111
147	UART0
148	UART1
149	HDLCD controller 0
152	Virtio block device
153	Virtio_P9
154	Virtio net
156	Virtio RNG
171	TRNG
181	RTCC
182	WDT
183	KMI0
186	System Register – USB
187	System Register – Tile
188	System Register – Push button
189	System Register – Ethernet

6.3. FVP non-PCIe peripherals memory map

The following non-PCIe devices in the RoS are connected to the IOMACRO2 instance in RD-V3-R1 and to the IOMACRO1 instance in the RD-V3-R1-Cfg1 Reference Design. The memory is allocated from the AP-Memory Expansion region and each IOMACRO port is allocated 32 MB.

IOMACRO port number	Peripherals	Start address	Size	Interrupt ID
Port_0	PL011_UART0	0x07_C000_0000	64 KB	192
	MEM0	0x07_C001_0000	4 MB	-
	Reserved	0x07_C041_0000	-	-
Port_1	PL330_DMA0_NS	0x07_C200_0000	64 KB	194 - 202
	PL330_DMA0_S	0x07_C201_0000	64 KB	-

IOMACRO port number	Peripherals	Start address	Size	Interrupt ID
	Reserved	0x07_C202_0000	-	-
Port_2	PL011_UART1	0x07_C400_0000	64 KB	193
	Reserved	0x07_C401_0000	-	-
Port_3	PL330_DMA1_NS	0x07_C600_0000	64 KB	204 - 212
	PL330_DMA1_S	0x07_C601_0000	64 KB	-
	MEM1	0x07_C602_0000	4 MB	-
	Reserved	0x07_C642_0000	-	-
Port_4	MEM2	0x07_C800_0000	4 MB	-
	Reserved	0x07_C840_0000	-	-
RESERVED	-	0x07_CA00_0000	96 MB	-

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Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

Product status

The information in this document is Final, that is for a developed product.

Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
1127-00	October 01, 2024	Confidential	New document for v11.27
1129-00	September 26, 2025	Non-Confidential	Update for v11.29

Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: https://developer.arm.com/glossary.

Typographical conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
italic	Citations.
bold	Terms in descriptive lists, where appropriate.
`monospace`	Text that you can enter at the keyboard, such as commands, file and program names, and source code.

Convention	Use
`monospace underline`	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Terms that have specific technical meanings as defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.
	We recommend the following. If you do not follow these recommendations your system might not work.
	Your system requires the following. If you do not follow these requirements your system will not work.
	You are at risk of causing permanent damage to your system or your equipment, or of harming yourself.
	This information is important and needs your attention.
	This information might help you perform a task in an easier, better, or faster way.
	This information reminds you of something important relating to the current content.

Useful resources

This document contains information that is specific to this product. See the following resources for other relevant information.

- Arm documents are available on developer.arm.com/documentation. Confidential documents are only available to licensees, when logged in.
- Each document link in the tables below provides direct access to the online version of the document.

Arm product resources	Document ID	Confidentiality
Arm® Neoverse™ V3	-	Non-Confidential
Fast Models Fixed Virtual Platforms Reference Guide	100966	Non-Confidential
Fast Models Reference Guide	100964	Non-Confidential
Fast Models User Guide	100965	Non-Confidential
Fixed Virtual Platforms	-	Non-Confidential
Knowledge Base Articles for FVPs	-	Non-Confidential