

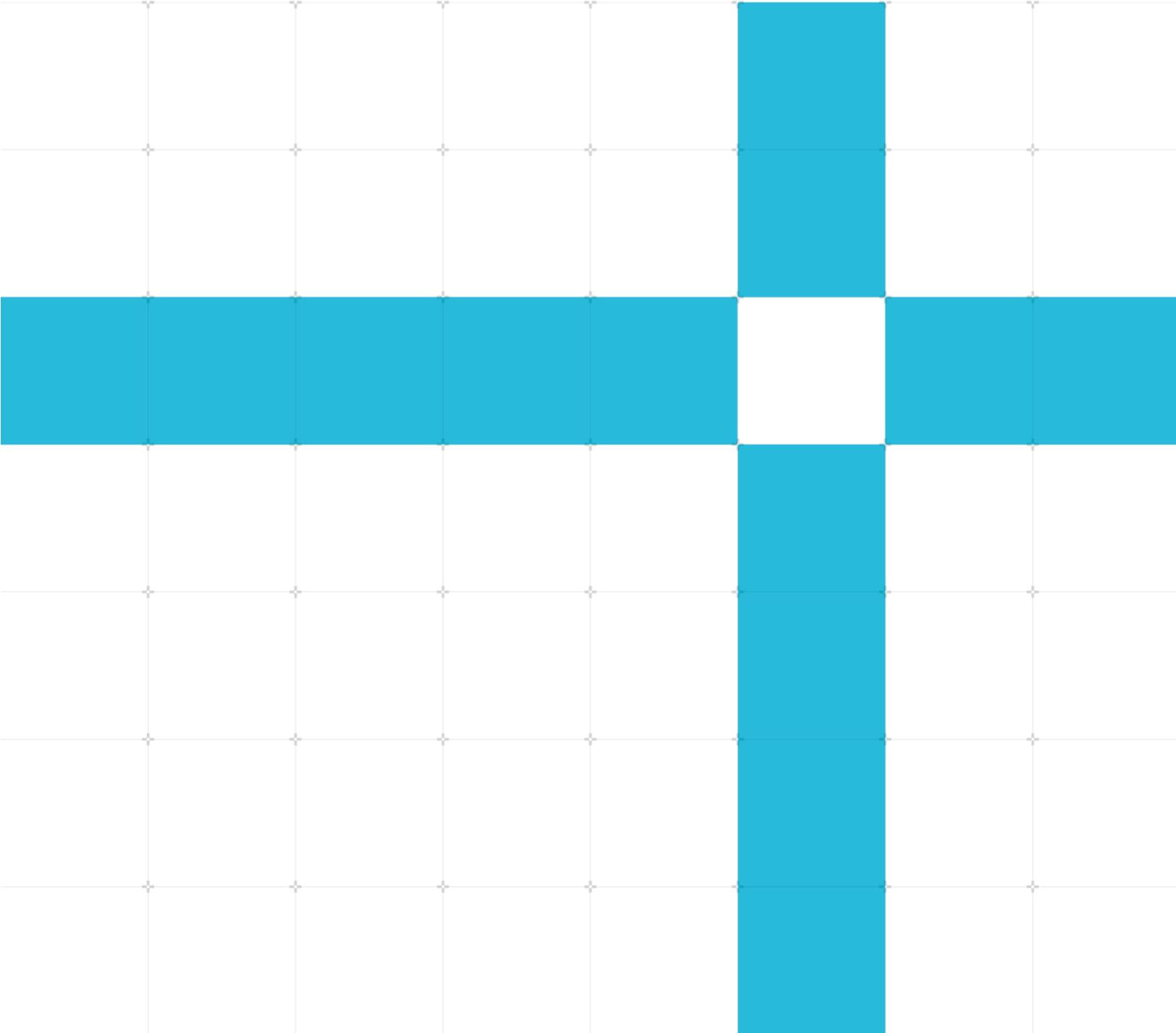


Base Boot Security Requirements

Non-Confidential

Issue 1.4

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Base Boot Security Requirements

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Release information

Document history

Issue	Date	Confidentiality	Change
1.0	06-10-2020	Non-Confidential	Initial release
1.1	10-06-2021	Non-Confidential	Updates <ul style="list-style-type: none"> • Updates to sync with BBR now that it has the base firmware update requirements • Fix error in requirement numbering • Moved the db/dbx variable attributes requirements to the Secure Boot section • For measured boot, made creating the TPM event log an explicit requirement. • Removed reference to the deprecated EFI_VARIABLE_AUTHENTICATED_WRITE_ACCESS attribute • Minor cleanup/clarifications
1.2	09-01-2023	Non-Confidential	Updates <ul style="list-style-type: none"> • Clean up • Add informative security checklist chapter
1.3	12-02-2024	Non-Confidential	Updates <ul style="list-style-type: none"> • Move to new document template • Recommends that the default secure boot variables (PKDefault, KEKDefault, dbDefault, dbxDefault) are implemented • Recommends that the new KEK and UEFI CA certificates issued by Microsoft in 2023 be added to systems • Update the referenced version of the TCG PFP spec to 1.05 • Update the referenced version of the UEFI spec to 2.9 • Add normative language that to clarify that platform reset attack mitigations can be done based on the mechanism described in the TCG specification or the Arm PSCI specification • Relax the lower bound of the maximum variable size for UEFI variables • Recommend that discrete TPM chips be FIFO based if accessed by Non-secure software

Issue	Date	Confidentiality	Change
1.4	07-14-2025	Non-Confidential	Updates <ul style="list-style-type: none"> • Update references section • Update Platform Reset Attack requirements • Clarify hash algorithm requirement to include all active PCR banks • Clarify Secure Boot variable protection rules • Clarify and emphasize PCR[7] measurements • Add requirement about bus-level attacks against TPMs • Clarify that all enabled PCR banks must be used in measured boot • Add rule for firmware update rollback attacks • Make firmware components referenced in R180_BBSR more general than just Secure world. • need to address EV_POSTCODE2 • DRTM requirement for PC-BSA based systems • Clarify that in-band firmware updates are not mandated • Requirement to mitigate DMA attacks • Add TPM implementation requirements • TPM clarification for PC-BSA • Clarify TPM event log space requirement • Clarify what critical data is being referred to R190_BBSR. • Fix typos

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Product Status

The information in this document is Final, that is for a developed product.

Feedback

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Contents

1. Introduction	8
1.1. Conventions.....	8
1.2. References	10
2. Introduction	11
3. Security requirements	12
3.1. Authenticated variables	12
3.2. Secure boot.....	13
3.3. Secure firmware update.....	14
3.4. TPMs and measured boot.....	15
3.5. Platform reset attacks.....	19
3.6. DMA Attacks	20
3.7. DRTM	20
4. Platform security checklist.....	21
4.1. Checklist overview.....	21
4.2. Security scope.....	21
4.3. Resources	22
4.4. Guideline conventions	22
4.5. Secure boot.....	22
4.5.1. Image integrity.....	23
4.5.2. Critical data integrity for secure boot	24
4.5.3. Secure boot hardening.....	25
4.6. Secure firmware update.....	25
4.7. Measured boot.....	26
4.8. Security hardening.....	27

1. Introduction

1.1. Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: <https://developer.arm.com/glossary>.

This document uses the following terms and abbreviations.

Terms and abbreviations

Term	Meaning
Critical data	Critical data includes configuration settings and policies that need to be in a valid state for a device to maintain its security posture during boot and runtime. All other data is non-critical.
Mutable	Changeable with respect to the platform of a system.
Non-host platform	A peripheral or controller in a system that has no DMA protections and cannot be restricted from reading or writing Normal world memory.
Non-secure	Something belonging to the Non-secure privilege levels (Non-secure EL0, EL1, and EL2).
Normal world	The Non-secure privilege levels (Non-secure EL0, EL1, and EL2) and resources, for example memory, registers, and devices, that are not part of the Secure world.
Platform	The set of hardware and firmware mechanisms and services that an operating system and applications can rely on.
Secure world	The environment that is provided by the Secure privilege levels in the Arm v8-A architecture, S-EL0, S-EL1, S-EL2, EL3, and the resources, for example memory, registers, and devices, that are accessible exclusively from the Secure privilege levels.
TCG	Trusted Computing Group
TPM	Trusted Platform Module. A security module that is defined by TCG.

Typographical conventions

Convention	Use
<i>italic</i>	Citations.
bold	Interface elements, such as menu names. Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace bold	Language keywords when used outside example code.
monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <code>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></code>
SMALL CAPITALS	Terms that have specific technical meanings as defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.
 Caution	Recommendations. Not following these recommendations might lead to system failure or damage.
 Warning	Requirements for the system. Not following these requirements might result in system failure or damage.
 Danger	Requirements for the system. Not following these requirements will result in system failure or damage.
 Note	An important piece of information that needs your attention.
 Tip	A useful tip that might make it easier, better, or faster to perform a task.
 Remember	A reminder of something important that relates to the information you are reading.

1.2. References

This document contains information that is specific to this product. See the following resources for other relevant information.

- Arm Non-Confidential documents are available on developer.arm.com/documentation. Each document link in the tables below provides direct access to the online version of the document.
- Arm Confidential documents are available to licensees only through the product package.

Ref	Title	Document number
1.	Arm® Base Boot Requirements 2.1, 2024	DEN0044H
2.	Unified Extensible Firmware Interface Specification. Version 2.11, December 2024	
3.	Arm® Base System Architecture 1.1, 2024	DEN0094D
4.	TCG PC Client Platform Firmware Profile Specification, Family "2.0", Level 00 Revision 1.06, December 4, 2023	-
5.	TCG EFI Protocol Specification, Family "2.0", Version 1.0, Revision 00.13, March 30, 2016	-
6.	TCG ACPI Specification, Family "1.2" and "2.0", Version 1.4, April 3, 2024	-
7.	TCG PC Client Platform Physical Presence Interface Specification, Family "1.2" and "2.0", Version 1.30, July 28, 2015	-
8.	TCG PC Client Platform Reset Attack Mitigation Specification, Family "2.0", Version 1.10, January 21, 2019	-
9.	Platform Security Architecture https://developer.arm.com/architectures/security-architectures/platform-security-architecture	PSA
10.	PSA Certified, https://www.psacertified.org/	PSA Certified
11.	Recommendation for Password-Based Key Derivation Part 1: Storage Applications, December 2010.	NIST SP 800-132
12.	Recommendation for Key Management, NIST Special Publication 800-57 Part1 Rev 5, May 2020.	NIST SP 800-57 Part 1 Rev. 5
13.	Arm® Power State Coordination Interface	DEN0022F.b
14.	Arm® PC Base System Architecture 1.0, 2024	DEN0151
15.	Arm® Dynamic Root of Trust for Measurement 1.1, 2024	DEN0113
16.	TCG PC Client Platform TPM Profile Specification for TPM 2.0, Version 1.06, April 2025	
17.	Arm® TPM Service CRB Interface Over FF-A v1.0, April 2025	DEN0138

2. Introduction

This document specifies security interface requirements and guidance for systems that are compliant with the *Arm® Base Boot Requirements* (BBR) specification [1]. BBR specifies the requirements for boot and runtime services that system software, like operating systems and hypervisors, can rely on. Meeting these requirements enables a compliant operating system image to run on all compliant systems. BBR is based on industry firmware standards like UEFI and ACPI. The focus of BBR is standards-based boot and runtime services, and it does not address security.

This document identifies the platform requirements for BBR-based systems that enable standard, suitably built operating systems to seamlessly use standard security interfaces. These interfaces include the following security related functionality:

- UEFI authenticated variables
- UEFI secure boot
- UEFI secure firmware update using Update Capsules
- TPMs and measured boot

Compliance with this specification provides assurance that the security features in scope are implemented according to standards. However, compliance does not provide assurance that a platform is secure. In the process of architecting a system, you should perform system-level threat modeling to evaluate threats, risks, and mitigations. The Platform Security Architecture (PSA) [9] and the PSA Certified framework [10] provide a comprehensive approach to platform security that is based on defined security goals. PSA provides architecture and requirements specifications for building secure platforms. This specification complements PSA. PSA Certified provides a measure of the robustness of an implementation, through an assessment process that is performed by a security certification laboratory.

3. Security requirements

The sections that follow contain tables with the normative requirements defined by this specification. These requirements are distinct from the supporting informative text which provides the rationale for each requirement.

Any system that is designed to conform to this specification must provide a complete implementation of the requirements in the following sections:

- [Authenticated variables](#) (section 3.1)
- [Secure boot](#) (section 3.2)
- [Secure firmware update](#) (section 3.3)

If the platform implements TPM-based measured boot, the implementation must comply with the requirements in [TPMs and measured boot](#) (section 3.4).

If the platform implements a platform reset attack mitigation, the implementation must comply with the requirements in [Platform reset attacks](#) (section 3.5).

3.1. Authenticated variables

UEFI authenticated variables enable a platform owner to control the setting of critical UEFI settings, such as variables that affect UEFI Secure Boot. Changes to authenticated variables are verified using digital signatures. The changes must be signed by an appropriate private key.

Authenticated variables must be protected from unauthorized modification. Arm recommends that the implementation of the protection of authenticated variables are considered as part of the platform threat model.

Systems must implement support for UEFI authenticated variables as Table 1 specifies.

Table 1, UEFI authenticated variable requirements

ID	Requirement
R010_BBSR	Authenticated variables must be supported and be compliant with the following sections of the UEFI Specification [2]: <ul style="list-style-type: none"> • Globally Defined Variables (section 3.3) • Variable Services (section 8.2)
R040_BBSR	A minimum of 128 KB of non-volatile storage must be available for NV UEFI variables. There is no maximum non-volatile storage limit.
R050_BBSR	The maximum supported variable size must be a least 60 KB.

ID	Requirement
RO60_BBSR	<p>The platform must support EFI variables with any valid combination of the following UEFI variable attributes set:</p> <ul style="list-style-type: none"> • EFI_VARIABLE_NON_VOLATILE • EFI_VARIABLE_BOOTSERVICE_ACCESS • EFI_VARIABLE_RUNTIME_ACCESS • EFI_VARIABLE_APPEND_WRITE • EFI_VARIABLE_TIME_BASED_AUTHENTICATED_WRITE_ACCESS

3.2. Secure boot

Secure boot cryptographically authenticates all firmware that runs on a system. Secure boot requires that all firmware is cryptographically signed. This enables the verification process to detect whether firmware components have been compromised or corrupted.

Secure boot begins in an immutable bootloader component, for example a boot ROM, that loads the first mutable firmware image. Before transferring control to the loaded image, the integrity and authenticity of the image is verified using digital signatures. The boot process continues with each image in the boot chain performing integrity and verification of the next image before that image is executed or used. This process forms a chain of trust that is anchored in the immutable bootloader and continues through all code that is executed up to the runtime environment, for example the OS.

As Figure 1 shows, one portion of the boot chain is UEFI secure boot, where all components loaded by UEFI-compliant firmware are cryptographically verified. UEFI secure boot includes standards for how secure boot keys are managed. UEFI Secure Boot is defined by the UEFI Specification [2].

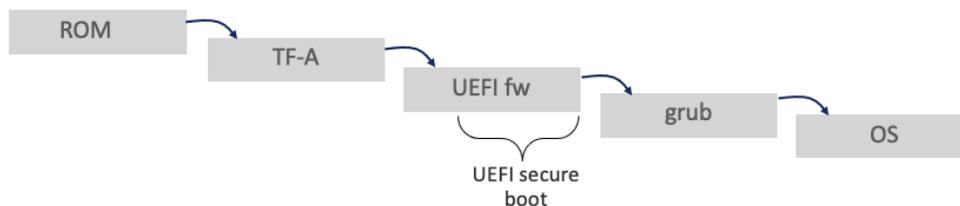


Figure 1, Secure boot chain example

Systems must implement support for UEFI Secure Boot as Table 2 specifies.

Table 2, Secure boot requirements

ID	Requirement
R070_BBSR	System firmware must implement UEFI Secure Boot to prevent unauthorized EFI drivers, option ROMs, or programs from being executed during boot.
R080_BBSR	To support UEFI Secure Boot, the system firmware must be compliant with the following sections of the UEFI Specification: <ul style="list-style-type: none"> • Runtime Services Rules and Restrictions (section 8.1) • Variable Services (section 8.2) • Secure Boot and Driver Signing (section 32)
R085_BBSR	The UEFI Secure Boot variables (PK, KEK, db, dbt, dbx, dbr) must be protected from unauthorized modification. <ul style="list-style-type: none"> • Software tampering: It must not be possible for software to modify the Secure boot variables by bypassing the authorization checks defined by the UEFI specification. • Physical tampering: Physical tampering of the Secure boot variables in non-volatile storage must be detected, including roll-back of the variables.
R020_BBSR	To prevent rollback, the db signature database variable EFI_IMAGE_SECURITY_DATABASE must be created to include the EFI_VARIABLE_TIME_BASED_AUTHENTICATED_WRITE_ACCESS attribute.
R030_BBSR	To prevent rollback, the dbx signature database variable EFI_IMAGE_SECURITY_DATABASE1 must be created to include the EFI_VARIABLE_TIME_BASED_AUTHENTICATED_WRITE_ACCESS attribute to prevent rollback.
R090_BBSR	All UEFI images, for example drivers, applications, boot loaders, that are not contained in the system firmware image must have their signature verified in accordance with Secure Boot UEFI Image Validation in the UEFI Specification section 32.5.
R100_BBSR	System firmware must implement the Secure Boot variable as documented in Globally Defined Variables in the UEFI Specification section 3.3.
R101_BBSR	System firmware should implement the default Secure Boot variables PKDefault, KEKDefault, dbDefault, and dbxDefault as documented in Globally Defined Variables in the UEFI Specification section 3.3. This enables the OEM default key set up to be recovered and audited.
R110_BBSR	If authentication of a component fails, that component must not continue to load or execute.
R120_BBSR	It must not be possible for a user to bypass UEFI Secure Boot failures. A physically present user override is not permitted for images that fail signature verification.

3.3. Secure firmware update

A secure firmware update process ensures that only authorized changes are permitted to the firmware in a system. This process ensures that firmware components maintain their integrity.

Firmware updates could be in-band (controlled by an OS) or out-of-band (for example controlled by a BMC that is trusted to perform updates to the system flash).

The Update Capsule architecture is defined by the UEFI Specification. This architecture provides a flexible mechanism to deliver and apply updates for system firmware components, for example Trusted Firmware-A or UEFI, or firmware for I/O devices in the system.

The Base Boot Requirements (BBR) [1] specification requires that in-band system firmware updates be implemented using UEFI Update Capsules. If in-band firmware update is implemented the following requirements must be implemented:

Table 3, Secure firmware update requirements

ID	Requirement
R130_BBSR	In-band firmware updates must be implemented in accordance with the requirements in BBR: <ul style="list-style-type: none"> • Firmware must implement UEFI update capsules (UEFI specification section 8.5.3) • Firmware must implement the Firmware Management Protocol Data Capsule Structure format (UEFI specification section 23.3). The EFI_FIRMWARE_MANAGEMENT_CAPSULE_IMAGE_HEADER structure must have a Version field value of 2 or greater. • Firmware must implement an ESRT that describes firmware updated in-band (UEFI specification section 23.4)
R140_BBSR	Capsule payloads for updating system firmware must be digitally signed.
R150_BBSR	Before updates to system firmware are applied, images must be verified using digital signatures.
R151_BBSR	The firmware update process must support anti-rollback protection to ensure that the firmware is not being rolled back to an unsupported insecure firmware version.



Prior to the call to UpdateCapsule(), operating systems need to clean the cache by VA to Point of Coherency using the DC CVAC instruction on each ScatterGatherList element that is passed. This is needed only when UpdateCapsule() is called after ExitBootServices(). This requirement will be clarified in a future version of the UEFI specification.



Capsules might be delivered through a file within the EFI system partition, as described in Delivery of Capsules via file on Mass Storage device in the UEFI Specification section 8.5.5.

3.4. TPMs and measured boot

Measured boot shares some common characteristics with secure boot. During the boot flow hashes are computed of all firmware components before use. However, instead of verifying the components using digital signatures, the hashes are securely stored in a TPM. These hashes are referred to as measurements.

A TPM is a security module that provides foundational building blocks for platform security, including:

- Platform Configuration Registers (PCRs) that securely store boot measurements and form the basis for a system to be able to perform secure attestation. PCRs provide one mechanism to implement security policies by sealing TPM objects to PCR values.
- Endorsement key that provides a unique, unclonable identity that is bound to the hardware
- Key storage and management
- Secure cryptography in which keys are never brought into the clear
- Key generation
- True random number generator

A TPM implementation is typically a discrete chip but can also be implemented as a component in a protected environment such as an on-die secure enclave or as a service in the Secure world. System-level threat modeling is required to evaluate potential threats and mitigations to any TPM implementation.

The PC-BSA specification requires that systems provide hardware-enforced protection for TPM locality 4. For discrete TPM chips, a recommended approach is to attach the TPM as a Secure device managed by a service running in a TrustZone-based secure partition. This TPM service acts as a proxy, mediating all access to the TPM and enforcing locality 4 protection. A similar approach can be applied to enclave-based TPM implementations.

Platforms based on the PC-BSA specification [14] must comply with the requirements in Table 4.

Table 4, TPM implementation requirements

ID	Requirement
R160_BBSR	A firmware TPM or TPM service must implement an interface compliant with the Command Response Buffer interface defined in the TCG PC Client Platform TPM Profile Specification for TPM 2.0 [16].
R161_BBSR	A firmware TPM or TPM service must implement a TPM start method compliant with the TCG ACPI specification [6].
R162_BBSR	A TrustZone-based firmware TPM or TPM service should implement the CRB interface and TPM start method in compliance with the Arm TPM Service CRB Interface Over FF-A specification [17].



The Arm Base System Architecture specification [3] specifies that, if a system implements a TPM, it must be compliant with version 2.0 of the TCG specifications. Discrete TPM 2.0 chips can have either a FIFO or CRB interface as defined by TCG. Because of limitations in discrete CRB-based TPMs, discrete TPMs should have a FIFO interface if the TPM is accessible by Non-secure software.

Platforms based on the PC-BSA specification [14] must implement the measured boot requirements in Table 4. For other platforms, if TPM-based measured boot is implemented the implementation must follow the requirements in Table 5.

Table 5, TPM-based measured boot requirements

ID	Requirement
R170_BBSR	Mutable firmware components and security relevant data must be measured into PCR[0] through PCR[7] during boot following the PCR usage guidelines in the TCG PC Client Platform Firmware Profile Specification [4].
R180_BBSR	Mutable firmware components for the Secure world and auxiliary controllers must be measured into PCR[0] through the TPM2_PCR_Extend() command or the H-CRTM interface.
R190_BBSR	Security relevant data that is unsigned must be measured into PCR[1]. Security relevant data that is signed with a digital signature must be measured into PCR[0].
R191_BBSR	Firmware must measure the UEFI Secure boot policy into PCR[7] as specified in the TCG PC Client Platform Firmware Profile Specification [4]. Secure boot policy variables include: PK, KEK, db, dbx, dbt, dbr, dbdev, SecureBoot, AuditMode, DeployedMode.
R200_BBSR	All measurements that are made into TPM PCRs must include a SHA-256 or stronger hashing algorithm.
R201_BBSR	Firmware must make measurement into all enabled TPM PCR banks.
R210_BBSR	All measurements that are made into TPM PCRs must be logged in an event log compliant with the definition in the TCG PC Client Platform Firmware Profile Specification [4].
R211_BBSR	Firmware must allocate (statically or dynamically) sufficient memory for the TPM event log for all uses cases the platform is intended to support. Event log sizing should consider measurements made through the EFI_TCG2_PROTOCOL which come from extensible components that are not part of the firmware itself.
R220_BBSR	For systems that implement system description using ACPI, a TPM 2.0 device must be advertised through ACPI tables, as specified in the TCG ACPI Specification [6]. This enables the TPM to be discovered by an operating system or hypervisor.
R230_BBSR	UEFI firmware must implement the EFI_TCG2_PROTOCOL as defined in the TCG EFI Protocol Specification Family 2.0 [5].
R231_BBSR	It is optional whether a firmware implementation of EFI_TCG2_PROTOCOL.GetCapability() implements backwards compatibility support for 1.0 clients. 1.0 clients assume that EFI_TCG2_BOOT_SERVICE_CAPABILITY fields StructureVersion=1.0 and ProtocolVersion=1.0. If firmware does not support version 1.0 clients, it must return EFI_UNSUPPORTED if the firmware detects a 1.0 sized EFI_TCG2_BOOT_SERVICE_CAPABILITY structure.
R240_BBSR	If physical presence authorization for a TPM is implemented by firmware in a platform, the implementation must follow the requirements in TCG PC Client Platform Physical Presence Interface Specification [7]. The TCG specification describes two methods to provide physical presence authorization: the command method and the hardware method. Either method is acceptable to comply with this specification.
R250_BBSR	A system that implements a discrete TPM should mitigate attacks against the physical bus the TPM is connected to (e.g. interposer or sniffing attacks).



It is acceptable for the first mutable firmware component to measure itself if that component has been cryptographically verified by the immutable bootloader.

As required by the TCG PC Client Platform Firmware Profile Specification [4], firmware components that are measured into PCR[0] must be logged in the event log using the event type EV_POST_CODE2 with event data in a UEFI_PLATFORM_FIRMWARE_BLOB2 structure. Table 6 contains recommended BlobDescription strings for Secure world firmware components. In the following table, %d represents a platform appropriate integer value, and %s represents a platform appropriate string for the component.

Table 6, EV_POST_CODE2 event strings

EV_POST_CODE2 event strings	Component description
SYS_CTRL_%d	For firmware for any kind of auxiliary controller in the SoC
BL_%d	For any bootloader component on the application processor. For example, BL2 in Trusted Firmware-A would be "BL_2".
SECURE_RT_ELO_%s	Secure ELO runtime component
SECURE_RT_EL1_%s	Secure EL1 runtime component
SECURE_RT_EL2	Secure EL2 runtime component
SECURE_RT_EL3	EL3 runtime component. For example, BL31 in Trusted Firmware-A nomenclature.

For measurements of configuration data made by auxiliary controllers or Secure world firmware to PCR[1], the event type used should be EV_TABLE_OF_DEVICES. Table 7 contains recommended ASCII strings for the event data. In Table 7, %d represents a platform appropriate integer value, and %s represents a platform appropriate string for the component.

Table 7, EV_TABLE_OF_DEVICES event data

EV_TABLE_OF_DEVICES event data	Component description
SYS_CONFIG_%s	Configuration measured by any kind of auxiliary controller in the SoC.
BL_%d_CONFIG_%s	Configuration measured by a bootloader component on the application processor.
SECURE_CONFIG_ELO_%s	Configuration measured by Secure ELO runtime component.
SECURE_CONFIG_EL1_%s	Configuration measured by Secure EL1 runtime component.
SECURE_CONFIG_EL2_%s	Configuration measured by Secure EL2 runtime component.
SECURE_CONFIG_EL3_%s	Configuration measured by EL3 runtime component.

3.5. Platform reset attacks

A platform reset attack occurs when an attacker with physical presence causes a system to be unexpectedly rebooted without a clean shutdown of the operating system. The attacker then makes the system boot on an alternate boot device, like a USB drive or DVD, into an OS that is under the control of the attacker. Actions such as resetting the system, power cycling the system, or causing a kernel crash can cause the reboot. A key to the attack succeeding is that the volatile system memory can retain its contents across the attacker-forced reboot. The retention of memory contents can happen even when cycling the system power. After booting into the attacker-controlled OS, the attacker can then scan memory to identify secrets like disk encryption keys.

A mitigation against this attack is defined in TCG PC Client Platform Reset Attack Mitigation Specification [8]. The TCG specification defines two UEFI variables that can be set by an operating system to mitigate the attack. The UEFI MemoryOverwriteRequestControl variable tells the firmware to clear memory prior to booting an operating system. The variable MemoryOverwriteRequestControlLock is a protection flag which prevents MemoryOverwriteRequestControl from being modified.

A mitigation against this attack is also defined in the Arm Power State Coordination Interface (PSCI) specification [13] through the MEM_PROTECT and MEM_PROTECT_CHECK_RANGE functions.

Table 8, Platform reset attack mitigations

ID	Requirement
R301_BBSR	Platforms based on the PC-BSA specification [14] must implement the platform reset attack mitigation (MEM_PROTECT and MEM_PROTECT_CHECK_RANGE) as defined in PSCI [13] or the UEFI variable method (Secure MOR) as defined by TCG [8]. Non-PC-BSA platforms should implement either the UEFI variable method or PSCI method.
R302_BBSR	Platforms that implement DRTM must implement the PSCI (MEM_PROTECT and MEM_PROTECT_CHECK_RANGE) method.
R300_BBSR	If the platform reset attack mitigation is implemented using UEFI variables, it must follow the requirements in UEFI Interface chapter of the TCG PC Client Platform Reset Attack Mitigation Specification, including support for MemoryOverwriteRequestControlLock Variable as described in the UEFI Interface.
R310_BBSR	If the Platform Reset Attack Mitigation is implemented through PSCI, then the implementation must follow the requirements in the Arm Power State Coordination Interface Specification [13].
R320_BBSR	On platforms not based on PC-BSA, when the UEFI MemoryOverwriteRequestControl variable and PSCI memory protection API co-exist, Operating Systems may call any of these interfaces to mitigate the reset attack.

3.6. DMA Attacks

DMA attacks during boot can allow an attacker to compromise the system's Trusted Computing Base (TCB). To mitigate this risk, an SMMU protects against unauthorized memory access by DMA-capable devices. The PC-BSA specification [14] mandates that all DMA requesters be located behind an SMMU. The following requirement requires enabling the SMMU early in the boot process to prevent DMA attacks during system initialization.

Table 9, DRTM Requirements

ID	Requirement
R350_BBSR	Platforms based on the PC-BSA specification [14] must enable DMA protections at the SMMU early enough during boot so that it is not possible for DMA requesters to access system address space except through explicit DMA mappings.

3.7. DRTM

DRTM is a form of TPM measured boot that provides a means to establish a TCB in the Normal world that excludes arbitrarily extensible components. See the DRTM Architecture for Arm [15].

Table 10, DRTM Requirements

ID	Requirement
R360_BBSR	Platforms based on the PC-BSA specification [14] should provide a DRTM implementation. A DRTM implementation must be compliant to the DRTM Architecture for Arm [15].

4. Platform security checklist

4.1. Checklist overview

Section 3, *Security requirements*, of this specification describes the requirements to conform to standard security interfaces for a system based on the Base Boot Requirements (BBR) standard [1]. These security interfaces include: UEFI secure boot, secure firmware update, and TPM-based measured boot. However, compliance to these interface standards does not provide assurance that a platform is secure. The underlying platform must have additional security properties to ensure the integrity of the system's firmware and runtime software. This section provides guidance in the form of a checklist to assist in assessing the security properties of a system that may impact secure boot, secure firmware update, and measured boot.

You can use this checklist alone or in conjunction with a security certification program. One program oriented towards embedded and IoT systems is the Platform Security Architecture (PSA) [9] and the PSA Certified framework [10]. PSA provides a comprehensive approach to platform security that is based on defined set of security goals. PSA provides architecture and requirements specifications for building secure platforms.

For PSA, this checklist can help you complete the PSA Level 1 Device Assessment Questionnaire when a system with BBR-compliant firmware is being PSA certified. The checklist provides specific details about how the requirements in the PSA questionnaire are met. For example, a PSA Level 1 requirement is that a system use secure storage to protect sensitive data. This checklist clarifies that for a BBR-based system, the UEFI secure boot variables are considered sensitive data and must be in tamper-evident storage.

Also, the checklist provides additional hardening requirements that are necessary for a secure system, but go beyond the PSA Level 1 requirements. For checklist items that map to a PSA Level 1 requirement, a cross-reference to the corresponding PSA requirement is provided.

The checklist is informative and is not required for SystemReady Security Interface Extension certification.

4.2. Security scope

The security goal of this checklist is limited to ensuring the integrity of firmware components, critical data, and other components loaded during the boot flow, such as bootloaders. System-level threat modeling is necessary to identify the set of threats a system might face in the wider context of its usage model.

The following threats are in scope for the checklist:

- Attacker tampers with components loaded and executed during boot
- Attacker tampers with firmware configuration data that affects secure boot, such as UEFI variables
- Attacker attempts to update a firmware component with an authentic but out-of-date image that may contain vulnerabilities

- Attacker bypasses image verification failures during secure boot
- DMA attacks against secure boot
- Attacker uses a signed EFI utility, such as the UEFI shell, to subvert the security posture of the system
- Attacker abuses a weak firmware password implementation to get access to firmware configuration

The following are not security goals of this checklist:

- Attacks against the availability of a system
- Glitches of the SoC power supply or clocks during secure boot in order to bypass verification checks
- Laboratory attacks in which devices are unpackaged and probed
- Physical attacks against a TPM, including physical man-in-the-middle attacks

4.3. Resources

The following resources can be useful to users of this checklist:

- Platform Security Boot Guide, v1.1, July 2020, <https://developer.arm.com/documentation/den0072/0101/>
- Platform Security Requirements, v1.0, September 2020, <https://developer.arm.com/documentation/den0106/latest/>
- PSA Certified™ Level 1 Questionnaire, <https://www.pscertified.org/development-resources/certification-resources/>
- U-Booting Securely, Dmitry Janushkevich, F-Secure Hardware Security Team, May 2020

4.4. Guideline conventions

In the guidance sections that follow each normative guideline is identified with an ID and the guidance description. Some guidelines have additional informative information such as examples or cross reference information to the corresponding PSA requirement. For PSA cross references, guidance is provided for how to complete the corresponding checklist item in the PSA Certified checklist.

The informative information is provided in a separate row in the guidance table and is italicized. See the example in Figure 2.

Figure 2, Guideline example

ID	Guideline
G100_BBSR	Systems must implement a secure boot flow that begins in a root of trust for verification.
	<i>For PSA Level 1 C1.2, describe the properties of the root of trust for verification.</i>

4.5. Secure boot

Secure boot is the process by which the integrity of all mutable firmware components in a system is verified before the components are used.

Secure boot is rooted in a root of trust for verification. A root of trust for verification is an immutable location, such as a boot ROM, which cryptographically verifies the first mutable firmware in the system. The verification is done using digital signatures before the mutable firmware is executed. Beginning with the root of trust for verification, each component verifies the next component in the boot chain. The firmware boot chain extends to include verifying the OS bootloader. See the example in Figure 3.

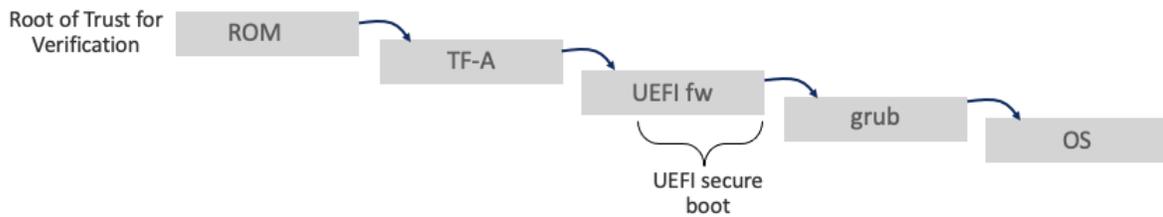


Figure 3, Example secure boot flow

Figure 3 shows the portion of the secure boot chain. UEFI secure boot is a portion of the secure boot chain, as can be seen in Figure 3. The effectiveness of UEFI secure boot depends on the integrity of preceding components in the boot chain, continuing back to the root of trust for verification.

4.5.1. Image integrity

The secure boot process verifies image integrity using digital signatures. Images verified during secure boot may include signed critical data as well as code. Table 11 describes the guidelines for secure boot.

Table 11, Secure boot guidelines

ID	Guideline
G100_BBSR	Systems must implement a secure boot flow that begins in a root of trust for verification. <i>For PSA Level 1 C1.2, describe the properties of the root of trust for verification.</i>
G110_BBSR	The public keys, or hash of the public keys, used by the root of trust for verification must be immutable or tamper resistant. <i>For PSA Level 1 C1.4, describe how the public key used by the root of trust for verification is protected.</i>
G120_BBSR	Each stage in the secure boot chain must verify the next stage image using digital signatures before the next stage firmware image is executed. <i>The firmware-based secure boot chain extends to the Non-secure bootloader. At a system-level the chain of verification may extend further and include the OS.</i> <i>Images loaded using network-based protocols (for example PXE, HTTP, iSCSI) must be verified in the same way as images from local storage devices.</i> <i>For PSA Level 1 C1.2 and D1.1, describe the secure boot chain and how each stage is verified. Note that for PSA the secure boot chain does extend to verifying the OS.</i>

ID	Guideline
G130_BBSR	Secure boot must use hashes and asymmetric keys with at minimum 128-bit security strength. See NIST SP 800-57 [12] for a definition of 128-bit security strength and a list of compliant cryptographic algorithms. <i>For PSA Level 1 C2.4 and S2.3, describe the cryptographic algorithms and key sizes used for secure boot image verification.</i>
G140_BBSR	If network-based protocols are used to load images, Arm strongly recommends that a protocol is used that can authenticate network connections. Cryptography such as asymmetric keys and hashes used must have at least 128-bit security strength. For example, for HTTP Boot, Arm strongly recommends using HTTPS.
G150_BBSR	Secure boot should have rollback detection during image verification to detect authentic but vulnerable images. <i>For PSA Level 1 C2.2, S1.2, and D1.2, describe how rollback detection is implemented.</i>

4.5.2. Critical data integrity for secure boot

In many secure boot architectures there is data, including configuration options and keys, that must be protected from tampering to achieve the security goals of secure boot. For UEFI-based firmware, this includes authenticated variables that enable secure boot and contain verification keys. For U-boot firmware this includes the U-boot environment.

Table 12 gives guidelines for protecting critical data that may affect secure boot.

Table 12, Secure boot critical data integrity

ID	Guideline
G200_BBSR	UEFI authenticated variables must be maintained in tamper-evident secure storage. <i>For example, UEFI secure boot variables must be kept in tamper-evident secure storage, including:</i> SecureBoot PK KEK db dbx dbt dbr <i>Tamper-evident means that it must be possible to detect unauthorized modifications made to the variables in non-volatile storage. The specific tamper-evident or tamper-resistant properties required for a given system are threat model dependent.</i> <i>For PSA Level 1 S2.2 and D4.5, describe how the storage for authenticated variables is protected.</i>
G210_BBSR	UEFI variable storage should be protected against rollback to valid but out of date variable data.
G220_BBSR	Firmware configuration parameters that control the firmware boot flow must be protected. It must be possible to configure a system to protect against unauthorized modifications made to firmware configuration parameters that affect secure boot.

ID	Guideline
	<p><i>For UEFI firmware, how are unauthorized users prevented from disabling secure boot or configuring the firmware to be in Setup Mode?</i></p> <p><i>Are the UEFI firmware configuration menus accessible without a password?</i></p> <p><i>For U-boot based systems describe how the U-boot environment is protected. Is CONFIG_ENV_IS_NOWHERE set?</i></p> <p><i>For PSA Level 1 S2.2, describe how firmware configuration parameters are protected.</i></p>

4.5.3. Secure boot hardening

In addition to image verification and the protection of sensitive data, additional hardening is needed so secure boot cannot be subverted by an attacker. For example, if image verification fails how does the system behave?

Table 13 gives guidelines for hardening secure boot.

Table 13, Secure boot hardening

ID	Guideline
G300_BBSR	<p>If image signature verification fails during secure boot, a recovery process may be initiated, or the boot process must halt in a secure state. A failure in signature verification must not leave the system firmware in a state where it is vulnerable to attack.</p> <p><i>For U-boot based systems, an improperly configured bootcmd variable can result in secure boot failures to fail open, giving an attacker open access to the U-boot command line.</i></p>
G310_BBSR	<p>It must not be possible for a user to interrupt the secure boot process or bypass secure boot failures. A physically present user override is not permitted for images that fail signature verification.</p> <p><i>For U-boot based systems, the bootdelay variable should be configured so that the boot process cannot be interrupted.</i></p>
G320_BBSR	<p>All devices in a system that are DMA capable should be behind an SMMU. This includes both Secure and Non-secure devices. An SMMU provides a means to mitigate DMA attacks from a malicious device.</p> <p>A device may be given unrestricted DMA access if it can be established to be trustworthy through an authentication process such as SPDm.</p> <p>The SMMU should have a default "deny" policy after reset. If this is not possible, firmware must configure the SMMU with a default policy of aborting transactions as early as possible during the boot process, preferably in the root of trust for verification.</p> <p>Note: A system with non-host platforms can comply with this guideline since non-host platforms are considered trustworthy.</p>

4.6. Secure firmware update

A secure firmware update process ensures that only authorized changes are permitted to all Secure and Non-secure firmware images in a system. This process ensures that firmware components maintain their integrity.

Table 14 gives guidelines for both out-of-band or in-band firmware updates. Firmware updates from a BMC are an example of out-of-band updates. Firmware updates from an OS are an example of in-band updates.

Table 14, Secure firmware update

ID	Guideline
G400_BBSR	Firmware update images must be signed with a digital signature that ensures the integrity and authorization of the update, and the update must be verified using digital signatures prior to the update being written to non-volatile storage. <i>For PSA Level 1 C2.1, S1.1, and D1.2, explain how firmware update images are verified.</i>
G410_BBSR	Firmware update must use hashes and asymmetric keys with at least 128-bit security strength. See NIST SP 800-57 [12] for a definition of 128-bit security strength and a list of compliant cryptographic algorithms. <i>For PSA Level 1 C2.4, describe the cryptographic algorithms and key sizes used for signing.</i>
G420_BBSR	The firmware update process must prevent unauthorized rollback of firmware images to older insecure firmware versions. A mechanism may be provided to support authorized rollback for recovery reasons. <i>For PSA Level 1 C2.2, S1.2, and D1.2, describe rollback protection during firmware updates.</i>

4.7. Measured boot

Measured boot shares some common characteristics with secure boot. During the boot flow hashes are computed of all firmware components before use. However, instead of verifying the firmware components using digital signatures, the measurements of the components are securely stored in a TPM device. Also, measurements may be computed of critical data and security relevant system state. The measurements can be later used for attestation or for implementing TPM-based security policies. See PSA Level 1 requirement S4.1.

Table 15 gives the guidelines for measured boot.

Table 15, Measured boot guidelines

ID	Guideline
G500_BBSR	Measured boot must be rooted in a root of trust for measurement (RTM). The RTM makes the initial integrity measurement into the TPM. The RTM may be a single, immutable component such as a boot ROM. Alternatively, the RTM may consist of multiple components in the boot chain where measurements are held in memory before being placed in the TPM. In this case each component must verify the next using digital signatures and the RTM boot chain must be rooted in a root of trust for verification. If a component in the RTM is verified it may measure itself.
G510_BBSR	Each stage in the measured boot chain must measure the next stage firmware before the next stage image is executed. This includes Non-secure firmware images. Other security-critical data and state may be measured.

ID	Guideline
G520_BBSR	Starting with the root of trust for measurement, each stage of boot should extend the measurement made into the TPM. If this is not possible because of system architecture constraints, the measurement may be held in protected memory until the digest value can be extended into the TPM.
	<i>For systems that implement a firmware TPM, it is not possible to extend measurements until the firmware TPM is operational. In this case it is permissible to hold measurements in secure memory until the measurements can be extended.</i>
G530_BBSR	Firmware configuration parameters that control measured boot must be protected. It must not be possible for an unauthorized user to modify firmware configuration parameters that affect measured boot.
	<i>An example of a parameter that may affect measured boot is a firmware option that enables and disables the TPM or measured boot.</i>

4.8. Security hardening

Table 16 gives additional hardening guidance.

Table 16, Hardening guidelines

ID	Guideline
G600_BBSR	Functionality that is not needed for the intended use of the system software shall not be installed, or must be disabled if non-installation is not practical.
	<i>For UEFI firmware, components that are not required to boot the platform must not be signed by a production secure boot certificate. This includes components such as the UEFI shell and utilities for manufacturing, test, and debug.</i>
	<i>For U-boot firmware, commands not needed for the operation of the system should be disabled. For PSA Level 1 S4.2 and D3.3, describe how this requirement is met.</i>
G610_BBSR	If firmware makes use of passwords they should conform with security best practices, in particular, password storage, password length and complexity, and the number of failed authentication attempts. See NIST 800-132, Recommendation for Password-Based Key Derivation Part 1: Storage Applications [11].
	<i>For PSA Level 1 S5.1, S5.2, S5.3, D4.1, and D4.2, describe how this requirement is met.</i>
G620_BBSR	Where default passwords are used, they must be unique per device and must not be easily determined by automated means or obtained from publicly available information.
	<i>For PSA Level 1 S5.2 and D4.2, describe how this requirement is met.</i>