

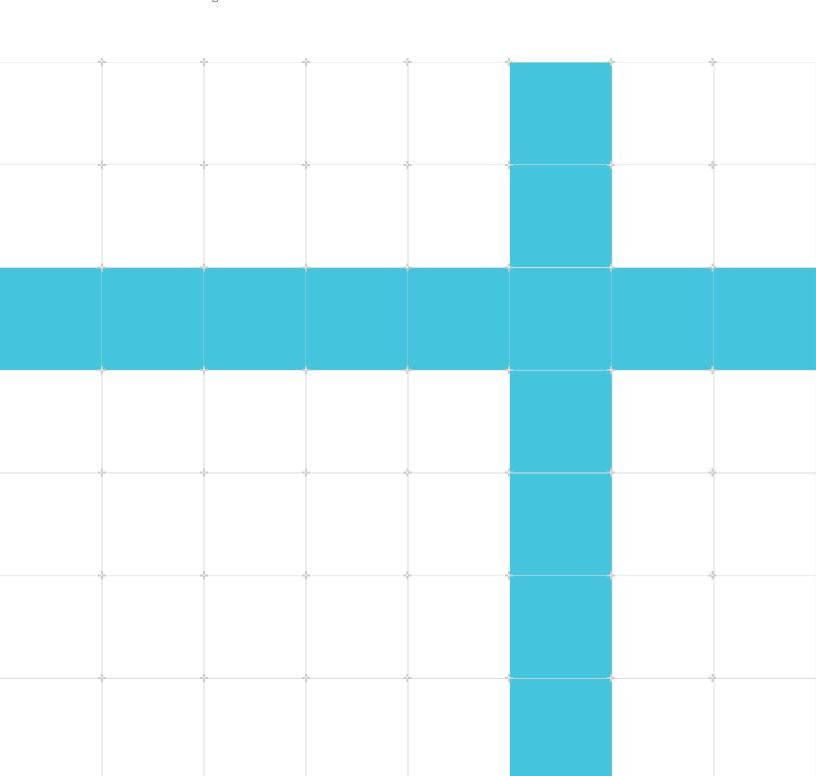
Release notes for the AArch32 Instruction Set **Architecture for Arm A-profile Architecture**

2025-03

Non-Confidential

Issue 01

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Release notes for the AArch32 Instruction Set Architecture for Arm A-profile Architecture

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Release information

Document history

Issue	Date	Confidentiality	Change
2025_03-01	26 March 2025	Non-Confidential	2025-03 release
2024_12-01	17 December 2024	Non-Confidential	2024-12 release
2024_09-01	30 September 2024	Non-Confidential	2023-09 release
2024_06-01	5 July 2024	Non-Confidential	2023-06 release
2024_03-01	27 March 2024	Non-Confidential	2024-03 release
2023_12-01	19 December 2023	Non-Confidential	2023-12 release
2023_09-01	29 September 2023	Non-Confidential	2023-09 release

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Contents

1. Release notes for AArch32 ISA XML for A-profile Architecture (2025-03)

The information relating to the 2024 Extensions is at Alpha quality. Alpha quality means that most major features of the specification are described in this release, but some features and details might be missing. The information relating to the rest of the A-profile Architecture is at Beta quality. Beta quality means that all major features of the specification are described, but some details might be missing.

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Change history

Many simple clarifications and corrections are present, but are too small to be listed here. Some minor formatting changes are suppressed and not highlighted in the diff output.

Known issues

All issues identified in the below list will be fixed in a future release.

- In VAND (immediate) and VORN (immediate), the I16 and I32 type specifiers in the assembly syntax will be corrected.
- There is a mismatch between the encoding for VMOVL and some other instructions and the conditions defined for the groups they appear in. The encoding is correct. The group conditions for affected instructions will be clarified.
- The setting of FPEXC.DEX and FPEXC.TFV bits for an invalid FPSCR.Len and FPSCR.Stride, for an allocated CP10 or CP11 instruction is missing from pseudocode.

Potential Upcoming Changes

The details of the architecture are presented in pseudocode in Architecture Specification Language (ASL). Arm is defining a new version of the Architecture Specification Language, ASL1, to improve and expand the capabilities of the language. Please see https://developer.arm.com/Architectures/Architecture%20Specification%20Language for details on this language. Arm will be publishing an equivalent release in ASL1 format later in 2025.

Intention and quality statements for all ArmARM architecture releases

The intention and scope of the Architecture releases is to describe changes from the existing architecture to the next release. The quality of the architecture releases refers to the accuracy and completeness of the changes described in the specifications.

The intention and scope of the XML releases is to describe the content and behavior of the registers, system registers, instructions, pseudocode and features of the architecture in full, for

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human readers in a way that enables correct information for the current or any previous release can be deduced. The quality of the XML releases refers to the accuracy and completeness of the content to a human reader.

The intention and scope of the JSON releases is to describe aspects of the XML releases in a structured, machine readable format. The content of the architectural content will be approximately equivalent to the corresponding XML release. However there are some aspects of the architecture which cannot yet be represented in a machine readable format.

The intention and scope of the Schema for the JSON releases is to describe the syntax and format of the json files used in the json releases. The schema is still under development and is subject to change.