



Arm[®] Compiler for Embedded

Version 6.23

Migration and Compatibility Guide

Non-Confidential

Copyright © 2019–2024 Arm Limited (or its affiliates).
All rights reserved.

Issue 01

100068_6.23_01_en



Arm® Compiler for Embedded Migration and Compatibility Guide

This document is Non-Confidential.

Copyright © 2019–2024 Arm Limited (or its affiliates). All rights reserved.

This document is protected by copyright and other intellectual property rights.

Arm only permits use of this document if you have reviewed and accepted [Arm's Proprietary Notice](#) found at the end of this document.

This document (100068_6.23_01_en) was issued on 2024-10-16. There might be a later issue at <https://developer.arm.com/documentation/100068>

The product version is 6.23.

See also: [Proprietary notice](#) | [Product and document information](#) | [Useful resources](#)

Start reading

If you prefer, you can skip to [the start of the content](#).

Intended audience

This document is intended for software developers who are currently using Arm® Compiler 5 to build applications and want to use Arm Compiler for Embedded 6. It describes the differences between the two toolchains and the changes that are needed in your C, C++, and assembly source code.

Inclusive language commitment

Arm values inclusive communities. Arm recognizes that we and our industry have used language that can be offensive. Arm strives to lead the industry and create change.

We believe that this document contains no offensive language. To report offensive language in this document, email terms@arm.com.

Feedback

Arm welcomes feedback on this product and its documentation. To provide feedback on the product, create a ticket on <https://support.developer.arm.com>.

To provide feedback on the document, fill the following survey: <https://developer.arm.com/documentation-feedback-survey>.

Contents

1. Configuration and Support Information.....	6
1.1 Support level definitions.....	6
1.2 Compiler configuration information.....	11
2. Migrating from Arm Compiler 5 to Arm Compiler for Embedded 6.....	12
2.1 Migration overview.....	12
2.2 Toolchain differences.....	13
2.3 Default differences.....	14
2.4 Optimization differences.....	18
2.5 Backwards compatibility issues.....	20
2.6 Diagnostic messages.....	20
2.7 Migration example.....	23
3. Migrating from armcc to armclang.....	26
3.1 Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.....	26
3.2 Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior.....	35
3.3 Command-line options for preprocessing assembly source code.....	37
3.4 Inline assembly with Arm Compiler for Embedded 6.....	38
3.5 Migrating architecture and processor names for command-line options.....	41
3.6 Preprocessing a scatter file when linking with armlink.....	46
3.7 Migrating predefined macros.....	46
4. Compiler Source Code Compatibility.....	47
4.1 Language extension compatibility: keywords.....	47
4.2 Language extension compatibility: attributes.....	50
4.3 Language extension compatibility: pragmas.....	54
4.4 Language extension compatibility: intrinsics.....	57
4.5 Diagnostics for pragma compatibility.....	61
4.6 C and C++ implementation compatibility.....	62
4.7 Compatibility of C++ objects.....	65
5. Migrating from armasm to the armclang Integrated Assembler.....	67

5.1 Migration of assembler command-line options from armasm to the armclang integrated assembler.....	67
5.2 Overview of differences between armasm and GNU syntax assembly code.....	72
5.3 Comments.....	74
5.4 Labels.....	75
5.5 Numeric local labels.....	76
5.6 Functions.....	77
5.7 Sections.....	78
5.8 Symbol naming rules.....	80
5.9 Numeric literals.....	81
5.10 Operators.....	82
5.11 Alignment.....	82
5.12 PC-relative addressing.....	83
5.13 Instruction substitutions.....	84
5.14 A32 and T32 pseudo-instructions.....	84
5.15 Conditional directives.....	85
5.16 Data definition directives.....	86
5.17 Instruction set directives.....	88
5.18 Miscellaneous directives.....	89
5.19 Symbol definition directives.....	90
5.20 Migration of armasm macros to integrated assembler macros.....	91
6. Changes Between Different Versions of Arm Compiler for Embedded 6.....	100
6.1 Documentation changes between Arm Compiler for Embedded releases.....	100
6.2 Summary of changes between Arm Compiler for Embedded 6.22 and Arm Compiler for Embedded 6.23.....	101
6.3 Summary of changes between Arm Compiler for Embedded 6.21 and Arm Compiler for Embedded 6.22.....	102
6.4 Summary of changes between Arm Compiler for Embedded 6.20 and Arm Compiler for Embedded 6.21.....	104
6.5 Summary of changes between Arm Compiler for Embedded 6.19 and Arm Compiler for Embedded 6.20.....	105
6.6 Summary of changes between Arm Compiler for Embedded 6.18 and Arm Compiler for Embedded 6.19.....	106
6.7 Summary of changes between Arm Compiler for Embedded 6.17 and Arm Compiler for Embedded 6.18.....	107
6.8 Summary of changes between Arm Compiler 6.16 and Arm Compiler for Embedded 6.17....	108
6.9 Summary of changes between Arm Compiler 6.15 and Arm Compiler 6.16.....	109

6.10 Summary of changes between Arm Compiler 6.14 and Arm Compiler 6.15.....	111
6.11 Summary of changes between Arm Compiler 6.13 and Arm Compiler 6.14.....	111
6.12 Summary of changes between Arm Compiler 6.12 and Arm Compiler 6.13.....	112
6.13 Summary of changes between Arm Compiler 6.11 and Arm Compiler 6.12.....	113
6.14 Summary of changes between Arm Compiler 6.10 and Arm Compiler 6.11.....	115
6.15 Summary of changes between Arm Compiler 6.9 and Arm Compiler 6.10.....	116
6.16 Summary of changes between Arm Compiler 6.8 and Arm Compiler 6.9.....	117
6.17 Summary of changes between Arm Compiler 6.7 and Arm Compiler 6.8.....	118
6.18 Summary of changes between Arm Compiler 6.6 and Arm Compiler 6.7.....	120
6.19 Summary of changes between Arm Compiler 6.5 and Arm Compiler 6.6.....	122
7. Code Examples.....	125
7.1 Example startup code for Arm Compiler 5 project.....	125
7.2 Example startup code for Arm Compiler for Embedded 6 project.....	127
8. Licenses.....	130
8.1 Apache License.....	130
Proprietary notice.....	134
Product and document information.....	136
Product status.....	136
Revision history.....	136
Conventions.....	140
Useful resources.....	142

1. Configuration and Support Information

A summary of the support levels and FlexNet versions supported by the Arm compilation tools.

1.1 Support level definitions

Arm® Compiler for Embedded 6 is built on Clang and LLVM technology. Therefore, it has more functionality than the set of product features described in the documentation.

Arm welcomes feedback regarding the use of all Arm Compiler for Embedded 6 features, and intends to support users to a level that is appropriate for that feature. You can contact support at <https://developer.arm.com/support>.

The following definitions clarify the levels of support and guarantees on functionality that are expected from these features.

Identification in the documentation

All features that are documented in the Arm Compiler for Embedded 6 documentation are product features, except where explicitly stated. The limitations of non-product features are explicitly stated.

Product features

Product features are suitable for use in a production environment. The functionality is well-tested, and is expected to be stable across feature and update releases.

- Arm intends to give advance notice of significant functionality changes to product features.
- If you have a support and maintenance contract, Arm provides full support for use of all product features.
- Arm welcomes feedback on product features.
- Any issues with product features that Arm encounters or is made aware of are considered for fixing in future versions of Arm Compiler for Embedded.

In addition to fully supported product features, some product features are only alpha or beta quality.

Beta product features

Beta product features are implementation complete, but have not been sufficiently tested to be regarded as suitable for use in production environments.

Beta product features are identified with [BETA].

- Arm endeavors to document known limitations on beta product features.
- Beta product features are expected to eventually become product features in a future release of Arm Compiler for Embedded 6.
- Arm encourages the use of beta product features, and welcomes feedback on them.

- Any issues with beta product features that Arm encounters or is made aware of are considered for fixing in future versions of Arm Compiler for Embedded.

Alpha product features

Alpha product features are not implementation complete, and are subject to change in future releases, therefore the stability level is lower than in beta product features.

Alpha product features are identified with [ALPHA].

- Arm endeavors to document known limitations of alpha product features.
- Arm encourages the use of alpha product features, and welcomes feedback on them.
- Any issues with alpha product features that Arm encounters or is made aware of are considered for fixing in future versions of Arm Compiler for Embedded.

Community features

Arm Compiler for Embedded 6 is built on LLVM technology and preserves the functionality of that technology where possible. This means that there are additional features available in Arm Compiler for Embedded that are not listed in the documentation. These additional features are known as community features. For information on these community features, see the [Clang Compiler User's Manual](#).

Where community features are referenced in the documentation, they are identified with [COMMUNITY].

- Arm makes no claims about the quality level or the degree of functionality of these features, except when explicitly stated in this documentation.
- Functionality might change significantly between feature releases.
- Arm makes no guarantees that community features are going to remain functional across update releases, although changes are expected to be unlikely.

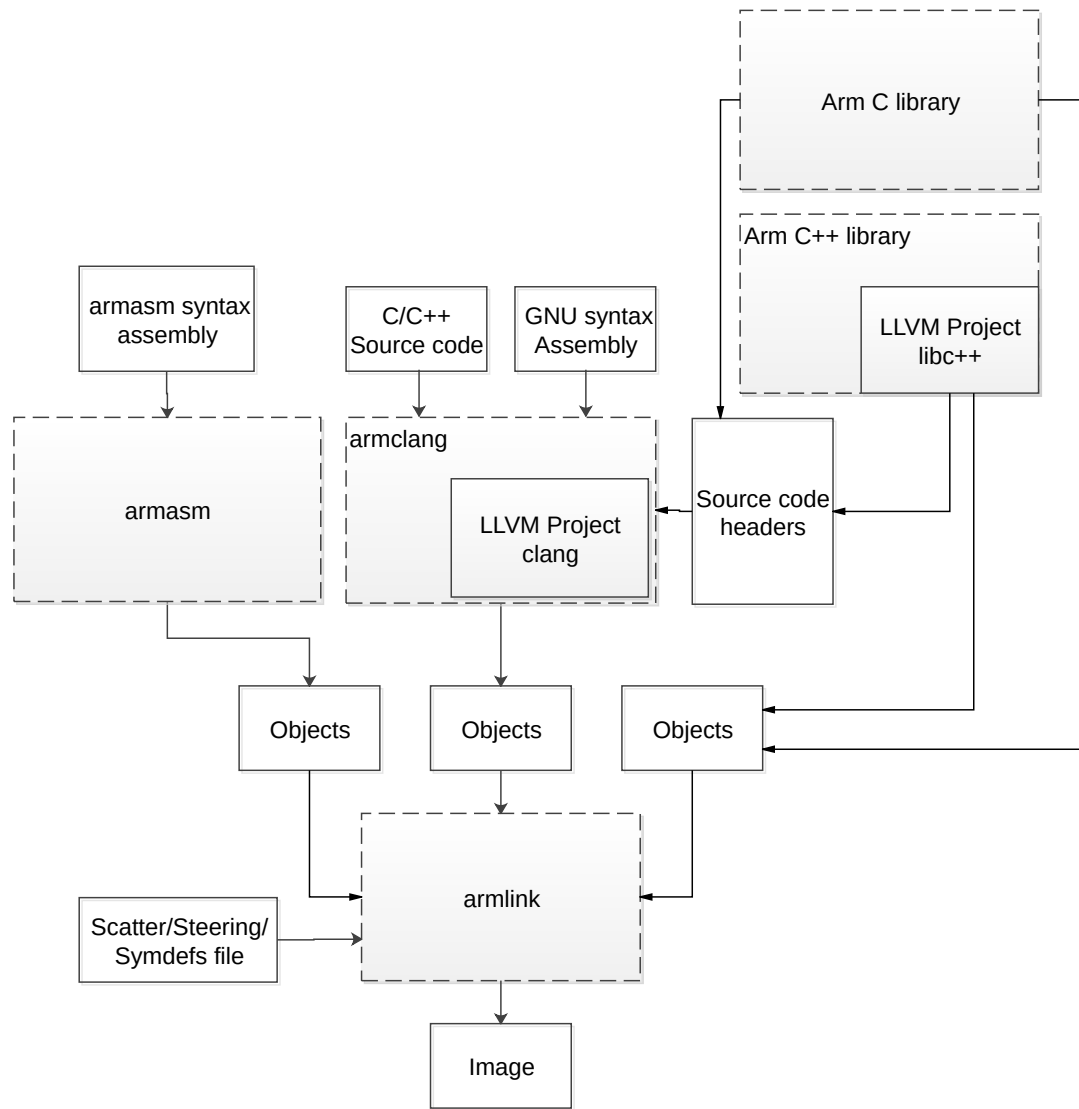
Some community features might become product features in the future, but Arm provides no roadmap for this. Arm is interested in understanding your use of these features, and welcomes feedback on them. Arm supports customers using these features on a best-effort basis, unless the features are unsupported. Arm accepts defect reports on these features, but does not guarantee that these issues are going to be fixed in future releases.

Guidance on use of community features

There are several factors to consider when assessing the likelihood of a community feature being functional:

- The following figure shows the structure of the Arm Compiler for Embedded 6 toolchain:

Figure 1-1: Integration boundaries in Arm Compiler for Embedded 6



The dashed boxes are toolchain components, and any interaction between these components is an integration boundary. Community features that span an integration boundary might have significant limitations in functionality. The exception to this is if the interaction is codified in one of the standards supported by Arm Compiler for Embedded 6. See [Application Binary Interface \(ABI\)](#). Community features that do not span integration boundaries are more likely to work as expected.

- Features primarily used when targeting hosted environments such as Linux or BSD might have significant limitations, or might not be applicable, when targeting bare-metal environments.

- The Clang implementations of compiler features, particularly those that have been present for a long time in other toolchains, are likely to be mature. The functionality of new features, such as support for new language features, is likely to be less mature and therefore more likely to have limited functionality.

Deprecated features

A deprecated feature is one that Arm plans to remove from a future release of Arm Compiler for Embedded. Arm does not make any guarantee regarding the testing or maintenance of deprecated features. Therefore, Arm does not recommend using a feature after it is deprecated.

For information on replacing deprecated features with supported features, see the Arm Compiler for Embedded documentation and Release Notes. Where appropriate, each Arm Compiler document includes notes for features that are deprecated, and also provides entries in the changes appendix of that document.

Unsupported features

With both the product and community feature categories, specific features and use cases are known not to function correctly, or are not intended for use with Arm Compiler for Embedded 6.

Limitations of product features are stated in the documentation. Arm cannot provide an exhaustive list of unsupported features or use cases for community features. The known limitations on community features are listed in [Community features](#).

List of known unsupported features

The following is an incomplete list of unsupported features, and might change over time:

- The Clang option `-stdlib=libstdc++` is not supported.
- `-mabi=aapcs-soft` is not supported for A-profile targets in AArch64 state. The `aapcs-soft` ABI is defined only for Armv8-R AArch64 targets. For more information, see the [Soft-float](#) section of the [Procedure Call Standard for the Arm 64-bit Architecture](#).
- `-mabi=aapcs-soft` is not supported for C++ source language modes.
- C++ static initialization of local variables is not thread-safe when linked against the standard C++ libraries. For thread-safety, you must provide your own implementation of thread-safe functions as described in [Standard C++ library implementation definition](#).



This restriction does not apply to the [ALPHA]-supported multithreaded C++ libraries.

-
- Use of C11 library features is unsupported.
 - Any community feature that is exclusively related to non-Arm architectures is not supported.
 - Except for Armv6-M, compilation for targets that implement architectures lower than Armv7 is not supported.
 - The `long double` data type is not supported for AArch64 state because of limitations in the current Arm C library.

- C complex arithmetic is not supported, because of limitations in the current Arm C library.
- Complex numbers are defined in C++ as a template, `std::complex`. Arm Compiler for Embedded supports `std::complex` with the `float` and `double` types, but not the `long double` type because of limitations in the current Arm C library.



For C code that uses complex numbers, it is not sufficient to recompile with the C++ compiler to make that code work. How you can use complex numbers depends on whether or not you are building for Armv8-M targets.

-
- You must take care when mixing translation units that are compiled with and without the [COMMUNITY] `-fsigned-char` option, and that share interfaces or data structures.



The Arm ABI defines `char` as an unsigned byte, and this is the interpretation used by the C libraries supplied with the Arm compilation tools.

-
- There are limitations with the *Control Flow Integrity* (CFI) sanitizer implementation, `-fsanitize=cfi`, which requires *Link-Time Optimization* (LTO), `-flto`. The following are likely to occur:
 - When using features such as C++ I/O streams, the linker might report errors for a rejected local symbol, `L6654E`, or that a symbol is not preserved by the LTO code generation, `L6137E`.
 - The linker might report a diagnostic that a symbol has a size that extends outside of its containing section, `L6783E` or `L6784E`.

Use the linker option `--diag_suppress 6783` or `--diag_suppress 6784` to suppress the diagnostic.

Alternatives to C complex numbers not being supported

If you are building for Armv8-M targets, consider using the free and open-source CMSIS-DSP library that includes a data type and library functions for complex number support in C. For more information about CMSIS-DSP and complex number support see the following sections of the CMSIS documentation:

- [Complex Math Functions](#)
- [Complex Matrix Multiplication](#)
- [Complex FFT Functions](#)

If you are not building for Armv8-M targets, consider modifying the affected part of your project to use the C++ standard library type `std::complex` instead.

1.2 Compiler configuration information

Summarizes the FlexNet versions supported by the Arm compilation tools.

FlexNet versions in the compilation tools

Different versions of Arm® Compiler for Embedded support different versions of FlexNet.

The FlexNet versions in the compilation tools are:

Table 1-1: FlexNet versions

Compilation tools version	Windows	Linux
Arm Compiler 6.7 and later	11.14.1.0	11.14.1.0
Arm Compiler 6.01 and later	11.12.1.0	11.12.1.0
Arm Compiler 6.00	11.10.1.0	11.10.1.0

Related information

[Arm software product license management](#)

2. Migrating from Arm Compiler 5 to Arm Compiler for Embedded 6

Provides an overview of the differences between Arm® Compiler 5 and Arm Compiler for Embedded 6.

2.1 Migration overview

Migrating from Arm® Compiler 5 to Arm Compiler for Embedded 6 requires the use of new command-line options and might also require changes to existing source files.

Arm Compiler for Embedded 6 is based on the modern LLVM compiler framework. Arm Compiler 5 is not based on the LLVM compiler framework. Therefore migrating your project and source files from Arm Compiler 5 to Arm Compiler for Embedded 6 requires you to be aware of:

- Differences in the command-line options when invoking the compiler.
- Differences in the adherence to language standards.
- Differences in compiler specific keywords, attributes, and pragmas.
- Differences in optimization and diagnostic behavior of the compiler.

Even though these differences exist between Arm Compiler 5 and Arm Compiler for Embedded 6, it is possible to migrate your projects from Arm Compiler 5 to Arm Compiler for Embedded 6 by modifying your command-line arguments and by changing your source code if required.

Arm Compiler 5 does not support processors based on Armv8 and later architectures. Migrating to Arm Compiler for Embedded 6 enables you to generate highly efficient code for processors based on Armv8 and later architectures.

Related information

[Optimization differences](#) on page 18

[Diagnostic messages](#) on page 20

[Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6](#) on page 26

[Compiler Source Code Compatibility](#) on page 47

[Migrating projects from Arm Compiler 5 to Arm Compiler for Embedded 6](#)

2.2 Toolchain differences

Arm® Compiler 5 and Arm Compiler for Embedded 6 share many of the same compilation tools. However, the main difference between the two toolchains is the compiler tool `armclang`, which is based on Clang and LLVM.

The table lists the individual compilation tools and the toolchain they apply to.

Table 2-1: List of compilation tools

Arm Compiler 5	Arm Compiler for Embedded 6	Function
<code>armcc</code>	<code>armclang</code>	Compiles C and C++ language source files, including inline assembly.
<code>armcc</code>	<code>armclang</code>	Preprocessor.
<code>armasm</code>	<code>armasm</code>	Legacy assembler for assembly language source files written in <code>armasm</code> syntax. Use the <code>armclang</code> integrated assembler for all new assembly files.
Not available	<code>armclang</code> . This is also called the <code>armclang</code> integrated assembler.	Assembles assembly language source files written in GNU assembly syntax.
<code>fromelf</code>	<code>fromelf</code>	Converts Arm ELF images to binary formats and can also generate textual information about the input image, such as its disassembly and its code and data size.
<code>armlink</code>	<code>armlink</code>	Combines the contents of one or more object files with selected parts of one or more object libraries to produce an executable program.
<code>armar</code>	<code>armar</code>	Enables sets of ELF object files to be collected together and maintained in archives or libraries.

Arm Compiler for Embedded 6 uses the compiler tool `armclang` instead of `armcc`. The command-line options for `armclang` are different to the command-line options for `armcc`. These differences are described in [Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6](#).

Arm Compiler for Embedded 6 includes the legacy assembler `armasm`, which you can use to assemble your older assembly language source files if they are written in `armasm` syntax. Arm recommends that you write new assembly code using the GNU assembly syntax, which you can assemble using the `armclang` integrated assembler. You can also migrate existing assembly language source files from `armasm` syntax to GNU syntax, and then assemble them using the `armclang` integrated assembler. For more information see [Migrating from `armasm` to the `armclang` Integrated Assembler](#).

Related information

[Migrating projects from Arm Compiler 5 to Arm Compiler for Embedded 6](#)

2.3 Default differences

Some compiler and assembler options are different between Arm® Compiler 5 and Arm Compiler for Embedded 6, or have different default values.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

The following table lists these differences.

Table 2-2: Differences in defaults

Feature	Arm Compiler 5	Arm Compiler for Embedded 6	Notes	Further information
Symbol visibility	--hide_all	-fvisibility=hidden	These defaults are similar but -fvisibility=hidden does not affect extern declarations or symbol references. In Arm Compiler for Embedded 6, symbols in the final image are hidden if the reference or the definition is hidden. Therefore the visibility of the reference alone does not determine the visibility of the symbol, as it does in Arm Compiler 5.	--hide_all for Arm Compiler 5 -fvisibility for Arm Compiler for Embedded 6

Feature	Arm Compiler 5	Arm Compiler for Embedded 6	Notes	Further information
Floating-point linkage	<code>--apcs=/hardfp</code> or <code>--apcs=/softfp</code>	<code>-mfloat-abi=softfp</code>	<p>The default floating-point linkage in Arm Compiler 5 depends on the specified processor. If the processor has floating-point hardware, then Arm Compiler 5 uses hardware floating-point linkage. If the processor does not have floating-point hardware, then Arm Compiler 5 uses software floating-point linkage.</p> <p>In Arm Compiler for Embedded 6, the default is always software floating-point linkage for AArch32 state. For AArch64 state, Arm Compiler for Embedded 6 always uses hardware linkage.</p> <p>For AArch32 state, the <code>-mfloat-abi</code> option also controls the type of floating-point instructions that the compiler uses:</p> <ul style="list-style-type: none"> • <code>-mfloat-abi=softfp</code> uses hardware floating-point instructions and software floating-point linkage. • <code>-mfloat-abi=soft</code> to use software floating-point linkage and software library functions for floating-point operations. • <code>-mfloat-abi=hard</code> uses hardware floating-point instructions and hardware floating-point linkage. 	<p>--apcs (armcc) for Arm Compiler 5</p> <p>-mfloat-abi for Arm Compiler for Embedded 6</p>
Default output file	<code>__image.axf</code>	<code>a.out</code>	Default name for the executable image if none of <code>-o</code> , <code>-c</code> , <code>-E</code> , or <code>-S</code> are specified on the command-line.	<p>-o for Arm Compiler 5</p> <p>-o for Arm Compiler for Embedded 6</p>

Feature	Arm Compiler 5	Arm Compiler for Embedded 6	Notes	Further information
Enumerator size	<code>--enum_is_int</code> is disabled by default	<code>-fno-short-enums</code>	<code>--enum_is_int</code> is disabled by default in Arm Compiler 5, so the smallest data type that can hold the enumerator values is used. <code>-fno-short-enums</code> is the default in Arm Compiler for Embedded 6, so the size of the enumeration type is at least 32 bits.	--enum_is_int for Arm Compiler 5 -fno-short-enums for Arm Compiler for Embedded 6
Optimization level	<code>-O2</code>	<code>-O0</code>	Arm Compiler 5 uses high optimization (<code>-O2</code>) and optimizes for reduced code size (<code>-Ospace</code>) by default, rather than optimizing for performance (<code>-Otime</code>). Arm Compiler for Embedded 6 uses minimum optimization (<code>-O0</code>) by default, and the choice of code size versus performance is controlled by the optimization level.	-Onum for Arm Compiler 5 -Ospace for Arm Compiler 5 -Otime for Arm Compiler 5 -Olevel for Arm Compiler for Embedded 6 Optimization differences.
A32/T32 interwork	<code>--apcs=/nointerwork</code>	<code>--apcs=/interwork</code>	In Arm Compiler 5, <code>armasm</code> does not specify by default that code in the input file can safely interwork between A32 and T32. In Arm Compiler for Embedded 6, <code>armasm</code> specifies interworking by default for AArch32 targets that support A32 and T32 instruction sets.	--apcs (armasm) for Arm Compiler 5 --apcs for Arm Compiler for Embedded 6
Default C++ source language mode	<code>C++03</code>	<code>C++17</code>	In Arm Compiler 5, the default C++ source language mode is <code>C++03</code> . In Arm Compiler for Embedded 6, the default C++ source language mode is <code>C++17</code> . You can override the default source language with <code>-std</code> in Arm Compiler for Embedded 6.	--cpp for Arm Compiler 5 -std for Arm Compiler for Embedded 6

Feature	Arm Compiler 5	Arm Compiler for Embedded 6	Notes	Further information
Default C source language mode	C90	C11 [COMMUNITY]	In Arm Compiler 5, the default C source language mode is C90. In Arm Compiler for Embedded 6, the default C source language mode is C11 [COMMUNITY]. You can override the default source language with <code>-std</code> in Arm Compiler for Embedded 6.	--c90 for Arm Compiler 5 -std for Arm Compiler for Embedded 6
Exception handling	<code>--no_exceptions</code>	<code>-fexceptions</code> or <code>-fno-exceptions</code>	In Arm Compiler 5, C++ exceptions are disabled by default (<code>--no_exceptions</code>). In Arm Compiler for Embedded 6, C++ exceptions are enabled by default (<code>-fexceptions</code>) for C++ sources, or disabled by default (<code>-fno-exceptions</code>) for C sources.	--no_exceptions for Arm Compiler 5 -fexceptions, -fno-exceptions for Arm Compiler for Embedded 6
Wide chars	<code>--wchar16</code>	<code>-fno-short-wchar</code>	In Arm Compiler 5, the size of <code>wchar_t</code> is 2 bytes by default (<code>--wchar16</code>). In Arm Compiler for Embedded 6, the size of <code>wchar_t</code> is 4 bytes by default (<code>-fno-short-wchar</code>).	--wchar16 for Arm Compiler 5 -fno-short-wchar for Arm Compiler for Embedded 6

Feature	Arm Compiler 5	Arm Compiler for Embedded 6	Notes	Further information
Section placement	<code>--split_sections</code> (is disabled by default)	<code>-ffunction-sections</code> (is enabled by default)	<p>In Arm Compiler 5, functions are not put into separate ELF sections by default (<code>--split_sections</code> is disabled).</p> <p>In Arm Compiler for Embedded 6, each function is put into a separate ELF section by default (<code>-ffunction-sections</code> is enabled). Although each function is located in a separate section its associated debug information is not. As a result, when functions are optimized out, the debug information is still part of the executable and might show incorrect debug information. To resolve this situation, use the <code>armlink</code> option <code>--dangling-debug-address</code>.</p>	<p>--split_sections for Arm Compiler 5</p> <p>-ffunction-sections for Arm Compiler for Embedded 6</p> <p>-dangling-debug-address=address for Arm Compiler 6</p> <p>Dealing with dangling debug data for code and data removed by armlink for Arm Compiler 6</p>

2.4 Optimization differences

Arm® Compiler for Embedded 6 provides more performance optimization settings than are present in Arm Compiler 5. However, the optimizations that are performed at each optimization level might differ between the two toolchains.

The table compares the optimization settings and functions in Arm Compiler 5 and Arm Compiler for Embedded 6.

Table 2-3: Optimization settings

Description	Arm Compiler 5	Arm Compiler for Embedded 6	Notes
Optimization levels for performance.	<ul style="list-style-type: none"> • <code>-Otime -O0</code> • <code>-Otime -O1</code> • <code>-Otime -O2</code> • <code>-Otime -O3</code> 	<ul style="list-style-type: none"> • <code>-O0</code> • <code>-O1</code> • <code>-O2</code> • <code>-O3</code> • <code>-Ofast</code> • <code>-Omax</code> 	<p>The Arm Compiler 5 <code>-O0</code> option is more similar to the Arm Compiler for Embedded 6 <code>-O1</code> option than the Arm Compiler for Embedded 6 <code>-O0</code> option.</p> <p>The Arm Compiler for Embedded 6 <code>-Omax</code> option refers to maximum performance, with <i>Link-Time Optimization (LTO)</i> enabled.</p>
Optimization levels for code size.	<ul style="list-style-type: none"> • <code>-Ospace -O0</code> • <code>-Ospace -O1</code> • <code>-Ospace -O2</code> • <code>-Ospace -O3</code> 	<ul style="list-style-type: none"> • <code>-Os</code> • <code>-Oz</code> • <code>-Omin</code> 	<p>The Arm Compiler 5 <code>-O0</code> option is more similar to the Arm Compiler for Embedded 6 <code>-O1</code> option than the Arm Compiler for Embedded 6 <code>-O0</code> option.</p> <p>The Arm Compiler for Embedded 6 <code>-Omin</code> option refers to minimum code size, with LTO enabled..</p>
Default.	<code>-Ospace -O2</code>	<code>-O0</code>	-
Best trade-off between image size, performance, and debug.	<code>-Ospace -O2</code>	<code>-O1</code>	-
Highest optimization for performance.	<code>-Otime -O3</code>	<ul style="list-style-type: none"> • <code>-Omax</code> • <code>-Ofast</code> 	The <code>-Omax</code> option uses LTO. If LTO is not appropriate for you, use <code>-Ofast</code> .
Highest optimization for code size.	<code>-Ospace -O3</code>	<ul style="list-style-type: none"> • <code>-Omin</code> • <code>-Oz</code> 	The <code>-Omin</code> option uses LTO. If LTO is not appropriate for you, use <code>-Oz</code> .

Arm Compiler for Embedded 6 provides an aggressive performance optimization option, `-Omax`, which automatically enables a feature called Link-Time Optimization. For more information, see [-flt0](#).

At the opposite end of the spectrum, the `-Omin` option in Arm Compiler for Embedded 6 is an aggressive code size optimization setting. This also enables Link-Time Optimization and aggressively removes unused code and data.

When using `-Omax` or `-Omin`, `armclang` can perform link-time optimizations that were not possible in Arm Compiler 5. In some cases these link-time optimizations can expose latent bugs in a program, which manifest as an image with different or unanticipated behavior. Therefore, an image built with Arm Compiler 5 might have a different behavior to the image built with Arm Compiler for Embedded 6.

For example, unused variables without the `volatile` keyword might be removed when using `-Omax` or `-Omin` in Arm Compiler for Embedded 6. If the unused variable is actually a `volatile` variable that requires the `volatile` keyword, then the removal of the variable can cause the generated image to behave unexpectedly. Since Arm Compiler 5 does not have these aggressive

optimization settings, it might not have removed the unused variable, and the resulting image might behave as expected, and therefore the error in the code would be more difficult to detect.

Related information

[-flto armclang option](#)

[-O armclang option](#)

[Effect of the volatile keyword on compiler optimization](#)

[Optimizing across modules with Link-Time Optimization](#)

2.5 Backwards compatibility issues

Some Arm® Compiler 5 options produce objects that are not compatible with Arm Compiler for Embedded 6.

SHF_COMDEF ELF sections

Linking with legacy objects that contain ELF sections with the legacy `SHF_COMDEF` ELF section flag is deprecated. Use the `GRP_COMDAT` ELF section group instead of the legacy `SHF_COMDEF` ELF section flag by:

- Replacing the `COMDEF` section attribute of the legacy `armasm` syntax `AREA` directive with the `COMGROUP=<symbol_name>` section attribute.
- Rebuilding incompatible legacy objects using one of the following:
 - Arm Compiler 5 but with the `--dwarf3` option. Other incompatibilities might still exist.
 - Arm Compiler for Embedded 6.

Related information

[AREA directive](#)

[--dwarf3](#)

2.6 Diagnostic messages

In general, `armclang` provides more precise and detailed diagnostic messages compared to `armcc`. Therefore you can expect to see more information about your code when using Arm® Compiler for Embedded 6, which can help you understand and fix your source more quickly.

`armclang` and `armcc` differ in the quality of diagnostic information they provide about your code. The following sections demonstrate some of the differences.

Assignment in condition

The following code is an example of `armclang` providing more precise information about your code. The error in this example is that the assignment operator, `=`, must be changed to the equality operator, `==`.

```
//main.cpp:
#include <stdio.h>

int main()
{
    int a = 0, b = 0;
    if (a = b)
    {
        printf("Right\n");
    }
    else
    {
        printf("Wrong\n");
    }
    return 0;
}
```

Compiling this example with Arm Compiler 5 gives the message:

```
"main.cpp", line 6: Warning: #1293-D: assignment in condition
if (a = b)
   ^
```

Compiling this example with Arm Compiler for Embedded 6 gives the message:

```
main.cpp:6:7: warning: using the result of an assignment as a condition without
parentheses[-Wparentheses]
if (a = b)
   ~^~

main.cpp:6:7: note: place parentheses around the assignment to silence this warning
if (a = b)
   ^
   ( )

main.cpp:6:7: note: use '==' to turn this assignment into an equality comparison
if (a = b)
   ^
   ==
```

`armclang` highlights the error in the code, and also suggests two different ways to resolve the error. The warning messages highlight the specific part which requires attention from the user.



When using `armclang`, it is possible to enable or disable specific warning messages. In the example above, you can enable this warning message using the `-Wparentheses` option, or disable it using the `-Wno-parentheses` option.

Automatic macro expansion

Another very useful feature of diagnostic messages in Arm Compiler for Embedded 6, is the inclusion of notes about macro expansion. These notes provide useful context to help you understand diagnostic messages resulting from automatic macro expansion.

Consider the following code:

```
//main.cpp:

#include <stdio.h>

#define LOG(PREFIX, MESSAGE) fprintf(stderr, "%s: %s", PREFIX, MESSAGE)
#define LOG_WARNING(MESSAGE) LOG("Warning", MESSAGE)

int main(void)
{
    LOG_WARNING(123);
}
```

The macro `LOG_WARNING` has been called with an integer argument. However, expanding the two macros, you can see that the `fprintf` function expects a string. When the macros are close together in the code it is easy to spot these errors. These errors are not easy to spot if they are defined in different part of the source code, or in other external libraries.

Compiling this example with Arm Compiler 5 `armcc main.cpp` reports the message:

```
main.cpp", line 8: Warning:  #181-D: argument is incompatible with corresponding
format string conversion

    LOG_WARNING(123);
    ^
```

Compiling this example with Arm Compiler for Embedded 6 `armclang --target=arm-arm-none-eabi -march=armv8-a` reports the message:

```
main.cpp:8:14: warning: format specifies type 'char *' but the argument has type
'int' [-Wformat]

    LOG_WARNING(123);
    ~~~~~^~~

main.cpp:4:45: note: expanded from macro 'LOG_WARNING'
#define LOG_WARNING(MESSAGE) LOG("Warning", MESSAGE)
                               ~~~~~^~~~~~

main.cpp:3:64: note: expanded from macro 'LOG'
#define LOG(PREFIX, MESSAGE) fprintf(stderr, "%s: %s", PREFIX, MESSAGE)
                                           ~~~~^~~~~~
```

For more information, see [Diagnostics for pragma compatibility](#).

**Note**

When starting the migration from Arm Compiler 5 to Arm Compiler for Embedded 6, you can expect additional diagnostic messages because `armclang` does not recognize some of the pragmas, keywords, and attributes that were specific to `armcc`. When you replace the pragmas, keywords, and attributes from Arm Compiler 5 with their Arm Compiler for Embedded 6 equivalents, the majority of these diagnostic messages disappear. You might require additional code changes if there is no direct equivalent for Arm Compiler for Embedded 6. For more information see [Compiler Source Code Compatibility](#).

2.7 Migration example

This topic shows you the process of migrating an example code from Arm® Compiler 5 to Arm Compiler for Embedded 6.

**Note**

This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

Compiling with Arm Compiler 5

For an example startup code that builds with Arm Compiler 5, see [Example startup code for Arm Compiler 5 project](#).

To compile this example with Arm Compiler 5, enter:

```
armcc startup_ac5.c --cpu=7-A -c
```

This command generates a compiled object file for the Armv7-A architecture.

Compiling with Arm Compiler for Embedded 6

Try to compile the `startup_ac5.c` example with Arm Compiler for Embedded 6. The first step in the migration is to use the new compiler tool, `armclang`, and use the correct command-line options for `armclang`.

To compile this example with Arm Compiler for Embedded 6, enter:

```
armclang --target=arm-arm-none-eabi startup_ac5.c -march=armv7-a -c -O1 -std=c90
```

The following table shows the differences in the command-line options between Arm Compiler 5 and Arm Compiler for Embedded 6:

Table 2-4: Command-line changes

Description	Arm Compiler 5	Arm Compiler for Embedded 6
Tool	armcc	armclang
Specifying an architecture	--cpu=7-A	<ul style="list-style-type: none"> -march=armv7-a --target is a mandatory option for armclang. <p>To generate A64 instructions for AArch64 state, specify --target=aarch64-arm-none-eabi. To generate A32 / T32 instructions for AArch32 state, specify --target=arm-arm-none-eabi (you must also specify -mthumb for T32 instructions).</p> <p>Specify either an architecture (-march) or processor (-mcpu), but not both.</p>
Optimization	The default optimization is -O2.	The default optimization is -O0. To get similar optimizations as the Arm Compiler 5 default, use -O1.
Source language mode	The default source language mode for .c files is c90.	The default source language mode for .c files is gnu11 [COMMUNITY]. To compile for c90 in Arm Compiler for Embedded 6, use -std=c90.

Arm Compiler for Embedded 6 generates the following errors and warnings when trying to compile the example `startup_ac5.c` file in c90 mode:

```

startup_ac5.c:39:22: error: 'main' must return 'int'
__declspec(noreturn) void main (void)
                        ^~~~
                        int
startup_ac5.c:45:9: error: '#pragma import' is an ARM Compiler 5 extension, and is
not supported by ARM Compiler 6 [-Warmcc-pragma-import]
#pragma import (__use_no_semihosting)
^
startup_ac5.c:60:7: error: expected '(' after 'asm'
__asm void Vectors(void) {
^
startup_ac5.c:60:6: error: expected ';' after top-level asm block
__asm void Vectors(void) {
^
;
startup_ac5.c:61:3: error: use of undeclared identifier 'IMPORT'
IMPORT Undef_Handler
^
startup_ac5.c:80:7: error: expected '(' after 'asm'
__asm void Reset_Handler(void) {
^
startup_ac5.c:80:6: error: expected ';' after top-level asm block
__asm void Reset_Handler(void) {
^
;
startup_ac5.c:83:3: error: use of undeclared identifier 'CPSID'
CPSID if
^
8 errors generated.

```

The following section describes how to modify the source file to fix these errors and warnings.

Modifying the source code for Arm Compiler for Embedded 6

You must make the following changes to the source code to compile with `armclang`.

- The return type of function `main` cannot be `void` in standard C. Replace the following line:

```
__declspec(noreturn) void main(void)
```

With:

```
__declspec(noreturn) int main(void)
```

- The intrinsic `__enable_irq()` is not supported in Arm Compiler for Embedded 6. You must replace the intrinsic with an inline assembler equivalent. Replace the following line:

```
__enable_irq();
```

With:

```
__asm("CPSIE i");
```

- The `#pragma import` is not supported in Arm Compiler for Embedded 6. You must replace the pragma with an equivalent directive using inline assembler. Replace the following line:

```
#pragma import(__use_no_semihosting)
```

With:

```
__asm(".global __use_no_semihosting");
```

- In certain situations, `armclang` might remove infinite loops that do not have side-effects. You must use the `volatile` keyword to tell `armclang` not to remove such code. Replace the following line:

```
while(1);
```

With:

```
while(1) __asm volatile("");
```

3. Migrating from armcc to armclang

Compares Arm® Compiler for Embedded 6 command-line options to older versions of Arm Compiler.

3.1 Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6

Arm® Compiler for Embedded 6 provides many command-line options, including most Clang command-line options and several Arm-specific options.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

The following table describes the most common Arm Compiler 5 command-line options, and shows the equivalent options for Arm Compiler for Embedded 6.

More information about command-line options is available:

- The *Arm Compiler for Embedded Reference Guide* provides more information about the supported command-line options. The options described are fully supported, unless the level of support is indicated.
- For a full list of Clang command-line options, see the Clang and LLVM documentation.

Table 3-1: Comparison of compiler command-line options in Arm Compiler 5 and Arm Compiler for Embedded 6

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
--allow_fpreg_for_nonfpdata, --no_ allow_fpreg_for_nonfpdata	-mimplicit-float, -mno-implicit-float [COMMUNITY]	Enables or disables the use of VFP and SIMD registers and data transfer instructions for non-VFP and non-SIMD data.
--apcs=/nointerwork	No equivalent.	Disables interworking between A32 and T32 code. Interworking is always enabled in Arm Compiler for Embedded 6.
--apcs=/ropi --apcs=/noropi	-fropi -fno-ropi	Enables or disables the generation of <i>Read-Only Position Independent</i> (ROPI) code.
--apcs=/rwpi --apcs=/norwpi	-frwpi -fno-rwpi	Enables or disables the generation of <i>Read/Write Position Independent</i> (RWPI) code.
--arm	-marm	Targets the A32 instruction set. The compiler is permitted to generate both A32 and T32 code, but recognizes that A32 code is preferred.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
<code>--arm_only</code>	No equivalent.	Enforces A32 instructions only. The compiler does not generate T32 instructions.
<code>--asm</code>	<code>-save-temps</code>	Instructs the compiler to generate intermediate assembly files as well as object files.
<code>--bigend</code>	<code>-mbig-endian</code>	Generates code for big-endian data.
<code>--branch_tables, --no_branch_tables</code>	No equivalent.	<code>-fno-jump-tables</code> is the closest option [COMMUNITY]
<code>-c</code>	<code>-c</code>	Performs the compilation step, but not the link step.
<code>--c90</code>	<code>-xc -std=c90</code>	Enables the compilation of C90 source code. <code>-xc</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.
<code>--c90 --gnu</code>	<code>-xc -std=gnu90</code>	Enables the compilation of C90 source code with additional GNU extensions. <code>-xc</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.
<code>--c99</code>	<code>-xc -std=c99</code>	Enables the compilation of C99 source code. <code>-xc</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.
<code>--c99 --gnu</code>	<code>-xc -std=gnu99</code>	Enables the compilation of C99 source code with additional GNU extensions. <code>-xc</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.
<code>--cpp</code>	<code>-xc++ -std=c++03</code>	Enables the compilation of C++03 source code. <code>-xc++</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension. The default C++ language standard is different between Arm Compiler 5 and Arm Compiler for Embedded 6.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
<code>--cpp --gnu</code>	<code>-xc++ -std=gnu++03</code>	<p>Enables the compilation of C++03 source code with additional GNU extensions.</p> <p><code>-xc++</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.</p> <p>The default C++ language standard is different between Arm Compiler 5 and Arm Compiler for Embedded 6.</p>
<code>--cpp11</code>	<code>-xc++ -std=c++11</code>	<p>Enables the compilation of C++11 source code.</p> <p><code>-xc++</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.</p> <p>The default C++ language standard is different between Arm Compiler 5 and Arm Compiler for Embedded 6.</p>
<code>--cpp11 --gnu</code>	<code>-xc++ -std=gnu++11</code>	<p>Enables the compilation of C++11 source code with additional GNU extensions.</p> <p><code>-xc++</code> is a positional argument and only affects subsequent input files on the command-line. It is also only required if the input files do not have the appropriate file extension.</p> <p>The default C++ language standard is different between Arm Compiler 5 and Arm Compiler for Embedded 6.</p>
<code>--cpp_compat</code>	No equivalent.	Compiles C++ code to maximize binary compatibility.
<code>--cpu=8-A.32</code>	<code>--target=arm-arm-none-eabi -march=armv8-a</code>	Targets Armv8-A and AArch32 state.
<code>--cpu 8-A.64</code>	<code>--target=aarch64-arm-none-eabi</code>	Targets Armv8-A and AArch64 state. (Implies <code>-march=armv8-a</code> if <code>-mcpu</code> is not specified.)
<code>--cpu=7-A</code>	<code>--target=arm-arm-none-eabi -march=armv7-a</code>	Targets the Armv7-A architecture.
<code>--cpu=Cortex-M4</code>	<code>--target=arm-arm-none-eabi -mcpu=cortex-m4</code>	Targets the Cortex®-M4 processor.
<code>--cpu=Cortex-A15</code>	<code>--target=arm-arm-none-eabi -mcpu=cortex-a15</code>	Targets the Cortex-A15 processor.
<code>-D</code>	<code>-D</code>	Defines a preprocessing macro.
<code>--depend</code>	<code>-MF</code>	Specifies a filename for the makefile dependency rules.
<code>--depend_dir</code>	No equivalent. Use <code>-MF</code> to specify each dependency file individually.	Specifies the directory for dependency output files.
<code>--depend_format=unix_escaped</code>	-	Dependency file entries use UNIX-style path separators and escapes spaces with <code>\\</code> . This is the default in Arm Compiler for Embedded 6.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
--depend_system_headers, --no_depend_system_headers	No direct equivalent to the standalone command-line option. However, see the Arm Compiler 5 entries in this table for --md, --md --no_depend_system_headers, and --mm.	Enables and disables the output of system include dependency lines when generating makefile dependency information using either the -M option or the --md option.
--depend_target	-MT	Changes the target name for the makefile dependency rule.
--diag_error	-Werror	Turn compiler warnings into errors.
--diag_style=<string>	No equivalent.	armclang produces diagnostic messages in the following format: <source-file>:<line-number>:<char-number>: <description> [<diagnostic-flag>]
--diag_suppress=<code>	-Wno-<flag>	Suppress warning message <flag>. The error or warning codes might be different between Arm Compiler 5 and Arm Compiler for Embedded 6.
--dollar --no_dollar	-Wno-dollar-in-identifier-extension -Werror=dollar-in-identifier-extension	Disable or enable error messages if the dollar character \$ is used in identifiers. By default Arm Compiler for Embedded 6 does not give an error if \$ is used. However, if you are using the -pedantic-errors option, this generates an error if \$ is used. In this case, use both the -pedantic-errors and -Wno-dollar-in-identifier-extension options to suppress the error. If you are not using the -pedantic-errors option, use -Werror=dollar-in-identifier-extension to generate errors.
-E	-E	Executes only the preprocessor step.
--enum_is_int	-fno-short-enums, -fshort-enums	Sets the minimum size of an enumeration type. By default Arm Compiler 5 does not set a minimum size. By default Arm Compiler for Embedded 6 uses -fno-short-enums to set the minimum size to 32-bit.
--feedback	No equivalent.	Linker feedback is not supported by Arm Compiler for Embedded 6. Arm Compiler for Embedded 6 supports <i>Link-Time Optimization</i> (LTO) with the armclang option -flto, which you use in conjunction with the linker option -lto. For more information, see Optimizing across modules with Link-Time Optimization and -flto, -fno-lto.
--float_literal_pools, --no_float_literal_pools	No equivalent.	The way that literals are merged is handled differently in Arm Compiler for Embedded 6 compared to Arm Compiler 5. For more information, see Literal pool options in armclang .
--forceline	No equivalent.	Forces aggressive inlining of functions. Arm Compiler for Embedded 6 automatically decides whether to inline functions depending on the optimization level.
--fpmode=std	-ffp-mode=std	Provides IEEE-compliant code with no IEEE exceptions, NaNs, and Infinities. Denormals are sign preserving. This is the default.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
<code>--fpmode=fast</code>	<code>-ffp-mode=fast</code>	Similar to the default behavior, but also performs aggressive floating-point optimizations and therefore it is not IEEE-compliant.
<code>--fpmode=ieee_full</code>	<code>-ffp-mode=full</code>	Provides full IEEE support, including exceptions. If you are using NaN or infinity, set <code>-ffp-mode=full</code> . For more information, see -ffp-mode .
<code>--fpmode=ieee_fixed</code> <code>--fpmode=ieee_no_fenv</code>	There are no supported equivalent options.	There might be community features that provide these IEEE floating-point modes.
<code>--fpu</code> For example, <code>--fpu=fpv5_d16</code>	<code>-mfpu</code> For example, <code>-mfpu=fpv5-d16</code>	Specifies the target FPU architecture. Note: <code>--fpu=none</code> checks the source code for floating-point operations, and if any are found it produces an error. <code>-mfpu=none</code> prevents the compiler from using hardware-based floating-point functions. If the compiler encounters floating-point types in the source code, it uses software-based floating-point library functions. The option values might be different. For example <code>fpv5_d16</code> in Arm Compiler 5 is equivalent to <code>fpv5-d16</code> in Arm Compiler for Embedded 6, and targets the FPU5-D16 floating-point extension.
<code>--global_reg=<reg_name></code>	<code>-ffixed-r<N></code>	Prevents the compiler from using the specified core register, unless the use is required for Arm ABI compliance. In Arm Compiler 5, <code><reg_name></code> is an integer starting from 1 to 8, which maps to registers R4 to R11. In Arm Compiler for Embedded 6, <code><N></code> is an integer starting from 6 to 11, which maps to registers R6 to R11.
<code>--gnu_instrument,</code> <code>--no_gnu_instrument</code>	<code>-finstrument-functions</code> [COMMUNITY]	Inserts instrumentation calls for profiling entry and exit to functions.
<code>-I</code>	<code>-I</code>	Adds the specified directories to the list of places that are searched to find included files.
<code>--ignore_missing_headers</code>	<code>-MG</code>	Prints dependency lines for header files even if the header files are missing.
<code>--inline</code>	Default at all optimization levels except <code>-O0</code> .	There is no equivalent of the <code>--inline</code> option. Arm Compiler for Embedded 6 automatically decides whether to inline functions at all optimization levels except at <code>-O0</code> . However, the threshold at which the compiler decides to inline depends on the level.
<code>--integer_literal_pools,</code> <code>--no_integer_literal_pools</code>	No equivalent.	The way that literals are merged is handled differently in Arm Compiler for Embedded 6 compared to Arm Compiler 5. For more information, see Literal pool options in armclang .
<code>-J</code>	<code>-isystem</code>	Adds the specified directories to the list of places that are searched to find included system header files.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
-L	-Xlinker	Specifies command-line options to pass to the linker when a link step is being performed after compilation.
--library_interface=armcc	This is the default.	Arm Compiler for Embedded 6 by default uses the Arm standard C library.
--library_interface=<lib> Where <lib> is one of: <ul style="list-style-type: none"> aeabi_clib aeabi_clib90 aeabi_clib99 	-nostdlib -nostdlibinc -fno-builtin	Specifies that the compiler output works with any ISO C library compliant with the <i>Arm Embedded Application Binary Interface</i> (AEABI).
--library_interface=<lib> Where <lib> is not one of: <ul style="list-style-type: none"> aeabi_clib aeabi_clib90 aeabi_clib99 armcc 	No equivalent.	Arm Compiler for Embedded 6 assumes the use of an AEABI compliant library.
--licretry	No equivalent.	There is no equivalent of the --licretry option. The Arm Compiler for Embedded 6 tools automatically retry failed attempts to obtain a license.
--list_macros	-E -dM	List all the macros that are defined at the end of the translation unit, including the predefined macros.
--littleend	-mlittle-endian	Generates code for little-endian data.
--lower_ropi, --no_lower_ropi	-fropi-lowering, -fno-ropi-lowering	Enables or disables less restrictive C when generating <i>Read-Only Position Independent</i> (ROPI) code. Note: In Arm Compiler 5, when --acps=/ropi is specified, --lower_ropi is not switched on by default. In Arm Compiler for Embedded 6, when -fropi is specified, -fropi-lowering is switched on by default.
--lower_rwpi, --no_lower_rwpi	-frwpi-lowering, -fno-rwpi-lowering	Enables or disables less restrictive C when generating <i>Read/Write Position Independent</i> (RWPI) code.
-M	-M	Instructs the compiler to produce a list of makefile dependency lines suitable for use by a make utility.
--md	-MD	Creates makefile dependency files, including the system header files. In Arm Compiler 5, this is equivalent to --md --depend_system_headers.
--md --no_depend_system_headers	-MMD	Creates makefile dependency files, without the system header files.
--mm	-MM	Creates a single makefile dependency file, without the system header files. In Arm Compiler 5, this is equivalent to -M --no_depend_system_headers.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
--multifile, --no_multifile	No direct equivalent. However, see Optimizing across modules with Link-Time Optimization in the <i>Arm Compiler for Embedded User Guide</i> .	Enables and disables optimizations between multiple source files.
--no_comment_section	-fno-ident	Removes the .comment section from object files.
--no_exceptions	-fno-exceptions	Disables the generation of code needed to support C++ exceptions. Note: For C++ code, Arm Compiler for Embedded 6 defaults to -fexceptions. As a result, there might be a large increase in the code size. If you use -fno_exceptions, then the code size is in the range of that created with Arm Compiler 5.
--no_hide_all	-fvisibility=default	Sets the default visibility of ELF symbols to the specified option, unless overridden in the source with the __attribute__((visibility("<visibility_type>"))) attribute. The default is -fvisibility=hidden. Note: The behavior of the armclang option -fvisibility=hidden is different from that of the armcc option --hide-all. With the armclang option -fvisibility=hidden, extern declarations are visible, and all other symbols are hidden. With the armcc option --hide-all, all symbols are hidden.
--no_protect_stack	-fno-stack-protector	Explicitly disables stack protection. For more information, see Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior .
-rtti	-frtti	C++ only. -frtti enables the generation of code that is needed to support <i>Run-Time Type Information</i> (RTTI) features. This option is the default when compiling for C++. See -frtti, -fno-rtti
-no_rtti	-fno-rtti	C++ only. -fno-rtti disables the generation of code that is needed to support RTTI features. See -frtti, -fno-rtti
-o	-o	Specifies the name of the output file.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
-O<num>	-O<num>	Specifies the level of optimization to be used when compiling source files. The default for Arm Compiler 5 is -O2. The default for Arm Compiler for Embedded 6 is -O0. For Arm Compiler for Embedded 6, Arm recommends -O1 rather than -O0 for best trade-off between debug view, codesize, and performance. For more information, see Optimization differences .
-Ospace	-Oz /-Os	Performs optimizations to reduce image size at the expense of a possible increase in execution time.
-Otime	This is the default.	Performs optimizations to reduce execution time at the expense of a possible increase in image size. There is no equivalent of the -Otime option. Arm Compiler for Embedded 6 optimizes for execution time by default, unless you specify the -Os or -Oz options.
--phony_targets	-MP	Emits dummy makefile rules.
--preinclude	-include	Include the source code of a specified file at the beginning of the compilation.
--protect_stack	-fstack-protector, -fstack-protector-strong	Enables stack protection on vulnerable functions. For more information, see Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior .
--protect_stack_all	-fstack-protector-all	Enables stack protection on all functions. For more information, see Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior .
--relaxed_ref_def	-fcommon	Places zero-initialized definitions in a common block.
--retain	-O	The optimization level to use for the best code coverage might depend on your source code. In Arm Compiler 5 the --retain option disables specific optimizations by name. There is no direct equivalent of this for Arm Compiler for Embedded 6. Instead you must select the optimization level that best satisfies your requirements. For more information, see -O in the <i>Arm Compiler for Embedded Reference Guide</i> .
-S	-S	Outputs the disassembly of the machine code that the compiler generates. The output from this option differs between releases. Arm Compiler 5 produces output with <code>armasm</code> syntax while Arm Compiler for Embedded 6 produces output with GNU syntax.
--show_cmdline	-v	Shows how the compiler processes the command-line. The commands are shown normalized, and the contents of any via files are expanded.

Arm Compiler 5 option	Arm Compiler for Embedded 6 option	Description
<code>--split_ldm</code>	<code>-fno-ldm-stm</code>	Disables the generation of LDM and STM instructions. Note: While the armcc option <code>--split_ldm</code> limits the size of generated LDM/STM instructions, the armclang option <code>-fno-ldm-stm</code> disables the generation of LDM and STM instructions altogether.
<code>--split_sections</code>	<code>-ffunction-sections</code>	Generates one ELF section for each function in the source file. In Arm Compiler for Embedded 6, <code>-ffunction-sections</code> is the default. Therefore, the merging of identical constants cannot be done by armclang. Instead, the merging is done by armlink. For more information, see Merging identical constants in the <i>Arm Compiler for Embedded Reference Guide</i> .
<code>--strict</code>	<code>-pedantic-errors</code>	Generate errors if code violates strict ISO C and ISO C++.
<code>--strict_warnings</code>	<code>-pedantic</code>	Generate warnings if code violates strict ISO C and ISO C++.
<code>--string_literal_pools, --no_string_literal_pools</code>	No equivalent.	The way that literals are merged is handled differently in Arm Compiler for Embedded 6 compared to Arm Compiler 5. For more information, see Literal pool options in armclang .
<code>--thumb</code>	<code>-mthumb</code>	Targets the T32 instruction set.
<code>--no_unaligned_access, --unaligned_access</code>	<code>-mno-unaligned-access, -munaligned-access</code>	Enables or disables unaligned accesses to data on Arm processors.
<code>--use_frame_pointer, --no_use_frame_pointer</code>	<code>-fno-omit-frame-pointer, -fomit-frame-pointer</code>	Controls whether a register is reserved for storing the stack frame pointer.
<code>--vectorize</code> <code>--no_vectorize</code>	<code>-fvectorize</code> <code>-fno-vectorize</code>	Enables or disables the generation of Advanced SIMD vector instructions directly from C or C++ code.
<code>--via</code>	<code>@file</code>	Reads an additional list of compiler options from a file.
<code>--vla</code>	No equivalent.	Support for variable length arrays. Arm Compiler for Embedded 6 automatically supports variable length arrays in accordance with the language standard.
<code>--vsn</code>	<code>--version</code>	Displays version information and license details. In Arm Compiler for Embedded 6 you can also use <code>--vsn</code> .
<code>--wchar16, --wchar32</code>	<code>-fshort-wchar,</code> <code>-fno-short-wchar</code>	Sets the size of <code>wchar_t</code> type. The default for Arm Compiler 5 is <code>--wchar16</code> . The default for Arm Compiler for Embedded 6 is <code>-fno-short-wchar</code> .

Related information

[armclang Command-line Options](#)
[Compiler-specific Function, Variable, and Type Attributes](#)

The LLVM Compiler Infrastructure Project

3.2 Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior

You can see which functions are protected and compare Arm® Compiler 5 protection with Arm Compiler for Embedded 6 protection after migration.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

The behavior of `armclang -fstack-protector` and `armclang -fstack-protector-strong` is different from the behavior of the `armcc --protect_stack` option:

- With `armcc --protect_stack`, a function is considered vulnerable if it contains a `char` or `wchar_t` array of any size.
- With `armclang -fstack-protector`, a function is considered vulnerable if it contains at least one of the following:
 - A character array larger than 8 bytes.
 - An 8-bit integer array larger than 8 bytes.
 - A call to `alloca()` with either a variable size or a constant size bigger than 8 bytes.
- With `armclang -fstack-protector-strong`, a function is considered vulnerable if it contains:
 - An array of any size and type.
 - A call to `alloca()`.
 - A local variable that has its address taken.

Arm recommends the use of `-fstack-protector-strong`.



When using Arm Compiler 5, the value of the variable `__stack_chk_guard` could change during the life of the program. With Arm Compiler for Embedded 6, a suitable implementation might set this variable to a random value when the program is loaded, before the first protected function is entered. The value must then remain unchanged during the life of the program.

Example

1. Create the file `test.c` containing the following code:

```
// test.c
#include <stdio.h>
```

```
#include <stdlib.h>
#include <string.h>

void *__stack_chk_guard = (void *)0xdeadbeef;

void __stack_chk_fail(void) {
    printf("Stack smashing detected.\n");
    exit(1);
}

static void copy(const char *p) {
    char buf[9];
    strcpy(buf, p);
    printf("Copied: %s\n", buf);
}

int main(void) {
    const char *t = "Hello World!";
    copy(t);
    printf("%s\n", t);
    return 0;
}
```

2. For Arm Compiler 5, search for branches to the `__stack_chk_fail()` function in the output from the `fromelf -c` command. The functions containing such branches are protected.

```
armcc -c --cpu=7-A --protect_stack test.c -o test.o

fromelf -c test.o
...
    main
      0x00000010:    e92d407f    .@-    PUSH    {r0-r6,lr}
      0x00000014:    e28f4064    d@..    ADR     r4,{pc}+0x6c ; 0x80
      0x00000018:    e59f5070    pP..    LDR     r5,[pc,#112] ;
      [__stack_chk_guard = 0x90] = 0
      0x0000001c:    e1a01004    ....    MOV     r1,r4
      0x00000020:    e5950000    ....    LDR     r0,[r5,#0]
      0x00000024:    e58d000c    ....    STR     r0,[sp,#0xc]
      0x00000028:    e1a0000d    ....    MOV     r0,sp
      0x0000002c:    ebfffffe    ....    BL      strcpy
      0x00000030:    e1a0100d    ....    MOV     r1,sp
      0x00000034:    e28f0058    X...    ADR     r0,{pc}+0x60 ; 0x94
      0x00000038:    ebfffffe    ....    BL      __2printf
      0x0000003c:    e59d000c    ....    LDR     r0,[sp,#0xc]
      0x00000040:    e5951000    ....    LDR     r1,[r5,#0]
      0x00000044:    e1500001    ..P.    CMP     r0,r1
      0x00000048:    1bfffffe    ....    BLNE    __stack_chk_fail ; 0x0
    Section #1
      0x0000004c:    e1a01004    ....    MOV     r1,r4
    ...
```

3. For Arm Compiler for Embedded 6, use the `armclang [COMMUNITY] -Rpass` remark option.

```
> armclang -c --target=arm-arm-none-eabi -march=armv8-a -O0 -fstack-protector -
Rpass=stack-protector test.c
test.c:14:13: remark: Stack protection applied to function main due to a stack
allocated buffer or struct containing a
    buffer [-Rpass=stack-protector]
int main(void) {
    ^
```

**Note**

You can also use the `fromelf -c` command and search the output for functions containing branches to the `__stack_chk_fail()` function.

Related information

[-fstack-protector](#), [-fstack-protector-all](#), [-fstack-protector-strong](#), [-fno-stack-protector](#)
[-Rpass](#)

3.3 Command-line options for preprocessing assembly source code

The functionality of the `--cpreproc` and `--cpreproc_opts` command-line options in the version of `armasm` supplied with Arm® Compiler for Embedded 6 is different from the options used in earlier versions of `armasm` to preprocess assembly source code.

If you are using `armasm` to assemble source code that requires the use of the preprocessor, you must use both the `--cpreproc` and `--cpreproc_opts` options together. Also:

- As a minimum, you must include the `armclang` options `--target` and either `-mcpu` or `-march` in `--cpreproc_opts`.
- The input assembly source must have an upper-case extension `.s`.

If you have existing source files, which require preprocessing, and that have the lower-case extension `.s`, then to avoid having to rename the files:

1. Perform the preprocessing step separately using the `armclang` option `-x assembler-with-cpp`.
2. Assemble the preprocessed file without using the `--cpreproc` and `--cpreproc_opts` options.

Example using `armclang -x`

This example shows the use of the `armclang -x` option.

```
armclang --target=aarch64-arm-none-eabi -march=armv8-a -x assembler-with-cpp -E  
test.s -o test_preproc.s  
armasm --cpu=8-A.64 test_preproc.s
```

Example using `armasm --cpreproc_opts`

The options to the preprocessor in this example are `--cpreproc_opts=--target=arm-arm-none-eabi,-mcpu=cortex-a9,-D,DEF1,-D,DEF2`.

```
armasm --cpu=cortex-a9 --cpreproc --cpreproc_opts=--target=arm-arm-none-eabi,-  
mcpu=cortex-a9,-D,DEF1,-D,DEF2 -I /path/to/includes1 -I /path/to/includes2 input.S
```



Note

Ensure that you specify compatible architectures in the `armclang` options `--target`, `-mcpu` or `-march`, and the `armasm` option `--cpu`.

Related information

[--cpreproc assembler option](#)

[--cpreproc_opts assembler option](#)

[Mandatory armclang options](#)

[-march armclang option](#)

[-mcpu armclang option](#)

[--target armclang option](#)

[-x armclang option](#)

[Preprocessing assembly code](#)

3.4 Inline assembly with Arm Compiler for Embedded 6

Inline assembly in Arm® Compiler for Embedded 6 must be written in GNU assembly syntax. Inline assembly in Arm Compiler 5 is written in `armasm` syntax. If you have inline assembly written in `armasm` syntax, you must modify the `armasm` syntax assembly to use GNU assembly syntax.

In Arm Compiler 5:

- You can use C variable names directly inside inline assembly statements.
- You do not have direct access to physical registers. You must use C or C++ variables names as operands, and the compiler maps them to physical register. You must set the value of these variables before you read them within an inline assembly statement.
- If you use register names in inline assembly code, they are treated as C or C++ variables. They do not necessarily relate to the physical register of the same name. If the register name is not declared as a C or C++ variable, the compiler generates a warning.

In Arm Compiler for Embedded 6:

- You cannot use C or C++ variable names directly inside inline assembly statements. You can map the physical registers to C or C++ variable names using operand mapping and constraints.
- You have direct access to physical registers. There is no need to set the value of the registers before you read them within inline assembly statements.
- If you use register names in inline assembly code, they are the physical register of the same name.

In Arm Compiler for Embedded 6 you cannot use C variable names directly within inline assembly. However, the GNU assembly syntax in Arm Compiler for Embedded 6 provides a way for mapping input and output operands to C variable names.

Arm Compiler 5 optimizes inline assembly, but Arm Compiler for Embedded 6 emits it exactly as written.

While Arm Compiler for Embedded 6 does not attempt to optimize the inline assembly instructions, it can remove a block of code containing inline assembly during optimization. The compiler is unaware of the content of the assembly, so might in some cases remove the block while attempting to remove unused code.



Note

The `volatile` qualifier disables certain compiler optimizations that might otherwise lead to the compiler removing the code block. The `volatile` qualifier is optional. However, consider using it around your assembly code blocks to ensure the compiler does not remove them when compiling at any optimization level other than `-O0`.

See the documentation of the `volatile` keyword in the *Arm Compiler for Embedded 6 User Guide* for details.

For more information on writing inline assembly using `__asm` in armclang, see [__asm](#).

For more information on GNU assembly syntax, see [Overview of differences between armasm and GNU syntax assembly code](#).

Inline assembly example in Arm Compiler 5

The following example shows inline assembly code in Arm Compiler 5:

```
//foo.c:
int add(int i, int j)
{
    int res;
    __asm
    (
        "ADD res, i, j \t\n"
        "SUB res, i, res \t\n"
    );
    return res;
}
```

The following example shows an alternative syntax for inline assembly code in Arm Compiler 5:

```
//foo.c:
int add(int i, int j)
{
    int res;
    __asm
    {
        ADD    res, i, j
        SUB    res, i, res
    }
    return res;
}
```

Compile `foo.c` using `armcc`:

```
armcc foo.c -c -S -o foo.s
```

Arm Compiler 5 converts the example inline assembly code to:

```
;foo.s:
add PROC
    ADD r1,r0,r1
    SUB r0,r0,r1
    BX  lr
    ENDP
```

Inline assembly example in Arm Compiler for Embedded 6

The example below shows the equivalent inline assembly code in Arm Compiler for Embedded 6.

```
//foo.c:
int add(int i, int j)
{
    int res = 0;
    __asm
    (
        "ADD %[result], %[input_i], %[input_j] \t\n"
        "SUB %[result], %[input_i], %[result] \t\n"
        : [result] "=&r" (res)
        : [input_i] "r" (i), [input_j] "r" (j)
    );
    return res;
}
```

Compile `foo.c` using `armclang` with optimization level `-O1`:

```
armclang foo.c --target=arm-arm-none-eabi -march=armv8-a -O1 -c -S -o foo.s
```

Arm Compiler for Embedded 6 converts the example inline assembly code to:

```
;foo.s:
add:
    .fnstart
@ BB#0:
    @APP
    add r2,r0,r1
    sub r2,r0,r2
    @NO_APP
    mov r0,r2
    bx  lr
```



Note

Arm Compiler for Embedded 6 supports inline assembly using the `__asm` or `asm` keywords. However, the `asm` keyword is accepted only when:

- Used within C++ language source files.

- Used within C language source files without strict ISO C Standard compliance. For example, `asm` is accepted when using `-std=gnu11`.

The compiler supports the GNU form of inline assembly. The compiler does not support the Microsoft form of inline assembly. More detailed documentation of the `asm` construct is available at <https://gcc.gnu.org/onlinedocs/gcc/Extended-Asm.html>.

Related information

[armclang Inline Assembler](#)

[How to Use Inline Assembly Language in C Code](#)

[Constraints for asm Operands](#)

[Constraint Modifier Characters](#)

3.5 Migrating architecture and processor names for command-line options

There are minor differences between the architecture and processor names that Arm® Compiler for Embedded 6 recognizes, and the names that Arm Compiler 5 recognizes. Within Arm Compiler for Embedded 6, there are differences in the architecture and processor names that `armclang` recognizes and the names that `armasm`, `armlink`, and `fromelf` recognize. This topic shows the differences in the architecture and processor names for the different tools in Arm Compiler 5 and Arm Compiler for Embedded 6.

The tables show the documented `--cpu` options in Arm Compiler 5 and their corresponding options for migrating your Arm Compiler 5 command-line options to Arm Compiler for Embedded 6.



Note

The tables assume the default floating-point unit derived from the `--cpu` option in Arm Compiler 5. However, in Arm Compiler for Embedded 6, `armclang` selects different defaults for floating-point unit (VFP) and Advanced SIMD. Therefore, the tables also show how to use the `armclang` options `-mfloat-abi` and `-mfpu` to be compatible with the default floating-point unit in Arm Compiler 5. The tables do not provide an exhaustive list.

Table 3-2: Architecture selection in Arm Compiler 5 and Arm Compiler for Embedded 6

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Architecture description
<code>--cpu=4</code>	Not supported	Not supported	Armv4
<code>--cpu=4T</code>	Not supported	Not supported	Armv4T
<code>--cpu=5T</code>	Not supported	Not supported	Armv5T
<code>--cpu=5TE</code>	Not supported	Not supported	Armv5TE
<code>--cpu=5TEJ</code>	Not supported	Not supported	Armv5TEJ
<code>--cpu=6</code>	Not supported	Not supported	Generic Armv6

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Architecture description
--cpu=6-K	Not supported	Not supported	Armv6 -K
--cpu=6-Z	Not supported	Not supported	Armv6 -Z
--cpu=6T2	Not supported	Not supported	Armv6 T2
--cpu=6-M	--target=arm-arm-none-eabi -march=armv6-m	--cpu=6S-M	Armv6-M
--cpu=6S-M	--target=arm-arm-none-eabi -march=armv6s-m	--cpu=6S-M	Armv6 S-M
--cpu=7-A --cpu=7-A.security	--target=arm-arm-none-eabi -march=armv7-a -mfloat-abi=soft	--cpu=7-A.security	Armv7-A without VFP and Advanced SIMD. In Arm Compiler 5, security extension is not enabled with --cpu=7-A but is enabled with --cpu=7-A.security. In Arm Compiler for Embedded 6, armclang always enables the Armv7-A TrustZone security extension with -march=armv7-a. However, armclang does not generate an SMC instruction unless you specify it with an intrinsic or inline assembly.
--cpu=7-R	--target=arm-arm-none-eabi -march=armv7-r -mfloat-abi=soft	--cpu=7-R	Armv7-R without VFP and Advanced SIMD
--cpu=7-M	--target=arm-arm-none-eabi -march=armv7-m	--cpu=7-M	Armv7-M
--cpu=7E-M	--target=arm-arm-none-eabi -march=armv7e-m -mfloat-abi=soft	--cpu=7E-M	Armv7 E-M

Table 3-3: Processor selection in Arm Compiler 5 and Arm Compiler for Embedded 6

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Description
--cpu=Cortex-A5	--target=arm-arm-none-eabi -mcpu=cortex-a5 -mfloat-abi=soft	--cpu=Cortex-A5.no_neon.no_vfp	Cortex®-A5 without Advanced SIMD and VFP
--cpu=Cortex-A5.neon	--target=arm-arm-none-eabi -mcpu=cortex-a5 -mfloat-abi=hard	--cpu=Cortex-A5	Cortex-A5 with Advanced SIMD and VFP
--cpu=Cortex-A5.vfp	--target=arm-arm-none-eabi -mcpu=cortex-a5 -mfloat-abi=hard -mfpu=vfpv4-d16	--cpu=Cortex-A5.no_neon	Cortex-A5 with VFP, without Advanced SIMD
--cpu=Cortex-A7	--target=arm-arm-none-eabi -mcpu=cortex-a7 -mfloat-abi=hard	--cpu=Cortex-A7	Cortex-A7 with Advanced SIMD and VFP

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Description
--cpu=Cortex-A7.no_neon.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-a7 -mfloat-abi=soft	--cpu=Cortex-A7.no_neon.no_vfp	Cortex-A7 without Advanced SIMD and VFP
--cpu=Cortex-A7.no_neon	--target=arm-arm-none-eabi -mcpu=cortex-a7 -mfloat-abi=hard -mfpv4-d16	--cpu=Cortex-A7.no_neon	Cortex-A7 with VFP, without Advanced SIMD
--cpu=Cortex-A8	--target=arm-arm-none-eabi -mcpu=cortex-a8 -mfloat-abi=hard	--cpu=Cortex-A8	Cortex-A8 with VFP and Advanced SIMD
--cpu=Cortex-A8.no_neon	--target=arm-arm-none-eabi -mcpu=cortex-a8 -mfloat-abi=soft	--cpu=Cortex-A8.no_neon	Cortex-A8 without Advanced SIMD and VFP
--cpu=Cortex-A9	--target=arm-arm-none-eabi -mcpu=cortex-a9 -mfloat-abi=hard	--cpu=Cortex-A9	Cortex-A9 with Advanced SIMD and VFP
--cpu=Cortex-A9.no_neon.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-a9 -mfloat-abi=soft	--cpu=Cortex-A9.no_neon.no_vfp	Cortex-A9 without Advanced SIMD and VFP
--cpu=Cortex-A9.no_neon	--target=arm-arm-none-eabi -mcpu=cortex-a9 -mfloat-abi=hard -mfpv3-d16-fp16	--cpu=Cortex-A9.no_neon	Cortex-A9 with VFP but without Advanced SIMD
--cpu=Cortex-A12	--target=arm-arm-none-eabi -mcpu=cortex-a12 -mfloat-abi=hard	--cpu=Cortex-A12	Cortex-A12 with Advanced SIMD and VFP
--cpu=Cortex-A12.no_neon.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-a12 -mfloat-abi=soft	--cpu=Cortex-A12.no_neon.no_vfp	Cortex-A12 without Advanced SIMD and VFP
--cpu=Cortex-A15	--target=arm-arm-none-eabi -mcpu=cortex-a15 -mfloat-abi=hard	--cpu=Cortex-A15	Cortex-A15 with Advanced SIMD and VFP
--cpu=Cortex-A15.no_neon	--target=arm-arm-none-eabi -mcpu=cortex-a15 -mfloat-abi=hard -mfpv4-d16	--cpu=Cortex-A15.no_neon	Cortex-A15 with VFP, without Advanced SIMD
--cpu=Cortex-A15.no_neon.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-a15 -mfloat-abi=soft	--cpu=Cortex-A15.no_neon.no_vfp	Cortex-A15 without Advanced SIMD and VFP
--cpu=Cortex-A17	--target=arm-arm-none-eabi -mcpu=cortex-a17 -mfloat-abi=hard	--cpu=Cortex-A17	Cortex-A17 with Advanced SIMD and VFP
--cpu=Cortex-A17.no_neon.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-a17 -mfloat-abi=soft	--cpu=Cortex-A17.no_neon.no_vfp	Cortex-A17 without Advanced SIMD and VFP
--cpu=Cortex-R4	--target=arm-arm-none-eabi -mcpu=cortex-r4	--cpu=Cortex-R4	Cortex-R4 without VFP

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Description
--cpu=Cortex-R4F	--target=arm-arm-none-eabi -mcpu=cortex-r4f -mfloat-abi=hard	--cpu=Cortex-R4F	Cortex-R4 with VFP
--cpu=Cortex-R5	--target=arm-arm-none-eabi -mcpu=cortex-r5 -mfloat-abi=soft	--cpu=Cortex-R5.no_vfp	Cortex-R5 without VFP
--cpu=Cortex-R5F	--target=arm-arm-none-eabi -mcpu=cortex-r5 -mfloat-abi=hard	--cpu=Cortex-R5	Cortex-R5 with double precision VFP
--cpu=Cortex-R5F-rev1.sp	--target=arm-arm-none-eabi -mcpu=cortex-r5 -mfloat-abi=hard -mfpv3xd	--cpu=Cortex-R5.sp	Cortex-R5 with single precision VFP
--cpu=Cortex-R7	--target=arm-arm-none-eabi -mcpu=cortex-r7 -mfloat-abi=hard	--cpu=Cortex-R7	Cortex-R7 with VFP
--cpu=Cortex-R7.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-r7 -mfloat-abi=soft	--cpu=Cortex-R7.no_vfp	Cortex-R7 without VFP
--cpu=Cortex-R8	--target=arm-arm-none-eabi -mcpu=cortex-r8 -mfloat-abi=hard	--cpu=Cortex-R8	Cortex-R8 with VFP
--cpu=Cortex-R8.no_vfp	--target=arm-arm-none-eabi -mcpu=cortex-r8 -mfloat-abi=soft	--cpu=Cortex-R8.no_vfp	Cortex-R8 without VFP
--cpu=Cortex-M0	--target=arm-arm-none-eabi -mcpu=cortex-m0	--cpu=Cortex-M0	Cortex-M0
--cpu=Cortex-M0plus	--target=arm-arm-none-eabi -mcpu=cortex-m0plus	--cpu=Cortex-M0plus	Cortex-M0+
--cpu=Cortex-M1	--target=arm-arm-none-eabi -mcpu=cortex-m1	--cpu=Cortex-M1	Cortex-M1
--cpu=Cortex-M3	--target=arm-arm-none-eabi -mcpu=cortex-m3	--cpu=Cortex-M3	Cortex-M3
--cpu=Cortex-M4	--target=arm-arm-none-eabi -mcpu=cortex-m4 -mfloat-abi=soft	--cpu=Cortex-M4.no_fp	Cortex-M4 without VFP
--cpu=Cortex-M4.fp	--target=arm-arm-none-eabi -mcpu=cortex-m4 -mfloat-abi=hard	--cpu=Cortex-M4	Cortex-M4 with VFP
--cpu=Cortex-M7	--target=arm-arm-none-eabi -mcpu=cortex-m7 -mfloat-abi=soft	--cpu=Cortex-M7.no_fp	Cortex-M7 without VFP
--cpu=Cortex-M7.fp.dp	--target=arm-arm-none-eabi -mcpu=cortex-m7 -mfloat-abi=hard	--cpu=Cortex-M7	Cortex-M7 with double precision VFP

armcc, armlink, armasm, and fromelf option in Arm Compiler 5	armclang option in Arm Compiler for Embedded 6	armlink, armasm, and fromelf option in Arm Compiler for Embedded 6	Description
--cpu=Cortex-M7.fp.sp	--target=arm-arm-none-eabi -mcpu=cortex-m7 -mfloat-abi=hard -mfpv5-sp-d16	--cpu=Cortex-M7.fp.sp	Cortex-M7 with single precision VFP

Enabling or disabling architectural features in Arm Compiler for Embedded 6

Arm Compiler for Embedded 6, by default, automatically enables or disables certain architectural features such as the floating-point unit, Advanced SIMD, and Cryptographic extensions depending on the specified architecture or processor. For a list of architectural features, see `-mcpu` in the *Arm Compiler for Embedded Reference Guide*. You can override the defaults using other options.

For `armclang`:

- For AArch64 targets, you must use either `-march` or `-mcpu` to specify the architecture or processor and the required architectural features. You can use `+ [no] feature` with `-march` or `-mcpu` to override any architectural feature.
- For AArch32 targets, you must use either `-march` or `-mcpu` to specify the architecture or processor and the required architectural features. You can use `-mfloat-abi` to override floating-point linkage. You can use `-mfpv` to override floating-point unit, Advanced SIMD, and Cryptographic extensions. You can use `+ [no] feature` with `-march` or `-mcpu` to override certain other architectural features.

For `armasm`, `armlink`, and `fromelf`, you must use the `--cpu` option to specify the architecture or processor and the required architectural features. You can use `--fpu` to override the floating-point unit and floating-point linkage. The `--cpu` option is not mandatory for `armlink` and `fromelf`, but is mandatory for `armasm`.



Note

- In Arm Compiler 5, if you use the `armcc` option `--fpu=none`, the compiler generates an error if it detects floating-point code. This behavior is different in Arm Compiler for Embedded 6. If you use the `armclang` option `-mfpv=none`, the compiler automatically uses software floating-point libraries if it detects any floating-point code. You cannot use the `armlink` option `--fpu=none` to link object files created using `armclang`.
- To link object files created using the `armclang` option `-mfpv=none`, you must set the `armlink` option `--fpu` to an option that supports software floating-point linkage, for example `--fpu=softvfp`, rather than using `--fpu=none`.

Related information

[-mcpu \(armclang\)](#)
[-march \(armclang\)](#)
[-mfloat-abi \(armclang\)](#)
[-mfpv \(armclang\)](#)
[--target \(armclang\)](#)
[--cpu \(armlink\)](#)

```
--fpu (armlink)
--cpu (fromelf)
--fpu (fromelf)
--cpu (armasm)
--fpu (armasm)
```

3.6 Preprocessing a scatter file when linking with armlink

Preprocessing a scatter file when linking with `armlink` in Arm® Compiler for Embedded 6 requires extra options.

The following shows the required change to the first line of the scatter file:

Arm Compiler 5

```
#!armcc -E
```

Arm Compiler for Embedded 6

```
#!armclang -E --target=arm-arm-none-eabi -mcpu=cortex-m7 -xc
```

The mandatory option `--target` specifies the target state, either AArch32 state, as shown in this example, or AArch64 state. See [--target](#).

The option `-mcpu` specifies a processor, Cortex-M7 in this example. Alternatively, you can use `-march` to specify an architecture. See [-mcpu](#) or [-march](#).

The option `-x` specifies the source language. See [-x](#).

The option `-E` makes `armclang` only execute the preprocessor step. See [-E](#).

3.7 Migrating predefined macros

The functionality of the Arm® Compiler 5 predefined macro `__MODULE__` is provided by the `__FILE_NAME__` macro in Arm Compiler for Embedded 6.

Related information

[Predefined macros](#)

4. Compiler Source Code Compatibility

Provides details of source code compatibility between Arm® Compiler for Embedded 6 and older armcc compiler versions.

4.1 Language extension compatibility: keywords

Arm® Compiler for Embedded 6 supports some keywords that are supported in Arm Compiler 5.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

The following table lists some of the commonly used keywords that Arm Compiler 5 supports and shows whether Arm Compiler for Embedded 6 supports them using `__attribute__`. Replace any instances of these keywords in your code with the recommended alternative where available or use inline assembly instructions.



This table is not an exhaustive list of all keywords.

Table 4-1: Keyword language extensions in Arm Compiler 5 and Arm Compiler for Embedded 6

Keyword supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 keyword or alternative
<code>__align(x)</code>	<code>__attribute__((aligned(x)))</code>
<code>__alignof__</code>	<code>__alignof__</code>
<code>__ALIGNOF__</code>	<code>__alignof__</code>
Embedded assembly using <code>__asm</code>	Arm Compiler for Embedded 6 does not support the <code>__asm</code> keyword on function definitions and declarations for embedded assembly. Instead, you can write embedded assembly using the <code>__attribute__((naked))</code> function attribute. See __attribute__((naked)) .
<code>__const</code>	<code>__attribute__((const))</code> Note: Older versions of armcc supported the <code>__const</code> keyword. The equivalent for this keyword in Arm Compiler 5 and Arm Compiler for Embedded 6 is <code>__attribute__((const))</code> .
<code>__attribute__((const))</code>	<code>__attribute__((const))</code>

Keyword supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 keyword or alternative
<code>__forceinline</code>	<ul style="list-style-type: none"> For C90, use <code>__inline__</code> and <code>__attribute__((always_inline))</code>. For other source languages, use <code>inline</code> and <code>__attribute__((always_inline))</code>. See <code>__attribute__((always_inline))</code>.
<code>__global_reg(N)</code>	<p>Use the <code>register</code> and <code>__asm</code> keywords for global named register variables using core registers.</p> <p>For example:</p> <pre>register int Reg5 __asm("r5")</pre> <p>In Arm Compiler for Embedded 6, you must also use the relevant <code>armclang</code> option <code>-ffixed-r<N></code>.</p> <p>Alternatively, you can use equivalent inline assembler instructions.</p>
<code>__inline(x)</code>	<code>__inline__</code> . The use of this keyword depends on the language mode.
<code>__int64</code>	<p>You can use <code>int64_t</code>, which is a 64-bit integer type defined in the header file <code><stdint.h></code> (for C source files) or <code><stdint></code> (for C++ source files). You can also use <code>long long</code>. However, if you use <code>long long</code> in C90 mode, the compiler gives:</p> <ul style="list-style-type: none"> A warning. An error, if you also use <code>-pedantic-errors</code>.
<code>__INTADDR__</code>	No equivalent.
<code>__irq</code>	<code>__attribute__((interrupt))</code> . This keyword is not supported in AArch64.
<code>__packed</code> for removing padding within structures.	<p><code>__attribute__((packed))</code>. This keyword provides limited functionality when compared to <code>__packed</code>:</p> <ul style="list-style-type: none"> The <code>__attribute__((packed))</code> variable attribute applies to members of a structure or union. It does not apply to variables that are not members of a structure or union. <code>__attribute__((packed))</code> is not a type qualifier. Taking the address of a packed member can result in unaligned pointers, and usually the compiler generates a warning. We recommend upgrading this warning to an error when migrating code that uses <code>__packed</code>. To upgrade the warning to an error, use the <code>armclang</code> option <code>-Werror=<name></code>. <p>The placement of the attribute is different from the placement of <code>__packed</code>. If your legacy code contains <code>typedef __packed struct</code>, then replace it with:</p> <pre>typedef struct __attribute__((packed))</pre>

Keyword supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 keyword or alternative
<code>__packed</code> as a type qualifier for unaligned access.	<p><code>__unaligned</code>. This keyword provides limited functionality when compared to the <code>__packed</code> type qualifier.</p> <p>You can use the <code>__unaligned</code> type qualifier over a structure only when using <code>typedef</code> or when declaring a structure variable. This limitation does not apply when using <code>__packed</code> in Arm Compiler 5. Therefore, there is no migration for legacy code that contains <code>__packed struct S{...};</code>.</p>
<code>__pure</code>	<code>__attribute__((const))</code>
<code>__smc</code>	Use inline assembler instructions or equivalent routine.
<code>__softfp</code>	<code>__attribute__((pcs("aapcs")))</code>
<code>__svc</code>	Use inline assembler instructions or equivalent routine.
<code>__svc_indirect</code>	Use inline assembler instructions or equivalent routine.
<code>__svc_indirect_r7</code>	Use inline assembler instructions or equivalent routine.
<code>__thread</code>	<code>__thread</code>
<code>__value_in_regs</code>	<code>__attribute__((value_in_regs))</code>
<code>__weak</code>	<code>__attribute__((weak))</code>
<code>__writeonly</code>	No equivalent.
<p>Named register variables for direct manipulation of a core register as if it were a C variable. For example:</p> <pre>register int R5 __asm("r5")</pre>	<p>Use the <code>register</code> and <code>__asm</code> keywords for global named register variables using core registers.</p> <p>For example:</p> <pre>register int Reg5__asm("r5")</pre> <p>In Arm Compiler for Embedded 6, you must also use the relevant <code>armclang</code> option <code>-ffixed-r<N></code>.</p>
<p>Named register variables for direct manipulation of a system register, other than core registers, as if it were a C variable. For example:</p> <pre>register int fpscr__asm("fpscr")</pre>	No equivalent. To access FPSCR, use the <code>__vfp_status</code> intrinsic or inline assembly instructions.

Migrating the `__packed` keyword from Arm Compiler 5 to Arm Compiler for Embedded 6

The `__packed` keyword in Arm Compiler 5 has the effect of:

- Removing the padding within structures.
- Qualifying the variable for unaligned access.

Arm Compiler for Embedded 6 does not support `__packed`, but supports the `__attribute__((packed))` attribute and the `__unaligned` keyword. Depending on the use, you might need to replace `__packed` with both `__attribute__((packed))` and `__unaligned`. The following table shows the migration paths for various uses of `__packed`.

Table 4-2: Migrating the `__packed` keyword

Arm Compiler 5	Arm Compiler for Embedded 6
<code>__packed int x;</code>	<code>__unaligned int x;</code>
<code>__packed int *x;</code>	<code>__unaligned int *x;</code>
<code>int * __packed x;</code>	<code>int * __unaligned x;</code>
<code>__unaligned int * __packed x;</code>	<code>__unaligned int * __unaligned x;</code>
<code>typedef __packed struct S{...} s;</code>	<code>typedef __unaligned struct</code> <code>__attribute__((packed)) S{...} s;</code>
<code>__packed struct S{...};</code>	There is no migration. Use a <code>typedef</code> instead.
<code>__packed struct S{...} s;</code>	<code>__unaligned struct __attribute__((packed)) S{...}</code> <code>s;</code> Subsequent declarations of variables of type <code>struct S</code> must use <code>__unaligned</code> , for example <code>__unaligned struct S s2</code> .
<code>struct S {__packed int a;}</code>	<code>struct S {__attribute__((packed)) __unaligned int</code> <code>a;}</code>

Related information

[Unaligned access support in Arm Compiler for Embedded](#)
[Compiler-specific Keywords and Operators](#)
[Compiler-specific Function, Variable, and Type Attributes](#)
[-W](#)

4.2 Language extension compatibility: attributes


Arm® Compiler for Embedded 6 supports some function, variable, and type attributes that were supported in Arm Compiler 5. Other attributes are not supported, or have an alternate implementation.



Note

This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

Arm Compiler 5 and Arm Compiler for Embedded 6 support the following attributes. These attributes do not require modification in your code:



Note

The `__declspec` keyword is deprecated.

- `__attribute__((aligned(<n>)))`

- `__attribute__((const))`
- `__attribute__((deprecated))`
- `__attribute__((noinline))`
- `__declspec(noinline)`
- `__attribute__((nonnull))`
- `__attribute__((noreturn))`
- `__declspec(noreturn)`
- `__attribute__((nothrow))`
- `__declspec(nothrow)`
- `__attribute__((pcs("<calling convention>")))`
- `__attribute__((pure))`
- `__attribute__((unused))`
- `__attribute__((used))`
- `__attribute__((visibility))`
- `__attribute__((weak))`
- `__attribute__((weakref))`

The following Arm Compiler 5 attributes are not supported by Arm Compiler for Embedded 6:

- `__attribute__((nomerge))`
- `__attribute__((notailcall))`

However, because Arm Compiler for Embedded 6 is built on LLVM technology and preserves the functionality of that technology where possible, you might consider using the following [COMMUNITY] (open-source Clang) features instead:

- `__attribute__((nomerge))`
- `__attribute__((not_tail_called))`

[COMMUNITY] features are not supported by Arm and are used at your own risk. You are responsible for making sure that any generated code using [COMMUNITY] features is operating correctly. For more information, see [Support level definitions](#).

`__declspec` attributes

Though Arm Compiler for Embedded 6 supports certain `__declspec` attributes, Arm recommends using `__attribute__` where available.

Table 4-3: Support for `__declspec` attributes

declspec supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
<code>__declspec(dllimport)</code>	None. There is no support for BPABI linking models.
<code>__declspec(dllexport)</code>	None. There is no support for BPABI linking models.

declspec supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
<code>__declspec(noinline)</code>	<code>__attribute__((noinline))</code>
<code>__declspec(noreturn)</code>	<code>__attribute__((noreturn))</code>
<code>__declspec(nothrow)</code>	<code>__attribute__((nothrow))</code>
<code>__declspec(notshared)</code>	None. There is no support for BPABI linking models.
<code>__declspec(thread)</code>	<code>__thread</code>

`__attribute__((always_inline))`

Arm Compiler 5 and Arm Compiler for Embedded 6 support `__attribute__((always_inline))`. However, this attribute might require modification in your code.

When using Arm Compiler 5, `__attribute__((always_inline))` affects the linkage of the function according to the inline semantics of the source language.

When using Arm Compiler for Embedded 6, `__attribute__((always_inline))` does not force inlining, but is a hint to the compiler to inline that function. `armclang` still decides whether to inline the function. You can also use the keyword `inline` or `__inline__` (for C90). To determine which functions have been inlined and which ones could not be inlined, you can consider using `-Rpass=inline` and the [COMMUNITY] option `-Rpass-missed=inline`. For more information, see:

- [-Rpass](#).
- `__attribute__((always_inline))`.
- [Inline functions](#)
- [Inlining functions](#).

`__attribute__((section("name")))`

Arm Compiler 5 and Arm Compiler for Embedded 6 support `__attribute__((section("<name>")))`. However, this attribute might require modification in your code.

When using Arm Compiler 5, section names do not need to be unique. Therefore, you could use the same section name to create different section types.

When using Arm Compiler for Embedded 6, you must ensure that variables of different types do not have the same section name.



Note

Arm Compiler for Embedded 6 supports multiple sections with the same section name only if you use the `.section` assembly directive with a unique ID. For more information, see [Section directives](#).

If you use the same section name for another section or symbol without a unique ID, then `armclang` integrated assembler merges the sections and gives the merged section the flags of the first section it discovers with that name.

Migrating `__attribute__((at(address)))` and zero-initialized `__attribute__((section("name")))` from Arm Compiler 5 to Arm Compiler for Embedded 6

Arm Compiler 5 supports the following attributes, which Arm Compiler for Embedded 6 does not support:

- `__attribute__((at(<address>)))` to specify the absolute address of a function or variable.
- `__attribute__((at(<address>), zero_init))` to specify the absolute address of a zero-initialized variable.
- `__attribute__((section(<name>), zero_init))` to place a zero-initialized variable in a zero-initialized section with the given <name>.
- `__attribute__((zero_init))` to generate an error if the variable has an initializer.

The following table shows migration paths for these features using Arm Compiler for Embedded 6 supported features:

Table 4-4: Migrating `__attribute__((at(<address>)))` and zero-initialized `__attribute__((section("<name>")))`

Arm Compiler 5 attribute	Arm Compiler for Embedded 6 attribute	Description
<code>__attribute__((at(<address>)))</code>	<code>__attribute__((section(".ARM.__at_<address>")))</code>	Although <code>armlink</code> in Arm Compiler for Embedded 6 supports the placement of sections in the form of <code>.ARM.__at_<address></code> , the implementation is not the same as in Arm Compiler 5. Note: The Arm Compiler for Embedded 6 attribute only supports a string to specify the section. To use an arithmetic expression, see Supporting arithmetic expressions in the <code>at(address)</code> attribute in Arm Compiler for Embedded 6 .
<code>__attribute__((at(<address>), zero_init))</code>	<code>__attribute__((section(".bss.ARM.__at_<address>")))</code>	<code>armlink</code> in Arm Compiler for Embedded 6 supports the placement of zero-initialized sections in the form of <code>.bss.ARM.__at_<address></code> . The <code>.bss</code> prefix is case-sensitive and must be all lowercase.
<code>__attribute__((section(<name>), zero_init))</code>	<code>__attribute__((section(".bss.<name>")))</code>	<name> is a name of your choice. The <code>.bss</code> prefix is case-sensitive and must be all lowercase.
<code>__attribute__((zero_init))</code>	Arm Compiler for Embedded 6 by default places zero-initialized variables in a <code>.bss</code> section. However, there is no equivalent to generate an error when you specify an initializer.	If the variable has an initializer, Arm Compiler 5 generates an error. Otherwise, it places the zero-initialized variable in a <code>.bss</code> section.

Supporting arithmetic expressions in the at(address) attribute in Arm Compiler for Embedded 6

The at(<address>) attribute in Arm Compiler 5 supports arithmetic expressions to specify the section, for example:

```
#include <stdint.h>

/* Define the variable and place at calculated address directly */
__attribute__((at(0x30000000 + 0x4000))) volatile uint32_t foo = 0x11223344;
```

Arm Compiler for Embedded 6 does not support arithmetic expressions with `__attribute__((section(".ARM.__at_<address>")))`. To do the equivalent in Arm Compiler for Embedded 6, you must use a pointer-based approach as follows:

- 1. Use pointer arithmetic to define a pointer that points to the required address.
- 2. The value pointed to by the pointer is not automatically initialized. Instead, you must initialize the value manually within a function.

For example:

```
#include <stdio.h>
#include <stdint.h>

/* 1. Define pointer to point to a calculated address */
volatile uint32_t * const foo_ptr = (volatile uint32_t *) (0x30000000 + 0x4000);

int main(void)
{
    *foo_ptr = 0x11223344; /* 2. Initialize the value pointed to by the pointer */
    printf("%p: %8x\n", foo_ptr, *foo_ptr); /* Use the pointer as needed */

    return 0;
}
```

Related information

- [Placing functions and data in a named section](#)
- [Placement of __at sections at a specific address](#)

4.3 Language extension compatibility: pragmas

Arm® Compiler for Embedded 6 provides support for some pragmas that are supported in Arm Compiler 5. Other pragmas are not supported, or must be replaced with alternatives.

The following table lists some of the commonly used pragmas that are supported by Arm Compiler 5 but are not supported by Arm Compiler for Embedded 6. Replace any instances of these pragmas in your code with the recommended alternative.

Table 4-5: Pragma language extensions that must be replaced

Pragma supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
#pragma import (<symbol>)	__asm(".global <symbol>\\n\\t");

Pragma supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
<pre>#pragma anon_unions</pre> <pre>#pragma no_anon_unions</pre>	<p>In C, anonymous structs and unions are a C11 extension which is enabled by default in <code>armclang</code>. If you specify the <code>-pedantic</code> option, the compiler emits warnings about extensions do not match the specified language standard. For example:</p> <pre>armclang --target=aarch64-arm-none-eabi -c -pedantic --std=c90 test.c</pre> <pre>test.c:3:5: warning: anonymous structs are a C11 extension [-Wc11-extensions]</pre> <p>In C++, anonymous unions are part of the language standard, and are always enabled. However, anonymous structs and classes are an extension. If you specify the <code>-pedantic</code> option, the compiler emits warnings about anonymous structs and classes. For example:</p> <pre>armclang --target=aarch64-arm-none-eabi -c -pedantic -xc++ test.c</pre> <pre>test.c:3:5: warning: anonymous structs are a GNU extension [-Wgnu-anonymous-struct]</pre> <p>Introducing anonymous unions, struct and classes using a <code>typedef</code> is a separate extension in <code>armclang</code>, which must be enabled using the <code>-fms-extensions</code> option.</p>
<pre>#pragma arm</pre> <pre>#pragma thumb</pre>	<p><code>armclang</code> provides the <code>__attribute__((target("arm" "thumb")))</code> function attribute to specify the instruction set for a function. You can also use the command-line options <code>-marm</code> and <code>-mthumb</code> to specify the instruction set for a whole file.</p>
<pre>#pragma arm section</pre>	<pre>#pragma clang section</pre> <p>In Arm Compiler 5, the section types you can use this pragma with are <code>rodata</code>, <code>rdata</code>, <code>zidata</code>, and <code>code</code>. In Arm Compiler for Embedded 6, the equivalent section types are <code>rodata</code>, <code>data</code>, <code>bss</code>, and <code>text</code> respectively.</p>

Pragma supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
<pre>#pragma diag_default #pragma diag_suppress #pragma diag_remark #pragma diag_warning #pragma diag_error</pre>	<p>The following pragmas provide equivalent functionality for <code>diag_suppress</code>, <code>diag_warning</code>, and <code>diag_error</code>:</p> <ul style="list-style-type: none"> <code>#pragma clang diagnostic ignored "-Wmultichar"</code> <code>#pragma clang diagnostic warning "-Wmultichar"</code> <code>#pragma clang diagnostic error "-Wmultichar"</code> <p>Note that these pragmas use <code>armclang</code> diagnostic groups, which do not have a precise mapping to <code>armcc</code> diagnostic tags.</p> <p><code>armclang</code> has no equivalent to <code>diag_default</code> or <code>diag_remark</code>. <code>diag_default</code> can be replaced by wrapping the change of diagnostic level with <code>#pragma clang diagnostic push</code> and <code>#pragma clang diagnostic pop</code>, or by manually returning the diagnostic to the default level.</p> <p>There is an additional diagnostic level supported in <code>armclang</code>, <code>fatal</code>, which causes compilation to fail without processing the rest of the file. You can set this as follows:</p> <pre>#pragma clang diagnostic fatal "-Wmultichar"</pre>
<pre>#pragma exceptions_unwind #pragma no_exceptions_unwind</pre>	<p><code>armclang</code> does not support these pragmas.</p> <p>Use the <code>__attribute__((nothrow))</code> function attribute instead.</p>
<pre>#pragma GCC system_header</pre>	<p>This pragma is supported by both <code>armcc</code> and <code>armclang</code>, but <code>#pragma clang system_header</code> is the preferred spelling in <code>armclang</code> for new code.</p>
<pre>#pragma hdrstop #pragma no_pch</pre>	<p><code>armclang</code> does not support these pragmas.</p>
<pre>#pragma import(__use_no_semihosting) #pragma import(__use_no_semihosting_swi)</pre>	<p><code>armclang</code> does not support these pragmas. However, in C code, you can replace these pragmas with:</p> <pre>__asm(".global __use_no_semihosting\n\t");</pre>
<pre>#pragma import(__use_two_region_memory)</pre>	<p>This pragma is required for scatter-loading when the stack and heap are separate. <code>armclang</code> does not support this pragma. However, in C code, you can replace this pragma with:</p> <pre>__asm(".global __use_two_region_memory\n\t");</pre>
<pre>#pragma inline #pragma no_inline</pre>	<p><code>armclang</code> does not support these pragmas. However, inlining can be disabled on a per-function basis using the <code>__attribute__((noinline))</code> function attribute.</p> <p>The default behavior of both <code>armcc</code> and <code>armclang</code> is to inline functions when the compiler considers this worthwhile, and this is the behavior selected by using <code>#pragma inline</code> in <code>armcc</code>. To force a function to be inlined in <code>armclang</code>, use the <code>__attribute__((always_inline))</code> function attribute.</p>

Pragma supported by Arm Compiler 5	Recommended Arm Compiler for Embedded 6 alternative
#pragma Onum #pragma Ospace #pragma Otime	armclang does not support changing optimization options within a file. Instead these must be set on a per-file basis using command-line options.
#pragma pop #pragma push	<p>armclang does not support these pragmas. Therefore, you cannot push and pop the state of all supported pragmas.</p> <p>However, you can push and pop the state of the diagnostic pragmas and the state of the pack pragma.</p> <p>To control the state of the diagnostic pragmas, use #pragma clang diagnostic push and #pragma clang diagnostic pop.</p> <p>To control the state of the pack pragma, use #pragma pack(push) and #pragma pack(pop).</p>
#pragma softfp_linkage	armclang does not support this pragma. Instead, use the __attribute__((pcs("aapcs")) function attribute to set the calling convention on a per-function basis, or use the -mfloat-abi=soft command-line option to set the calling convention on a per-file basis.
#pragma no_softfp_linkage	armclang does not support this pragma. Instead, use the __attribute__((pcs("aapcs-vfp")) function attribute to set the calling convention on a per-function basis, or use the -mfloat-abi=hard command-line option to set the calling convention on a per-file basis.
#pragma unroll[(<n>)] #pragma unroll_completely	<p>armclang supports these pragmas.</p> <p>The default for #pragma unroll (that is, with no iteration count specified) differs between armclang and armcc:</p> <ul style="list-style-type: none"> With armclang, the default is to fully unroll a loop. With armcc, the default is #pragma unroll(4).

Related information

[Compiler-specific Pragmas](#)

[Compiler-specific Function, Variable, and Type Attributes](#)

4.4 Language extension compatibility: intrinsics

Arm® Compiler for Embedded 6 provides support for some intrinsics that are supported in Arm Compiler 5.

The following table lists some of the commonly used intrinsics that are supported by Arm Compiler 5 and shows whether Arm Compiler for Embedded 6 supports them or provides an alternative. If there is no support in Arm Compiler for Embedded 6, you must replace them with suitable inline assembly instructions or calls to the standard library. To use the intrinsic in Arm Compiler for Embedded 6, you must include the appropriate header file. The ACLE intrinsics that are supported

by Arm Compiler 5 are described in the [Arm C Language Extensions 2.1](#). For more information on the ACLE intrinsics that are supported by Arm Compiler for Embedded 6, see the latest [Arm C Language Extensions](#).



- This is not an exhaustive list of all the intrinsics.
- The intrinsics provided in `<arm_compat.h>` are only supported for AArch32.

Table 4-6: Compiler intrinsic support in Arm Compiler for Embedded 6

Intrinsic in Arm Compiler 5	Function	Support in Arm Compiler for Embedded 6	Header file for Arm Compiler for Embedded 6
<code>__breakpoint</code>	Inserts a BKPT instruction.	Yes	<code>arm_compat.h</code>
<code>__cdp</code>	Inserts a coprocessor instruction.	Yes. In Arm Compiler for Embedded 6, the equivalent intrinsic is <code>__arm_cdp</code> .	<code>arm_acle.h</code>
<code>__clrex</code>	Inserts a CLREX instruction.	No	-
<code>__clz</code>	Inserts a CLZ instruction or equivalent routine.	Yes	<code>arm_acle.h</code>
<code>__current_pc</code>	Returns the program counter at this point.	Yes	<code>arm_compat.h</code>
<code>__current_sp</code>	Returns the stack pointer at this point.	Yes	<code>arm_compat.h</code>
<code>__isb</code>	Inserts ISB or equivalent.	Yes	<code>arm_acle.h</code>
<code>__disable_fiq</code>	Disables FIQ interrupts (Arm®v7 architecture only). Returns previous value of FIQ mask.	Yes	<code>arm_compat.h</code>
<code>__disable_irq</code>	Disable IRQ interrupts. Returns previous value of IRQ mask.	Yes	<code>arm_compat.h</code>
<code>__dmb</code>	Inserts a DMB instruction or equivalent.	Yes	<code>arm_acle.h</code>
<code>__dsb</code>	Inserts a DSB instruction or equivalent.	Yes	<code>arm_acle.h</code>
<code>__enable_fiq</code>	Enables fast interrupts.	Yes	<code>arm_compat.h</code>
<code>__enable_irq</code>	Enables IRQ interrupts.	Yes	<code>arm_compat.h</code>
<code>__fabs</code>	Inserts a VABS or equivalent code sequence.	No. We recommend using the standard C library function <code>fabs()</code> .	-
<code>__fabsf</code>	Single precision version of <code>__fabs</code> .	No. We recommend using the standard C library function <code>fabsf()</code> .	-
<code>__force_stores</code>	Flushes all external variables visible from this function, if they have been changed.	Yes	<code>arm_compat.h</code>
<code>__ldrex</code>	Inserts an appropriately sized Load Exclusive instruction.	No. This intrinsic is deprecated in ACLE 2.0.	-
<code>__ldrexd</code>	Inserts an LDREXD instruction.	No. This intrinsic is deprecated in ACLE 2.0.	-
<code>__ldrt</code>	Inserts an appropriately sized user-mode load instruction.	No	-

Intrinsic in Arm Compiler 5	Function	Support in Arm Compiler for Embedded 6	Header file for Arm Compiler for Embedded 6
<code>__memory_changed</code>	Is similar to <code>__force_stores</code> , but also reloads the values from memory.	Yes	<code>arm_compat.h</code>
<code>__nop</code>	Inserts a NOP or equivalent instruction that will not be optimized away. It also inserts a sequence point, and scheduling barrier for side-effecting function calls.	Yes	<code>arm_acle.h</code>
<code>__pld</code>	Inserts a PLD instruction, if supported.	Yes	<code>arm_acle.h</code>
<code>__pldw</code>	Inserts a PLDW instruction, if supported (Arm®v7 architecture with MP).	No. We recommend using <code>__pldx</code> described in the ACLE document.	<code>arm_acle.h</code>
<code>__pli</code>	Inserts a PLI instruction, if supported.	Yes	<code>arm_acle.h</code>
<code>__promise</code>	Compiler assertion that the expression always has a nonzero value. If asserts are enabled then the promise is checked at runtime by evaluating <code><expr></code> using <code>assert(<expr>)</code> .	Yes. However, you must <code>#include <assert.h></code> to use <code>__promise</code> . <code>__promise</code> has the same behavior as <code>assert()</code> unless at least one of <code>NDEBUG</code> or <code>_DO_NOT_LINK_PROMISE_WITH_ASSERT</code> is defined.	<code>assert.h</code>
<code>__qadd</code>	Inserts a saturating add instruction, if supported.	Yes	<code>arm_acle.h</code>
<code>__qdbl</code>	Inserts instructions equivalent to <code>qadd(val, val)</code> , if supported.	Yes	<code>arm_acle.h</code>
<code>__qsub</code>	Inserts a saturating subtract, or equivalent routine, if supported.	Yes	<code>arm_acle.h</code>
<code>__rbit</code>	Inserts a bit reverse instruction.	Yes	<code>arm_acle.h</code>
<code>__rev</code>	Insert a REV, or endian swap instruction.	Yes	<code>arm_acle.h</code>
<code>__return_address</code>	Returns value of LR when returning from current function, without inhibiting optimizations like inlining or tailcalling.	No. We recommend using inline assembly instructions.	-
<code>__ror</code>	Insert an ROR instruction.	Yes	<code>arm_acle.h</code>
<code>__schedule_barrier</code>	Create a sequence point without effecting memory or inserting NOP instructions. Functions with side effects cannot move past the new sequence point.	Yes	<code>arm_compat.h</code>
<code>__semlhost</code>	Inserts an SVC or BKPT instruction.	Yes	<code>arm_compat.h</code>
<code>__sev</code>	Insert a SEV instruction. Error if the SEV instruction is not supported.	Yes	<code>arm_acle.h</code>
<code>__sqrt</code>	Inserts a VSQRT instruction on targets with a VFP coprocessor.	No. We recommend using the C library functions.	<code>math.h</code>

Intrinsic in Arm Compiler 5	Function	Support in Arm Compiler for Embedded 6	Header file for Arm Compiler for Embedded 6
<code>__sqrtf</code>	Single precision version of <code>__sqrt</code> .	No. We recommend using the C library functions.	<code>math.h</code>
<code>__ssat</code>	Inserts an <code>SSAT</code> instruction. Error if the <code>SSAT</code> instruction is not supported.	Yes	<code>arm_acle.h</code>
<code>__strex</code>	Inserts an appropriately sized Store Exclusive instruction.	No. This intrinsic is deprecated in ACLE 2.0.	-
<code>__strexld</code>	Inserts a doubleword Store Exclusive instruction.	No. This intrinsic is deprecated in ACLE 2.0.	-
<code>__strt</code>	Insert an appropriately sized <code>STRT</code> instruction.	No	-
<code>__swp</code>	Inserts an appropriately sized <code>SWP</code> instruction.	Yes. However, the <code>SWP</code> instruction is deprecated, and we do not recommend the use of <code>__swp</code> .	<code>arm_acle.h</code>
<code>__usat</code>	Inserts a <code>USAT</code> instruction. Error if the <code>USAT</code> instruction is not supported.	Yes	<code>arm_acle.h</code>
<code>__wfe</code>	Inserts a <code>WFE</code> instruction. Error if the <code>WFE</code> instruction is not supported.	Yes	<code>arm_acle.h</code>
<code>__wfi</code>	Inserts a <code>WFI</code> instruction. Error if the <code>WFI</code> instruction is not supported.	Yes	<code>arm_acle.h</code>
<code>__yield</code>	Inserts a <code>YIELD</code> instruction. Error if the <code>YIELD</code> instruction is not supported.	Yes	<code>arm_acle.h</code>
Armv6 SIMD intrinsics	Inserts an Armv6 SIMD instruction.	No	-
ETSI intrinsics	35 intrinsic functions and 2 global variable flags specified in ETSI G729 used for speech encoding. These are provided in the Arm headers in <code>dspfns.h</code> .	No	-
C55x intrinsics	Emulation of selected TI C55x compiler intrinsics.	No	-
<code>__vfp_status</code>	Reads the FPSCR.	Yes	<code>arm_compat.h</code>
FMA intrinsics	Intrinsics for fused-multiply-add on the Cortex®-M4 or Cortex-A5 processor in c99 mode.	No	-

4.5 Diagnostics for pragma compatibility

Older `armcc` compiler versions supported many pragmas which are not supported by `armclang`, but which could change the semantics of code. When `armclang` encounters these pragmas, it generates diagnostic messages.

The following table shows which diagnostics are generated for each pragma type, and the diagnostic group to which that diagnostic belongs. `armclang` generates diagnostics as follows:

- Errors indicate use of an `armcc` pragma which could change the semantics of code.
- Warnings indicate use of any other `armcc` pragma which is ignored by `armclang`.
- Pragmas other than those listed are silently ignored.

Table 4-7: Pragma diagnostics

Pragma supported by older compiler versions	Default diagnostic type	Diagnostic group
<code>#pragma anon_unions</code>	Warning	<code>armcc-pragma-anon-unions</code>
<code>#pragma no_anon_unions</code>	Warning	<code>armcc-pragma-anon-unions</code>
<code>#pragma arm</code>	Error	<code>armcc-pragma-arm</code>
<code>#pragma arm section [<section_type_list>]</code>	Error	<code>armcc-pragma-arm</code>
<code>#pragma diag_default <tag>[,<tag>,...]</code>	Error	<code>armcc-pragma-diag</code>
<code>#pragma diag_error <tag>[,<tag>,...]</code>	Error	<code>armcc-pragma-diag</code>
<code>#pragma diag_remark <tag>[,<tag>,...]</code>	Warning	<code>armcc-pragma-diag</code>
<code>#pragma diag_suppress <tag>[,<tag>,...]</code>	Warning	<code>armcc-pragma-diag</code>
<code>#pragma diag_warning <tag>[,<tag>,...]</code>	Warning	<code>armcc-pragma-diag</code>
<code>#pragma exceptions_unwind</code>	Error	<code>armcc-pragma-exceptions-unwind</code>
<code>#pragma no_exceptions_unwind</code>	Error	<code>armcc-pragma-exceptions-unwind</code>
<code>#pragma GCC system_header</code>	None	-
<code>#pragma hdrstop</code>	Warning	<code>armcc-pragma-hdrstop</code>
<code>#pragma import <symbol_name></code>	Error	<code>armcc-pragma-import</code>
<code>#pragma inline</code>	Warning	<code>armcc-pragma-inline</code>
<code>#pragma no_inline</code>	Warning	<code>armcc-pragma-inline</code>
<code>#pragma no_pch</code>	Warning	<code>armcc-pragma-no-pch</code>
<code>#pragma O<num></code>	Warning	<code>armcc-pragma-optimization</code>
<code>#pragma once</code>	None	-
<code>#pragma Ospace</code>	Warning	<code>armcc-pragma-optimization</code>
<code>#pragma Otime</code>	Warning	<code>armcc-pragma-optimization</code>
<code>#pragma pack</code>	None	-
<code>#pragma pop</code>	Error	<code>armcc-pragma-push-pop</code>

Pragma supported by older compiler versions	Default diagnostic type	Diagnostic group
#pragma push	Error	armcc-pragma-push-pop
#pragma softfp_linkage	Error	armcc-pragma-softfp-linkage
#pragma no_softfp_linkage	Error	armcc-pragma-softfp-linkage
#pragma thumb	Error	armcc-pragma-thumb
#pragma weak <symbol>	None	-
#pragma weak <symbol1> = <symbol2>	None	-

In addition to the above diagnostic groups, there are the following additional diagnostic groups:

armcc-pragmas

Contains all of the above diagnostic groups.

unknown-pragmas

Contains diagnostics about pragmas which are not known to armclang, and are not in the above table.

pragmas

Contains all pragma-related diagnostics, including **armcc-pragmas** and **unknown-pragmas**.

Any non-fatal **armclang** diagnostic group can be ignored, upgraded, or downgraded using the following command-line options:

Suppress a group of diagnostics:

`-Wno-<diag-group>`

Upgrade a group of diagnostics to warnings:

`-W<diag-group>`

Upgrade a group of diagnostics to errors:

`-Werror=<diag-group>`

Downgrade a group of diagnostics to warnings:

`-Wno-error=<diag-group>`

Related information

[Language extension compatibility: pragmas](#) on page 54

4.6 C and C++ implementation compatibility

Arm® Compiler for Embedded 6 C and C++ implementation details differ from previous compiler versions.

The following table describes the C and C++ implementation detail differences.

Table 4-8: C and C++ implementation detail differences

Feature	Older versions of Arm Compiler	Arm Compiler for Embedded 6
Integer operations		
Shifts	<pre>int shifts > 0 && < 127 int left_shifts > 31 == 0 int right_shifts > 31 == 0 (for unsigned or positive) int right_shifts > 31 == -1 (for negative) long long shifts > 0 && < 63</pre>	<p>Warns when shift amount > width of type.</p> <p>You can use the <code>-Wshift-count-overflow</code> option to suppress this warning.</p>
Integer division	Checks that the sign of the remainder matches the sign of the numerator	The sign of the remainder is not necessarily the same as the sign of the numerator.
Floating-point operations		
Default standard	IEEE 754 standard, rounding to nearest representable value, exceptions disabled by default.	<p>All facilities, operations, and representations guaranteed by the IEEE standard are available in single and double-precision. Modes of operation can be selected dynamically at runtime.</p> <p>This is equivalent to the <code>--fpmode=ieee_full</code> option in older versions of Arm Compiler.</p>
<code>#pragma STDC FP_CONTRACT</code>	<code>#pragma STDC FP_CONTRACT</code>	Might affect code generation.
Unions, enums and structs		
Enum packing	Enums are implemented in the smallest integral type of the correct sign to hold the range of the enum values, except for when compiling in C++ mode with <code>--enum_is_int</code> .	By default enums are implemented as int, with long long used when required.
Allocation of bit-fields in containers	Allocation of bit-fields in containers.	A container is an object, aligned as the declared type. Its size is sufficient to contain the bit-field, but might be smaller or larger than the bit-field declared type.
Signedness of plain bit-fields	<p>Unsigned.</p> <p>Plain bit-fields declared without either the signed or unsigned qualifiers default to unsigned. The <code>--signed_bitfields</code> option treats plain bit-fields as signed.</p>	<p>Signed.</p> <p>Plain bit-fields declared without either the signed or unsigned qualifiers default to signed. There is no equivalent to either the <code>--signed_bitfields</code> or <code>--no_signed_bitfields</code> options.</p>
Arrays and pointers		
Casting between integers and pointers	No change of representation	<p>Converting a signed integer to a pointer type with greater bit width sign-extends the integer.</p> <p>Converting an unsigned integer to a pointer type with greater bit width zero-extends the integer.</p>
Misc C		
<code>sizeof(wchar_t)</code>	2 bytes	4 bytes

Feature	Older versions of Arm Compiler	Arm Compiler for Embedded 6
<code>size_t</code>	Defined as unsigned int, 32-bit.	Defined as unsigned int in 32-bit architectures, and unsigned long; in 64-bit architectures.
<code>ptrdiff_t</code>	Defined as signed int, 32-bit.	Defined as unsigned int in 32-bit architectures, and signed long in 64-bit architectures.
Misc C++		
C++ library	Rogue Wave Standard C++ Library	LLVM libc++ Library Note: When the C++ library is used in source code, there is limited compatibility between object code created with Arm Compiler for Embedded 6 and object code created with Arm Compiler 5. This also applies to indirect use of the C++ library, for example memory allocation or exception handling.
Implicit inclusion	If compilation requires a template definition from a template declared in a header file <code>xyz.h</code> , the compiler implicitly includes the file <code>xyz.cc</code> or <code>xyz.CC</code> .	Not supported.
Alternative template lookup algorithms	When performing referencing context lookups, name lookup matches against names from the instantiation context as well as from the template definition context.	Not supported.
Exceptions	Off by default, function unwinding on with <code>--exceptions</code> by default.	On by default in C++ mode. Note: For C++ code, <code>-fexceptions</code> has a large increase in the code size. If you use <code>-fno_exceptions</code> , then the code size is in the range of that created with Arm Compiler 5.
Translation		
Diagnostics messages format	<code>source-file, line-number :</code> <code>severity : error-code :</code> <code>explanation</code>	<code>source-file:line-number:char-number: description</code> <code>[diagnostic-flag]</code>
Environment		
Physical source file bytes interpretation	Current system locale dependent or set using the <code>--locale</code> command-line option.	UTF-8, either with or without the <i>Byte Order Mark</i> (BOM).

Related information

[Language extension compatibility: keywords](#) on page 47

[Language extension compatibility: attributes](#) on page 50

[Language extension compatibility: pragmas](#) on page 54

4.7 Compatibility of C++ objects

The compatibility of C++ objects compiled with Arm® Compiler 5 depends on the C++ libraries used.

Compatibility with objects compiled using Rogue Wave standard library headers

Arm Compiler for Embedded 6 does not support binary compatibility with objects compiled using the Rogue Wave standard library include files.

There are warnings at link time when objects are mixed. `L6869W` is reported if an object requests the Rogue Wave standard library. `L6870W` is reported when using an object that is compiled with Arm Compiler 5 with exceptions support.

The impact of mixing objects that have been compiled against different C++ standard library headers might include:

- Undefined symbol errors.
- Increased code size.
- Possible runtime errors.

If you have Arm Compiler for Embedded 6 objects that have been compiled with the legacy `--stdlib=legacy_cpplib` option then these objects use the Rogue Wave standard library and therefore might be incompatible with objects created using Arm Compiler 6.4 or later. To resolve these issues, you must recompile all object files with Arm Compiler 6.4 or later.

Compatibility with C++ objects compiled using Arm Compiler 5

The choice of C++ libraries at link time must match the choice of C++ include files at compile time for all input objects. Arm Compiler 5 objects that use the Rogue Wave C++ libraries are not compatible with Arm Compiler for Embedded 6 objects. Arm Compiler 5 objects that use C++ but do not make use of the Rogue Wave header files can be compatible with Arm Compiler for Embedded 6 objects that use `libc++` but this is not guaranteed.

Arm recommends using Arm Compiler for Embedded 6 for building the object files.

Compatibility of arrays of objects compiled using Arm Compiler 5

Arm Compiler for Embedded 6 is not compatible with objects from Arm Compiler 5 that use `operator new[]` and `delete[]`. Undefined symbol errors result at link time because Arm Compiler for Embedded 6 does not provide the helper functions that Arm Compiler 5 depends on. For example:

```
//construct.cpp:

class Foo
{
public:
    Foo() : x_(new int) { *x_ = 0; }
    void setX(int x) { *x_ = x; }
    ~Foo() { delete x_; }
private:
    int* x_;
```

```
};

void func(void)
{
    Foo* array;
    array = new Foo [10];
    array[0].setX(1);
    delete[] array;
}
```

Build this example with the Arm Compiler 5 compiler, `armcc`, and link with the Arm Compiler for Embedded 6 linker, `armlink`, using:

```
armcc -c construct.cpp -Ospace -O1 --cpu=cortex-a9
armlink construct.o -o construct.axf
```

The linker reports:

```
Error: L6218E: Undefined symbol __aeabi_vec_delete (referred from construct.o).
Error: L6218E: Undefined symbol __aeabi_vec_new_cookie_nodtor (referred from
construct.o).
```

To resolve these linker errors, you must use the Arm Compiler for Embedded 6 compiler, `armclang`, to compile all C++ files that use the `new[]` and `delete[]` operators.



You do not have to specify `--stdlib=libc++` for `armlink`, because this is the default and only option in Arm Compiler 6.4, and later.

Related information

[--stdlib](#)

5. Migrating from armasm to the armclang Integrated Assembler

Describes how to migrate assembly code from legacy `armasm` syntax to GNU syntax (used by `armclang`).



The `armasm` legacy assembler is deprecated, and it has not been updated since Arm® Compiler 6.10. Also, `armasm` does not support:

- Armv8.4-A or later architectures.
- Certain backported options in Armv8.2-A and Armv8.3-A.
- Assembling `svt` instructions.
- Armv8.1-M or later architectures, including MVE.
- All versions of the Armv8-R architecture.

As a reminder, `armasm` always reports the deprecation warning `A1950w`. To suppress this message, specify the `--diag_suppress=1950` option.

5.1 Migration of assembler command-line options from armasm to the armclang integrated assembler

Arm® Compiler for Embedded 6 provides many command-line options, including most Clang command-line options as well as several Arm-specific options.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).



The following GNU assembly directives are [COMMUNITY] features:

- `.eabi_attribute Tag_ABI_PCS_RO_data, <value>`
- `.eabi_attribute Tag_ABI_PCS_R9_use, <value>`
- `.eabi_attribute Tag_ABI_PCS_RW_data, <value>`
- `.eabi_attribute Tag_ABI_VFP_args, <value>`
- `.eabi_attribute Tag_CPU_unaligned_access, <value>`
- `.ident`
- `.protected`

- `.section .note.GNU-stack, "x"`
- `-Wa,--noexecstack`
- `-Wa,-L`
- `-Wa,-defsym,<symbol>=<value>`

The following table describes the most common `armasm` command-line options, and shows the equivalent options for the `armclang` integrated assembler.

Additional information about command-line options is available:

- The *Arm Compiler for Embedded Reference Guide* provides more detail about the command-line options.
- For a full list of Clang command-line options, consult the Clang and LLVM documentation.

Table 5-1: Comparison of command-line options in `armasm` and the `armclang` integrated assembler

armasm option	armclang integrated assembler option	Description
<code>--arm_only</code>	No equivalent.	Enforces A32 instructions only.
<code>--apcs=/nointerwork</code>	No equivalent.	Specifies that the code in the input file can interwork between A32 and T32 safely. Interworking is always enabled in Arm Compiler for Embedded 6.
<code>--apcs=/ropi,</code> <code>--apcs=/noropi</code>	No direct equivalent.	With <code>armasm</code> , the options specify whether the code in the input file is Read-Only Position Independent (ROPI) code. With the <code>armclang</code> integrated assembler, use the GNU assembly <code>.eabi_attribute</code> directive instead. To specify that the code is ROPI code, use the directive as follows: <code>.eabi_attribute Tag_ABI_PCS_RO_data, 1</code> The code is marked as not ROPI code by default.
<code>--apcs=/rwpi,</code> <code>--apcs=/norwpi</code>	No direct equivalent.	With <code>armasm</code> , the options specify whether the code in the input file is Read/Write Position Independent (RWPI) code. With the <code>armclang</code> integrated assembler, use the GNU assembly <code>.eabi_attribute</code> directive instead. To specify that the code is RWPI code, use the directive as follows: <code>.eabi_attribute Tag_ABI_PCS_R9_use, 1</code> <code>.eabi_attribute Tag_ABI_PCS_RW_data, 2</code> The code is marked as not RWPI code by default.

armasm option	armclang integrated assembler option	Description
--apcs=/hardfp, --apcs=/softfp	No direct equivalent.	<p>With armasm, the options set attributes in the object file to request hardware or software floating-point linkage.</p> <p>With the armclang integrated assembler, use the GNU assembly .eabi_attribute directive instead.</p> <p>To request hardware floating-point linkage, use the directive as follows:</p> <pre>.eabi_attribute Tag_ABI_VFP_args, 1</pre> <p>To request software floating-point linkage, use the directive as follows:</p> <pre>.eabi_attribute Tag_ABI_VFP_args, 0</pre>
--checkreglist, --diag_warning=1206	This is the default.	<p>Generates warnings if register lists in LDM and STM instructions are not provided in increasing register number order.</p> <p>Note: This warning cannot be suppressed or upgraded to an error.</p>
--comment_section, --no_comment_section	No direct equivalent.	<p>With armasm, the option controls the inclusion of a comment section .comment in object files.</p> <p>With the armclang integrated assembler, use the GNU assembly .ident directive to manually add a comment section.</p>
--debug, -g	-g	<p>Instructs the assembler to generate DWARF debug tables.</p> <p>With armasm, the default format for debug tables is DWARF 3. Named local labels are not preserved in the object file, unless the --keep option is used.</p> <p>With the armclang integrated assembler, the default format for debug tables is DWARF 4. Named local labels are always preserved in the object file. See the entry for --keep in this table for details.</p>
--diag_warning=1645	No equivalent.	<p>With armasm, the option enables warnings about instruction substitutions.</p> <p>With the armclang integrated assembler, instruction substitution support is limited. Where it is not supported, the assembler generates an error message.</p> <p>Use the armasm warning when migrating code to find instructions being substituted and perform the substitution manually.</p>

armasm option	armclang integrated assembler option	Description
<code>--diag_warning=1763</code>	No equivalent.	<p>With <code>armasm</code>, the option enables warnings about automatic generation of <code>IT</code> blocks when assembling T32 code (formerly Thumb code).</p> <p>With the <code>armclang</code> integrated assembler, automatic generation of <code>IT</code> blocks is disabled by default. The assembler generates an error message when assembling conditional instructions without an enclosing <code>IT</code> block. To enable automatic generation of <code>IT</code> blocks, use the command-line option <code>-mimplicit-it=always</code> or <code>-mimplicit-it=thumb</code>.</p>
<code>--dllexport_all</code>	No direct equivalent.	<p>With <code>armasm</code>, the option gives all exported global symbols <code>STV_PROTECTED</code> visibility in <code>ELF</code> rather than <code>STV_HIDDEN</code>, unless overridden by source directives.</p> <p>With the <code>armclang</code> integrated assembler, use the GNU assembly <code>.protected</code> directive to manually give exported symbols <code>STV_PROTECTED</code> visibility.</p>
<code>--execstack,</code> <code>--no_execstack</code>	<code>-Wa,--noexecstack</code> No direct equivalent for <code>--execstack.</code>	<p>With <code>armasm</code>, the option generates a <code>.note.GNU-stack</code> section marking the stack as either executable or non-executable.</p> <p>With the <code>armclang</code> integrated assembler, the equivalent option can be used to generate a <code>.note.GNU-stack</code> section marking the stack as non-executable.</p> <p>To generate such a section and mark the stack as executable, use the GNU assembly <code>.section</code> directive as follows:</p> <pre>.section .note.GNU-stack, "x"</pre> <p>The command-line option <code>-Wa,--noexecstack</code> overrides the use of the <code>.section</code> directive.</p>
<code>--keep</code>	No direct equivalent.	<p>With <code>armasm</code>, the option instructs the assembler to keep named local labels in the symbol table of the object file, for use by the debugger.</p> <p>With the <code>armclang</code> integrated assembler, named local labels defined without using the GNU assembly local symbol name prefix <code>.L</code> are always preserved in the object file.</p> <p>Use the command-line option <code>-Wa,-L</code> to automatically preserve all named local labels defined using the GNU assembly local symbol name prefix.</p>

armasm option	armclang integrated assembler option	Description
-M	-M	<p>Instructs the assembler to produce a list of makefile dependency lines suitable for use by a make utility.</p> <p>Note: Only dependencies visible to the preprocessor are included. Files added using the GNU assembler syntax <code>.incbin</code> or <code>.include</code> directives, or armasm syntax <code>INCBIN</code>, <code>INCLUDE</code>, or <code>GET</code> directives, are not included.</p> <p>Note: With the <code>armclang</code> integrated assembler, using this option with <code>-o</code> outputs the makefile dependency lines to the file specified. An object file is not produced.</p>
--mm	-MM	<p>Creates a single makefile dependency file, without the system header files.</p> <p>Note: Only dependencies visible to the preprocessor are included. Files added using the GNU assembler syntax <code>.incbin</code> or <code>.include</code> directives (or armasm syntax <code>INCBIN</code>, <code>INCLUDE</code>, or <code>GET</code> directives) are not included.</p> <p>Note: With the <code>armclang</code> integrated assembler, using this option with <code>-o</code> outputs the makefile dependency file to the file specified. An object file is not produced.</p>
--no_hide_all	-fvisibility=default	<p>Gives all exported and imported global symbols <code>STV_DEFAULT</code> visibility in <code>ELF</code> rather than <code>STV_HIDDEN</code>, unless overridden using source directives.</p>
--predefine "<directive>", --pd "<directive>"	-Wa,-defsym,<symbol>=<value>	<p>With <code>armasm</code>, the option instructs the assembler to pre-execute one of the <code>SETA</code>, <code>SETL</code>, or <code>SETS</code> directives as specified using <code><directive></code>.</p> <p>With the <code>armclang</code> integrated assembler, the option instructs the assembler to pre-define the symbol <code><symbol></code> with the value <code><value></code>. This GNU assembly <code>.set</code> directive can be used to change this value in the file being assembled.</p>
--reduce_paths, --no_reduce_paths	No direct equivalent.	<p>Windows systems impose a 260 character limit on file paths. Arm recommends that you avoid using long and deeply nested file paths, in preference to minimizing path lengths using the <code>armasm</code> option <code>--reduce_paths</code>, which only works on 32-bit Windows systems.</p>

armasm option	armclang integrated assembler option	Description
<code>--unaligned_access,</code> <code>--no_unaligned_access</code>	No direct equivalent.	<p>With <code>armasm</code>, the options instruct the assembler to set an attribute in the object file to enable or disable the use of unaligned accesses.</p> <p>With the <code>armclang</code> integrated assembler, use the GNU assembly <code>.eabi_attribute</code> directive instead.</p> <p>To enable the use of unaligned access, use the directive as follows:</p> <pre>.eabi_attribute Tag_CPU_unaligned_access, 1</pre> <p>To disable the use of unaligned access, use the directive as follows:</p> <pre>.eabi_attribute Tag_CPU_unaligned_access, 0</pre>
<code>--unsafe</code>	No direct equivalent.	<p>With <code>armasm</code>, the option enables instructions for architectures other than the target architecture to be assembled without error.</p> <p>With the <code>armclang</code> integrated assembler, use the GNU assembly <code>.inst</code> directive to generate such instructions.</p>

Related information

[GNU Binutils - Using `as`: `.section`](#)

5.2 Overview of differences between `armasm` and GNU syntax assembly code

`armasm` (for assembling legacy assembly code) uses `armasm` syntax assembly code.

`armclang` aims to be compatible with GNU syntax assembly code (that is, the assembly code syntax supported by the GNU assembler, `as`).

If you have legacy assembly code that you want to assemble with `armclang`, you must convert that assembly code from `armasm` syntax to GNU syntax.

The specific instructions and order of operands in your UAL syntax assembly code do not change during this migration process.

However, you need to make changes to the syntax of your assembly code. These changes include:

- The directives in your code.
- The format of labels, comments, and some types of literals.

- Some symbol names.
- The operators in your code.

The following examples show simple, equivalent, assembly code in both `armasm` and GNU syntax.

GNU syntax

```
// Simple GNU syntax example [1]
//
// Iterate round a loop 10 times, adding 1 to a register each time.

.section .text,"ax"      // [2]
.global main
.balign 4
.type main, %function
main:                    // [3]
    MOV     w5,#0x64      // W5 = 100  [4]
    MOV     w4,#0         // W4 = 0
    B       test_loop     // branch to test_loop
loop:
    ADD     w5,w5,#1      // Add 1 to W5
    ADD     w4,w4,#1      // Add 1 to W4
test_loop:
    CMP     w4,#0xa       // if W4 < 10, branch back to loop
    BLT     loop
.end                     // [5]
```

Example notes

[1] See [Comments](#).

[2] See [Sections](#).

[3] See [Labels](#).

[4] See [Numeric literals](#).

[5] See [Miscellaneous directives](#).

armasm syntax

```
; Simple armasm syntax example
;
; Iterate round a loop 10 times, adding 1 to a register each time.
AREA ||.text||, CODE, READONLY, ALIGN=2
ENTRY
main PROC
    MOV     w5,#0x64      ; W5 = 100
    MOV     w4,#0         ; W4 = 0
    B       test_loop     ; branch to test_loop
loop
    ADD     w5,w5,#1      ; Add 1 to W5
    ADD     w4,w4,#1      ; Add 1 to W4
test_loop
    CMP     w4,#0xa       ; if W4 < 10, branch back to loop
    BLT     loop
    ENDP
END
```

Related information

[Comments](#) on page 74
[Labels](#) on page 75
[Numeric local labels](#) on page 75
[Functions](#) on page 77
[Sections](#) on page 78
[Symbol naming rules](#) on page 80
[Numeric literals](#) on page 80
[Operators](#) on page 82
[Alignment](#) on page 82
[PC-relative addressing](#) on page 83
[Conditional directives](#) on page 85
[Data definition directives](#) on page 86
[Instruction set directives](#) on page 88
[Miscellaneous directives](#) on page 88
[Symbol definition directives](#) on page 90
[About the Unified Assembler Language](#)

5.3 Comments

A comment identifies text that the assembler ignores.

GNU syntax

GNU syntax assembly code provides two different methods for marking comments:

- The `/*` and `*/` markers identify multiline comments:

```
/* This is a comment
that spans multiple
lines */
```

- The `//` marker identifies the remainder of a line as a comment:

```
MOV R0,#16    // Load R0 with 16
```

armasm syntax

A comment is the final part of a source line. The first semicolon on a line marks the beginning of a comment except where the semicolon appears inside a string literal.

The end of the line is the end of the comment. A comment alone is a valid line.

For example:

```
; This whole line is a comment
```

```
; And also this line  
  
myProc: PROC  
    MOV     r1, #16      ; Load R0 with 16
```

Related information

[GNU Binutils - Using as: Comments](#)

5.4 Labels

Labels are symbolic representations of addresses. You can use labels to mark specific addresses that you want to refer to from other parts of the code.

GNU syntax

A label is written as a symbol that either begins in the first column, or has nothing but whitespace between the first column and the label. A label can appear either in a line on its own, or in a line with an instruction or directive. A colon ":" follows the label (whitespace is allowed between the label and the colon):

```
    MOV R0,#16  
loop:      // "loop" label on its own line  
    SUB R0,R0,#1  
    CMP R0,#0  
    BGT loop
```

```
    MOV R0,#16  
loop: SUB R0,R0,#1 // "loop" label in a line with an instruction  
    CMP R0,#0  
    BGT loop
```

armasm syntax

A label is written as a symbol beginning in the first column. A label can appear either in a line on its own, or in a line with an instruction or directive. Whitespace separates the label from any following instruction or directive:

```
    MOV R0,#16  
loop SUB R0,R0,#1 ; "loop" is a label  
    CMP R0,#0  
    BGT loop
```

Related information

[GNU Binutils - Using as: Labels](#)

5.5 Numeric local labels

Numeric local labels are a type of label that you refer to by a number rather than by name. Unlike other labels, the same numeric local label can be used multiple times and the same number can be used for more than one numeric local label.

GNU syntax

A numeric local label is a number in the range 0-99.

Numeric local labels follow the same syntax as all other labels.

Refer to numeric local labels using the following syntax:

<n>{f|b}

Where:

- <n> is the number of the numeric local label in the range 0-99.
- f and b instruct the armclang integrated assembler to search forwards and backwards respectively. There is no default. You must specify one of f or b.

For example, the following code implements an incrementing loop:

```
MOV    r4,#1      // r4=1
1:     ADD    r4,r4,#1  // Local label
      CMP    r4,#0x5  // Increment r4
      BLT    1b      // if r4 < 5...
      // ...branch backwards to local label "1"
```



GNU syntax assembly code does not provide mechanisms for restricting the scope of local labels.

armasm syntax

A numeric local label is a number in the range 0-99, optionally followed by a scope name corresponding to a ROUT directive.

Numeric local labels follow the same syntax as all other labels.

Refer to numeric local labels using the following syntax:

%[F|B][A|T]<n>[<route>]

Where:

- F and B instruct the legacy assembler to search forwards and backwards respectively. By default, the legacy assembler searches backwards first, then forwards.

- **a** and **T** instruct the legacy assembler to search all macro levels or only the current macro level respectively. By default, the assembler searches all macros from the current level to the top level, but does not search lower level macros.
- **<n>** is the number of the numeric local label in the range 0-99.
- **<rouname>** is an optional scope label corresponding to a **ROUT** directive. If **<rouname>** is specified in either a label or a reference to a label, the legacy assembler checks it against the name of the nearest preceding **ROUT** directive. If it does not match, the legacy assembler generates an error message and the assembly fails.

For example, the following code implements an incrementing loop:

```
1      MOV      r4,#1      ; r4=1
      ADD      r4,r4,#1    ; Local label
      CMP      r4,#0x5     ; Increment r4
      BLT      %b1         ; if r4 < 5...
                        ; ...branch backwards to local label "1"
```

Here is the same example using a **ROUT** directive to restrict the scope of the local label:

```
routA  ROUT      ; Start of "routA" scope
1routA MOV      r4,#1      ; r4=1
      ADD      r4,r4,#1    ; Local label
      CMP      r4,#0x9     ; Increment r4
      BLT      %b1routA    ; if r4 < 9...
                        ; ...branch backwards to local label "1routA"
routB  ROUT      ; Start of "routB" scope (and therefore end of "routA"
scope)
```

Related information

[GNU Binutils - Using as: Labels](#)

[ROUT directive](#)

5.6 Functions

Assemblers can identify the start of a function when producing DWARF call frame information for ELF.

GNU syntax

Use the **.type** directive to identify symbols as functions. For example:

```
.type myproc, "function"
myproc:
    // Procedure body
```

GNU syntax assembly code provides the `.func` and `.endfunc` directives. However, these are not supported by `armclang`. `armclang` uses the `.size` directive to set the symbol size:

```
.type myproc, "function"

myproc:
    // Procedure body
.Lmyproc_end0:
    .size myproc, .Lmyproc_end0-myproc
```



Functions must be typed to link properly.

armasm syntax

The `FUNCTION` directive marks the start of a function. `PROC` is a synonym for `FUNCTION`.

The `ENDFUNC` directive marks the end of a function. `ENDP` is a synonym for `ENDFUNC`.

For example:

```
myproc PROC

    ; Procedure body
    ENDP
```

Related information

[GNU Binutils - Using `as`: `.type`](#)

5.7 Sections

Sections are independent, named, indivisible chunks of code or data that are manipulated by the linker.

GNU syntax

The `.section` directive instructs the `armclang` integrated assembler to assemble a new code or data section.

Flags provide information about the section. Available section flags include the following:

- `a` specifies that the section is allocatable.
- `x` specifies that the section is executable.
- `w` specifies that the section is writable.
- `s` specifies that the section contains null-terminated strings.

For example:

```
.section mysection,"ax"
```

Not all `armasm` syntax `AREA` attributes map onto GNU syntax `.section` flags. For example, the `armasm` syntax `ALIGN` attribute corresponds to the GNU syntax `.balign` directive, rather than a `.section` flag:

```
.section mysection,"ax"  
.balign 8
```

When using Arm® Compiler 5, section names do not need to be unique. Therefore, you could use the same section name to create different section types.

Arm Compiler for Embedded 6 supports multiple sections with the same section name only if you specify a [unique ID](#). You must ensure that different section types either:

- Have a unique section name.
- Have a unique ID, if they have the same section name.



If you use the same section name for another section or symbol, without a unique ID, then integrated assembler gives an error.

```
.section test, "ax", %progbits  
nop  
  
.section test, "aw", %progbits  
.word 0
```

The integrated assembler gives an error when you assemble this example with:

```
armclang --target=arm-arm-none-eabi -c -mcpu=cortex-a8 err.s  
err.s:4:9: error: changed section flags for test, expected: 0x6  
    .section test, "aw", %progbits  
    ^
```

armasm syntax

The `AREA` directive instructs the legacy assembler to assemble a new code or data section.

Section attributes within the `AREA` directive provide information about the section. Available section attributes include the following:

- `CODE` specifies that the section contains machine instructions.
- `READONLY` specifies that the section must not be written to.
- `ALIGN=<n>` specifies that the section is aligned on a $2^{<n>}$ byte boundary

For example:

```
AREA mysection, CODE, READONLY, ALIGN=3
```



Note

The `ALIGN` attribute does not take the same values as the `ALIGN` directive. The `ALIGN=<n>` attribute on the `AREA` directive aligns on a $2^{<n>}$ byte boundary. The `ALIGN <n>` directive aligns on an `<n>`-byte boundary.

Related information

[GNU Binutils - Using as: .section](#)

5.8 Symbol naming rules

`armasm` syntax assembly code and GNU syntax assembly code use similar, but different naming rules for symbols.

Symbol naming rules which are common to both `armasm` syntax and GNU syntax include:

- Symbol names must be unique within their scope.
- Symbol names are case-sensitive, and all characters in the symbol name are significant.
- Symbols must not use the same name as built-in variable names or predefined symbol names.

Symbol naming rules which differ between `armasm` syntax and GNU syntax include:

- `armasm` syntax symbols must start with a letter or the underscore character "_".
- GNU syntax symbols must start with a letter, the underscore character "_", or a period ".".
- `armasm` syntax symbols use double bars to delimit symbol names containing non-alphanumeric characters (except for the underscore):

```
IMPORT ||Image$$ARM_LIB_STACKHEAP$$ZI$$Limit||
```

GNU syntax symbols do not require double bars:

```
.global Image$$ARM_LIB_STACKHEAP$$ZI$$Limit
```

Related information

[GNU Binutils - Using as: Symbol Names](#)

5.9 Numeric literals

armasm syntax assembly and GNU syntax assembly provide different methods for specifying some types of numeric literal.

Implicit shift operations

armasm syntax assembly allows immediate values with an implicit shift operation. For example, the `movk` instruction takes a 16-bit operand with an optional left shift. `armasm` accepts the instruction `MOVK x1, #0x40000`, converting the operand automatically to `MOVK x1, #0x4, LSL #16`.

GNU syntax assembly expects immediate values to be presented as encoded. The instruction `movk x1, #0x40000` results in the following message: `error: immediate must be an integer in range [0, 65535]`.

Hexadecimal literals

armasm syntax assembly provides two methods for specifying hexadecimal literals, the prefixes "&" and "0x".

For example, the following are equivalent:

```
ADD    r1, #0xAF
ADD    r1, #&AF
```

GNU syntax assembly only supports the "0x" prefix for specifying hexadecimal literals. Convert any "&" prefixes to "0x".

<n-base>_<n-digits> format

armasm syntax assembly lets you specify numeric literals using the following format:

<n-base>_<n-digits>

For example:

- `2_1101` is the binary literal 1101 (13 in decimal).
- `8_27` is the octal literal 27 (23 in decimal).

GNU syntax assembly does not support the <n-base>_<n-digits> format. Convert all instances to a supported numeric literal form.

For example:

```
ADD    r1, #2_1101
```

You could convert this instruction to:

```
ADD    r1, #13
```

or:

```
ADD    r1, #0xD
```

Related information
[GNU Binutils - Using as: Integers](#)

5.10 Operators

armasm syntax assembly and GNU syntax assembly provide different methods for specifying some operators.

The following table shows how to translate `armasm` syntax operators to GNU syntax operators.

Table 5-2: Operator translation

armasm syntax operator	GNU syntax operator
:OR:	
:EOR:	^
:AND:	&
:NOT:	~
:SHL:	<<
:SHR:	>>
:LOR:	
:LAND:	&&
:ROL:	No GNU equivalent
:ROR:	No GNU equivalent

Related information
[GNU Binutils - Using as: Infix Operators](#)

5.11 Alignment

Data and code must be aligned to appropriate boundaries.

For example, The T32 pseudo-instruction `ADR` can only load addresses that are word aligned, but a label within T32 code might not be word aligned. You must use an alignment directive to ensure four-byte alignment of an address within T32 code.

An alignment directive aligns the current location to a specified boundary by padding with zeros or `NOP` instructions.

**Note**

The integrated assembler sets a minimum alignment of 4 bytes for a `.text` section. However, if you define your own sections with the integrated assembler, then you must include the `.balign` directive to set the correct alignment. For a section containing T32 instructions, set the alignment to 2 bytes. For a section containing A32 instructions, set the alignment to 4 bytes.

GNU syntax

GNU syntax assembly provides the `.balign <n>` directive, which uses the same format as `ALIGN`.

Convert all instances of `ALIGN <n>` to `.balign <n>`.

**Note**

GNU syntax assembly also provides the `.align <n>` directive. However, the format of `<n>` varies from system to system. The `.balign` directive provides the same alignment functionality as `.align` with a consistent behavior across all architectures.

Convert all instances of `PRESERVE8` to `.eabi_attribute Tag_ABI_align_preserved, 1`.

armasm syntax

`armasm` syntax assembly provides the `ALIGN <n>` directive, where `<n>` specifies the alignment boundary in bytes. For example, the directive `ALIGN 128` aligns addresses to 128-byte boundaries.

`armasm` syntax assembly also provides the `PRESERVE8` directive. The `PRESERVE8` directive specifies that the current file preserves eight-byte alignment of the stack.

Related information

[GNU Binutils - Using as: ARM Machine Directives](#)

5.12 PC-relative addressing

`armasm` syntax assembly and GNU syntax assembly provide different methods for performing PC-relative addressing.

GNU syntax

GNU syntax assembly does not support the `{pc}` symbol. Instead, it uses the special dot `"."` character, as follows:

```
ADRP x0, .
```

armasm syntax

`armasm` syntax assembly provides the symbol `{pc}` to let you specify an address relative to the current instruction.

For example:

```
ADRP x0, {pc}
```

Related information
[GNU Binutils - Using as: The Special Dot Symbol](#)

5.13 Instruction substitutions

When the value of an Operand2 constant is not available with a given instruction, but its logical inverse or negation is available, then both `armasm` and `armclang` produce an equivalent instruction with the inverted or negated constant.

For more information, see [A32 and T32 instruction substitutions](#).

Substitutions when using `armasm`

To find instruction substitutions in code assembled using `armasm`, use the command-line option `--diag_warning=1645`.

Substitutions when using `armclang` integrated assembler

`armclang` does not generate a warning when instruction substitutions occur. You can disable this substitution using the `armclang` option `-mno-neg-immediates`.

Related information
[-mno-neg-immediates armclang option](#)

5.14 A32 and T32 pseudo-instructions

`armasm` supports several A32 and T32 pseudo-instructions. The support for the pseudo-instructions varies with the `armclang` integrated assembler.

More information about the A32 and T32 pseudo-instructions is available in the *Arm Compiler for Embedded Reference Guide*. The following table shows how to migrate the pseudo-instructions for use with the `armclang` integrated assembler:

Table 5-3: A32 and T32 pseudo-instruction migration

A32 and T32 pseudo-instruction	armclang integrated assembler equivalent
ADRLcond <Rd>, <label>	No equivalent. Use an ADR instruction if <i>label</i> is within the supported offset range. Use an LDR pseudo-instruction if <i>label</i> is outside the supported offset range for an ADR instruction.
CPYcond <Rd>, <Rm>	movcond <Rd>, <Rm>

A32 and T32 pseudo-instruction	armclang integrated assembler equivalent
LDRcond{.W} <Rt>, =<expr>	Identical.
LDRcond{.W} <Rt>, =<label_expr>	Identical.
MOV32cond <Rd>, <expr>	Use the following instruction sequence: movw{cond} Rd, #:lower16:expr movt{cond} Rd, #:upper16:expr
NEGcond <Rd>, <Rm>	rsbscond <Rd>, <Rm>, #0
UNDcond{.W} {#<expr>}	Use the following instruction for the A32 instruction set: udf{c}{q} {#}imm Use the following instruction for the T32 instruction set with 8-bit encoding: udf{c}{q} {#}imm Use the following instruction for the T32 instruction set with 16-bit encoding: udf{c}.w {#}imm

Related information

[ADRL pseudo-instruction](#)

5.15 Conditional directives

Conditional directives specify conditions that control whether or not to assemble a sequence of assembly code.

The following table shows how to translate `armasm` syntax conditional directives to GNU syntax directives:

Table 5-4: Conditional directive translation

armasm syntax directive	GNU syntax directive
IF	.if family of directives
IF :DEF:	.ifdef
IF :LNOT::DEF:	.ifndef
ELSE	.else
ELSEIF	.elseif
ENDIF	.endif

In addition to the change in directives shown, the following syntax differences apply:

- In `armasm` syntax, the conditional directives can use forward references. This is possible as `armasm` is a two-pass assembler. In GNU syntax, forward references are not supported, as the `armclang` integrated assembler only performs one pass over the main text.

If a forward reference is used with the `.ifdef` directive, the condition will always fail implicitly. Similarly, if a forward reference is used with the `.ifndef` directive, the condition will always pass implicitly.

- In `armasm` syntax, the maximum total nesting depth for directive structures such as `IF...ELSE...ENDIF` is 256. In GNU syntax, this limit is not applicable.

Related information

[GNU Binutils - Using `as`: `.if`](#)

5.16 Data definition directives

Data definition directives allocate memory, define data structures, and set initial contents of memory.

The following table shows how to translate `armasm` syntax data definition directives to GNU syntax directives:



This list only contains examples of common data definition assembly directives. It is not exhaustive.

Table 5-5: Data definition directives translation

armasm syntax directive	GNU syntax directive	Description
DCB	<code>.byte</code>	Allocate one-byte blocks of memory, and specify the initial contents.
DCW	<code>.hword</code>	Allocate two-byte blocks of memory, and specify the initial contents.
DCD	<code>.word</code>	Allocate four-byte blocks of memory, and specify the initial contents.
DCI	<code>.inst</code>	Allocate a block of memory in the code, and specify the opcode. In A32 code, this is a four-byte block. In T32 code, this can be a two-byte or four-byte block. <code>.inst.n</code> allocates a two-byte block and <code>.inst.w</code> allocates a four-byte block.
DCQ	<code>.quad</code>	Allocate eight-byte blocks of memory, and specify the initial contents.

armasm syntax directive	GNU syntax directive	Description
SPACE	.org	Allocate a zeroed block of memory. The armasm syntax SPACE directive allocates a zeroed block of memory with the specified size. The GNU assembly .org directive zeroes the memory up to the given address. The address must be greater than the address at which the directive is placed.

Example: Creating a 100-byte zeroed block of memory using the armasm syntax SPACE directive


The following example shows the armasm syntax and GNU syntax methods of creating a 100-byte zeroed block of memory using these directives:

```
; armasm syntax
; implementation

start_address  SPACE  0x100
```

Example: Creating a 100-byte zeroed block of memory using the GNU syntax .org directive

```
// GNU syntax implementation
start_address:
.org  start_address + 0x100
```



Note

If label arithmetic is not required, you can use the GNU assembly .space directive instead of the .org directive. However, Arm recommends using the .org directive wherever possible.

Example: Write a vector table in armasm syntax

```
Vectors
    LDR PC, Reset_Addr
    LDR PC, Undefined_Addr
    LDR PC, SVC_Addr
    LDR PC, Prefetch_Addr
    LDR PC, Abort_Addr
    B . ; Reserved vector
    LDR PC, IRQ_Addr
    LDR PC, FIQ_Addr

Reset_Addr    DCD    Reset_Handler
Undefined_Addr DCD    Undefined_Handler
SVC_Addr      DCD    SVC_Handler
Prefetch_Addr DCD    Prefetch_Handler
Abort_Addr    DCD    Abort_Handler
IRQ_Addr      DCD    IRQ_Handler
FIQ_Addr      DCD    FIQ_Handler
```

Example: Rewrite a vector table in GNU syntax

```
Vectors:
    ldr pc, Reset_Addr
```

```
        ldr pc, Undefined_Addr
        ldr pc, SVC_Addr
        ldr pc, Prefetch_Addr
        ldr pc, Abort_Addr
        b . // Reserved vector
        ldr pc, IRQ_Addr
        ldr pc, FIQ_Addr

Reset_Addr:
        .balign 4
        .word Reset_Handler
Undefined_Addr:
        .word Undefined_Handler
SVC_Addr:
        .word SVC_Handler
Prefetch_Addr:
        .word Prefetch_Handler
Abort_Addr:
        .word Abort_Handler
IRQ_Addr:
        .word IRQ_Handler
FIQ_Addr:
        .word FIQ_Handler
```

Related information
[GNU Binutils - Using as: .byte](#)

5.17 Instruction set directives

Instruction set directives instruct the assembler to interpret subsequent instructions as either A32 or T32 instructions.

The following table shows how to translate `armasm` syntax instruction set directives to GNU syntax directives:

Table 5-6: Instruction set directives translation

armasm syntax directive	GNU syntax directive	Description
ARM or CODE32	.arm or .code 32	Interpret subsequent instructions as A32 instructions.
THUMB or CODE16	.thumb or .code 16	Interpret subsequent instructions as T32 instructions.

Related information
[GNU Binutils - Using as: ARM Machine Directives](#)

5.18 Miscellaneous directives

Miscellaneous directives perform a range of different functions.



This topic includes descriptions of [COMMUNITY] features. See [Support level definitions](#).

The following table shows how to translate `armasm` syntax miscellaneous directives to GNU syntax directives:

Table 5-7: Miscellaneous directives translation

armasm syntax directive	GNU syntax directive	Description
<code>foo EQU 0x1C</code>	<code>.equ foo, 0x1C</code>	Assigns a value to a symbol. Note the rearrangement of operands. <code>.equ</code> is a synonym for <code>.set</code> .
<code>EXPORT StartHere</code> <code>GLOBAL StartHere</code>	<code>.global StartHere</code>	Declares a symbol that can be used by the linker (that is, a symbol that is visible to the linker). <code>armasm</code> automatically determines the types of exported symbols. However, by default <code>armclang</code> declares symbols as the <code>%object</code> type. For a function call or function address you must specify the <code>%function</code> type using the <code>.type</code> directive, for example: <code>.type StartHere, %function</code> For more information, see Type directive . If the symbol type is incorrect, the linker outputs warnings of the form: Warning: L6437W: Relocation #RELA:1 in test.o(.text) with respect to <symbol>... Warning: L6318W: test.o(.text) contains branch to a non-code symbol <symbol>.
<code>GET file</code> <code>INCLUDE file</code>	<code>.include file</code>	Includes a file within the file being assembled.
<code>IMPORT foo</code>	<code>.global foo</code>	Provides the assembler with a name that is not defined in the current assembly.
<code>INCBIN</code>	<code>.incbin</code>	Includes a file within the file being assembled. The file is included verbatim. The assembler always emits a <code>\$d</code> (data) mapping symbol for the <code>.incbin</code> directive. [COMMUNITY]

armasm syntax directive	GNU syntax directive	Description
INFO <n>, "string"	.warning "string"	The INFO directive supports diagnostic generation on either pass of the assembly (specified by <n>). The .warning directive does not let you specify a particular pass, because the armclang integrated assembler only performs one pass.
ENTRY	armlink --entry=<location>	The ENTRY directive declares an entry point in an armasm legacy assembler file. armclang does not provide an equivalent directive. Use either the armclang option -e or the armlink option --entry=<location> to specify the initial entry point directly to the linker. If you need additional entry points in other objects, then use the armlink option --keep=<section_id> to identify them. This option ensures the sections for the additional entry points are not removed by unused section elimination.
END	.end	Marks the end of the assembly file.
PRESERVE8	.eabi_attribute Tag_ABI_align_preserved, 1	<p>Emits a build attribute which guarantees that the functions in the file preserve 8-byte stack alignment.</p> <p>Note: For armasm syntax assembly language source files, even if you do not specify the PRESERVE8 directive, armasm automatically emits the build attribute if all functions in the file preserve 8-byte stack alignment. For GNU syntax assembly language source files, the armclang integrated assembler does not automatically emit this build attribute. Therefore you must manually inspect and ensure that all functions in your GNU syntax assembly language source file preserve 8-byte stack alignment and then manually add the directive to the file.</p>

Related information

-e
--entry=location
--keep=section_id (armlink)
[GNU Binutils - Using as: .type](#)

5.19 Symbol definition directives

In armasm, symbol definition directives declare and set arithmetic, logical, or string variables. In the GNU assembler syntax, these directives define ELF symbols. There are no direct GNU syntax equivalents for armasm variables.

The following table shows how to translate armasm syntax symbol definition directives to GNU syntax directives:



This list only contains examples of common symbol definition directives. It is not exhaustive.

Table 5-8: Symbol definition directives translation

armasm syntax directive	GNU syntax directive	Description
foo RN r11	foo .req r11	Define an alias foo for register R11.
foo QN q5.I32 VADD foo, foo, foo	foo .req q5 VADD.I32 foo, foo, foo	Define an I32-typed alias foo for the quad-precision register Q5. When using the <code>armasm</code> syntax, you can specify a typed alias for quad-precision registers. The example defines an I32-typed alias foo for the quad-precision register Q5. When using GNU syntax, you must specify the type on the instruction rather than on the register. The example specifies the I32 type on the VADD instruction.
foo DN d2.I32 VADD foo, foo, foo	foo .req d2 VADD.I32 foo, foo, foo	Define an I32-typed alias foo for the double-precision register D2. When using the <code>armasm</code> syntax, you can specify a typed alias for double-precision registers. The example defines an I32-typed alias foo for the double-precision register D2. When using GNU syntax, you must specify the type on the instruction rather than on the register. The example specifies the I32 type on the VADD instruction.

Related information

[GNU Binutils - Using as: ARM Machine Directives](#)

5.20 Migration of armasm macros to integrated assembler macros

The `armclang` integrated assembler provides similar macro features to those provided by `armasm`. The macro syntax is based on GNU assembler macro syntax.

Additional information about macro features is available:

- The *Arm Compiler for Embedded Reference Guide* provides more detail about the macro directives supported, and examples of using macros.
- The *GNU Binutils - Using as* document provides more detail about GNU assembly macro directives.

Macro directive features

The following table describes the most common `armasm` macro directive features, and shows the equivalent features for the `armclang` integrated assembler.

Table 5-9: Comparison of macro directive features provided by `armasm` and the `armclang` integrated assembler

armasm feature	armclang integrated assembler feature	Description
MACRO, MEND directives	.macro, .endm directives	Directives to mark the start and end of the definition of a macro.
{ \$label } macro parameter	Use a normal macro parameter.	Optionally define an internal label to use within the macro.
{ \$cond } macro parameter	Use a normal macro parameter.	Optionally define a condition code to use within the macro.
{ \$parameter{ , \$parameter } ... } custom macro parameter specification	{ parameter{ :type } { , parameter{ :type } } . .. } custom macro parameter and parameter type specification	<p>With <code>armasm</code>, any number of custom macro parameters can be defined. Unspecified parameters are substituted with an empty string.</p> <p>With the <code>armclang</code> integrated assembler, the custom macro parameters can optionally have a parameter type <code>type</code>. This can be either <code>req</code> or <code>vararg</code>. Unspecified parameters are substituted with an empty string.</p> <p>The <code>req</code> type specifies a required parameter. The assembler generates an error when instantiating a macro if a required parameter is missing and a default value is not available.</p> <p>The <code>vararg</code> type collects all remaining parameters as one parameter. It can only be used as the last parameter within the list of parameters for a given macro. Only one <code>vararg</code> parameter can be specified.</p>
MEXIT directive	.exitm directive	Exit early from a macro definition.

armasm feature	armclang integrated assembler feature	Description
IF, ELSE, ELIF, ENDIF conditional assembly directives	.if family of directives, and the .else, .elseif, .endif directives	<p>The directives allow conditional assembly of instructions.</p> <p>With armasm, the conditional assembly directives use a logical expression that evaluates to either TRUE or FALSE as their controlling expression.</p> <p>With the armclang integrated assembler, multiple variants of the GNU assembly .if directive are available, referred to as the .if family of directives.</p> <p>For the .if and .elseif directives, the controlling expression is a logical expression that evaluates to either TRUE or FALSE.</p> <p>For other directives in the .if family of directives, the controlling expression is an implicit part of the directive used, and varies for each such directive.</p>
WHILE, WEND directives	.rept, .endr directives	<p>The directives allow a sequence of instructions or directives to be assembled repeatedly.</p> <p>With armasm, the WHILE directive uses a logical expression that evaluates to either TRUE or FALSE as its controlling expression. The sequence enclosed between a WHILE and WEND directive pair is assembled until the logical expression evaluates to FALSE.</p> <p>With the armclang integrated assembler, the GNU assembly .rept directive takes a fixed number of repetitions as a parameter. The sequence enclosed between a .rept and .endr directive pair is assembled the specified fixed number of times.</p> <p>To replicate the effect of using a logical expression to repeatedly assemble a code sequence, the .rept directive can be used within a macro. See the example provided later in this section.</p>

armasm feature	armclang integrated assembler feature	Description
ASSERT directive	Use a combination of the .if family of directives and the .error directive.	<p>With armasm, the ASSERT directive generates an error message during assembly if a given assertion is false. A logical expression that evaluates to TRUE or FALSE is used as the assertion.</p> <p>With the armclang integrated assembler, this functionality can be achieved by using a GNU assembly directive from the .if family of directives to conditionally display an error message during assembly using the GNU assembly .error directive.</p> <p>Macros can be created to simplify this process. See the example provided later in this section.</p>

Notable differences between armasm macro syntax and GNU macro syntax

The following syntax restrictions apply to GNU macro syntax in addition to the differences due to macro directives:

- In **armasm** macro syntax, using the pipe character `\|` as the parameter value when instantiating a macro selects the default value of the parameter. In GNU macro syntax, leaving the parameter value empty when instantiating a macro selects the default value of the parameter. If a default value is not specified in the macro definition, an empty string is used.
- In **armasm** macro syntax, a dot can be used between a parameter and subsequent text, or another parameter, if a space is not required in the expansion. In GNU macro syntax, a set of parentheses `()` can be used between a parameter and subsequent text, if a space is not required in the expansion. There is no need to separate a parameter from another subsequent parameter.
- Although the integrated assembler is case-insensitive to register names, the GNU assembly **.ifc** directive always performs a case-sensitive comparison. Manually check that the register names use the same case-sense when comparing them using the directive.

Migration of macro examples provided in the Arm Compiler for Embedded Reference Guide

NOT EQUALS assertion - armasm syntax implementation:

```
ASSERT arg1 <> arg2
```

NOT EQUALS assertion - GNU syntax implementation:

```
/* Helper macro to replicate ASSERT <> directive
   functionality from armasm.
   Displays error if NE assertion fails. */
.macro assertNE arg1:req, arg2:req, message:req
.ifc \arg1, \arg2
.error "\message"
.endif
.endm
```

Unsigned integer division macro - armasm syntax implementation

The macro takes the following parameters:

\$Bot

The register that holds the divisor.

\$Top

The register that holds the dividend before the instructions are executed. After the instructions are executed, it holds the remainder.

\$Div

The register where the quotient of the division is placed. It can be `NULL` ("") if only the remainder is required.

\$Temp

A temporary register used during the calculation.

```
MACRO
$Lab    DivMod    $Div,$Top,$Bot,$Temp
        ASSERT    $Top <> $Bot        ; Produce an error message if the
        ASSERT    $Top <> $Temp        ; registers supplied are
        ASSERT    $Bot <> $Temp        ; not all different
        IF        "$Div" <> ""
            ASSERT    $Div <> $Top        ; These three only matter if $Div
            ASSERT    $Div <> $Bot        ; is not null ("")
            ASSERT    $Div <> $Temp        ;
        ENDIF
$Lab    MOV        $Temp, $Bot          ; Put divisor in $Temp
        CMP        $Temp, $Top, LSR #1  ; double it until
90      MOVLS      $Temp, $Temp, LSL #1  ; 2 * $Temp > $Top
        CMP        $Temp, $Top, LSR #1
        BLS        %b90                ; The b means search backwards
        IF        "$Div" <> ""
            ; Omit next instruction if $Div
            ; is null
            MOV        $Div, #0          ; Initialize quotient
        ENDIF
91      CMP        $Top, $Temp            ; Can we subtract $Temp?
        SUBCS      $Top, $Top,$Temp      ; If we can, do so
        IF        "$Div" <> ""
            ; Omit next instruction if $Div
            ; is null
            ADC        $Div, $Div, $Div   ; Double $Div
        ENDIF
        MOV        $Temp, $Temp, LSR #1 ; Halve $Temp,
        CMP        $Temp, $Bot          ; and loop until
        BHS        %b91                ; less than divisor
        MEND
```

Unsigned integer division macro - GNU syntax implementation

The macro takes the following parameters:

Lab

A label to mark the start of the code. This parameter is required.

BotRegNum

The register number for the register that holds the divisor. This parameter is required.

TopRegNum

The register number for the register that holds the dividend before the instructions are executed. After the instructions are executed, it holds the remainder. This parameter is required.

DivRegNum

The register number for the register where the quotient of the division is placed. It can be NULL ("") if only the remainder is required. This parameter is optional.

TempRegNum

The register number for a temporary register used during the calculation. This parameter is required.

```
.macro DivMod Lab:req, DivRegNum, TopRegNum:req, BotRegNum:req,
TempRegNum:req
    assertNE \TopRegNum, \BotRegNum, "Top and Bottom cannot be the same
register"
    assertNE \TopRegNum, \TempRegNum, "Top and Temp cannot be the same
register"
    assertNE \BotRegNum, \TempRegNum, "Bottom and Temp cannot be the same
register"
    .ifnb \DivRegNum
        assertNE \DivRegNum, \TopRegNum, "Div and Top cannot be the same
register"
        assertNE \DivRegNum, \BotRegNum, "Div and Bottom cannot be the same
register"
        assertNE \DivRegNum, \TempRegNum, "Div and Temp cannot be the same
register"
    .endif
\Lab:
    mov     r\TempRegNum, r\BotRegNum          // Put divisor in r\TempRegNum
    cmp     r\TempRegNum, r\TopRegNum, lsr #1  // double it until
90:
    movls   r\TempRegNum, r\TempRegNum, lsl #1 // 2 * r\TempRegNum > r
\TopRegNum
    cmp     r\TempRegNum, r\TopRegNum, lsr #1
    bls     90b                               // The 'b' means search backwards
    .ifnb \DivRegNum                          // Omit next instruction if r\DivRegNum is null
        mov r\DivRegNum, #0                    // Initialize quotient
    .endif
91:
    cmp     r\TopRegNum, r\TempRegNum          // Can we subtract r
\TempRegNum?
    subcs   r\TopRegNum, r\TopRegNum, r\TempRegNum // If we can, then do so
    .ifnb \DivRegNum                          // Omit next instruction if r\DivRegNum is null
        adc r\DivRegNum, r\DivRegNum, r\DivRegNum // Double r\DivRegNum
    .endif
    mov     r\TempRegNum, r\TempRegNum, lsr #1 // Halve r\TempRegNum
    cmp     r\TempRegNum, r\BotRegNum          // and loop until
    bhs     91b                               // less than divisor
.endm
```

Notable differences from the `armasm` syntax implementation:

- A custom macro, `assertNE`, is used instead of the `armasm` directive `ASSERT`.
- Register numbers are used instead of registers as parameters. This is because the GNU assembly `.ifc` directive used for the `assertNE` assertions treats its operands as case-sensitive.
- The GNU assembly `.ifnb` directive is used to check if the parameter `DivRegNum` has been defined. In the `armasm` syntax implementation, the `armasm` directive `IF` is used.

Assembly-time diagnostics macro - armasm syntax implementation

```
MACRO                                ; Macro definition
diagnose $param1="default"           ; This macro produces
INFO    0,$param1                    ; assembly-time diagnostics
MEND                                     ; (on second assembly pass)
; macro expansion
diagnose                                ; Prints blank line at assembly-time
diagnose "hello"                       ; Prints "hello" at assembly-time
diagnose |                             ; Prints "default" at assembly-time
```

Assembly-time diagnostics macro - GNU syntax implementation

```
// macro definition
.macro diagnose, param1="default"
.warning "\param1"
.endm
// macro instantiation
.section "diagnoseMacro", "ax"
diagnose "" // Prints a warning with an empty string at assembly-
time
// Cannot print blank line as the .print directive is
not supported
diagnose "hello" // Prints a warning with the message "hello" at
assembly-time
diagnose // Prints a warning with the default message "default"
// at assembly-time
```

Notable differences from the `armasm` syntax implementation:

- It is not possible to print a blank line at assembly-time using the GNU assembly `.warning` directive. Only a warning with an empty message can be printed.
- The format of the diagnostic message displayed is different between `armasm` and the `armclang` integrated assembler.

With `armasm`, the diagnostic messages displayed at assembly-time by the macro example are:

```
"macros_armasm.S", line 11:
"macros_armasm.S", line 12: hello
"macros_armasm.S", line 13: default
```

With the `armclang` integrated assembler, the diagnostic messages displayed at assembly-time by the macro example are:

```
<instantiation>:1:1: warning:
.warning ""
^
macros_armclang.S:11:5: note: while in macro instantiation
diagnose ""
^
<instantiation>:1:1: warning: hello
.warning "hello"
^
macros_armclang.S:13:5: note: while in macro instantiation
diagnose "hello"
^
<instantiation>:1:1: warning: default
.warning "default"
^
macros_armclang.S:14:5: note: while in macro instantiation
diagnose
```

Conditional loop macro - armasm syntax implementation

The macro takes the following parameters:

\$counter

The assembly-time variable for the loop counter. This parameter is required. The `{label}` parameter for the `MACRO` directive has been used for this parameter. If a normal macro parameter is used, the parameter cannot be instantiated as a label.

\$N

The maximum number of iterations for the loop. This parameter is required.

\$decr

The loop decrement value. This parameter is optional.

do

The text to which `$counter` is appended in each iteration of the loop. This parameter is required.

```
MACRO
$counter    WhileLoop $N, $decr="1", $do           ; macro definition
  ASSERT    "$counter" <> ""                        ; check that $counter has been
                                                    ; specified
  ASSERT    "$N" <> ""                              ; check that $N has been specified
  ASSERT    "$do" <> ""                              ; check that $do has been
                                                    ; specified
  GBLA      $counter                                ; create new local variable
                                                    ; $counter
$counter     SETA $N                                ; initialize $counter
  WHILE     $counter > 0                            ; loop while $counter > 0
    $do$counter                                     ; assemble in each iteration
                                                    ; of the loop
$counter     SETA $counter-$decr                    ; decrement the counter by $decr
  WEND
MEND
; macro instantiation
AREA       WhileLoopMacro, CODE
THUMB
counter    WhileLoop 10, 2, "mov r0, #"
END
```

Conditional loop macro - GNU syntax implementation

The macro takes the following parameters:

counter

The assembly-time variable for the loop counter. This parameter is required.

N

The maximum number of iterations for the loop. This parameter is required.

decr

The loop decrement value. This parameter is optional.

do

The text to which `\counter` is appended in each iteration of the loop. This parameter is required.

```
/* Macro that inserts the \counter value
   at the end of all \do varargs,
   up to N times. */
.macro WhileLoop, counter:req, N:req, decre=1, do:vararg
.set \counter, \N      // initialise the variable \counter to 0
.rept \N               // loop up to \N times
.ifgt \counter         // assemble only if \counter is greater than zero
\do\counter
.set \counter, \counter-\decre // decrement the counter by \decre
.endif
.endr
.endm
// macro instantiation
.section "WhileLoopMacro", "ax"
WhileLoop counter, 10, 2, mov r0, #
```

**Note**

The order in which the GNU assembly `.ifgt`, `.endif`, `.rept`, and `.endr` directives are used is important. Including the `.endr` directive as a statement within the `.ifgtendif` structure produces an error. Similarly, placing the `.endif` directive outside the `.reptendr` structure produces an error.

The macro expansion produces the following code:

```
mov r0, #0xa
mov r0, #8
mov r0, #6
mov r0, #4
mov r0, #2
```

Notable differences from the `armasm` syntax implementation:

- In the `armasm` syntax implementation, the `ASSERT` directive is used to raise an error if a required parameter is missing. In the GNU syntax implementation, this can be achieved by using the parameter type `req` for required parameters in the macro definition.
- In the `armasm` syntax implementation, the macro instantiation uses a string as the value to the `$do` parameter. The quotes are implicitly removed at assembly-time. Quotes are required as the parameter value contains spaces. In the GNU syntax implementation, this is achieved using the parameter type `vararg` for the `\do` parameter in the macro definition.
- In the GNU syntax implementation, the `.reptendr` structure is always evaluated `\N` times at assembly-time. This is because the `.ifgtendif` structure must be placed within the `.reptendr` structure. In the `armasm` syntax implementation, the `WHILE...WEND` structure is only evaluated the required number of times at assembly-time based on the controlling expression of the `WHILE` directive.

Related information

[GNU Binutils - Using `as`: `.error`](#)

6. Changes Between Different Versions of Arm Compiler for Embedded 6

A description of the changes that affect migration and compatibility between different versions of Arm® Compiler for Embedded 6.

- Arm does not guarantee the compatibility of C++ compilation units compiled with different major or minor versions of Arm Compiler for Embedded and linked into a single image. Therefore, Arm recommends that you always build your C++ code from source with a single version of the toolchain.



Note

You can mix C++ with C code or C libraries.

- All C++ compilation units that are to be linked into a single image must be compiled with the same version of the C++ standard library ABI. If the ABI version changes between Arm Compiler for Embedded releases, then you must recompile your object files.

If you are unable to recompile some of your object files, then contact Arm Support at <https://developer.arm.com/support>.



Note

The documentation changes for Arm Compiler 6.15 and later releases are listed in an appendix for each document.

6.1 Documentation changes between Arm Compiler for Embedded releases

Each document contains a list of technical changes that have been made to the documentation, starting from Arm® Compiler 6.15.

The following sections list these changes:

- [Arm Compiler for Embedded User Guide Revision history.](#)
- [Arm Compiler for Embedded Reference Guide Revision history.](#)
- [Arm Compiler for Embedded Migration Guide Revision history.](#)
- [Arm Compiler for Embedded Arm C and C++ Libraries and Floating-Point Support User Guide Revision history.](#)
- [Arm Compiler for Embedded Errors and Warnings Reference Guide Revision history.](#)

6.2 Summary of changes between Arm Compiler for Embedded 6.22 and Arm Compiler for Embedded 6.23

A summary of the changes between Arm® Compiler for Embedded 6.22 and Arm Compiler for Embedded 6.23.

Architecture and optional extension changes

The architecture and extension changes are:

- FEAT_FAMINMAX is on by default from Armv9.5-A.
- FEAT_LUT is on by default from Armv9.5-A.
- FEAT_FPMR no longer has the `+fpmr` option to control it.
- The 64-bit Armv9.6-A architecture support level is [BETA].
- Features supported:

Table 6-1: AArch64 state A-profile features

Feature identifier	Optional from	Enabled by default	Support level
FEAT_CMPBR	Armv9.5-A	Armv9.6-A	[BETA]
FEAT_F8F16MM	Armv9.2-A	-	[BETA]
FEAT_F8F32MM	Armv9.2-A	-	[BETA]
FEAT_FPRCVT	Armv9.5-A	Armv9.6-A	[BETA]
FEAT_LSFE	Armv9.5-A	-	[BETA]
FEAT_LSUI	Armv9.5-A	Armv9.6-A	[BETA]
FEAT_OCCMO	Armv9.5-A	Armv9.6-A	[BETA]
FEAT_PCDPHINT	Armv9.5-A	-	[BETA]
FEAT_PoPS	Armv9.5-A	-	[BETA]
FEAT_RME_GPC3	Armv9.5-A	-	[BETA]
FEAT_SVE2p1	Armv9.4-A	-	Supported
FEAT_SME2p1	Armv9.2-A	-	Supported
FEAT_SME2p2	Armv9.5-A	-	[BETA]
FEAT_SME_B16B16	Armv9.2-A	-	[BETA]
FEAT_SSVE_AES	Armv9.5-A	-	[BETA]
FEAT_SSVE_F8F16MM	Armv9.2-A	-	[BETA]
FEAT_SSVE_F8F32MM	Armv9.2-A	-	[BETA]
FEAT_SVE2p2	Armv9.5-A	-	[BETA]
FEAT_SVE_AES2	Armv9.5-A	-	[BETA]
FEAT_SVE_B16B16	Armv9.2-A	-	Supported
FEAT_SVE_BFSCALE	Armv9.2-A	-	[BETA]

Feature identifier	Optional from	Enabled by default	Support level
FEAT_SVE_F16F32MM	Armv9.2-A	-	[BETA]

For more information, see [-march](#) and [-mcpu](#).

Command-line options

The following `armclang` command-line options are now supported:

- `--print-enabled-extensions`

6.3 Summary of changes between Arm Compiler for Embedded 6.21 and Arm Compiler for Embedded 6.22

A summary of the changes between Arm® Compiler for Embedded 6.21 and Arm Compiler for Embedded 6.22.

Architecture and optional extension changes

The architecture and extension changes are:

- Armv9.5-A is fully supported.
- The following architecture extensions are supported:
 - `faminmax`
 - `fp8dot2`
 - `fp8dot4`
 - `fp8fma`
 - `lut`
 - `sme-fp8f16`
 - `sme-fp8f32`
- Armv8-R AArch32 does not support any of the Armv8.x extensions.

Security features

The following security features are now supported:

- Added a topic on memory-safety best practices. See [Memory-safety best practices](#) for more information.

Command-line options

The following `armclang` command-line options are now supported:

- `-faligned-new`
- `-foptimize-sibling-calls` and `-fno-optimize-sibling-calls`
- `-fstack-usage`

- `-isystem`
- `-mabi`
- `-mdefault-build-attributes` and `-mno-default-build-attributes`
- `-Wformat=<n>`
- `--verbose`

Variable and function attributes

The following function attributes are now supported:

- `__attribute__((optnone))`
- `__attribute__((target("arm"|"thumb")))`

Removed features

- The Base Platform linking model and *Base Platform Application Binary Interface* (BPABI) are no longer supported.
- The following linker options are no longer supported:
 - `--base_platform.`
 - `--bpabi.`
 - `--dll.`
 - `--pltgot=type.`
 - `--pltgot_opts=mode.`

Other changes

The following are additional changes to Arm Compiler for Embedded:

- You can now use the `armlink` option `--cpu` for Armv8-R AArch64 targets.
- `#pragma message` is supported.
- The `strlen()` library function is supported.
- Added documentation for the `longjmp()` and `setjmp()` functions.
- Added information for `math_errhandling` in relation to the `-ffp-mode` command-line option.
- Added overview information for aligned and unaligned accesses. See [Alignment support in Arm Compiler for Embedded 6](#).
- Added overview information and an example that you can build and run for *Thread Local Storage* (TLS). See [Thread Local Storage](#).
- Added documentation on [How to build for an Armv8-R AArch64 target without hardware floating-point support](#).

6.4 Summary of changes between Arm Compiler for Embedded 6.20 and Arm Compiler for Embedded 6.21

A summary of the changes between Arm® Compiler for Embedded 6.20 and Arm Compiler for Embedded 6.21.

Architecture and optional extension changes

The following architectures and extensions are supported:

- The 64-bit Armv9.5-A architecture is supported as [BETA].
- The `cpa` and `fp8` features are supported as [ALPHA].
- The `pauth-lr` and `tlbiw` features are supported as [BETA].

Security features

The following security features are now supported:

- Return address signing hardening.
- *Straight-Line Speculation* (SLS) hardening.
- Stack tagging is now fully supported.

Command-line options

The following `armclang` command-line options are now supported:

- `-mharden-sls`.
- `-mharden-pac-ret`.
- `-ffreestanding`.
- `-nobuiltinc`.

Variable and function attributes

The following variable attributes are now supported:

- `__attribute__((common))`.
- `__attribute__((noccommon))`.

The following options are supported for the `__attribute__((target("<options>")))` function attribute:

- `harden-pac-ret=none`.
- `harden-pac-ret=load-return-address`.

Deprecated features

- The Base Platform linking model and *Base Platform Application Binary Interface* (BPABI) are deprecated.
- The following linker options are deprecated:

- `--base_platform.`
- `--bpabi.`
- `--dll.`
- `--pltgot=type.`
- `--pltgot_opts=mode.`

Other changes

The following are additional changes to Arm Compiler for Embedded:

- Execute-only code is now supported on the Armv6-M architecture. However, execute-only is not supported on Armv6-M for any form of position independent code.

6.5 Summary of changes between Arm Compiler for Embedded 6.19 and Arm Compiler for Embedded 6.20

A summary of the changes between Arm® Compiler for Embedded 6.19 and Arm Compiler for Embedded 6.20.

Architecture and optional extension changes

The following architectures and extensions are supported:

- The Armv8.9-A and Armv9.4-A architectures are fully supported.
- The `cssc`, `d128`, `ite`, `lse128`, `predres2`, `rasv2`, `rcpc3`, and the features are fully supported.
- The `b16b16` feature is supported as [ALPHA].

C and C++ standards changes

The default C++ language standard is `gnu++17`.

Added support for the C++17 standard library header `<memory_resource>`.

Command-line options

The following `armclang` command-line options are now supported:

- `-ffp-contract.`
- `-fsanitize=memtag-heap` and `-fsanitize=memtag-stack.`

armclang pragmas

The following pragmas are supported:

- `#pragma STDC FP_CONTRACT.`

Other changes

The following are additional changes to Arm Compiler for Embedded:

- `-fsanitize=memtag` is not supported.

6.6 Summary of changes between Arm Compiler for Embedded 6.18 and Arm Compiler for Embedded 6.19

A summary of the changes between Arm® Compiler for Embedded 6.18 and Arm Compiler for Embedded 6.19.

Architecture and optional extension changes

The following architectures and extensions are supported:

- The Armv8.9-A and Armv9.4-A architectures are supported as [BETA].
- Added support for Armv8-R AArch64 with hardware floating-point.
- The Cortex®-M85 processor features are fully supported.

Security features

The following security features are now supported:

- *Control Flow Integrity* (CFI) sanitizer.
- Shadow call stack.
- *Undefined Behavior Sanitizer* (UBSan).

C and C++ standards changes

C++17 is fully supported, with some exceptions that are listed in [Standard C++ library implementation definition](#).

For `std::vector<bool>::const_reference` and `std::bitset::const_reference`, the `const_reference` type is defined as `bool`. The statement that they did not conform to the standards has been removed.

Command-line options

The following command-line options are now supported:

- The following `armclang` options:
 - `-feliminate-unused-debug-types` and `-fno-eliminate-unused-debug-types` are supported as [COMMUNITY] features.
 - `-fcomplete-member-pointers`.
 - `-fsanitize` and `-fno-sanitize`.
 - `-fsanitize-ignorelist=<ignorelistfile>` and `-fno-sanitize-ignorelist`.
 - `-fsanitize-minimal-runtime`.
 - `-fsanitize-recover` and `-fno-sanitize-recover`.
 - `-fsanitize-trap=<option>`.

- `-mframe-chain`.
- `-mtune` is supported as a [COMMUNITY] feature.
- `-mpure-code` is supported as an alias for `-mexecute-only`.
- `-mglobal-merge` and `-mno-global-merge`.
- The following `armlink` options:
 - `--check_pac_mismatch` and `--info=pac`.
 - `--mcmodel=large` is now fully supported.
 - `--elf-output-format`, `--scatterload-enabled`, and `--no-scatterload-enabled`.

armclang attributes and pragmas

The following attributes and pragmas are supported:

- `__attribute__((no_sanitize("<option>")))`
- `#pragma import(__use_two_region_memory)`
- The `relro` option is now supported for `#pragma clang section`.

Other changes

The following are additional changes to Arm Compiler for Embedded:

- The `armasm` legacy assembler is deprecated.
- DWARF 5 is supported, except for `fromelf` disassembly.
- The `_sys_tmpnam()` function is deprecated, and the `_sys_tmpnam2()` function is supported.

6.7 Summary of changes between Arm Compiler for Embedded 6.17 and Arm Compiler for Embedded 6.18

A summary of the changes between Arm® Compiler for Embedded 6.17 and Arm Compiler for Embedded 6.18.

Architecture and optional extension changes

The following architectures and extensions are supported:

- The PACBTI extension for Armv8.1-M targets with the Main Extension is now fully supported. This extension is enabled using the `+pactbi` feature option for the `-march` and `-mcpu` command-line options.
- The A-profile Hinted Conditional Branches Extension is supported. This is specified by the `+hbc` feature option for the `-march` and `-mcpu` command-line options.
- The *Performance Monitor Extension v3* (PMUv3) for Armv8-A targets is supported. This extension is enabled by default if you use `-mcpu` to enable code generation for a specific CPU that implements PMUv3. However, if you use `-march` to target an architecture profile, then `pmuv3` is not enabled by default and must be specified explicitly using the `pmuv3` feature option for the `-march` and `-mcpu` command-line options when required.

- The Armv8.8-A and Armv9.3-A support for the A-profile Memory Operations Extension is now supported. This extension is enabled using the `+mops` feature option for the `-march` and `-mcpu` command-line options, and the predefined macro `__ARM_FEATURE_MOPS`.

For more information, see:

- [-march](#)
- [-mcpu](#)
- [Predefined macros](#)

Command-line options

Arm Compiler for Embedded 6.18 adds support for the `armlink` command-line options, `--require-bti` and `--info=bti` option, and there is a change in behavior when linking BTI with non-BTI user objects:

- [--info=topic \(armlink\)](#)
- [--library_security=protection](#)
- [--require-bti](#)

Arm Compiler for Embedded 6.18 provides the new `armclang` option `-mrestrict-it`:

- [-mrestrict-it](#), [-fno-restrict-it](#)

SVE auto-vectorization is supported in 6.18, but without SVE optimized libraries:

- [-fvectorize](#), [-fno-vectorize](#)
- [-O](#)

C++ Library changes

The function `__ARM_TPL_condvar_monotonic_timedwait()` is supported as [ALPHA]:

- [Condition variables \[ALPHA\]](#)

6.8 Summary of changes between Arm Compiler 6.16 and Arm Compiler for Embedded 6.17

A summary of the changes between Arm® Compiler 6.16 and Arm Compiler for Embedded 6.17.



This topic includes descriptions of [ALPHA] and [BETA] features. See [Support level definitions](#).

Product name change

The Arm Compiler product name has changed to Arm Compiler for Embedded from version 6.17.

Architecture and optional extension changes

The following architectures and extensions are supported:

- Armv8.8-A [ALPHA].
- Armv9-A, Armv9.1-A, and Armv9.2-A.
- Armv9.3-A [ALPHA].
- *Scalable Matrix Extension* (SME) [ALPHA].
- *Realm Management Extension* (RME) [ALPHA].
- Armv8.1-M PACBTI extension [BETA].

For more information, see [-march](#) and [-mcpu](#).

6.9 Summary of changes between Arm Compiler 6.15 and Arm Compiler 6.16

A summary of the changes between Arm® Compiler 6.15 and Arm Compiler 6.16.

Architecture and optional extension changes

Armv8.7-A is fully supported, and enables the following in the release:

- The following base Armv8.7-A ISA features:
 - the HCRX_EL2 System register
 - the WFET, WFIT, DSBNXS, and TLBINXS instructions.
- The Extended Event Filter of the Statistical Profiling Extension, that consists of an extra register in the Statistical Profiling Extension.
- The Invalidate the Branch Record Buffer extension, `+brbe`.
- The accelerator support extension, `+ls64`, is fully supported. The extension enables the 64-byte load and store instruction family. That is, `LD64B` and `ST64BV0`, and the `ACCDATA_EL1` system register.

For more information, see [-march](#) and [-mcpu](#).

C++ library changes

The following changes have been made to the C++ library, `libc++`:

- The *Application Binary Interface* (ABI) version used for the C++ library is now version 2. The change of ABI version has some consequences:
 - C++ objects or libraries built using Arm Compiler 6.15 or earlier are not guaranteed to be compatible with C++ objects or libraries built using 6.16. Therefore, you might see link-time errors or, in rare circumstances, unexpected runtime behavior.

To make sure your C++ objects and libraries are compatible with Arm Compiler 6.16, you must rebuild all your C++ code with 6.16.



Note

If you cannot rebuild any of your C++ objects or libraries, then you must continue to use your previous Arm Compiler version.

- `std::pointer_safety` and `std::get_pointer_safety()` are no longer available in C++03. However, because the `get_pointer_safety()` function always returns `pointer_safety::relaxed`, you can either reimplement the function or avoid using it.
- The Arm Compiler implementation of `std::deque<T>` allocates memory for storing its elements as blocks of certain size. In Arm Compiler 6.15 and earlier versions, the number of elements per block is computed as follows:
 - If `sizeof(T) < 256`, each block can hold `4096/sizeof(T)` elements.
 - Otherwise, each block can hold 16 elements.

For Arm Compiler 6.16 and later versions, the formula is different:

- If `sizeof(T) < 8`, each block can hold `64/sizeof(T)` elements.
- Otherwise, each block can hold 8 elements.

armlink changes

Arm Compiler 5 does not support literal pool merging.

Arm Compiler for Embedded 6 merges literal pools by default. In Arm Compiler 6.15 and earlier, marking a load region as `PROTECTED` prevents merging of literal pools for const strings but not for other const values in literal pools. For example, your code might have three literal pools, each containing the same const value, where two of the literal pools are in a `PROTECTED` region. In Arm Compiler 6.15 and earlier, `armlink` merges the three const values but leaves a single copy in the `PROTECTED` regions. However, the function containing the copy still references that copy, but the referencing function is now part of a different region.

In Arm Compiler 6.16, `armlink` prevents merging literal pool entries of const strings and const values across regions that have the `PROTECTED` load region attribute.

Here, the terms const string and const value have the following meanings:

const string

A string literal from an ELF section with the `SHF_MERGE` and `SHF_STRINGS` flags.

const value

A constant defined in a constant pool where the constant pool is in the same section as the code that uses it.

6.10 Summary of changes between Arm Compiler 6.14 and Arm Compiler 6.15

A summary of the changes between Arm® Compiler 6.14 and Arm Compiler 6.15.

Architecture and optional extension changes

Arm Compiler 6.15 adds the following:

- [ALPHA] support for the Armv8.7-A architecture and the Accelerator Support Extension, +ls64, for 64-byte atomic loads and stores.
- [BETA] support for the Armv8-R AArch64 architecture.

Other changes are as follows:

The *Custom Datapath Extension* (CDE), +cdcep<N> is fully supported.

For more information, see [-march](#) and [-mcpu](#).

Command-line options

Arm Compiler 6.15 adds support for the `armlink` command-line option, `--dangling-debug-address=<address>`. See [--dangling-debug-address=address](#).

Arm Compiler 6.15 adds a new `-omin` command-line option for `armclang` and `armlink` which aims to produce the minimum code size using link-time optimization. The value `omin` can also be specified for the `armlink` command-line option `--lto-level`. For more information, see the [--lto-level](#) `armclang` reference page.

6.11 Summary of changes between Arm Compiler 6.13 and Arm Compiler 6.14

A summary of the changes between Arm® Compiler 6.13 and Arm Compiler 6.14.



This topic includes descriptions of [BETA] features. See [Support level definitions](#).

New architectures and optional extensions

Arm Compiler 6.14 adds [BETA] support for the *Custom Datapath Extension* (CDE), +cdcep<N>. For more information, see [-march](#).

New processors

Arm Compiler 6.14 adds Cortex-M55 processor support. For information about the *M-profile Vector Extension* (MVE) and floating-point (FP) combinations for this processor, see [Supported architecture feature combinations for specific processors](#).

Command-line options

Arm Compiler 6.14 adds [BETA] support for the `fromelf` command-line option, `--coproc<N>=<value>`, to enable T32 encodings of the CDE. See `--coprocN=value`.

Function attributes

Arm Compiler 6.14 adds support for the `__attribute__((target("<options>")))` function attribute. See `__attribute__((target("<options>")))` for more information.

Library-related features

The Arm implementation of the C++ standard library class `std::random_device` is described in [Numerics library](#).

6.12 Summary of changes between Arm Compiler 6.12 and Arm Compiler 6.13

A summary of the changes between Arm® Compiler 6.12 and Arm Compiler 6.13.



This topic includes descriptions of [ALPHA] and [BETA] features. See [Support level definitions](#).

New architectures and optional extensions

Arm Compiler 6.13 adds:

- Early support for Future Architecture Technologies:
 - Assembly for the *Embedded Trace Extension* (ETE). This is enabled by default.
 - Assembly for the *Trace Buffer Extension* (TRBE). This is enabled by default.
 - Assembly for *Scalable Vector Extension 2* (SVE2).
 - Assembly and intrinsics for *Transactional Memory Extension* (TME).

For more information, see [-march](#).

- [ALPHA] support for the Armv8.6-A architecture:
 - [ALPHA] support assembly and intrinsics for the BFloat16 Extension.
 - [ALPHA] support assembly and intrinsics for the *Matrix Multiplication Extension* (MME).

For more information, see [-march](#).

- Support for the Armv8.1-M architecture:
 - Assembly and intrinsics for the *M-profile Vector Extension* (MVE).
 - [BETA] support for the automatic vectorization for MVE.

For more information, see [-march](#).

- Intrinsics for the Armv8.5-A architecture *Memory Tagging Extension* (MTE) are promoted from [ALPHA] support to full product quality support. See [-march](#).

Command-line options

- Arm Compiler 6.13 supports the SysV dynamic linking model, using the following command-line options:
 - [armclang -fpic](#), [armclang -fno-pic](#)
 - [armclang -fsysv](#), [armclang -fno-sysv](#)
 - [armclang -shared](#)
 - [armlink -dynamiclinker=name](#)
 - [armlink -import_unresolved](#), [armlink -no_import_unresolved](#)
 - [armlink -soname](#)
 - [armlink -sysv](#)
 - [armlink -shared](#)
- The [armclang -fsanitize](#), [-fno-sanitize](#) option replaces the [armclang -mmemtag-stack](#) option.

6.13 Summary of changes between Arm Compiler 6.11 and Arm Compiler 6.12

A summary of the changes between Arm® Compiler 6.11 and Arm Compiler 6.12.



Note

This topic includes descriptions of [ALPHA] features. See [Support level definitions](#).

New architectures and optional extensions

Arm Compiler 6.12 adds:

- [armclang](#) inline assembler and integrated assembler support for the *Speculation Barrier* (SB) instruction in the AArch32 and AArch64 states. This is mandatory for the Armv8.5-A and later architectures. This is optional for the Armv8-A to Armv8.4-A architectures. To enable the use of the SB instruction, use [-march=armv8-a+sb](#). For more information, see [-march](#).
- [armclang](#) inline assembler and integrated assembler support for the *Speculative Store Bypass Safe* (SSBS) register and instructions in the AArch64 state. This is mandatory for the Armv8.5-A and later architectures. This is optional for the Armv8-A to Armv8.4-A architectures. To enable

the use of the SSBS register and instructions, use `-march=armv8-a+ssbs`. For more information, see [-march](#).

- `armclang` inline assembler and integrated assembler support for the Prediction Restriction by Context registers and instructions in the AArch64 state. This is mandatory for the Armv8.5-A and later architectures. This is optional for the Armv8-A to Armv8.4-A architectures. To enable the Prediction Restriction by Context registers and instructions, use `-march=armv8-a+predres`. For more information, see [-march](#).

Command-line options

Arm Compiler 6.12 adds support for the following command-line options.

- These [ALPHA] options support generation of code for protecting the stack with the memory tagging extension:
 - `armclang -mmemtag-stack`
 - `armlink --library_security=v8.5a`

The memory tagging extension is optional in Armv8.5-A and later architectures.

To disable this stack protection, use `-mno-memtag-stack`.



Note

Arm Compiler 6.12 also adds support for heap protection using the memory tagging extension, when defining the symbol `__use_memtag_heap`.

-
- These options support generation of code for protecting the stack with stack guard variables:
 - `armclang -fstack-protector`
 - `armclang -fstack-protector-strong`
 - `armclang -fstack-protector-all`

To disable this stack protection, use `armclang -fno-stack-protector`.

- The `armclang -ffixed-r<N>` option prevents the compiler from using the specified core register, unless the use is required for Arm ABI compliance.

Keywords

Arm Compiler 6.12 adds support for the `register` keyword. The `register` keyword enables the use of certain core registers as global named register variables in the AArch32 state.

6.14 Summary of changes between Arm Compiler 6.10 and Arm Compiler 6.11

A summary of the changes between Arm® Compiler 6.10 and Arm Compiler 6.11.

New architectures and optional extensions

Arm Compiler 6.11 adds:

- `armclang` inline assembler and integrated assembler support for the Armv8.5-A architecture. To target the Armv8.5-A architecture, use `-march=armv8.5-a`. For more information, see [-march](#).
- `armclang` inline assembler and integrated assembler support for the optional *Memory Tagging Extension* (MTE) for the Armv8.5-A architecture. To target MTE, use `-march=armv8.5-a+mementag`. For more information, see [-march](#).
- `armclang` inline assembler and integrated assembler support for the optional Random Number Instructions for the Armv8.5-A architecture. To target the Random Number Instructions, use `-march=armv8.5-a+rng`. For more information, see [-march](#).
- Support for branch protection features for Armv8.3-A and later architectures. For more information, see [-mbranch-protection](#).
- Support for half-precision floating-point multiply with add or multiply with subtract instructions for Armv8.2-A and later architectures. To target these instructions, use `+fp16fm1` with `-mcpu` or `-march`. For more information, see [-march](#) and [-mcpu](#).

Command-line options

Arm Compiler 6.11 adds support for the following command-line options.

- These options support generation of code with branch protection:
 - [-mbranch-protection](#)
 - [--library_security=protection](#)
- These options control whether the output file contains compiler name and version information:
 - [-fident](#)
 - [-fno-ident](#)
- These options enable the generation of *Position Independent eXecute Only* (PIXO) library features for Armv7-M targets:
 - [-mpixolib](#)
 - [--pixolib](#)

Deprecated features

Arm Compiler 6.11 deprecates the following features:

- `__declspec` attributes has been deprecated.
- Support for ELF sections that contain the legacy `SHF_COMDEF` ELF section flag is deprecated.
 - The `COMDEF` section attribute of the legacy `armasm` syntax [AREA](#) directive is deprecated.

- Linking with legacy objects that contain ELF sections with the legacy `SHF_COMDEF` ELF section flag is deprecated.
- The legacy R-type dynamic linking model, which does not conform to the *32-bit Application Binary Interface* for the Arm Architecture, has been deprecated.
 - Linking with `--reloc` command-line option has been deprecated.
 - Linking without `--base_platform`, with a scatter file that contains the [Load region attributes](#) load region attribute, has been deprecated.

For more information, see [Backwards compatibility issues](#).

Removed features

The following options have been removed from Arm Compiler 6.11:

- `armlink --compress_debug` and `--no_compress_debug` command-line options.
- `armlink --match=crossmangled` command-line option.
- `armlink --strict_enum_size` and `--no_strict_enum_size` command-line options.
- `armlink --strict_wchar_size` and `--no_strict_wchar_size` command-line options.

Product quality support level

Support for `-std=c++14` and `-std=gnu++14` has changed from [BETA] to fully supported, with the exception of certain C++14 features. For more information, see [-std](#) in the *armclang Reference Guide* and [Clang and LLVM documentation](#) in the *Arm Compiler for Embedded 6 User Guide*.

For earlier versions of the compiler, Arm recommended the use of `-std=c++11` when compiling C++ source files. This recommendation has been removed.

6.15 Summary of changes between Arm Compiler 6.9 and Arm Compiler 6.10

A summary of the changes between Arm® Compiler 6.9 and Arm Compiler 6.10.

General changes

The following are general changes in Arm Compiler 6.10:

- When using the legacy assembler, `armasm`, to assemble for AArch32 targets that support A32 and T32 instruction sets, the `apcs` interworking default has changed from `/nointerwork` to `/interwork`. If you must use the non-interworking `apcs`, then you must specify `--apcs=/nointerwork` on the command-line of the legacy assembler, `armasm`. However, from Arm Compiler 6.10, the compiler does not include pure A32 libraries for non-interworking `apcs`. Therefore, if you use the non-interworking `apcs` for A32 code and require library support, then `armlink` generates an error unless you provide your own supporting libraries.
- In certain circumstances, when a legacy assembler or linker process invoked the compiler as a subprocess to preprocess a file but all suitable licenses were already in use, the processes could deadlock. This issue has been fixed.

- The default C++ source language mode has changed from gnu++98 to gnu++14. gnu++14 language and library features are a [BETA] product feature. Arm recommends compiling with `-std=c++11` to restrict Arm Compiler to using only C++11 language and library features, which are fully supported. See [-std](#) in the *armclang Reference Guide*.

Enhancements

The following are enhancements in Arm Compiler 6.10:

Compiler and integrated assembler (armclang)

Added support for the `-fno-builtin` option that can prevent the compiler from optimizing calls to certain standard C library functions, such as `printf()`. When compiling without `-fno-builtin`, the compiler can replace such calls with inline code or with calls to other library functions.

See [-fno_builtin](#) in the *armclang Reference Guide*.

6.16 Summary of changes between Arm Compiler 6.8 and Arm Compiler 6.9

A summary of the changes between Arm® Compiler 6.8 and Arm Compiler 6.9.

General changes

The following are general changes in Arm Compiler 6.9:

- Added support for the Armv8.4-A architecture. To target Armv8.4-A, use the following options:

State	armclang options	armlink, and fromelf options
AArch64	<code>--target=aarch64-arm-none-eabi</code> <code>-march=armv8.4-a</code>	Do not use the <code>--cpu=<name></code> option.
AArch32	<code>--target=arm-arm-none-eabi</code> - <code>march=armv8.4-a</code>	Do not use the <code>--cpu=<name></code> option.



The legacy assembler, `armasm`, does not support the Armv8.4-A architecture.

- Added support for the optional Cryptographic Extension in Armv8.4-A. To target Armv8.4-A with the Cryptographic Extension, use the following options:

State	armclang options	armlink and fromelf options
AArch64	<code>--target=aarch64-arm-none-eabi</code> <code>-march=armv8.4-a+crypto</code>	Do not use the <code>--cpu=<name></code> option.

State	armclang options	armlink and fromelf options
AArch32	<code>--target=arm-arm-none-eabi - march=armv8.4-a -mfpu=crypto- neon-fp-armv8</code>	Do not use the <code>--cpu=<name></code> option.

**Note**

The legacy assembler, `armasm`, does not support the Armv8.4-A architecture.

For more information about selecting specific cryptographic algorithms, see [-mcpu](#) in the *Arm Compiler for Embedded Reference Guide*.

- A change in Arm Compiler 6.9 means that compiling with `-mexecute-only` always generates an empty `.text` section that is read-only.

For more information about handling this section, see [Compiling with -mexecute-only generates an empty .text section](#) in the *Arm Compiler for Embedded User Guide*.

6.17 Summary of changes between Arm Compiler 6.7 and Arm Compiler 6.8

A summary of the changes between Arm® Compiler 6.7 and Arm Compiler 6.8.

General changes

The following are general changes in Arm Compiler 6.8:

- Added support for the optional Dot Product instructions in Armv8.2-A and Armv8.3-A. To target Armv8.2-A and Armv8.3-A with the Dot Product instructions, use the following options:

Processor	armclang options	armasm, armlink, and fromelf options
Armv8.3-A and AArch64 state	<code>--target=aarch64-arm-none-eabi - march=armv8.3-a+dotprod</code>	<code>--cpu=8.3-A.64.dotprod</code>
Armv8.3-A and AArch32 state	<code>--target=arm-arm-none-eabi - march=armv8.3-a+dotprod</code>	<code>--cpu=8.3-A.32.dotprod</code>
Armv8.2-A and AArch64 state	<code>--target=aarch64-arm-none-eabi - march=armv8.2-a+dotprod</code>	<code>--cpu=8.2-A.64.dotprod</code>
Armv8.2-A and AArch32 state	<code>--target=arm-arm-none-eabi - march=armv8.2-a+dotprod</code>	<code>--cpu=8.2-A.32.dotprod</code>

- Added support for the Cortex®-A75 and Cortex-A55 processors. To target Cortex-A75 and Cortex-A55, use the following options:

Processor	armclang options	armasm, armlink, and fromelf options
Cortex-A 75 for AArch64 state	<code>--target=aarch64-arm-none-eab -mcpu=cortex-a75</code>	8.2-A.64
Cortex-A 75 for AArch32 state	<code>--target=arm-arm-none-eab -mcpu=cortex-a75</code>	8.2-A.32
Cortex-A 55 for AArch64 state	<code>--target=aarch64-arm-none-eab -mcpu=cortex-a55 -mcpu=cortex-a55</code>	8.2-A.64
Cortex-A 55 for AArch32 state	<code>--target=arm-arm-none-eab -mcpu=cortex-a55 -mcpu=cortex-a55</code>	8.2-A.32

- When resolving the relocations of a branch instruction from a function with build attributes that include `~PRES8` to another function with build attributes that include `REQ8`, the linker previously reported:

```
Error: L6238E: <objname>(<secname>) contains invalid call from '~PRES8 (The user
did not require code to preserve 8-byte alignment of 8-byte data objects)' function
to 'REQ8 (Code was permitted to depend on the 8-byte alignment of 8-byte data
items)' function <sym>.
```

This behavior has been changed. By default, the linker no longer reports an error in these circumstances. To restore the previous behavior, use the option `--strict_preserve8_require8`. For more information about this option, see `--strict_preserve8_require8` in the *Arm Compiler for Embedded Reference Guide*.

To successfully link with `--strict_preserve8_require8`:

1. Manually inspect assembly language source files that are assembled using the integrated assembler.
2. Ensure that all functions preserve 8-byte alignment of the stack and of 8-byte data items.
3. Add the directive `.eabi_attribute Tag_ABI_align_preserved, 1` to each such source file.

Enhancements

The following are enhancements in Arm Compiler 6.8:

Compiler and integrated assembler (armclang)

- Previously, the inline assembler and integrated assembler provided limited support for instruction substitutions for the A32 and T32 instruction sets. Substitution occurs when a valid encoding does not exist for an instruction with a particular immediate, but an equivalent instruction that has the same result with the inverted or negated immediate is available. To disable this feature, use the option `-mno-neg-immediates`.

When `-mno-neg-immediates` is not specified, the range of substitutions that the inline assembler and integrated assembler perform has also been extended to cover extra valid substitutions for A64, A32, and T32.

For more information about this option, see [-mno-neg-immediates](#) in the *armclang Reference Guide*.

- Added support for:
 - `#pragma clang section`. This pragma enables migration of source code that previously used the legacy `armcc` feature `#pragma arm section`. See [#pragma clang section](#) in the *armclang Reference Guide*.
 - `-nostdlib` and `-nostdlibinc` options that enable objects to be linked with other ABI-compliant libraries. See [-nostdlib](#) and [-nostdlibinc](#) in the *armclang Reference Guide*.
 - `__unaligned` keyword. This keyword aids migration of source code that previously used the legacy `armcc` feature `__packed`. See [__unaligned](#) in the *armclang Reference Guide*.

General enhancements

Added support for C++14 source language modes. Use one of the following options to enable the compilation of C++14 source code:

- `-std=c++14`.
- `-std=gnu++14`.

See [-std](#) in the *armclang Reference Guide*.

6.18 Summary of changes between Arm Compiler 6.6 and Arm Compiler 6.7

A summary of the changes between Arm® Compiler 6.6 and Arm Compiler 6.7.

General changes

The following are general changes in Arm Compiler 6.7:

- Armv8-M architecture-based targets are now supported when using an Arm DS-5 Professional license.
- Arm Compiler 6.7 includes FlexNet Publisher 11.14.1.0 client libraries. This version of the license client is not compatible with previous versions of the FlexNet Publisher license server software. When used with a license server running an `armlmd` and `lmgrd` version earlier than 11.14.1.0, Arm Compiler 6.7 can report any of the following:
 - `Failed to check out a license. Bad message command.`
 - `Failed to check out a license. Version of vendor daemon is too old.`
 - `Flex error code: -83.`
 - `Flex error code: -140.`

A license server running `armlmd` and `lmgrd` version 11.14.1.0 (or later) is compatible with Arm Compiler 6.7 and all previous releases of Arm tools.

Arm recommends that you always use the latest version of the license server software that is available from <https://developer.arm.com/products/software-development-tools/license-management/downloads>.

- Previously, when generating execute-only sections, the tools set the ELF section header flag to `SHF_ARM_NOREAD`. For compliance with forthcoming changes to the *Application Binary Interface (ABI) for the Arm Architecture*, this behavior has changed. For execute-only sections, the tools now set the ELF section header flag to `SHF_ARM_PURECODE`.

Enhancements

The following are enhancements in Arm Compiler 6.7:

Compiler and integrated assembler (armclang)

- Added support for the `-ffp-mode=model` option that you can use to specify the level of floating-point standard compliance:
 - `-ffp-mode=std` selects the default compiler behavior.
 - `-ffp-mode=fast` is equivalent to `-ffast-math`.
 - `-ffp-mode=full` is equivalent to `-fno-fast-math`.

Arm recommends using `-ffp-mode` rather than `-ffast-math` OR `-fno-fast-math`.

For more information about this option, see [-ffp-mode](#) in the *armclang Reference Guide*.

- Extended the support for the `__attribute__((value_in_regs))` function attribute to improve compatibility with the equivalent Arm Compiler 5 feature.

For more information about this attribute, see the [__attribute__\(\(value_in_regs\)\) function attribute](#) in the *armclang Reference Guide*.

- Added support for the generation of implicit `IT` blocks when assembling for T32 state. To specify the behavior of the inline assembler and integrated assembler if there are conditional instructions outside `IT` blocks, use the option `-mimplicit-it=<name>`.

For more information about this option, see [-mimplicit-it](#) in the *armclang Reference Guide*.

- Previously, when compiling at `-Os`, the compiler could over-align literal pools that are generated during vectorization to a 128-bit boundary. This behavior has been changed. The compiler now avoids adding excessive padding.

armlink

Added support for `__at` sections that are named `.bss.ARM.__at_<address>`. The linker places the associated ZI data at the specified address.

6.19 Summary of changes between Arm Compiler 6.5 and Arm Compiler 6.6

A summary of the changes between Arm® Compiler 6.5 and Arm Compiler 6.6.

General changes

The following are general changes in Arm Compiler 6.6:

- Added support for the Armv8.3-A architecture. To target Armv8.3-A, use the following options:

State	armclang options	armasm, armlink, and fromelf options
AArch64	--target=aarch64-arm-none-eabi -march=armv8.3-a	--cpu=8.3-A.64
AArch32	--target=arm-arm-none-eabi - march=armv8.3-a	--cpu=8.3-A.32

- Added support for the Armv8-A AArch64 state *Scalable Vector Extension* (SVE) to the compiler. To target bare-metal systems with SVE, use the option `-march=armv8-a+sve`.

To disassemble objects that have been built for SVE, `11vm-objdump` is provided as an interim solution.

SVE features are available under a separate license. Contact Arm for more information. Added support for the Cortex®-R52 processor. To target Cortex-R52, use the following options:

Processor variant	armclang options	armasm, armlink, and fromelf options
D32 and Advanced SIMD	--target=arm-arm-none-eab - mcpu=cortex-r52	--cpu=Cortex-R52
D16 and single-precision only	--target=arm-arm-none-eab - mcpu=cortex-r52 -mfpv5=fpv5-d16	--cpu=Cortex-R52 --fpu=FPv5-SP

- Added support for the Cortex-M23 processor. To target Cortex-M23, use the following options:

armclang

--target=arm-arm-none-eabi -mcpu=cortex-m23

armasm, armlink, and fromelf

--cpu=Cortex-M23

- Added support for the Cortex-M33 processor. To target Cortex-M33, use the following options:

Processor variant	armclang options	armasm, armlink, and fromelf options
With both DSP and FP	--target=arm-arm-none-eab - mcpu=cortex-m33	--cpu=Cortex-M33
Without DSP but with FP	--target=arm-arm-none-eab - mcpu=cortex-m33+nodsp	--cpu=Cortex-M33.no_dsp

Processor variant	armclang options	armasm, armlink, and fromelf options
With DSP but without FP	<code>--target=arm-arm-none-eab -mcpu=cortex-m33 -mfloat- abi=soft</code>	<code>--cpu=Cortex-M33 --fpu=SoftVFP</code>
Without both DSP and FP	<code>--target=arm-arm-none-eab - mcpu=cortex-m33+nodsp -mfloat- abi=soft</code>	<code>--cpu=Cortex-M33.no_dsp -- fpu=SoftVFP</code>

- The default compiler behavior has changed. The following options are selected by default:
 - `-fdata-sections`.
 - `-ffunction-sections`.
 - `-fomit-frame-pointer`.
 - `-fvisibility=hidden`.
 - Configuration options that select a smaller, less IEEE 754 compliant floating-point math library.

To restore the previous behavior, select from the following options:

- `-fno-data-sections`.
- `-fno-function-sections`.
- `-fno-omit-frame-pointer`.
- `-fvisibility=default` [COMMUNITY].



Note

Arm recommends not using this option to restore the previous behavior.

- `-fno-fast-math`.

For more information about support level definitions and a subset of these options, see [Support level definitions](#).

- The `--cpu=<name>` option in `armasm`, `armlink`, and `fromelf` has changed to improve compatibility with the `-mcpu` compiler option.

Replace this option name	With this option name
<code>Cortex-A5.neon</code>	<code>Cortex-A5</code>
<code>Cortex-A5.vfp</code>	<code>Cortex-A5.no_neon</code>
<code>Cortex-A5</code>	<code>Cortex-A5.no_neon.no_vfp</code>
<code>Cortex-R5F-rev1</code>	<code>Cortex-R5</code>
<code>Cortex-R5F</code>	<code>Cortex-R5-rev0</code>
<code>Cortex-R5</code>	<code>Cortex-R5-rev0.no_vfp</code>
<code>Cortex-R5F-rev1.sp</code>	<code>Cortex-R5.sp</code>

Replace this option name	With this option name
Cortex-R5-rev1	Cortex-R5.no_vfp
Cortex-M4F or Cortex-M4.fp	Cortex-M4
Cortex-M4	Cortex-M4.no_fp
Cortex-M7.fp.dp	Cortex-M7
Cortex-M7	Cortex-M7.no_fp

- The following linker options are deprecated and are to be removed in a future release:
 - `--compress_debug`.
 - `--gnu_linker_defined_syms`.
 - `--legacyalign`.
 - `--match=crossmangled`.
 - `--strict_enum_size`.
 - `--strict_wchar_size`.

Enhancements

The following are enhancements in Arm Compiler 6.6:

Compiler and integrated assembler (armclang)

Added support for:

- `__attribute__((naked))` function attribute. This function attribute enables migration of Arm Compiler 5 and earlier embedded assembler functions to Arm Compiler for Embedded 6.
- Use of floating-point code in secure functions when compiling with `-mcmse -mfloat-abi=hard`.

armlink

Added full support for link-time optimization (LTO). To use LTO, specify the `-flto` option to the compiler and the `--lto` option to the linker.

Libraries and system headers

- Added [ALPHA] support for multithreading features in the C++11 standard library, for example `std::atomic` and `std::thread`. The API for these features is in the `arm-tp1.h` header file, but you must implement the low-level interface to the underlying operating system. The specification of this thread porting API is available through a separate document. Contact Arm Support for more information.
- Added support to the Arm C library to implement semihosting calls using the `HLT` instruction for Armv8-A and Armv8-R targets in AArch32 state.
- Added support for use of the C++ library without exceptions. To target C++ without exceptions, compile with the option `-fno-exceptions`.

When linking objects compiled without exceptions, a specialized C++ library variant is selected that does not have the code-size overhead of exceptions. This C++ library variant has undefined behavior at points where the normal library variant results in an exception being thrown.

7. Code Examples

Provides source code examples for Arm® Compiler 5 and Arm Compiler for Embedded 6.

7.1 Example startup code for Arm Compiler 5 project

This is an example startup code that compiles without errors using Arm® Compiler 5.

This code has been modified to demonstrate migration from Arm Compiler 5 to Arm Compiler for Embedded 6. This code requires other modifications for use in a real application.

```
// startup_ac5.c:

/*
 * Copyright (c) 2009-2017 ARM Limited. All rights reserved.
 *
 * SPDX-License-Identifier: Apache-2.0
 *
 * Licensed under the Apache License, Version 2.0 (the License); you may
 * not use this file except in compliance with the License.
 * You may obtain a copy of the License at
 *
 * www.apache.org/licenses/LICENSE-2.0
 *
 * Unless required by applicable law or agreed to in writing, software
 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
 * See the License for the specific language governing permissions and
 * limitations under the License.
 */

/*-----
 * Definitions
 *-----*/
#define USR_MODE 0x10          // User mode
#define FIQ_MODE 0x11         // Fast Interrupt Request mode
#define IRQ_MODE 0x12         // Interrupt Request mode
#define SVC_MODE 0x13         // Supervisor mode
#define ABT_MODE 0x17         // Abort mode
#define UND_MODE 0x1B         // Undefined Instruction mode
#define SYS_MODE 0x1F         // System mode

/*-----
 * Internal References
 *-----*/
void Vectors          (void) __attribute__ ((section("RESET")));
void Reset_Handler(void);
extern int printf(const char *format, ...);

__declspec(noreturn) void main (void)
{
    __enable_irq();
    printf("Starting main\n");
    while(1);
}
#pragma import (__use_no_semihosting)

/*-----
 * Exception / Interrupt Handler
 *-----*/
void Undef_Handler (void) __attribute__ ((weak, alias("Default_Handler")));
```

```

void SVC_Handler (void) __attribute__((weak, alias("Default_Handler")));
void PAbt_Handler (void) __attribute__((weak, alias("Default_Handler")));
void DAbt_Handler (void) __attribute__((weak, alias("Default_Handler")));
void IRQ_Handler (void) __attribute__((weak, alias("Default_Handler")));
void FIQ_Handler (void) __attribute__((weak, alias("Default_Handler")));

/*-----
Exception / Interrupt Vector Table
-----*/
__asm void Vectors(void) {
    __IMPORT Undef_Handler
    __IMPORT SVC_Handler
    __IMPORT PAbt_Handler
    __IMPORT DAbt_Handler
    __IMPORT IRQ_Handler
    __IMPORT FIQ_Handler
    LDR    PC, =Reset_Handler
    LDR    PC, =Undef_Handler
    LDR    PC, =SVC_Handler
    LDR    PC, =PAbt_Handler
    LDR    PC, =DAbt_Handler
    NOP
    LDR    PC, =IRQ_Handler
    LDR    PC, =FIQ_Handler
}

/*-----
Reset Handler called on controller reset
-----*/
__asm void Reset_Handler(void) {

    // Mask interrupts
    CPSID    if

    // Put any cores other than 0 to sleep
    MRC      p15, 0, R0, c0, c0, 5    // Read MPIDR
    ANDS     R0, R0, #3
goToSleep
    WFINE
    BNE      goToSleep

    // Reset SCTLR Settings
    MRC      p15, 0, R0, c1, c0, 0    // Read CP15 System Control register
    BIC      R0, R0, #(0x1 << 12)    // Clear I bit 12 to disable I Cache
    BIC      R0, R0, #(0x1 << 2)     // Clear C bit 2 to disable D Cache
    BIC      R0, R0, #0x1            // Clear M bit 0 to disable MMU
    BIC      R0, R0, #(0x1 << 11)    // Clear Z bit 11 to disable branch prediction
    BIC      R0, R0, #(0x1 << 13)    // Clear V bit 13 to disable hivecs
    MCR      p15, 0, R0, c1, c0, 0    // Write value back to CP15 System Control
register
    ISB

    // Configure ACTLR
    MRC      p15, 0, r0, c1, c0, 1    // Read CP15 Auxiliary Control Register
    ORR      r0, r0, #(1 << 1)       // Enable L2 prefetch hint (UNK/WI since r4p1)
    MCR      p15, 0, r0, c1, c0, 1    // Write CP15 Auxiliary Control Register

    // Set Vector Base Address Register (VBAR) to point to this application's vector
table
    LDR      R0, =Vectors
    MCR      p15, 0, R0, c12, c0, 0

    // Setup Stack for each exceptional mode
    __IMPORT |Image$$FIQ_STACK$$ZI$$Limit|
    __IMPORT |Image$$IRQ_STACK$$ZI$$Limit|
    __IMPORT |Image$$SVC_STACK$$ZI$$Limit|
    __IMPORT |Image$$ABT_STACK$$ZI$$Limit|
    __IMPORT |Image$$UND_STACK$$ZI$$Limit|
    __IMPORT |Image$$ARM_LIB_STACK$$ZI$$Limit|
    CPS      #0x11
    LDR      SP, =|Image$$FIQ_STACK$$ZI$$Limit|

```

```
CPS    #0x12
LDR    SP, =|Image$$IRQ_STACK$$ZI$$Limit|
CPS    #0x13
LDR    SP, =|Image$$SVC_STACK$$ZI$$Limit|
CPS    #0x17
LDR    SP, =|Image$$ABT_STACK$$ZI$$Limit|
CPS    #0x1B
LDR    SP, =|Image$$UND_STACK$$ZI$$Limit|
CPS    #0x1F
LDR    SP, =|Image$$ARM_LIB_STACK$$ZI$$Limit|

// Call SystemInit
IMPORT SystemInit
BL      SystemInit

// Unmask interrupts
CPSIE  if

// Call main
IMPORT main
BL      main
}

/*-----
   Default Handler for Exceptions / Interrupts
   -----*/
void Default_Handler(void) {
    while(1);
}
```

Related information

[Apache License](#) on page 130

7.2 Example startup code for Arm Compiler for Embedded 6 project

This is an example startup code that compiles without errors using Arm® Compiler for Embedded 6.

This code has been modified to demonstrate migration from Arm Compiler 5 to Arm Compiler for Embedded 6. This code requires other modifications for use in a real application.

```
// startup_ac6.c:

/*
 * Copyright (c) 2009-2017 ARM Limited. All rights reserved.
 *
 * SPDX-License-Identifier: Apache-2.0
 *
 * Licensed under the Apache License, Version 2.0 (the License); you may
 * not use this file except in compliance with the License.
 * You may obtain a copy of the License at
 *
 * www.apache.org/licenses/LICENSE-2.0
 *
 * Unless required by applicable law or agreed to in writing, software
 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
```

```

* See the License for the specific language governing permissions and
* limitations under the License.
*/

/*-----
Definitions
-----*/
#define USR_MODE 0x10          // User mode
#define FIQ_MODE 0x11         // Fast Interrupt Request mode
#define IRQ_MODE 0x12         // Interrupt Request mode
#define SVC_MODE 0x13         // Supervisor mode
#define ABT_MODE 0x17         // Abort mode
#define UND_MODE 0x1B         // Undefined Instruction mode
#define SYS_MODE 0x1F         // System mode

/*-----
Internal References
-----*/
void Vectors      (void) __attribute__((naked, section("RESET")));
void Reset_Handler (void) __attribute__((naked));
extern int printf(const char *format, ...);

__declspec(noreturn) int main (void)
{
    __asm("CPSIE i");
    printf("Starting main\n");
    while(1) __asm volatile("");
}
__asm(".global __use_no_semihosting");

/*-----
Exception / Interrupt Handler
-----*/
void Undef_Handler (void) __attribute__((weak, alias("Default_Handler")));
void SVC_Handler   (void) __attribute__((weak, alias("Default_Handler")));
void PAbt_Handler   (void) __attribute__((weak, alias("Default_Handler")));
void DAbt_Handler   (void) __attribute__((weak, alias("Default_Handler")));
void IRQ_Handler    (void) __attribute__((weak, alias("Default_Handler")));
void FIQ_Handler    (void) __attribute__((weak, alias("Default_Handler")));

/*-----
Exception / Interrupt Vector Table
-----*/
void Vectors(void) {
    __asm volatile(
        "LDR    PC, =Reset_Handler      \n"
        "LDR    PC, =Undef_Handler      \n"
        "LDR    PC, =SVC_Handler         \n"
        "LDR    PC, =PAbt_Handler        \n"
        "LDR    PC, =DAbt_Handler        \n"
        "NOP                                \n"
        "LDR    PC, =IRQ_Handler          \n"
        "LDR    PC, =FIQ_Handler          \n"
    );
}

/*-----
Reset Handler called on controller reset
-----*/
void Reset_Handler(void) {
    __asm volatile(

        // Mask interrupts
        "CPSID   if                        \n"

        // Put any cores other than 0 to sleep
        "MRC     p15, 0, R0, c0, c0, 5    \n" // Read MPIDR
        "ANDS    R0, R0, #3                \n"
        "goToSleep:                        \n"
        "WFINE                                \n"
        "BNE     goToSleep                \n"
    );
}

```



```
// Reset SCTL Settings
"MRC      p15, 0, R0, c1, c0, 0      \n" // Read CP15 System Control
register                                     \n"
"BIC      R0, R0, #(0x1 << 12)      \n" // Clear I bit 12 to disable
I Cache                                     \n"
"BIC      R0, R0, #(0x1 << 2)       \n" // Clear C bit 2 to disable
D Cache                                     \n"
"BIC      R0, R0, #0x1               \n" // Clear M bit 0 to disable
MMU                                         \n"
"BIC      R0, R0, #(0x1 << 11)      \n" // Clear Z bit 11 to disable
branch prediction                         \n"
"BIC      R0, R0, #(0x1 << 13)      \n" // Clear V bit 13 to disable
hivects                                     \n"
"MCR      p15, 0, R0, c1, c0, 0      \n" // Write value back to CP15
System Control register
"ISB                                         \n"

// Configure ACTLR
"MRC      p15, 0, r0, c1, c0, 1      \n" // Read CP15 Auxiliary
Control Register                          \n"
"ORR      r0, r0, #(1 << 1)         \n" // Enable L2 prefetch hint
(UNK/WI since r4p1)
"MCR      p15, 0, r0, c1, c0, 1      \n" // Write CP15 Auxiliary
Control Register

// Set Vector Base Address Register (VBAR) to point to this application's vector
table
"LDR      R0, =Vectors                \n"
"MCR      p15, 0, R0, c12, c0, 0      \n"

// Setup Stack for each exceptional mode
"CPS      #0x11                      \n"
"LDR      SP, =Image$$FIQ_STACK$$ZI$$Limit \n"
"CPS      #0x12                      \n"
"LDR      SP, =Image$$IRQ_STACK$$ZI$$Limit \n"
"CPS      #0x13                      \n"
"LDR      SP, =Image$$SVC_STACK$$ZI$$Limit \n"
"CPS      #0x17                      \n"
"LDR      SP, =Image$$ABT_STACK$$ZI$$Limit \n"
"CPS      #0x1B                      \n"
"LDR      SP, =Image$$UND_STACK$$ZI$$Limit \n"
"CPS      #0x1F                      \n"
"LDR      SP, =Image$$ARM_LIB_STACK$$ZI$$Limit \n"

// Call SystemInit
"BL      SystemInit                  \n"

// Unmask interrupts
"CPSIE   if                          \n"

// Call main
"BL      main                        \n"
);
}

/*-----
Default Handler for Exceptions / Interrupts
*-----*/
void Default_Handler(void) {
    while(1);
}
```

Related information

[Apache License](#) on page 130

8. Licenses

Describes the Apache license.

8.1 Apache License

Version 2.0, January 2004

<http://www.apache.org/licenses/> TERMS AND CONDITIONS FOR USE, REPRODUCTION, AND DISTRIBUTION

1. Definitions. "License" shall mean the terms and conditions for use, reproduction, and distribution as defined by Sections 1 through 9 of this document.

"Licensor" shall mean the copyright owner or entity authorized by the copyright owner that is granting the License.

"Legal Entity" shall mean the union of the acting entity and all other entities that control, are controlled by, or are under common control with that entity. For the purposes of this definition, "control" means (i) the power, direct or indirect, to cause the direction or management of such entity, whether by contract or otherwise, or (ii) ownership of fifty percent (50%) or more of the outstanding shares, or (iii) beneficial ownership of such entity.

"You" (or "Your") shall mean an individual or Legal Entity exercising permissions granted by this License.

"Source" form shall mean the preferred form for making modifications, including but not limited to software source code, documentation source, and configuration files.

"Object" form shall mean any form resulting from mechanical transformation or translation of a Source form, including but not limited to compiled object code, generated documentation, and conversions to other media types.

"Work" shall mean the work of authorship, whether in Source or Object form, made available under the License, as indicated by a copyright notice that is included in or attached to the work (an example is provided in the Appendix below).

"Derivative Works" shall mean any work, whether in Source or Object form, that is based on (or derived from) the Work and for which the editorial revisions, annotations, elaborations, or other modifications represent, as a whole, an original work of authorship. For the purposes of this License, Derivative Works shall not include works that remain separable from, or merely link (or bind by name) to the interfaces of, the Work and Derivative Works thereof.

"Contribution" shall mean any work of authorship, including the original version of the Work and any modifications or additions to that Work or Derivative Works thereof, that is intentionally submitted to Licensor for inclusion in the Work by the copyright owner or by an individual or Legal Entity authorized to submit on behalf of the copyright owner. For the purposes of this definition, "submitted" means any form of electronic, verbal, or written

communication sent to the Licensor or its representatives, including but not limited to communication on electronic mailing lists, source code control systems, and issue tracking systems that are managed by, or on behalf of, the Licensor for the purpose of discussing and improving the Work, but excluding communication that is conspicuously marked or otherwise designated in writing by the copyright owner as "Not a Contribution."

"Contributor" shall mean Licensor and any individual or Legal Entity on behalf of whom a Contribution has been received by Licensor and subsequently incorporated within the Work.

2. Grant of Copyright License. Subject to the terms and conditions of this License, each Contributor hereby grants to You a perpetual, worldwide, non-exclusive, no-charge, royalty-free, irrevocable copyright license to reproduce, prepare Derivative Works of, publicly display, publicly perform, sublicense, and distribute the Work and such Derivative Works in Source or Object form.
3. Grant of Patent License. Subject to the terms and conditions of this License, each Contributor hereby grants to You a perpetual, worldwide, non-exclusive, no-charge, royalty-free, irrevocable (except as stated in this section) patent license to make, have made, use, offer to sell, sell, import, and otherwise transfer the Work, where such license applies only to those patent claims licensable by such Contributor that are necessarily infringed by their Contribution(s) alone or by combination of their Contribution(s) with the Work to which such Contribution(s) was submitted. If You institute patent litigation against any entity (including a cross-claim or counterclaim in a lawsuit) alleging that the Work or a Contribution incorporated within the Work constitutes direct or contributory patent infringement, then any patent licenses granted to You under this License for that Work shall terminate as of the date such litigation is filed.
4. Redistribution. You may reproduce and distribute copies of the Work or Derivative Works thereof in any medium, with or without modifications, and in Source or Object form, provided that You meet the following conditions:
 - a. You must give any other recipients of the Work or Derivative Works a copy of this License; and
 - b. You must cause any modified files to carry prominent notices stating that You changed the files; and
 - c. You must retain, in the Source form of any Derivative Works that You distribute, all copyright, patent, trademark, and attribution notices from the Source form of the Work, excluding those notices that do not pertain to any part of the Derivative Works; and
 - d. If the Work includes a "NOTICE" text file as part of its distribution, then any Derivative Works that You distribute must include a readable copy of the attribution notices contained within such NOTICE file, excluding those notices that do not pertain to any part of the Derivative Works, in at least one of the following places: within a NOTICE text file distributed as part of the Derivative Works; within the Source form or documentation, if provided along with the Derivative Works; or, within a display generated by the Derivative Works, if and wherever such third-party notices normally appear. The contents of the NOTICE file are for informational purposes only and do not modify the License. You may add Your own attribution notices within Derivative Works that You distribute, alongside or as an addendum to the NOTICE text from the Work, provided that such additional attribution notices cannot be construed as modifying the License. You may add Your own copyright statement to Your modifications and may provide additional or different license terms and conditions for use, reproduction, or distribution of Your modifications, or for any

such Derivative Works as a whole, provided Your use, reproduction, and distribution of the Work otherwise complies with the conditions stated in this License.

5. **Submission of Contributions.** Unless You explicitly state otherwise, any Contribution intentionally submitted for inclusion in the Work by You to the Licensor shall be under the terms and conditions of this License, without any additional terms or conditions. Notwithstanding the above, nothing herein shall supersede or modify the terms of any separate license agreement you may have executed with Licensor regarding such Contributions.
6. **Trademarks.** This License does not grant permission to use the trade names, trademarks, service marks, or product names of the Licensor, except as required for reasonable and customary use in describing the origin of the Work and reproducing the content of the NOTICE file.
7. **Disclaimer of Warranty.** Unless required by applicable law or agreed to in writing, Licensor provides the Work (and each Contributor provides its Contributions) on an "AS IS" BASIS, WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied, including, without limitation, any warranties or conditions of TITLE, NON-INFRINGEMENT, MERCHANTABILITY, or FITNESS FOR A PARTICULAR PURPOSE. You are solely responsible for determining the appropriateness of using or redistributing the Work and assume any risks associated with Your exercise of permissions under this License.
8. **Limitation of Liability.** In no event and under no legal theory, whether in tort (including negligence), contract, or otherwise, unless required by applicable law (such as deliberate and grossly negligent acts) or agreed to in writing, shall any Contributor be liable to You for damages, including any direct, indirect, special, incidental, or consequential damages of any character arising as a result of this License or out of the use or inability to use the Work (including but not limited to damages for loss of goodwill, work stoppage, computer failure or malfunction, or any and all other commercial damages or losses), even if such Contributor has been advised of the possibility of such damages.
9. **Accepting Warranty or Additional Liability.** While redistributing the Work or Derivative Works thereof, You may choose to offer, and charge a fee for, acceptance of support, warranty, indemnity, or other liability obligations and/or rights consistent with this License. However, in accepting such obligations, You may act only on Your own behalf and on Your sole responsibility, not on behalf of any other Contributor, and only if You agree to indemnify, defend, and hold each Contributor harmless for any liability incurred by, or claims asserted against, such Contributor by reason of your accepting any such warranty or additional liability.

END OF TERMS AND CONDITIONS

APPENDIX: HOW TO APPLY THE APACHE LICENSE TO YOUR WORK

To apply the Apache License to your work, attach the following boilerplate notice, with the fields enclosed by brackets "[]" replaced with your own identifying information. (Don't include the brackets!) The text should be enclosed in the appropriate comment syntax for the file format. We also recommend that a file or class name and description of purpose be included on the same "printed page" as the copyright notice for easier identification within third-party archives.

```
Copyright [yyyy] [name of copyright owner]

Licensed under the Apache License, Version 2.0 (the "License");
you may not use this file except in compliance with the License.
You may obtain a copy of the License at

    http://www.apache.org/licenses/LICENSE-2.0
```

Unless required by applicable law or agreed to in writing, software distributed under the License is distributed on an "AS IS" BASIS, WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied. See the License for the specific language governing permissions and limitations under the License.

Proprietary Notice

This document is protected by copyright and other related rights and the use or implementation of the information contained in this document may be protected by one or more patents or pending patent applications. No part of this document may be reproduced in any form by any means without the express prior written permission of Arm Limited ("Arm"). No license, express or implied, by estoppel or otherwise to any intellectual property rights is granted by this document unless specifically stated.

Your access to the information in this document is conditional upon your acceptance that you will not use or permit others to use the information for the purposes of determining whether the subject matter of this document infringes any third party patents.

The content of this document is informational only. Any solutions presented herein are subject to changing conditions, information, scope, and data. This document was produced using reasonable efforts based on information available as of the date of issue of this document. The scope of information in this document may exceed that which Arm is required to provide, and such additional information is merely intended to further assist the recipient and does not represent Arm's view of the scope of its obligations. You acknowledge and agree that you possess the necessary expertise in system security and functional safety and that you shall be solely responsible for compliance with all legal, regulatory, safety and security related requirements concerning your products, notwithstanding any information or support that may be provided by Arm herein. In addition, you are responsible for any applications which are used in conjunction with any Arm technology described in this document, and to minimize risks, adequate design and operating safeguards should be provided for by you.

This document may include technical inaccuracies or typographical errors. THIS DOCUMENT IS PROVIDED "AS IS". ARM PROVIDES NO REPRESENTATIONS AND NO WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, SATISFACTORY QUALITY, NON-INFRINGEMENT OR FITNESS FOR A PARTICULAR PURPOSE WITH RESPECT TO THE DOCUMENT. For the avoidance of doubt, Arm makes no representation with respect to, and has undertaken no analysis to identify or understand the scope and content of, any patents, copyrights, trade secrets, trademarks, or other rights.

TO THE EXTENT NOT PROHIBITED BY LAW, IN NO EVENT WILL ARM BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES, HOWEVER CAUSED AND REGARDLESS OF THE THEORY OF LIABILITY, ARISING OUT OF ANY USE OF THIS DOCUMENT, EVEN IF ARM HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Reference by Arm to any third party's products or services within this document is not an express or implied approval or endorsement of the use thereof.

This document consists solely of commercial items. You shall be responsible for ensuring that any permitted use, duplication, or disclosure of this document complies fully with any relevant

export laws and regulations to assure that this document or any portion thereof is not exported, directly or indirectly, in violation of such export laws. Use of the word “partner” in reference to Arm’s customers is not intended to create or refer to any partnership relationship with any other company. Arm may make changes to this document at any time and without notice.

This document may be translated into other languages for convenience, and you agree that if there is any conflict between the English version of this document and any translation, the terms of the English version of this document shall prevail.

The validity, construction and performance of this notice shall be governed by English Law.

The Arm corporate logo and words marked with ® or ™ are registered trademarks or trademarks of Arm Limited (or its affiliates) in the US and/or elsewhere. Please follow Arm’s trademark usage guidelines at <https://www.arm.com/company/policies/trademarks>. All rights reserved. Other brands and names mentioned in this document may be the trademarks of their respective owners.

Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

PRE-1121-V1.0

Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in Arm documents.

Product status

All products and services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

Product completeness status

The information in this document is Final, that is for a developed product.

Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
0623-01	16 October 2024	Non-Confidential	Arm Compiler for Embedded v6.23 Release.
0622-00	13 March 2024	Non-Confidential	Arm Compiler for Embedded v6.22 Release.
0621-00	11 October 2023	Non-Confidential	Arm Compiler for Embedded v6.21 Release.
0620-00	15 March 2023	Non-Confidential	Arm Compiler for Embedded v6.20 Release.
0619-00	12 October 2022	Non-Confidential	Arm Compiler for Embedded v6.19 Release.
0618-00	22 March 2022	Non-Confidential	Arm Compiler for Embedded v6.18 Release.

Issue	Date	Confidentiality	Change
0617-00	20 October 2021	Non-Confidential	Arm Compiler for Embedded v6.17 Release.
0616-01	12 March 2021	Non-Confidential	Documentation update 1 for Arm Compiler v6.16 Release.
0616-00	3 March 2021	Non-Confidential	Arm Compiler v6.16 Release.
0615-01	14 December 2020	Non-Confidential	Documentation update 1 for Arm Compiler v6.15 Release.
0615-00	7 October 2020	Non-Confidential	Arm Compiler v6.15 Release.
0614-00	26 February 2020	Non-Confidential	Arm Compiler v6.14 Release.
0613-00	9 October 2019	Non-Confidential	Arm Compiler v6.13 Release.

Change history

The first table is for the first release. Then, each table compares the new issue of the manual with the last released issue of the manual. Release numbers match the revision history in [Document release information](#) on page 136.

Table 2: Issue 0615-01

Change	Topics affected
Added comparison for Arm Compiler 5 <code>--retain</code> option and Arm Compiler for Embedded 6 <code>-o</code> option.	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.
Corrected the miscellaneous directives translation table.	<ul style="list-style-type: none"> Miscellaneous directives.
Mentioned that <code>.equ</code> is a synonym for <code>.set</code> .	<ul style="list-style-type: none"> Symbol definition directives.
Improved explanation of when to use the volatile keyword to prevent unwanted removal of inline assembler code when building optimized output.	<ul style="list-style-type: none"> Inline assembly with Arm Compiler for Embedded 6.
Added details of the new <code>-Omin</code> compiler option.	<ul style="list-style-type: none"> Optimization differences.
Removed outdated note about using <code>__ARM_use_no_argv</code> with <code>-O0</code> optimization level in Arm Compiler for Embedded 6. The <code>-O0</code> option now supports <code>argv</code> / <code>argc</code> optimization.	<ul style="list-style-type: none"> Optimization differences.
Updated the entry for the Arm Compiler 5 <code>--multifile</code> option.	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.
Update language extension compatibility section to clarify that the <code>nomerge</code> and <code>notailcall</code> Arm Compiler 5 attributes are not supported in Arm Compiler for Embedded 6, but that the Community features <code>nomerge</code> and <code>not_tail_called</code> might be considered.	<ul style="list-style-type: none"> Language extension compatibility: attributes.
Progressive terminology commitment added to Proprietary notices section (all documents).	<ul style="list-style-type: none"> Proprietary notices

Change	Topics affected
Added a list of the changes between Arm Compiler 6.14 and Arm Compiler 6.15.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler 6.14 and Arm Compiler 6.15.

Table 3: Issue 0616-00

Change	Topics affected
A note has been added to include a <code>.balign</code> directive when defining your own sections with the <code>armclang</code> integrated assembler.	<ul style="list-style-type: none"> Alignment.
Added <code>--diag_style</code> to the Migration of command-line options section.	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.
Added note about mixing objects compiled with different C/C++ standards and the change in ABI version.	<ul style="list-style-type: none"> Changes Between Different Versions of Arm Compiler for Embedded 6.
Added note about the change in ABI version.	<ul style="list-style-type: none"> Changes Between Different Versions of Arm Compiler for Embedded 6.
Added information to reflect the change in behavior of literal pool merging when using the <code>PROTECTED</code> load region attribute.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler 6.15 and Arm Compiler 6.16.
Added a list of the changes between Arm Compiler 6.15 and Arm Compiler 6.16.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler 6.15 and Arm Compiler 6.16.

Table 4: Issue 0617-00

Change	Topics affected
Improved <code>#pragma clang</code> section documentation.	<ul style="list-style-type: none"> Language extension compatibility: pragmas.
Updated information for <code>-frtti</code> , <code>-fno-rtti</code> .	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.
Updated the table comparing command-line options in <code>armasm</code> and the integrated assembler. There is no direct equivalent for the <code>--reduce_paths</code> , <code>--no_reduce_paths</code> command-line options with the integrated assembler. Arm recommends that you avoid using long and deeply nested file paths on Windows.	<ul style="list-style-type: none"> Migration of assembler command-line options from <code>armasm</code> to the <code>armclang</code> integrated assembler.
Added a list of the changes between Arm Compiler 6.16 and Arm Compiler for Embedded 6.17.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler 6.16 and Arm Compiler for Embedded 6.17.

Table 5: Issue 0618-00

Change	Topics affected
Updated the table of differences in defaults between Arm Compiler 5 and Arm Compiler for Embedded 6.	<ul style="list-style-type: none"> Default differences.
Clarified the information about image entry points.	<ul style="list-style-type: none"> Miscellaneous directives.
Removed the note that certain GNU assembly directives were [COMMUNITY] features.	<ul style="list-style-type: none"> Migration of <code>armasm</code> macros to integrated assembler macros

Table 6: Issue 0619-00

Change	Topics affected
Added the summary of changes between Arm Compiler for Embedded 6.18 and Arm Compiler for Embedded 6.19.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler for Embedded 6.18 and Arm Compiler for Embedded 6.19.
Added details of the <code>__use_two_region_memory</code> pragma.	<ul style="list-style-type: none"> Language extension compatibility: pragmas.
Added <code>--dollar</code> and <code>-Wno-dollar-in-identifier-extension</code> to the Migration of command-line options section.	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.

Change	Topics affected
Updated the description of <code>-ffunction-sections</code> and added links to dangling debug data content.	<ul style="list-style-type: none"> Default differences.
Improved the stack protection example.	<ul style="list-style-type: none"> Arm Compiler 5 and Arm Compiler for Embedded 6 stack protection behavior.
Added a note that the <code>armasm</code> legacy assembler is deprecated.	<ul style="list-style-type: none"> Migrating from <code>armasm</code> to the <code>armclang</code> Integrated Assembler.
Added the <i>Useful resources</i> topic.	<ul style="list-style-type: none"> Useful resources.

Table 7: Issue 0620-00

Change	Topics affected
Added the summary of changes between Arm Compiler for Embedded 6.19 and Arm Compiler for Embedded 6.20.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler for Embedded 6.19 and Arm Compiler for Embedded 6.20.
Updated the description of <code>--dollar</code> and <code>-Wno-dollar-in-identifier-extension</code> in the <i>Migration of command-line options</i> section.	<ul style="list-style-type: none"> Migration of compiler command-line options from Arm Compiler 5 to Arm Compiler for Embedded 6.
Clarified that the implementation of <code>.ARM.__at_address</code> in Arm Compiler for Embedded 6 is different to the implementation in Arm Compiler 5.	<ul style="list-style-type: none"> Language extension compatibility: attributes.
Updated the description of the <code>.global</code> directive.	<ul style="list-style-type: none"> Miscellaneous directives.

Table 8: Issue 0621-00

Change	Topics affected
Added the summary of changes between Arm Compiler for Embedded 6.20 and Arm Compiler for Embedded 6.21.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler for Embedded 6.20 and Arm Compiler for Embedded 6.21.
Changed the title and updated the description of <i>A32 and T32 instruction substitutions</i> .	<ul style="list-style-type: none"> Instruction substitutions.

Table 9: Issue 0622-00

Change	Topics affected
Added the summary of changes between Arm Compiler for Embedded 6.21 and Arm Compiler for Embedded 6.22.	<ul style="list-style-type: none"> Summary of changes between Arm Compiler for Embedded 6.21 and Arm Compiler for Embedded 6.22.
Added that <code>armclang</code> provides the <code>__attribute__((target("arm" "thumb")))</code> function attribute as an alternative to the Arm Compiler 5 pragmas <code>#pragma arm</code> and <code>#pragma thumb</code> .	<ul style="list-style-type: none"> Language extension compatibility: pragmas

Table 10: Issue 0623-01

Change	Topics affected
Moved the topic <i>Compiling with <code>-mexecute-only</code> generates an empty <code>.text</code> section</i> to the <i>User Guide</i> .	-.
Minor updates for <code>__sqrt</code> and <code>__sqrtf</code> .	<ul style="list-style-type: none"> Language extension compatibility: intrinsics

Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

Typographic conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
<i>italic</i>	Citations.
bold	Interface elements, such as menu names. Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <div>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></div>
SMALL CAPITALS	Terms that have specific technical meanings as defined in the <i>Arm® Glossary</i> . For example, IMPLEMENTATION DEFINED , IMPLEMENTATION SPECIFIC , UNKNOWN , and UNPREDICTABLE .



We recommend the following. If you do not follow these recommendations your system might not work.



Your system requires the following. If you do not follow these requirements your system will not work.



You are at risk of causing permanent damage to your system or your equipment, or harming yourself.



This information is important and needs your attention.



A useful tip that might make it easier, better or faster to perform a task.



A reminder of something important that relates to the information you are reading.

Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Access to Arm documents depends on their confidentiality:

- Non-Confidential documents are available at developer.arm.com/documentation. Each document link in the following tables goes to the online version of the document.
- Confidential documents are available to licensees only through the product package.

Arm product resources	Document ID	Confidentiality
Arm Compiler for Embedded User Guide	100748	Non-Confidential
Arm Compiler for Embedded Reference Guide	101754	Non-Confidential
Arm Compiler for Embedded Arm C and C+ + Libraries and Floating-Point Support User Guide	100073	Non-Confidential
Arm Compiler for Embedded Errors and Warnings Reference Guide	100074	Non-Confidential
Arm Support	-	-
Manage Arm Compiler Versions	-	Non-Confidential
User-based licensing User Guide	102516	Non-Confidential
Complex Math Functions	-	Non-Confidential
Complex Matrix Multiplication	-	Non-Confidential
Complex FFT Functions	-	Non-Confidential

Arm® architecture and specifications	Document ID	Confidentiality
Arm Architecture Reference Manual for A-profile architecture	DDI 0487	Non-Confidential
ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition	DDI 0406	Non-Confidential
C++ ABI for the Arm Architecture	-	Non-Confidential
C++ Application Binary Interface Standard for the Arm 64-bit Architecture	-	Non-Confidential
Addenda to, and Errata in, the ABI for the Arm Architecture	-	Non-Confidential
Whitepaper - Armv8-M Architecture Technical Overview	-	Non-Confidential

Non-Arm resources	Document ID	Organization
GCC	-	https://gcc.gnu.org/onlinedocs/gcc
GNU Binutils	-	https://sourceware.org/binutils
Itanium C++ ABI	-	https://itanium-cxx-abi.github.io/cxx-abi

Non-Arm resources	Document ID	Organization
The Security Implications Of Compiler Optimizations On Cryptography - A Review	-	https://arxiv.org
Using Clang as a Compiler	-	https://clang.llvm.org/docs
Automatic variable initialization	-	https://reviews.llvm.org
How to Use Inline Assembly Language in C Code	-	https://gcc.gnu.org
Constraints for asm Operands	-	https://gcc.gnu.org
Constraint Modifier Characters	-	https://gcc.gnu.org