Arm® Total Compute 2023 Reference Design

1.0

Software Developer Guide

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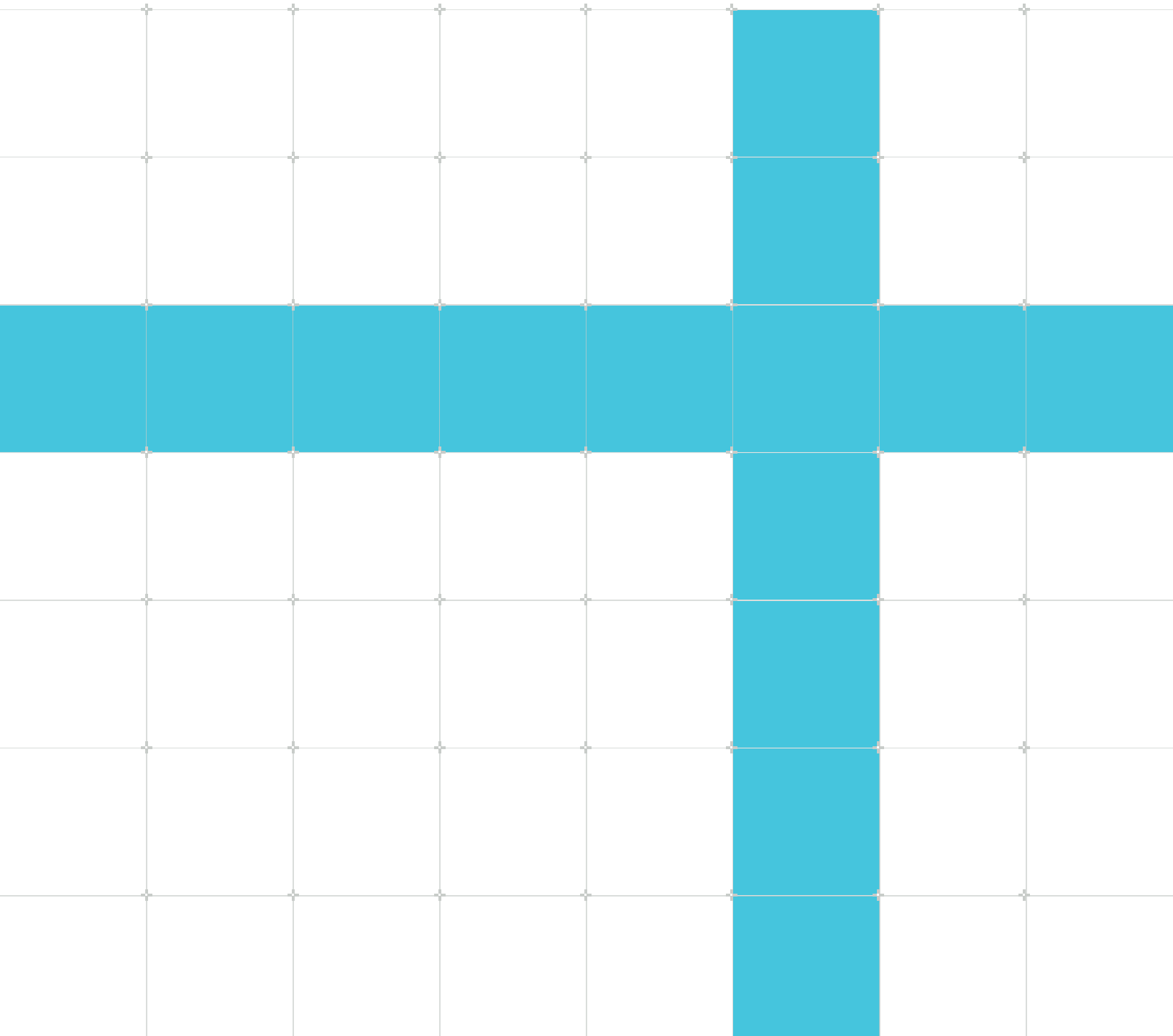

Arm® Total Compute 2023 Reference Design Software Developer Guide

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The product is 1.0.

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Start reading

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Intended audience

The Software Developer Guide is intended to assist software developers working with the Total Compute 2023 Reference Design, Open Source Software stack, and FVP.

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Contents

1. Overview of Total Compute 2023 Reference Design

The Arm® Total Compute 2023 Reference Design describes and models the design choices for the Arm Compute Subsystem for Client. The design targets the client market for smartphones, laptops, and set-top boxes. RD-TC23 incorporates 2023-generation Arm IP and technologies, other system IP, and a reference software stack targeted at Android smartphones.

The RD-TC23 *Fixed Virtual Platform* (FVP) is a functional model for software development on the recommended subsystem configurations. For more information on the Arm IP used in the FVP, see RD-TC23 Fixed Virtual Platform Details.

1.1 About Arm Development tools

Arm tools and models are designed as Arm® Success Kits for partner access, supporting hardware SoC development and software development.

To understand Success Kits and their use cases, see the Data Sheet, or visit Arm Success Kits for more information.

1.2 Deliverables

Arm provides documentation, an FVP, and a reference software stack to help you develop software.

Total Compute 2023 Reference Design Software Developer Guide

This guide provides a high-level overview of RD-TC23, the architecture from which the RD-TC23 design has been derived, the associated software stack, and the FVP.

Fixed Virtual Platform

The *Fixed Virtual Platform* (FVP) provides a software model of the RD-TC23 reference mobile configuration design. The FVP models the programmer's view of the design, allowing programmers to execute software without an actual hardware platform. The execution speeds make it possible to run Linux and Android on the model. The Total Compute software stack executes directly on the FVP. For more information on the FVP, see Total Compute on the Arm Developer website.

Total Compute Reference Software Stack

The software stack that covers all the necessary software components for a client platform, from low-level firmware to the high-level OS, including:

- The Secure software components that run in the Secure world of the design
- A starting point to modify, extend, and develop software for a SoC similar to RD-TC23.

The FVP is used with the Total Compute reference software stack. For instructions on software, and how to set up and run the FVP, see Total Compute on the Arm Developer website.

1.3 Features of RD-TC23

RD-TC23 supports the Arm®v9.2-A architecture extensions, and provides key features built around 2023-generation IP.

- A single processor cluster, build around DSU-120 in a 2+4+2 configuration:
  - Arm® Cortex®-X925 Core, Arm's next generation Cortex-X core with a step change in IPC performance raising the bar for general compute and AI performance
  - Arm® Cortex®-A725 Core, a new "big" core with up to 1 MB L2 cache
  - Arm® Cortex®-A520 Core
- Arm® Immortalis™-G925 GPU with support for ray tracing and up to 24 shader cores, Arm's most performant and efficient GPU to date. For more information, see *Ray Tracing in Vulkan®*. For a list of Arm IP used in the FVP, see RD-TC23 Fixed Virtual Platform Details.

For a high-level overview of the architecture and the IP, see System architecture.

1.4 Reference Configuration

The RD-TC23 models many of the Arm® IP involved in the subsystem, and supports a reference subsystem configuration for premium smartphones.

- 8 Armv9.2-A processor cores with *DynamIQ™ Shared Unit* (DSU) connect, in the following configuration:
  - 2 x Cortex®-X925 Core (L1D:64 KB, L1I:64 KB, L2:2 MB)
  - 4 x Cortex®-A725 Core (L1D:64 KB, L1I:64 KB, L2:1 MB)
  - 2 x Cortex®-A520 Core (L1D:64 KB, L1I:64 KB, L2:512 KB per two-core complex)
  - DynamIQ™ Shared Unit-120 (L3:16 MB, 4 cache slices)
- Arm® Immortalis™-G925 GPU with 14 cores
- Next-generation CoreLink interconnect (pre-release version) with shared 32 MB *System Level Cache* (SLC)
- Multiple expansion ports from the interconnect for multimedia components, modem, USB, sensors, and other general peripherals
- Cortex®-M85-based *System Control Processor* (SCP)
- Cortex®-M55-based *Runtime Security Engine* (RSE)
- CoreSight™ SoC-600 based debug and profiling

1.5 Compliance

The Total Compute 2023 Reference Design complies with, or includes components that comply with, the specifications listed in this section.


Remember

The *Useful resources* section at the end of this document lists all relevant specifications and their document IDs.

Confidential documents are only available to licensees through the product package, so links to online versions are not available in this document.

- *Arm® Architecture Reference Manual for A-profile architecture*
- *Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3 and version 4*
- *AMBA® 5 CHI Architecture Specification*
- *AMBA® AXI and ACE Protocol Specification*
- *AMBA® Low Power Interface Specification*
- *AMBA® CXS Protocol Specification*
- *Arm® CoreSight™ Base System Architecture 1.0, Arm Platform Design Document*
- *Arm® Power Policy Unit Architecture Specification, version 1.1*
- *Arm® System Memory Management Unit Architecture Specification, SMMU architecture version 3.2*
- *Arm Base System Architecture 1.0C*
- *Arm® Power Control System Architecture, version 2.1*
- *Arm® Platform Security Requirements, version 1.0*

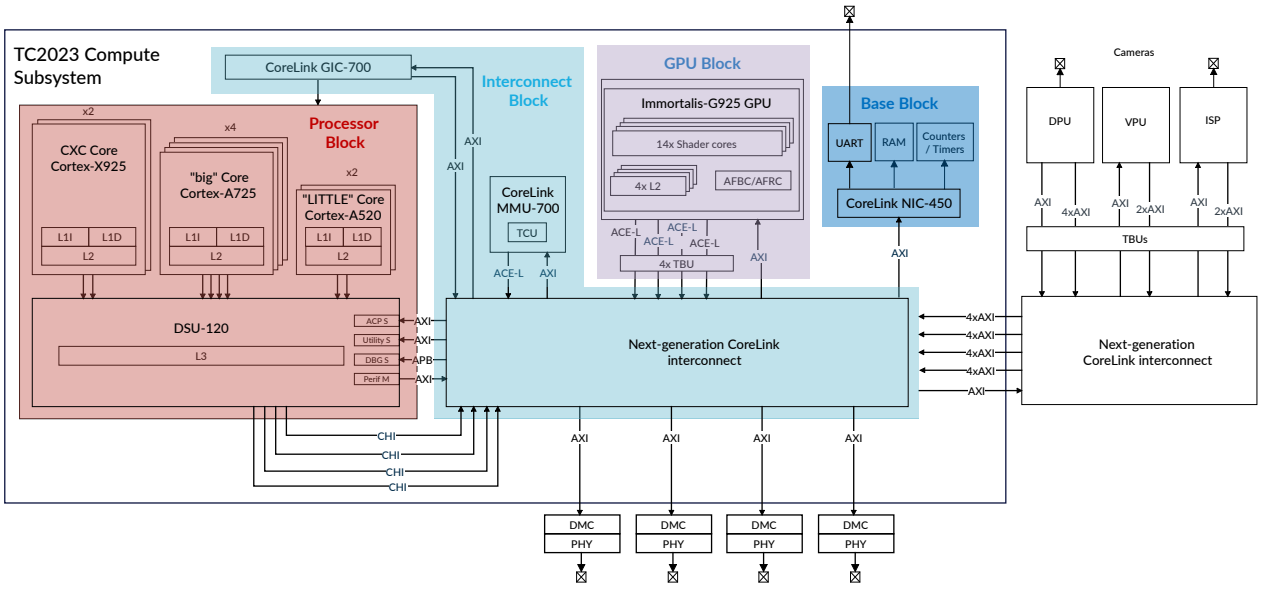
2. System architecture

The reference subsystems of RD-TC23 are partitioned into functional blocks that combine IP and its supporting logic.

Some features of the design incorporate functionality from multiple blocks. The block-based design approach provides flexibility, scalability, and modularity.

The following figure shows the high-level architectural view of the Mobile reference subsystem.

Figure 2-1: System Architecture



2.1 Processor Block

The Processor Block contains Arm® v9.2-A cores wrapped in the *DynamIQ™ Shared Unit* (DSU) along with other support logic such as debug logic reset generation, and clock generation.

2.1.1 Cores

Three tiers of Arm® v9.2-A cores are used in the Processor Block for achieving optimal balance between performance and power while running various workloads.

Cortex-X Custom (CXC) core: Cortex®-X925 Core

Built for pushing performance by adding extra hardware resources. It boosts the maximum single-thread performance of the premium tier solution.

“big” core: Cortex®-A725 Core

Designed for high performance while maintaining a certain level of power efficiency. It does the heavy lifting and improves the overall performance of the system.

“LITTLE” core: Cortex®-A520 Core

Designed for high-efficiency, low-power. It improves the system efficiency while the workload is low.

For more information on the cores, see the following documents:

- *Arm® Cortex®-X925 Core Technical Reference Manual*
- *Arm® Cortex®-X925 Core Cryptographic Extension Technical Reference Manual*
- *Arm® Cortex®-A725 Core Technical Reference Manual*
- *Arm® Cortex®-A725 Core Cryptographic Extension Technical Reference Manual*
- *Arm® Cortex®-A520 Core Technical Reference Manual*
- *Arm® Cortex®-A520 Core Cryptographic Extension Technical Reference Manual*

2.1.2 DSU cluster

The DynamIQ™ Shared Unit, DSU-120 provides a shared L3 memory system, snoop control and filtering, and other control logic to support a cluster of A-class architecture cores. The cluster is called a DSU cluster.

The L3 cache system and external system interconnect are clocked synchronously in integer multiple ratio to minimize memory access latency.

For more information on the DSU and its parameters, see the *Arm® DynamIQ™ Shared Unit-120 Technical Reference Manual*.

2.2 GPU Block

The GPU Block consists of an Arm® Immortalis™-G925 GPU, *Translation Buffer Unit* (TBU) of the *System Memory Management Unit* (SMMU), and other supporting logic.

The Arm® Immortalis™ GPU family supports configurable shader cores for different *Power, Performance, and Area* (PPA) targets. Arm® Immortalis™ GPUs also support Arm® graphic compression technology, which significantly reduces their bandwidth to main memory, reducing power consumption and improving overall system performance.

2.3 Interconnect Block

The Interconnect Block provides data paths between all other blocks through its interconnect components. It also contains the *Generic Interrupt Controller* (GIC) for application processor interrupt generation, and one of the *System Memory Management Units* (SMMU) for address translation.

Key features of the main IP in the Interconnect Block include the following:

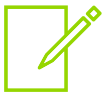
- Next-generation CoreLink interconnect designed for Mali GPU workflows, Performance predictability, and accessible to all components in the system.
- The CoreLink™ GIC-700 provides interrupt services to the application processor. The GIC Distributor communicates with the GIC Cluster Interface located inside the DSU through an Advanced eXtensible Interface 4 Stream (AXI4-stream) link.
- The CoreLink™ MMU-700 provides address translation to requesters which do not have a built-in MMU. It uses a distributed structure which separates the *Translation Control Unit* (TCU) and *Translation Buffer Unit* (TBU) for easy integration and implementation. The TCU and TBUs are connected using *Direct Translation Interface* (DTI) links.

For more information, see the following:

- *Arm® CoreLink™ GIC-700 Generic Interrupt Controller Technical Reference Manual*
- *Arm® CoreLink™ MMU-700 System Memory Management Unit Technical Reference Manual*

2.4 Base Block

The Base Block contains on-chip memory and system peripherals for *Application Processors* (APs).


Note

NIC-400 is part of the CoreLink™ NIC-450 Network Interconnect IP package.

APs can access memory and peripherals through the *Advanced eXtensible Interface* (AXI) connected to the system main interconnect. Arm® TrustZone® technology supports two sets of memory and peripherals for Secure and Non-secure applications as shown in the following table.

Table 2-1: Memories and system peripherals of Base Block

Name	Description
Secure ROM	Contains the code for initializing the boot process. It is accessible only in Secure mode. For more information on memories and peripherals, see AP memory map
Secure RAM	Scratch RAM used by Secure applications processor software. It is accessible only in Secure mode. For more information on memories and peripherals, see AP memory map

Name	Description
Non-secure ROM	Contains code required during firmware updates. It is accessible in both Secure and Non-secure modes. For more information on memories and peripherals, see AP memory map
Non-secure RAM	Scratch RAM used by Non-secure applications processor software. It is accessible in both Secure and Non-secure modes. For more information on memories and peripherals, see AP memory map
Secure UART	PrimeCell PL011 *Universal Asynchronous Receiver Transmitter* (UART) It is accessible only in Secure mode.
Non-secure UART	PrimeCell PL011 UART It is accessible in both Secure and Non-secure modes.
Secure Watchdog	Generic Watchdog Timer for Secure applications
Non-secure Watchdog	Generic Watchdog Timer for Non-secure applications
Secure timer	Generic timer for Secure applications
Non-secure timer	Generic timer for Non-secure applications

For more information on the PrimeCell PL011 UART, see the *PrimeCell UART (PL011) Technical Reference Manual*.

For more information on the NIC-400 Interconnect, see the *Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual*.

3. RD-TC23 Fixed Virtual Platform Details

Arm *Fixed Virtual Platform* (FVP) models use Arm Fast Models technology to deliver fast simulations of Arm-based systems. They allow you to develop software ahead of hardware availability and to explore the design from a software perspective. You can efficiently develop software and firmware by using the FVP together with the corresponding software stack, reducing the amount of development work.

The Arm FVP models a *Programmer's View* (PV) of processors and other components in a system. A PV provides functional behavior equivalent to what a programmer sees using the hardware. The PV sacrifices timing accuracy to achieve fast simulation execution speeds. Therefore, you can use the FVP to confirm software functionality, but must not rely on the accuracy of cycle counts, low-level component interactions, or other hardware-specific behavior. Neither can you use the FVP to measure software performance.

Total Compute FVPs are standalone executables for Linux. They are not customizable, although some aspects of their behavior can be configured through command-line parameters.

For more information on the Fixed Virtual Platforms, see the following documentation:

- *Fast Models Fixed Virtual Platforms (FVP) Reference Guide*
- *Fast Models Reference Guide*

Reference software stacks are described in Software.

3.1 About Total Compute 2023 Reference Design FVP

The Total Compute 2023 Reference Design (RD-TC23) *Fixed Virtual Platform* (FVP) models the key components of premium mobile reference subsystems.

- Arm® Cortex®-X925 Core
- Arm® Cortex®-A725 Core
- Arm® Cortex®-A520 Core
- Arm® DynamIQ™ Shared Unit-120
- Arm® Immortalis™-G925 GPU
- Arm® CoreLink™ GIC-700 Generic Interrupt Controller
- Arm® CoreLink™ MMU-700 *Memory Management Unit* (MMU)
- *System Control Processor* (SCP) based on the Arm® Cortex®-M85 processor
- Arm® CoreLink™ NIC-450 Network Interconnect

- Arm® CoreLink™ TZC-400 Address Space Controller
- Arm® CoreLink™ PCK-600 Power Control Kit
- On-Chip ROM, RAM, and other peripherals
- Clock generators with support for dynamic clock gating

The FVP does not model every component in the reference subsystem. For example, the following subsystem components are not included.

- Arm® CoreSight™ System-on-Chip SoC-600
- Third-party *Dynamic Memory Controller* (DMC)

See Total Compute on the Arm Developer website for instructions on software, and how to set up and run the FVP.

3.2 Rest of the System

As its name suggests, the *Rest of the System* (RoS) contains the components that do not reside in the RD-TC23 reference subsystem. These components create the necessary environment for running and developing a software stack.

The RD-TC23 *Fixed Virtual Platform* (FVP) includes and represents the following parts of a system:

- *Compute Subsystem* (CSS)
- *System on Chip* (SoC) which contains the CSS
- Board that contains the SoC

The SoC and board that contain it are covered by the RoS.

Similar to how the CSS should be integrated in an SoC and a board, the RoS components connect to the CSS through its expansion interfaces. This adds to the expansion sections of the memory map and interrupt map of the CSS.

The following table lists the components used inside the RoS.

Table 3-1: List of RoS components

Component name	Function
ADB-400	AMBA domain bridge
NIC-400	Fixed configuration AMBA bus matrix
PL354 SMC	Dual channel combined Static memory / NAND Flash controller
SMC memory	Simple SRAM RTL model
DFI PHY	DFI DDR physical interface
LPDDR5X memory	LPDDR5X Simulation memory
TRNG	Registers for True Random Number Generator
NVCounter	Registers for Non-Volatile Counter

Component name	Function
Keys	Register block for Secure keys
PL011 UART	UART for test output
PL180 MCI	Multimedia Card Interface
PL031 RTC	Real Time clock
SP805 watchdog	Watchdog
SP804 Timer	Dual Timer
PL050 KMI	Keyboard and Mouse Interface
PL061 GPIO	General purpose I/O
PL370 HDLCD	HDLCD controller
DMA-330	DMA controller
PSRAM	Pseudo-static DRAM
SMSC 91C111	SMSC 91C111 Ethernet controller

3.2.1 RoS memory map

The RoS memory sections are mapped to the *Compute Subsystem* (CSS) AP memory map Expansion AXI space.

The RoS sections are mapped at the following address ranges.

- `0x000_0800_0000-0x000_1FFF_FFFF`
- `0x000_6000_0000-0x000_7FFF_FFFF`

The following table shows the memory sections and their mapping.

Table 3-2: RoS memory sections

RoS memory section	Beginning address in AP memory map	Size	Description
ROS_SMC_BASE0	`0x000_0800_0000`	64 MB	CS0 – Boot flash
ROS_SMC_BASE1	`0x000_0C00_0000`	64 MB	CS4 – flash (Non-secure Storage)
ROS_SMC_BASE2	`0x000_1000_0000`	64 MB	CS5 – flash (Secure storage)
ROS_SMC_BASE3	`0x000_1400_0000`	64 MB	CS1 - PSRAM
ROS_SMC_BASE4	`0x000_1800_0000`	64 MB	CS2 – Ethernet controller
ROS_BOARD_BASE	`0x000_1C00_0000`	32 MB	RoS board peripherals
PCIE_BASE	`0x000_6000_0000`	512 MB	PCIe root complexes
ROS_SOC_BASE	`0x000_7F00_0000`	32 MB	RoS SoC peripherals
SDRAM PHY	`0x000_7FB6_0000`	32 x 64 KB	SDRAM PHYs (0-31)
SMMU	`0x000_7FB0_0000`	256 KB	SMMU

For details of AP memory, see Memory maps.

RoS board components are memory-mapped to the addresses listed in the following table. The addresses are offset from ROS_BOARD_BASE.

Table 3-3: RoS board peripherals memory map

Start Address Offset	End Address Offset	Size	Component
0x00_0000	0x00_FFFF	64 KB	Reserved
0x01_0000	0x01_FFFF	64 KB	System registers
0x02_0000	0x02_FFFF	64 KB	SP810 Sysctrl
0x03_0000	0x04_FFFF	128KB	Reserved
0x05_0000	0x05_FFFF	64 KB	PL180 MCI
0x06_0000	0x06_FFFF	64 KB	KMI 0
0x07_0000	0x07_FFFF	64 KB	KMI 1
0x08_0000	0x08_FFFF	64 KB	Reserved
0x09_0000	0x09_FFFF	64 KB	UART 2
0x0A_0000	0x0A_FFFF	64 KB	UART 3
0x0B_0000	0x0E_FFFF	256 KB	Reserved
0x0F_0000	0x0F_FFFF	64 KB	SP805 Watchdog
0x10_0000	0x10_FFFF	64 KB	Reserved
0x11_0000	0x11_FFFF	64 KB	SP084 Dual Timer
0x12_0000	0x12_FFFF	64 KB	Reserved
0x13_0000	0x13_FFFF	64 KB	Virtio Block Device
0x14_0000	0x14_FFFF	64 KB	Reserved
0x15_0000	0x15_FFFF	64 KB	Virtio Net
0x16_0000	0x16_FFFF	64 KB	GPIO 2 Wire (DVI)
0x17_0000	0x17_FFFF	64 KB	RTC 0
0x18_0000	0x18_FFFF	64 KB	RTC 1
0x19_0000	0x1E_FFFF	256 KB	Reserved
0x1D_0000	0x1D_FFFF	64 KB	GPIO 0
0x1E_0000	0x1E_FFFF	64 KB	GPIO 1
0x1F_0000	0x1F_FFFF	64 KB	Reserved

RoS SoC components are memory-mapped to the addresses listed in the following table. The addresses are offset from ROS_SOC_BASE.

Table 3-4: RoS SoC peripherals memory map

Start Address Offset	End Address Offset	Size	Name
0x00_0000	0x00_FFFF	64 KB	SMMU_DMA
0x01_0000	0x01_FFFF	64 KB	SMMU_HDLCD 0
0x02_0000	0x02_FFFF	64 KB	SMMU_HDLCD 1
0x03_0000	0x03_FFFF	64 KB	SMMU_USB
0x04_0000	0xAF_FFFF	11008 KB	Reserved
0xB0_0000	0xCF_FFFF	32 x 64 KB	SDRAM PHY 0-31 (not used)

Start Address Offset	End Address Offset	Size	Name
0xD0_0000	0xDF_FFFF	1 MB	NIC GPV
0xE0_0000	0xE0_0FFF	4 KB	PVT Monitor STD
0xE1_0000	0xE1_0FFF	4 KB	PVT Monitor SoC
0xE2_0000	0xE2_0FFF	4 KB	PVT Monitor GPU
0xE3_0000	0xE3_0FFF	4 KB	PVT Monitor CPU 0
0xE4_0000	0xE4_0FFF	4 KB	PVT Monitor CPU 1
0xE5_0000	0xE5_0FFF	4 KB	Surge
0xE6_0000	0xE6_FFFF	64 KB	TRNG
0xE7_0000	0xE7_FFFF	64 KB	NV Counter
0xE8_0000	0xE8_FFFF	64 KB	Keys
0xE9_0000	0xE9_0FFF	4 KB	GPIO
0xE9_1000	0xEF_FFFF	444 KB	Reserved
0xF0_0000	0xF0_FFFF	64 KB	DMA S
0xF1_0000	0xF1_FFFF	64 KB	DMA NS
0xF2_0000	0xF2_FFFF	64 KB	PCIe Macro
0xF3_0000	0xF3_FFFF	64 KB	PCIe Root port
0xF5_0000	0xF5_FFFF	64 KB	HDLCD 1
0xF6_0000	0xF6_FFFF	64 KB	HDLCD 0
0xF7_0000	0xF7_FFFF	64 KB	UART 0
0xF8_0000	0xF8_FFFF	64 KB	UART 1
0xF9_0000	0xFC_FFFF	256 KB	Reserved
0xFD_0000	0xFD_FFFF	64 KB	SMC PL354 Cfg
0xFE_0000	0xFE_FFFF	64 KB	Platform register block
0xFF_0000	0xFF_FFFF	64 KB	SoC SOR HDLCD security override

3.2.2 RoS interrupt map

The interrupts of the RoS components are mapped to the AP expansion interrupts area of the AP interrupt map, starting at interrupt ID 128.

The following table summarizes these interrupts, where

- Interrupt ID = 128 + INTERRUPT_OFFSET
- GIC IRQ NUM = Interrupt ID - 32

Table 3-5: RoS interrupt map

INTERRUPT_OFFSET	Interrupt source
0-2	Reserved
3	RTC1
4	RTC0 (EXT_IRQ[0])
5	UART0 (EXT_IRQ[1]) (Board)

INTERRUPT_OFFSET	Interrupt source
6	UART1 (EXT_IRQ[2]) (Board)
7	KMI1
8	GPIO0
9	GPIO1
10	I2C GPIO
11	MCIINTR0
12	MCIINTR1
13	SMSC 91C111
14-18	Reserved
19	UART0 (SoC)
20	UART1 (SoC)
21	HDLCD controller 0
22	Reserved
23	Reserved
24-28	Reserved
29	HDLCD controller 1
30	Reserved
31	Reserved
32	Reserved
33	Reserved
34-41	Reserved
42	Reserved
43	TRNG
44-51	DMA1 IRQ7-0
52	DMA1 IRQ ABORT
53-73	Reserved
74	Reserved
75	Reserved
76	Reserved
99	RTCC
100	WDT
101	KMI0
102	Dual Timer
103	Reserved
104	System register – USB
105	System register – Tile
106	System register – Push button
107	System register – Ethernet

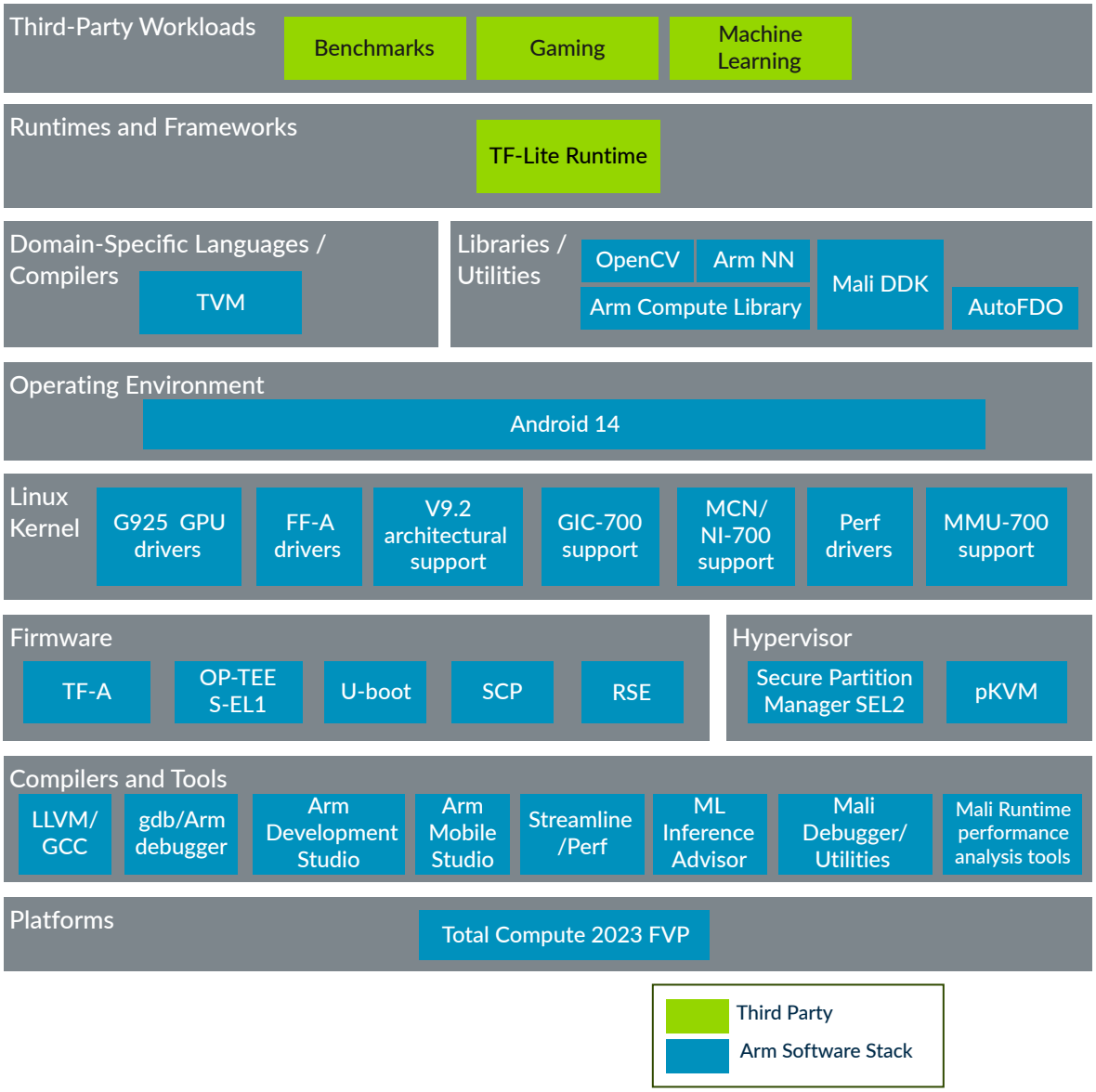
4. Software

The Total Compute reference software stack is a fully integrated open-source software stack, from Firmware up to Android. This stack enables pre-silicon software development. It provides a starting point to modify, extend, and develop the software for a *System on Chip* (SoC) based on the Total Compute reference designs. Using the software stack allows you to achieve early testing, system integration, and validation, reducing time to market and boosting product security and reliability.

The software stack includes open-source code available from the relevant upstream projects, including *System Control Processor* (SCP) firmware, Trusted firmware, Linux kernel, Android, Arm NN, and more.

Figure 4-1: Components of Total Compute 2023 software stack on page 19 shows the components of the software stack.

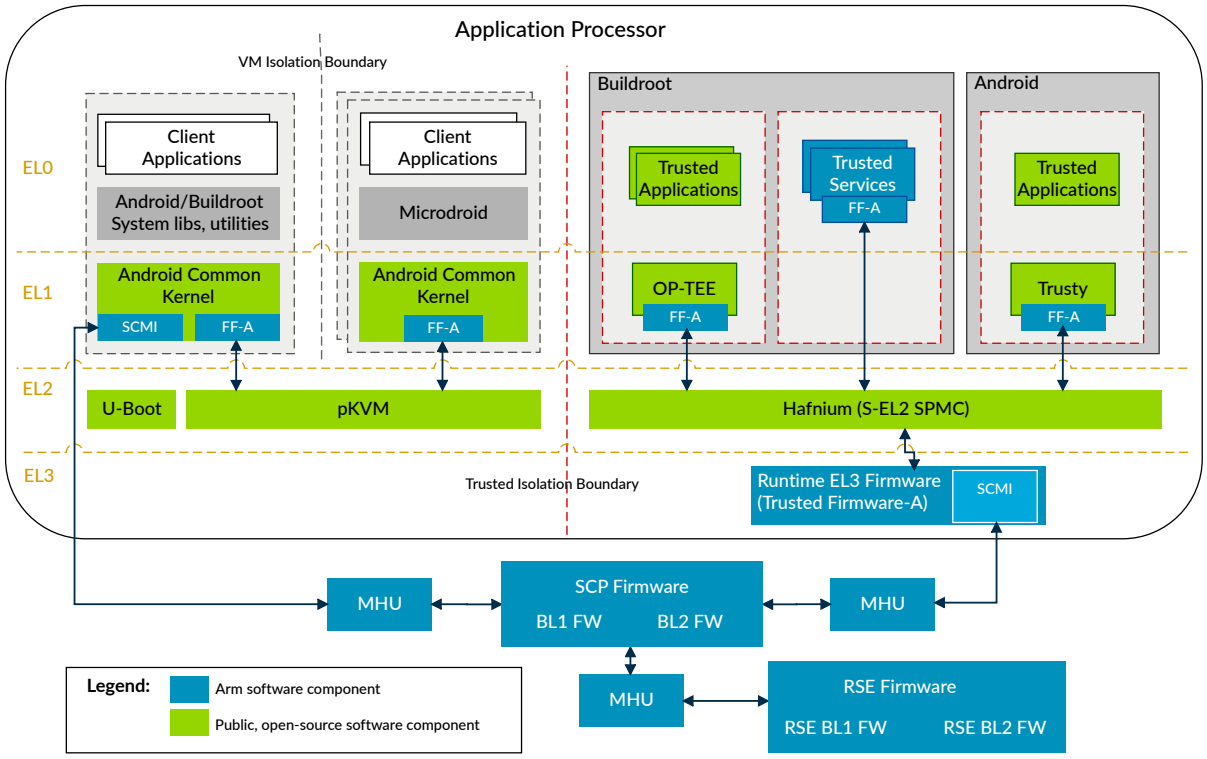
Figure 4-1: Components of Total Compute 2023 software stack



The software stack is developed and validated against the Total Compute FVP and proven on Arm® internal hardware emulation environments. See RD-TC23 Fixed Virtual Platform Details.

For a runtime view of the software stack, see Figure 4-2: Runtime view of Total Compute 2023 software stack on page 20.

Figure 4-2: Runtime view of Total Compute 2023 software stack



For more information on setting up and running the software stack on the FVP, see Total Compute on the Arm Developer website.

5. Programmer's model

You can interact with the FVP by accessing the Total Compute subsystem memory maps and interrupt maps, which are described in the following sections.

5.1 Memory maps

The *System Control Processor* (SCP) and *Application Processor* (AP) have their own memory maps.

5.1.1 AP memory map

Describes the memory map for the *Application Processor* (AP).

The AP memory map is visible to the following:

- *Application Processors* (APs)
- *System Control Processor* (SCP) (through an ATU)
- RSE (through an ATU)
- Embedded Trace Router
- Application Processor *Debug Access Port* (DAP)

These security attributes are split into the following regions:

Always Secure access

A region that is only accessible to Secure transactions. Any Non-secure access targeting these, results in a DECERR decode error response.

Secure and Non-secure access

A region that is accessible to both Secure and Non-secure transactions.

Programmable access security

Programmable access security is also known as Securable. It is a region that is defined to be independently software-configurable, and can be changed between the following states by trusted software:

- Always Secure access
- Secure and Non-secure access

These can be configured in the Network Interconnect (NIC) or in the component itself, and the default state is Secure access only from reset.

User-defined

A region that is mapped to expansion interfaces. Their access security is defined by the components outside of the Arm Total Compute 2023 Reference Design (RD-TC23) subsystem. These components must use the ARPROT[1] or AWPROT[1] bits provided on the

expansion interfaces to determine the security permission of each access. Any accesses that fail any external security checks must result in a DECERR response.

In general, unless explicitly stated otherwise:

- When a region maps a peripheral or device that occupies less than the region size used, access to the unmapped region results in a DECERR response. For example, when a peripheral occupies 4KB from the 64KB region that is reserved for it.
- Accesses to reserved areas within the memory map also result in a DECERR response. When accessing areas that peripherals or devices occupy, the peripherals or devices themselves determine the response to return. These areas can include unmapped or reserved areas within the areas that the peripheral or device occupies.
- If the SCP needs to access external peripherals that reside outside the subsystem, those peripherals should be mapped to the lower 2GB of the address space

The following table lists the memory map for the AP.

Table 5-1: AP memory map

Region	Description	Size	Address start (Hex)	Address end (Hex)	Additional information
RAM / ROM	Secure Boot RAM	512 KB	0x00_0000_0000	0x00_0007_FFFF	-
RAM / ROM	Reserved	63.5 MB	0x00_0008_0000	0x00_03FF_FFFF	-
RAM / ROM	Secure RAM	512 KB	0x00_0400_0000	0x00_0407_FFFF	-
RAM / ROM	Reserved	15.5 MB	0x00_0408_0000	0x00_04FF_FFFF	-
RAM / ROM	Reserved	512 KB	0x00_0500_0000	0x00_0507_FFFF	-
RAM / ROM	Reserved	15.5 MB	0x00_0508_0000	0x00_05FF_FFFF	-
RAM / ROM	Non-secure RAM	512 KB	0x00_0600_0000	0x00_0607_FFFF	-
RAM / ROM	Reserved	31.5 MB	0x00_0608_0000	0x00_07FF_FFFF	-
Peripheral expansion	Peripheral expansion	256 MB	0x00_0800_0000	0x00_17FF_FFFF	-
Peripheral expansion	Peripheral expansion	128 MB	0x00_1800_0000	0x00_1FFF_FFFF	Used for RoS MPS3
Reserved	Reserved	16 MB	0x00_2000_0000	0x00_20FF_FFFF	-
DMC expansion	DMC0 configuration	16 MB	0x00_2100_0000	0x00_21FF_FFFF	-
DMC expansion	DMC1 configuration	16 MB	0x00_2200_0000	0x00_22FF_FFFF	-
DMC expansion	DMC2 configuration	16 MB	0x00_2300_0000	0x00_23FF_FFFF	-

Region	Description	Size	Address start (Hex)	Address end (Hex)	Additional information
DMC expansion	DMC3 configuration	16 MB	0x00_2400_0000	0x00_24FF_FFFF	-
DMC expansion	RESERVED	16 MB	0x00_2500_0000	0x00_25FF_FFFF	-
DMC expansion	RESERVED	16 MB	0x00_2600_0000	0x00_26FF_FFFF	-
DMC expansion	RESERVED	16 MB	0x00_2700_0000	0x00_27FF_FFFF	-
DMC expansion	RESERVED	16 MB	0x00_2800_0000	0x00_28FF_FFFF	-
DMC expansion	RESERVED	20 MB	0x00_2900_0000	0x00_2A3F_FFFF	-
Base Peripherals	Non-Secure UART	64 KB	0x00_2A40_0000	0x00_2A40_FFFF	-
Base Peripherals	Secure UART	64 KB	0x00_2A41_0000	0x00_2A41_FFFF	-
Base Peripherals	RESERVED	64 KB	0x00_2A42_0000	0x00_2A42_FFFF	-
SCP	GTCLK CNTControl / RESERVED	64 KB	0x00_2A43_0000	0x00_2A43_FFFF	-
Base Peripherals	Generic Watchdog Control	64 KB	0x00_2A44_0000	0x00_2A44_FFFF	-
Base Peripherals	Generic Watchdog Refresh	64 KB	0x00_2A45_0000	0x00_2A45_FFFF	-
Base Peripherals	RESERVED	128 KB	0x00_2A46_0000	0x00_2A47_FFFF	-
Base Peripherals	Trusted Watchdog Control	64 KB	0x00_2A48_0000	0x00_2A48_FFFF	-
Base Peripherals	Trusted Watchdog Refresh	64 KB	0x00_2A49_0000	0x00_2A49_FFFF	-
SCP	System ID registers / RESERVED	64 KB	0x00_2A4A_0000	0x00_2A4A_FFFF	-
Base Peripherals	RESERVED	3.3 MB	0x00_2A4B_0000	0x00_2A7F_FFFF	-
SCP	GTCLK CNTRead / RESERVED	64 KB	0x00_2A80_0000	0x00_2A80_FFFF	-
Base Peripherals	AP_GTCLK_CNTCTL	64 KB	0x00_2A81_0000	0x00_2A81_FFFF	-
Base Peripherals	AP_GTCLK_S_CNTBase0	64 KB	0x00_2A82_0000	0x00_2A82_FFFF	-
Base Peripherals	AP_GTCLK_NS_CNTBase1	64 KB	0x00_2A83_0000	0x00_2A83_FFFF	-
Base Peripherals	RESERVED	35.8 MB	0x00_2A84_0000	0x00_2CBF_FFFF	-
DPU	Display Block	3 MB	0x40_0000_0000	0x40_005F_FFFF	-

Region	Description	Size	Address start (Hex)	Address end (Hex)	Additional information
DPU	RESERVED	1 MB	0x40_0060_0000	0x40_007F_FFFF	-
GPU	GPU Block	16 MB	0x00_2D00_0000	0x00_2DFF_FFFF	-
GPU	RESERVED	32 MB	0x00_2E00_0000	0x00_2FFF_FFFF	-
GIC	GIC	128 MB	0x00_3000_0000	0x00_37FF_FFFF	-
GIC	RESERVED	112 MB	0x00_3800_0000	0x00_3EFF_FFFF	-
SMMU	SMMU0 (GPU)	80 MB	0x00_3F00_0000	0x00_43FF_FFFF	-
SMMU	RESERVED	16 MB	0x00_4400_0000	0x00_44FF_FFFF	-
SMS	SCP	64 MB	0x00_4500_0000	0x00_48FF_FFFF	-
SMS	RSS	64 MB	0x00_4900_0000	0x00_4CFF_FFFF	-
SMS	RESERVED	1 MB	0x00_4D00_0000	0x00_4D0F_FFFF	-
SMS	RESERVED	31 MB	0x00_4D10_0000	0x00_4EFF_FFFF	-
Interconnect	NCI/MCN-data GPV	64 MB	0x00_4F00_0000	0x00_52FF_FFFF	Depending on config; expect 16MB used
Interconnect	NCI-per GPV	64 MB	0x00_5300_0000	0x00_56FF_FFFF	Depending on config; expect <MB used
Interconnect		0	0x00_5700_0000	0x00_56FF_FFFF	-
PIK	PIKs	16 MB	0x00_5700_0000	0x00_57FF_FFFF	-
RESERVED	RESERVED	16 MB	0x00_5800_0000	0x00_58FF_FFFF	-
RESERVED /	RESERVED	64 MB	0x00_5900_0000	0x00_5CFF_FFFF	-
Debug	STM	16 MB	0x00_5D00_0000	0x00_5DFF_FFFF	-
Debug	RESERVED	8 MB	0x00_5E00_0000	0x00_5E7F_FFFF	-
Debug	RESERVED	8 MB	0x00_5E80_0000	0x00_5EFF_FFFF	-
DSU	Cluster0 Utility space	8 MB	0x00_5F00_0000	0x00_5F7F_FFFF	0x01_0000->0x01_ffff and 0x04_0000->0x04_ffff must be accessible by AP cores (for MPAM and AMU registers), but other ranges cannot be
DSU	RESERVED	8 MB	0x00_5F80_0000	0x00_5FFF_FFFF	-
Peripheral expansion	Peripheral expansion	128 MB	0x00_6000_0000	0x00_67FF_FFFF	Used for RoS MPS3

Region	Description	Size	Address start (Hex)	Address end (Hex)	Additional information
Peripheral expansion	Peripheral expansion	128 MB	0x00_6800_0000	0x00_6FFF_FFFF	-
Peripheral expansion		64 MB	0x00_7000_0000	0x00_73FF_FFFF	-
Peripheral expansion	Peripheral expansion	64 MB	0x00_7400_0000	0x00_77FF_FFFF	-
Peripheral expansion	Peripheral expansion	64 MB	0x00_7800_0000	0x00_7BFF_FFFF	-
Peripheral expansion	Peripheral expansion	64 MB	0x00_7C00_0000	0x00_7FFF_FFFF	-
-	DRAM	2 GB	0x00_8000_0000	0x00_FFFF_FFFF	striped
-	RESERVED	12 GB	0x01_0000_0000	0x03_FFFF_FFFF	-
Debug	Debug memory map (CSS)	512 MB	0x04_0000_0000	0x04_1FFF_FFFF	-
Debug	Debug memory map (RoS)	512 MB	0x04_2000_0000	0x04_3FFF_FFFF	-
-	RESERVED	7 GB	0x04_4000_0000	0x05_FFFF_FFFF	-
-	RESERVED	2 GB	0x06_0000_0000	0x06_7FFF_FFFF	-
-	RESERVED	2 GB	0x06_8000_0000	0x06_FFFF_FFFF	-
-	RESERVED	2 GB	0x07_0000_0000	0x07_7FFF_FFFF	-
-	RESERVED	2 GB	0x07_8000_0000	0x07_FFFF_FFFF	-
-	HOLE	2 GB	0x08_0000_0000	0x08_7FFF_FFFF	striped
-	DRAM	30 GB	0x08_8000_0000	0x0F_FFFF_FFFF	striped
-	RESERVED	192 GB	0x10_0000_0000	0x3F_FFFF_FFFF	-
-	Peripheral expansion	256 GB	0x40_0000_0000	0x7F_FFFF_FFFF	Mapped to the Peripheral expansion tab
-	HOLE	32 GB	0x80_0000_0000	0x87_FFFF_FFFF	striped
-	DRAM	480 GB	0x88_0000_0000	0x100_0000_0000	striped

5.1.1.1 SMS region memory map

The SMS Block integrates the Runtime Security Engine and System Control Processor.

Table 5-2: SMS region memory map

Region	Description	Size	Address start (Hex)	Address end (Hex)	Access permission (by static NCI config.)
RESERVED	RESERVED	512 KB	0x00_0000_0000	0x00_0007_FFFF	-
RESERVED	RESERVED	512 KB	0x00_0008_0000	0x00_000F_FFFF	-
RESERVED	RESERVED	3 MB	0x00_0010_0000	0x00_003F_FFFF	-
-	RESERVED	4 MB	0x00_0040_0000	0x00_007F_FFFF	-
-	RESERVED	8 MB	0x00_0080_0000	0x00_00FF_FFFF	-
S-MHU	AP_SCP_MHU_0_s	64 KB	0x00_0100_0000	0x00_0100_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_1_s	64 KB	0x00_0101_0000	0x00_0101_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_2_s	64 KB	0x00_0102_0000	0x00_0102_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_3_s	64 KB	0x00_0103_0000	0x00_0103_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_4_s	64 KB	0x00_0104_0000	0x00_0104_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_5_s	64 KB	0x00_0105_0000	0x00_0105_FFFF	AP and AXIAP-SYS only
S-MHU	AP_SCP_MHU_6_s	64 KB	0x00_0106_0000	0x00_0106_FFFF	AP and AXIAP-SYS only
S-MHU	Reserved	576 KB	0x00_0107_0000	0x00_010F_FFFF	AP and AXIAP-SYS only
S-MHU	SCP_AP_MHU_0_r	64 KB	0x00_0110_0000	0x00_0110_FFFF	D2D only
S-MHU	SCP_AP_MHU_1_r	64 KB	0x00_0111_0000	0x00_0111_FFFF	-
S-MHU	SCP_AP_MHU_2_r	64 KB	0x00_0112_0000	0x00_0112_FFFF	-
S-MHU	SCP_AP_MHU_3_r	64 KB	0x00_0113_0000	0x00_0113_FFFF	-
S-MHU	SCP_AP_MHU_4_r	64 KB	0x00_0114_0000	0x00_0114_FFFF	-
S-MHU	SCP_AP_MHU_5_r	64 KB	0x00_0115_0000	0x00_0115_FFFF	-
S-MHU	SCP_AP_MHU_6_r	64 KB	0x00_0116_0000	0x00_0116_FFFF	-
S-MHU	Reserved	576 KB	0x00_0117_0000	0x00_011F_FFFF	-
NS-MHU	Reserved	64 KB	0x00_0120_0000	0x00_0120_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0121_0000	0x00_0121_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0122_0000	0x00_0122_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0123_0000	0x00_0123_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0124_0000	0x00_0124_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0125_0000	0x00_0125_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0126_0000	0x00_0126_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0127_0000	0x00_0127_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0128_0000	0x00_0128_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0129_0000	0x00_0129_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	384 KB	0x00_012A_0000	0x00_012F_FFFF	-

Region	Description	Size	Address start (Hex)	Address end (Hex)	Access permission (by static NCI config.)
NS-MHU	Reserved	2 MB	0x00_0130_0000	0x00_014F_FFFF	-
NS-MHU	SCP1_SCP0_MHU_0_s	2 MB	0x00_0150_0000	0x00_016F_FFFF	-
NS-MHU	Reserved	9 MB	0x00_0170_0000	0x00_01FF_FFFF	-
GTCounter	GTCLK CNTControl / Reserved	64 KB	0x00_0200_0000	0x00_0200_FFFF	-
GTCounter	GTCLK CNTRead / Reserved	64 KB	0x00_0201_0000	0x00_0201_FFFF	-
GTCounter	RESERVED	896 KB	0x00_0202_0000	0x00_020F_FFFF	-
GTCounter	GTCLK TSYNC / Reserved	64 KB	0x00_0210_0000	0x00_0210_FFFF	-
GTCounter	RESERVED	960 KB	0x00_0211_0000	0x00_021F_FFFF	-
GTCounter	RESERVED	14 MB	0x00_0220_0000	0x00_02FF_FFFF	-
MISC	System ID registers / Reserved	64 KB	0x00_0300_0000	0x00_0300_FFFF	-
MISC	RESERVED	960 KB	0x00_0301_0000	0x00_030F_FFFF	-
MISC	RESERVED	1 MB	0x00_0310_0000	0x00_031F_FFFF	-
MISC	RESERVED	2 MB	0x00_0320_0000	0x00_033F_FFFF	-
MISC	RESERVED	4 MB	0x00_0340_0000	0x00_037F_FFFF	-
MISC	RESERVED	8 MB	0x00_0380_0000	0x00_03FF_FFFF	-
S-MHU	AP_RSS_MHU_0_s	64 KB	0x00_0400_0000	0x00_0400_FFFF	APand AXIAP-SYS only
S-MHU	AP_RSS_MHU_1_s	64 KB	0x00_0401_0000	0x00_0401_FFFF	AP and AXIAP-SYS only
S-MHU	Reserved	64 KB	0x00_0402_0000	0x00_0402_FFFF	-
S-MHU	Reserved	64 KB	0x00_0403_0000	0x00_0403_FFFF	-
S-MHU	Reserved	64 KB	0x00_0404_0000	0x00_0404_FFFF	-
S-MHU	Reserved	64 KB	0x00_0405_0000	0x00_0405_FFFF	-
S-MHU	Reserved	64 KB	0x00_0406_0000	0x00_0406_FFFF	-
S-MHU	Reserved	576 KB	0x00_0407_0000	0x00_040F_FFFF	-
S-MHU	RSS_AP_MHU_0_r	64 KB	0x00_0410_0000	0x00_0410_FFFF	D2D only
S-MHU	RSS_AP_MHU_1_r	64 KB	0x00_0411_0000	0x00_0411_FFFF	-
S-MHU	Reserved	64 KB	0x00_0412_0000	0x00_0412_FFFF	-
S-MHU	Reserved	64 KB	0x00_0413_0000	0x00_0413_FFFF	-
S-MHU	Reserved	64 KB	0x00_0414_0000	0x00_0414_FFFF	-
S-MHU	Reserved	64 KB	0x00_0415_0000	0x00_0415_FFFF	-
S-MHU	Reserved	64 KB	0x00_0416_0000	0x00_0416_FFFF	-
S-MHU	Reserved	576 KB	0x00_0417_0000	0x00_041F_FFFF	-
NS-MHU	Reserved	64 KB	0x00_0420_0000	0x00_0420_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	64 KB	0x00_0421_0000	0x00_0421_FFFF	AP and AXIAP-SYS only
NS-MHU	Reserved	896 KB	0x00_0422_0000	0x00_042F_FFFF	-
NS-MHU	Reserved	64 KB	0x00_0430_0000	0x00_0430_FFFF	-

Region	Description	Size	Address start (Hex)	Address end (Hex)	Access permission (by static NCI config.)
NS-MHU	Reserved	960 KB	0x00_0431_0000	0x00_043F_FFFF	-
NS-MHU	Reserved	64 KB	0x00_0440_0000	0x00_0440_FFFF	-
NS-MHU	Reserved	960 KB	0x00_0441_0000	0x00_044F_FFFF	-
NS-MHU	RSS_RSS_MHU_0_s	64 KB	0x00_0450_0000	0x00_0450_FFFF	-
NS-MHU	Reserved	960 KB	0x00_0451_0000	0x00_045F_FFFF	-
NS-MHU	Reserved	10 MB	0x00_0460_0000	0x00_04FF_FFFF	-
MISC	RESERVED	16 MB	0x00_0500_0000	0x00_05FF_FFFF	-
MISC	RESERVED	16 MB	0x00_0600_0000	0x00_06FF_FFFF	-
MISC	RESERVED	16 MB	0x00_0700_0000	0x00_07FF_FFFF	-

5.1.1.2 PIK region memory map

The System Power Integration Kit (PIK) is only mapped into the System Control Processor (SCP) memory map. For more information, see SCP memory map.

Table 5-3: PIK region memory map

Description	Size	Address Start (Hex)	Address End (Hex)	Access permission
System PIK	256 KB	0x0000_0000	0x0003_FFFF	SCP/RSS/debug only
CPU PIK	256 KB	0x0004_0000	0x0007_FFFF	SCP/RSS/debug only
GPU PIK	256 KB	0x0008_0000	0x000B_FFFF	SCP/RSS/debug only
DBGTOP PIK	256 KB	0x000C_0000	0x000F_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0010_0000	0x0013_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0014_0000	0x0017_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0018_0000	0x001B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x001C_0000	0x001F_FFFF	SCP/RSS/debug only
SCP PIK	256 KB	0x0020_0000	0x0020_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0024_0000	0x0027_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0028_0000	0x002B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x002C_0000	0x002F_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0030_0000	0x0033_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0034_0000	0x0037_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0038_0000	0x003B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x003C_0000	0x003F_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0040_0000	0x0043_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0044_0000	0x0047_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0048_0000	0x004B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x004C_0000	0x004F_FFFF	SCP/RSS/debug only

Description	Size	Address Start (Hex)	Address End (Hex)	Access permission
RESERVED	256 KB	0x0050_0000	0x0053_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0054_0000	0x0057_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0058_0000	0x005B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x005C_0000	0x005F_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0060_0000	0x0063_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0064_0000	0x0067_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0068_0000	0x006B_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x006C_0000	0x006F_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0070_0000	0x0073_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0074_0000	0x0077_FFFF	SCP/RSS/debug only
RESERVED	256 KB	0x0078_0000	0x007B_FFFF	SCP/RSS/debug only
Display PIK	256 KB	0x007C_0000	0x007F_FFFF	SCP/RSS/debug only
RESERVED	8 MB	0x0080_0000	0x00FF_FFFF	SCP/RSS/debug only
RESERVED	0	0x00FF_FFFF	0x00FF_FFFF	SCP/RSS/debug only
RESERVED	0	0x00FF_FFFF	0x00FF_FFFF	SCP/RSS/debug only

5.1.2 SCP memory map

The *System Control Processor* (SCP) is a Cortex®-M85-based subsystem which implements a 32-bit address space. The Cortex®-M85 uses a fixed high-level memory map as specified in the *Arm®v8-M Architecture Reference Manual*.

The SCP is a Trusted CPU and will always run Trusted code. Therefore, all the regions of the SCP memory map that are not mapped to the *Application Processor* (AP) Memory Map are Secure by default.

A boot ROM and an on-chip SRAM are mapped in the bottom 512MB of the address space. The first 1MB of the top 512MB of address space is reserved for the *Private Peripheral Bus* (PPB).

This region is further divided into the following spaces:

Internal PPB

The Internal PPB space is the bottom 256KB of the PPB space and is accessed through an *Advanced High-performance Bus Lite* (AHB-Lite) bus with the SCP subsystem. The following Cortex-M85 system components are in this space:

- *System Control Space* (SCS)
- *Flash Patch and Breakpoint* (FPB)
- *Data Warehouse Trace* (DWT)
- *Instrumentation Trace Macrocell* (ITM)

For more information on Cortex-M85 address space, see the *Arm® Cortex®-M85 Processor Technical Reference Manual*.

External PPB

The External PPB space contains more Cortex-M85 system components. These are generally debug-related components like such as the SWO, *Embedded Trace Macrocell* (ETM), *Cross Trigger Interface* (CTI), SCP Funnel, and ROM Table. The rest of the address space is Reserved. The ROM table follows the format specified in the *Arm® Cortex®-M85 Processor Technical Reference Manual*, with the part number set to `0x4D0`.

For more information on Cortex-M85 address space, see the *Arm® Cortex®-M85 Processor Technical Reference Manual*.

All other address space is accessed through the Cortex-M85 system bus, and is divided into the following regions:

SCP Peripherals (64KB)

The SCP Peripherals region contains the SCP peripherals such as Generic Timers, Generic Counters, Watchdog Timer, Configuration registers, and Power registers.

External RAM (1GB)

The External RAM region is assumed to behave as Normal memory. For information on the Normal memory type, see the *Arm®v8-M Architecture Reference Manual*.

This region is mapped to a single contiguous 1GB region of the AP memory map starting at `0x00_4000_0000`. Any SCP memory accesses in the External RAM region, `0x6000_0000` to `0x9FFF_FFFF`, targets memory locations in the region `0x00_4000_0000` to `0x00_7FFF_FFFF` of the AP memory map.

This region of the AP memory map contains an expansion *Advanced eXtensible Interface* (AXI) space.

External Device (1GB)

The External Device region is intended for off-chip Device memory. For information on the Device type memory, see the *Arm®v8-M Architecture Reference Manual*.

This region is mapped to a single contiguous 1GB region of the AP memory map starting at `0x00_0000_0000`. Any SCP memory accesses in the External Device region, `0xA000_0000` to `0xDFFF_FFFF`, targets memory locations in the region `0x00_0000_0000` to `0x00_3FFF_FFFF` of the AP memory map.

This region of the AP memory map contains the Boot area, Total Compute 2023 Reference Design (RD-TC23) system peripherals, and an expansion AXI area.

Expansion AHB

The Expansion AHB region contains:

- 511MB, starting at `0x00_E010_0000`
- 64MB, starting at `0x00_4000_0000`

All vendor-specific peripherals such as the register state for controlling the *Power Management Integrated Circuit* (PMIC), *Phase-Locked Loops* (PLLs) and *Process, Voltage, and*

Temperature (PVT) sensors can be put in this space. Peripheral I/O control such as the *Serial Peripheral Interface* (SPI), *Integrated Circuit* (I2C) can also be put in this space.

This area is accessible through the SCP external AHB Expansion interface. For more information on memory types such as Device and Normal, and other recommendations regarding the use of these memory areas, see the *Arm®v8-M Architecture Reference Manual*.

Reserved

All remaining regions are Reserved. Any access targeting these regions results in a BusFault exception.

The following table lists the memory map of the System Control Processor. There are security attributes associated with each area of memory. These security attributes are defined as:

S

Secure access only.

NS

Non-secure access only.

Exempt

Any access with no security limitations.

Table 5-4: SCP memory map

Name (type)	Row ID	Start address	End address	Security	Size	Region name	Description
CODE(Normal)	1	0x0000_0000	0x00FF_FFFF	NS	16 MB	ITCM	CPU Instruction TCM up to 16MB Boot (Unused areas are reserved)
CODE(Normal)	2	0x0100_0000	0x09FF_FFFF	NS	144 MB	Main Expansion Interfaces	Manager Code Main Expansion Interface (XMSTEXPCODE)
CODE(Normal)	3	0x0A00_0000	0x0DFF_FFFF	NS	64 MB	CPUs ITCM	CPUs S-AHB Instruction TCM Access (Unused areas are reserved)
CODE(Normal)	4	0x0E00_0000	0x0FFF_FFFF	NS	32 MB	Reserved	Reserved (bus error)
CODE(Normal)	5	0x1000_0000	0x10FF_FFFF	S	16 MB	ITCM	CPU Instruction TCM up to 16MB Boot (Unused areas are reserved)
CODE(Normal)	6	0x1100_0000	0x19FF_FFFF	S	144 MB	Main Expansion Interfaces	Manager Code Main Expansion Interface (XMSTEXPCODE)
CODE(Normal)	7	0x1A00_0000	0x1DFF_FFFF	S	64 MB	CPUs ITCM	CPUs S-AHB Instruction TCM Access (Unused areas are reserved)
CODE(Normal)	8	0x1E00_0000	0x1FFF_FFFF	S	32 MB	Reserved	Reserved (bus error)
SRAM(Normal)	9	0x2000_0000	0x20FF_FFFF	NS	16 MB	DTCM	CPU Data TCM up to 16MB (Unused areas are reserved)
SRAM(Normal)	10	0x2100_0000	0x23FF_FFFF	NS	48 MB	Volatile Memory	VM1/VM2 Memory Banks (Unused areas are reserved)
SRAM(Normal)	11	0x2400_0000	0x27FF_FFFF	NS	64 MB	CPUs DTCM	CPUs S-AHB Data TCM Access

Name (type)	Row ID	Start address	End address	Security	Size	Region name	Description
SRAM(Normal)	12	0x2800_0000	0x2FFF_FFFF	NS	128 MB	Main Expansion Interfaces	Manager AXI Expansion Interface (XMSTEXPSRAM) ATU
SRAM(Normal)	13	0x3000_0000	0x30FF_FFFF	S	16 MB	DTCM	CPU Data TCM up to 16MB (Unused areas are reserved)
SRAM(Normal)	14	0x3100_0000	0x33FF_FFFF	S	48 MB	Volatile Memory	VM1/VM2 Memory Banks (Unused areas are reserved)
SRAM(Normal)	15	0x3400_0000	0x37FF_FFFF	S	64 MB	CPUs DTCM	CPUs S-AHB Data TCM Access
SRAM(Normal)	16	0x3800_0000	0x3FFF_FFFF	S	128 MB	Main Expansion Interfaces	Manager AXI Expansion Interface (XMSTEXPSRAM) ATU
PERIPHERAL (Device)	17	0x4000_0000	0x4000_FFFF	NS	64 KB	Peripheral Region	Non-secure region for low latency peripherals that are expected to be aliased in its associated Secure region, 0x5000_0000 to 0x5000_FFFF.
PERIPHERAL (Device)	18	0x4001_0000	0x4001_FFFF	NS	64 KB	CPU Private Region	CPU Private Peripheral Region Low Latency
PERIPHERAL (Device)	19	0x4002_0000	0x4003_FFFF	NS	128 KB	System Control Peripheral Region	Non-secure region for low latency system control peripherals. Some peripherals may be expected to be aliased in its associated Secure region, 0x5002_0000 to 0x5003_FFFF
PERIPHERAL (Device)	20	0x4004_0000	0x400F_FFFF	NS	768 KB	Peripheral Region	Non-secure region for low latency peripherals that are expected to be not aliased.
PERIPHERAL (Device)	21	0x4010_0000	0x47FF_FFFF	NS	127 MB	AHB Peripheral Expansion	Manager AHB Peripheral Expansion Interface (HMSTEXPPILL)
PERIPHERAL (Device)	22	0x4800_0000	0x4800_FFFF	NS	64 KB	Peripheral Region	Non-secure region for high latency peripherals that are expected to be aliased in its associated Secure region, 0x5800_0000 to 0x5800_FFFF.
PERIPHERAL (Device)	23	0x4801_0000	0x4801_FFFF	NS	64 KB	CPU Private Region	CPU Private Peripheral Region High Latency
PERIPHERAL (Device)	24	0x4802_0000	0x4803_FFFF	NS	128 KB	System Control Peripheral Region	Non-secure region for high latency system control peripherals. Some peripherals may be expected to be aliased in its associated Secure region, 0x5802_0000 to 0x5803_FFFF
PERIPHERAL (Device)	25	0x4804_0000	0x480F_FFFF	NS	768 KB	Peripheral Region	Non-secure region for high latency peripherals that are expected to be not aliased.
PERIPHERAL (Device)	26	0x4810_0000	0x4FFF_FFFF	NS	127 MB	AHB Peripheral Expansion	Manager AHB Peripheral Expansion Interface (HMSTEXPPIHL)
PERIPHERAL (Device)	27	0x5000_0000	0x5000_FFFF	S	64 KB	Peripheral Region	Secure region for low latency peripherals that are expected to be aliased in its associated Non-secure region, 0x4000_0000 to 0x4000_FFFF
PERIPHERAL (Device)	28	0x5001_0000	0x5001_FFFF	S	64 KB	CPU Private Region	CPU Private Peripheral Region Low Latency
PERIPHERAL (Device)	29	0x5002_0000	0x5003_FFFF	S	128 KB	System Control Peripheral Region	Secure region for low latency system control peripherals. Some peripherals may be expected to be aliased in its associated Non-secure region, 0x4002_0000 to 0x4003_FFFF.

Name (type)	Row ID	Start address	End address	Security	Size	Region name	Description
PERIPHERAL (Device)	30	0x5004_0000	0x500F_FFFF	S	768 KB	Peripheral Region	Secure region for low latency peripherals that are expected to be not aliased
PERIPHERAL (Device)	31	0x5010_0000	0x57FF_FFFF	S	127 MB	AHB Peripheral Expansion	Manager AHB Peripheral Expansion Interface (HMSTEXPPILL)
PERIPHERAL (Device)	32	0x5800_0000	0x5800_FFFF	S	64 KB	Peripheral Region	Secure region for high latency peripherals that are expected to be aliased in its associated Non-secure region, 0x4800_0000 to 0x4800_FFFF
PERIPHERAL (Device)	33	0x5801_0000	0x5801_FFFF	S	64 KB	CPU Private Region	CPU Private Peripheral Region High Latency
PERIPHERAL (Device)	34	0x5802_0000	0x5803_FFFF	S	128 KB	System Control Peripheral Region	Secure region for low latency system control peripherals. Some peripherals may be expected to be aliased in its associated Non-secure region, 0x4802_0000 to 0x4803_FFFF.
PERIPHERAL (Device)	35	0x5804_0000	0x580F_FFFF	S	768 KB	Peripheral Region	Secure region for high latency peripherals that are expected to be not aliased
PERIPHERAL (Device)	36	0x5810_0000	0x5FFF_FFFF	S	127 MB	AHB Peripheral Expansion	Manager AHB Peripheral Integration Expansion Interface (HMSTEXPPIHL)
RAM WB(Normal)	37	0x6000_0000	0x6FFF_FFFF	NS	256 MB	Main Expansion Interfaces	Manager AXI Main Expansion Interface (XMSTEXPSRAM) - ATU
RAM WB(Normal)	38	0x7000_0000	0x7FFF_FFFF	S	256 MB	Main Expansion Interfaces	Manager AXI Main Expansion Interface (XMSTEXPSRAM) - ATU
RAM WT(Normal)	39	0x8000_0000	0x8FFF_FFFF	NS	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface (XMSTEXPSRAM) - ATU
RAM WT(Normal)	40	0x9000_0000	0x9FFF_FFFF	S	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface (XMSTEXPSRAM) - ATU
DEVICE (Outer Sharable)	41	0xA000_0000	0xAFFF_FFFF	NS	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface - (XMSTEXPDEV)
DEVICE (Outer Sharable)	42	0xB000_0000	0xBFFF_FFFF	S	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface (XMSTEXPDEV)
DEVICE (Outer Sharable)	43	0xC000_0000	0xCFFF_FFFF	NS	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface (XMSTEXPDEV) - ATU
DEVICE (Outer Sharable)	44	0xD000_0000	0xDFFF_FFFF	S	256 MB	Main Expansion Interfaces	Manager AXI Integration Expansion Interface (XMSTEXPDEV) - ATU
SYSTEM PPB (Strongly-ordered)	45	0xE000_0000	0xE00F_FFFF	Exempt	1 MB	Private Peripheral Bus Region	CPU Private Peripheral Bus Region. Local to Each CPU

Name (type)	Row ID	Start address	End address	Security	Size	Region name	Description
SYSTEM Vendor_SYS (Device)	46	0xE010_0000	0xE01F_FFFF	NS	1 MB	Debug System Access (Gated using DTACG)	DSROM. Debug System ROM
SYSTEM Vendor_SYS (Device)	47	0xE020_0000	0xEFFF_FFFF	NS	254 MB	AHB Peripheral Expansion	Manager AHB Peripheral Integration Expansion Interface (HMSTEXPPILL)
SYSTEM Vendor_SYS (Device)	48	0xF000_0000	0xF00F_FFFF	Exempt	1 MB	Reserved	Reserved (bus error). Only Visible via the Debug Access Interface and through the System Debug Access Region via APs
SYSTEM Vendor_SYS (Device)	49	0xF010_0000	0xF01F_FFFF	S	1 MB	Debug System Access (Gated using DTACG)	DSROM. Debug System ROM
SYSTEM Vendor_SYS (Device)	50	0xF020_0000	0xFFFF_FFFF	S	254 MB	AHB Peripheral Expansion	Manager AHB Peripheral Integration Expansion Interface (HMSTEXPPILL)

5.2 Interrupt maps

The *System Control Processor* (SCP) and *Application Processor* (AP) have their own interrupt maps.

5.2.1 AP interrupt map

Describes the interrupt map for the *Application Processor* (AP).

The *Generic Interrupt Controller* (GIC) Architecture defines two types of physical interrupts.

They are:

- *Private Peripheral Interrupts* (PPIs) that separately exist for every processor.
- *Shared Peripheral Interrupts* (SPIs) that are shared for all processors.

PPI and SPI interrupts have configurable options, including number of interrupts, Edge or Level triggered, and Polarity. For example, active-LOW, active-HIGH, or Rising edge.


Note

GIC PPI inputs are either active-LOW level sensitive, or triggered on a rising edge.

Table 5-5: AP interrupt map

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
0-15	SGI	-	-	Software Generated Interrupt
16	RESERVED	-	-	-
17	pmbirqn	Level	active-LOW	Statistical Profiling Extension interrupt (Only for CXC and "big" cores)
18	trbirqn	Level	active-LOW	Statistical Profiling Extension interrupt
19	cnthvsirqn	Level	active-LOW	Secure Virtual Timer event
20	cnthpsirqn	Level	active-LOW	Secure Physical Timer event
21	RESERVED	-	-	-
22	commirqn	Level	active-LOW	Debug Communications Channel receive or transmit request
23	pmuirqn	Level	active-LOW	PMU interrupt
24	ctiirqn	Rising Edge	-	CTI interrupt
25	vcpumntirqn	Level	active-LOW	Virtual Maintenance Interrupt
26	cnthpirqn	Level	active-LOW	Non-secure PL2 Timer event
27	cntvirqn	Level	active-LOW	Virtual Timer event
28	cnthvirqn	Level	active-LOW	EL2 virtual timer
29	cntpsirqn	Level	active-LOW	Secure PL1 Physical Timer event
30	cntpnsirqn	Level	active-LOW	Non-secure PL1 Physical Timer event
31	RESERVED	-	-	-
32	RESERVED	-	-	-
33	RESERVED	-	-	-
34	RESERVED	-	-	-
35	RESERVED	-	-	-
36	RESERVED	-	-	-
37	RESERVED	-	-	-
38	RESERVED	-	-	-
39	RESERVED	-	-	-
40	RESERVED	-	-	-
41	RESERVED	-	-	-
42	RESERVED	-	-	-
43-47	RESERVED	-	-	-

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
48	MCN0 - Combined S	Rising Edge	-	irpt_comb_s
49	MCN0 - Combined NS	Rising Edge	-	irpt_comb_ns
50	RESERVED	-	-	-
51	RESERVED	-	-	-
52	MCN1 - Combined S	Rising Edge	-	-
53	MCN1 - Combined NS	Rising Edge	-	-
54	RESERVED	-	-	-
55	RESERVED	-	-	-
56	MCN2 - Combined S	Rising Edge	-	-
57	MCN2 - Combined NS	Rising Edge	-	-
58	RESERVED	-	-	-
59	RESERVED	-	-	-
60	MCN3 - Combined S	Rising Edge	-	-
61	MCN3 - Combined NS	Rising Edge	-	-
62	RESERVED	-	-	-
63	RESERVED	-	-	-
64	MCN4 - Combined S	Rising Edge	-	-
65	MCN4 - Combined NS	Rising Edge	-	-
66	RESERVED	-	-	-
67	RESERVED	-	-	-
68	MCN5 - Combined S	Rising Edge	-	-
69	MCN5 - Combined NS	Rising Edge	-	-
70	RESERVED	-	-	-
71	RESERVED	-	-	-
72	MCN6 - Combined S	Rising Edge	-	-
73	MCN6 - Combined NS	Rising Edge	-	-
74	RESERVED	-	-	-
75	RESERVED	-	-	-
76	MCN7 - Combined S	Rising Edge	-	-

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
77	MCN7 - Combined NS	Rising Edge	-	-
78	RESERVED	-	-	-
79	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
80-81	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
82	ETRBUFINT	Level	active-HIGH	From ETR
83	STM-500 synchronisation	Edge	rising edge	-
84	System CTI trigger output	Edge	rising edge	driven from debug subsystem CTM
85	System CTI trigger output	Edge	rising edge	driven from debug subsystem CTM
86	Secure Watchdog (WS0)	Level	active-HIGH	Bit 0: First Secure WD Expiry
87	Secure Watchdog (WS1)	Level	active-HIGH	Bit 1: Second Secure WD Expiry
90:88	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
91	AP_GTCLK Generic timer (secure)	Level	active-HIGH	-
92	AP_GTCLK Generic timer (non-secure)	Level	active-HIGH	-
93	Non-Secure Watchdog WS0	Level	active-HIGH	Bit 0: First Non-secure WD Expiry
94	Non-Secure Watchdog WS1	Level	active-HIGH	Bit 1: Second Non-secure WD Expiry
95	AP_NS_UART_INT	Level	active-HIGH	-
96	AP_S_UART_INT	Level	active-HIGH	-
97	GPU interrupt	Level	active-HIGH	-
98	GPU Job interrupt	Level	active-HIGH	-
99	GPU MMU interrupt	Level	active-HIGH	-
100	GPU event request	Level	active-HIGH	-
101	DMC0_link_err_int (expansion)	-	-	DMC: Link Error Interrupt: link_err_interrupt
102	DMC0_combined_ras_int (expansion	-	-	DMC: Combined RAS Interrupt: s0_failed_access / ce_ram_interrupt / ue_ram_interrupt / cfg_failed_access_interrupt
103	DMC0_combined_pmu_int (expansion)	-	-	DMC: Combined PMU Interrupt: s0_pmu_interrupt / m_pmu_interrupt
104	DMC0_combined_misc_int (expansion)	-	-	DMC: Combined Misc Interrupt: cfg_interrupt / m_phy_interrupt

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
105	DMC1_combined_ras_int (expansion)	-	-	-
106	DMC1_link_err_int (expansion)	-	-	-
107	DMC1_combined_pmu_int (expansion)	-	-	-
108	DMC1_combined_misc_int (expansion)	-	-	-
109	DMC2_combined_ras_int (expansion)	-	-	-
110	DMC2_link_err_int (expansion)	-	-	-
111	DMC2_combined_pmu_int (expansion)	-	-	-
112	DMC2_combined_misc_int (expansion)	-	-	-
113	DMC3_combined_ras_int (expansion)	-	-	-
114	DMC3_link_err_int (expansion)	-	-	-
115	DMC3_combined_pmu_int (expansion)	-	-	-
116	DMC3_combined_misc_int (expansion)	-	-	-
117-127	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
128-255	Expansion interrupts	-	-	to be treated like RESERVED interrupts and tied LOW
256	TCU PMU IRPT	Edge	rising edge	For information about TCU and TBU interrupts, see *Arm® CoreLink™ MMU-700 System Memory Management Unit Technical Reference Manual*
257	TCU Event Queue Secure IRPT	Edge	rising edge	-
258	TCU CMD SYNC Secure	Edge	rising edge	-
259	TCU Global Secure	Edge	rising edge	-
260	TCU Event Queue Non-secure	Edge	rising edge	-
261	TCU CMD SYNC Non-secure	Edge	rising edge	-
262	TCU Global Non-secure	Edge	rising edge	-
263	CS TBU PMU interrupt	Edge	rising edge	-
264	GPU0 TBU PMU interrupt	Edge	rising edge	-
265	GPU1 TBU PMU interrupt	Edge	rising edge	-

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
266	GPU2 TBU PMU interrupt	Edge	rising edge	-
267	GPU3 TBU PMU interrupt	Edge	rising edge	-
268-271	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
272	RESERVED	-	-	-
273	RESERVED	-	-	-
274-319	RESERVED	-	-	Treated as active-HIGH level interrupt, tied LOW
320	AP_SCP_MHU_0_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
321	AP_SCP_MHU_1_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
322	AP_SCP_MHU_2_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
323	AP_SCP_MHU_3_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
324	AP_SCP_MHU_4_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
325	AP_SCP_MHU_5_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
326	AP_SCP_MHU_6_s_Int	Level	active-HIGH	AP-to-SCP - AP is sender
327	RESERVED	-	-	-
328	SCP_AP_MHU_0_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
329	SCP_AP_MHU_1_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
330	SCP_AP_MHU_2_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
331	SCP_AP_MHU_3_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
332	SCP_AP_MHU_4_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
333	SCP_AP_MHU_5_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
334	SCP_AP_MHU_6_r_Int	Level	active-HIGH	SCP-to-AP - AP is receiver
335	RESERVED	-	-	-
336	AP_RSE_MHU_0_s_Int	Level	active-HIGH	AP-to-RSE - AP is sender
337	AP_RSE_MHU_1_s_Int	Level	active-HIGH	AP-to-RSE - AP is sender
338-343	RESERVED	-	-	-
344	RSE_AP_MHU_0_r_Int	Level	active-HIGH	RSE-to-AP - AP is receiver

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
345	RSE_AP_MHU_1_r_Int	Level	active-HIGH	RSE-to-AP - AP is receiver
346-351	RESERVED	-	-	-
352-475	RESERVED	Level	active-HIGH	-
476	Data NCI PMU sysclk	Level	active-LOW	For information about NCI interrupts, see *Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual*
477	Data NCI PMU periphclk	Level	active-LOW	-
478	Data NCI PMU gpu_coregroupclk	Level	active-LOW	-
479	Data NCI PMU smsclk	Level	active-LOW	-
480	Data NCI PMU ros_nciclk	Level	active-LOW	-
481	Peripheral NCI PMU sysclk	Level	active-LOW	-
482	Peripheral NCI PMU periphclk	Level	active-LOW	-
483	Peripheral NCI PMU gpuclk	Level	active-LOW	-
484	Peripheral NCI PMU dsu_ppuclk	Level	active-LOW	-
485	Peripheral NCI PMU smsclk	Level	active-LOW	-
486-491	Reserved	-	-	-
492	Data PD_SYSTOP_s	Level	active-HIGH	-
493	Data PD_SYSTOP_ns	Level	active-HIGH	-
494	Data PD_GPUGLBL_s	Level	active-HIGH	-
495	Data PD_GPUGLBL_ns	Level	active-HIGH	-
496	Peripheral PD_SYSTOP_s	Level	active-HIGH	-
497	Peripheral PD_SYSTOP_ns	Level	active-HIGH	-
498	Peripheral PD_GPUGLBL_s	Level	active-HIGH	-
499	Peripheral PD_GPUGLBL_ns	Level	active-HIGH	-
500	Peripheral PD_DSUTOP_s	Level	active-HIGH	-
501	Peripheral PD_DSUTOP_ns	Level	active-HIGH	-

Interrupt ID	Interrupt source	Trigger	Polarity	Additional information
502-507	RESERVED	-	-	-
508	RESERVED	-	-	-
509	RESERVED	-	-	-
510	RESERVED	-	-	-
511	RESERVED	-	-	-
512-767	RESERVED	-	-	-

5.2.2 SCP interrupt map

Describes the interrupt map for the *System Control Processor* (SCP).

The SCP receives interrupts from the following sources:

- Application processor system wakeup interrupts
- CoreSight power and reset request interrupts
- Internal SCP subsystem interrupts
- Expansion SCP interrupts

These interrupts are routed to the *Nested Vector Interrupt Controller* (NVIC) that is included in the Cortex-M85 processor, where they can be managed by software. The *Non-Maskable Interrupt* (NMI) and interrupt IDs 0-31 are wakeup sources.

The following table summarizes the regions of the SCP interrupt map.

Table 5-6: SCP interrupt map

Interrupt number	EWIC wake support	Source	Trigger	Polarity
NMI	Y	Combined Secure Watchdog, SLOWCLK Watchdog and CPU<n>EXPNMI. The Expansion NMI (CPU<n>EXPNMI) has been tied off and is not in use.	Level	Active-High
0	Y	Non-secure Watchdog Reset Request	Level	Active-High
1	Y	Non-Secure Watchdog Interrupt	Level	Active-High
2	Y	SLOWCLK Timer	Level	Active-High
3	Y	Timer 0	Level	Active-High
4	Y	Timer 1	Level	Active-High
5	Y	Timer 2	Level	Active-High
6	Y	Reserved	Level	Active-High(tie off 0b0)
7	Y	Reserved	Level	Active-High(tie off 0b0)

Interrupt number	EWIC wake support	Source	Trigger	Polarity
8	Y	Reserved	Level	Active-High(tie off 0b0)
9	Y	MPC Combined (Secure)	Level	Active-High
10	Y	PPC Combined (Secure)	Level	Active-High
11	Y	MSC Combined (Secure)	Level	Active-High
12	Y	Bridge Error Combined Interrupt (Secure)	Level	Active-High
13	N	Reserved	Level	Active-High(tie off 0b0)
14	Y	PPU_Combined	Level	Active-High
15	Y	Reserved	Level	Active-High
16	Y	Reserved	Level	Active-High(tie off 0b0)
17	Y	Reserved	Level	Active-High(tie off 0b0)
18	Y	Reserved	Level	Active-High(tie off 0b0)
19	Y	Reserved	Level	Active-High(tie off 0b0)
20	N	Reserved	Level	Active-High(tie off 0b0)
21	N	Reserved	Level	Active-High(tie off 0b0)
22	N	Reserved	Level	Active-High(tie off 0b0)
23	N	Reserved	Level	Active-High(tie off 0b0)
24	Y	Reserved	Level	Active-High(tie off 0b0)
25	Y	Reserved	Level	Active-High(tie off 0b0)
26	N	Reserved	Level	Active-High(tie off 0b0)
27	Y	Timer 3 AON	Level	Active-High
28	N	CPU0CTIIRQ0 (local CPU CTI only)	Level	Active-High

Interrupt number	EWIC wake support	Source	Trigger	Polarity
29	N	CPU0CTIIRQ1 (local CPU CTI only)	Level	Active-High
30	N	Reserved	Level	Active-High(tie off 0b0)
31	N	Reserved	Level	Active-High(tie off 0b0)
32	N	Reserved	Level	Active-High(tie off 0b0)
33	N	Reserved	Level	Active-High(tie off 0b0)
34	N	Reserved	Level	Active-High(tie off 0b0)
35	Y	Reserved	Level	Active-High
36	Y	Reserved	Level	Active-High
37-67	N	Reserved	Level	Active-High(tie off 0b0)
67-87	N	Reserved	Level	Active-High(tie off 0b0)
88	Y	SCP_AP_MHU_0_s_Int	Level	Active-High
89	Y	AP_SCP_MHU_0_r_Int	Level	Active-High
90	Y	SCP_AP_MHU_1_s_Int	Level	Active-High
91	Y	AP_SCP_MHU_1_r_Int	Level	Active-High
92	Y	SCP_AP_MHU_2_s_Int	Level	Active-High
93	Y	AP_SCP_MHU_2_r_Int	Level	Active-High
94	Y	SCP_AP_MHU_3_s_Int	Level	Active-High
95	Y	AP_SCP_MHU_3_r_Int	Level	Active-High
96	Y	SCP_AP_MHU_4_s_Int	Level	Active-High
97	Y	AP_SCP_MHU_4_r_Int	Level	Active-High
98	Y	SCP_AP_MHU_5_s_Int	Level	Active-High
99	Y	AP_SCP_MHU_5_r_Int	Level	Active-High
100	Y	SCP_AP_MHU_6_s_Int	Level	Active-High
101	Y	AP_SCP_MHU_6_r_Int	Level	Active-High
102	Y	SCP1_SCP0_MHU_0_r_int	Level	Active-High
103	N	Reserved	Level	Active-High(tie off 0b0)

Interrupt number	EWIC wake support	Source	Trigger	Polarity
104	N	Reserved	Level	Active-High(tie off 0b0)
105	N	Reserved	Level	Active-High(tie off 0b0)
106	N	Reserved	Level	Active-High(tie off 0b0)
107	N	Reserved	Level	Active-High(tie off 0b0)
108	N	Reserved	Level	Active-High(tie off 0b0)
109	N	Reserved	Level	Active-High(tie off 0b0)
110-115	N	Reserved	Level	Active-High(tie off 0b0)
116	Y	ATU INT	Level	Active-High
117-120	N	Reserved	Level	Active-High(tie off 0b0)

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Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

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Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in Arm documents.

Product status

All products and services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

Product completeness status

The information in this document is Final, that is for a developed product.

Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
0000-01	6 September 2024	Non-Confidential	First release

Change history

The revisions tables describe the technical changes between released issues of this document.

Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

Typographic conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
italic	Citations.
bold	Interface elements, such as menu names. Terms in descriptive lists, where appropriate.
`monospace`	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace underline`	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`<and>`	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Terms that have specific technical meanings as defined in the *Arm® Glossary*. For example, **IMPLEMENTATION DEFINED**, **IMPLEMENTATION SPECIFIC**, **UNKNOWN**, and **UNPREDICTABLE**.

We recommend the following. If you do not follow these recommendations your system might not work.

Your system requires the following. If you do not follow these requirements your system will not work.

You are at risk of causing permanent damage to your system or your equipment, or harming yourself.

This information is important and needs your attention.

A useful tip that might make it easier, better or faster to perform a task.

A reminder of something important that relates to the information you are reading.

Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Access to Arm documents depends on their confidentiality:

- Non-Confidential documents are available at developer.arm.com/documentation. Each document link in the following tables goes to the online version of the document.
- Confidential documents are available to licensees only through the product package.

Arm product resources	Document ID	Confidentiality
Arm® CoreLink™ GIC-700 Generic Interrupt Controller Technical Reference Manual	101516	Non-Confidential
Arm® CoreLink™ MMU-700 System Memory Management Unit Technical Reference Manual	101542	Non-Confidential
Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual	DDI 0475	Non-Confidential
Arm® CoreLink™ NIC-450 Network Interconnect Technical Overview	100459	Non-Confidential
Arm® CoreLink™ PCK-600 Power Control Kit Technical Reference Manual	101150	Non-Confidential
Arm® CoreLink™ TZC-400 TrustZone® Address Space Controller Technical Reference Manual	100325	Non-Confidential
Arm® CoreSight™ Components Technical Reference Manual	DDI 0314	Non-Confidential
Arm® CoreSight™ STM-500 System Trace Macrocell Technical Reference Manual	DDI 0528	Non-Confidential
Arm® CoreSight™ System-on-Chip SoC-600 Technical Reference Manual	100806	Non-Confidential
Arm® CoreSight™ Trace Memory Controller Technical Reference Manual	DDI 0461	Non-Confidential
Arm® Cortex®-A520 Core Cryptographic Extension Technical Reference Manual	102519	Non-Confidential
Arm® Cortex®-A520 Core Technical Reference Manual	102517	Non-Confidential
Arm® Cortex®-A725 Core Cryptographic Extension Technical Reference Manual	107654	Non-Confidential
Arm® Cortex®-A725 Core Technical Reference Manual	107652	Non-Confidential
Arm® Cortex®-M System Design Kit Technical Reference Manual	DDI 0479	Non-Confidential
Arm® Cortex®-M85 Processor Technical Reference Manual	101924	Non-Confidential
Arm® Cortex®-X925 Core Cryptographic Extension Technical Reference Manual	102809	Non-Confidential
Arm® Cortex®-X925 Core Technical Reference Manual	102807	Non-Confidential
Arm® DynamIQ™ Shared Unit-120 Technical Reference Manual	102547	Non-Confidential
Fast Models Fixed Virtual Platforms (FVP) Reference Guide	100966	Non-Confidential
Fast Models Reference Guide	100964	Non-Confidential
PrimeCell UART (PL011) Technical Reference Manual	DDI 0183	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
AMBA® 5 CHI Architecture Specification	IHI 0050E.a	Non-Confidential
AMBA® AXI and ACE Protocol Specification	IHI 0022	Non-Confidential
AMBA® CXS Protocol Specification	IHI 0079B	Non-Confidential
AMBA® Low Power Interface Specification	IHI 0068	Non-Confidential
Arm Base System Architecture 1.0C	DEN 0094	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
Arm® Architecture Reference Manual for A-profile architecture	DDI 0487	Non-Confidential
Arm® Base System Architecture 1.0 Platform Design Document	DEN 0094	Non-Confidential
Arm® CoreSight™ Architecture Specification v3.0	IHI 0029	Non-Confidential
Arm® CoreSight™ Base System Architecture 1.0, Arm Platform Design Document	DEN 0068.v	Non-Confidential
Arm® Debug Interface Architecture Specification ADIv5.0 to ADIv5.2	IHI 0031	Non-Confidential
Arm® Debug Interface Architecture Specification ADIv6.0	IHI 0074	Non-Confidential
Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3 and version 4	IHI 0069	Non-Confidential
Arm® Platform Security Requirements, version 1.0	DEN 0106	Non-Confidential
Arm® Power Control System Architecture, version 2.1	DEN 0050	Non-Confidential
Arm® Power Policy Unit Architecture Specification, version 1.1	DEN 0051E	Non-Confidential
Arm® System Control and Management Interface Platform Design Document	DEN 0056	Non-Confidential
Arm® System Memory Management Unit Architecture Specification, SMMU architecture version 3.2	IHI 0070C.a	Non-Confidential
Arm®v8-M Architecture Reference Manual	DDI0553B.y	Non-Confidential

Non-Arm resources	Document ID	Organization
Ray Tracing in Vulkan®	–	Khronos® Group