

# ARM<sup>®</sup> Design Simulation Model

for SystemC

**User Guide**



# ARM Design Simulation Model User Guide

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## Release Information

The following changes have been made to this book.

Change history			
Date	Issue	Confidentiality	Change
September 2016	A	Non-Confidential	First release for SystemC.

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### Revisions

# Preface

This preface introduces the *ARM® Design Simulation Model (DSM) User Guide*. It contains the following sections:

- *About this book on page viii.*
- *Feedback on page x.*

## About this book

This book is for the *ARM Design Simulation Model* (DSM) for SystemC.

## Intended audience

This book is written for experienced hardware engineers, software engineers and System-on-Chip (SoC) designers who might have experience of ARM products. You are expected to have experience of SystemC.

## Using this book

This book is organized into the following chapters:

### Chapter 1 *Introduction*

Read this for a high-level description of DSMs and how they are used in simulations. This chapter describes the contents of the package and potential simulation inaccuracies when using DSMs.

### Chapter 2 *Initial DSM Configuration*

Read this for a description of how to install, set up, and test a DSM.

### Chapter 3 *Model Limitations*

This chapter describes some of the limitations of DSMs.

### Appendix A *Revisions*

Read this for a description of the technical changes between released issues of this book.

## Glossary

The *ARM® Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM® Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

The *ARM® Glossary* is available on the ARM Infocenter at <http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html>.

## Conventions

Conventions that this book can use are described in:

- *Typographical conventions.*

### Typographical conventions

The following table describes the typographical conventions:

Style	Purpose
<i>italic</i>	Introduces special terminology, denotes cross-references, and citations.
<b>bold</b>	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
monospace	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.



(continued)

Style	Purpose
<u>monospace</u>	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
monospace <i>italic</i>	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
<b>monospace bold</b>	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the <i>ARM® glossary</i> . For example, IMPLEMENTATION DEFINED, UNKNOWN, and UNPREDICTABLE.

### Additional reading

This section lists publications by ARM and by third parties.

See Infocenter <http://infocenter.arm.com> for access to ARM documentation.

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- The title.
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# Chapter 1

## Introduction

This chapter introduces the *ARM Design Simulation Model* (DSM) for SystemC. It contains the following sections:

- *About Design Simulation Models on page 1-2.*
- *DSM package contents on page 1-3.*
- *Simulation with DSMs on page 1-4.*

## 1.1 About Design Simulation Models

DSMs are cycle accurate, simulation models that you can include in a range of target HDL simulators. Each DSM is specific to a host platform. The DSM fully matches the architecture and functionality of the RTL model.

The DSMs are derived directly from the RTL model. DSMs can function with a wide range of industry-standard Verilog simulators. Performance depends on:

- The simulator interface efficiency.
- The complexity of the design in which it is instantiated.
- The complexity of the original design.

The DSM consists of:

- A functional core block.
- A SystemC wrapper.

The wrapper uses the foreign language interface of the host simulator to instantiate the functional model. The DSM is generally derived from the RTL source of the ARM design using the *ARM Cycle Model* compiler. For some ARM products, this might be augmented with extra functionality, such as TARMAC trace, added by ARM.

The DSM interfaces to the wrapper using technology developed by ARM to enable a single compiled model to function with a variety of logic simulators. For some products, the DSMs might include behavioral debug facilities, such as TARMAC trace. When you use compiled models, it enables distribution of models without compromising the intellectual property that they embody.

———— **Note** —————

The DSM is intended for functional simulation and verification only, not for timing or final design signoff.

### 1.1.1 Features of ARM DSMs

Table 1-1 shows the main features of ARM DSMs.

**Table 1-1 ARM DSM features**

Feature	Description
Full device functionality	Unless otherwise noted, the DSM fully matches the architecture and functionality of the RTL model.
Phase accuracy	You can expect the DSM to exhibit the same intra-cycle timing as the RTL model.
Register visibility	For register visibility, use the TARMAC trace or see the included README for a list of registers that support visibility. Refer to the <i>ARM TARMAC Specification</i> available with your DSM installation.
Cache and memory size configuration	You can configure the size of the cache, or TCM, for each particular DSM instance, where applicable.  ———— <b>Note</b> ————— This feature does not apply if your ARM product has no such configuration, or where your DSM generation flow does not support multiple configurations.
Disassembler	To view disassembled code, use the TARMAC trace.

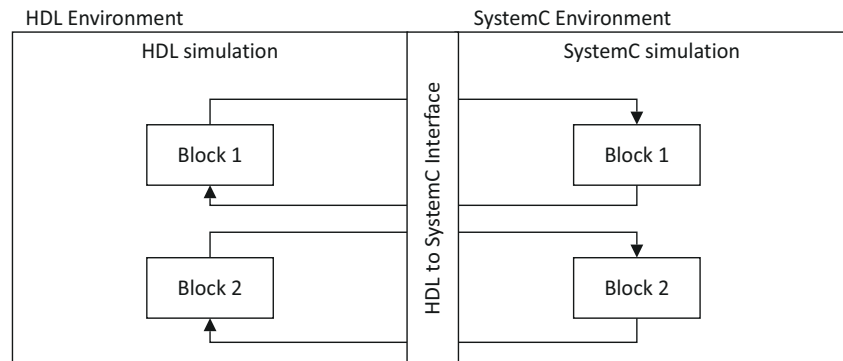
## 1.2 DSM package contents

Each DSM contains the following components:

- DSM SystemC wrapper.
- DSM library, including a dynamic .so file, static .a file, and header files.
- One or more implementation libraries as .so files.
- A testbench file to check the DSM setup.
- Documentation, including the *ARM TARMAC Specification*, this document, and a README.

### 1.3 Simulation with DSMs

Figure 1-1 shows the integration of DSMs (Block 1 and Block 2) into an HDL simulation. During simulation, the DSM interfaces to the simulator through the HDL to the SystemC Interface, which synchronizes between the two environments.



**Figure 1-1 DSM integration**

———— **Note** ————

For synthesizable cores, the DSM is a pre-implementation, pre-synthesis model. It does not contain any scan test insertion or BIST and is not a *Sign-Off Model* (SOM).

# Chapter 2

## Initial DSM Configuration

This chapter describes the functionality of the *ARM Design Simulation Model for SystemC* (DSM).

It contains the following sections:

- *Prerequisites on page 2-2*
- *Extracting and Installing the DSM on page 2-3.*
- *How to test the DSM on page 2-4.*
- *Integrating with Simulators on page 2-5.*
- *TARMAC Trace on page 2-8*

## 2.1 Prerequisites

This section describes prerequisites to using the DSM.

- DSM built and downloaded in .tgz format from ARM IP Exchange ([www.armipexchange.com](http://www.armipexchange.com)).
- GCC Compiler. If you are using Synopsys VCS, refer to the Synopsys documentation for the required gcc versions.
- Refer to the README file in your installation directory for specific tool versions required, model-specific limitations or restrictions, and supported registers.



## 2.2 Extracting and Installing the DSM

Before proceeding, ensure you have built and downloaded the `<dsm package>.tgz` for the desired IP from ARM IP Exchange ([www.armipexchange.com](http://www.armipexchange.com)).

### 2.2.1 Installing Using the Command Line

To install using the command line, follow the instructions below:

1. `cd` to the directory where you wish to install the DSM.
2. Extract the files from the `<dsm package>.tgz` as follows:

```
% tar -xvzf <dsm package>.tgz
gcc/EULA.pdf
gcc/docs
gcc/dsm
gcc/testbench
...
```

The directory now contains the DSM release.

## 2.3 How to test the DSM

---

### Note

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You must set the `DSM_MODEL_PATH` environment variable to point to the directory that contains the DSM implementation libraries. If you do not set the variable, the `[DSM MODULE NAME]_TESTBENCH.sh` script assume the `DSM_MODEL_PATH` is one directory above the scripts location in the `dsm` directory. If the path is not set correctly, the simulator compiler exits with an error looking for the `[DSM MODULE NAME]` files or library files.

---

For all simulators, the module search path must include the path to the DSM libraries. Reference the `[DSM MODULE NAME]_TESTBENCH.sh` for a detailed example. In the following sections, variables are defined as follows:

- `[DSM_PATH]` is the path the DSM release `dsm` directory (i.e., `$DSM_RELEASE_DIR/dsm`).
- `[DSM MODULE NAME]` is the Component name specified on the portal.
- `[PRODUCT NAME]` is the ARM IP name.

Execute the `[DSM MODULE NAME]_TESTBENCH.sh` executable within the expanded package to check that operation is valid. The DSM is contained within a testbench that is supplied with the package. The script requires that you select a system-installed simulator. You can specify the simulator to use by setting one of the following parameters:

- |                  |   |
|------------------|---|
| <code>ves</code> | Selects the VCS simulator.              |
| <code>ius</code> | Selects the Cadence Incisive simulator. |
| <code>mti</code> | Selects the QuestaSim simulator.        |

---

### Note

---

The DSM is not intended for use with Accellera (OSCI) simulations.

---

A test that executes correctly prints the following message at the end of the simulation:

```
DSM: *** TEST PASSED ***
```

## 2.4 Integrating with Simulators

To use the DSM Model, add the following environment variables to your environment:

bash commands:

- export PATH=[DSM\_PATH]/univentUtil/bin:\$PATH
- export LD\_LIBRARY\_PATH=[DSM\_PATH]/univentUtil/lib:[DSM\_PATH]:\$LD\_LIBRARY\_PATH

C shell commands:

- setenv PATH [DSM\_PATH]/univentUtil/bin:\$PATH
- setenv LD\_LIBRARY\_PATH [DSM\_PATH]/univentUtil/lib:[DSM\_PATH]:\$LD\_LIBRARY\_PATH

### 2.4.1 VCS

To integrate the DSM with VCS:

1. Create the Verilog wrapper:

```
syscan -full64 -sysc=230 -cflags "-DCM_SYSC_IO_UNIVENT_TARMAC -DCM_SYSC_REMOVE_SCOPE"
[DSM_PATH]/[DSM MODULE NAME].cpp:[DSM MODULE NAME]
```

2. Add the following to the VCS command line:

```
-full64 -sysc=230 -sysc=adjust_timeres -LDFLAGS "-L[DSM_PATH]" [DSM_PATH]/univentUtil/lib/[PRODUCT
NAME]_tarmac_dpi.so [DSM_PATH]/libcarbon5.so [DSM_PATH]/lib[DSM MODULE NAME].a
[DSM_PATH]/univent_tarmac.cpp
```

### 2.4.2 Cadence Incisive

To integrate the DSM with Cadence Incisive, add the following to the irun command line:

```
-64bit [DSM_PATH]/univentUtil/lib/[PRODUCT NAME]_tarmac_dpi.so -sysc -scautoshell verilog
-DCM_SYSC_IO_UNIVENT_TARMAC -DCM_SYSC_REMOVE_SCOPE -I[DSM_PATH] -L[DSM_PATH]
[DSM_PATH]/[DSM MODULE NAME].cpp [DSM_PATH]/univent_tarmac.cpp -L[DSM_PATH] -lcarbon5 [DSM_PATH]/lib[DSM
MODULE NAME].a
```

### 2.4.3 Mentor QuestaSim (ModelSim)

To integrate the DSM with Mentor QuestaSim:

Before running vsim, compile and link the libraries as follows:

```
sccom -64 -g -suppress 6102 -DCM_SYSC_IO_UNIVENT_TARMAC -DCM_SYSC_REMOVE_SCOPE -I[DSM_PATH]
[DSM_PATH]/[DSM MODULE NAME].cpp [DSM_PATH]/univent_tarmac.cpp
sccom -64 -link -suppress 6102 -L[DSM_PATH] -I[DSM MODULE NAME] -lcarbon5 [DSM_PATH]/univentUtil/lib/[DSM
MODULE NAME]_tarmac_dpi.so
```

## 2.5 TARMAC Trace

This section describes enabling and disabling TARMAC trace.

### 2.5.1 Enabling TARMAC Trace

To enable the TARMAC trace, refer to the TARMAC specifications in the docs directory of the DSM release, or review the `[DSM MODULE NAME]_TESTBENCH.sh` file for the `*TARMAC*` environment variables.

You must also compile with the define `CM_SYS_IO_UNIVENT` (for example, `-DCM_SYS_IO_UNIVENT`) to enable.

### 2.5.2 Disabling TARMAC Trace

To disable the TARMAC trace, remove the `CM_SYS_IO_UNIVENT` define from the compile. Or, set the environment variable `*_TARMAC_ENABLE` to `never`.

# Chapter 3

## Model Limitations

This chapter contains the following sections:

- *Limitations of use on page 3-2.*

## 3.1 Limitations of use

Although DSMs match the architecture and functionality of the appropriate core designs, they are subject to the limitations that the following sections describe:

- *Supported simulators*
- *Unsupported simulator functions.*
- *Internal scan chain modeling.*
- *Caches and registers.*

### 3.1.1 Supported simulators

The DSM model is limited to Linux 64-bit. It has been tested and is supported on the following simulators:

- Synopsys VCS
- Cadence Incisive
- Mentor QuestaSim

### 3.1.2 Unsupported simulator functions

The following simulator functions are not supported:

#### **Save and Restore, also known as checkpointing**

Save the simulation at a determined point of time, also known as a snapshot, and restore the simulation to that point of time.

#### **Power-aware simulation**

Power-aware simulation.

### 3.1.3 Internal scan chain modeling

DSMs are derived from the RTL description of the core that they model. The final netlist for the core might contain internal scan chains that were added during synthesis. It is not possible to use DSMs to model these scan chains because they do not exist in the device RTL. However, the *Sign-Off Model (SOM)* of a device models the scan chains.

### 3.1.4 Caches and registers

The DSM Model provides visibility into certain registers. Refer to the README file included with your DSM Model for a list of supported registers.

### 3.1.5 Waveform dumping

Refer to the README file included with your DSM Model for instructions and limitations of Waveform dumping for your particular model.

# Appendix A

## Revisions

This appendix describes the technical changes between released issues of this book.

**Table A-1 Issue A**

<b>Change</b>	<b>Location</b>	<b>Affects</b>
First release for SystemC models	-	-

