Arm® CoreLink™ CI-700 Coherent Interconnect

Revision: r3p0

Technical Reference Manual

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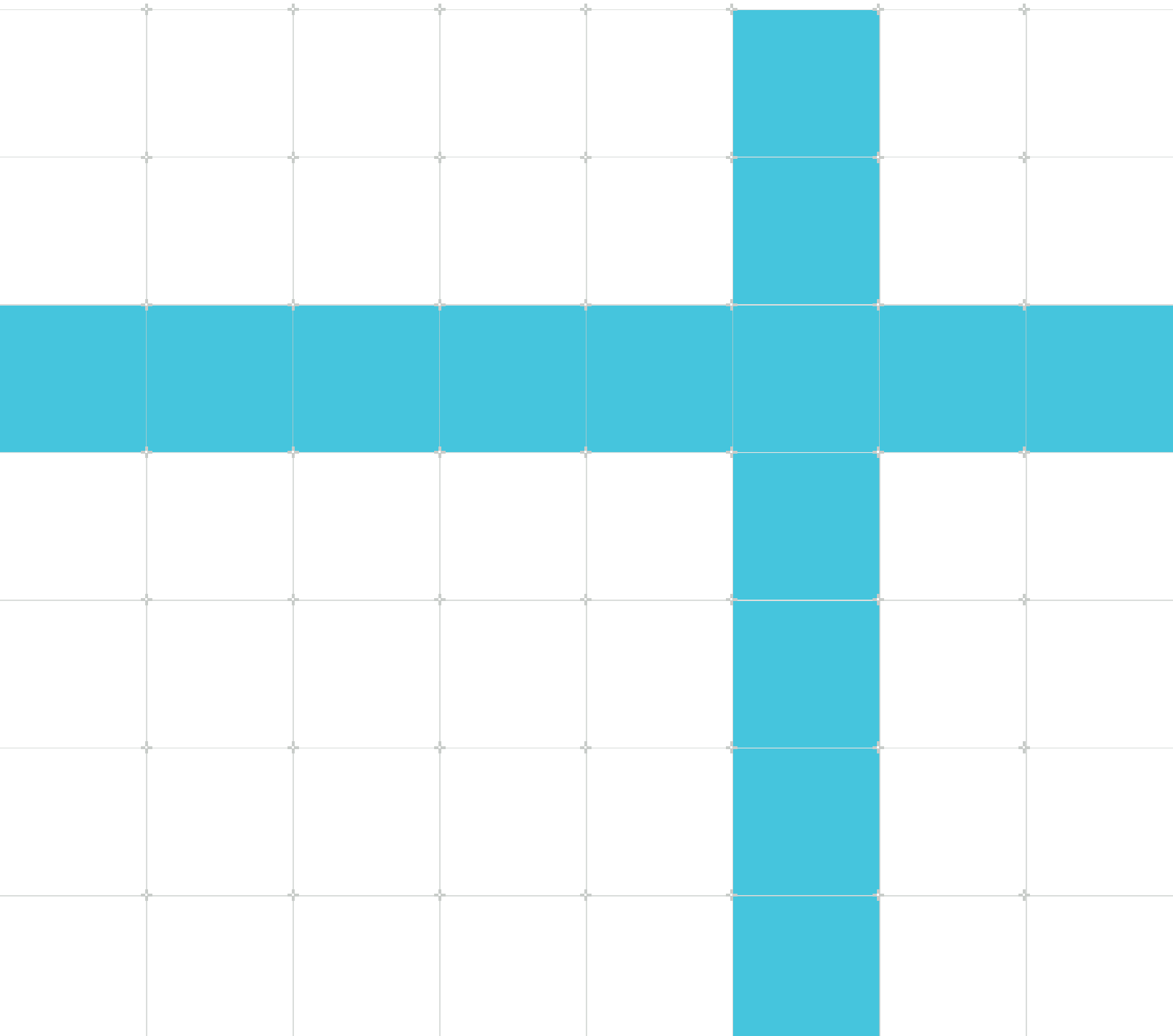
Issue 06
101569_0300_06_en



Arm® CoreLink™ CI-700 Coherent Interconnect

Technical Reference Manual

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Release Information

Document history

Issue	Date	Confidentiality	Change
0000-01	25 February 2020	Confidential	First development release for r0p0
0000-02	11 March 2020	Confidential	First Limited Access release for r0p0
0100-03	12 August 2020	Confidential	First Early Access release for r1p0
0100-04	21 May 2021	Non-Confidential	Second Early Access release for r1p0
0200-05	20 July 2021	Non-Confidential	First Early Access release for r2p0
0300-06	12 April 2022	Non-Confidential	First Early Access release for r3p0

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1 Introduction

1.1 Product revision status

The r*x*p*y* identifier indicates the revision status of the product described in this manual, for example, r1p2, where:

r*x* Identifies the major revision of the product, for example, r1.

p*y* Identifies the minor revision or modification status of the product, for example, p2.

1.2 Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a *System on Chip* (SoC) that uses the Arm® CI-700 Coherent Interconnect.

1.3 Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

Typographic conventions

Convention	Use
italic	Citations.
bold	Interface elements, such as menu names. Signal names. Terms in descriptive lists, where appropriate.
`monospace`	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace bold`	Language keywords when used outside example code.

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Convention	Use
`monospace underline`	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`<and>`	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Terms that have specific technical meanings as defined in the *Arm® Glossary*. For example, **IMPLEMENTATION DEFINED**, **IMPLEMENTATION SPECIFIC**, **UNKNOWN**, and **UNPREDICTABLE**.
Caution	Recommendations. Not following these recommendations might lead to system failure or damage.
Warning	Requirements for the system. Not following these requirements might result in system failure or damage.
Danger	Requirements for the system. Not following these requirements will result in system failure or damage.
Note	An important piece of information that needs your attention.
Tip	A useful tip that might make it easier, better or faster to perform a task.
Remember	A reminder of something important that relates to the information you are reading.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

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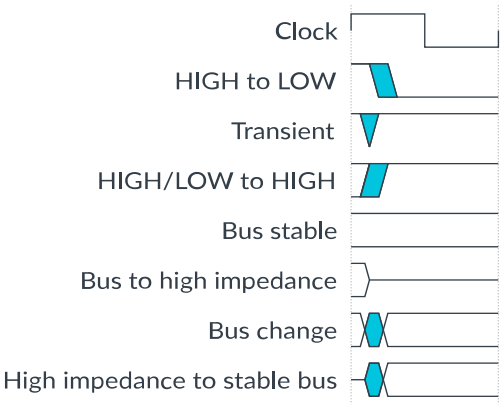
Figure 1-1: Key to timing diagram conventions



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

1.4 Additional reading

This document contains information that is specific to this product. See the following documents for other relevant information:

Table 1-2: Arm Publications

Document name	Document ID	Licensee only
AMBA® AXI and ACE Protocol Specification	IHI 0022H	No
AMBA® Low Power Interface Specification Arm® Q-Channel and P-Channel Interfaces	IHI 0068C	No
AMBA® 4 AXI4-Stream Protocol Specification	IHI 0051A	No
AMBA® 5 CHI Architecture Specification	IHI 0050E	No
Arm® CoreSight™ Architecture Specification	IHI 0029E	No
Arm® Architecture Reference Manual Armv7-A and Armv7-R edition	DDI 0406	No
Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile	DDI 0487	No
Arm® Architecture Reference Manual Supplement Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A	DDI 0598	No

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Document name	Document ID	Licensee only
Arm® Reliability, Availability, and Serviceability (RAS) Specification Armv8, for the Armv8-A architecture profile	DDI 0587	No
Principles of Arm® Memory Maps White Paper	DEN 0001	No
Arm® CoreLink™ CI-700 Coherent Interconnect Release Note	PJDOC-1779577084-29448	Yes
Arm® CoreLink™ CI-700 Coherent Interconnect Configuration and Integration Manual	101570	Yes
Arm® Socrates™ for CoreLink™ CI-700 Coherent Interconnect User Guide	101572	Yes
Arm® Neoverse™ N1 hyperscale reference design GIC-600 Integration using CMN-600 AXI4-Stream Interfaces White Paper	PJDOC-1779577084-5931	Yes

Table 1-3: Other Publications

Document ID	Document name
JEP106	*JEDEC Standard Manufacturers Identification Code*



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2 What is CI-700?

This chapter introduces CI-700 which is an AMBA® 5 CHI interconnect with a customizable mesh topology.

2.1 About CI-700

The CI-700 product is a scalable configurable coherent interconnect that is designed to meet the *Power, Performance, and Area* (PPA) requirements for Coherent Interconnect systems that are used in client applications.

CI-700 is a scalable mesh interconnect that supports 1-8 processor compute clusters.

You can configure CI-700 using the Arm® Socrates™ system IP Tooling platform. Socrates™ is an environment for the configuration of Arm IP. Using Socrates™, you can configure the following CI-700 characteristics:

- Custom interconnect size and device placement
- Optional *System Level Cache* (SLC). For more information about the features of the SLC memory system, see 6.1 About the SLC memory system on page 1296.

For information about using Socrates™, see the *Arm® Socrates™ for CoreLink™ CI-700 Coherent Interconnect User Guide*, which is bundled with the tool.

CI-700 supports AMBA® 5 CHI Issue E, including the following features:

- MakeReadUnique, writes with optional data, and write zero with no data transactions
- Enhanced exclusive transactions
- Various transaction optimizations and enhancements
- Connection of devices with multiple interfaces
- Extended TxnID and GroupID
- DVM updates
- Memory tagging

CI-700 provides system-level alignment by providing the following system functionality:

- *Quality of Service* (QoS)
- *Reliability, Availability, and Serviceability* (RAS)
- *Debug Trace* (DT)

CI-700 is compatible with the following types of IP:

- *Dynamic Memory Controller* (DMC)
- *Generic Interrupt Controller* (GIC)

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- *Memory Management Unit* (MMU)
- Interconnect
- Armv8.0, Armv8.2, Armv8.4, and Armv9 processors

2.2 Compliance

The CI-700 product is based on Issue E of the AMBA® 5 CHI Architecture Specification.

This *Technical Reference Manual* (TRM) complements Architecture Reference Manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

AMBA® 5 CHI architecture

CI-700 supports the *AMBA® 5 CHI Architecture Specification* Issue E, and is also backwards compatible with Issue D, Issue C, and Issue B. For more information about compatibility, see 4.14 Backward compatible RN-F support on page 138.

The CI-700 product implements the following architecture capabilities:

- Fully compliant with CHI interconnect architecture
- Non-blocking coherence protocol
- Packet-based communication
- The following four types of channels:
  - *Request* (REQ)
  - *Response* (RSP)
  - *Snoop* (SNP)
  - *Data* (DAT)
- Credited end-to-end protocol-layer flow-control with a retry once mechanism for flexible bandwidth and resource allocation
- Integrated end-to-end *Quality-of-Service* (QoS) capabilities

For more information, see the *AMBA® 5 CHI Architecture Specification*

2.3 Features

The CI-700 product provides the following key features:

- Highly scalable mesh network topology configurable up to a 12 crosspoint mesh
- Custom mesh size and device placement
- A programmable *System Address Map* (SAM)

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- Up to eight RN-F interfaces for CHI-based compute clusters, accelerators, graphic processing units, or other cache coherent masters
- Optional *Component Aggregation Layer* (CAL) for device interface port expansion
- Up to eight SN interfaces
- Up to eight RN-Is with up to three ACE5-Lite ports each (24 total)


Note

More devices are supported by adding more levels of interconnect hierarchy to the system. For example, you can use the Arm® CoreLink™ NI-700 Network-on-Chip Interconnect or the Arm® CoreLink™ NIC-450 Network Interconnect to add more levels of interconnect hierarchy.

- Optional support for non-XY routing algorithm between specified source-target pairs
- TxnID of 12 bits for all flits
- Maximum *Physical Address* (PA) width of 40 bits
- DVM message transport between masters
- QoS regulation for shaping traffic profiles
- Configurable QoS override to transactions targeting specific memory regions
- A *Performance Monitoring Unit* (PMU) to count performance-related events
- High-performance distributed SLC and *Snoop Filter* (SF) up to eight HN-Fs and cache sizes of 0-32MB total:
  - The HN-F includes an integrated *Point-of-Serialization* (PoS) and *Point-of-Coherency* (PoC). The HN-F SLC (also referred to as Agile System Cache) can be used both for compute and I/O caching.
  - SF up to 64MB of tag RAM for increased coherency scalability consisting of up to eight partitions (one per HN-F).
- Up to four HN-Is, each with an ACE-Lite master port
- CHI *Memory Tagging Enhancements* (MTE)
- Optional support for extra device ports on MXPs. CI-700 supports a maximum of between four and six device ports on a single MXP, depending on your system configuration.
- *Device Credited Slices* (DCSs) used for register slices at device interfaces, allowing flexibility in device placement
- *Mesh Credited Slices* (MCSs) used for X-Y register slices, allowing flexibility in mesh floorplanning
- *CAL Credited Slices* (CCSs), allowing flexibility in mesh floorplanning in configurations that use the CAL
- *On-Chip Memory* (OCM) allows for the creation of CI-700 systems without physical DDR memory.
- RAS features including transport parity, optional data path parity, *Single-Error Correction and Double-Error Detection* (SECDED) ECC, and data poisoning signaling
- *Address Based Flush* (ABF)

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- Way-based SLC partitioning
- Source-based way locking
- *AXI4-Stream* (A4S) support (for GIC traffic only)
- Support for AXI loopback signaling
- *RN-F Direct Slave Access* (DSA-F), which provides a direct path from RN-F to MTSX
- Support for *Downstream Exclusive Cache* (DSC) functionality
- *Memory Tag Slave interface* (MTSX) slice channel configuration

2.4 Global configuration parameters

CI-700 has various global configuration parameters that define the properties and behavior of interconnect. These parameters also set and define the behavior of some of the optional features.

The following table shows the global configuration parameters for CI-700.

Table 2-1: Global configuration parameters

Parameter	Description	Values (default)	Comments
CHI_MPAM_ENABLE	MPAM feature enable	0, 1 (True)	-
REQ_RSVDC_WIDTH	Width of RSVDC field in REQ flit	4, 8, 16, 24, 32 (4)	-
REQ_ADDR_WIDTH	Width of ADDR field in REQ flit	44, 48 (48)	-
PA_WIDTH	System *Physical Address* (PA) width	34, 40 (40)	-
DATACHECK_EN	Data check enable	0, 1 (False)	Data check refers to data byte parity checking.
FLIT_PAR_EN	Flit parity enable	0, 1 (True)	-
RNSAM_NUM_NONHASH_REGION	Number of non-hashed regions that RN SAM supports.	2, 4, 8, 12, 16, 20 (8)	-
RNSAM_NUM_ADD_HASHED_TGT	Number of extra hashed target IDs supported by the RN SAM, beyond the local HN-F count	0, 2, 4, 8, 16, 32 (0)	Set to 0 for CI-700.
RNSAM_NUM_QOS_REGIONS	Number of memory regions for QoS override	0, 4, 8 (0)	-
XY_OVERRIDE_CNT	Number of Src-Tgt pairs whose XY route path can be overridden	0, 2, 4, 8, 16 (0)	-
MXP_MULTIPLE_DTM_EN	Multiple DTMs feature enable. This parameter is used if number of device ports on the XP is > 2.	0, 1 (False)	For the entire mesh, you can select either: • One DTM with support for up to six device ports per MXP • Multiple DTMs per MXP, one for every two device ports
DSC_ENABLE	Enables *Downstream Exclusive Cache* (DSC) feature	0, 1 (False)	-

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2.4.1 Addressing capabilities

CI-700 supports a 34-bit or 40-bit PA width. The PA width defines the PA space for which read and write transactions are supported in the interconnect. It is configured using Socrates and results in the `PA_WIDTH` global parameter in the CI-700 RTL.

CHI interfaces in CI-700 support 44-bit and 48-bit address field widths for REQ channel flits. This width is also configured using Socrates and results in the `REQ_ADDR_WIDTH` global parameter in the CI-700 RTL.

The address field width for SNP channel flits is derived automatically based on the `REQ_ADDR_WIDTH` global parameter.

The following table shows the legal combinations of physical address widths and flit address widths.

Table 2-2: Legal combinations of physical address and flit address widths

Physical address width	REQ flit address width	SNP flit address width (derived)
34b	44b	41b
34b	48b	45b
40b	44b	41b
40b	48b	45b

2.5 Device-level configuration parameters

Each internal device and external CHI device port have a set of configuration parameters. These parameters define the properties and behavior of the device or port and also set up optional features.

The following table shows the configuration parameters for individual CI-700 devices.


Note

When CAL is present, all the devices that are connected to it must be configured identically.

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Table 2-3: CHI device configurable options

Feature	Parameter	Description	Values (default)	Comments
RN-F port, SN-F port	POISON	Data poison enable (RN-F port only)	0, 1 (True)	-
	DATACHECK	Data check enable (RN-F port only) **Note:** DATACHECK must be set to 0 when global parameter DATACHECK is 0.	0, 1 (False)	End-to-end data byte parity enable
	RXBUF_NUM	Number of receive flit buffers inside CI-700 on this port. To achieve full bandwidth operation, this number must equal the CHI credit return latency (in cycles) for flit transfers from RN-F or SN-F to the interconnect. **Note:** The credit return latency is one cycle in the interconnect. This value must be added to the credit latency in the RN-F or SN-F to arrive at the total credit return latency.	2-4 (3)	The minimum value of 2 corresponds to a credit return latency of one cycle in the interconnect and one cycle in the RN-F or SN-F.
RN-I, RN-D	AXDATA_WIDTH	Data width on AXI or ACE-Lite interface	128, 256, 512 (128)	-
	NUM_WR_REQ	Number of write request tracker entries	4, 16, 24, 32, 64 (32)	-
	NUM_ATOMIC_BUF	Depth of atomic data buffers	2, 4, 8, 16, 32 (2)	-
	NUM_RD_REQ	Number of read request tracker entries	4, 32, 64, 96, 128, 256 (32)	If NUM_RD_BUF is 128 or 256, NUM_RD_REQ must be the same value. The number of tracker entries must be the same or larger than data buffer entries. NUM_RD_REQ ≥ NUM_RD_BUF.
	NUM_RD_BUF	Number of read data buffers	4, 8, 16, 24, 32, 64, 96, 128, 256 (24)	This value must be 256 when NUM_RD_REQ is 256 and should be less than or equal to NUM_RD_REQ for all other cases. NUM_RD_BUF > 64 instantiates RAM for data buffer.
	NUM_PREALLOC_RD_BUF	Number of pre-allocated read data buffers	4, 8, 16, 32 (8)	This value must be ≤ NUM_RD_BUF.
	AXDATAPOISON_EN	Data poison enable on AXI or ACE-Lite interface	0, 1 (0)	-
	AXLOOPBACK_EN	2-bit loopback enable on AXI or ACE-Lite interface	0, 1 (0)	-
	AXMPAM_EN	Enables MPAM feature on AXI or ACE-Lite interfaces.	0, 1 (True)	-
	FORCE_RDB_PREALLOC	Force read data buffer pre-allocation.	0, 1 (0)	-
	ID_WIDTH	ID width for slave ports	11, 16, 24, 32 (11)	-

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Feature	Parameter	Description	Values (default)	Comments
HN-F	SLC_SIZE	Size of system cache slice	0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, 4MB (2MB)	-
	SF_SIZE	Size of SF tag RAM slice	512KB, 1MB, 2MB, 4MB, 8MB (4MB)	-
	SLC_TAG_RAM_LATENCY	Latency of system cache tag RAM	1-3 cycles (2 cycles)	Valid Tag:Data RAM latency combinations: • 1:2 • 2:2 • 3:3
	SLC_DATA_RAM_LATENCY	Latency of system cache data RAM	2 cycles, 3 cycles (2 cycles)	
	NUM_ENTRIES_POCQ	Number of entries in the POCQ tracker	16, 32, 64 (32)	-
	MPAM_NS_PARTID_MAX	Maximum number of Non-secure MPAM partitions	1, 2, 4, 8, 16, 32, 64, 128, 256, 512 (64)	-
	MPAM_S_PARTID_MAX	Maximum number of Secure MPAM partitions	1, 2, 4, 8, 16, 32, 64, 128, 256, 512 (16)	-
	MPAM_NS_PMG_MAX	Maximum number of Non-secure MPAM PMGs	1, 2 (2)	-
	MPAM_S_PMG_MAX	Maximum number of Secure MPAM PMGs	1, 2 (2)	-
	MPAM_NUM_CSUMON	Maximum number of MPAM CSU monitors	1, 2, 4, 8, 16 (4)	-
HN-I, HN-D, HN-T	AXDATA_WIDTH	Data width on AXI or ACE-Lite interface	128, 256, 512 (128)	-
	NUM_AXI_REQS	Number of request tracker entries	8, 32, 64 (32)	-
	AXDATAPOISON_EN	Data poison enable on AXI or ACE-Lite interface	0, 1 (True)	-
	AXMPAM_EN	Enables MPAM feature on AXI or ACE-Lite interfaces.	0, 1 (True)	-
SBSX	NUM_DART	Number of DART tracker entries	64, 128 (64)	-
	NUM_WR_BUF	Number of write data buffers	8, 16 (8)	-
	AXDATA_WIDTH	Data width on AXI or ACE-Lite interface	128, 256 (128)	-
	AXDATAPOISON_EN	Data poison enable on AXI or ACE-Lite interface	0, 1 (True)	-
	AXMPAM_EN	Enables MPAM feature on AXI or ACE-Lite interfaces.	0, 1 (True)	-
	SBSX_CMO_ON_AW	Enables write channel CMOs on AXI or ACE-Lite interface.	0, 1 (False)	If enabled, CMOs are sent only on AW channel.
	NUM_SBSX_MTU_RDB	Number of read data buffers in SBSX	4, 8, 16, 32, 64 (32)	This parameter is only applicable to MTSX nodes.
MTU	TC_SIZE	Size of tag cache	0KB, 128KB, 256KB, 512KB, 1MB, 2MB (1MB)	-
	NUM_TCQ_REQ	Number of TCQ request tracker entries	16, 32, 64 (32)	-

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Feature	Parameter	Description	Values (default)	Comments
	NUM_TCQ_DATA_BUF	Number of TCQ data buffer entries	4, 8, 16, 32 (16)	-
	MAX_DRAM_ADDR_WIDTH	Width of DRAM addr downstream of MTU block	30, 31, 32, 33, 34, 36 (30)	-

2.6 Test features

The CI-700 product includes several test features.

For information about the test features, see the *Arm® CoreLink™ CI-700 Coherent Interconnect Configuration and Integration Manual*

2.7 Product documentation and design flow

The CI-700 product manuals support the design flow process.

Documentation

The following documentation supports the CI-700 product:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality, and how functional options affect the behavior of CI-700. It is required at all stages of the design flow. The choices that you make in the design flow can mean that some behavior that is described in the TRM is not relevant. If you are programming the CI-700 product, contact the following people:

- The implementer to determine:
  - The build configuration of the implementation
  - What integration, if any, was performed before implementing the CI-700 product
- The integrator to determine the pin configuration of the device that you are using

Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes how to integrate the CI-700 product into an SoC. It includes a description of the pins that the integrator must tie off to configure the macrocell for the required integration. The CIM also describes:

- The available build configuration options and related issues in selecting them
- How to configure the *Register Transfer Level* (RTL) with the build configuration options
- How to integrate RAM arrays
- How to run test patterns
- The processes to sign off the configured design

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The Arm product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by Arm are example reference implementations. Contact your EDA vendor for EDA tool support.

User Guide

The *User Guide* (UG) describes how to use Socrates™ to configure and integrate a custom mesh interconnect.



The UG is part of the Socrates™ product download bundle.

Design flow

CI-700 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer configures and synthesizes the RTL to produce a hard macrocell. This process includes integrating RAMs into the design.

Integration

The integrator connects the implemented design into an SoC. This process includes connecting a memory system and peripherals.

Programming

Programming is the last process. The system programmer develops the software that is required to configure and initialize the CI-700 product, and tests the required application software.

Each process can:

- Be performed by a different party
- Include implementation and integration choices that affect the behavior and features of the CI-700 product

The operation of the final device depends on:

Build configuration

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

Configuration inputs

The integrator configures some features of the CI-700 product by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration

The programmer configures the CI-700 product by programming particular values into registers. The register configuration affects the behavior of the CI-700 product.

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Note

This manual refers to **IMPLEMENTATION DEFINED** features that are applicable to build configuration options. A reference to a feature that is included means that the appropriate build and pin configuration options are selected. A reference to an enabled feature means one that software has also configured.

2.8 Product revisions

This section describes the differences in functionality between successive product revisions of the CI-700 product.

r0p0

First release.

r1p0

Added the following functionality:

- *RN-F Direct Slave Access* (DSA-F)

r2p0

Added the following functionality:

- *Downstream Exclusive Cache* (DSC) support

r3p0

Added the following functionality:

- MTSX slice channel configuration

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3 Components and configuration

This chapter describes the structure of a CI-700 interconnect. It also describes the internal and external components and things to consider when you configure the interconnect.

You must use the Socrates™ system IP tooling to configure a CI-700 interconnect instance. This TRM does not provide information about how to use Socrates™. For information about using Socrates™, see the *Arm® Socrates™ for CoreLink™ CI-700 Coherent Interconnect User Guide*, which is bundled with the tool.

3.1 Structure of a CI-700 interconnect

The structure of a CI-700 interconnect is always an arrangement of *Crosspoints* (XPs) and CHI-compliant devices. XPs connect together to form a mesh, and CHI-compliant devices connect to device ports on the XPs. When configuring CI-700, you create a topology from these building blocks, according to your system requirements.

A CI-700 interconnect is a network that is made up of two types of component: CHI devices and XPs. CHI devices generate and receive network requests and responses, and process data. CHI devices connect to XPs through XP device ports. XPs are network routers, which send requests, responses, and data in packets between devices on an XP, or to another XP in the network.

A CI-700 configuration can have multiple XPs or a single XP. We refer to configurations with more than one XP as mesh configurations and configurations with one XP as single-XP configurations.

In a mesh configuration, the XPs connect horizontally and vertically to each other to form a two-dimensional mesh structure.

XPs have device ports for connecting external CHI-compliant devices, or internal CI-700 devices.

For example, the following figure shows a 4 × 2 mesh configuration containing various types of external and internal CHI devices.

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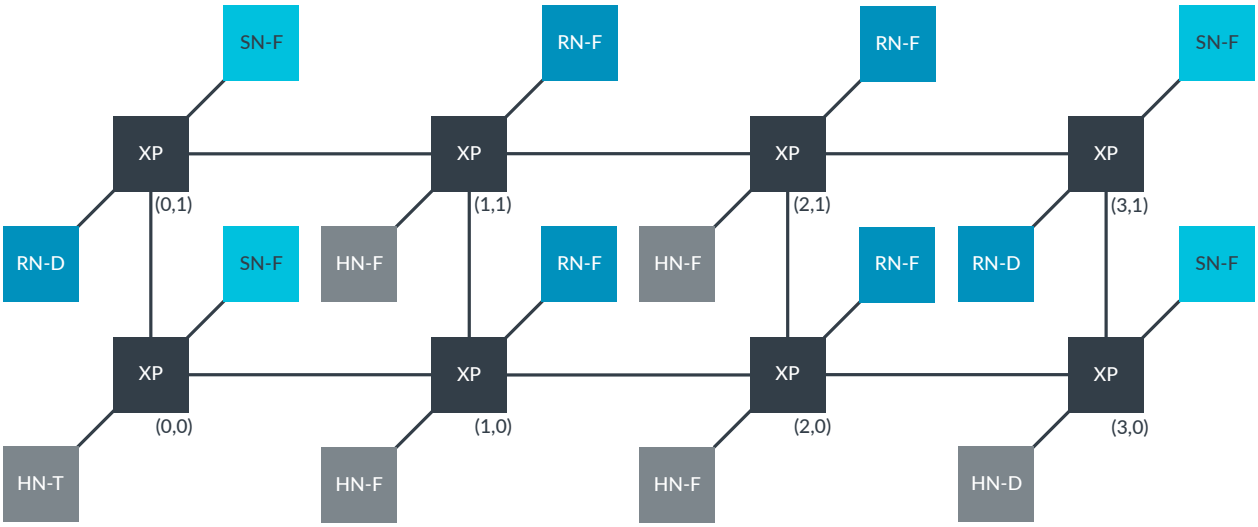
Figure 3-1: Example 4 × 2 mesh configuration



The number of device ports per XP depends on whether you use a mesh configuration or single-MXP configuration. For more information, see 3.2 Crosspoint (XP) on page 28.

Internal CI-700 devices have various functions. For example, some of these devices have AXI and ACE-Lite interfaces to attach external AXI and ACE-Lite hardware. These devices form bridges between the external hardware and CI-700, which is a CHI interconnect.

Related information

- 2.2 Compliance on page 18
- 3.3 External interfaces on page 32
- 3.4 Components on page 34
- 3.5 Configure CI-700 on page 43

3.2 Crosspoint (XP)

The *crosspoint* (XP) is a switch or router logic module. It is the fundamental building block of the CI-700 transport mechanism.

Note

The terms XP, *Mesh Crosspoint* (MXP), and *Super Mesh Crosspoint* (SMXP) are used interchangeably throughout this TRM.

The CI-700 mesh interconnect is built using a set of XP modules. By default, each XP can connect to up to four neighboring XPs using mesh ports, the following figure shows.

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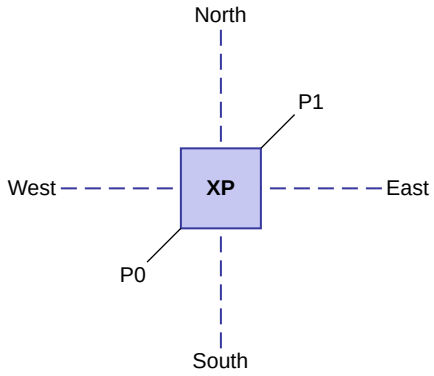
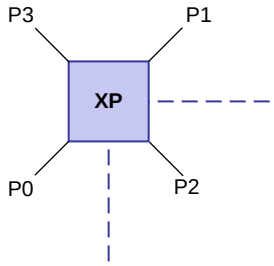
Figure 3-2: Default crosspoint configuration



The dashed lines in the preceding figure represent mesh ports. By default, each XP also has two device ports, P0 and P1, for connecting devices.

CI-700 also supports extra device ports on an MXP. When using extra device ports in a mesh configuration, you can have up to four device ports per XP, as the following figure shows.

Figure 3-3: Crosspoint structure in mesh configuration with extra device ports



When using a single-XP configuration with extra device ports, you can have up to six device ports on the XP, as the following figure shows.

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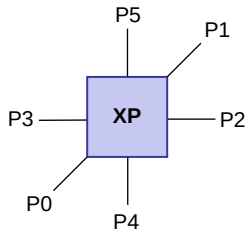
Figure 3-4: Crosspoint structure in single-XP configuration with extra device ports



For more information about support for extra device ports, see 3.10 Support for extra device ports on MXPs on page 50.

Each XP supports four CHI channels for transporting flits across the mesh from a source device to a destination or target device:

- *Request* (REQ)
- *Response* (RSP)
- *Snoop* (SNP)
- *Data* (DAT)

The XP modules can be arranged in a two-dimensional rectangular mesh topology.

The maximum size for the CI-700 mesh is 12 XPs. Each XP in the grid is referenced using an (X,Y) coordinate system. (0,0) represents the bottom-left corner, and the maximum coordinate, which represents the upper-right corner, depends on your configuration. The following figure shows a 3 × 4 mesh configuration with some (X,Y) coordinate values.

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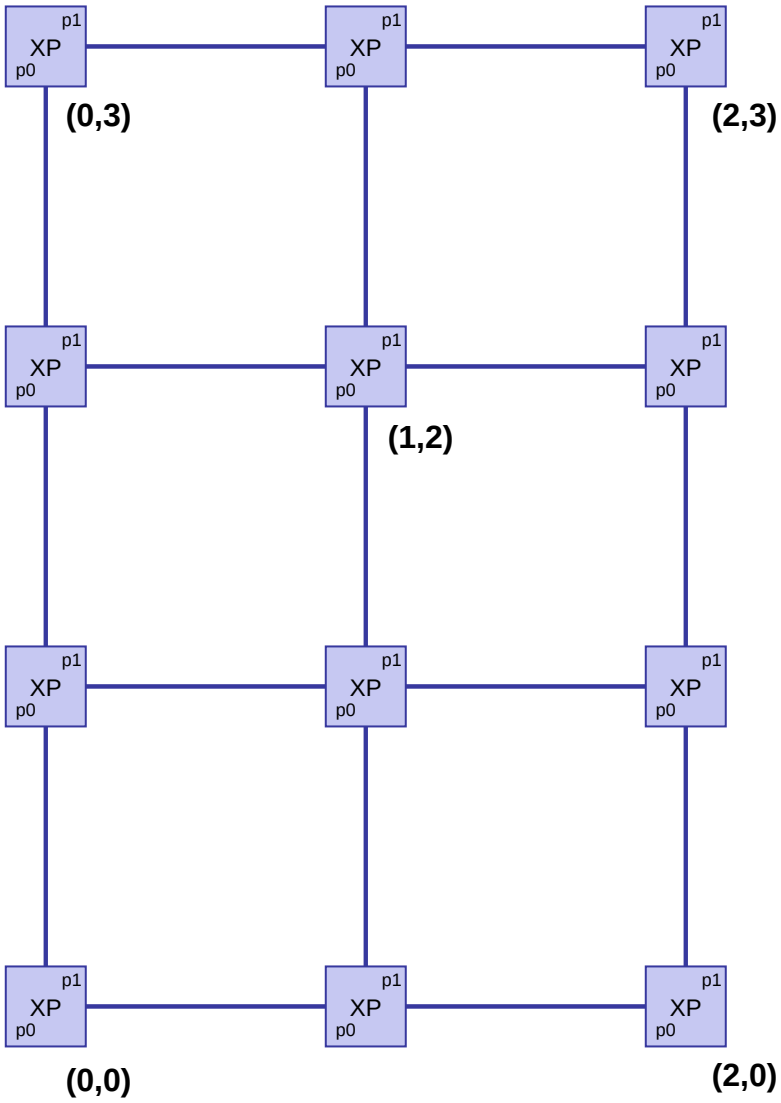
Figure 3-5: 3 × 4 mesh configuration



The following figure shows an example 3 × 3 mesh configuration, with devices attached to XP ports.

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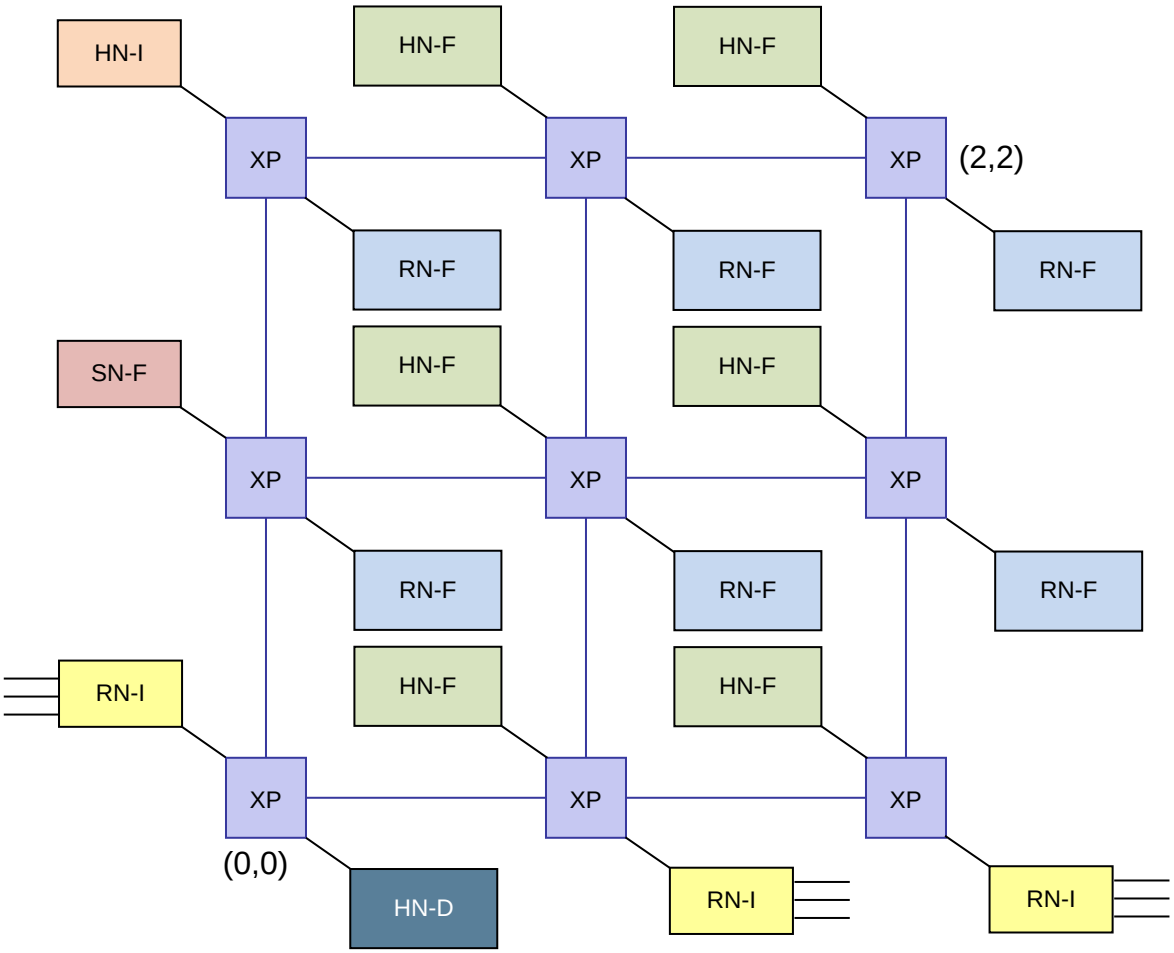
Figure 3-6: Example 3 × 3 mesh configuration



Note

The x and y coordinates of an XP are also known as the XID and YID respectively.

3.3 External interfaces

You can connect external CHI-compatible hardware, such as a processor cluster or memory controller, directly to CI-700 through an XP device port. Alternatively, CI-700 has various internal devices with external interfaces for connecting non-CHI external hardware.

The following figure shows the types of external interfaces that the CI-700 product has.

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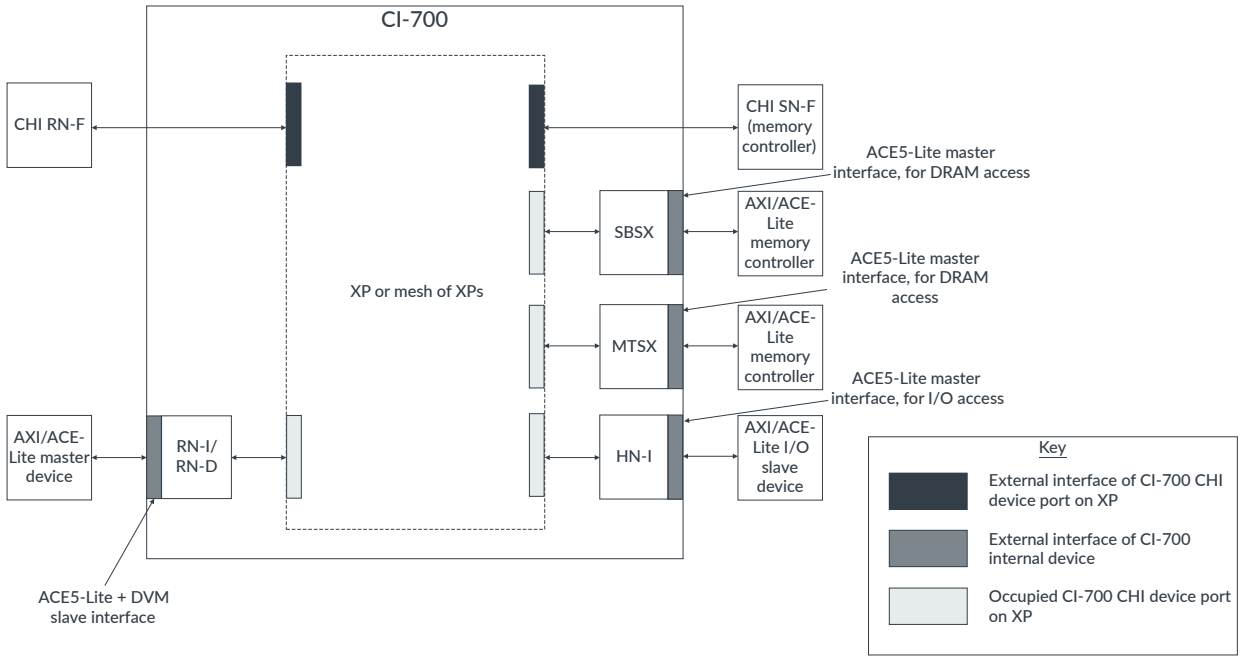
Note

The figure shows one instance of each interface type, but the number of each type is configurable according to your system requirements. For more information about the supported number of each interface, see Table 3-1: CHI external interface type use, location, and permitted number on page 33.

Figure 3-7: CI-700 interfaces



The following table shows information about the use, location, and permitted number of each type of CI-700 external interface.

Table 3-1: CHI external interface type use, location, and permitted number

External interface type	Use	Location	Permitted number
Interface on CHI device port	Connect native CHI *Fully coherent Request Nodes* (RN-Fs). RN-Fs are master devices with hardware-coherent caches.	XP	1-8
	Connect native CHI *Fully coherent Slave Nodes* (SN-Fs), such as DRAM memory controllers.		1-8 SN-Fs, SBSXs, and MTSXs are counted together, meaning that CI-700 supports a maximum combined total of 8 of these interfaces.
ACE5-Lite master interface, for DRAM access	Connect AXI or ACE-Lite DRAM memory controllers.	*CHI to AXI or ACE-Lite bridge* (SBSX)	
		Memory Tag Slave Interface (MTSX)	
ACE5-Lite master interface, for I/O access	Connect AXI or ACE-Lite slave devices, such as an I/O slave or subsystem containing multiple I/O slaves.	HN-I or HN-I variant	1-4

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External interface type	Use	Location	Permitted number
ACE5-Lite + DVM slave interface	Connect AXI or ACE-Lite master devices, that do not contain hardware-coherent caches.	RN-I or RN-D	3-24

Related information

- 3.4 Components on page 34
- 3.6 System component selection on page 44

3.4 Components

CI-700 is made up of various types of devices with different functionality, including router modules, CHI nodes, and bridges. The full list of components that you need depends on the requirements of your system. Some components are optional or only used if certain requirements are met.


Note

CI-700 can be integrated into a complete SoC system that includes devices that this section does not describe.

External devices

You can connect CHI *Fully coherent Requesting Nodes* (RN-Fs) and *CHI Slave Nodes* (SN-Fs) as external system components to the CI-700 interconnect through device ports. The CI-700 product does not include these components, but you must specify them when you are building your interconnect topology.

The following table shows the external device types that CI-700 supports.

Table 3-2: Supported external devices

Device	Description
RNF_CHIB_ESAM	A CHI Issue B-compliant RN-F without a built-in SAM. RN-Fs are processors, clusters, GPUs, or other RNs with a coherent cache. ESAM-type RN-Fs do not have a built-in SAM, and the SAM logic is contained within CI-700. For more information about backward-compatible RN-F support and the SAM, see 4.14 Backward compatible RN-F support on page 138 and 4.4 System Address Map on page 82.
RNF_CHIC_ESAM	A CHI Issue C-compliant RN-F without a built-in SAM. For more information about backward-compatible RN-F support and the SAM, see 4.14 Backward compatible RN-F support on page 138 and 4.4 System Address Map on page 82.
RNF_CHID_ESAM	A CHI Issue D-compliant RN-F without a built-in SAM. For more information about backward-compatible RN-F support and the SAM, see 4.14 Backward compatible RN-F support on page 138 and 4.4 System Address Map on page 82.
RNF_CHIE_ESAM	A CHI Issue E-compliant RN-F without a built-in SAM. For more information about backward-compatible RN-F support and the SAM, see 4.14 Backward compatible RN-F support on page 138 and 4.4 System Address Map on page 82.

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Device	Description
CHI Slave Node (SN-F)	SN-Fs are CHI memory controllers. SN-Fs are devices which solely receive CHI commands, limited to fulfilling simple read, write, and CMO requests targeting normal memory. CI-700 supports SN-Fs with a native CHI-C, CHI-D, or CHI-E SN interface.

Internal CI-700 devices

CI-700 contains several CHI-compliant device components with different functionality. These components connect to the device ports on XPs. You can use some of these devices to connect certain types of non-CHI master and slave devices to CI-700.

The following table lists the device types that are supplied with CI-700.

Table 3-3: CI-700 device types

Device	Description
IO coherent Request Node (RN-I)	Use an RN-I to connect one or more AXI or ACE-Lite master devices to CI-700. RN-Is have 3 external AXI or ACE-Lite slave interfaces for connecting AXI or ACE-Lite master devices to, and bridges between AXI/ACE-Lite and CHI protocols. Within the interconnect, the RN-I is a non-caching I/O-coherent master device. Therefore, it acts as a CHI RN-I proxy for each upstream AXI or ACE-Lite master device. There is no capability to issue snoop transactions to RN-Is. For more information about the RN-I, see 3.4.1 I/O coherent Request Node (RN-I) and I/O coherent Request Node with DVM support (RN-D) on page 37.
IO coherent Request Node with DVM support (RN-D)	A subtype of RN-I with an ACE-Lite-with-DVM slave interface, allowing the RN-D to accept *Distributed Virtual Memory* (DVM) messages on the snoop channel
Fully coherent Home Node (HN-F)	The HN-F acts as a *Home Node* (HN) for a coherent region of memory. HN-Fs accept coherent requests from RN-Fs and RN-Is, and generate snoops to all applicable RN-Fs in the system as required to support the coherency protocol. HN-Fs are typically configured with one or both of the internal SLC and SF components. The SLC acts as a last-level cache and the SF tracks cachelines that RN-Fs in the system have cached. HN-Fs also contain the combined *Point-of-Serialization and Point-of-Coherency* (PoS and PoC), which is responsible for ordering of all memory requests sent to the HN-F. For more information about the HN-F and its internal components, see 3.4.2 Fully coherent Home Node (HN-F) on page 37.
IO coherent Home Node (HN-I)	Use HN-Is to connect non-coherent I/O slaves or subsystems to CI-700. HN-Is have an external AXI or ACE-Lite master interface and act as an HN for a downstream I/O slave or subsystem. They are responsible for ensuring proper ordering of requests targeting the slave. HN-Is do not support caching of any data read from or written to the downstream I/O slave or slave subsystem. For more information about this topic and more general information about the HN-I, see 3.4.3 I/O coherent Home Node (HN-I) on page 38.
IO coherent Home Node with Debug Trace Controller (HN-T)	A subtype of HN-I with a built-in *Debug Trace Controller* (DTC) and ATB. For more information about the DTC, see Debug Trace Controller (DTC) on page 39.

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Device	Description
IO coherent Home Node with DVM node (HN-D)	A subtype of HN-I with the following built-in components: • DTC • *DVM Node* (DN) • *Configuration Node* (CFG) • Global Configuration Slave • *Power/Clock Control Block* (PCCB) **Note:** Exactly one HN-D is required per CI-700 instance. The HN-D has an AXI or ACE-Lite external master interface, an APB interface, and supports ATB. For more information about the DTC, CFG, and DTC, see the following sections: • Debug Trace Controller (DTC) on page 39 • Configuration Node (CFG) on page 39 • Power/Clock Control Block (PCCB) on page 40
CHI to AXI or ACE-Lite bridge (SBSX)	Use an SBSX to connect an AXI or ACE-Lite slave memory device to CI-700. For example, you can use an SBSX to connect the CoreLink™ DMC-400 Dynamic Memory Controller to a CI-700 system. SBSXs have an external AXI or ACE-Lite master interface for connecting an AXI or ACE-Lite slave to, and bridges between CHI and AXI/ACE-Lite protocols. They convert and forward simple CHI read, write, and CMO commands to the slave memory device. If connecting a device that supports AXI-G or earlier through the SBSX, then you must tie some of the SBSX pins to certain values. For more information, see B.4.5 Conditions for tying off AXI/ACE-Lite master interface pins on page 1391. For more information about the SBSX, see 3.4.4 AMBA 5 CHI to ACE5-Lite bridge (SBSX) on page 40.
Memory Tag Slave Interface (MTSX)	Use an MTSX to connect AXI slave devices that do not support memory tagging to CI-700. MTSXs have an external AXI or ACE-Lite master interface for connecting an AXI or ACE-Lite slave to, and bridges between CHI and AXI/ACE-Lite protocols. They convert and forward simple CHI read, write, and CMO commands to the slave memory device. For more information about the MTSX, see 3.4.5 Memory Tag Slave Interface (MTSX) on page 40.

Mesh components

CI-700 includes various internal components that you can use to customize the structure of the interconnect.

The following table shows the mesh components that CI-700 supports.

Table 3-4: CI-700 mesh components

Component	Description
Crosspoint (XP)	A switch or router logic module. XPs are the fundamental building block of the CI-700 transport mechanism. XPs connect together through mesh ports. Devices connect to the mesh through device ports on XPs. For more information about the XP, see 3.2 Crosspoint (XP) on page 28.

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Component	Description
Component Aggregation Layer (CAL)	Allows multiple devices to connect to a single device port on an XP. Only certain devices can connect to CALs. All devices that connect to a single CAL must be of the same type and you must configure them identically. For more information, see 3.4.6 Component Aggregation Layer (CAL) on page 41.
Credited Slices (CSs)	Credited register slices that incur latency in communication but help with timing closure. There are various types of CSs, which are used for different parts of the interconnect. For more information, see the following sections: • 3.4.7 Credited Slices (CSs) on page 41 • 3.4.7.1 Mesh Credited Slice (MCS) on page 43 • 3.4.7.2 Device Credited Slice (DCS) on page 43 • 3.4.7.3 CAL Credited Slice (CCS) on page 43
CHI Domain Bridge (CDB)	Bridges two CHI interfaces that operate in two different clock domains, power/voltage domains, or both. For more information about the CDB, see the *Arm® CoreLink™ CI-700 Coherent Interconnect Configuration and Integration Manual*, which is only available to licensees.
AMBA Domain Bridge (ADB)	Bridges two AXI, ACE5-Lite, or ACE5-Lite-with-DVM interfaces that operate in two different clock domains, power/voltage domains, or both. For more information about the ADB, see the *Arm® CoreLink™ CI-700 Coherent Interconnect Configuration and Integration Manual*, which is only available to licensees.

Related information

- 3.8 Permitted numbers of devices and system resources in the mesh on page 47

3.4.1 I/O coherent Request Node (RN-I) and I/O coherent Request Node with DVM support (RN-D)

The *I/O-coherent Request Node* (RN-I) and *I/O coherent Request Node with DVM support* (RN-D) connect I/O-coherent AMBA masters to the rest of the CI-700 system.

An RN-I bridge includes three ACE-Lite slave interfaces. An RN-D bridge includes three ACE-Lite-with-DVM slave ports.

The RN-I and RN-D bridges can act as a proxy only for masters that do not contain hardware-coherent caches. There is no capability to issue snoop transactions to RN-Is or RN-Ds.

3.4.2 Fully coherent Home Node (HN-F)

HN-Fs are responsible for managing the coherent part of the system address space. HN-Fs have various subcomponents, which support its function as the HN for coherent memory. Some of these components are required and some are optional.

Each HN-F in the system is configured to manage a specific portion of the overall address space. The entire DRAM space is managed through the combination of all HN-Fs in the system.

The HN-F consists of the following components:

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SLC

The SLC is a last-level cache. The SLC allocation policy is exclusive for data lines, except where sharing patterns are detected and pseudo-inclusive for code lines, as indicated by the RN-Fs. All code lines can be allocated into the SLC on the initial request.

When MTE is enabled, SLC stores data and tags.

Combined PoS and PoC

The combined PoS and PoC are responsible for the ordering of all memory requests sent to the HN-F. Ordering includes serialization of multiple outstanding requests and actions to the same cache line, and request ordering as required by the RN-F.

SF

The SF tracks cache lines that are present in the RN-Fs. Using the SF reduces snoop traffic in the system by favoring directed snoops over snoop broadcasts when possible. This approach substantially reduces the snoop response traffic that might otherwise be required.



The HN-F is architecturally defined to manage only well-behaved memory, which is memory without any possible side effects. The HN-F includes microarchitectural optimizations to exploit this architectural guarantee.

3.4.3 I/O coherent Home Node (HN-I)

The *I/O coherent Home Node* (HN-I) is an HN for all CHI transactions targeting AMBA slave devices.

The HN-I acts as a proxy for all the RNs of CI-700, converting CHI transactions to ACE5-Lite transactions. The HN-I includes support for the correct ordering of Arm device types.

The HN-I does not support caching of any data read from or written to the downstream ACE5-Lite I/O slave subsystem. Any cacheable request that is sent to the HN-I does not result in any snoops being sent to RN-Fs in the system. Instead, the request is converted to the appropriate ACE5-Lite read or write command and sent to the downstream ACE5-Lite subsystem.



If an RN-F caches data that is read from or written to the downstream ACE5-Lite I/O slave subsystem, coherency is not maintained. Any subsequent access to that data reads from or writes to the ACE5-Lite I/O slave subsystem directly, ignoring the cached data.

CI-700 also has the following HN-I variants with extra functionality:

***IO coherent Home Node with Debug Trace Controller* (HN-T)**

HN-I subtype with a built-in *Debug Trace Controller* (DTC) and ATB.

***IO coherent Home Node with DVM node* (HN-D)**

HN-I subtype with the following built-in components:

- DTC

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- *DVM Node* (DN)
- *Configuration Node* (CFG)
- Global configuration slave
- *Power/Clock Control Block* (PCCB)

Debug Trace Controller (DTC)

The DTC controls distributed *Debug and Trace Monitors* (DTMs) and generates time stamped trace using the ATB interface. DTCs are present in HN-D and HN-T nodes.

The DTC performs the following functions:

- Generates event or PMU-based interrupts
- Receives packets from DTM and packs them into ATB format trace
- Time stamps trace with SoC timer input
- Generates alignment sync for the ATB trace output
- Handles ATB flush requests
- Handles debug and Secure debug external requests
- Provides a consistent view of distributed and central PMU counters
- Handles PMU snapshot requests
- Generates interrupt **INTREQPMU** assertion on overflow of PMU counters

Configuration Node (CFG)

The CFG is co-located with the HN-D node and handles various CI-700 configuration, control, and monitoring features.

The CFG carries out the following functions:

- Configuration accesses
- Error reporting and signaling
- Interrupt generation

The CFG includes the following elements:

- Ports to collect error signals from CHI components within CI-700
- A configuration bus which connects to all the nodes to handle internal configuration register reads and writes
- A dedicated APB interface for configuration accesses

The CFG does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

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Power/Clock Control Block (PCCB)

The PCCB, co-located with the HN-D node, provides separate communication channels. These channels pass information about the power and clock management between the SoC and the network.

The PCCB acts as an aggregator to convey information between the SoC and the other CI-700 components, in the following way:

1. The PCCB receives transaction activity indicators from other relevant CI-700 components and conveys that information to the external power and clock control units.
2. The PCCB receives power or clock control management requests from the external power or clock control units. Where applicable, it conveys that request to the relevant CI-700 components.
3. The PCCB waits for the appropriate responses from the relevant CI-700 components, and conveys an aggregated response to the external power and clock control units.

The PCCB does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

3.4.4 AMBA 5 CHI to ACE5-Lite bridge (SBSX)

The *AMBA 5 CHI to ACE5-Lite bridge* (SBSX) enables an ACE5-Lite slave device such as a CoreLink™ DMC-400 Dynamic Memory Controller, to be used in a CI-700 system.

If connecting a device that supports AXI-G or earlier through the SBSX, then you must tie some of the SBSX pins to certain values. For more information, see B.4.5 Conditions for tying off AXI/ACE-Lite master interface pins on page 1391.

3.4.5 Memory Tag Slave Interface (MTSX)

The *Memory Tag Slave Interface* (MTSX) node connects AXI slave devices without memory tagging support to a CHI-E interconnect that requires MTE support.

MTSX contains two internal elements, an SBSX element and a *Memory Tag Unit* (MTU) element. The MTU element is made up of the following parts:

- *Tag Control Queue* (TCQ)
- Optional *Tag Cache* (TC)

In the HN-F SAM, MTSX can only be targeted using non-hashed SN target-based SAM programming.

For more information about the MTSX, see the following sections:

- 4.18.6 MTSX functionality on page 167
- 4.17.8 MTU error handling on page 155
- 5.4.6 MTSX programming on page 1284

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- 8.6 MTSX performance events on page 1360

3.4.6 Component Aggregation Layer (CAL)

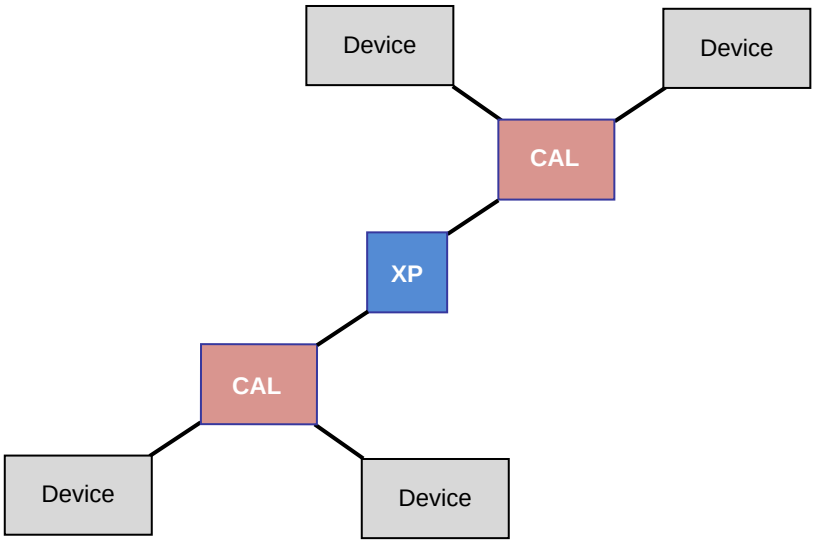
The *Component Aggregation Layer* (CAL) allows up to two devices to connect to a single device port on the XP.

You can connect the following device types to a CAL:

- RN-F_CHIB_ESAM
- RN-F_CHIC_ESAM
- RN-F_CHID_ESAM
- RN-F_CHIE_ESAM
- RN-I
- RN-D
- HN-F
- HN-I
- SBSX
- MTSX

Both devices that are connected to a single CAL must be of the same type and you must configure them identically. The following figure shows an example XP with two CALs.

Figure 3-8: CAL example configuration



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3.4.7 Credited Slices (CSs)

You can configure various optional credited register slices in your CI-700 system. These *Credited Slices* (CSs) can help with timing closure.

CSs enable synchronous but higher latency communication at any point in the system.

CI-700 includes the following optional CSs:

Mesh Credited Slice

Placed between XPs. For more information, see 3.4.7.1 Mesh Credited Slice (MCS) on page 43.

Device Credited Slice

Placed between a device and a CAL, or a device and an XP. For more information, see 3.4.7.2 Device Credited Slice (DCS) on page 43.

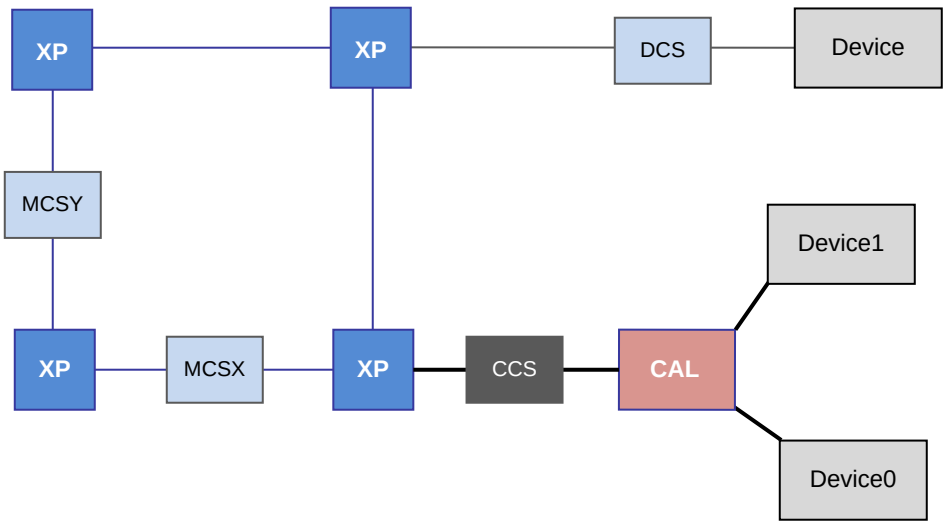
CAL Credited Slice

Placed between a CAL and an XP. For more information, see 3.4.7.3 CAL Credited Slice (CCS) on page 43.

The slices are simple repeater-flop structures that are applied across the entire communication boundary. The supported number of CSs of each type is specified in 3.9 Configurable options for mesh structure on page 49.

The following figure shows where various CSs fit in the structure of the mesh. The example mesh includes two MCSs, which are denoted as MCSX and MCSY according to the X or Y direction of the link. It also includes a DCS and a CCS.

Figure 3-9: Example MCSX, MCSY, CCS, and DCS configuration



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3.4.7.1 Mesh Credited Slice (MCS)

You can configure one or more *Mesh Credited Slices* (MCSs) between CI-700 XPs. MCSs are optional register slices that can help timing closure in a CI-700 system.

The CI-700 mesh can operate with a single cycle of latency between XPs. However, depending on the fabrication process and the distance between XPs, a single-cycle XP-XP connection might limit frequency. In this case, one or more MCSs can be added to lengthen the XP-XP links. Register slices add link transfer latency, but also allow certain CI-700 implementations to run at higher frequencies.

Each MCS on an XP-XP link adds an extra cycle for transfer between XPs. One to four MCSs can be added to any link between XPs.

An MCS that is placed between adjacent XPs in the same row is called an MCSX. Similarly, an MCS that is placed between adjacent XPs in the same column is called an MCSY.

3.4.7.2 Device Credited Slice (DCS)

You can configure one or more *Device Credited Slices* (DCSs) on a link between a device and an XP. DCSs help with timing closure in a CI-700 system.

DCSs are optional register slices that you can add to your CI-700 configuration. You can add up to four DCSs on any link between a device and an XP.

3.4.7.3 CAL Credited Slice (CCS)

You can configure up to two CCSs on the link between a CAL and an XP.


Note

When CCS is used, the number of DCSs on the upstream link between the device and the CAL is limited to a maximum of two.

3.5 Configure CI-700

Using Socrates™, you can configure the structure and properties of the CI-700 to suit the requirements of your system. There are specific steps you can follow to ensure that you have the correct components and configuration as you build and refine your CI-700 topology.

Before you begin

You must install and familiarize yourself with the Socrates™ system IP tooling before configuring CI-700.

We recommend that you follow the tutorial in *Chapter 4* in the *Arm® Socrates™ for CoreLink™ CI-700 Coherent Interconnect User Guide* before creating your own system.

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About this task

CI-700 has configuration parameters to customize the properties of the whole mesh and individual devices. You use Socrates™ to configure the values of these parameters and adjust the structure and of your mesh configuration and the placement of devices within it.

For more information about using Socrates™ to configure CI-700, see the *Arm® Socrates™ for CoreLink™ CI-700 Coherent Interconnect User Guide*. The *User Guide* is bundled with the Socrates™ tool.

See 3.12 Example system configurations on page 52.

Procedure

1. Select your system devices.
   This step identifies the external interfaces and therefore the external and internal devices to specify in the mesh topology. It also identifies some of the internal devices that you require to set up specific CI-700 functionality. For more information, see 3.6 System component selection on page 44.
2. Configure the mesh size and top-level parameters.
   During this step, you set physical parameters to determine the dimensions of the mesh, and global interconnect configuration parameters. For more information about the constraints on mesh sizing and the global configuration parameters and their values, see the following sections:
   - 3.7 Deciding on the size of the mesh on page 47
   - 3.8 Permitted numbers of devices and system resources in the mesh on page 47
   - 2.4 Global configuration parameters on page 20
3. Place and configure individual devices and CSs within the mesh.
   Each device has its own set of configuration parameters which adjust its behavior. You can also place different types of CSs on certain paths to help with timing closure.
   See 2.5 Device-level configuration parameters on page 21.

3.6 System component selection

Your system architecture and requirements for certain functionality determine the number and type of components to specify in the mesh topology. Specific components perform specific functions, so requirements differ between CI-700 configurations.

To understand what components you must specify in your mesh topology, you must consider the following factors:

- The functional requirements of your system
- The types of master and slave devices that you have

These factors determine the number and type of external interfaces and the amount of system resources that you require. Therefore, they affect the number and type of devices that you require. The considerations can be split into several categories:

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- The number and type of requesting masters in your system
- The number and type of *Home Nodes* (HNs) that you require, which is affected by the following factors:
  - The coherent memory requirements of your system
  - The number and type of I/O slaves or I/O subsystems in your system
- The number and type of memory controllers in your system

There are constraints on the number of certain types of components. For the full list of these design constraints, see 3.8 Permitted numbers of devices and system resources in the mesh on page 47.

Requesting masters

Requesting masters are located outside of the mesh and connect to slave ports on CI-700.

Requesting CHI masters with coherent caches, such as processors, GPUs, or processing elements with internal coherent caches, are referred to as RN-F devices. They connect directly to the CI-700 interconnect mesh using a CHI RN-F port.

Typically a CI-700 system requires a single RN-F port per RN-F in your system. However, if your system contains RN-Fs with multiple interfaces, then you might require more than one RN-F port per RN-F. Alternatively, you can use a CAL to connect those devices to CI-700.

I/O coherent requesting masters are either I/O masters, processing elements without internal caches, or processing elements with internal caches that are not hardware coherent. They connect to CI-700 RN-I bridge devices using ACE-Lite ports. Each RN-I bridge device has three ACE-Lite interfaces.

A single I/O coherent requesting master can be connected directly to a CI-700 ACE-Lite port. Alternatively, multiple masters can share a single ACE-Lite port by connecting through external AMBA interconnect components. The following factors affect the number of RN-Is that you require:

- How many of the ports on an RN-I are in use
- How many I/O coherent requesting masters are connected to a single port

Optimal use of RN-Is and the slave interfaces depend on traffic bandwidth requirements and physical floorplan tradeoffs. These constraints are outside the scope of this TRM.

Home nodes

In a CHI interconnect, you assign a single HN to each byte of the system address space. That HN is responsible for handling all memory transactions that are associated with that address. There are two types of HNs in CI-700: HN-Fs and HN-Is.

HN-F devices are the HNs for all coherent memory, although they also support non-coherent memory accesses. Memory that is mapped to an HN-F targets DRAM.

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Your SLC requirements affect the number of HN-Fs that you require. If your CI-700 instance has an SLC memory system, each HN-F contains a slice of the SLC. You can configure the size of the SLC slice per HN-F up to a maximum of 4MB. Therefore, the total amount of SLC in your system and the relative size of each SLC slice affects the number of HN-Fs that you require.


Note

The amount of SLC and number of HN-Fs are configured separately.

The other factor that affects the number of HN-Fs that you require is system performance. If your system has many RN-Fs, system performance might be improved by increasing the number of HN-Fs. By increasing the number of HN-Fs, you reduce the amount of traffic targeting each HN-F. However, you must balance this decision with the power and area requirements of your CI-700 instance.

HN-I devices are the HNs for all memory that targets an ACE-Lite slave device or subsystem. HN-Is do not support coherent memory. However, cacheable transactions can be sent to HN-I.

Each HN-I instance contains a single ACE-Lite master port to send bus transactions to one or more slaves through an AMBA® interconnect. The total ACE-Lite master bandwidth requirement and the physical placement of slave peripherals determines the number of HN-I instances that are required.

CI-700 also has the following variants of HN-I that have extra functionality:

HN-T HN-I that has a DTC
CI-700 can have zero or more HN-I and HN-T instances

HN-D HN-I that has a DTC, DVM node, and configuration slave
CI-700 must have exactly one HN-D instance

Whether you use a standard HN-I or one of the variants depends on the requirements of your system. The exception to this choice is the HN-D. There must be exactly one HN-D in any CI-700 instance.

Memory controllers

CI-700 has various types of memory interfaces for connecting different kinds of memory controllers to.

Native CHI memory controllers, such as the CoreLink™ DMC-620 Dynamic Memory Controller, are referred to as SN-Fs. SN-Fs connect directly to CI-700 through SN-F ports. CI-700 supports SN-Fs that comply with the following protocols:

- CHI Issue C
- CHI Issue D
- CHI Issue E

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You can also connect AXI or ACE-Lite memory controllers to CI-700 through an ACE-Lite memory interface on one of the following node types:

SBSX

SBSXs bridge between CHI and ACE-Lite protocols. Each SBSX has a single ACE-Lite interface.

MTSX

MTSXs also bridge between CHI and ACE-Lite protocols, and each MTSX has a single ACE-Lite interface. However, MTSXs are only instantiated when the system requires MTE support but the slave AXI or ACE-Lite memory controller does not support MTE.

The number and type of memory interfaces that you require depends on the design of your system.

Related information

- 2.5 Device-level configuration parameters on page 21

3.7 Deciding on the size of the mesh

The number of XPs and their arrangement determines the size of the mesh. The number of XPs that you require depends on the number of devices in your configuration. There are also constraints on how the XPs can be arranged.

By default, you require one XP for every two devices in your configuration. Therefore the number of XPs that you require in your configuration is half of the number of devices, rounded up. Depending on your configuration you can expand the number of device ports on an XP. For more information, see 3.10 Support for extra device ports on MXPs on page 50

The mesh must be rectangular, so you might require more than the minimum number of XPs to complete the mesh. For example, consider a default configuration with 13 devices, which requires a minimum of seven XPs. In this case, to ensure that the mesh is rectangular, the configuration must contain 8 XPs. The XPs in this example could be arranged in a 2×4 or 4×2 mesh.

Related information

- 3.8 Permitted numbers of devices and system resources in the mesh on page 47
- 3.9 Configurable options for mesh structure on page 49

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3.8 Permitted numbers of devices and system resources in the mesh

CI-700 has constraints on the amount of some system resources and the number of each device type that you can use in the configuration.

The following table shows the permitted amounts of system resources and numbers of devices in CI-700.

Table 3-5: Amount of system resources and number of devices

Category	Resource	Description	Values (default)	Comments
Processor resources	Number of RN-Fs	The number of RN-Fs in the system. RN-Fs can be one of the following types: • RNF_CHIB_ESAM • RNF_CHIC_ESAM • RNF_CHID_ESAM • RNF_CHIE_ESAM	1-8 without CAL 2-8 with CAL	For single-MXP configurations, RN-F devices must not be on device port P4 or P5.
I/O resources	Number of RN-Is	The number of RN-I instances in the system	0-8	At least one RN-I or RN-D must be present. The total number of RN-Is and RN-Ds must not exceed eight. CI-700 supports connection of RN-I and RN-D nodes to CAL. If connecting RN-I or RN-D nodes to a CAL, those nodes can only have a single A4S port. **Note:** There must not be any RN-I nodes in a configuration that uses DSA-F mode.
	Number of RN-Ds	The number of RN-D instances in the system	0-8	
	Number of HN-Is	The number of HN-I instances in the system. This count also includes any HN-Ts and the HN-D which is always present.	0-4 without CAL 2-4 with CAL	CI-700 supports connection of HN-I to CAL.

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Category	Resource	Description	Values (default)	Comments
Debug resources	Number of DTCs	The total number of DTC domains.	1-4	The following constraints apply to debug resources: • The number of DTC domains must not exceed the number of HN-D and HN-T nodes. • For single-MXP configurations, only one DTC domain is supported. • HN-D can be on any device port in a single-MXP configuration. • If the following conditions are true, then HN-D must be on device port P2: ◦ The CI-700 system contains more than one MXP. ◦ The MXP that the HN-D is attached to has more than two device ports.
System cache	Number of HN-Fs	The total number of HN-F instances in the system. The number of HN-Fs referred to by a given cache group (hashed entry in the SAM) must be a power of two.	0-8 without CAL 2-8 with CAL	For more details, refer to 6 SLC memory system on page 1296. **Note:** There must not be any HN-F nodes in a configuration that uses DSA-F mode.
Memory resources	Number of SN-Fs	The number of SN-Fs (CHI interfaces)	0-8	At least one SN-F, SBSX, or MTSX must be present. The total count of SN-Fs, SBSXs, and MTSXs must not exceed eight. CI-700 supports connection of SBSXs and MTSXs to CAL. When CAL is present, the number of SBSXs and MTSXs must be even.
	Number of SBSXs	The number of SBSX instances (AXI interfaces)	0-8	
	Number of MTSXs	The number of MTSX instances (AXI interfaces without memory tagging support)	0-8	

3.9 Configurable options for mesh structure

These configurable options define the dimensions of the mesh and the number of different types of CSs across different links. Each value has a specific range and there are some constraints that apply to these values.

The following table shows the configurable options for mesh structure.

Table 3-6: Mesh structure configurable options

Parameter	Description	Values	Comments
Mesh X dimension	Number of mesh columns	1-8	The following constraints apply to the mesh dimensions: • Mesh supports a maximum of 12 XPs. • Mesh supports a maximum X dimension of eight XPs. • Mesh supports a maximum Y dimension of eight XPs.
Mesh Y dimension	Number of mesh rows	1-8	

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Parameter	Description	Values	Comments
MCSX count	Number of credited slices on an XP-XP mesh link in X dimension	0-4	This count is per link and can be different for each link.
MCSY count	Number of credited slices on an XP-XP mesh link in Y dimension	0-4	
DCS count	Number of credited slices on a device-XP link	0-4	
CCS count	Number of credited slices on a CAL-XP link	0-2	

3.10 Support for extra device ports on MXPs

You can expand the number of device ports on an MXP beyond the default number of two. This feature reduces the power consumption of CI-700 configurations by reducing mesh transfer activity between MXPs.

By default, a single MXP has two device ports and four mesh ports. CI-700 also supports extra device ports on MXPs. The maximum permitted number of device ports per MXP is configuration-dependent. For example, a single-MXP configuration is possible where there are up to six device ports on the MXP.

Enabling extra device ports affects the following aspects of CI-700:

- The overall system topology. For more information, see 3.11 Topology considerations when using extra device ports on page 50.
- The number and mapping of DTMs in the MXP. For more information, see 7.1.1 DTM changes when using extra device ports on page 1322.
- The mapping scheme for node IDs. For more information, see 4.3.2 Node ID mapping for configurations with extra device ports on page 77.

3.11 Topology considerations when using extra device ports

The number of devices in your CI-700 design determines the number of MXPs and device ports that you require. The design is also affected by whether you choose to put a CAL on any of the device ports.

If you have more than 6-8 devices in your CI-700 configuration, you must use a mesh configuration with multiple MXPs.

The following figure shows an example mesh configuration using extra device ports.

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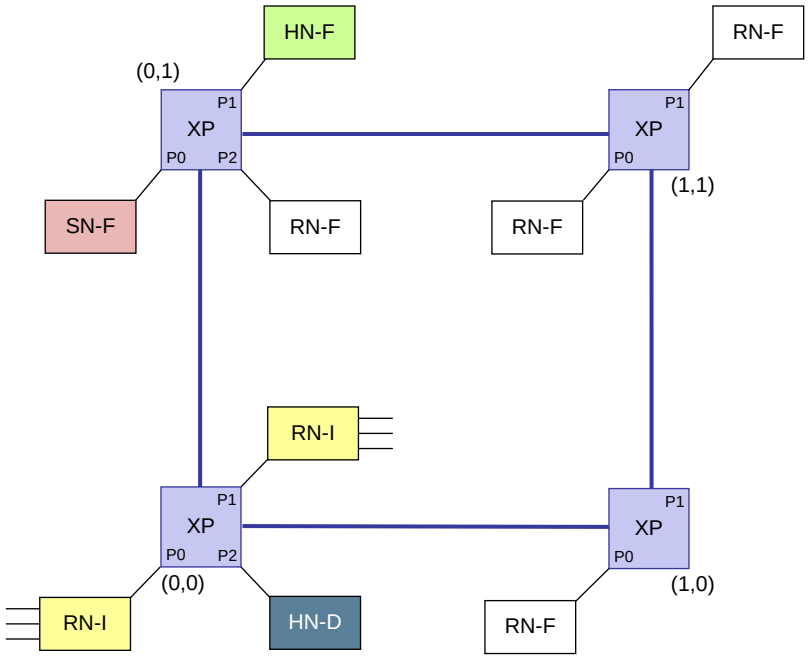
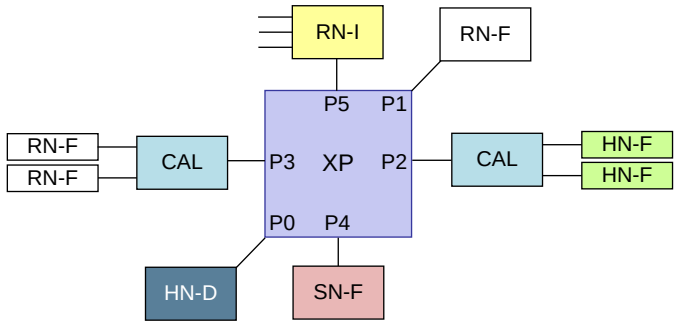
Figure 3-10: Mesh configuration using extra device ports



If you have six or fewer devices in your configuration, or eight or fewer if you are using CAL, you can use a single-MXP configuration. All devices can then be attached to one MXP, as the following figure shows.

Figure 3-11: Single-MXP configuration with extra device ports



The following table shows the MXP design restrictions depending on whether you use a single-MXP or multiple-MXP configuration.

Table 3-7: MXP design restrictions when using extra device ports

MXP configuration type	Maximum number of device ports per MXP	Maximum number of devices per MXP	Maximum number of supported ESAMs per MXP
Single MXP	6	8	4

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MXP configuration type	Maximum number of device ports per MXP	Maximum number of devices per MXP	Maximum number of supported ESAMs per MXP
MXP in mesh configuration without HN-D or HN-T connected	4	8	4
MXP in mesh configuration with HN-D or HN-T connected	3	5, including HN-D or HN-T	4

A mesh configuration is a configuration with more than one MXP, which means, not a single-MXP configuration. If the MXP in a mesh configuration has more than two device ports, HN-D or HN-T is only permitted on device port P2.

You can attach only a maximum of four RN-Fs to an MXP directly. This restriction is because of the maximum supported number of ESAMs per MXP, which is four for all configuration types. To increase the number of RN-Fs on an MXP, you must use a CAL.

3.12 Example system configurations

Because CI-700 is highly configurable, different system configurations can vary significantly. These examples show possible small, medium, and large configurations, with varying node types and system components.

The following figure shows a small 1 × 3 mesh configuration with single instances of the following node types:

- RN-F
- HN-F
- RN-D
- SN-F
- HN-D

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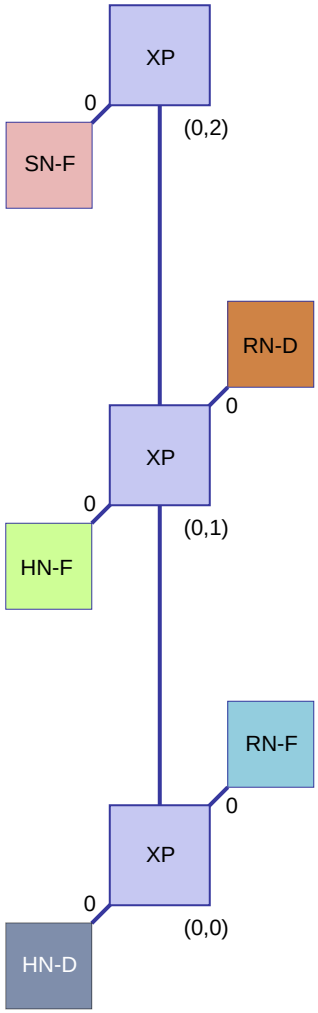
Figure 3-12: Example 1 × 3 mesh configuration



The following figure shows a medium 2 × 2 mesh configuration with single and multiple instances of the node types in the preceding figure.

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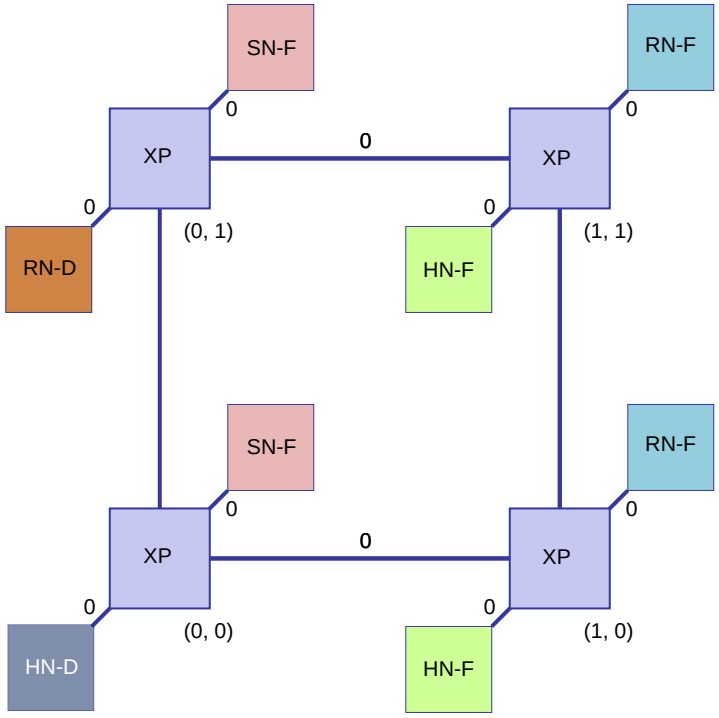
Figure 3-13: Example 2 × 2 mesh configuration



The following figure shows a large 3 × 4 mesh configuration with multiple instances of the same node types as the other examples.

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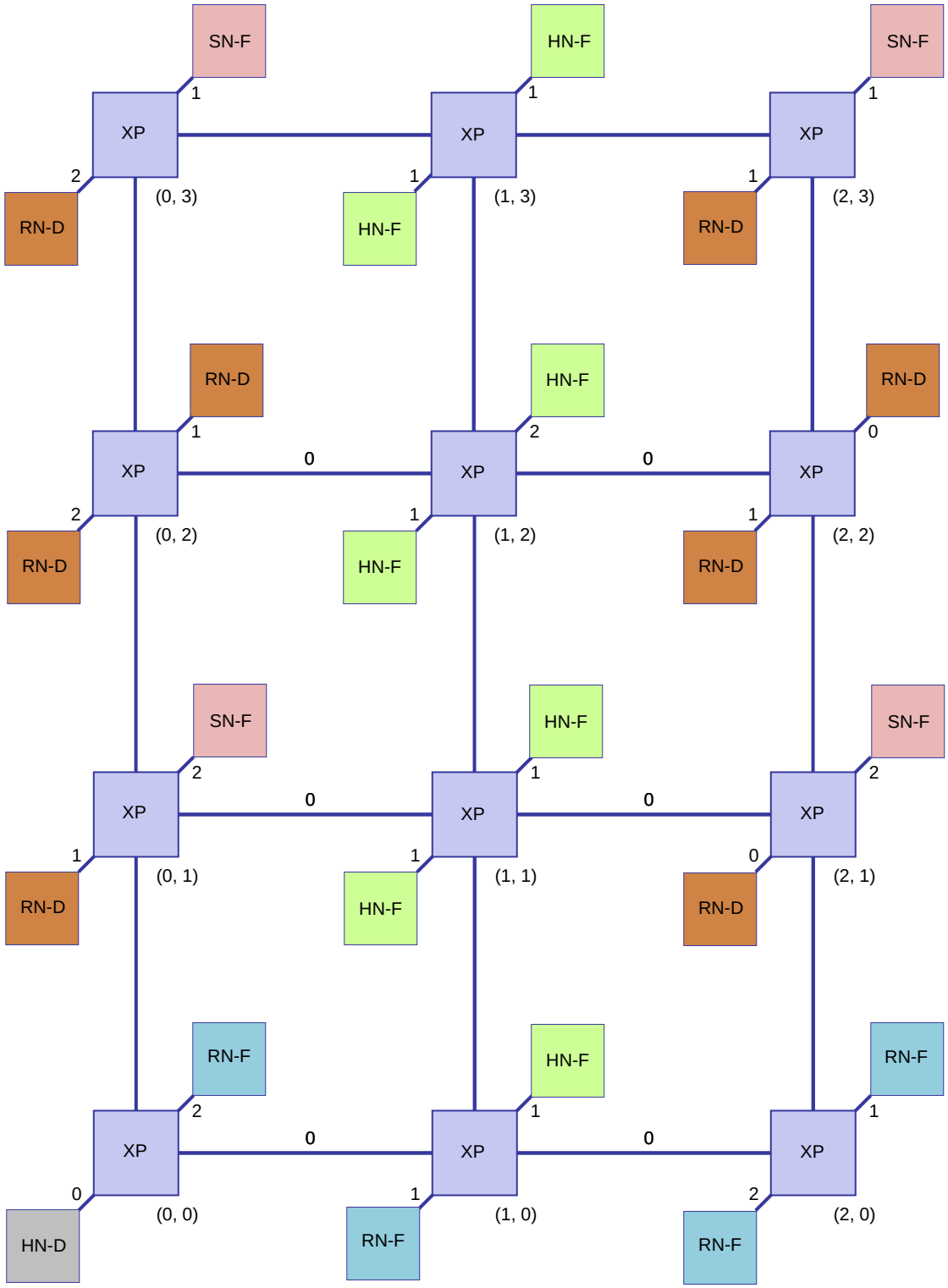
Figure 3-14: Example 3 × 4 mesh configuration



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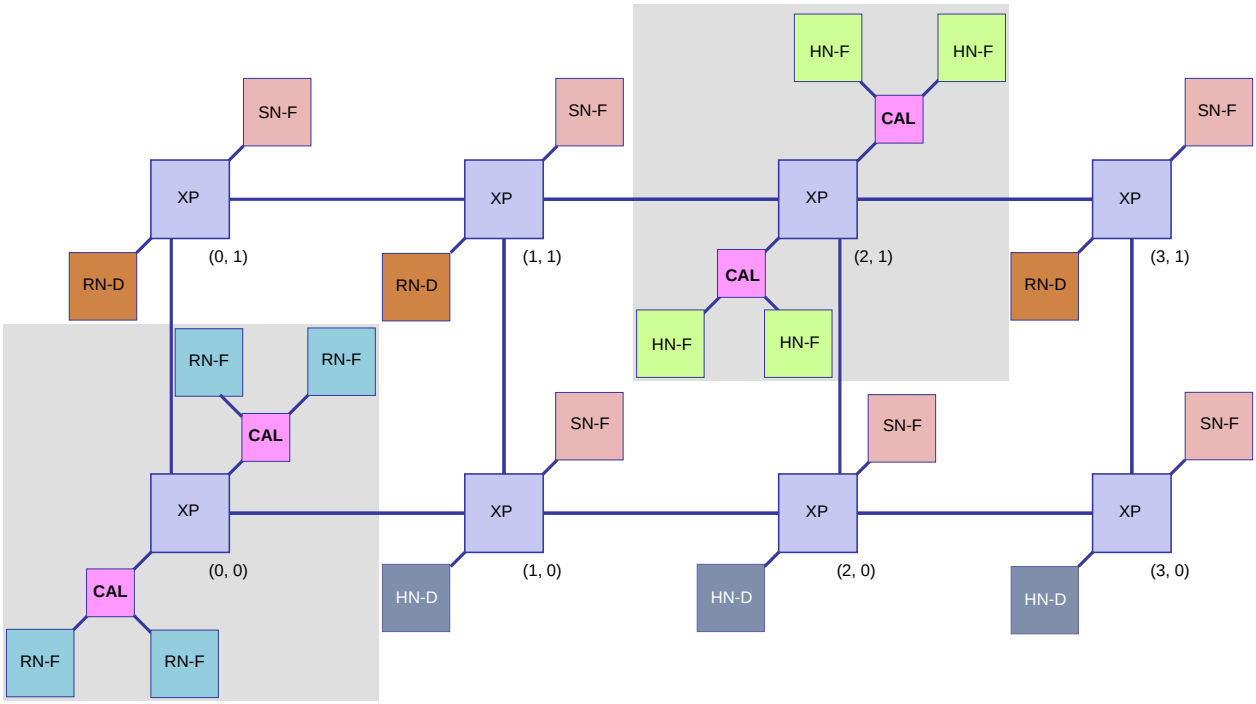
The following figure shows a medium 4 × 2 mesh configuration with RN-F and HN-F CAL, that the gray areas show.

Figure 3-15: Example 4 × 2 mesh configuration with CAL



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4 Functional description

This chapter describes functionality achieved when you design and configure the CI-700 interconnect and its components.

4.1 Clocks and resets

CI-700 provides a hierarchical clocking microarchitecture which enables dynamic clock management for power efficiency. It also has a global reset signal.

CI-700 has a *High-level Clock Gating* (HCG) mechanism for clock signal management during periods of inactivity. See 4.1.4 High-level Clock Gating on page 60.

4.1.1 Clock domains

CI-700 has a single, fully synchronous clock domain. This clock domain is supplied by a single global clock signal, **GCLK0**.

The following figure shows an example mesh topology and the boundaries of the CI-700 clock domain.

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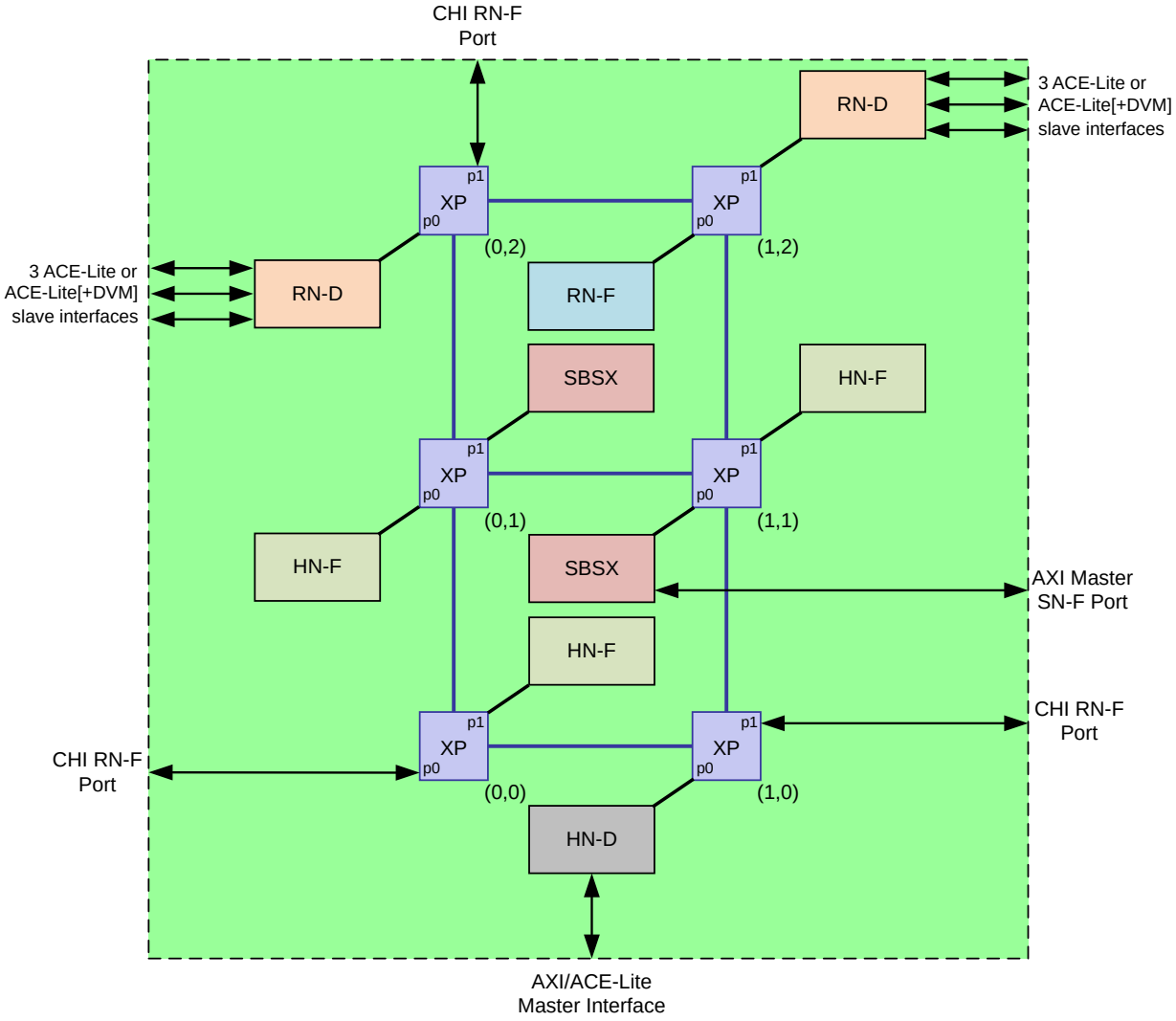
Figure 4-1: CI-700 fully synchronous clock domain



4.1.2 Clock hierarchy

The clocking delivery and clock gating architecture are hierarchical.

Within the clock gating hierarchy, the following levels of clocks are defined:

Global clock The global clock is the clock input to the CI-700 system. Another level of clock gating or clock control outside of the system is likely to control the global clock that is provided by the SoC. Although it is not a system requirement, CI-700 includes support for external clock control.

Regional clocks Regional clocks are created as an output of regional clock gaters that include a coarse enable for coarse-grained clock gating under idle or mostly idle conditions. Regional clock gaters can shut down the clock network between

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regional and local gaters. Therefore, this level of hierarchy enables greater power reduction than is possible using local clock gating. The regional clock gaters are instantiated in and controlled by the CI-700 RTL. The exact set of regional clocks is internal to CI-700 and is not described in this manual.

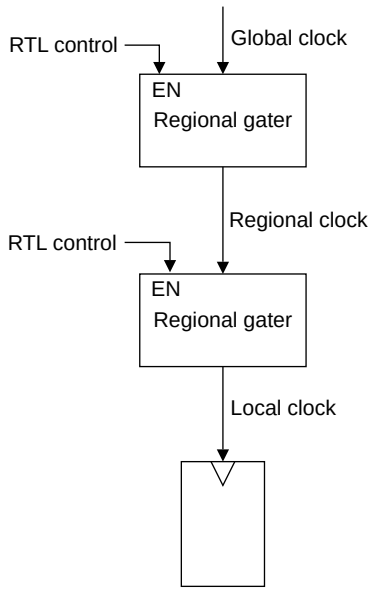
Local clocks Local clocks are created according to the following hierarchy:

1. RTL creates fine-grained enable signals.
2. Fine-grained enable signals control local clock gaters.
3. Local clock gaters output local clock signals.

   Local clock signals are used to directly clock sequential elements in CI-700. The exact set of local clocks is internal to CI-700 and is not described in this manual.

The following figure shows the clocking hierarchy.

Figure 4-2: Clocking hierarchy



4.1.3 Clock enable inputs

CI-700 includes several clock enable inputs, enabling synchronous communication with slower SoC logic.

The clock enable input signals are:

ACLKEN_S Present on each AMBA® slave interface.
ACLKEN_M Present on each AMBA® master interface.

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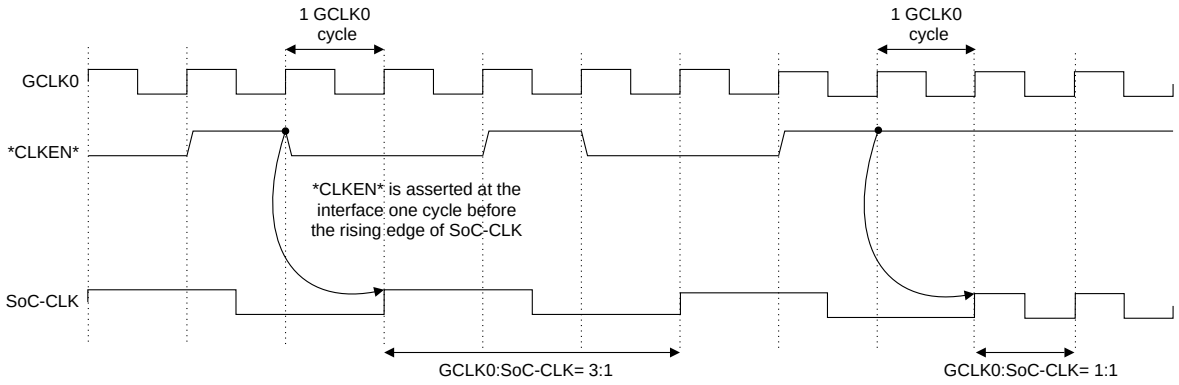
ATCLKEN Present on each debug and trace ATB interface.

All clock enable signals, shown here as ***CLKEN***, have identical functionality: they enable their respective interface to run at integer fractions of **GCLK0**. In other words, the clock enable signals run slower than **GCLK0**. **ACLKEN_S** and **ACLKEN_M** can run at any integer ratio from 1:1 to 4:1 of the frequency of **GCLK0**. **ATCLKEN** is limited to 1:1, 2:1, and 4:1 integer ratios.

CLKEN asserts one **GCLK0** cycle before the rising edge of the SoC clock, **SoC-CLK**. SoC control logic can change the ratio of **GCLK0** frequency to **SoC-CLK**, frequency dynamically using ***CLKEN***.

The following figure shows a timing example of a ***CLKEN*** ratio change. In the example, ***CLKEN*** changes the ratio of the relevant interface frequency respective to **GCLK0** from 3:1 to 1:1.

Figure 4-3: *CLKEN* with GCLK0:SoC-CLK ratio changing from 3:1 to 1:1



4.1.4 High-level Clock Gating

The PCCB supports a *High-level Clock Gating* (HCG) mechanism. This mechanism notifies the SoC when CI-700 is inactive and therefore reduces dynamic power consumption.

HCG enables an external SoC clock control unit, the *External Clock Controller* (ExtCC), to stop the **GCLK0** clock inputs. See 4.1.5 External Clock Controller on page 60.

CI-700 includes a Q-Channel interface that enables CI-700 and the SoC to communicate to achieve HCG functionality through the PCCB. See the *AMBA® Low Power Interface Specification Arm® Q-Channel and P-Channel Interfaces*.

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4.1.5 External Clock Controller

The *External Clock Controller* (ExtCC) is used to control the HCG flow.

The following figure shows an example of how the ExtCC controls the clock gating flow. This example clock gating sequence begins and ends with the Q-Channel in either of the following states:

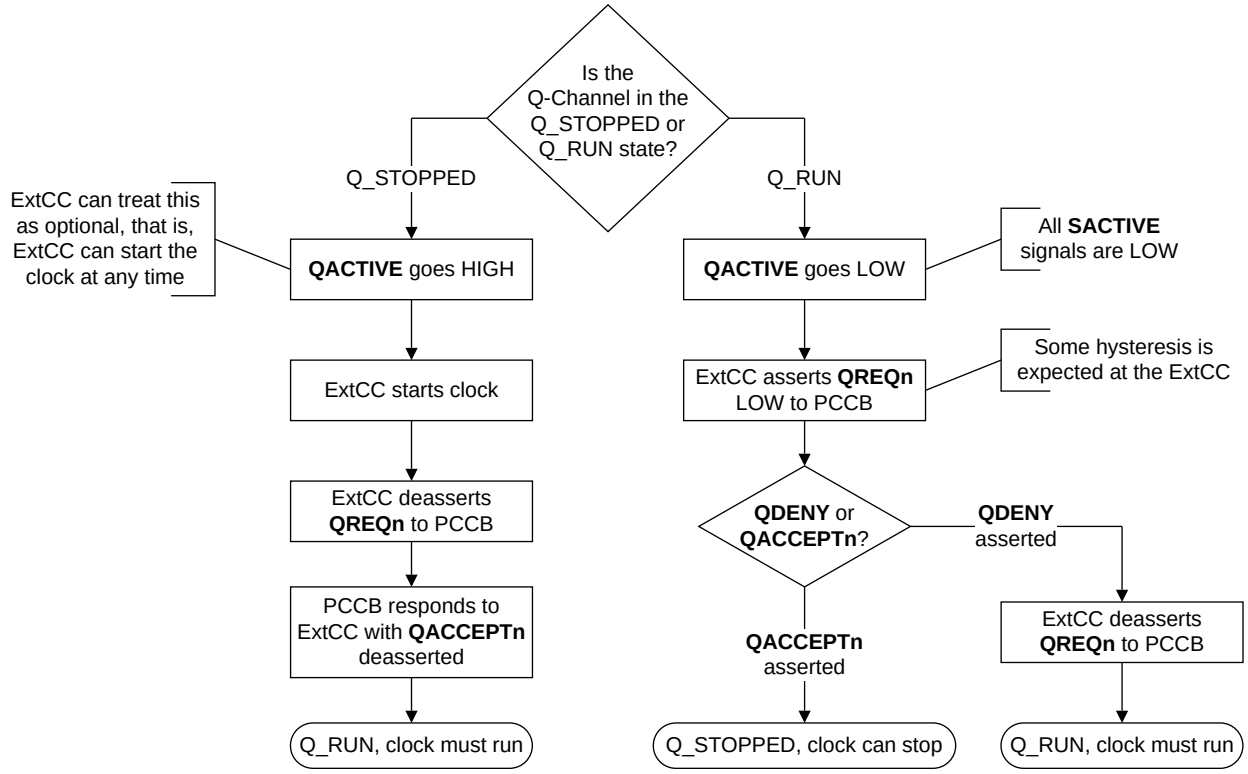
Q_STOPPED

Quiescent state, where **QREQn** and **QACCEPTn** are asserted.

Q_RUN

Active state, where **QREQn** and **QACCEPTn** are deasserted.

Figure 4-4: Clock gating control using ExtCC



The requirements of the ExtCC are as follows:

- It must supply a clock to CI-700 when the Q-Channel is in any state other than Q_STOPPED.
- The ExtCC can either:
  - Choose to gate the clock to CI-700 when the Q-Channel is in the Q_STOPPED state.
  - Choose to run the clock at any time.
- ExtCC is responsible for bringing the Q-Channel to Q_RUN state after reset deassertion.
- This manual does not describe the exact behavior of the ExtCC and its usage of **QREQn** in response to **QACTIVE** deassertion. However, the design of the ExtCC is likely to include a

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control loop with some hysteresis. Therefore HCG is enabled when the system is inactive for long periods, but is not enabled for short periods of inactivity. If the clocks are stopped in response to short periods of inactivity, performance of CI-700 can be negatively affected.

- It is the responsibility of the SoC designer to fully control the clock management Q-Channel. If you require a control or configuration bit to completely enable or disable HCG functionality, it must exist outside of CI-700. CI-700 has no internal means of disabling HCG.

4.1.6 Reset

CI-700 has a single global reset input signal, **nSRESET**.

nSRESET is an active-LOW signal that can be asynchronously or synchronously asserted and deasserted. All paths from reset synchronizers are required to meet single cycle timing.

When asserted, **nSRESET** must remain asserted for 72 clock cycles. Likewise, when deasserted, **nSRESET** must remain deasserted for 72 clock cycles. This requirement ensures that all internal CI-700 components enter and exit their reset states correctly.

All CI-700 clock inputs must be active during the required 72-cycle, or larger, period of **nSRESET** assertion. The clock inputs must also remain active for at least 72 cycles following deassertion of **nSRESET**.

4.2 Power management

CI-700 includes several power-management capabilities, that are either externally controllable or that the SoC assists.

CI-700 has the following power management capabilities:

- Several distinct predefined power states. These states include ones in which all, half, or none of the SLC tag and data RAMs can be powered up, powered down, or in retention:
  - A state in which only the HN-F SF is active
  - A state in which the SLC RAMs and SF RAMs are inactive

  These power states reduce static and dynamic power consumption.
- Support for static retention in HN-F in which the SoC places SLC and SF RAMs in a retention state. This capability reduces static power consumption.
- Support for in-pipeline low-latency data RAM retention control, in which a programmable idle counter can be used to put the SLC RAMs in retention.


Note

The clocking hierarchy and clock gating mechanism are described elsewhere. For more information, see 4.1 Clocks and resets on page 57.

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4.2.1 Power domains

The power domains in CI-700 are divided into logic domains and domains for the RAMs in the HN-F partitions.

CI-700 has the following power domains:

Logic

All logic except HN-F SLC tag and data RAMs and HN-F SF RAMs.

SLC RAM0

SLC tag and data RAMs, way[7:0] within HN-F partitions. The RAMs in each HN-F partition can be independently controlled.

SLC RAM1

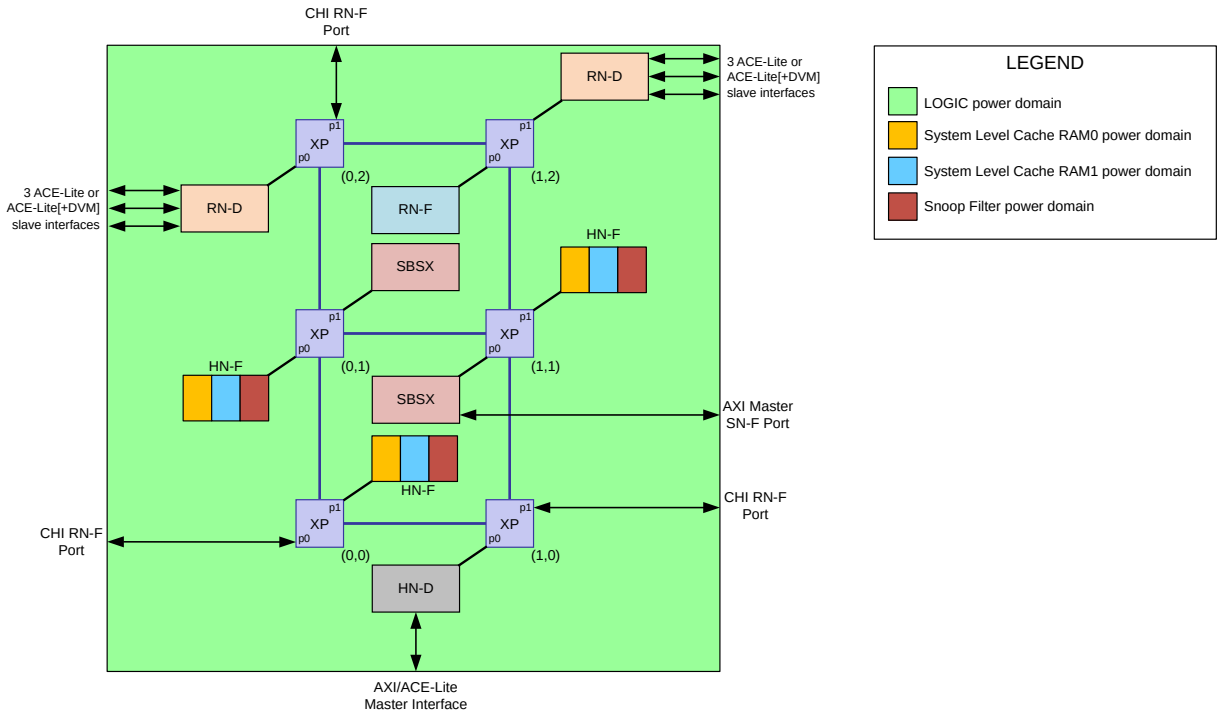
SLC tag and data RAMs, way[15:8] within HN-F partitions. The RAMs in each HN-F partition can be independently controlled. For 3MB SLC size configurations, the RAM1 domain includes way[11:8].

Snoop filter only mode

SF RAMs within HN-F partitions. The RAMs in each HN-F partition can be independently controlled.

The following figure shows an example power domain configuration.

Figure 4-5: CI-700 power domain example



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Note

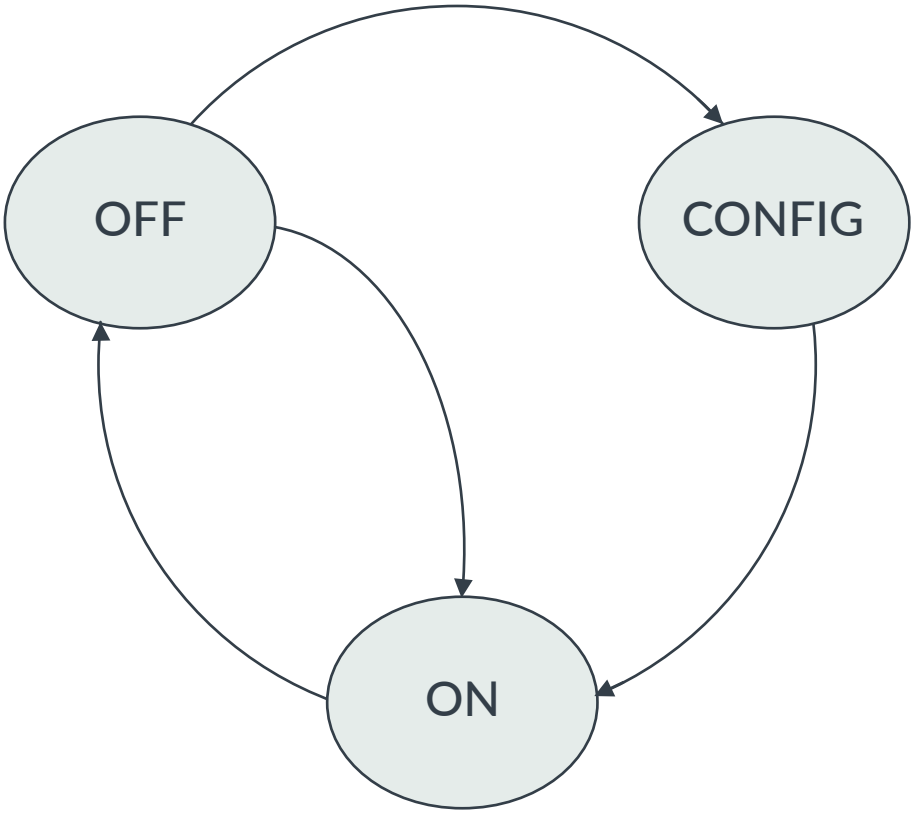
MTU RAMs within MTSX are in the logic domain and cannot be independently controlled.

4.2.2 Power domain control

The CI-700 logic P-Channel controls all power domains except for the RAM power domains.

In addition to controlling the logic domain, the logic P-Channel allows synchronization between the HN-F software-controlled power domains and the logic domain. This synchronization is achieved through a CONFIG state, as the following figure shows.

Figure 4-6: Logic domain states



There are two paths for transitioning from the OFF to ON state:

Cold reset

The logic **PSTATE** OFF to ON transition also initiates NOSFSLC to FAM transition for all HN-F partitions.

Exit from HN-F static retention state

The logic **PSTATE** transitions from OFF to CONFIG, indicating that CI-700 is exiting a memory retention state. The transition does not initiate any HN-F partition power transitions.

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The following table contains the power modes of components within the domain and the associated **PSTATE** values.

Table 4-1: Power mode configurations and PSTATE values

Power mode	PSTATE	CI-700 logic	HN-F
OFF	0b00000	OFF	OFF/MEM_RET
CONFIG	0b11000	ON	ANY
ON	0b01000	ON	ANY

Note

The CI-700 P-Channel interface requires clocks when either **QACTIVE_ICN** or **QACTIVE_DEV** are asserted to function properly, including **PACTIVE**.

For an introduction to HN-F states, see 4.2.5 HN-F power domains on page 66.

For P-Channel signal information, see B.9 Power management signals on page 1400.

4.2.3 P-Channel on device reset

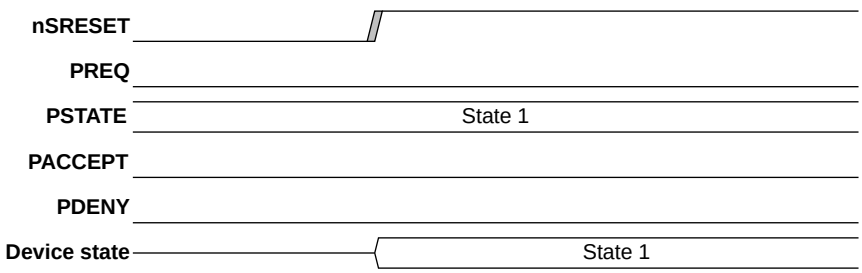
This section shows how to initialize the power state of a power domain.

Certain device power states might power down the control logic. When powering this control logic back on, the power controller must indicate the state that the device must power up. The device detects the required state by sampling **PSTATE** when **nSRESET** deasserts. The **PSTATE** inputs must be asserted before the deassertion of reset and remain after the deassertion of **nSRESET**, to allow reset propagation within CI-700. The power controller must ensure that the reset sequence is complete before transitioning **PSTATE**, otherwise the device might sample an undetermined value. The following figure shows the state initialization on reset.

Note

PSTATE inputs must be static 100 cycles before deassertion of **nSRESET**, and also for 100 cycles after the deassertion of **nSRESET**.

Figure 4-7: Reset state initialization



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For an introduction to HN-F states, see 4.2.5 HN-F power domains on page 66.

4.2.4 HN-F Memory retention mode

When isolating the CI-700 outputs, handshake protocols on certain interfaces must be followed. This section describes the steps to take to enter and exit HN-F Memory retention mode.

Entering HN-F Memory retention mode

1. Program the HN-Fs to enter the required power state
2. Quiesce the interconnect, and wait for **QACTIVE** to drop
3. Place CI-700 in the LOGIC_OFF state through the logic P-Channel
4. Isolate the CI-700 outputs. If the logic on the other side of the interface is being powered down or reset, this step might not be required.
5. Turn off power to CI-700

Exiting HN-F Memory retention mode

1. Apply power to CI-700
2. Assert reset
3. Enable clocks
4. Disable isolation of the CI-700 outputs
5. Deassert reset
6. Place CI-700 in LOGIC_CONFIG state through the logic P-Channel
7. Reprogram the por_hnf_ppu_pwpr register to the retention mode the HN-F was in before turning off power
8. Reprogram the por_hnf_ppu_pwpr register to ON
9. Reprogram the CI-700 configuration registers, including the RN SAM and any other registers that are written during cold boot
10. Place CI-700 in the LOGIC_ON state through the P-Channel
11. Resume traffic and normal operation

4.2.5 HN-F power domains

The HN-F has various power states. Transitioning between different states enables or disables different parts of the HN-F.

The HN-F has the following classes of power states:

1. Operational states, where logic is on and enabled RAMs are operating as normal
2. Functional retention states, where logic is on, and enabled RAMs are in retention
3. Memory retention states, where logic is off and enabled RAMs are in retention

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Within these power states, the HN-Fs in an SCG operate in four modes:

***Full Associativity Mode* (FAM)**

The SF and the entire SLC are enabled.

***Half Associativity Mode* (HAM)**

The SF is enabled but the upper half of the SLC ways are disabled and powered off.

***Snoop Filter Only Mode* (SFONLY)**

The SF is enabled but the whole SLC is powered off.

***No SLC Mode* (NOSFSLC)**

The SF and SLC are disabled and powered off.

The following constraints apply to the power states and transitions:

- If SLC size is 0KB, the HN-F does not support transitions to FAM or HAM modes.
- After initialization, the power status register indicates FAM instead of SFONLY for 0KB SLC configurations.
- When a power transition is initiated, another must not be initiated until the first one completes.

The following table shows the valid HN-F power states and their requirements.

Table 4-2: HN-F power states

State	Description	Control logic	SF power state	SLC way[7:0] power state	SLC way[15:8] power state
FAM	Full Run mode	On	On	On	On
HAM	Run mode with SLCH2 (SLC upper ways) disabled.	On	On	On	Off
SF	Run mode with SLCH1 and SLCH2 disabled.	On	On	Off	Off
NOSFSLC	Run mode with SLCH1, SLCH2, and SF disabled.	On	Off	Off	Off
FAM FUNC_RET	Run mode with SLCH1, SLCH2, and SF in dynamic retention.	On	Retention	Retention	Retention
HAM FUNC_RET	Run mode with SLCH1 and SF in retention, and SLCH2 in power down.	On	Retention	Retention	Off
SF FUNC_RET	Run mode with SF in retention, and SLCH1 and SLCH2 in power down.	On	Retention	Off	Off
FAM MEM_RET	Shut down with SLCH1, SLCH2, and SF in retention	Off	Retention	Retention	Retention
HAM MEM_RET	Shut down with SLCH1 and SF in retention, and SLCH2 in power down	Off	Retention	Retention	Off
SF MEM_RET	Shut down with SF in retention, and SLCH1 and SLCH2 in power down	Off	Retention	Off	Off
OFF	Shutdown	Off	Off	Off	Off

The following figure shows the valid power states and transitions for a CI-700 system.

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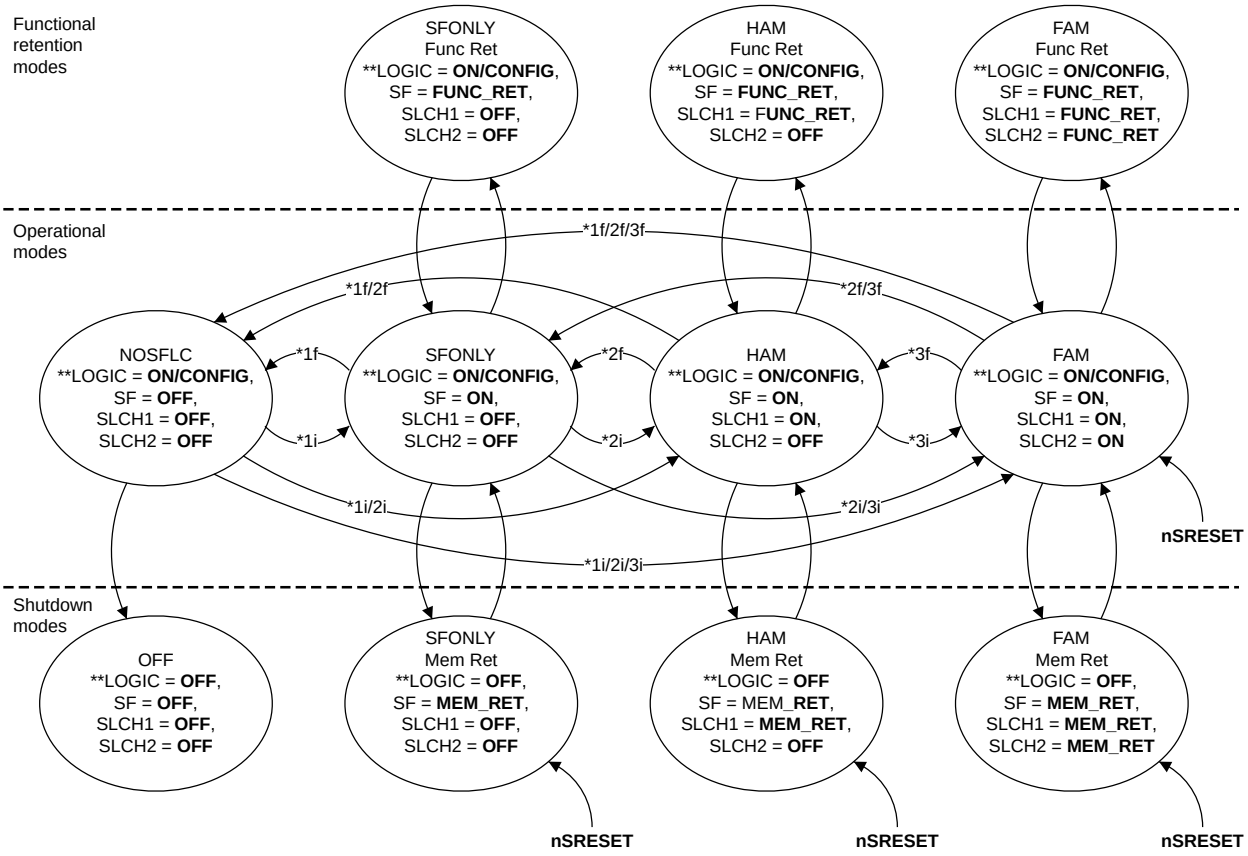
Figure 4-8: Power state transitions



Note: **BOLD** text shows the required power state.

* Automatic initialization and flushing actions:
1i: Initialize snoop filter RAMs.
2i: Initialize lower ways of tag RAMs.
3i: Initialize upper ways of tag RAMs.
1f: Flush (force back-invalidations as necessary and invalidate) snoop filter RAMs.
2f: Flush (clean/invalidate) lower ways of tag/data RAMs.
3f: Flush (clean/invalidate) upper ways of tag/data RAMs.

** All designations refer to P-state values required to enter the respective state.

The SF does not track RN-F coherence while the HN-F is in NOSFSLC state. Therefore, the RN-F caches must be flushed before transitioning from NOSFSLC to SFONLY, HAM, or FAM states.

These HN-F power states are transitioned using configuration register writes that must target all HN-Fs in the SCG region. Also, the logic domain P-Channel interface can initiate a NOSFSLC→FAM transition.

To transition HN-F partitions to a required power state, write to the following por_hnf_ppu_pwpr register fields:

- policy
- op_mode

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When the power state transition is complete, the following por_hnf_ppu_pwsr register fields are updated:

- pow_status
- op_mode_status

If either the SLC, the SF, or both are flushed as part of a power transition, then the power state transition can take many thousands of clock cycles. Also, the **INTREQPPU** interrupt output can be used to indicate the completion of the HN-F power state transitions.

From the FAM, HAM, or SFONLY modes, the HN-F can enter a dynamic retention mode using configuration register writes, where:

- The logic power is on
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bitcell retention but insufficient for normal operation
- The array pipeline is blocked, and a handshake occurs to allow array access when exiting the retention state

These dynamic power transitions are executed autonomously within each HN-F partition. Each HN-F has a programmable idle cycle counter and initiates a P-Channel handshake with the corresponding RAMs to enter the dynamic retention state. The pipeline then blocks transactions that target the HN-F RAMs. A coherent transaction triggers an exit from the dynamic retention state, initiates another P-Channel handshake, and takes the RAMs out of dynamic retention mode.

From these states, the SLC can also enter a Memory retention mode, where:

- The logic power is turned off
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bitcell retention but insufficient for normal operation
- Reset deassertion is essential when exiting retention after logic power down

A P-Channel interface controls the CI-700 logic domain power state. This P-Channel interface also interacts with the HN-F power control logic using an internal bus. The HN-F power control logic waits for a command on the deassertion of **nSRESET**, depending on the overall power state transition that is required. For the Cold reset HN-F FAM transition case, the PCCB block initiates the HN-F NOSFSLC→FAM command. To exit static retention cases, the SCP initiates configuration register writes to the HN-F to indicate the HN-F power state.

The circumstances in which the HN-F enters dynamic retention modes or static retention modes are different. Dynamic retention is entered because of a dynamic activity or inactivity indicator from the HN-F to the SoC. This indicator is an output of the HN-F, and is used to determine periods of inactivity long enough to warrant entering retention mode. However the inactivity is either not long enough or not the type of inactivity to make the SoC place the SLC and SF into static retention. In addition to the static retention modes, the control logic can be powered down from the NOSFSLC state, at which point CI-700 is fully off.

The HN-Fs automatically perform all activity that is required to enable safe transition between the respective power states in response to input P-Channel **PSTATE** transitions. It is not necessary

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for the SoC logic to perform any extra activity to enable transitions between power states. For example, the HN-F performs clean and invalidation of half of the ways of the SLC and clean and invalidation of all ways of the SLC. This clean and invalidation activity occurs as required by the respective power state transitions.


Note

CI-700 cannot make any power transitions while the control logic is powered off. Consider a transition from FAM static retention to OFF. To complete this transition, the power state must first move through FAM and NOSFSLC states while the LOGIC power domain is on. These transitions allow the SLC and SF to be flushed.

The following table shows the **PSTATE** encodings for the HN-F and power domains including RAM configurations for the different operational modes.


Note

HN-F cannot process any transactions while in static retention (FUNC_RET or MEM_RET). HN-F must be in the ON state before sending any transactions to HN-F in this case. If HN-F is in dynamic retention, any activity autonomously takes HN-F out of dynamic retention.

Table 4-3: Power modes, operational modes, and RAM configurations

Operational mode	Power mode	PSTATE	Bank 0 RAM	Bank 1 RAM	SF RAM
FAM	ON	11_1000	ON	ON	ON
	FUNC_RET	11_0111	RET	RET	RET
	MEM_RET	11_0010	RET	RET	RET
HAM	ON	10_1000	ON	OFF	ON
	FUNC_RET	10_0111	RET	OFF	RET
	MEM_RET	10_0010	RET	OFF	RET
SFONLY	ON	01_1000	OFF	OFF	ON
	FUNC_RET	01_0111	OFF	OFF	RET
	MEM_RET	01_0010	OFF	OFF	RET
NOSFSLC	MEM_OFF	00_0110	OFF	OFF	OFF
	OFF	00_0000	OFF	OFF	OFF

4.2.6 HN-F RAM Power Control State Machine interface

Each HN-F RAM interface contains a *Power Control State Machine* (PCSM).

The following items depend on the completion of all P-Channel transactions:

- Each PCSM P-Channel interface that can be used to convert power state transitions into technology-specific controls
- The overall HN-F partition power state transition

The following table lists the valid **PSTATE** values for this interface.

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Table 4-4: PSTATE Encodings

PSTATE	Value
ON	0b1000
FUNC_RET	0b0111
MEM_RET	0b0010
OFF	0b0000


Note

This interface does not have a **PDENY** signal.

4.2.7 HN-F power domain completion interrupt

The PCCB can be configured to generate an **INTREQPPU** interrupt on completion of power state transitions for a collection of HN-Fs.

The PCCB contains a global status register, por_ppu_int_status, which indicates HN-F power state transition completion. The PCCB also contains a mask register, por_ppu_int_mask, which allows filtering on all or a subset of the HN-Fs in the CI-700 configuration. The bit positions in the por_ppu_int_status and por_ppu_int_mask registers correspond to the logical ID of the HN-Fs.

INTREQPPU asserts when the HN-F power transition completion sets all por_ppu_int_status register bits and the corresponding por_ppu_int_mask register bit.

To deassert **INTREQPPU**, write 1 to the bits of the por_ppu_int_status register that correspond to the masked group of HN-Fs that completed the power transitions.

4.2.8 RN entry to and exit from snoop and DVM domains

CI-700 includes a feature that allows RNs to be included or excluded from the system coherency domain. This domain is also known as the snoop domain or DVM domain.

This feature ensures correct operations of snoops and DVMs when:

- An RN is taken out of reset
- An RN is powered down and then later powered up

RN-Fs behave as follows:

- If an RN-F is included in the system coherency domain, it must respond to snoop and DVM requests from CI-700
- If an RN-F is excluded from the system coherency domain, it does not receive snoop or DVM requests from CI-700

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RN-Ds behave as follows:

- If an RN-D is included in the system coherency domain, it must respond to DVM requests from CI-700
- If an RN-D is excluded from the system coherency domain, it does not receive DVM requests from CI-700

4.2.8.1 Hardware interface

This section describes the hardware interface for RN inclusion into and exclusion from system coherency domain.

CI-700 provides two signals for RN system coherency entry and exit:

- **SYSCOREQ** input (to CI-700)
- **SYSCOACK** output (from CI-700)

These two signals implement a four-phase handshake between the RN and CI-700 with four states. The following table describes this handshake.

Table 4-5: RN system coherency states

SYSCOREQ	SYSCOACK	State
0	0	DISABLED
1	0	CONNECT
1	1	ENABLED
0	1	DISCONNECT

Coming out of reset, the RN is in the DISABLED system coherency state.

CONNECT

To enter system coherency, an RN must assert **SYSCOREQ** and transition to the CONNECT state. The RN must be ready to receive and respond to snoop and DVM requests in this state.

ENABLED

Next, CI-700 asserts **SYSCOACK** and transitions to the ENABLED state. The RN is now included in the system coherency domain. The RN can receive and must respond to snoop and DVM requests in this state.

DISCONNECT

When the RN is ready to exit system coherency, it must deassert **SYSCOREQ** and transition to the DISCONNECT state. The RN continues to receive and must respond to snoop and DVM requests in this state.

DISABLED

When all outstanding snoop and DVM responses have been received, CI-700 deasserts **SYSCOACK** and transitions to the DISABLED state. In this state, no snoop or DVM transactions are sent to the RN which can now be powered down.

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The following rules must be obeyed to adhere to the four-phase handshake protocol.

- When **SYSCOREQ** is asserted, it must remain asserted until **SYSCOACK** is asserted.
- When **SYSCOREQ** is deasserted, it must remain deasserted until **SYSCOACK** is deasserted.

4.2.8.2 Software interface

This section describes the software interface for RN inclusion into and exclusion from system coherency domain.

CI-700 provides two configuration registers for system coherency entry and exit:

RN-F
- por_mxp_p{1,0}_syscoreq_ctl
- por_mxp_p{1,0}_syscoack_status

RN-D
- por_rnd_syscoreq_ctl
- por_rnd_syscoack_status

Reading and writing to these configuration registers provides a software alternative to the four-phase hardware handshake.


Note

It is possible the configuration registers contain multiple bits where each bit corresponds to a different RN. The following description is about the read and write of the configuration register bit that corresponds to a given RN. When configuring the system coherency entry or exit for a given RN, software must adopt a Read-Modify-Write strategy. This strategy ensures configuration register bits corresponding to other RNs are not modified when writing into the syscoreq_ctl configuration register.

Coming out of reset, both configuration registers are cleared, indicating DISABLED state.

CONNECT

To initiate an RN entry into the system coherency domain, software must first poll both configuration registers. This poll ensures the configuration register bits corresponding to that RN are set to 0. When the RN is ready to receive and respond to snoop and DVM requests, software must write a 1 into the corresponding bit in the syscoreq_ctl configuration register. This write process transitions the RN to CONNECT state.

ENABLED

Next, CI-700 indicates a transition to ENABLED state by setting the corresponding configuration register bit in the syscoack_status register to 1. The RN is now inside the system coherency domain. Software can poll the syscoack_status register to determine this state transition.

DISCONNECT

To initiate an RN exit from the system coherency domain, software must first poll both configuration registers. After ensuring that the configuration register bits corresponding to that RN are set, software must clear the corresponding syscoreq_ctl bit to transition the RN

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to DISCONNECT state. The RN continues to receive and must respond to snoop and DVM requests in this state.

DISABLED

When all outstanding snoop and DVM responses have been received, CI-700 clears the corresponding syscoack_status bit indicating the transition to DISABLED state. In this state, no snoop or DVM transactions are sent to the RN. Software must poll the syscoack_status register to ensure that this state transition has occurred before initiating RN powerdown.


Note

To adhere to the four-phase handshake protocol, the following rules apply:

- The hardware interface is intended as the primary interface. The software interface is provided as an alternative for legacy RN devices and systems that do not support the hardware interface.
- Either the hardware interface or the software interface must be used, but not both. Coming out of reset, the hardware interface is enabled by default. The first write into the syscoreq_ctl register disables the hardware interface and enables the software interface. There must be a reset to re-enable hardware interface.
- When the software interface is employed, **SYSCOREQ** must remain deasserted.
- When the hardware interface is employed, software must not write to the syscoreq_ctl configuration register.

4.3 Identifying devices in the mesh

CI-700 supports various types of IDs that are used to identify devices in the mesh. It uses these IDs, for example, for routing purposes.

4.3.1 Default node ID mapping

The physical position of a device in the mesh determines the node ID that the device is mapped to.


Note

This scheme is the default node ID-mapping scheme. This scheme is different from the one that is used when using extra device ports on MXPs. For more information about that scheme, see 4.3.2 Node ID mapping for configurations with extra device ports on page 77.

The following items determine the physical position of a device:

1. The X coordinate of its XP
2. The Y coordinate of its XP
3. The XP device port (0 or 1) that it connects to

Therefore, the device node ID is mapped to (X, Y, port, device ID).

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Note

The naming convention for I/O signals uses decimal values of the node ID. For example, `RXREQFLIT_NIDxxx` uses `xxx` values in decimal.

The node ID size depends on the X and Y dimensions of the CI-700 mesh. The larger of the X and Y dimensions determines the size of the node ID. The following table shows the relationship between mesh X and Y dimensions and the node ID size.

Table 4-6: Node ID size selection

X mesh dimension	Y mesh dimension	Node ID size
4 or less	4 or less	7 bits
5-8	1-2	9 bits
1-2	5-8	

The following tables show the different node ID formats, depending on whether the node ID is 7 bits or 9 bits wide.

Table 4-7: 7-bit node ID format

[6:5]	[4:3]	[2]	[1:0]
X position	Y position	Port	Device ID

Table 4-8: 9-bit node ID format

[8:6]	[5:3]	[2]	[1:0]
X position	Y position	Port	Device ID

The following figure shows a CI-700 system with 7-bit node IDs in decimal format.

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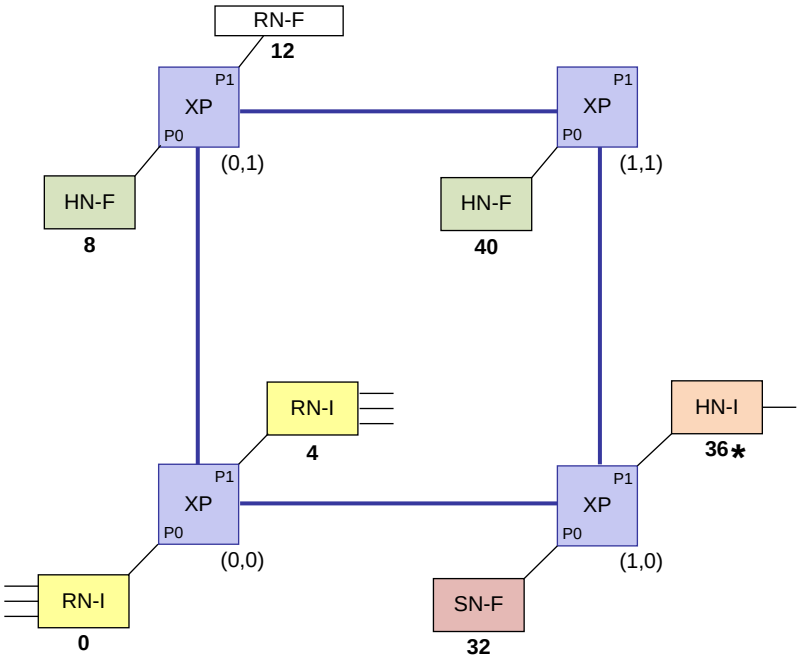
Figure 4-9: Example system with node IDs



Example 4-1: Node ID format

For the HN-I connected to XP (1,0), the node ID reads as 36.

The equivalent binary value is `0b0100100`. In other words, the X position value = `0b01`, the Y position value = `0b00`, the device port value = `0b1`, and the device ID value = `0b00`.

If CAL is present, the devices that are connected to the CAL are assigned consecutive node IDs. For example, if two devices are attached to a CAL, one device is assigned NodeID[1:0]=`0b00` and the other device is assigned NodeID[1:0]=`0b01`.

The following figure shows a CI-700 system with CAL and node IDs in decimal format.

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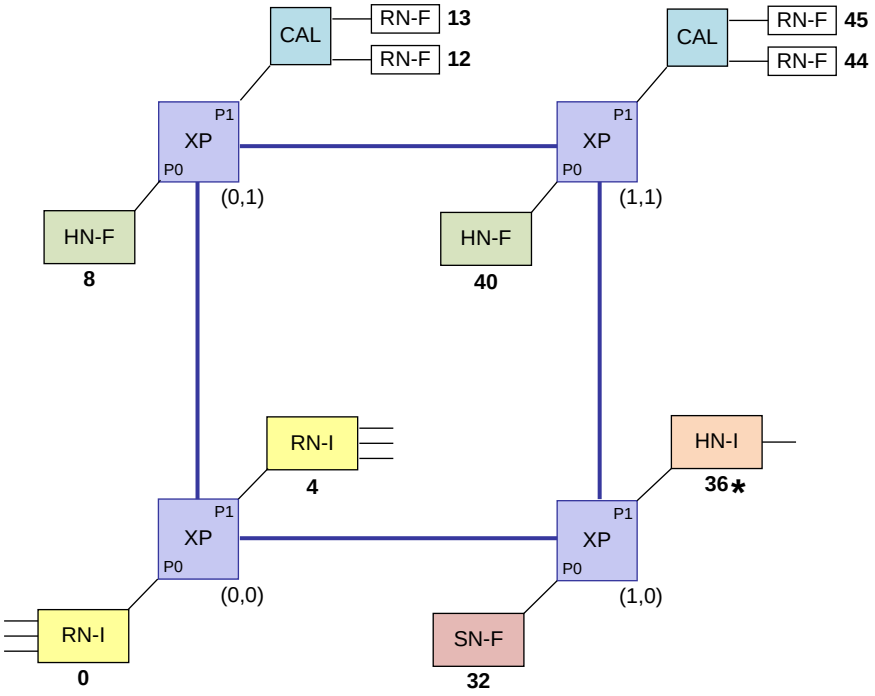
Figure 4-10: Example system with node IDs and CAL



4.3.2 Node ID mapping for configurations with extra device ports

The node ID mapping for a CI-700 configuration changes from the default scheme when you use extra device ports. In this case, the way that node IDs are mapped depends on whether you are using a mesh configuration or a single-MXP configuration.

The node ID-mapping scheme which is described here is used for configurations with extra device ports. This scheme is different to the default scheme. If your configuration does not use extra device ports, see 4.3.1 Default node ID mapping on page 74.

CHI device node ID for mesh configurations



The naming convention for I/O signals uses decimal values of the node ID. For example, `RXREQFLIT_NIDxxx` uses `xxx` values in decimal.

The following items determine the physical position of a device in a CI-700 mesh configuration with extra device ports:

1. The X coordinate of its XP

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2. The Y coordinate of its XP
3. The XP device port (0, 1, 2, or 3) that it connects to

The CHI device node ID is mapped to (X, Y, device port plus device ID).

The node ID size depends on the X and Y dimensions of the CI-700 mesh. The larger of the X and Y dimensions determines the size as shown in the following table.

Table 4-9: Node ID size selection

X mesh dimension	Y mesh dimension	Node ID size
4 or less	4 or less	7 bits
5-8	1-2	9 bits
1-2	5-8	

The following tables show the 7-bit and 9-bit node ID format for a CI-700 mesh configuration using extra device ports.

Table 4-10: 7-bit node ID format for mesh configuration with extra device ports

[6:5]	[4:3]	[2:0]
X position	Y position	Device port plus device ID **[2:1]** Indicates device port **[0]** Indicates device ID on the device port

Table 4-11: 9-bit node ID format for mesh configuration with extra device ports

[8:6]	[5:3]	[2:0]
X position	Y position	Device port plus device ID **[2:1]** Indicates device port **[0]** Indicates device ID on the device port

The following figure shows a CI-700 system with node IDs in decimal format.

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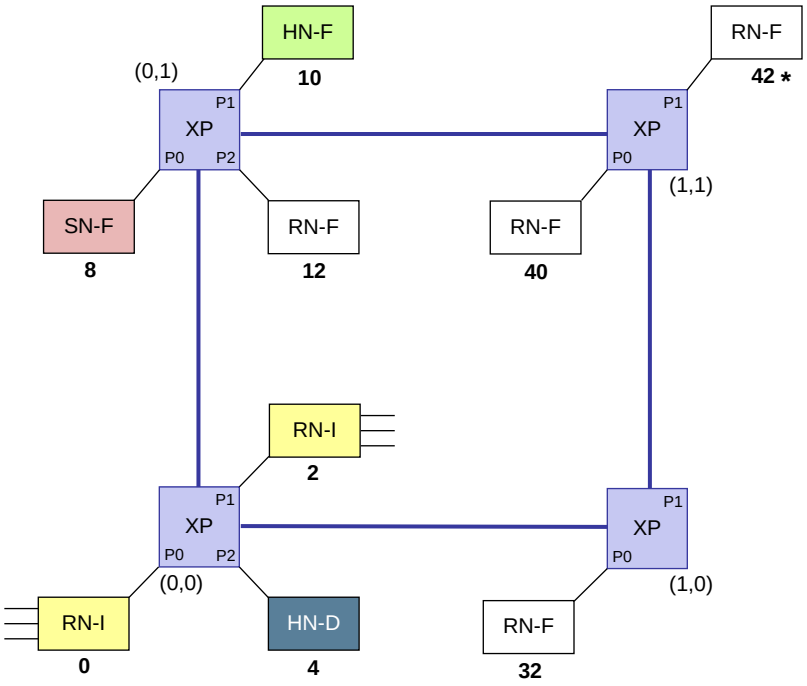
Figure 4-11: Example mesh system with node IDs



Example 4-2: Node ID format for mesh system with extra device ports

For the RN-F on P1 of XP (1,1), the node ID reads as 42.

The equivalent binary value is `0b0101010`. In other words, the X position value = `0b01`, the Y position value = `0b01`, and the device port plus device ID value = `0b010`.

If using CAL in a CI-700 mesh configuration with extra device ports, only CAL2 configurations are permitted. If CAL is present, the devices that are connected to the CAL are assigned consecutive node IDs. For example, consider two devices that are attached to a CAL on P0. One device is assigned NodeID[2:0]=`0b000` and the other device is assigned NodeID[2:0]=`0b001`.

The following figure shows a CI-700 system with CAL and node IDs in decimal format.

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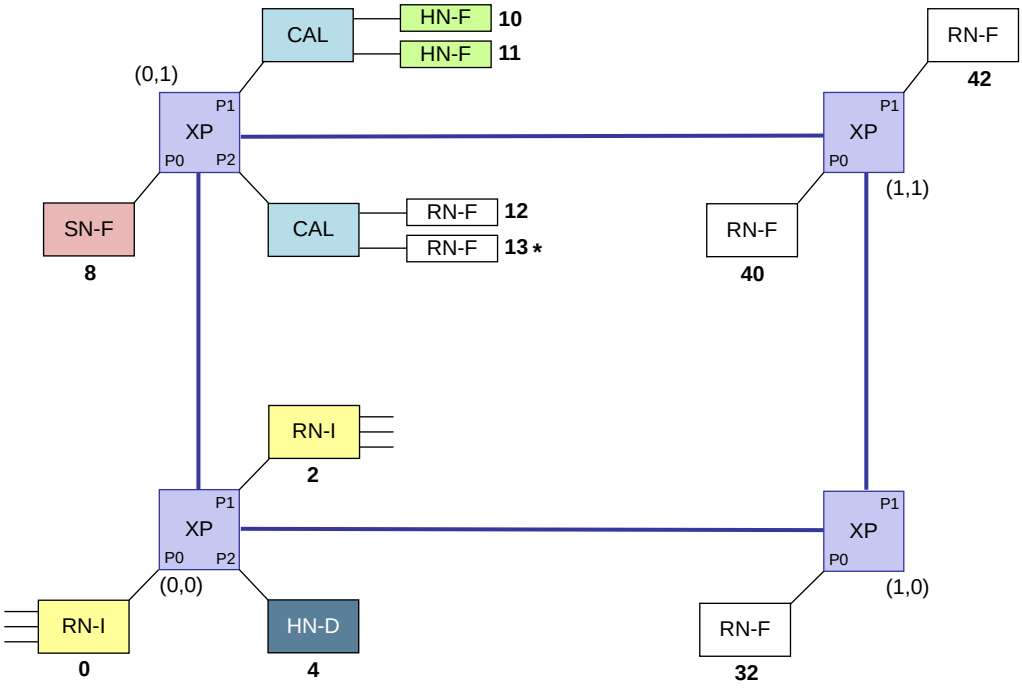
Figure 4-12: Example mesh system using CAL with node IDs



Example 4-3: Node ID format for mesh system with extra device ports and CAL

For the second RN-F attached to the CAL on P2 of XP (0,1), the node ID reads as 13.

The equivalent binary value is `0b0001101`. In other words, the X position value = `0b00`, the Y position value = `0b01`, and the device port plus device ID value = `0b101`.

The following table shows the possible node ID[2:0] encodings for a mesh configuration with extra device ports.

Table 4-12: Node ID[2:0] encodings for mesh configuration with extra device ports

Device port number	Device number	Node ID[2:1]	Node ID[0]
P0	0	`0b00`	`0b0`
	1	`0b00`	`0b1`
P1	0	`0b01`	`0b0`
	1	`0b01`	`0b1`
P2	0	`0b10`	`0b0`
	1	`0b10`	`0b1`
P3	0	`0b11`	`0b0`
	1	`0b11`	`0b1`

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CHI node IDs for single-MXP configurations

The XP device port to which a device connects determines the physical location of a device in a CI-700 single-MXP configuration. For single-MXP configurations, the device port can be P0, P1, P2, P3, P4, or P5.

The device node ID is mapped to (port, device).

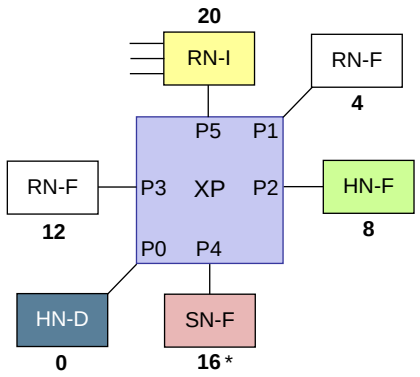
The following table shows the CHI node ID format for a CI-700 single-MXP configuration with extra device ports.

Table 4-13: CHI node ID format for single-MXP configuration with extra device ports

[10:5]	[4:2]	[1:0]
Unused	Port	Device

The following figure shows a CI-700 single-MXP system with node IDs in decimal format.

Figure 4-13: Example single-MXP system with node IDs



Example 4-4: Node ID format for single-MXP with extra device ports

For the SN-F attached to P4, the node ID reads as 16.

The equivalent binary value is `0b10000`. In other words, the device port value = (`0b100` and the device ID value = `0b00`).

If using CAL in a CI-700 single-MXP configuration with extra device ports, all CAL configurations are permitted. If CAL is present, the devices that are connected to the CAL are assigned consecutive node IDs. For example, if two devices are attached to a CAL, one device is assigned NodeID[1:0]=`0b00` and the other device is assigned NodeID[1:0]=`0b01`.

The following figure shows a CI-700 single-MXP system with CAL and node IDs in decimal format.

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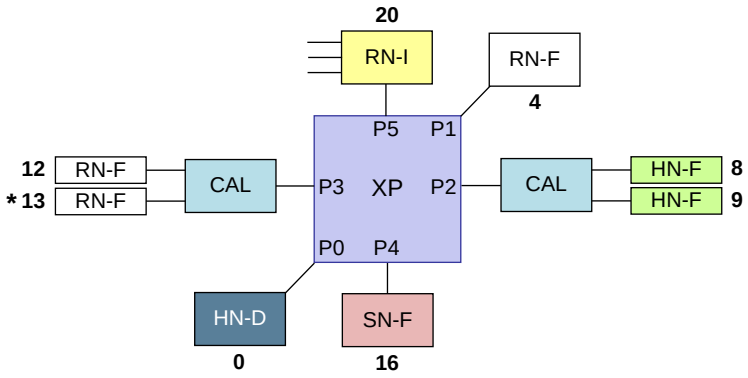
Figure 4-14: Example single-MXP CAL system with node IDs



Example 4-5: Node ID format for single-MXP CAL system

For the second RN-F connected to the CAL on device port P3, the node ID reads as 13.

The equivalent binary value is `0b01101`. In other words, the device port value = `0b011` and the device ID value = `0b01`.

The following table shows the possible node ID[4:0] encodings for a single-MXP configuration with extra device ports.

Table 4-14: Node ID[4:0] encodings for single-MXP configuration with extra device ports

Target device port ID	Target device ID	Node ID[4:2]	Node ID[1:0]
0	0	0b000	0b00
	1	0b000	0b01
1	0	0b001	0b00
	1	0b001	0b01
2	0	0b010	0b00
	1	0b010	0b01
3	0	0b011	0b00
	1	0b011	0b01
4	0	0b100	0b00
	1	0b100	0b01
5	0	0b101	0b00
	1	0b101	0b01

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4.4 System Address Map

All CHI commands must include a fully resolved network address. The address includes a source and target ID. Target IDs are acquired by passing a request address through a *System Address Map* (SAM). The SAM effectively maps a memory or I/O address for the transaction to a target device.

The entire system address space can be partitioned into subregions. Each partition must be designated as one of the following types:

- I/O space
- DDR space

In CI-700, HN-I, HN-D, and HN-T nodes service requests to I/O space. HN-F, SN-F, SBSX, and MTSX nodes service requests to DDR space.

The SAM maps regions in the system address space to the correct target. CI-700 has software-configurable SAM blocks which allow a single implementation of CI-700 to support programmable mappings of addresses to downstream targets.

Every master that is connected to CI-700 must have the same view of memory. Therefore the SAM functionality is required for each requesting device, and each requesting device SAM must generate the same target ID value given the same address.

The SAM consists of several logical units:

RN SAM

Present for all RNs. Maps addresses to HN-F, HN-I, HN-D, and HN-T target IDs. The RN SAM supports generation of SN-F, SBSX, and MTSX target IDs. The RN uses SN-F, SBSX, and MTSX target IDs to issue PrefetchTgt operations directly to the memory controller.



Unmapped addresses are routed to the HN-D.

HN-F SAM

Present in all HN-Fs. Maps addresses to SN-F, SBSX, and MTSX target IDs.

HN-I SAM

Present in all HN-Is. Maps the address of the incoming CHI request to an I/O subregion for ordering purposes.

Related information

- 4.5 RN SAM on page 84
- 4.6 HN-F SAM on page 98
- 4.7 HN-I SAM on page 107

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4.5 RN SAM

Transactions from an RN must pass through an RN SAM to generate a CHI target ID. The target ID is used to send the flit to the correct target node in the mesh.

CI-700 RN-Fs, RN-Is, and RN-Ds use an RN SAM that is internal to the interconnect.

The RN SAM uses two characteristics of a transaction to map requests to downstream target nodes:

- The *Physical Address* (PA) of the request
- Whether the request is a DVM operation, a PrefetchTgt operation, or neither

The RN SAM also has a defined default target, the HN-D. It uses the default target if the preceding characteristics do not result in a match or the RN SAM has not been programmed yet.

Software can configure the mapping structure for addressable requests. To configure the RN SAM, you define discrete regions of your address map and program them in the RN SAM registers. You also specify the target or group of targets for transactions to all addresses in that region.


Note

In your final RN SAM configuration, the boot code region target must not change from the HN-D.

Related information

- 5.4.3 RN SAM and HN-F SAM programming on page 1278

4.5.1 RN SAM memory regions and target types

When you set up the RN SAM, you configure it to map regions of the memory space to specific targets in the mesh. The RN SAM supports various memory region types and target types. It also has some predefined targets, including a default target, that are used in certain scenarios.

The CI-700 RN SAM can contain the following memory region types:

- *Generic Interrupt Controller* (GIC) memory region
- Non-hashed memory region
- Hashed memory region

GIC memory region

The GIC memory region maps specific GIC-related addresses to a specific target ID. You can only specify one GIC memory region.

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Non-hashed memory regions

Non-hashed memory regions are intended to target the I/O space of your system memory map. In other words, the HN targets of non-hashed regions are typically, but not always, one of the following HNs:

- HN-I
- HN-D
- HN-T

A non-hashed memory region always has a single target.

You can specify 8, 12, 16, or 20 non-hashed memory regions in the RN SAM non-hashed region registers.


Note

For RN-F ESAM node types, there is a latency consideration when using 12, 16, or 20 non-hashed regions in the RN SAM. Having 12, 16, or 20 non-hashed regions adds an extra cycle of latency for RN SAM lookup in the XP on the REQ flit.

Hashed memory regions

Hashed memory regions are intended to target the DRAM space of your system memory map. In other words, the targets of hashed regions are typically, but not always, a group of HN-Fs. Accesses to hashed memory regions are distributed across multiple HN-Fs based on a passing the PA of the transaction through a hash function.

The group of HN-Fs that a hashed memory region targets are known as a *System Cache Group* (SCG). You can specify up to four SCGs in the RN SAM SCG region registers. Each SCG supports a primary and secondary address range, so the RN SAM supports up to eight hashed memory regions.

The following figure shows an example system memory map with the memory regions identified.

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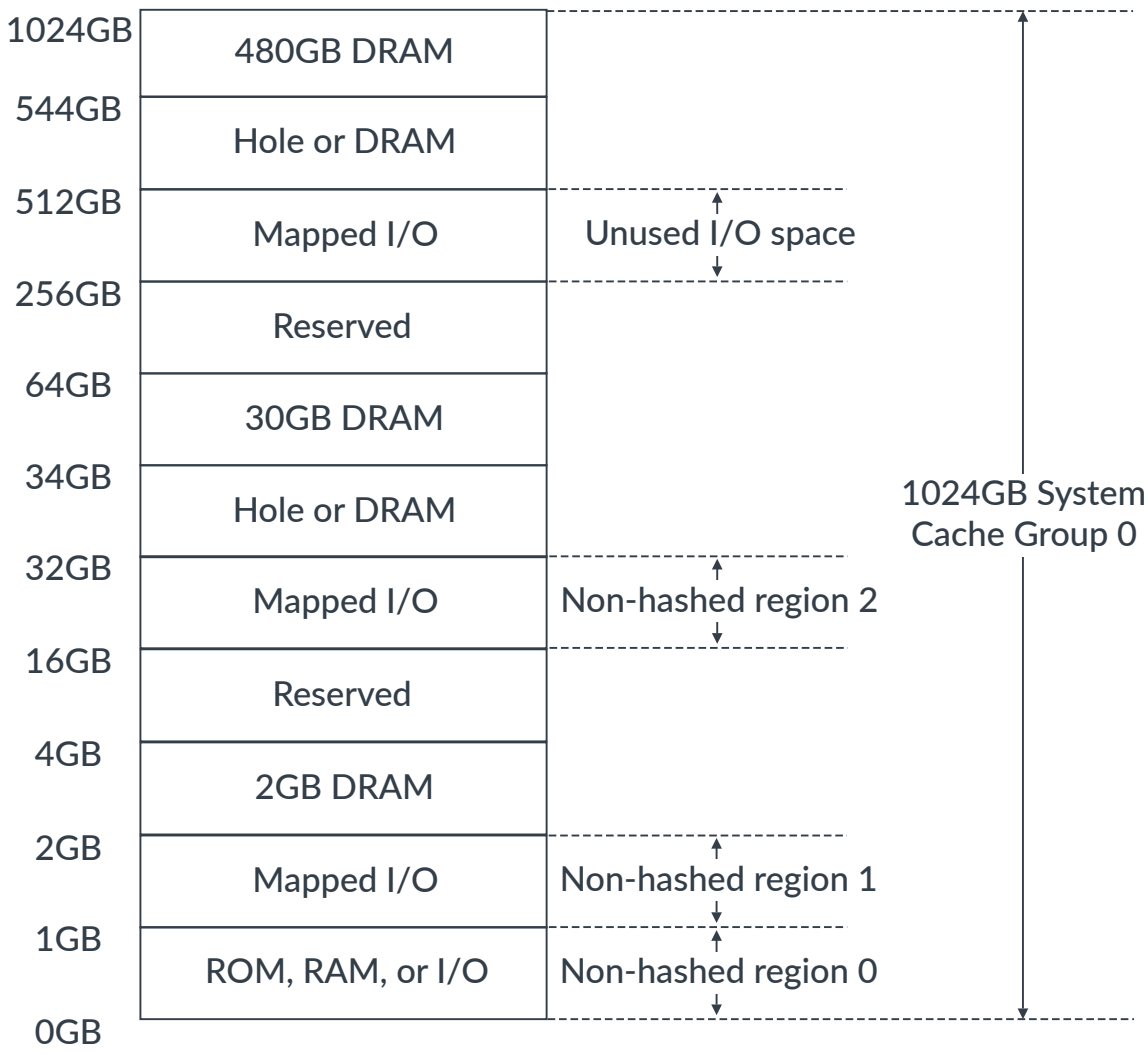
Figure 4-15: Example memory map



Memory regions of the same type cannot overlap with one another, but different memory regions of different types can overlap. For example, two non-hashed regions cannot overlap with one another, but a non-hashed memory region can overlap with a hashed memory region. A priority-based scheme determines the target of an access to an address that is in two overlapping regions. For more information, see 4.5.3 RN SAM target ID selection on page 89.

RN SAM memory region requirements

Each of the programmed region sizes must be a power of two and the region must be size-aligned. The region size can range from 64KB–256TB. For example, a 1GB partition must start at a 1GB-aligned boundary.

It is possible to support complex memory maps where DRAM region sizes are not a power of two or are not size-aligned. For example, Figure 4-15: Example memory map on page 86 shows a more complex memory map. The entire address space is assigned to a single hashed region,

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SCG0. Then, non-hashed regions are individually programmed within that space, which is possible because of their higher target ID selection priority. Software must prevent accesses to addresses in a hashed region that physical memory does not actually serve. For more information, see the *Principles of Arm® Memory Maps White Paper*.

Alternative configurations for non-hashed and hashed memory regions

Usually, non-hashed regions target the I/O space, and hashed regions target the DRAM space. However, alternative configurations are also possible. CI-700 supports the following alternative memory region configurations:

- Using a hashed region to target only one HN-F, instead of multiple HN-Fs
- Using a non-hashed region to target an HN-F, and therefore DRAM. This scenario might be useful if all the SCG region registers have already been used. For target ID selection purposes, this HN-F is classified as a non-hashed target.
- Using an SCG region register for an HN-I, HN-D, or HN-T target. This scenario might be useful if all the non-hashed region registers have already been used. Optionally, you can classify SCG regions 1, 2, or 3 as a non-hashed region. You cannot classify SCG region 0 as a non-hashed region.

Non-region-based targets

The RN SAM contains logic to map certain transaction types to the HN-D node regardless of the PA of the request.

During the boot process, before RN SAM programming, the RN SAM applies a default target ID to all transactions. This default target ensures that transactions can progress. All RN SAMs define the HN-D node as the default target. The interconnect sends all transactions to the HN-D until RN SAM programming completes, when the configured RN SAM regions take effect.

The RN SAM also assigns all DVM transactions to the HN-D, which contains the DN. Therefore, RN SAMs map the target ID of all DVM transactions to the nodeID of the HN-D.

Related information

- 4.5.2 SAM memory region size configuration on page 87
- 4.5.3 RN SAM target ID selection on page 89

4.5.2 SAM memory region size configuration

Hashed, non-hashed, and GIC memory regions support various sizes. Each memory partition must be individually programmed in the SAM registers.

RN SAM and HN-F SAM support the following memory partition sizes:

Hashed and non-hashed

64MB for RN SAM and HN-F SAM up to maximum addressable space (2^{PA_WIDTH}).

GIC

64KB, 128KB, 256KB, and 512KB.

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The following table shows the GIC memory region size encodings to program the RN SAM and HN-F SAM registers.

Table 4-15: RN SAM and HN-F SAM configuration register GIC memory region sizes

GIC memory region size	regionX_size value
64KB	3'b000
128KB	3'b001
256KB	3'b010
512KB	3'b011

The following table shows the hashed and non-hashed memory region size encodings to program the RN SAM and HN-F SAM registers.

Table 4-16: RN SAM and HN-F SAM configuration register hashed and non-hashed memory region sizes

Hashed and non-hashed memory region size	regionX_size value
64MB	7'b0000000
128MB	7'b0000001
256MB	7'b0000010
512MB	7'b0000011
1GB	7'b0000100
2GB	7'b0000101
4GB	7'b0000110
8GB	7'b0000111
16GB	7'b0001000
32GB	7'b0001001
64GB	7'b0001010
128GB	7'b0001011
256GB	7'b0001100
512GB	7'b0001101
1TB	7'b0001110
2TB	7'b0001111
4TB	7'b0010000
8TB	7'b0010001
16TB	7'b0010010
32TB	7'b0010011
64TB	7'b0010100
128TB	7'b0010101
256TB	7'b0010110
512TB	7'b0010111
1PB	7'b0011000
2PB	7'b0011001

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Hashed and non-hashed memory region size	regionX_size value
4PB	7'b0011010

The RN SAM also outputs the target type of the device along with the target ID for the RN to use in various optimizations. The target type encodings are listed in the following table.

Table 4-17: Device target types

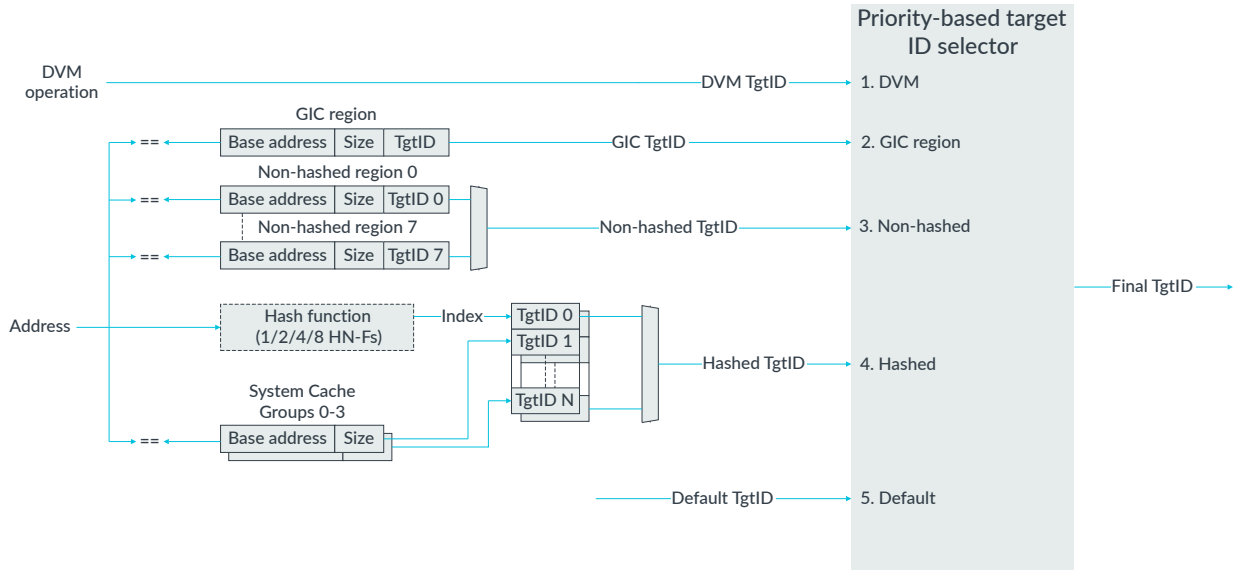
Device type	Target type
HN-F	2'b00
HN-I	2'b01
Reserved	2'b10, 2'b11

4.5.3 RN SAM target ID selection

The RN SAM uses a priority-based target ID selection scheme to select targets for specific addresses. This scheme determines the target ID for certain transaction types. It also resolves the target ID for a request with a PA that is within multiple overlapping memory regions in the RN SAM.

Until the RN SAM has been fully programmed, all addressable transactions use the default target ID. RN SAMs define the HN-D node ID as their default target ID. After the RN SAM has been programmed, the RN SAM selects the target for the transaction based on a defined set of priorities. The following figure shows the RN SAM target ID selection policy.

Figure 4-16: RN SAM target ID selection policy



As the preceding figure shows, different targets have the following priority (from highest priority to lowest priority):

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1. DVM target ID
2. GIC target ID
3. Non-hashed target ID
4. Hashed target ID
5. Default target ID

The DVM target has the highest priority. Therefore, if an RN sends a DVM request, the RN SAM always sends it to the DVM target ID. The DVM target ID is always the HN-D node.

The GIC target has the second highest priority. Therefore, the RN SAM always sends non-DVM requests that are in this region to the programmed GIC region target ID. The GIC memory region is higher priority than the non-hashed or hashed memory regions. Therefore, the RN SAM uses the GIC region target even if the GIC memory region overlaps with a non-hashed or hashed memory region.

The non-hashed targets have the third highest priority. Consider a non-DVM request with a PA that falls within the programmed non-hashed memory region. If the PA does not also fall into an overlapping GIC region, then the RN SAM sends the request to the non-hashed target. The RN SAM uses the non-hashed target even if the PA also falls into an overlapping hashed region, because of the higher non-hashed priority.

The hashed targets have the fourth highest priority. Consider a non-DVM request with a PA that falls within the programmed address range for an SCG. Usually, if the PA does not fall into an overlapping region with higher priority, the RN SAM hashes the PA to determine the target HN-F. Alternatively, if the hashed memory region is in non-hashed mode, then the RN SAM sends the request to the programmed target HN-F. Hashed mode and non-hashed mode for a given hashed region are mutually exclusive.

The default target ID has the lowest priority. Consider a non-DVM request with a PA that does not fall within one of the programmed address regions. In this case, the RN SAM sends the request to the default target ID. The default target ID is always the HN-D node. Read and write requests that do not target the CI-700 configuration register space are issued on the HN-D ACE-Lite interface.

4.5.4 System Cache Groups

An SCG is a group of HN-Fs that share a contiguous memory region. A single HN-F in the SCG services a subset of addresses in the address region. To select the target HN-F in the SCG, the RN SAM uses a hash function.

Each HN-F in an SCG must have the same SLC size.

Each SCG supports two memory regions in the RN SAM, a primary and a secondary memory region. If an incoming address matches either of the two programmed, valid regions, then the RN SAM selects an HN-F as the target ID for the request. To select the HN-F, the RN SAM hashes the PA bits of the request. The hash function outputs an index value that corresponds to a target HN-F ID in a table of target IDs.

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The following limitations apply to the secondary memory regions for an SCG:

- Secondary memory region sizes must be size-aligned and power of two-sized.
- If the primary region for an SCG is set to be in non-hashed mode, the secondary region is also set to be in non-hashed mode.

Related information

- 4.5.1 RN SAM memory regions and target types on page 84
- 4.5.5 SCG HN-F hash algorithm on page 91
- 4.5.6 Configuring SCGs in the RN SAM on page 92
- 4.5.7 Support for HN-Fs with CAL in the RN SAM on page 94

4.5.5 SCG HN-F hash algorithm

During RN SAM lookup, if the address falls within a hashed region, the SCG HN-F hash algorithm determines which HN-F services that request. The algorithm distributes addresses evenly across all HN-Fs in an SCG.

An SCG supports hashing over 1, 2, 4, or 8 HN-Fs, using bits[MSB:6] of the PA of the request. The hash algorithm assumes any bits above the MSB of the PA, which is determined by the value of the `PA_WIDTH` parameter, to be zero. For example, if the PA_WIDTH parameter is set to 34, all bits above bit[33] of the PA are assumed to be zero.

In an SCG, each HN-F is given an index value. The size of the index depends on the number of HN-Fs in the SCG. For example, for an SCG that contains eight HN-Fs, the index is 3 bits wide. The hash algorithm distributes cache lines for the hashed address region between the different indexes, and therefore across all HN-Fs in the SCG.

The algorithm uses bits[MSB:6] of the PA of the request, and calculates the index value of the HN-F that services that address. The index value is associated with the node ID of the HN-F, so the index indicates which HN-F to send the request to.

The following table explicitly shows the hash algorithm.


Note

All numbers on the right-hand side of the equations in the list are bit positions within the PA. For example, 11 corresponds to PA bit[11]. In the equations, ^ represents XOR.

Table 4-18: SCG HN-F hash function

Number of HN-Fs in SCG	Number of bits in index	Equations to calculate each index bit value
2	1	[0] = (6^7^8^...^51)
4	2	[0] = (6^8^10^...^50) [1] = (7^9^11^...^51)

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Number of HN-Fs in SCG	Number of bits in index	Equations to calculate each index bit value
8	3	[0] = (6^9^12^...^51) [1] = (7^10^13^...^49) [2] = (8^11^14^...^50)

Related information

- 4.5.7 Support for HN-Fs with CAL in the RN SAM on page 94

4.5.6 Configuring SCGs in the RN SAM

The CI-700 RN SAM supports up to four SCGs. The SCGs that can be used depend on the number of HN-Fs that you are allocating to each SCG.

The RN SAM supports up to 64 hashed HN-F and SN-F target IDs without using CAL mode. This feature allows up to 64 unique hashed target IDs in the RN SAM SCG target node ID registers. The RN SAM also supports up to 32 hashed target IDs when using CAL mode, with each target ID representing both HN-F nodes behind a CAL instance.


Note

For more information about how to program the RN SAM in DSA-F mode, see 4.8 RN-F Direct Slave Access on page 117.

Restrictions on SCG selection

The number of SCGs that are available depends on the assignment of HN-Fs to certain SCGs. For example, the following table shows an example configuration of SCGs with 8 hashed target IDs. If SCG0 uses 8 hashed HN-Fs, then SCGs 1, 2, and 3 cannot be used. Similarly, if SCG0 and SCG1 contain 4 HN-Fs each, then SCG2 and SCG3 cannot be used.

Table 4-19: Permitted allocation of HN-Fs into SCGs

SCG	Number of HN-Fs (or SN-Fs) per SCG			
	1 HN-F	2 HN-F	4 HN-F	8 HN-F
SCG 0	Y	Y	Y	Y
SCG 2	Y	Y	N	N
SCG 1	Y	Y	Y	N
SCG 3	Y	Y	N	N

To set the number of HN-Fs in an SCG, program the sys_cache_group_hn_count register. To assign HN-Fs (and SN-Fs for PrefetchTgt operations) to an SCG, program the sys_cache_grp_[hn, sn]_nodeid_reg<X> registers. Each sys_cache_grp_[hn, sn]_nodeid_reg<X> register contains space for four nodeIDs.

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The nodeIDs in sys_cache_grp_[hn, sn]_nodeid_reg<X> registers are shared between all the SCGs. Therefore, the number of nodeIDs that are available for each SCG depends on the number of HN-Fs or CALs. The following algorithm determines the distribution of nodeIDs.

SCG0 NodeID0 to nodeID[n - 1]
SCG1 NodeID[n / 4] to nodeID[(n / 2) - 1]
SCG2 NodeID[n / 2] to nodeID[n - 1]
SCG3 NodeID[n x 3 / 4] to nodeID[n - 1]

In the preceding algorithm, n represents the total number of hashed target IDs in the SAM.

If SCG0 uses all the available nodeIDs, then SCG1, SCG2, and SCG3 must not be used. If SCG0 only uses nodeID0 through nodeID[(n / 2) - 1], then SCG1 cannot be used. However, in this case, you can use SCG2 and SCG3 with (n / 4) nodeIDs in each of the SCGs.

Example SCG configurations

For example, the following table shows the register and nodeID allocation for each SCG in a system with eight hashed target IDs.


Note

The hashed target ID allocation in the following tables is also applicable to SN target IDs.

Table 4-20: RN SAM SCG target ID programming for eight hashed targets

SCG target ID registers (eight hashed targets)	Number of HN-Fs per SCG target ID table			
	8	4	2	1
sys_cache_grp_hn_nodeid_reg0	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs
				-
			SCG1_NIDs	SCG1_NIDs
				-
sys_cache_grp_hn_nodeid_reg1		SCG2_NIDs	SCG2_NIDs	SCG2_NIDs
				-
			SCG3_NIDs	SCG3_NIDs
				-

The following table shows the register and nodeID allocation for each SCG in a system with four hashed target IDs.

Table 4-21: RN SAM SCG target ID programming for four hashed targets

SCG target ID registers (four hashed targets)	Number of HN-Fs per SCG target ID table		
	4	2	1
sys_cache_grp_hn_nodeid_reg0	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs
			SCG1_NIDs
		SCG2_NIDs	SCG2_NIDs

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SCG target ID registers (four hashed targets)	Number of HN-Fs per SCG target ID table		
	4	2	1
			SCG3_NIDs

Non-hashed mode for SCGs

SCGs 1-3 can be configured to non-hashed mode. In non-hashed mode, the SCG can contain a single HN-I, HN-T, HN-D, or HN-F. A separate register is used to define the target HN node ID.

Related information

- 4.5.7 Support for HN-Fs with CAL in the RN SAM on page 94
- 5.3.9.40 sys_cache_group_hn_count on page 1018
- 5.3.9.42 sys_cache_grp_nonhash_nodeid on page 1022
- 5.3.9.43 sys_cache_grp_hn_nodeid_reg0 on page 1023-5.3.9.58 sys_cache_grp_hn_nodeid_reg15 on page 1043
- 5.3.9.59 sys_cache_grp_sn_nodeid_reg0 on page 1044-5.3.9.74 sys_cache_grp_sn_nodeid_reg15 on page 1064

4.5.7 Support for HN-Fs with CAL in the RN SAM

In CI-700, you can pair two HN-Fs at an MXP device port using a CAL. If you have HN-Fs with CAL in your configuration, there are extra configuration decisions to make when setting up the RN SAM.

CI-700 supports up to four CAL instances for HN-F nodes in a mesh, allowing up to eight HN-F nodes.

The device ID (NodeID[1:0]) field is the only thing that differentiates the NodeIDs for the HN-Fs that are paired at a CAL. For more information, see 4.3.1 Default node ID mapping on page 74.

Therefore, there are several options for assigning HN-F nodes to SCGs when CALs are used:

Note

The following description of these options uses the example configuration:

- Four CAL instances are used to connect eight HN-F nodes (two HN-F nodes per CAL).
- All eight HN-F nodes belong to the same SCG.

Normal mode

In normal mode, each HN-F node ID is explicitly assigned to an SCG using the methods that 4.5.6 Configuring SCGs in the RN SAM on page 92 describes. In the example configuration, all eight HN-F node IDs would be entered in the target ID registers of the SCG. Therefore, each HN-F has an entry in the hashed target ID table.

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CAL mode

In CAL mode, only one of the two HN-Fs on the CAL has its node ID entered into the SCG target ID registers. In the example configuration, only four HN-F node IDs would be entered in the SCG target ID registers (one per CAL). The HN-F count register for that SCG would be set to four. This approach allows up to eight HN-F nodes that are connected to eight CAL instances to be assigned to an SCG.

The RN SAM sys_cache_grp_cal_mode_reg register contains the CAL mode enable bit for each SCG. For example, to enable CAL mode for SCG 0, write 1 to bit[0] of this register.

The NodeID[1:0] field differentiates the HN-Fs that are attached to a CAL. In CAL mode, the RN SAM uses this differentiation to hash addresses over twice the number of HN-Fs using the existing hashed target ID registers.

For example, consider an SCG that is programmed to have four HN-Fs and HN-F CAL mode enabled for this region. For this SCG, the RN SAM generates eight unique target IDs according to the following function:

Number of bits in index = 3

[0] = (6^9^12^15^18^21^24^27^30^33^36^39^42^45^48^51)
[1] = (7^10^13^16^19^22^25^28^31^34^37^40^43^46^49)
[2] = (8^11^14^17^20^23^26^29^32^35^38^41^44^47^50)

Index bits[1:0] are used to pick between the programmed four HN-F target IDs. Index bit[2] is used to override the device ID field in the following manner:

Target NodeID[10:0] = {hash_nodeID_pick[10:1], hash_nodeID_pick[0] ^ index bit[2]}.

Therefore, in CAL mode, index bit[2] selects between the two HN-Fs on the CAL, which have consecutive NodeIDs.

The following limitations apply to the CAL mode in the RN SAM:

- This feature must only be used when the target HN-Fs are paired using CAL.
- RN SAM does not apply this method to SN-F target IDs. To fully utilize CHI-B PrefetchTgt operations to SN-F, you must map HN-Fs in CAL mode to SN-Fs in a specific way. The paired HN-Fs must always be mapped to same SN-F or group of SN-Fs if 3-SN or 6-SN hashing is used.
- Only one HN-F ID from each CAL group must be programmed in the RN SAM hashed target ID registers.

4.5.8 Address bit masking in the RN SAM

The CI-700 RN SAM supports masking of the address bits that are used for address range comparison and address hashing.

To enable address bit masking in the RN SAM, program the following registers:

- rnsam_region_cmp_addr_mask_reg

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- rnsam_hash_addr_mask_reg

When the RN SAM compares the incoming address against the programmed address ranges, it uses different address bit ranges for different region types:

- For hashed and non-hashed memory regions, RN SAM uses address bits[MSB:26].
- For the GIC memory region, RN SAM uses address bits[MSB:16].

By programming select bits to 0 in the rnsam_region_cmp_addr_mask_reg mask register, both the incoming address and the programmed address ranges can be masked off before comparison. This region mask is applied to hashed, non-hashed, and GIC memory regions.

For hashed regions, the RN SAM hashes all address bits[MSB:6] to equally distribute requests across all HN-F and SN-F target devices. By programming select bits in the rnsam_hash_addr_mask_reg mask register to 0, those address bits can be removed from the hashing logic. This masking only applies to hashed memory regions.

The following limitations apply to address bit masking in the RN SAM:

- If 3-SN or 6-SN mode is enabled in the HN-F SAM, address bits[16:7] and the top_addr_bits are essential in distributing the addresses between memory. We recommend that you mask these bits carefully to avoid memory aliasing.
- The range compare mask must not mask off bits that represent the size of the region. For example, if any of the region sizes are 64MB, address bit[26] must not be masked. Similarly, if a region size is 512MB, address bit[29] must not be masked.
- The address bits that are masked in the HN-F SAM and the RN SAM must be consistent. This requirement ensures that the same SN-F processes both PrefetchTgt requests to the address from an RN-F and SLC misses for the address from an HN-F.

Related information

- 4.5.3 RN SAM target ID selection on page 89
- 5.3.9.38 rnsam_hash_addr_mask_reg on page 1016
- 5.3.9.39 rnsam_region_cmp_addr_mask_reg on page 1017

4.5.9 Support for PrefetchTgt operations in the RN SAM

The RN SAM supports CHI PrefetchTgt operations. These operations are sent from RN-F directly to SN-F, bypassing the HN-F.

To support PrefetchTgt operations, the RN SAM integrates the functionality of HN-F SAM to determine the appropriate SN-F target ID for a given address. RN-Fs only use the SN-F target ID for PrefetchTgt requests. The PrefetchTgt RN SAM programming must match the HN-F SAM for SN-F target IDs.

The following registers configure the PrefetchTgt functionality in the RN SAM:

- sys_cache_grp_sn_attr

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- sys_cache_grp_sn_nodeid_reg{0-1}
- sys_cache_grp_sn_sam_cfg{0-1}

The PrefetchTgt RN SAM registers are only present in RN SAM blocks associated with CHI-B, CHI-C, CHI-D, or CHI-E RN-F nodes.


Note

For RN SAM blocks associated with other node types such as RN-I and RN-D:

- Reads of these register offsets always return a value of zero
- Writes to these register offsets have no effect
- These registers do not appear in the IP-XACT files

Related information

- 4.6 HN-F SAM on page 98
- 5.3.9.41 sys_cache_grp_sn_attr on page 1019
- 5.3.9.59 sys_cache_grp_sn_nodeid_reg0 on page 1044
- 5.3.9.60 sys_cache_grp_sn_nodeid_reg1 on page 1046
- 5.3.9.78 sys_cache_grp_sn_sam_cfg0 on page 1070
- 5.3.9.79 sys_cache_grp_sn_sam_cfg1 on page 1072

4.5.10 Address-range based QoS override

You can program the RN SAM to override the QoS value of requests from RNs to HNs that target certain memory regions. This feature is present in all instances of the RN SAM inside MXP, RN-I, and RN-D.

You can use this feature to change the priority of traffic targeting high-priority or low-priority memory or I/O devices. With this feature, requests that pass through the same QoS regulators can have different QoS values.

You configure the number of override memory regions using the `RNSAM_NUM_QOS_REGIONS` parameter. Each region corresponds to one of the sam_qos_mem_region_reg* registers. Each of these registers contains a bit to indicate the following details for the region:

- Region valid, which indicates that the programmed memory region is valid for comparison
- Region base address
- Region size
- Region QoS value
- Override bit, which determines whether override occurs for that memory region or not

The QoS regions follow the same base address and size properties as hashed and non-hashed regions.

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When you enable this feature, CI-700 compares the incoming address against the valid QoS override memory regions. If the address matches any of the programmed valid addresses, the REQ flit uses the corresponding QoS override value.

The memory regions that you specify for override are independent of the hashed and non-hashed memory regions in the RN SAM. Therefore, QoS override regions can overlap with either of the hashed or non-hashed regions. However, two QoS override regions must not overlap with each other.

The RN SAM QoS memory regions and QoS override do not apply to the GIC memory region. Therefore, you must not specify the GIC memory region as a target for QoS override.

Related information

- 4.5.1 RN SAM memory regions and target types on page 84
- 5.3.9.92 sam_qos_mem_region_reg0 on page 1097-5.3.9.99 sam_qos_mem_region_reg7 on page 1109

4.6 HN-F SAM

Transactions from an HN-F to an SN must pass through an HN-F SAM to generate a CHI target ID. The CHI target ID is used to route the transaction to the correct SN.

The HN-F SAM target of a transaction is based on one of two characteristics:

- The PA of the transaction
- The number of SNs that are downstream of the SCG that the HN-F belongs to

Software can configure the HN-F SAM. To configure the HN-F SAM, you program the HN-F SAM registers, defining address range-based targets and targets for HN-Fs within an SCG.

Related information

- 5.4.3 RN SAM and HN-F SAM programming on page 1278

4.6.1 Mapping SN targets in the HN-F SAM

The HN-F SAM has various methods of mapping transactions to an SN target ID. These methods are either based on the PA of the transaction, or a direct association between an HN-F and an SN.

The HN-F SAM uses three methods of mapping transactions at the HN-F to a downstream SN:

- Address range-based mapping
- Hashed modes
- Direct-mapped mode

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Note

The hashed modes and the direct-mapped mode are mutually exclusive. In other words, an SCG can only use one of the hashed modes or direct-mapped mode. The mode that the SCG uses depends on the number of target SNs that the SCG has.

Address range-based mapping

For address range-based mapping, you can specify up to two address regions in each HN-F SAM. For each address region, you also specify a specific SN target ID, which is the target for transactions in that address range. This mode is useful when you must explicitly map a partition of memory from the global DRAM to an individual SN, for example, an on-chip SRAM.

Hashed modes

In the hashed modes, transactions are striped according to PA across either three, five, or six SNs. These modes are used when the SCG targets three or six SNs, and are also known as 3-SN mode and 6-SN mode respectively.

Addresses within the address range of the SCG are striped at a 256B granularity between the selected SNs. The stripe function uses address bits[16:8], and an extra two (3-SN) or three (6-SN) user-defined address bits.

Direct-mapped mode

In direct-mapped mode, transactions across an SCG target a single SN, or are distributed across 2, 4, or 8 SNs. In other words, this mode is used for a group of SNs with a size that is a power of 2. In direct-mapped mode, you program each HN-F to target a single nodeID, which is known as SN0. To distribute accesses from an SCG across multiple SNs, you distribute target nodeIDs evenly across the HN-Fs in the SCG.

For example, consider an SCG that contains eight HN-Fs and targets eight SNs. In this configuration, the SN0 field of each HN-F would be programmed with a different SN node ID. If an SCG with eight HN-Fs targets four SNs instead, every two HN-F nodes would have the same SN0 field value.

A priority scheme determines the final target node ID. For more information about this priority scheme, see 4.6.2 HN-F SAM target ID selection on page 99.

Related information

- 4.6.4 Examples of 3-SN and 6-SN mode configurations on page 102

4.6.2 HN-F SAM target ID selection

A priority-based selection scheme determines the final target ID for any transaction that passes through the HN-F SAM.

The following figure shows how the target ID is determined from the HN-F SAM.

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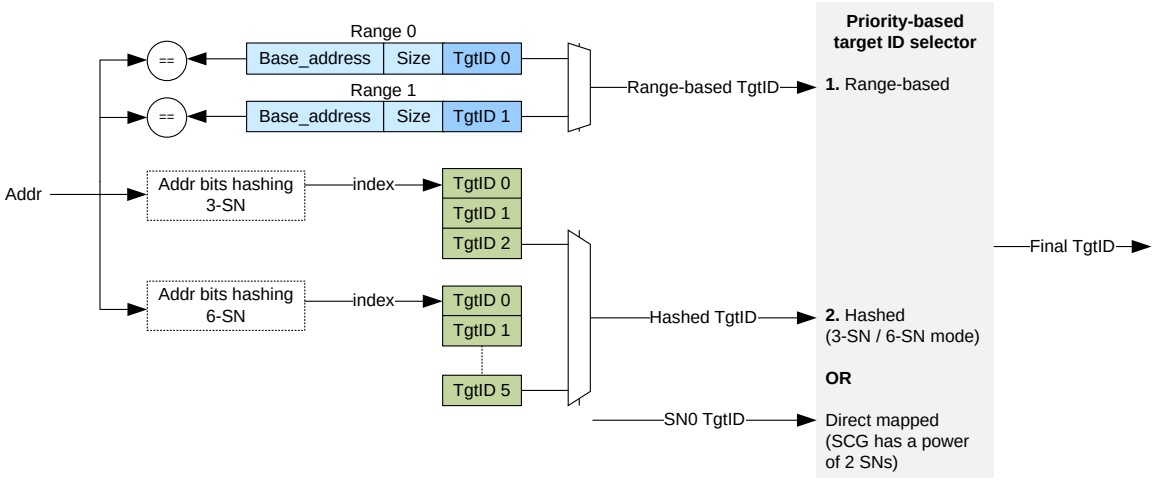
Figure 4-17: HN-F SAM target ID selection policy



As the preceding figure shows, different targets have the following priority (from highest priority to lowest priority):

1. Address range-based target
2. One of the following two mutually exclusive target types:
   - Hashed mode target
   - Direct-mapped mode target

The address range-based targets have the highest priority. Therefore, if the address falls into one of the two valid, programmed address ranges, the HN-F SAM always send the transaction to the address range-based target. Otherwise, one of the other two methods determines the target ID.

Whether the HN-F SAM uses one of the hashed modes or the direct-mapped mode depends on the number of downstream targets. The mode is defined across the whole SCG.

4.6.3 HN-F to SN-F memory striping in HN-F SAM

The CI-700 HN-F SAM supports two memory striping modes, which are known as 3-SN mode and 6-SN mode. In these modes, the HN-F stripes addresses across three SN-Fs or six SN-Fs respectively.

3-SN mode

In 3-SN mode, a stripe function ensures that traffic is distributed evenly among the three SNs. The stripe function is based on PA[16:8] and two higher bits in the PA. The two higher PA bits are referred to as top_address_bit1 and top_address_bit0. Select the top address bits so that the following is true:

- Three of the four combinations of the top address bits appear evenly in the selected address space.

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- The fourth combination never appears.


Note

In some situations, a top bit can be the inverse of the selected PA bit.

For each physical address, one of the three SNs is selected using the following formula:

SN = { ADDR[10:8] + ADDR[13:11] + ADDR[16:14] + ((top_addr_bit1<<1) | top_addr_bit0) } % 3

Example 4-6: Example SN distribution behavior

For a simple case with a 3GB flat address space starting at address `0x0`, top_address_bit1 is PA[31], and top_address_bit0 is PA[30]. With increasing physical address, the function steps between SNs at a 256-byte granularity. As the physical address iterates from 0-128KB, with top_address_bit1 = top_address_bit0 = 0, the first three terms distribute the traffic relatively evenly among the SNs. Of the 512 blocks (256B each) in the first 128KB, the distribution is:

SN[0] 170 blocks 33.2%
SN[1] 171 blocks 33.4%
SN[2] 171 blocks 33.4%

This pattern repeats over each 128KB until 1GB, where top_address_bit0 toggles. With top_address_bit1 = 0 and top_address_bit0 = 1, the pattern is shifted. For each 128KB:

SN[0] 171 blocks 33.4%
SN[1] 170 blocks 33.2%
SN[2] 171 blocks 33.4%

At 2GB, when top_address_bit1 = 1 and top_address_bit0 = 0, the pattern shifts again:

SN[0] 171 blocks 33.4%
SN[1] 171 blocks 33.4%
SN[2] 170 blocks 33.2%

Over the full 3GB, the same number of lines are distributed to each SN.

The HN-F uses the hn_cfg_three_sn_en bit in its por_hnf_sam_control register to enable routing to three SNs. In the por_hnf_sam_control register, the hn_cfg_sam_top_address_bit0 and hn_cfg_sam_top_address_bit1 fields must be configured at boot time. These two address bits are decoded, and used with a hashing function to determine the target SN-F.

6-SN mode

Similar to 3-SN hashing, the 6-SN mode extends the function to equally distribute addresses between six SNs. For each physical address, one of the six SNs is selected using the following formula:

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SN = { ADDR[10:8] + ADDR[13:11] + ADDR[16:14] + ((top_addr_bit2<<2) | (top_addr_bit1<<1) | top_addr_bit0) } % 6

HN-F SAM uses the hn_cfg_six_sn_en bit in the por_hnf_sam_control register to enable striping across six SN-Fs. In 6-SN mode, HN-F SAM also uses hn_cfg_sam_top_address_bit2 field in the por_hnf_sam_control register along with hn_cfg_sam_top_address_bit1 and hn_cfg_sam_top_address_bit0 to hash the incoming address.

Related information

- 4.6.1 Mapping SN targets in the HN-F SAM on page 98
- 4.6.4 Examples of 3-SN and 6-SN mode configurations on page 102
- 5.3.4.61 por_hnf_sam_control on page 460

4.6.4 Examples of 3-SN and 6-SN mode configurations

These hashed mode configuration examples use the Arm PDD memory map and show the configuration settings for each mode, including the top address bits.

The following figure shows the Arm proposed memory map.

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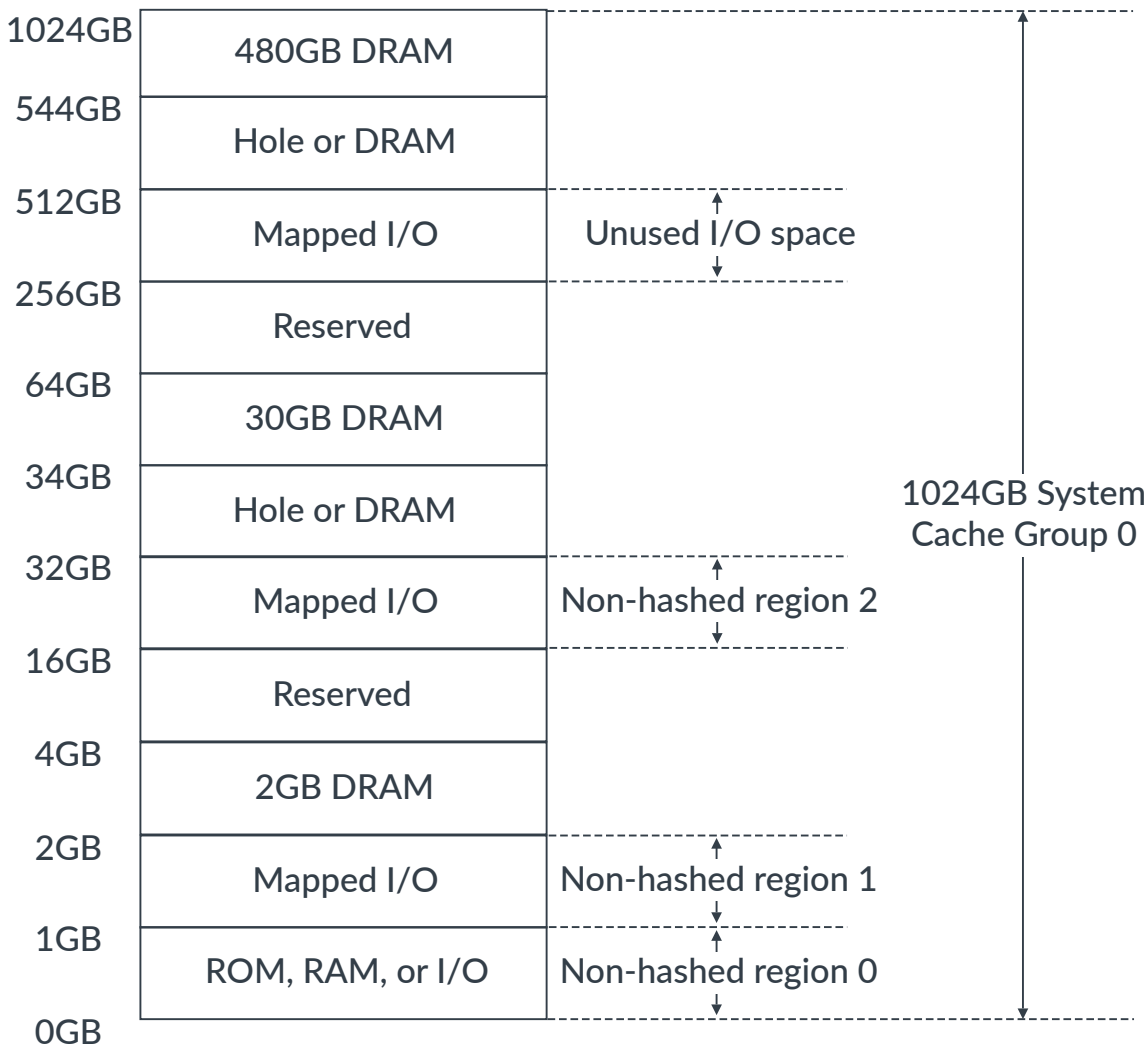
Figure 4-18: Example memory map



The following table shows the valid top address bits for the Arm PDD memory map. For more information, see the *Principles of Arm® Memory Maps White Paper*. This configuration ensures equal distribution of requests across all SN-Fs and prevents memory aliasing. The SAM also provides an inv_top_address_bit configuration bit, which can be used with top address bits as the following table shows.

Table 4-22: 3-SN mode top address bits [bit[1], bit[0]]

Combination 1 (inv_top_address_bit set to 0)	Combination 2 (inv_top_address_bit set to 0)	Combination 3 (inv_top_address_bit set to 1)	Combination 4 (inv_top_address_bit set to 1)
[0, 0]	[1, 1]	[0, 0]	[0, 0]
[0, 1]	[0, 1]	[1, 0]	[0, 1]
[1, 0]	[1, 0]	[1, 1]	[1, 1]

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Note

When inv_top_address_bit=1, it forces the SAM to invert the top most significant top address bit. For 3-SN mode, top_address_bit1 is inverted. For 6-SN mode, top_address_bit2 is inverted.

The following table shows the valid combinations for the address bits for 6-SN mode with the PDD memory map.

Table 4-23: 6-SN mode top address bits [bit[2], bit[1], bit[0]]

Combination 1 (inv_top_address_bit set to 0)	Combination 2 (inv_top_address_bit set to 0)	Combination 3 (inv_top_address_bit set to 1)
[0, 0, 0]	[0, 1, 0]	[0, 0, 0]
[0, 0, 1]	[0, 1, 1]	[0, 0, 1]
[0, 1, 0]	[1, 0, 0]	[0, 1, 0]
[0, 1, 1]	[1, 0, 1]	[0, 1, 1]
[1, 0, 0]	[1, 1, 0]	[1, 1, 0]
[1, 0, 1]	[1, 1, 1]	[1, 1, 1]

Example 4-7: Example for PDD memory map

Assume that a system supports three SN-Fs with 32GB of DRAM at each SN-F port and all three SN-Fs are used for SCG 0. Since the DRAM space is non-contiguous in this memory map (2GB + 30GB + 480GB), the base addresses for each DRAM partition are:

1. a. `000_8000_0000` to `000_FFFF_FFFF` (2GB)
   b. `008_8000_0000` to `00F_FFFF_FFFF` (30GB)
2. `088_0000_0000` to `08F_FFFF_FFFF` (32GB)
3. `090_0000_0000` to `097_FFFF_FFFF` (32GB)

The first two regions together comprise a 32GB region, while the remaining two regions are 32GB each. The following table breaks down the address bits for the regions that are shown in the preceding list.

Table 4-24: Address region example bit settings: 3-SN example

Region	39	38	37	36	35	34	33	32	31
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	1	X	X	X	1
2	1	0	0	0	1	X	X	X	X
3	1	0	0	1	0	X	X	X	X

From the address bit breakdown, the selected top address bits must make sure both regions that are marked as region 1 have the same values. This requirement ensures no aliasing in memory. For this memory map and DRAM size, there are no address bits that directly give combination 1 or combination 2 as Table 4-22: 3-SN mode top address bits [bit[1], bit[0]] on page 103 shows. However, if bits[39, 36] are used along with inv_top_address_bit = 1, then combination 3 is

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possible. This approach ensures that the memory requests are equally distributed across the three SN-Fs without memory aliasing.

The following tables show example address bits in 3-SN and 6-SN hashed modes with specific DRAM sizes. These address bits provide equal distribution of memory across all SN-Fs in the hashed group.

Table 4-25: 3-SN settings for specific DRAM sizes

3-SN DRAM size at each SN-F port	Top address bits [bit[1], bit[0]]	Inv_top_address_bit value
1GB (Total 3GB)	[35, 30]	0
2GB (Total 6GB)	[35, 31]	0
4GB (Total 12GB)	[33, 32]	0
8GB (Total 24GB)	[34, 33]	0
16GB (Total 48GB)	[39, 34]	0
32GB (Total 96GB)	[39, 36]	1
64GB (Total 192GB)	[37, 36]	0
128GB (Total 384GB)	[38, 37]	0

Table 4-26: 6-SN settings for specific DRAM sizes

6-SN DRAM size at each SN-F port	Top address bits [bit[2], bit[1], bit[0]]	Inv_top_address_bit value
1GB (Total 6GB)	[35, 31, 28]	0
2GB (Total 12GB)	[33, 32, 28]	0
4GB (Total 24GB)	[34, 33, 28]	0
8GB (Total 48GB)	[39, 34, 33]	0
16GB (Total 96GB)	[39, 36, 28]	1
32GB (Total 192GB)	[37, 36, 28]	0
64GB (Total 384GB)	[38, 37, 28]	0

4.6.5 Maintaining contiguous address spaces in SN-Fs

To retain contiguous address spaces in each SN-F, SN-Fs typically remove one or more of the PA bits that are presented to them. The bits that the SN-F can strip from the PA depend on several factors that you specify in the RN SAM and HN-F SAM.

If all HN-Fs send their cache misses to a single SN-F, that SN-F services the full address space. However, it is common for a system to have two or more SN-Fs, with each HN-F sending cache misses to a single SN-F. In this scenario, each SN-F services only part of the address space. To keep a contiguous address map, SN-Fs typically remove one or more address bits. The full physical address is presented to each SN-F for every request so that any SN-F based memory protection logic can function. However, the actual mapping to RAM locations can be done with the modified address. The address modification depends on multiple factors:

- Number of HN-Fs in the SCG
- Number of SN-Fs in the SCG

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- Which HN-Fs share SN-Fs

Direct-mapped SN targets

The following table shows direct-mapped HN-F and SN-F combinations that are supported within an SCG, along with the PA bits that we recommend removing.

Table 4-27: HN-F and SN-F combinations supported within an SCG

Number of HN-Fs	Number of SN-Fs	Bits to strip from full PA
2	1	None
	2	[6]
4	1	None
	2	[7]
	4	[7, 6]
8	1	None
	2	[8]
	4	[8, 7]
	8	[8, 7, 6]

For direct-mapped HN-F and SN combinations, use the following method to calculate the bits to remove:

- Calculate the highest bit to remove. To find this bit, determine the least significant address bit in the most significant index bit of the HN-F hash function. The following bits are the highest bit to remove for all the possible SCG HN-F counts:

  8 HN-Fs
  PA[8]

  4 HN-Fs
  PA[7]

  2 HN-Fs
  PA[6]

- The number of bits stripped is $\log_2$(number of SN-Fs). Remove bits sequentially below the highest bit that is calculated according to the preceding process.

This approach to bit stripping assumes that HN-Fs that share SN-Fs are sequential in the RN SAM cache group HN-F table. For example, consider an SCG configuration with eight HN-Fs targeting two SN-Fs. In this case, the bottom four HN-Fs in the RN SAM table would share one SN-F. Similarly, the top four HN-Fs would share the other SN-F.

3-SN and 6-SN address striped targets

3-SN and 6-SN address hashing modes implement a modulo function according to the top address bits used. Therefore, the SN-F must remove these bits to achieve a contiguous memory map in the DRAM.

3-SN mode The SN-F must remove top_address_bit1 and top_address_bit0.

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6-SN mode The SN-F must remove top_address_bit2, top_address_bit1, and top_address_bit0.

Related information

- 4.5.5 SCG HN-F hash algorithm on page 91

4.6.6 Address bit masking in the HN-F SAM

CI-700 supports masking of address bits in the HN-F SAM. You can configure address bit masking for address region comparison and address hashing in hashed mode.

Address bit masking for address range-based targets in the HN-F SAM

The HN-F SAM uses PA bits[MSB:26] when comparing the incoming PA against the programmed address ranges in the HN-F SAM. You can mask off the incoming address and the programmed address ranges before comparison by programming select bits to 0 in the hn_sam_region_cmp_addr_mask_reg mask register.

This region mask is applicable only to address range-based memory partitioning in the HN-F. Therefore the mask is not applied to the hashing scheme in 3-SN or 6-SN mode.

Address bit masking for hashed mode targets in the HN-F SAM

The HN-F SAM supports masking of the PA bits that are used for 3-SN or 6-SN address hashing. You can enable this feature by programming the hn_sam_hash_addr_mask_reg mask register.

Limitations for PA bit masking in the HN-F SAM

The following limitations apply to PA bit masking in the HN-F SAM:

- The address range comparison mask must not mask off bits that represent the size of the region. For example, if any of the region sizes are 64MB, address bit[26] cannot be masked. Similarly, if a region size is 512MB, address bit[29] cannot be masked.
- If 3-SN or 6-SN mode is enabled, address bits[16:7] and the top_addr_bits are essential to distributing the addresses between memory. We recommend that these bits are masked carefully to avoid memory aliasing.
- The address bits that are masked in the HN-F SAM and the RN SAM must be consistent. This requirement ensures that the same SN-F processes both PrefetchTgt requests to the address from an RN-F and SLC misses for the address from an HN-F.

Related information

- 4.6.1 Mapping SN targets in the HN-F SAM on page 98
- 5.3.4.60 hn_sam_region_cmp_addr_mask_reg on page 458
- 5.3.4.59 hn_sam_hash_addr_mask_reg on page 457

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4.7 HN-I SAM

To simplify mapping and ordering of downstream endpoint address space, the HN-I SAM maps an incoming address to a target endpoint that is connected downstream behind HN-I.

The endpoint that is connected to the HN-I can be one of the following types:

- Peripheral with memory-mapped I/O space, such as UART or GPIO
- Physical memory, such as SRAM or FLASH

To map and order the address space of these endpoints, the HN-I SAM supports several address regions. Each address region within the HN-I SAM can have its own specific properties, such as memory type.

The HN-I SAM has a default address region, which is known as address region 0. It can also contain up to three other address regions, which are known as address regions 1, 2, and 3.


Note

Address regions 1, 2, and 3 must not overlap.

Each address region in the HN-I SAM is also divided into one or more order regions. The width of all order regions within a single address region is the same. All accesses within an order region are kept in order, unless the address region is marked as physical memory. If the address region is marked as physical memory, only accesses to the same address are kept in order.

Related information

- 4.7.1 HN-I SAM address region 0 on page 108
- 4.7.2 Configuring HN-I SAM address regions and order regions on page 109

4.7.1 HN-I SAM address region 0

By default, the entire address space of a given HN-I is mapped to address region 0. All transactions to this region are kept in order.

The default order region size in address region 0 is `6'b111111`, which covers the entire HN-I address space. The order region size can also be configured to one of the following options:

- `6'b100100` when `REQ_ADDR_WIDTH`==48
- `6'b100000` when `REQ_ADDR_WIDTH`==44

To configure the properties of address region 0, you program the por_hni_sam_addrregion0_cfg register. Address region 0 is always valid. Therefore, this register does not define a valid bit.

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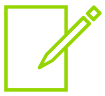
Related information

- 5.3.5.5 por_hni_sam_addrregion0_cfg on page 690

4.7.2 Configuring HN-I SAM address regions and order regions

To configure the HN-I SAM address regions and order regions, program the por_hni_sam_addrregion{0-3}_cfg registers. These registers contain several fields which control specific properties of the address regions and specify order regions. There are also some constraints on programming these registers.


Note

Arm recommends that the HN-I SAM is only programmed during the boot process.

Each address region can be programmed as either physical or peripheral memory. By default, each address region is mapped to peripheral memory.

The different types of memory have the following properties:

Physical memory

Follows normal memory ordering guarantees. Therefore, order region programming does not affect ordering for a physical memory address region.

Peripheral memory

- Follows device memory ordering guarantees
- These address regions can be further divided into smaller address spaces that are known as order regions. Device memory ordering guarantees are maintained within each order region.
- To enforce strict ordering for a specific address region, program its order region size to `6'b111111`.

An address region register must be disabled if the following conditions are true:

- There is potential for new requests to fall into the address region register that is newly configured
- These new requests require ordering in relation to the existing outstanding requests

The minimum address granularity for address regions and order regions is 4KB. This size is equivalent to the minimum slave address space granularity in AXI and ACE-Lite. Therefore, the base address in the por_hni_sam_addrregion{1-3}_cfg registers only includes bits[`REQ_ADDR_WIDTH`−1:12].

Related information

- 5.3.5.5 por_hni_sam_addrregion0_cfg on page 690
- 5.3.5.6 por_hni_sam_addrregion1_cfg on page 691

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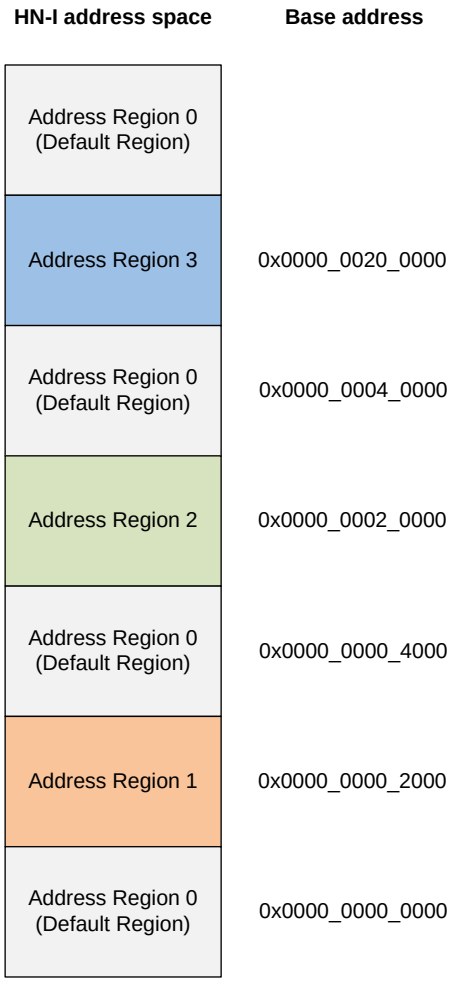
- 5.3.5.7 por_hni_sam_addrregion2_cfg on page 693
- 5.3.5.8 por_hni_sam_addrregion3_cfg on page 695

4.7.3 HN-I SAM example configuration

This example system configuration for HN-I SAM uses three address regions and an order region within each address region.

The following figure shows the high-level configuration of the address space and the base addresses of each address region.

Figure 4-19: HN-I address space example



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Note

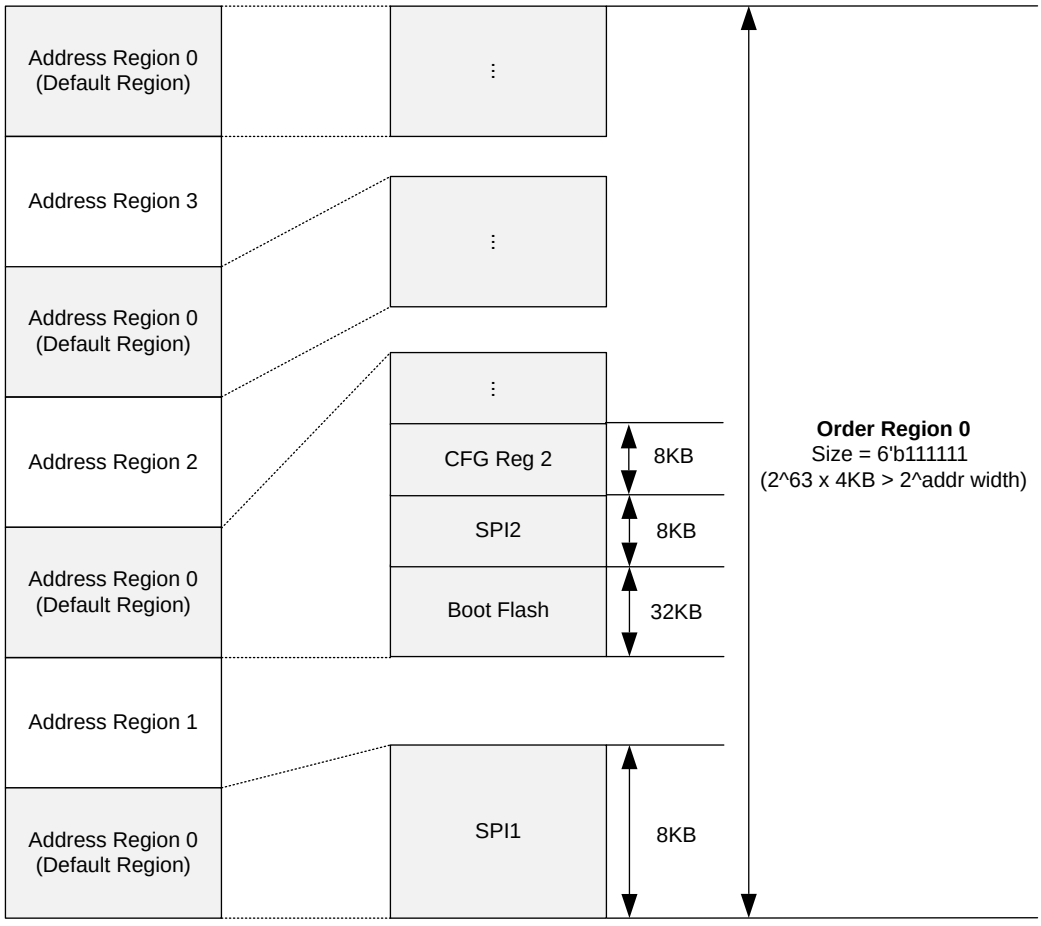
For this example, in the por_hni_sam_addrregion{0-3}_cfg registers, the following bit fields use the default value:

- ser_all_wr
- ser_devne_wr
- pos_early_wr_comp_en
- pos_early_rdack_en

Address region 0

In this example, address region 0 contains two SPI regions, SPI1 and SPI2, a boot flash region, and a configuration register region. The following figure shows this example address region 0 configuration.

Figure 4-20: Example address region 0 configuration



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The largest peripheral address region in address region 0 is the boot flash region, which is 32KB. Requests targeting this boot flash region must be kept in order. If we configure the order region 0 size to 32KB, then requests with addresses from `0x0000_0000_0000` to `0x0000_0000_8000` are ordered. However, the boot flash is not aligned to a 32KB boundary, and spans `0x0000_0000_4000` to `0x0000_0000_C000`). Therefore, part of the boot flash region sits between two order regions. Requests targeting that region might be kept out of order and cause issues. To ensure that the whole boot flash region is covered by a single order region, we must configure the order region 0 size at least 64KB.

However, if the order region 0 size is 64KB, then the SPI1, SPI2, and configuration register regions also fall into the first order region. Therefore, the following alternative configuration might be useful to optimize performance:

- Address region 0 has a memory map where boot flash is aligned to a 32KB boundary
- The order region 0 size is configured to 32KB

The following table shows the configured values for the por_hni_sam_addrregion0_cfg register when the order region size is 64KB.

Table 4-28: Example por_hni_sam_addrregion0_cfg register programming

Bits	Field name	Configured value
[62]	pos_early_wr_comp_en	`1'b1`
[61]	pos_early_rdack_en	`1'b1`
[60]	ser_devne_wr	`1'b0`
[59]	ser_all_wr	`1'b0`
[58]	physical_mem_en	`1'b0`
[5:0]	order_reg_size	`6'h4`

Address region 1

In this example, the whole of address region 1 is assigned to an 8KB SRAM region. The following figure shows the example configuration for address region 1.

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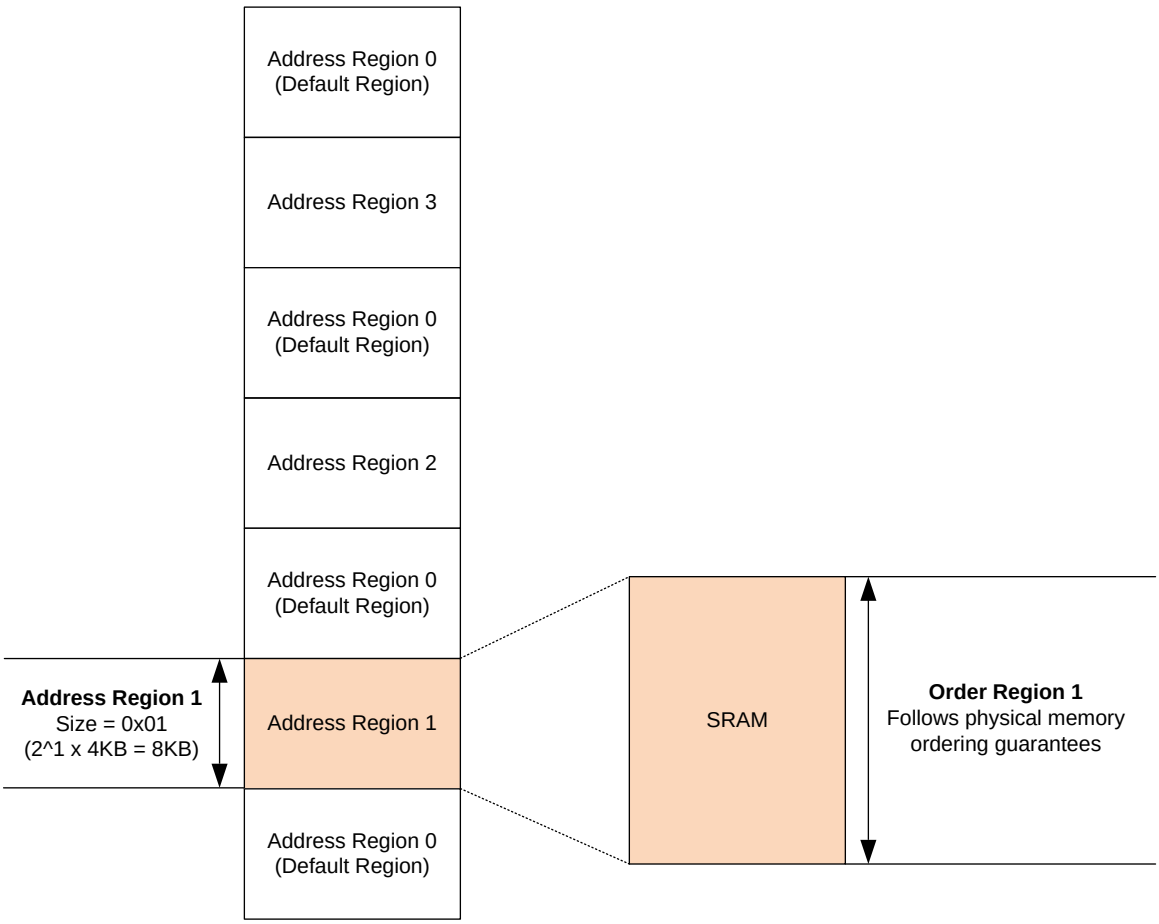
Figure 4-21: Example address region 1 configuration



Address region 1 starts at base address `0x0000_0000_2000`. The whole of address region 1 is considered as one order region, which is 8KB in size. However, because there is SRAM behind this region, it is mapped as physical memory. Therefore, ordering is maintained only between all overlapping requests to a single 64B cache line. This means that, accesses to different cache lines are not kept in order.

The following table shows the configured values for the por_hni_sam_addrregion1_cfg register.

Table 4-29: Example por_hni_sam_addrregion1_cfg register programming

Bits	Field name	Configured value
[63]	valid	`1'b1`
[62]	pos_early_wr_comp_en	`1'b1`
[61]	pos_early_rdack_en	`1'b1`
[60]	ser_devne_wr	`1'b0`
[59]	ser_all_wr	`1'b0`

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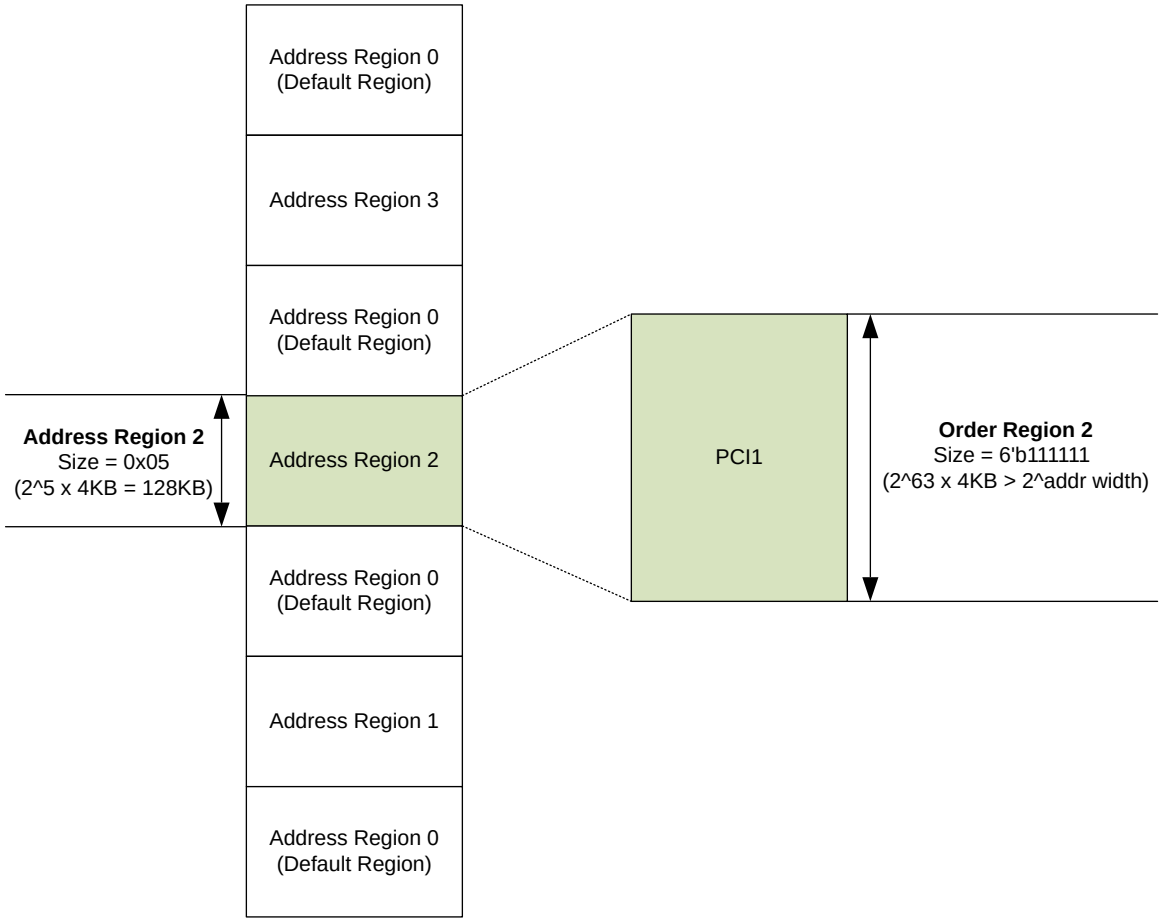
Bits	Field name	Configured value
[58]	physical_mem_en	1'b1
[55:16]	base_addr	40'h0000_0000_2
[15:10]	addr_region_size	6'h1
[5:0]	order_reg_size	6'h1

Address region 2

In this example, address region 2 is assigned to a PCI1 region. The following figure shows the example configuration for address region 2.

Figure 4-22: Example address region 2 configuration



Address region 2 starts at base address `0x0000_0002_0000` and is 128KB in size. The order region 2 size is configured to the maximum value, `6'b111111`, or 2^{63} × 4KB. Therefore, address region 2 is considered as one order region. PCI1 occupies the entire order region, so all PCI1 requests are ordered.

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The following table shows the configured values for the por_hni_sam_addrregion2_cfg register.

Table 4-30: Example por_hni_sam_addrregion2_cfg register programming

Bits	Field name	Configured value
[63]	valid	`1'b1`
[62]	pos_early_wr_comp_en	`1'b1`
[61]	pos_early_rdack_en	`1'b1`
[60]	ser_devne_wr	`1'b0`
[59]	ser_all_wr	`1'b0`
[58]	physical_mem_en	`1'b0`
[55:16]	base_addr	`40'h0000_0002_0`
[15:10]	addr_region_size	`6'h5`
[5:0]	order_reg_size	`6'b111111`

Address region 3

In this example, address region 3 is mapped to the following regions:

- UART0
- UART1
- SPI0
- GIC
- SRAM

The following figure shows the example configuration for address region 3.

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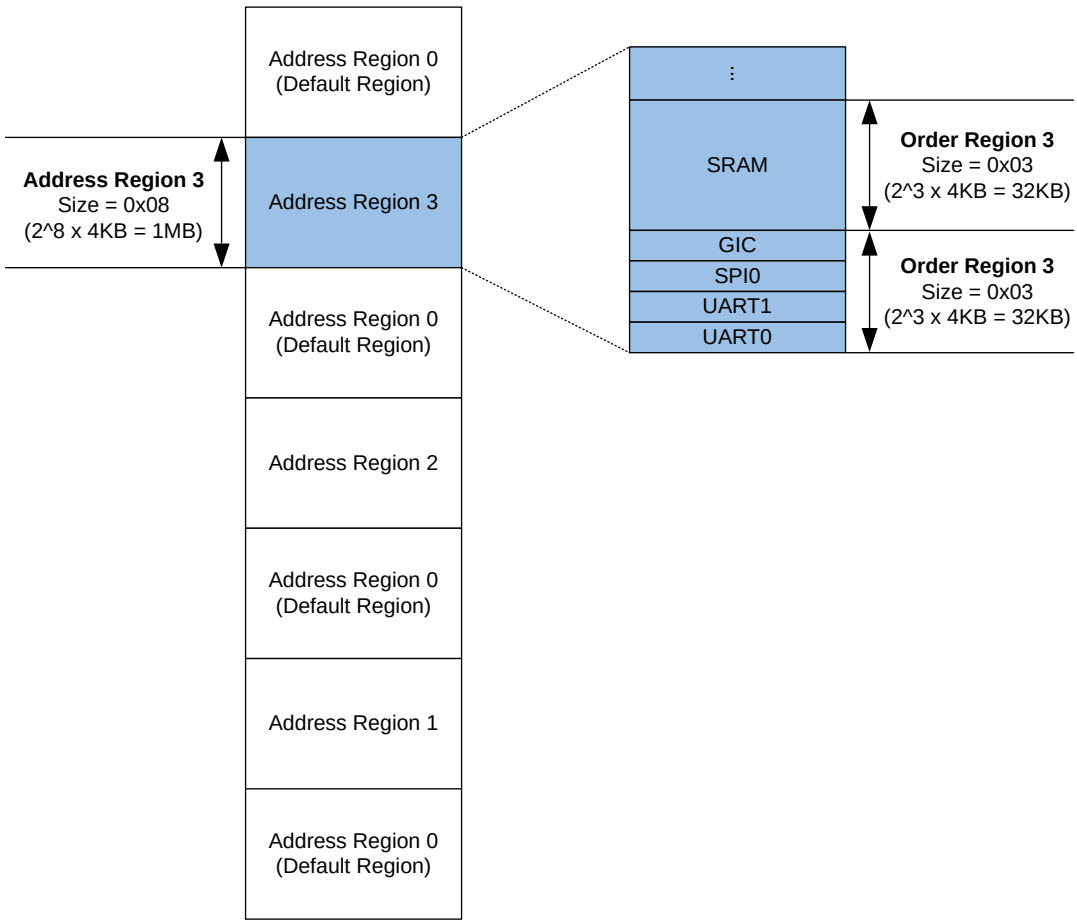
Figure 4-23: Example address region 3 configuration



Address region 3 starts at base address `0x0000_0020_0000` and is 1MB in size. The order region 3 size is set to 32KB, which is less than the address region 3 size of 1MB. Therefore, a total of 32 order regions of 32KB each are contained within address region 3. UART0, UART1, SPI0, and GIC regions map to one order region, so all requests to these peripherals are ordered. SRAM also maps to a single order region, so all requests to SRAM are ordered. SRAM maps to a separate order region from UART0, UART1, SPI0, and GIC. Therefore, requests to SRAM are not ordered with respect to requests to UART0, UART1, SPI0, and GIC, and the other way around.

The following table shows the configured values for the por_hni_sam_addrregion3_cfg register.

Table 4-31: Example por_hni_sam_addrregion3_cfg register programming

Bits	Field name	Configured value
[63]	valid	`1'b1`
[62]	pos_early_wr_comp_en	`1'b1`
[61]	pos_early_rdack_en	`1'b1`

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Bits	Field name	Configured value
[60]	ser_devne_wr	1'b0
[59]	ser_all_wr	1'b0
[58]	physical_mem_en	1'b0
[55:16]	base_addr	40'h0000_0020_0
[15:10]	addr_region_size	6'h8
[5:0]	order_reg_size	6'h3

4.8 RN-F Direct Slave Access

CI-700 supports direct communication between RN-F and MTSX nodes through the *RN-F Direct Slave Access* (DSA-F) feature. Using DSA-F means that RN-Fs can use the Memory Tagging features in the MTSX node without the latency penalty that HN-F nodes incur.

A CI-700 system that uses DSA-F has the following constraints:

- There is no hardware coherency support in the interconnect.
- There must not be any HN-F nodes or RN-I nodes in the CI-700 configuration.
- The RN SAM *System Cache Groups* (SCGs) must be programmed with hashed target IDs corresponding to the MTSX nodes, because no HN-Fs are present.
- MTSX does not support atomic operations. If atomics are sent to MTSX, the behavior of the MTSX is **UNDEFINED**.
- There are no exclusive monitors in MTSX. Exclusive transactions are handled at the MTSX in the following ways:
  - Non-coherent exclusive transactions, such as WriteNoSnp and ReadNoSnp exclusives, are propagated to AXI.
  - Coherent exclusive loads are downgraded to loads with an Exclusive_OKAY response. They are sent downstream on AXI.
  - Coherent exclusive stores are terminated with an Exclusive_OKAY response. They are not sent downstream on AXI.
- All coherent writes and reads are downgraded to non-coherent writes and reads. The MTSX terminates all other coherent operations.
- CI-700 in DSA-F mode does not support DVM requests.
- CI-700 in DSA-F mode does not support configuring HN-I SAM address regions with the physical_mem_en field of the por_hni_sam_addrregionX_cfg register set to 1. All HN-I SAM regions behave like I/O regions.
- CI-700 in DSA-F mode does not support write requests with *Ordered Write Observation* (OWO) signaled from RN-Fs. If OWO writes are sent to MTSX, the behavior of the MTSX is **UNDEFINED**.
- If the SBSX NUM_DART parameter = 64, CI-700 in DSA-F mode can have a maximum of two RN-Fs. If NUM_DART = 128, CI-700 in DSA-F mode can have a maximum of four RN-Fs.
- Device traffic must use HN-I or HN-D, MTSX does not maintain device ordering

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A CI-700 system that uses DSA-F has the following AXI constraints:

- CMOs are only sent on the AXI R channel. You must set the `SBSX_CMO_ON_AW` parameter to 0.
- Persistent CMOs on CHI are downgraded to CMOs on AXI.
- If `AXDATA_WIDTH` = 128 bits, read data cannot be interleaved within a 256-bit aligned address.

In DSA-F mode, you must not override the following por_sbsx_cfg_ctl configuration bits from their initial values:

- disable_write_zero
- disable_prefetch
- force_ncacheable_ncpybk_wr_late_comp
- force_cacheable_ncpybk_wr_late_comp


Note

Contact Arm to confirm that DSA-F configuration requirements are supported.

4.9 MTSX slice channel configuration

The MTSX slice channel enables a minimal configuration to support MTSX functionality.

This configuration includes DSA-F functionality and constraints. Additionally, it does not include RN-I, RN-D, and HN-I components if the additional AXI interfaces are not required.

The MTSX slice channel configuration contains:

- RNFE interface without RN SAM
- MTSX component
- Configuration Node (CFGN) component with the following features:
  - CFG node with APB-only access
  - DTC functionality
  - PCCB functionality
- RAS and interrupt functionality


Note

The only configurable option in this configuration is the MTSX TC size, all other global and MTSX options have fixed values.

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4.10 Downstream Exclusive Cache support

CI-700 supports a *Downstream Exclusive Cache* (DSC) between an MTSX and an AXI memory controller. If DSC mode is enabled, CI-700 generates and propagates specific attributes for DSC for both data accesses and memory tag accesses.

The attributes that CI-700 generates and propagates depend on the type of request.

For read requests on the **ARUSER** channel, CI-700 generates and propagates the following attributes for DSC:

Migratable
Indicates that the cache line can be migrated to CI-700.

Accept_dirty
Indicates if CI-700 can accept dirty data when set to 1 from DSC.

For write requests on the **AWUSER** channel, CI-700 generates and propagates the following attributes for DSC:

Is_copyback
Architecturally cached copy of the line being evicted out of CI-700

Is_dirty
Indicates the write request is dirty, to differentiate clean victims from dirty victims.

For read data on the **RUSER** channel, CI-700 generates and propagates the following attributes for DSC:

Dirty
Indicates that the read data is passed to CI-700 in dirty state.

For more information about the mapping of DSC bits on the AXI interface, see B.4.2 AXI/ACE-Lite master interface signals on page 1383.

4.11 Traffic flow functionality

CI-700 has optional features to optimize the traffic flow of the mesh.

4.11.1 Default XY routing behavior

By default, CI-700 uses an XY routing algorithm to decide which direction to route flits within the mesh. At each MXP, the XID and YID values of the target MXP and the current MXP are compared to determine the routing direction.

Routing directions are referred to by the mesh port that the MXP routes the flit through. For example, if the MXP routes the flit northwards, then the flit is sent through the north mesh port.

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If there is a mismatch between the target MXP XID and the current MXP XID, then the MXP uses the following rule to decide the routing direction:

- If target MXP XID > current MXP XID, then route eastwards.
- Otherwise, route westwards.

If the target MXP XID and the current MXP XID match, then the flit routing components are compared against the YID of the MXP. If YIDs do not match, then the MXP uses the following rule to decide the routing direction:

- If target MXP YID > current MXP YID, then route northwards.
- Otherwise, route southwards.

If the target MXP XID and YID match the current MXP XID and YID, then the flit has reached the target MXP. At this point, the flit is downloaded to the target device.

The following figure shows the default XY routing flow.

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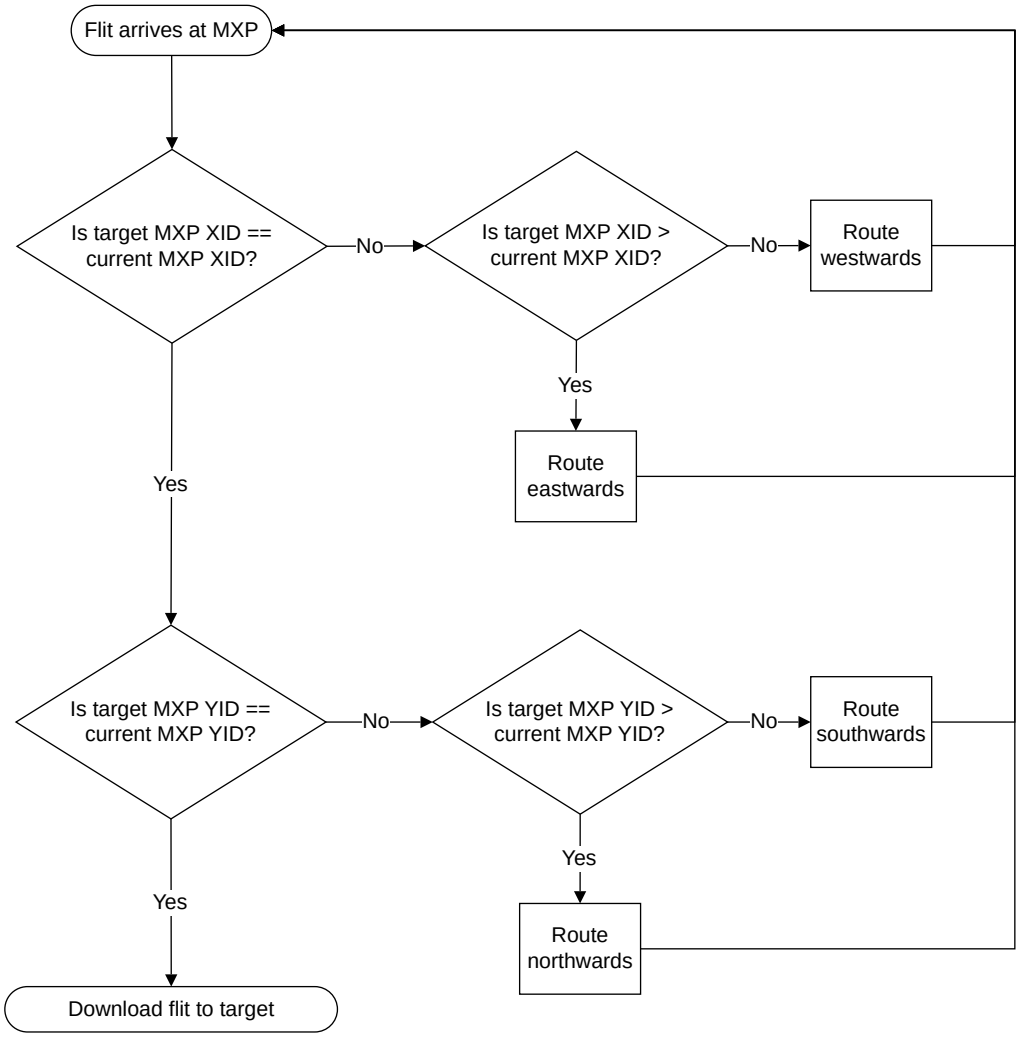
Figure 4-24: Default XY routing flow



You can configure CI-700 to override the default XY routing pattern for specific source-target pairs in the mesh. For more information about this feature, see 4.11.2 Non-XY routing on page 121.

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4.11.2 Non-XY routing

You can configure up to 16 XP pairs in the CI-700 mesh to route CHI traffic against the default XY routing algorithm. Non-XY routing improves the efficiency of traffic flow by reducing hotspots in the mesh layout.

By default, CI-700 uses an XY routing mechanism to route flits through the mesh. For more information about the default XY routing mechanism, see 4.11.1 Default XY routing behavior on page 119.

You can configure any source-target pair of XPs in your mesh configuration to use non-XY routing, up to a maximum of 16 pairs.

Enable this optional feature using the `XY_OVERRIDE_CNT` parameter, which supports values 0, 2, 4, 8, or 16. The value represents the number of source-target pairs which use non-XY routing. To define the non-XY routing XP pairs and their behavior, you can program the por_mxp_xy_override_sel_* registers at boot.

Based on an identified hotspot, select one XP for non-XY routing. This XP is the point of XY route override, which overrides the XY route for the flit while still honoring the XY algorithm.

This feature only applies to the CHI channels, REQ, RSP, DAT, and SNP, not to the PUB channel.

4.11.2.1 Configuring non-XY routing behavior

A boot-programmable static *Lookup Table* (LUT) in each XP controls non-XY routing.

You configure support for this feature by setting the `XY_OVERRIDE_CNT` parameter. For more information, see 4.11.2 Non-XY routing on page 121 and 2.4 Global configuration parameters on page 20.

Eight 64-bit boot-programmable registers control the non-XY routing feature (por_mxp_xy_override_sel_* registers). These registers support override of the route paths for up to 16 source-target XP pairs.

The contents of the por_mxp_xy_override_sel_* registers represent a static LUT. The following table shows the format of each entry in the LUT.

Table 4-32: LUT entry format

Field	Description
<SRCID>	The source ID of the source-target pair that is enabled for XY override.
<TGTID>	The target ID of the source-target pair that is enabled for XY override.
XY route override	Enables flit XY route override in the XP.

The following table shows the structure of a single non-XY routing register.

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Table 4-33: por_mxp_xy_override_sel_* structure

Bit field	Name
[63]	VALID
[62:59]	Reserved
[58:48]	srcid_1
[47]	Reserved
[46:36]	tgtid_1
[35:33]	Reserved
[32]	xy_override_enable_1
[31:27]	Reserved
[26:16]	srcid_0
[15]	Reserved
[14:4]	tgtid_0
[3:1]	Reserved
[0]	xy_override_enable_0

When routing flits between XPs, the XP compares the <SRCID> and <TGTID> flit fields against the entries in this LUT. This comparison and the XY route override value for each XP identify the route for the flit to take.

For the specific programming sequence to set up the LUT, see 5.4.4 Program non-XY routing registers on page 1283.

4.11.2.2 Rules for avoiding deadlocks in non-XY routing

You must follow rules to ensure that the non-XY routing implementation is free of deadlocks.

In the default XY routing scheme, the following turns are forbidden:

- S → E
- N → W
- S → W
- N → E

For non-XY routing, these turns are allowed, but you must apply the following rules to avoid deadlocks. xj or xi represents the XID value of an XP, and yj or yi represents the YID value of an XP.

- If N → W turn is allowed at $XP_{xi,yi}$, then S → E turn is disallowed at every $XP_{xj,yj}$ where (xj < xi) and (yj < yi).
- If S → E turn is allowed at $XP_{xi,yi}$, then N → W turn is disallowed at every $XP_{xj,yj}$ where (xj > xi) and (yj > yi).
- If N → E turn is allowed at $XP_{xi,yi}$, then S → W turn is disallowed at every $XP_{xj,yj}$ where (xj > xi) and (yj < yi).
- If S → W turn is allowed at $XP_{xi,yi}$, then N → E turn is disallowed at every $XP_{xj,yj}$ where (xj < xi) and (yj > yi).

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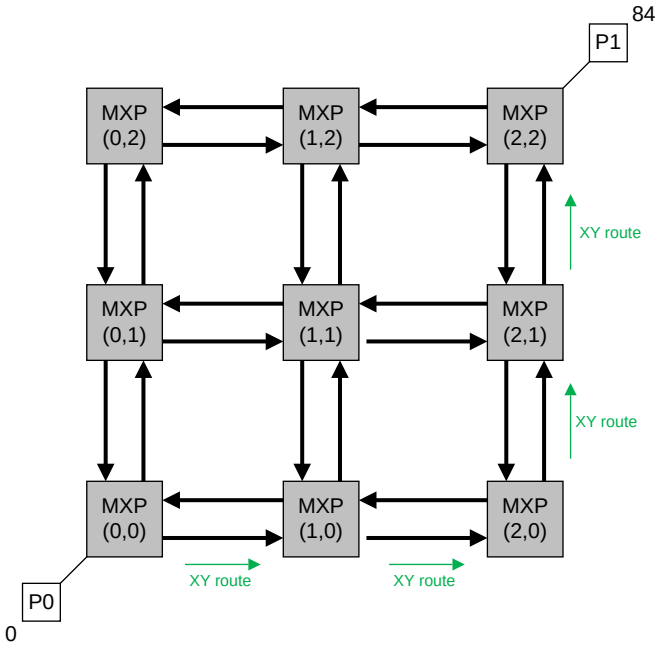
4.11.2.3 Non-XY routing examples

As an example, consider a flit that is uploaded from decimal source NodeID 0 and targets decimal NodeID 84 on a 3x3 mesh configuration.

The following figure shows the default routing of the flit without non-XY routing.

Figure 4-25: Default XY routing example



According to the standard XY routing algorithm, the flit follows the following route:

1. MXPs route the flit in the east direction until the flit reaches $MXP_{(2,0)}$.
2. MXPs route the flit in the north direction to $MXP_{(2,2)}$, where the target node downloads the flit.

XY override enabled

The following figure shows the default routing of a flit and the XY override route.

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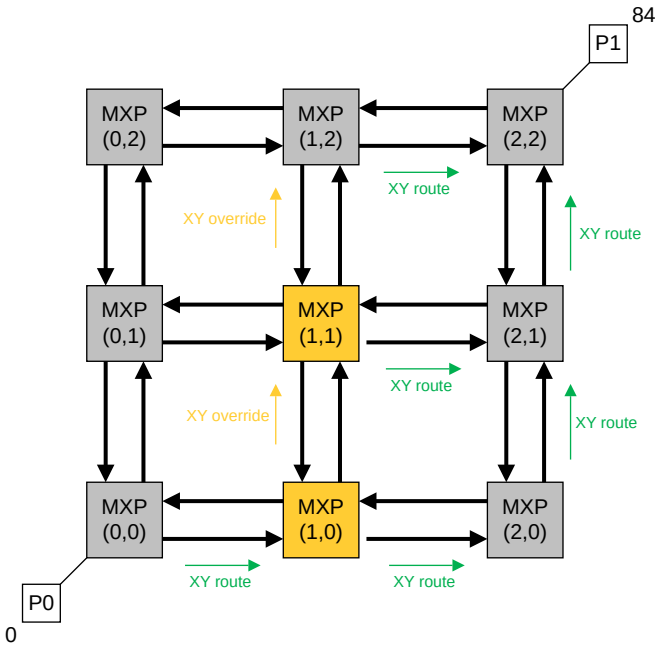
Figure 4-26: XY override enabled routing example



In the example, the non-XY routing registers in $MXP_{(1,0)}$ and $MXP_{(1,1)}$ are configured to override the XY route for a set of source-target pairs. This set includes NodeID 0 and NodeID 84, so the flit follows the following route:

1. $MXP_{(0,0)}$ routes the flit in the east direction.
2. $MXP_{(1,0)}$ and $MXP_{(1,1)}$ route the flit in the north direction, since their configuration has XY override enabled.
3. There is no override set in $MXP_{(1,2)}$. Therefore, the MXP routes the flit in the east direction according to the default XY routing algorithm.
4. At $MXP_{(2,2)}$, the flit has reached its destination, and the target node downloads the flit.

If the XY override option is enabled and YX turn option is disabled, the following assumptions and constraints apply to the routing algorithm:

- If target MXP YID ≥ current MXP YID and a northern mesh port is present, then route northwards.
- If target MXP YID < current MXP YID and a southern mesh port is present, then route southwards.
- If target MXP YID == current MXP YID, a southern mesh port is present, and a northern mesh port is absent, then route southwards.
- Otherwise follow the default XY routing algorithm.

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4.12 Discovery

Discovery is a software algorithm that is used to discover the configuration of CI-700.

Software uses the discovery mechanism to identify the following properties:

- The CHI node ID and LDID corresponding to all node types
- Whether a discovered node is internal or external to CI-700

CI-700 has the following valid logical node types:

- DVM
- Global CFG
- DTC
- HN-F
- HN-I
- RN-D
- RN SAM
- RN-I
- SBSX
- MTSX
- XP

The following figure shows an example configuration. In the example, after discovery, software has enough information to know the location of the following components:

- Global configuration registers
- Configuration registers for each XP
- Configuration registers for the HN-F
- Configuration registers for the RN SAM corresponding to the RN-F

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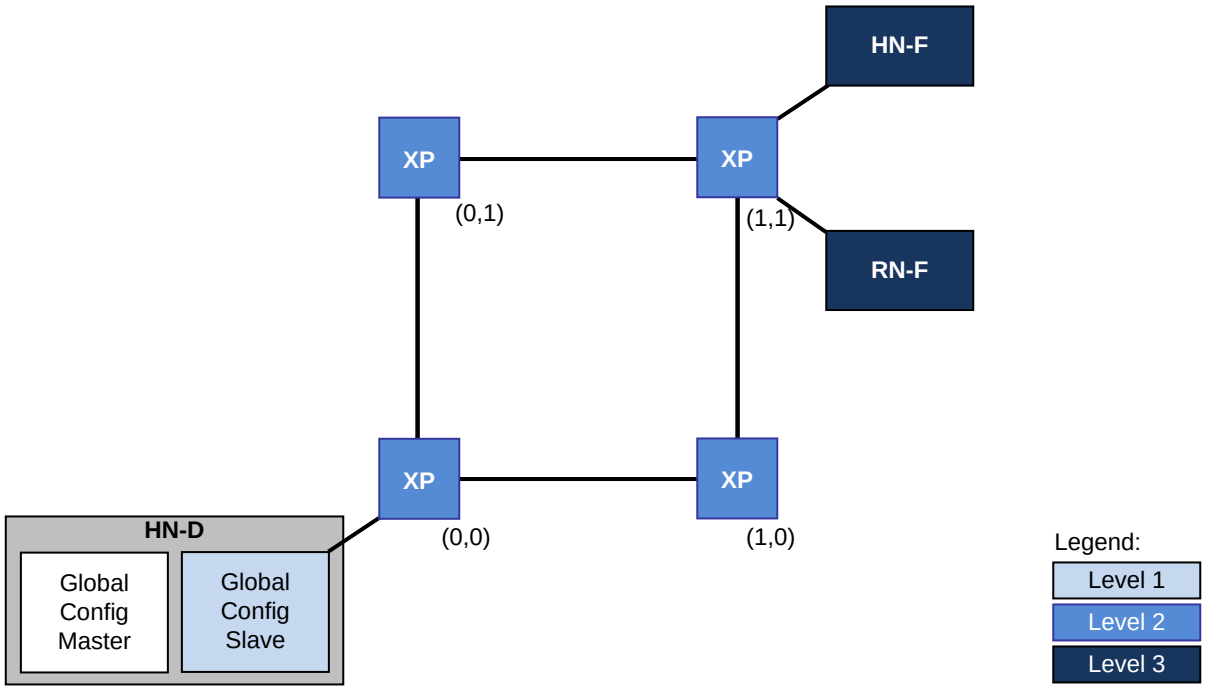
Figure 4-27: 2 × 2 register tree example



4.12.1 Configuration address space organization

The way the configuration address space is organized depends on the system configuration. It is based on one system address, which is known as PERIPHBASE.

PERIPHBASE is the starting address of the range that all CI-700 configuration registers are mapped to. For a CI-700 system in a mesh configuration:

- This address must be aligned to 256MB
- The maximum size of the address range is 256MB

For a CI-700 system in a single-MXP configuration:

- This address must be aligned to 8MB
- The maximum size of the address range is 8MB

Discovery determines specific addresses for individual system blocks that have **IMPLEMENTATION DEFINED** register spaces, as the following figure shows.

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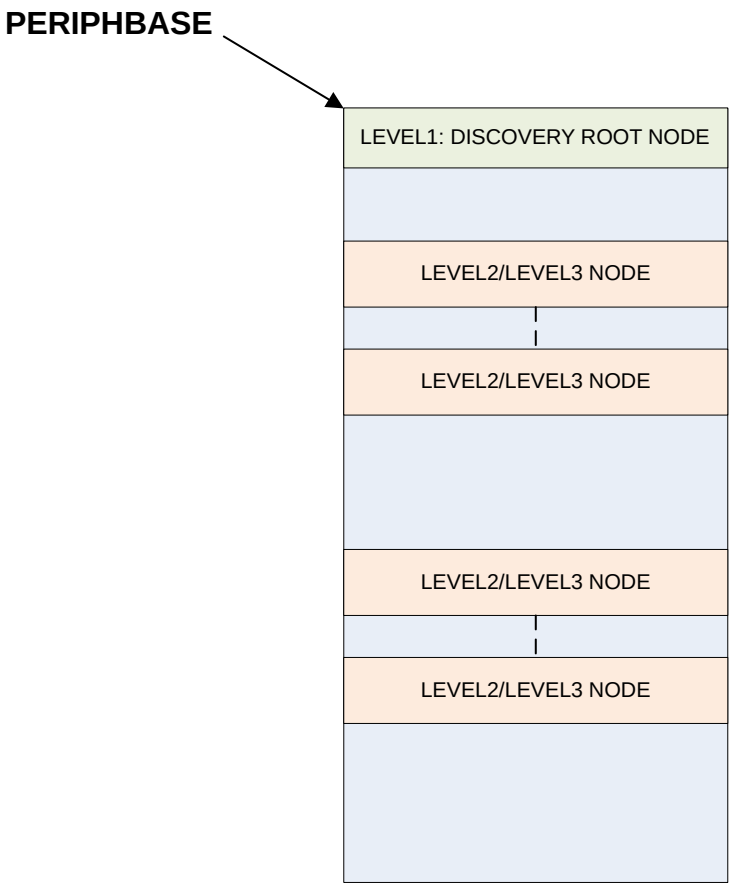
Figure 4-28: PERIPHBASE address map



CI-700 supports 4B and 8B software-accessible registers. Register organization consists of software using 32-bit and 64-bit register reads.

All registers are organized into several register blocks as nodes. A node:

- Is a register block with the size of 64KB
- Is associated with a logical block in the design
- Has information and configuration for that block that is specific to the implementation.

The different types of nodes are:

General Contains device information and has children
Leaf Contains device information, such as configuration data, but has no children.
Pure hierarchy Has children but contains no device information

If a node has more than one child, the node provides:

- The number of children.

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- A pointer to each child.



You can also find the address offsets for each node and configuration register in the IP-XACT file that Socrates™ generates for your custom mesh. Socrates™ stores the IP-XACT file with the rendered RTL in your Socrates™ workspace.

4.12.2 Configuration register node structure

Read-only registers that are organized into several register blocks are referred to as nodes.

Nodes are aligned on 8B boundaries (64KB aligned). The required registers are:

Node Information register — Identifies the product or node type, and the CHI node ID.

Child Information register — Indicates the child count and offset for the first register containing child node pointers. These optional Child Pointer registers each use 8B.



The Node Information and Child Information registers are at fixed offsets for all nodes.

The following figure shows the basic node structure.

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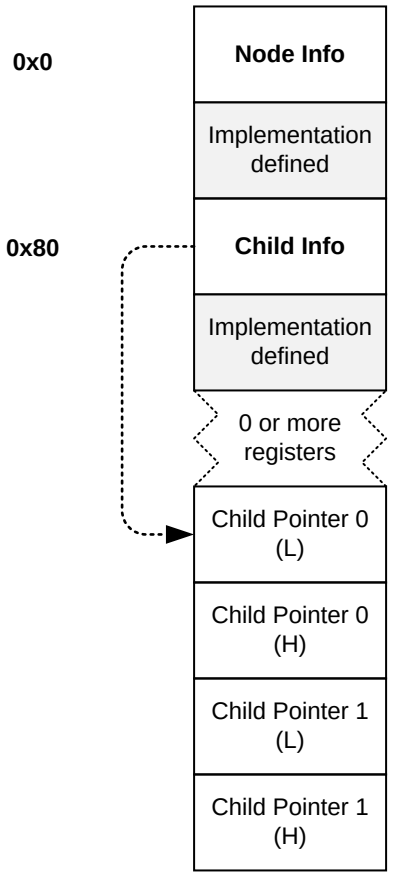
Figure 4-29: Basic node structure



The child_count field of the Child Information register indicates the number of children. This value also represents the number of functional units that are connected to the current unit on the next level of the discovery process.

The child_ptr_offset field of the Child Information register indicates the Child Pointer 0 register offset, in bytes, from the Node Information register address.

Note

For a leaf node (node with no children), the child_count and child_ptr_offset fields must be set to zero.

The following figure provides the node structure detail.

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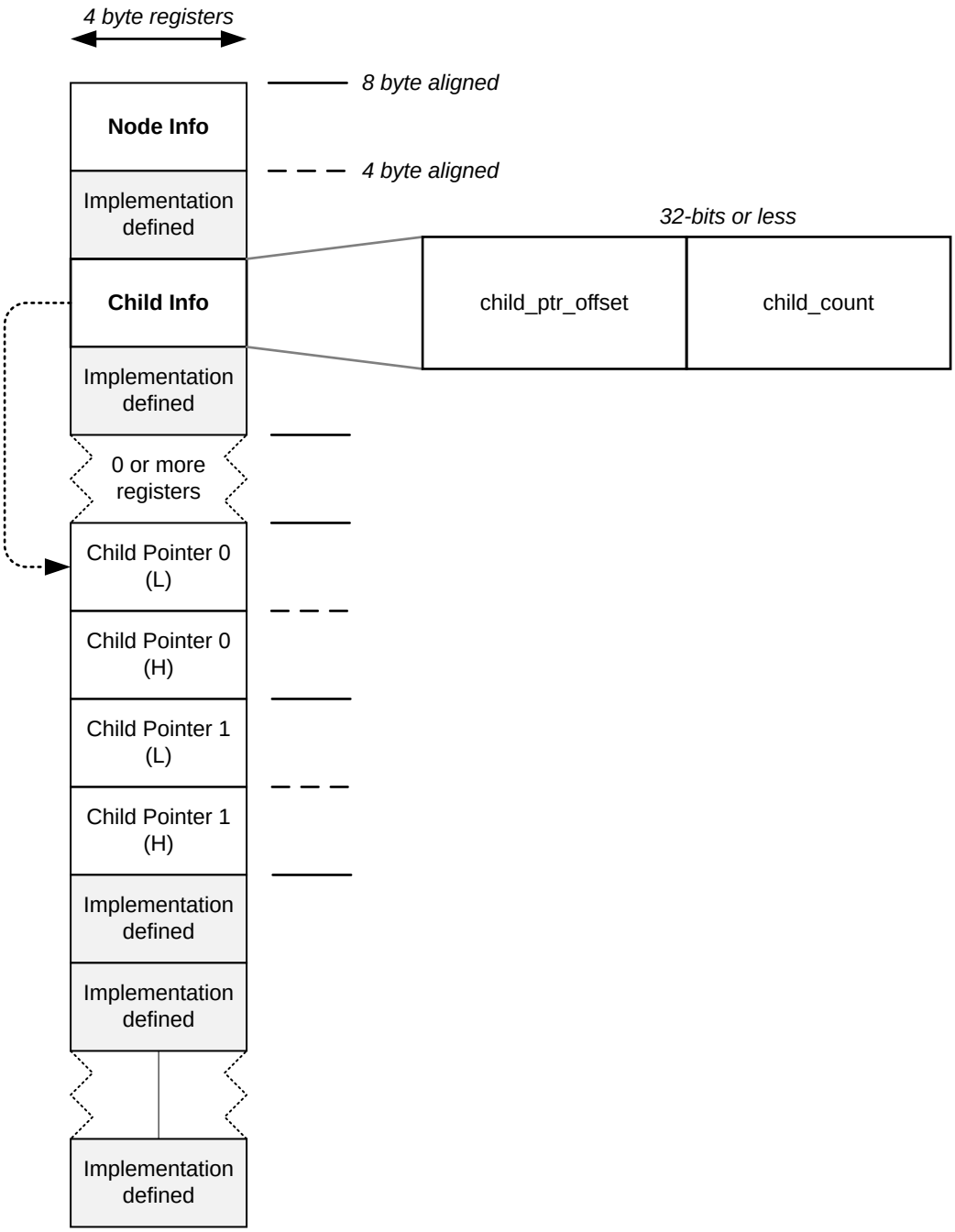
Figure 4-30: Node structure detail



The following table shows the supported node types and the corresponding node_type values in the Node Information register.

Table 4-34: node_type values

Node type	Value
Invalid	`16'h0000`

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Node type	Value
DVM	`16'h0001`
CFG	`16'h0002`
DTC	`16'h0003`
HN-I	`16'h0004`
HN-F	`16'h0005`
XP	`16'h0006`
SBSX	`16'h0007`
MPAM_S	`16'h0008`
MPAM_NS	`16'h0009`
RN-I	`16'h000A`
RN-D	`16'h000D`
RN SAM	`16'h000F`
MTSX	`16'h0010`

4.12.3 Child pointers

Each child node has one child pointer register.

The address of the register containing the first child pointer is calculated using the following addresses and offsets:

Base node address (of the current 64KB block) + the child_ptr_offset value (from the child_info register).

Each subsequent child pointer register is 8 bytes higher. For more information, see Figure 4-30: Node structure detail on page 131.

For example:

- Base node address = `0x40000`.
- Child_ptr_offset in child info register = `0x100`.
- Address of first child pointer register (child pointer 0) = base node address + child_ptr_offset = `0x40100`.
- Address to child pointer 1 = address of child pointer 0 (`0x40100`) + `0x8` = `0x40108`.

Child pointers are 32 bits or less and are contained in the low register. The high register is zero. Child pointer contents include the following:

- The child node address offset from PERIPHBASE (bits[0:29]) which is an unsigned integer (positive offset).
- One reserved bit (bit[30]).
- An External Child Node indicator (bit[31]).

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For example, address to 64KB block of the child node = PERIPHBASE + child pointer register [29:0]. The child pointer register holds the child node address offset relative to PERIPHBASE.

The External Child Node bit of the child pointer register (bit[31]) has the following encodings:

1 Indicates that this CHILD POINTER is pointing to a Config Node that is external to CI-700.

0 Indicates that this CHILD POINTER is pointing to a Config Node that is internal to CI-700.

For CI-700, external child nodes are only used for RN SAM. The software performing the discovery can use two pieces of information:

1. The CHI node ID corresponding to the Config child node in question.
2. Information in the device port connection information register for the device port that the child node is connected to:
   a. por_mxp_device_port_connect_info_p0
   b. por_mxp_device_port_connect_info_p1


Note

By default, CI-700 supports two device ports per MXP, P0 and P1. However, you can also extend the number of device ports. For more information, see 3.10 Support for extra device ports on MXPs on page 50.

The device type corresponding to that child node helps the discovery software determine if the child node is RN-F or RN SAM. It is the responsibility of the discovery software to ensure that the external child node is powered ON before sending any config accesses to it.

Depending on the size of the mesh (X and Y dimensions), CI-700 supports two different widths for encoding the X and Y dimension. The number of bits required is selected based on the larger of the X and Y values.

Table 4-35: Mesh size and encoding bits

Mesh width in X dimension	Mesh width in Y dimension	Number of bits used to encode X, Y
X ≤ 4	Y ≤ 4	2 bits for X, 2 bits for Y
4 < X ≤ 8	Y ≤ 8	3 bits for X, 3 bits for Y
X ≤ 8	4 < Y ≤ 8	3 bits for X, 3 bits for Y

4.12.4 Discovery tree structure

The one-time discovery process creates a lookup table that contains the addresses for all CI-700 configured devices.

The discovery tree structure consists of three levels:

Level 1 Root Node, or the HN-D containing the Global Configuration Slave.

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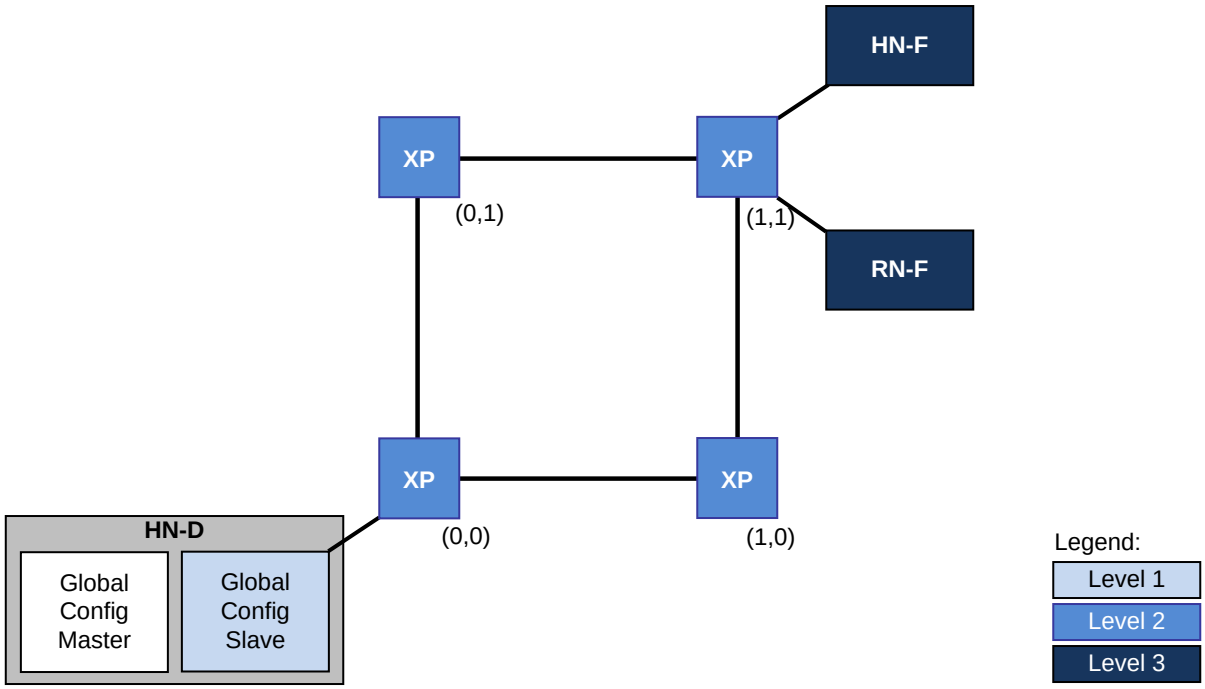
Level 2 XP layer.
Level 3 Leaf layer with one or two devices.

The following figure shows a 2 × 2 mesh configuration example with highlighted discovery tree levels.

Figure 4-31: 2 × 2 discovery tree example



The following figure shows the discovery tree structure for this 2 × 2 mesh configuration.

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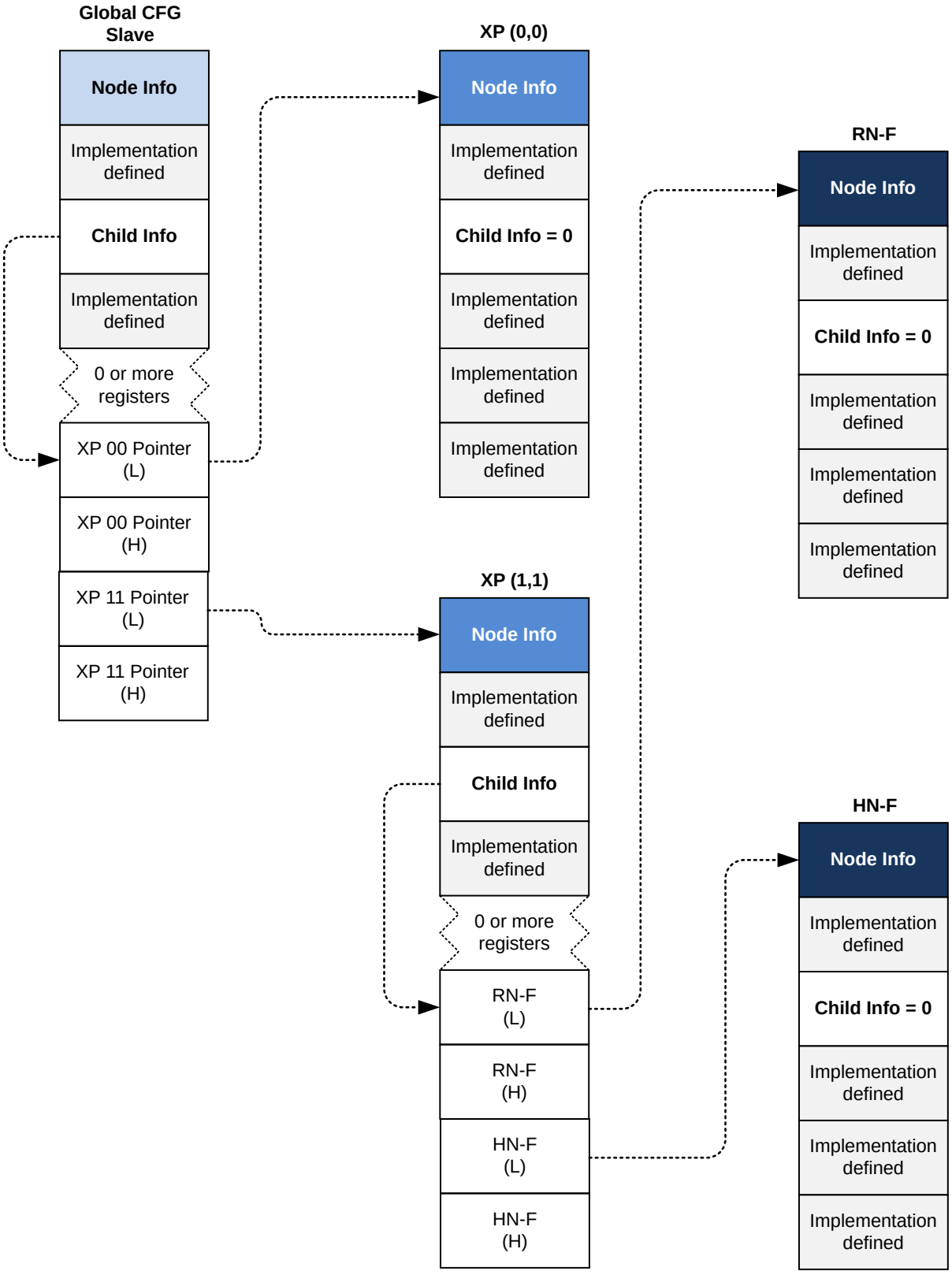
Figure 4-32: 2 × 2 discovery tree structure



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4.13 Link layer

CI-700 provides link initialization, flow-control, and link deactivation functionality at the RN-F and SN-F device interfaces.

This functionality comprises the following mechanisms:

- A link initialization mechanism by which the receiving device communicates link layer credits, on each CHI channel that is present, to a transmitting device.
- A flow-control mechanism by which the transmitting device uses link layer credits to send CHI flits. The transmitting device uses one credit per flit. The receiving device sends these credits back to the transmitting device, one at a time, after processing each flit. Subsequent flit transfers can then occur.

  
  Note

  This section refers to the credit roundtrip latency. This latency is measured in clock cycles, and is between:

  1. The time a transmitting device uses a link layer credit to send a flit to the receiving device.
  2. The earliest time when the transmitting device can receive that credit back from the receiving device and send a subsequent flit.

- A link deactivation mechanism. The transmitting device sends all unused link layer credits on each CHI channel back to the receiving device by sending corresponding link flits.

On flit upload channels, RN-F or SN-F is the transmitting device and CI-700 is the receiving device. On flit download channels, CI-700 is the transmitting device and RN-F or SN-F is the receiving device.

For a description of the functional requirements of the CHI link layer, see the *AMBA® 5 CHI Architecture Specification*.

4.13.1 Flit buffer sizing requirements

There are specific size requirements for the CI-700 flit buffers.

Flit buffer sizing at a receiving device is based on the following factors:

1. A transmitting device must be able to send flits continuously in a pipelined fashion without stalling because of insufficient link layer credits from the receiving device. This requirement ensures that the system can achieve the full link bandwidth. For a specific system, there is a minimum number of link layer credits that are required so that pipeline stalls can be prevented. You can use the credit roundtrip latency between the transmitting device and receiving device as a measure of the required number of link layer credits.
2. A receiving device must be able to accept and process as many flits as the number of link layer credits it has outstanding at the transmitting device. Therefore, the number of link layer credits that a receiving device sends must not exceed its flit buffering and processing capabilities.

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Therefore, flit buffer sizing and corresponding link layer crediting must reflect the credit roundtrip latency. If this requirement is met, the system can achieve optimal flit transfer bandwidth between transmitting and receiving devices. For more information about flit buffer sizing and link layer crediting for flit uploads and downloads at RN-F and SN-F interfaces, see the following sections:

- 4.13.2 Flit uploads from RN-F or SN-F on page 137
- 4.13.3 Flit downloads at RN-F or SN-F on page 137

4.13.2 Flit uploads from RN-F or SN-F

For flit uploads, the `RXBUF_NUM` parameter specifies the number of flit buffers in CI-700.

For more information about `RXBUF_NUM`, see 2.5 Device-level configuration parameters on page 21.

For optimal flit transfer bandwidth, this parameter must be set equal to the upload credit roundtrip latency, UpCrdLat<ch>. Use the following equation to calculate UpCrdLat<ch>:

UpCrdLat<ch> = UpCrdLatInt<ch> + UpCrdLatExt<ch>, where:

- <ch> is the CHI channel (REQ, RSP, SNP, or DAT).
- UpCrdLatInt<ch> is the upload credit latency inside CI-700. This latency is measured in clock cycles between the following time points:
  1. The time that the RN-F or SN-F asserts the RX<ch>FLITV input for a flit that is uploaded to CI-700.
  2. The earliest time when CI-700 asserts the RX<ch>LCRDV output to the RN-F or SN-F after the flit is processed and the credit sent back.

  At the RN-F and SN-F interfaces, UpCrdLatInt<ch> = 1 on all CHI channels.
- UpCrdLatExt<ch> is the upload credit latency outside CI-700. This latency is measured in clock cycles between the following time points:
  1. The time that CI-700 asserts the RX<ch>LCRDV output when the credit is sent back to the RN-F or SN-F.
  2. The earliest time when the RN-F or SN-F asserts the RX<ch>FLITV input when the credit is used to send a subsequent flit.

4.13.3 Flit downloads at RN-F or SN-F

For optimal flit downloads, the RN-F or SN-F must size its input buffers to reflect the download credit roundtrip latency, DnCrdLat<ch>.

Use the following equation to calculate DnCrdLat<ch>:

DnCrdLat<ch> = DnCrdLatInt<ch> + DnCrdLatExt<ch>, where:

- <ch> is the CHI channel (REQ, RSP, SNP, or DAT)
- DnCrdLatInt<ch> is the download credit latency inside CI-700. This latency is measured, in clock cycles, between the following time points:

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- The time that the RN-F or SN-F asserts the RX<ch>LCRDV input to CI-700
- The earliest time when CI-700 asserts the RX<ch>FLITV output to the RN-F or SN-F for a flit using that credit. At the RN-F or SN-F interfaces, DnCrdLatInt<ch> = 2 on all CHI channels.

- DnCrdLatExt<ch> is the download credit latency outside CI-700. This latency is measured, in clock cycles, between the following time points:
  - The time that CI-700 asserts the RX<ch>FLITV output for a flit downloaded to the RN-F or SN-F
  - The earliest time when RX<ch>LCRDV input is asserted when the RN-F or SN-F returns the corresponding credit to CI-700

4.14 Backward compatible RN-F support

CI-700 is compliant with CHI-E, but can also contain RN-Fs that comply with CHI-D, CHI-B, and CHI-C. Certain restrictions apply to how CI-700 handles transactions that are sent from older RN-Fs to maintain backwards compatibility.

The following table shows how all CI-700 blocks handle specific backward compatible CHI-B, CHI-C, CHI-D, and CHI-E features.

Table 4-36: All blocks backward compatibility

All blocks	CHI-B	CHI-C	CHI-D	CHI-E
DBID[9:8]	Must be `0b00`	Must be `0b00`	Can be used	Can be used
DBID[11:10]	Must be `0b00`	Must be `0b00`	Must be `0b00`	Can be used
SNP and DMT REQ **TxnID[9:8]**	Must be `0b00`	Must be `0b00`	Can be used	Can be used
SNP and DMT REQ **TxnID[11:10]**	Must be `0b00`	Must be `0b00`	Must be `0b00`	Can be used

Note

If RN-F **TxnID[9:8]** = `0b11`, DCT from a CHI-B, CHI-C, or CHI-D RN-F to a CHI-E RN-F cannot be done.

The following table shows how CI-700 HN-Fs handle specific backward compatible CHI-B, CHI-C, CHI-D, and CHI-E features.

Table 4-37: HN-F backward compatibility

HN-F protocol	CHI-B	CHI-C	CHI-D	CHI-E
Requests from RN-F	Supported	Supported	Supported	Supported
DMT	Yes	Yes	Yes	Yes
DCT	Yes	Yes	Yes	Yes
Separate response and data	No	Yes	Yes	Yes
SnpPreferUnique	No	No	No	Yes

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HN-F protocol	CHI-B	CHI-C	CHI-D	CHI-E
SnpQuery	No	No	No	Yes
New fields	MXP drives fixed values.	MXP drives fixed values.	MXP propagates new fields drives fixed values.	MXP to propagate

The following table shows how CI-700 DNs handle specific backward compatible CHI-B, CHI-C, CHI-D, and CHI-E features.

Table 4-38: DN backward compatibility

DN protocol	CHI-B	CHI-C	CHI-D	CHI-E
Requests from RN-F	Supported	Supported	Supported	Supported
CompDBID for DVM operations	No	No	No	No



In a system with heterogeneous components, the system configuration must determine the lowest common DVM specification that is supported in the system. In such a system, set the enable_8_4_termination bit in the por_dn_cfg_ctl register to 1.

If enable_8_4_termination is set to 1, the DN detects Arm®v8.4-A DVM operations, suppresses their propagation, and responds in a protocol-compliant manner. This behavior avoids deadlocks and denial of service.

The DN does not send any error indication or log errors.

4.15 PCIe integration

CI-700 supports integration of a PCIe *Root Complex* (RC) or *EndPoint* (EP).

4.15.1 PCIe topology requirements

There are specific topology rules that you must follow when integrating PCIe components with CI-700.

The following PCIe topology requirements apply:

- PCIe slaves must not be connected to HN-D
- PCIe slaves must not share HN-I with other non-PCIe slaves

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4.15.2 PCIe master and slave restrictions and requirements

There are restrictions on both the types and flow of transactions between PCIe devices and CI-700.



In this section, the term PCIe HN-I refers to an HN-I which has a PCIe slave that is connected to it. The term HN-I refers to all other HN-I.

CI-700 supports peer-to-peer PCIe traffic. This function allows one PCIe endpoint to communicate with another PCIe endpoint through the interconnect.

Transaction type restrictions

A PCIe master must not send any *Non-Posted Configuration and I/O Writes* (NPR-Wr) targeting CI-700.

Flow control requirements from CI-700 to PCIe slave

The PCIe slave must be able to sink at least one NPR-Wr from CI-700 sent on the PCIe HN-I AXI/ACE-Lite master port. This requirement guarantees that the PCIe HN-I AW channel remains unblocked. Therefore, *Posted Writes* (P-Wrs) from PCIe master targeting the downstream slave device can progress, as required by the PCIe ordering rules.

Flow control requirements from PCIe master to CI-700

If a *System Memory Management Unit* (SMMU) or GIC-ITS is in the path between the PCIe master interface and the RN-I slave interface, there are two possible options:

- *Non-Posted Reads* (NPR-Rds) from the PCIe master must not target any PCIe HN-I.
- Use a separate master interface port in the SMMU and GIC-ITS for translation table walks (TCU in MMU-500/GIC-600 and beyond). You can then connect this port to a different RN-I which does not send any requests to any PCIe HN-I. None of the masters that are connected to this RN-I can communicate with any PCIe HN-I.

4.15.3 System requirements for PCIe devices

There are certain system-level requirements that you must meet when integrating PCIe devices with CI-700. These requirements determine which CI-700 devices can handle certain request types and how PCIe and non-PCIe transactions must be handled.



In this section, the term PCIe HN-I refers to an HN-I which has a PCIe slave connected to it. The term HN-I refers to all other HN-Is.

CI-700 has the following system requirements for PCIe devices:

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- All non-PCIe I/O slave devices must complete all writes without creating any dependency on a transaction in the PCIe subsystem
- Your configuration might have an SMMU in the path between the PCIe master interface and the RN-I slave interface. If using this kind of configuration, table-walk requests from the SMMU can only be sent to memory through the HN-F or non-PCIe HN-I.
- Interrupt translation table walk requests from GIC-ITS can only be sent to memory through the HN-F or non-PCIe HN-I

There are certain programming requirements that your system must meet to ensure proper PCIe functionality. For more information, see 5.4.5 RN-I and HN-I PCIe programming sequence on page 1283.

4.16 Generic Interrupt Controller (GIC) communication over AXI4-Stream ports

CI-700 supports optional master and slave *AXI4-Stream* (A4S) ports on certain blocks for communication between a *Generic Interrupt Controller* (GIC) and CPUs. A4S ports are supported on RN-I, RN-D, and MXP device ports attached to RN-Fs. Certain requirements apply to the A4S routing and signaling.



If CAL is instantiated between RN-I or RN-D and an MXP, only a single A4S port is supported.

More system-level information is available in the *Arm® Neoverse™ N1 hyperscale reference design GIC-600 Integration using CMN-600 AXI4-Stream Interfaces White Paper* on request.

A4S routing

The A4S ports are addressed according to LDID, which are assigned sequentially from 0 to the number of A4S ports. To send a packet from one A4S port to the destination A4S port, the TDEST must be assigned to the LDID of the target A4S port. The discovery process returns the number of A4S ports and LDID information for each A4S port. The process returns this information by reading corresponding RN-I, RN-D, and XP unit information registers. For more information about the discovery process, see 4.12 Discovery on page 125.

Other requirements

The A4S master must assert **valid** irrespective of **ready** state to transmit data.

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4.17 Reliability, Availability, and Serviceability

The CI-700 *Reliability, Availability, and Serviceability* (RAS) features are implemented as a set of distributed logging and reporting registers and a central interrupt handling unit.

The distributed logging and reporting registers are associated with devices that can detect errors. The following CI-700 devices can detect errors:

- XP
- HN-I
- HN-F
- SBSX
- MTU

The central interrupt handling logic is in the HN-D.

Each device that can detect errors logs the error in local registers and sends error information to the central interrupt handling logic in the HN-D. The HN-D contains four sets of six error groups, which are based on the device type of the error source. The sets consist of a Secure and Non-secure group for errors, and a Secure and Non-secure group for fault-type errors. Each error group is represented in an *ERRor Group Status Register* (ERRGSR).

Error group, Secure
: por_cfgm_errgsr{0-5}

Fault group, Secure
: por_cfgm_errgsr{6-11}

Error group, Non-secure
: por_cfgm_errgsr{0-5}_NS

Fault group, Non-secure
: por_cfgm_errgsr{6-11}_NS

The following figure shows the six error groups, and the four respective interrupt request signals, with XP connections highlighted.

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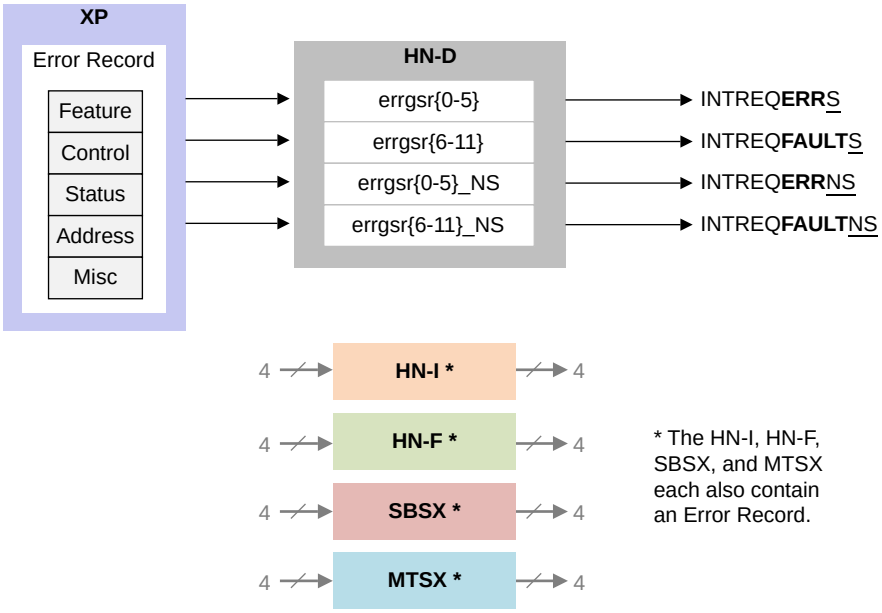
Figure 4-33: Error top-level diagram



The HN-I, HN-F, SBSX, and MTSX use the same input/output structure.

Each ERRGSR is partitioned according to device type, with a 64-bit vector representing the logical ID of each device instance. The following figure shows the partitioning.

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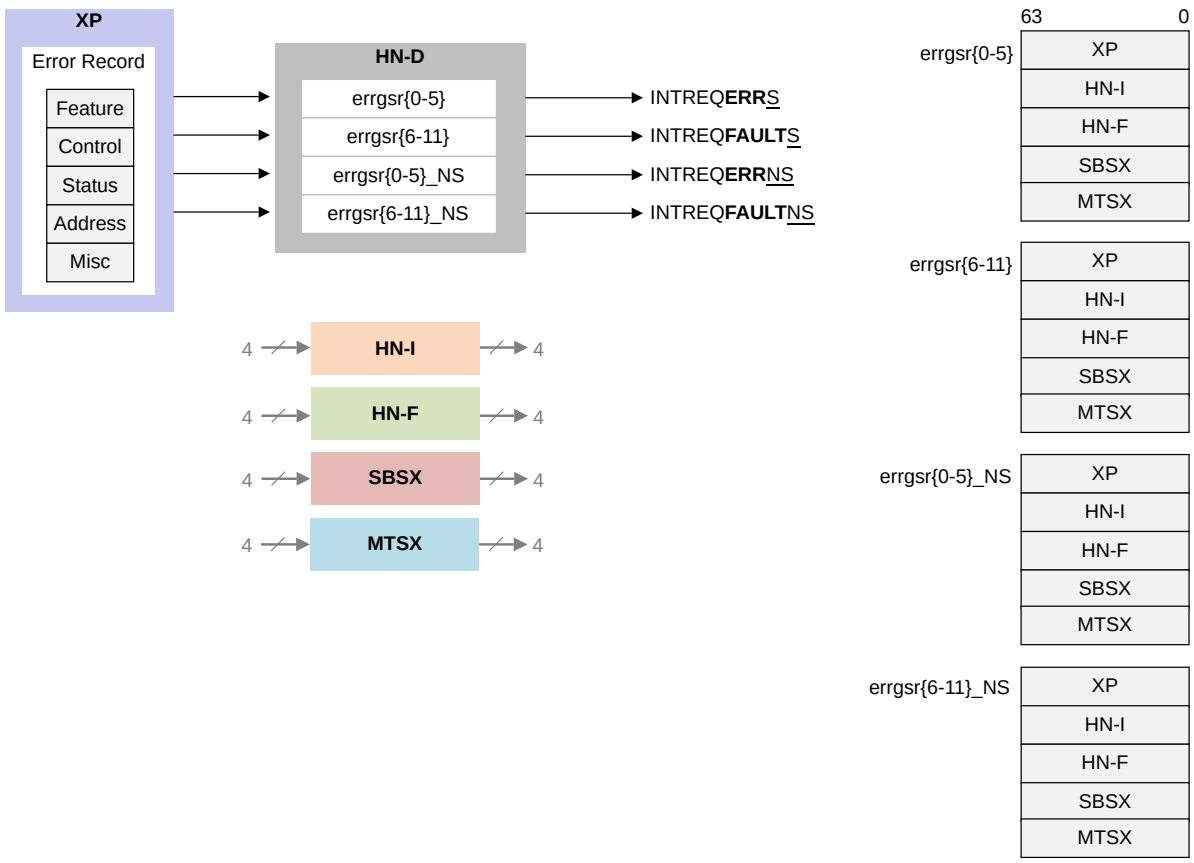
Figure 4-34: 256-bit error handling structure



Each device that can detect errors except MTSX has two sets of Error Record registers. The MTSX has four sets of Error Record registers. These registers contain the error type, along with other information such as the address and opcode. Error types include *Corrected Error* (CE), *Deferred Error* (DE), and *Uncorrected Error* (UE).

For more information on error types, refer to 4.17.1 Error types on page 145.

For register details, see 5.3 Register descriptions on page 207.

Error interrupt handler flow example

The following sequence of events and figure describe the process for determining the error source and type of an HN-F generating an interrupt request:

1. The HN-D generates an interrupt for one of the six error group types.
2. The error group indicates the error source device type, which can be:
   - XP
   - HN-I
   - HN-F, which is used in this case.

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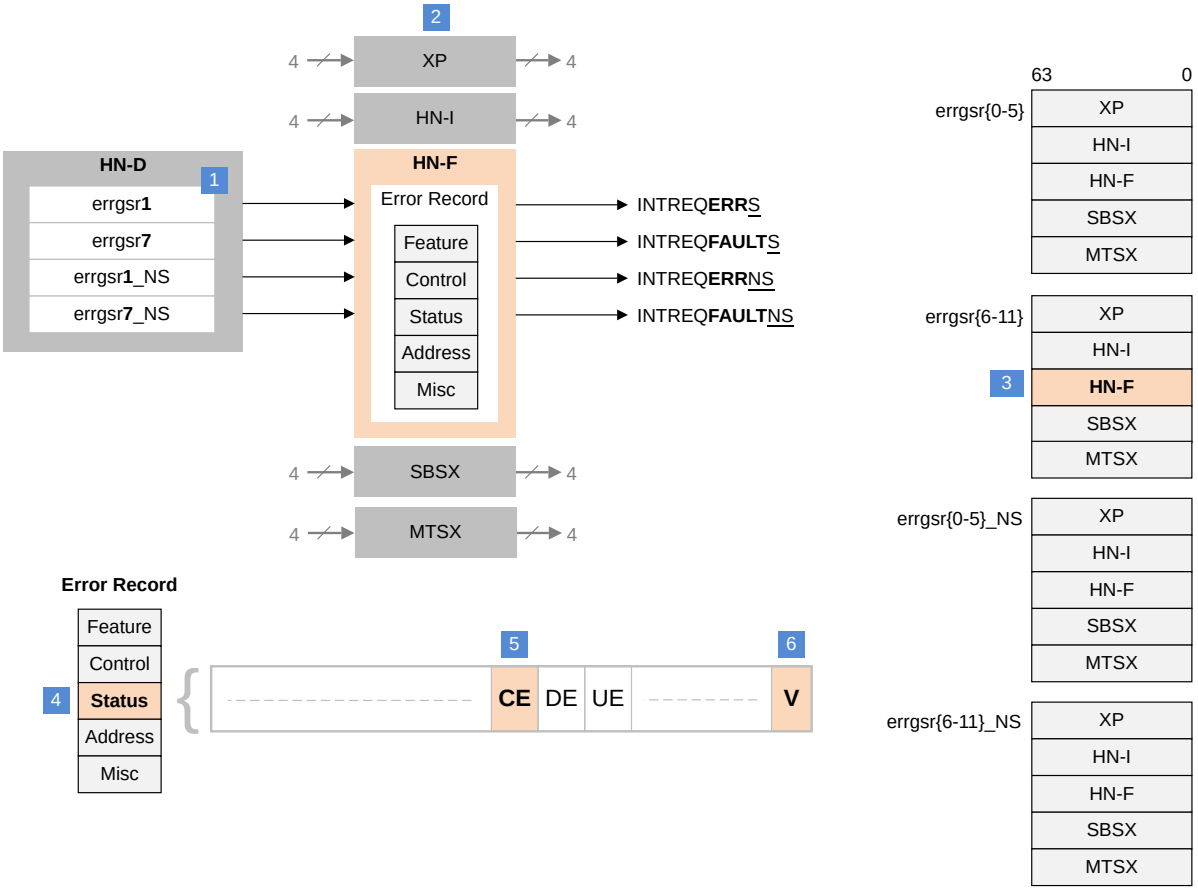
- SBSX
- MTSX

3. The bit location within the error group indicates the logical ID of that device type. In this case, it reveals an HN-F error, the HN-F Error Record Status block for this example.
4. The Status block of the Error Record for the specific XP, HN-I, HN-F, SBSX, or MTSX reveals the type of error.
5. The Address and Misc blocks of the Error Record provide further details regarding error root cause, in this case a Corrected Error.
6. The Valid bit is also asserted.
7. To clear the asserted interrupt on the pin, the valid bit of the error status has to be cleared.

Figure 4-35: Error interrupt handler flow example



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4.17.1 Error types

CI-700 supports several error types.

The supported errors are:

- *Corrected Error* (CE)
- *Deferred Error* (DE)
- *Uncorrected Error* (UE)


Note

CEs, DEs, and UEs can occur simultaneously.

There might be cases when an error occurs and sets the status register, but the interrupt reporting is not enabled. For other cases where the interrupt asserts, the interrupt request is generated immediately when enabled. Otherwise, if interrupt reporting is disabled, any interrupt is cleared and the error remains logged with UE, DE, and CE.


Note

If both ERRCTLR.UI (uncorrected interrupt) and ERRCTLR.FI (fault interrupt) are set and a UE occurs, both fault and error interrupts are delivered from CI-700.

Correctable errors

Single-bit *Error Correcting Code* (ECC) errors can be corrected using ECC or other methods. The system handles these errors by completing the following steps:

1. Detects the error and increments the ERRMISC.CEC counter. Sets ERRSTATUS.AV and ERRSTATUS.MV. Logs the attributes in the ERRADDR and ERRMISC registers.
2. If CEC counter overflowed, the system updates ERRSTATUS.V and ERRSTATUS.CE, and sets ERRMISC.CECOF.
3. Masks signaling of the error to the *RAS Control Block* (RCB) using ERRCTLR.CFI.
4. If there are multiple CEC overflows, then the system sets ERRSTATUS.OF.

Deferred errors

These errors are UEs that have the following properties:

- Detected in one node of CI-700, but the data is not used within the same node
- Poison bits are set for the data

The errors can be either fatal or non-fatal errors as described in this section. These errors are not correctable, but the system can operate for a time without being corrupted. These errors can be contained and the system might be able to recover through software intervention. They include:

- A data double bit ECC error in the SLC data RAM

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- Data check error detected in SLC

The system handles these errors by completing the following steps:

1. Logs the error information in the applicable ERRSTATUS, ERRADDR, and ERRMISC registers.
2. Sets ERRSTATUS.V and ERRSTATUS.DE.
3. Masks signaling of the error to the RAS control block using ERRCTLR.FI and ERRCTLR.UI.
4. If there are multiple DEs, then the system sets ERRSTATUS.OF.

Uncorrectable fatal errors

These errors are in the control logic at a node. Continuing operation might corrupt the system beyond recovery. They include:

- A double-bit ECC error in SLC tag
- Flit parity error
- *Non-data Error* (NDE) in a response packet

The system handles these errors by completing the following steps:

1. Logs the error information in the applicable ERRSTATUS, ERRADDR, and ERRMISC registers.
2. Sets ERRSTATUS.V and ERRSTATUS.UE.
3. Masks signaling of the error to the RAS control block using ERRCTLR.UI.
4. If there are multiple UEs, then the system sets ERRSTATUS.OF.

A component might not respond to further messages after an error is signaled. In this case, for the error handling routine to be successful, the component must still respond to configuration access requests from the configuration bus.

CI-700 follows the *Arm® Reliability, Availability, and Serviceability (RAS) Specification Armv8, for the Armv8-A architecture profile* for mapping of the different error types to the type of interrupt. The following table summarizes the mapping of various error types to the interrupt type.

Table 4-39: Mapping of error types

Interrupt type	Error type		
	Uncorrected error	Detected error	Corrected error
Fault handling	Yes (if ERRCTLR.FI==1)	Yes (if ERRCTLR.FI==1)	Yes (if ERRCTLR.CFI==1)
Error recovery	Yes (if ERRCTLR.UI==1)	No	No

4.17.2 Error detection and deferred error values

For XP, the default values of *Error Detection* (ED) and DE depend on build time parameters.

The default values of UI, FI, and CFI are `2'b10`, which enables control for the interrupt generation.

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Table 4-40: Default values of ED and DE for XP

POR_FLIT_PAR_EN	POR_DATACHECK_EN	MXP_DEV_DATACHECK_EN		ED	DE
		P0	P1		
0	0	0	0	2'b00	2'b00
0	1	0	0	2'b01	2'b01
		0	1	2'b01	2'b01
		1	0	2'b01	2'b01
		1	1	2'b00	2'b00
1	0	0	0	2'b01	2'b00
1	1	0	0	2'b01	2'b01
		0	1	2'b01	2'b01
		1	0	2'b01	2'b01
		1	1	2'b01	2'b00

For SBSX, if the AXDATAPOISON_EN parameter is not set, the default values of ED and DE are 2'b01. If the parameter is set, the default values are 2'b00.

For HN-I and HN-F, the default values of ED and DE are always 2'b01.

All fields are required, even though only HN-F has CE counters that are implemented in ERRMISC.

The default values of UI, FI, and CFI must be 2'b10, indicating that the interrupt generation is controllable.

4.17.3 Error detection, signaling, and reporting

Each CI-700 component that is connected to a configuration bus can be included in the local error reporting mechanism.

The error handling protocol is as follows:

- Error overflow
- ERRSTATUS.OF value after errors
- ERRMISC fields and register bits

Error overflow

The overflow is set when different types of errors are detected. It is also asserted when multiple errors of equal priority are detected.

0b1 More than one error has been detected.
0b0 Only one error of the most significant type that ERRSTATUS.{UE, CE, DE} describes has been detected.

This bit is read/write-one-to-clear.

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Note

ERRSTATUS.OF is only for the highest priority error. For example, if another DE follows the first DE, ERRSTATUS.OF is set. When the next UE happens, ERRSTATUS.OF is cleared. ERRSTATUS.OF is cleared because UE is the highest priority error in the system, and is the first occurrence of UE.

The following table shows the value of ERRSTATUS.OF after errors occur at t0, t1, and t2.

Table 4-41: ERRSTATUS.OF value after errors

Error at			Status of OF after error		
t0	t1	t2	t0	t1	t2
CE	CE	CE	0	1	1
CE	CE	DE	0	1	0
CE	CE	UE	0	1	0
CE	DE	CE	0	0	0
CE	DE	DE	0	0	1
CE	DE	UE	0	0	0
CE	UE	CE	0	0	0
CE	UE	DE	0	0	0
CE	UE	UE	0	0	1
DE	CE	CE	0	0	0
DE	CE	DE	0	0	1
DE	CE	UE	0	0	0
DE	DE	CE	0	1	1
DE	DE	DE	0	1	1
DE	DE	UE	0	1	0
DE	UE	CE	0	0	0
DE	UE	DE	0	0	0
DE	UE	UE	0	0	1
UE	CE	CE	0	0	0
UE	CE	DE	0	0	0
UE	CE	UE	0	0	1
UE	DE	CE	0	0	0
UE	DE	DE	0	0	0
UE	DE	UE	0	0	1
UE	UE	CE	0	1	1
UE	UE	DE	0	1	1
UE	UE	UE	0	1	1

ERRMISC fields

ERRMISC is the Secondary Error Syndrome Register. The fields of this register differ for ECC, parity, and other errors. The following table summarizes the valid fields for each unit.

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Error log clearing

In addition to the Error Syndrome Registers, each component has a write-only Error Syndrome Clear Register. Write the applicable mask bits to clear the first_err_vld and mult_err bits of the Error Syndrome 0 Register.

4.17.4 Error reporting rules

CI-700 uses specific error reporting rules, concerning which errors must be reported and propagated.

The rules regarding error reporting in CI-700 are:

- Any error originating in CI-700 is reported
- Any error originating outside CI-700 but corrupting CI-700 is reported
- If a response packet from outside CI-700 does not propagate the response any further, the HN-I can report an error in the response packet
- All non-posted write errors are propagated where possible

4.17.5 HN-F error handling

Errors are reported at the HN-F for various reasons.

The HN-F detects:

- ECC errors in SF tag, SLC tag, and data RAMs.
- Data check and poison errors on DAT flits.
- *Non-data Errors* (NDEs) on responses.

ECC errors in SF Tag, SLC Tag, and data RAMs

HN-F detects single-bit and double-bit ECC errors in the SF tag, SLC tag, and data RAMs. It can correct single-bit ECC errors. Such errors are logged and reported as CEs.

The source of the double-bit ECC errors determines how they are handled.

SLC data RAM

- Logged and reported as DEs.
- Propagated to the data consumer in the form of data poison.

SF tag RAM

- Logged and reported as DEs.
- Not propagated to the requestor.
- The SF tag RAM in the HN-F is disabled following the first occurrence of the double-bit ECC error.

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SLC tag RAM

- Fatal error.
- Logged and reported as UEs.
- Propagated to the requestor as NDEs in the responses.

Data check and poison errors on DAT flits

If data the HN-F allocates data, then it detects data check errors and poison error on the data flits. In such cases, HN-F logs and reports the data check error as a DE. If HN-F allocated the data in SLC data RAM, it converts the data check error into data poison for all subsequent requests to this cache line.

If por_hnf_aux_ctl.hnf_poison_intr_en == 1, then the poison errors originating from HN-F are logged and reported as UEs.

NDEs on responses

HN-F can receive NDEs from other data and response sources such as RN-F, RN-I, and SN-F. If the cache line was allocated in SLC data RAM, it is logged and reported as a UE. If the cache line is not allocated in HN-F SLC, it propagates the errors to the requestor as an NDE.

4.17.6 HN-I error handling

Errors are reported at the HN-I for various reasons.

4.17.6.1 Request errors at HN-I

The HN-I detects errors on receiving various request types and sends an NDE response to the requesting RN.

The HN-I logs request information in the error logging registers: por_hni_erraddr(_NS) and por_hni_errmisc(_NS). They are marked as DEs in the error status register, por_hni_errstatus(_NS). The HN-I detects errors on receiving the following request types:

- Coherent read
- CleanUnique/MakeUnique
- Coherent/CopyBack write
- Atomic
- Illegal configuration read or write, HN-D only

The reqerr_cohreq_en configuration bit in the por_hni_cfg_ctl register enables or disables the sending of NDE responses and logging of error information for following request types. By default, this bit is enabled. It can only be programmed during boot time to any one of the following:

- Coherent read

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- CleanUnique/MakeUnique
- Coherent/CopyBack write

The following table lists all the requests that an HN-I detects as errors and the support of reqerr_cohreq_en.

Table 4-42: HN-I request errors and support for configuration bit

Request type	Reqerr_cohreq_en controls sending of NDE and log error
Coherent read	Yes
CleanUnique/MakeUnique	Yes
Coherent/CopyBack write	Yes
Atomics	No
Illegal configuration read or write	No

- Coherent reads are downgraded to ReadNoSnp and sent downstream, AXI or ACE-Lite slave
- Coherent and Copyback writes are downgraded to WriteNoSnp and sent downstream, AXI or ACE-Lite slave
- Illegal configuration read is sent as ReadNoSnp to downstream AXI or ACE-Lite slave
- CleanUnique, MakeUnique, atomics, and illegal configuration writes are handled within HN-I
- StashOnceShared, StashOnceUnique, and PrefetchTgt are completed within HN-I without any errors

4.17.6.2 Data errors at HN-I

The HN-I only detects errors on write data if it does not detect an error on that request.

The following provides an overview of AXI and ACE-Lite write requests and configuration write requests, with no request error:

- For AXI and ACE-Lite write requests with no request error, when they receive poison error on data, the HN-I detects the error. If downstream does not support poison, the HN-I logs the request information in por_hni_erraddr(_NS) and por_hni_errmisc(_NS). The write requests are marked as UEs in the error status register, por_hni_errstatus(_NS).
- For configuration write requests with no request error, on receiving write data with partial ByteEnable error, data check error, or poison, HN-I detects and sends an NDE response to the requesting RN. It logs the SrcID and TxnID of the request and drops the write. They are marked as DEs in the error status register, por_hni_errstatus(_NS).


Note

StashOnceShared, StashOnceUnique, and PrefetchTgt are completed within HN-I without any errors.

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4.17.6.3 Response errors at HN-I

The HN-I only detects errors on write response if it does not detect an error on that request.

To summarize:

- For AXI or ACE-Lite write requests with early completions from HN-I and no request error, HN-I detects the error when it receives the following error response types on the downstream write response (**BRESP**):
  - *Slave Error* (SLVERR)
  - *Decode Error* (DECERR)

  HN-I logs request information in por_hni_erraddr(_NS) and por_hni_errmisc(_NS). They are marked as UEs in the error status register, por_hni_errstatus(_NS).
- For AXI or ACE-Lite write requests with downstream completions and no request error, SLVERR, or DECERR on downstream write response (**BRESP**) are passed on to the requesting RN as CHI DEs or NDEs.
- For AXI or ACE-Lite read requests, SLVERR and poison (if supported by downstream) are both converted to poison within the CI-700 system. This conversion occurs independent of error on request. DECERRs on downstream read responses are passed on to the requesting RN.

4.17.6.4 HN-I summary on sending NDE and DE

The HN-I sends NDE scenarios for certain situations.

The HN-I sends NDE in the following cases:

- Request error:
  - Coherent read, if reqerr_cohreq_en is set to 1
  - CleanUnique/MakeUnique, if reqerr_cohreq_en is set to 1
  - Coherent/CopyBack write, if reqerr_cohreq_en is set to 1
  - Atomic
  - Illegal configuration read or write, HN-D only


Note

For the legal format of configuration read/write request, refer to 5.1.5 Requirements of configuration register reads and writes on page 181.

- Write data error for configuration write request, HN-D only:
  - Partial ByteEnable error
  - Data check error
  - Poison

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- AXI or ACE-Lite response error:
  - DECERR on *downstream write response*, **BRESP**, for writes with downstream completions
  - DECERR on *downstream read response*, **RRESP**

The HN-I sends DE in the following cases:

- AXI or ACE-Lite response error:
  - SLVERR on **BRESP** for writes with downstream completions

4.17.6.5 HN-I summary on logging errors

The HN-I logs an error as deferred or uncorrected in certain conditions.

Deferred errors

The HN-I logs an error as deferred in the following cases:

- Request error:
  - Coherent read, if reqerr_cohreq_en is set to 1
  - CleanUnique/MakeUnique, if reqerr_cohreq_en is set to 1
  - Coherent/CopyBack write, if reqerr_cohreq_en is set to 1
  - Atomic
  - Illegal configuration read or write


Note

For the legal format of a configuration read or write request, see 5.1.5 Requirements of configuration register reads and writes on page 181.

- Write data error for configuration write request:
  - Partial ByteEnable error
  - Data check error
  - Poison error

Uncorrected errors

The HN-I logs an error as uncorrected in the following cases:

- Write data error for AXI or ACE-Lite write requests:
  - Poison error on data if downstream does not support poison
- AXI or ACE-Lite write response error:
  - SLVERR or DECERR on **BRESP** for writes that were sent early completions

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4.17.7 SBSX error handling

This section describes how errors are handled at the SBSX.

If the following circumstances are both true, then the SBSX detects and logs errors:

- The AXI memory controller downstream of SBSX does not support POISON, indicated by por_sbsx_unit_info.axdata_poison_en = 0
- CHI write data has poison set



SBSX does not have opcode-based request and response error class as does HN-I.

The following table shows the SBSX summary on sending an NDE or DE.

Table 4-43: SBSX summary on sending NDE or DE

Case number	Source of error	SBSX error response
1	Decode error on **RDATA** from AXI side	NDE on COMP_DATA on CHIE side
2	Slave error on **RDATA** from AXI side	Poison on COMP_DATA on CHIE side
3	Decode error on **BRESP** from AXI side	NDE on COMP for CMOs or writes with EWA = 0
4	Slave error on **BRESP** from AXI side	DE on COMP for CMOs or writes with EWA = 0

4.17.8 MTU error handling

Errors at MTU are reported for various reasons. All the errors are logged in MTU RAS registers.



Both the MTU and SBSX error handling functionality are combined to provide the full MTSX error handling functionality. When an MTSX error is reported, both SBSX and MTU RAS registers must be checked to determine the source of the error. Also, when clearing the error, the correct set of RAS registers must be cleared. For more information about SBSX error handling functionality, see 4.17.7 SBSX error handling on page 154.

When multiple MTU errors are detected in the same cycle, the RAS registers can only store the details of one error. Which error is saved depends on the priority of the error.

The following table shows the priority of the *Uncorrectable Errors* (UEs) that are reported at the MTU:

Table 4-44: Priority-ranking of UEs at the MTU

UE type	Priority
Tag control RAM double-bit error	1 (highest)

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UE type	Priority
Tag data RAM double-bit error	2
AXI-R slave error	3
AXI-R decode error	4
AXI-R poison	5
AXI-R DataCheck	6
AXI-B slave error	7
AXI-B decode error	8
Data PA out of bounds (if enabled)	9 (lowest)

The following table shows the priority of the *Correctable Errors* (CEs) that are reported at the MTU:

Table 4-45: Priority-ranking of CEs at the MTU

UE type	Priority
Tag control RAM single-bit error	1 (highest)
Tag data RAM single-bit error	2 (lowest

The following table shows the only circumstances where MTU sends an NDE response back to the requestor and how the MTU responds.

Table 4-46: Conditions when MTU returns NDE response to the requestor

Source of error	MTU error response
Tag RAM control double-bit error for read request	NDE on COMP_DATA on CHI-E
Tag RAM control double-bit error for tag match request	NDE on match response on CHI
AXI-R decode error for read request	NDE on COMP_DATA on CHI-E
AXI-R decode error for tag match request	NDE on match response on CHI-E
AXI-R decode error for CMO with late completion	NDE on COMP on CHI-E
AXI-B decode error for CMO with late completion	NDE on COMP on CHI-E

The MTU tag data RAM handles specific error types in the following way:

- Single-bit ECC errors are reported and logged.
- Corrected data after single-bit ECC error is written back into the same way.
- Double-bit ECC errors are reported and logged.
- Data with double-bit ECC is marked invalidated. This behavior could mean that modified tags are lost.

The MTU tag control RAM handles specific error types in the following way:

- Single-bit ECC errors are reported and logged.
- Corrected control bits after single-bit ECC error are written back into same way.
- Double-bit ECC errors are fatal.
- Double-bit ECC errors are reported and logged.

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- RAM way with control double-bit ECC is marked invalidated. This behavior could mean that modified tags are lost.

The MTU handles AXI read response (denoted as AXI-R) errors in the following way:

- Slave, poison, and data check errors are reported and logged. These errors are not propagated any further.
- Decode errors are reported and logged. MTU propagates the error to the requestor for tag read (transfer), tag match (match response), and CMO (if late completion).
- If AXI read is required to merge with tag update, modified tags could be lost.

The MTU handles AXI write response (denoted as AXI-B) errors in the following way:

- Slave, poison, and data check errors are reported and logged. These errors are not propagated any further.
- Decode errors are reported and logged. MTU propagates the error to the requestor for late completion CMO.

4.17.9 RN-I error handling

RN-I does not report any errors. When a parity error is detected in the *Read Data Buffer* (RDB) RAMs, RN-I or RN-D propagates the error on AXI R channel as **RPOISON** or **RRESP**.

4.17.10 XP error handling

Errors are reported at the XP for various reasons.

The following errors are detected in the XP:

- Flit parity error
- Data check error, DAT channel only

Flit parity error

Flit parity is generated on a flit upload from a device port to a mesh port, for both internal and external devices. Flit parity check is done on a flit download from a mesh port to a device port.

Flit parity is not generated or checked when a flit is bypassed or looped back across the device ports on the same XP.

Data check error

Data check is enabled in the XP using the `DATACHECK_EN` parameter.

Data check, Data Byte Parity, bits are generated corresponding to each byte of data on a DAT flit upload from a device port when the corresponding device does not support data check. Data check support is indicated by `DEV_DATACHECK_EN` = 0.

Data check is accomplished on a flit download to a device which does not support data check.

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Data check bits are generated and checked when a DAT flit is bypassed or looped back across the device ports on the same XP when the corresponding devices involved do not support data check.

Error reporting and logging

Flit parity and data check errors are reported to the RCB. The following table contains flit fields that are logged in the XP configuration register.

Table 4-47: XP configuration register flit fields

Error source	Errstatus					Errmisc			
-	DE	CE	MV	UE	V	ERRSRC	SRCID	OPCODE	TGTID
Data Parity P0 REQ channel	1	0	1	0	1	5'b00000	v	v	v
Data Parity P1 REQ channel	1	0	1	0	1	5'b00001	v	v	v
Data Parity P2 REQ channel	1	0	1	0	1	5'b00010	v	v	v
Data Parity P3 REQ channel	1	0	1	0	1	5'b00011	v	v	v
Data Parity P4 REQ channel	1	0	1	0	1	5'b00100	v	v	v
Data Parity P5 REQ channel	1	0	1	0	1	5'b00101	v	v	v
Data Parity P0 RSP channel	1	0	1	0	1	5'b01000	v	v	v
Data Parity P1 RSP channel	1	0	1	0	1	5'b01001	v	v	v
Data Parity P2 RSP channel	1	0	1	0	1	5'b01010	v	v	v
Data Parity P3 RSP channel	1	0	1	0	1	5'b01011	v	v	v
Data Parity P4 RSP channel	1	0	1	0	1	5'b01100	v	v	v
Data Parity P5 RSP channel	1	0	1	0	1	5'b01101	v	v	v
Data Parity P0 SNP channel	1	0	1	0	1	5'b10000	v	v	0
Data Parity P1 SNP channel	1	0	1	0	1	5'b10001	v	v	0
Data Parity P2 SNP channel	1	0	1	0	1	5'b10010	v	v	0
Data Parity P3 SNP channel	1	0	1	0	1	5'b10011	v	v	0
Data Parity P4 SNP channel	1	0	1	0	1	5'b10100	v	v	0
Data Parity P5 SNP channel	1	0	1	0	1	5'b10101	v	v	0
Data Parity P0 DAT channel	1	0	1	0	1	5'b11000	v	v	v
Data Parity P1 DAT channel	1	0	1	0	1	5'b11001	v	v	v
Data Parity P2 DAT channel	1	0	1	0	1	5'b11010	v	v	v
Data Parity P3 DAT channel	1	0	1	0	1	5'b11011	v	v	v
Data Parity P4 DAT channel	1	0	1	0	1	5'b11100	v	v	v
Data Parity P5 DAT channel	1	0	1	0	1	5'b11101	v	v	v
FLIT Parity P0 REQ channel	0	0	1	1	1	5'b00000	v	v	v
FLIT Parity P1 REQ channel	0	0	1	1	1	5'b00001	v	v	v
FLIT Parity P2 REQ channel	0	0	1	1	1	5'b00010	v	v	v
FLIT Parity P3 REQ channel	0	0	1	1	1	5'b00011	v	v	v
FLIT Parity P4 REQ channel	0	0	1	1	1	5'b00100	v	v	v
FLIT Parity P5 REQ channel	0	0	1	1	1	5'b00101	v	v	v
FLIT Parity P0 RSP channel	0	0	1	1	1	5'b01000	v	v	v
FLIT Parity P1 RSP channel	0	0	1	1	1	5'b01001	v	v	v
FLIT Parity P2 RSP channel	0	0	1	1	1	5'b01010	v	v	v

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Error source	Errstatus					Errmisc			
FLIT Parity P3 RSP channel	0	0	1	1	1	5'b01011	v	v	v
FLIT Parity P4 RSP channel	0	0	1	1	1	5'b01100	v	v	v
FLIT Parity P5 RSP channel	0	0	1	1	1	5'b01101	v	v	v
FLIT Parity P0 SNP channel	0	0	1	1	1	5'b10000	v	v	0
FLIT Parity P1 SNP channel	0	0	1	1	1	5'b10001	v	v	0
FLIT Parity P2 SNP channel	0	0	1	1	1	5'b10010	v	v	0
FLIT Parity P3 SNP channel	0	0	1	1	1	5'b10011	v	v	0
FLIT Parity P4 SNP channel	0	0	1	1	1	5'b10100	v	v	0
FLIT Parity P5 SNP channel	0	0	1	1	1	5'b10101	v	v	0
FLIT Parity P0 DAT channel	0	0	1	1	1	5'b11000	v	v	v
FLIT Parity P1 DAT channel	0	0	1	1	1	5'b11001	v	v	v
FLIT Parity P2 DAT channel	0	0	1	1	1	5'b11010	v	v	v
FLIT Parity P3 DAT channel	0	0	1	1	1	5'b11011	v	v	v
FLIT Parity P4 DAT channel	0	0	1	1	1	5'b11100	v	v	v
FLIT Parity P5 DAT channel	0	0	1	1	1	5'b11101	v	v	v

If the device supports Poison, indicated by `DEV_POISON_EN` = 1, the Datacheck error is factored in the POISON field of the DAT flit. Else, it is factored in as DataError in the RESPERR field.

4.18 Transaction handling

The handling of certain CHI transaction types and fields differs according to the CI-700 device type.

Some devices fully support certain transaction types or fields, whereas others do not do any processing of those transactions. Furthermore, some transaction types are unsupported, such as barriers.

4.18.1 Atomics

CI-700 supports atomic accesses to both cacheable and non-cacheable memory locations.

4.18.1.1 Atomic requests in HN-F

The HN-F completes all CHI atomic requests that it receives, both for cacheable and non-cacheable transactions.

For cacheable transactions, the HN-F completes any appropriate coherent actions and, if necessary, obtains the targeted cache line from memory. The HN-F then completes the required atomic operation and issues the appropriate response, with or without data.

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For non-cacheable transactions, the HN-F does not send an atomic request to the SN. As the final PoS/PoC for all memory traffic, the HN-F is able to process the transaction in the following way:

1. Issue a read to the SN
2. Atomically update the copy of the data in the HN-F
3. Write back the result to the SN

This approach means that the SN never receives CHI atomic requests, as the HN-F completely handles the requests.

4.18.1.2 Atomic requests in SN

The SN node (CHI memory controller, SBSX bridge, or MTSX bridge) does not process atomic requests.

4.18.1.3 Atomic requests in HN-I

The HN-I does not complete atomic transactions.

On receiving an atomic request, the HN-I generates an appropriate error response to the originating master.

4.18.1.4 Atomic requests in RN-I and RN-D

RN-I and RN-D support atomic transactions in CI-700. These nodes can receive atomics from ACE5-Lite and AXI5 masters, and translate them on CHI before sending them to HN-F or HN-I nodes.

Atomics and write transactions share a write tracker for processing in RN-I and RN-D.


Note

For atomic transactions arriving at RN-I and RN-D from ACE5-Lite and AXI5 masters, all write strobes within **AWSIZE** must be set. RN-I and RN-D do not allow sparse write strobes for atomic transactions.

4.18.2 Exclusive accesses

CI-700 supports exclusive accesses to both Shareable and Non-shareable locations.

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4.18.2.1 Exclusive accesses in HN-F

The HN-F supports exclusive access on ReadNoSnp, WriteNoSnp, ReadShared, ReadClean, ReadNotSharedDirty, and CleanUnique transactions to any address that maps to the HN-F.

RNs generate ReadNoSnp and WriteNoSnp exclusives for memory locations that are marked non-cacheable or device. ReadShared, ReadClean, ReadNotSharedDirty, and CleanUnique exclusives are used for shareable and coherent memory locations. Each HN-F partition includes 64 exclusive monitors for tracking of these transaction types. Each monitor can act as both a PoC monitor and System monitor, as the *AMBA® 5 CHI Architecture Specification* defines.

Only 64 unique logical threads, which are designated by a unique combination of SrcID and LPID, can concurrently access the HN-F exclusive monitors.

4.18.2.2 Exclusive accesses in HN-I

HN-Is support exclusive access on ReadNoSnp and WriteNoSnp transactions to any address that maps to an HN-I.

Each HN-I partition includes exclusive monitors, as defined in the *AMBA® 5 CHI Architecture Specification*, for tracking of these transaction types. The number of monitors is specific to the configuration and is determined by the number of RN-Fs, RN-Is, and RN-Ds in the configuration. The number of monitors determines the number of unique logical threads that can concurrently access the HN-I system exclusive monitors. These threads can be either processor or device threads, and are designated by a unique combination of SrcID and LPID.

All exclusives targeting the HN-I are terminated at the HN-I and are not propagated downstream. Exclusives are terminated regardless of the value of the HN-I PoS control register and auxiliary control register.

4.18.2.3 Exclusive accesses in RN-I and RN-D

RN-I supports up to two active exclusive threads at any given AXI port. To differentiate the exclusive threads, RN-Is provide a per port 11-bit mask to extract the bit from **AxID**.

The 11-bit mask por_{rni, rnd}_s<X>_port_control can be found in the respective RN-I and RN-D AXI port control registers.

4.18.3 Barriers

Barriers were deprecated from CHI-B onwards. All masters (fully coherent and I/O coherent) must handle barriers at the source.

When memory barrier ordering or completion guarantees are required, masters must wait for the responses from all required previous transactions that are issued into the interconnect. No barrier requests can be issued into the interconnect.

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All requesting devices that are attached to an interconnect must have a configuration option or strap that prevents issuing of any barriers. If a barrier is issued into the interconnect, the results are unpredictable.


Note

The DVM_SYNC command, the DVM synchronization that might be initiated by an Arm DSB instruction, is sent to the DVM block, and executes appropriately.

For more information about barriers, see the *AMBA® 5 CHI Architecture Specification* and the *AMBA® AXI and ACE Protocol Specification*.

4.18.4 Distributed Virtual Memory messages

If an RN-F supports *Distributed Virtual Memory* (DVM) messages, it can send DVM requests and receive DVM snoops.


Note

If CI-700 is in DSA-F mode, then DVM messages are not supported.

A DVM message from an RN-F is sent to the HN-D. On receiving the DVM message, the HN-D:

- Forwards the DVM message as a snoop to the participating RNs. To do this action, the HN-D uses a static list to replace the DVM Domain Control register used with legacy products.
- Collects the individual snoop responses
- Sends a single response back to the RN-F that originated the DVM message transaction

The **SYSCOREQ**/**SYSCOACK** mechanism provides proxy snoop responses in scenarios when the RN is powered down. For more **SYSCOREQ**/**SYSCOACK** information, refer to 4.2.8 RN entry to and exit from snoop and DVM domains on page 71.


Note

- An RN that issues DVM messages must also be able to receive DVM messages. If this requirement is violated, the system must not rely on the DVM message causing any DVM snoops.
- An RN-F can issue only one outstanding DVMOp (sync).

For more information about DVM messages, see the *AMBA® 5 CHI Architecture Specification*.

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4.18.5 Completer Busy indication

Transaction completers can use the Completer Busy (CBusy) field to indicate their current level of activity. RNs use this indication to determine whether to throttle outgoing traffic.

CI-700 implements the CBusy indication function in the following node types:

- HN-F
- SBSX
- MTSX

HN-I and HN-D always drive the CBusy values as `0b000`.

HN-F CBusy

HN-F uses the *Point-of-Coherency Queue* (POCQ) occupancy level to indicate its current activity level. The following table shows the default CBusy values for a 32 entry POCQ. These values represent the default HN-F CBusy response behavior to RNs.

Table 4-48: HN-F POCQ CBusy thresholds

CBusy[2:0]	Tracker occupancy level
`0b011`	≥24
`0b010`	≥16
`0b001`	≥8
`0b000`	<8

HN-F also supports a CBusy multi-source mode. The CBusy[2] bit indicates that multiple sources, or RNs, have outstanding requests pending in the HN-F POCQ. HN-F also supports a mode where, when calculating CBusy[2], it excludes outstanding RN-I requests in the POCQ. This mode is enabled if the hnf_cbusy_mtbit_exclude_rni field of the por_hnf_cbusy_limit_ctl register is set to `0b1`. If this field is set, then HN-F ignores outstanding requests from the RN-I while calculating the CBusy[2] value.

SBSX and MTSX CBusy

SBSXs and MTSXs only drive CBusy on returning **TXDAT** flits targeting RNs. These nodes use two hierarchical trackers to drive the CBusy field: ReqTracker and DART. The CBusy field reflects the occupancy levels of both trackers combined. Similar to HN-F, the activity thresholds are programmable. The following table shows the default occupancy threshold for 96 entry trackers.

Table 4-49: SBSX and MTSX tracker CBusy thresholds

CBusy[2:0]	Tracker occupancy level
`0b011`	≥72
`0b010`	≥48
`0b001`	>24
`0b000`	<24

SBSXs and MTSXs do not use the multi-source mode bit, so CBusy[2] is always set to `0b0`.

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4.18.5.1 Advanced CBusy handling in HN-F

CI-700 HN-F supports advanced CBusy handling and request throttling to SN-F.

HN-F to RN CBusy handling

The responses that are sent from HN-F to RN through RSP and DAT channels carry CBusy values. HN-F has multiple different modes to determine how the CBusy values are specified in the response messages.

HN-F can be configured to respond to RNs with a CBusy value that reflects one of the following options:

- Total number of outstanding requests in the HN-F POCQ.
- Independent CBusy values for reads and writes:

  CompData type requests (All Read* requests)

  CBusy value is based on number of outstanding reads in the POCQ.

  Comp type requests (writes, Evict, atomics, CMOs)

  CBusy value is based on number outstanding writes in the POCQ.
- Return SN-F CBusy value instead of returning value that is based on HN-F POCQ:
  - Read requests receive the read CBusy of the SN-F.
  - Write requests receive the write CBusy of the SN-F.
- Return whichever CBusy value is the highest between HN-F POCQ and SN-F.

Comp type requests can be further filtered into the following categories:

- CopyBack type requests (Evict, WriteClean, WriteEvictFull, or WriteBack*).
- NonCopyBack type requests (including WriteNoSnp*, WriteUnique*, combined write and (P)CMOs, and atomics).

Write filtering of CopyBack versus NonCopyBack types is only supported when you configure HN-F to respond with the CBusy of the POCQ. Write filtering is not supported if the HN-F returns the CBusy value of the SN-F.

The following table shows the format of the por_hnf_cbusy_limit_ctl_register. This register controls the HN-F CBusy threshold for Read requests.

Table 4-50: por_hnf_cbusy_limit_ctl register for CBusy thresholds (all requests or read types)

Bits	Name	Description
[63]	hnf_cbusy_mtbit_exclude_rni	Allows HN-F to ignore outstanding read requests from RN-I when calculating busyness.
[48]	hnf_cbusy_rd_wr_types_en	Allows separate CBusy values for reads versus writes. When enabled, the thresholds in this register are only applicable to read type requests. Otherwise these values are the default thresholds for calculating CBusy for all request types in POCQ of the HN-F. This bit must be set when sn_cbusy_prop_en = `0b1` to propagate the SN CBusy.
[23:16]	hnf_cbusy_high_limit	Specifies the POC valid threshold at which HN-F is considered very busy.
[15:8]	hnf_cbusy_med_limit	Specifies the POC valid threshold at which HN-F is considered medium busy.

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Bits	Name	Description
[7:0]	hnf_cbusy_low_limit	Specifies the POC valid threshold at which HN-F is considered least busy.

The following table shows the format of the por_hnf_cbusy_write_limit_ctl register. This register controls the HN-F CBusy threshold for write requests.

Table 4-51: Register for CBusy thresholds (write requests)

Bit field	Field	Description
[48]	hnf_cbusy_sep_copyback_types	When set, HN-F calculates CBusy based on outstanding CopyBack and NonCopyBack type requests independently in the HN-F POCQ.
[23:16]	hnf_cbusy_high_limit	Specifies the POC valid threshold at which HN-F is considered very busy.
[15:8]	hnf_cbusy_med_limit	Specifies the POC valid threshold at HN-F is considered medium busy.
[7:0]	hnf_cbusy_low_limit	Specifies the POC valid threshold at which HN-F is considered least busy.

The following table shows the CBusy values that are returned to RNs according to programming.

Table 4-52: HN-F CBusy value propagation according to programming

hnf_adv_cbusy_mode_en	hnf_cbusy_rd_wr_types_en	sn_cbusy_prop_en	cbusy_highest_of_all_en	CBusy value passed to RN
0b0	x	x	x	POCQ CBusy value is returned.
0b1	0b0	x	x	POCQ CBusy value is returned.
0b1	0b1	0b0	0b0	POCQ CBusy value for read or write is returned, according to the request type.
0b1	0b1	0b1	0b0	SN CBusy value for read or write is returned for the corresponding SN group, according to the request type.
0b1	0b1	x	0b1	Highest of either the SN or POCQ CBusy value for read or write is returned, according to the request type.

Where applicable, HN-F returns the read or write CBusy value according to opcode type.

Write CBusy values can be further separated into CopyBack and NonCopyBack values using the hnf_cbusy_sep_copyback_types field. This separation only applies when HN-F is programmed to propagate the POCQ CBusy values. In this mode, CopyBack write type values account for pending WriteClean*, WriteBack*, WriteEvictFull*, and Evict type operations. NonCopyBack write type values account for all other pending write operations (WriteUnique*, WriteNoSnp*). Combined Write* and (P)CMO operations are counted towards NonCopyBack types. Standalone CMOs are not counted towards either of the CopyBack or NonCopyBack type requests.

HN-F to SN-F CBusy based throttling

HN-F can identify two groups of memory controllers using a configuration bit for each SN. These groups are known as group A or group B. You can use the two groups to identify fast and slow memory types. Therefore, the HN-F can handle traffic to and from the two types independently of each other. HN-F can track the read and write busyness to each SN-F group over a configurable

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transaction window. It can be programmed to track the last 128 or 256 transactions. When HN-F has received as many responses from SN-F, it measures the current busyness for each group of SN and request types (read and write). The measured busyness is then used to throttle the traffic to SN-F appropriately. The threshold for measuring the CBusy for the last 128 or 256 transactions is also configurable. For example, if HN-F receives ≥16 transactions and CBusy = `0b11` from Group 0 SN-Fs, then HN-F treats the SN-F CBusy value as `0b11`. This value corresponds to very busy.

The threshold for measuring the CBusy for the last 128 or 256 transactions is also configurable. For example, consider a scenario where HN-F is programmed to calculate the last 128 CBusy responses. HN-F tracks the number of times it receives CBusy values of `0b00`, `0b01`, `0b10`, and `0b11` for each SN group. In this example, the HN-F receives more than 16 CBusy = `0b11` responses from Group 0 SN-Fs out of the last 128 responses. In this case, HN-F treats the final SN-F CBusy value as `0b11` for the subsequent 128 transactions while continuing to accumulate new CBusy response values.

HN-F can be configured to throttle outgoing requests in either a static mode or a default dynamic mode:

- Static throttling mode: HN-F controls the fixed number of transactions outstanding at any point for a given SN group and request type:
  - CBusy = `0b11` (very busy): HN-F restricts transactions to a maximum of a quarter of the number of POCQ entries.
  - CBusy = `0b10` (medium busy): HN-F restricts transactions to a maximum of half of the number of POCQ entries.
  - CBusy = `0b01` (low busy): HN-F restricts transactions to three quarters of the number of POCQ entries.
  - CBusy = `0b00` (not busy): HN-F can issue as many requests as the number of POCQ entries.
- Dynamic throttling mode: The number of *Outstanding Transactions* (OTs) can be dynamically throttled according to programmed values. It can be configured to increment or decrement the transaction count by two, four, or eight transactions after every 128 or 256 transaction window (as programmed).
  - CBusy = `0b11` (very busy): Decrement the OT count.
  - CBusy = `0b10` (medium busy): No change to the current OT count.
  - CBusy = `0b01` (low busy): Increment the OT count.
  - CBusy = `0b00` (not busy): Increment the OT count.

When you configure an HN-F to respond to RNs with the CBusy value of an SN-F, HN-F can propagate the CBusy value according to the SN-F group that the request targets. For example, consider an RN-F sending a read request that is targeting SN group A. The RN can receive the CBusy value for a group A SN, even if the request hits in SLC and therefore the HN-F completes the request.

The following table shows the format of the por_hnf_cbusy_resp_ctl register. This register controls the CBusy responses.

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Table 4-53: por_hnf_cbusy_resp_ctl register for configuring CBusy value on responses

Bits	Name	Description: Controls the CBusy responses
[21:16]	cbusy_sn_dynamic_ot_count	Count by which the OT count is incremented or decremented for dynamic OT throttling.
[7]	cbusy_sn_static_ot_mode_en	Enables the static OT throttling to SN.
[4]	Cbusy_highest_of_all_en	When set to `0b1`, HN-F responds with the CBusy values from the highest of group A and group B.
[0]	sn_cbusy_prop_en	When set to `0b1`, HN-F responds with the CBusy values from SN-F instead of using its own POCQ occupancy-based thresholding. Read and write modes are still controlled using por_hnf_cbusy_limit_ctl and por_hnf_cbusy_write_limit_ctl.

The following table shows the format of the por_hnf_sam_sn_properties1 register. This register controls the group to which each SN belongs.

Table 4-54: Register for identifying SN groups

Bit field	Field	Description
[57]	Region1_sn_group	**0b0** Group A **0b1** Group B
[49]	Region0_sn_group	
[41]	sn5_group	
[33]	sn4_group	
[25]	sn3_group	
[17]	sn2_group	
[9]	sn1_group	
[1]	sn0_group	

The following table shows the format of the por_hnf_cbusy_sn_ctl register. This register controls the CBusy sampling.

Table 4-55: por_hnf_cbusy_sn_ctl register for CBusy sampling control

Bit field	Field	Description
[56:48]	hnf_cbusy_txn_cnt	Number of SN responses over which the CBusy counters are tracked.
[41:32]	hnf_cbusy_threshold_cntr11	CBusy threshold at which SN-F is considered busy for Counter_11.
[25:16]	hnf_cbusy_threshold_cntr10	CBusy threshold at which SN-F is considered busy for Counter_10.
[9:0]	hnf_cbusy_threshold_cntr01	CBusy threshold at which SN-F is considered busy for Counter_01.

HN-F continues to propagate the multi-source bit (CBusy[2]) in the advanced modes.

4.18.6 MTSX functionality

The MTSX device is used when you require support for *Memory Tagging Extensions* (MTE), but an AXI slave device in your system does not support MTE. Internally, MTSX includes all SBSX functionality and support for MTE using a *Memory Tag Unit* (MTU).

MTSX can generate separate data and tag requests on the AXI interface according to the CHI request. For the MTSX to generate tag requests, you must program the MTSX address generation

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registers. For more information about programming these registers, see 5.4.6 MTSX programming on page 1284.

Optionally, the MTSX can include a *Tag Cache* (TC) to store tags locally. This configuration allows for faster tag access and reduced AXI traffic. If the TC is not included, each CHI request requiring tag access causes the MTSX to generate two AXI requests. One request is for data and one request is for tag access.

4.18.6.1 Software-configurable error injection in MTSX

The MTSX supports software-configurable error injection and reporting. This feature enables testing of the software error handler routine for TC double-bit ECC data errors.

The por_mtu_err_inj configuration register enables configurable error injection and reporting for a given PA value.

Any read for which the TC provides the data is defined as a TC hit. If error injection and reporting are enabled, any TC hit drives the data double-bit error and a fault interrupt through the RAS control block for the TC hit. This functionality emulates a double-bit ECC error in the TC data RAM but does not pollute the TC data RAM through the fill path.


Note

This mechanism is designed to mimic TC data ECC errors for TC hits. If enabled, the mechanism only causes an error to be logged and, optionally, an interrupt to be generated. TC misses do not drive any errors or error interrupts.

For more information about configuring error injection, see 5.3.13.24 por_mtu_err_inj on page 1269.

4.18.6.2 Hardware-based TC flush engine in MTSX

The MTSX supports a flush engine mechanism to flush the TC. The flush engine ensures that all cache lines in the TC are flushed from CI-700.

Two configuration registers per MTSX instance support the TC flush engine:

por_mtu_tc_flush_pr
: The TC flush policy register. This register triggers a flush to start and indicates the flush operation type.

por_mtu_tc_flush_sr
: The TC flush status register. This register indicates flush completion.

A flush request is initiated by writing to the por_mtu_tc_flush_pr. After a flush request has been initiated, the por_mtu_tc_flush_pr register must not be written again until the flush completes.

When all cache lines are flushed, the mtu_tc_flush_complete bit in the por_mtu_tc_flush_sr register is set. Setting this bit indicates that the flush engine has completed its operation.

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The flush engine has two modes of operation:

CleanInvalid
: The default mode. The flush engine writes back any modified data to memory before invalidating a cache line.

CleanShared
: The flush engine writes any modified data is back to memory but keeps a clean copy of the cache line in the TC.

The mtu_tc_flush_mode bit of the por_mtu_tc_flush_pr register sets the mode of operation for a flush.

For more information about configuring TC flush, see the following register descriptions:

- 5.3.13.7 por_mtu_tc_flush_pr on page 1221
- 5.3.13.8 por_mtu_tc_flush_sr on page 1222

4.19 Processor events

CI-700 supports communicating processor events to all processors in the system.

Refer to the processor event interface signals described in B.12 Processor event interface signals on page 1402.

When a processor generates an output event that an SEV instruction triggers, it is broadcast to all processors in the system. Similarly, anytime an exclusive monitor within HN-F or HN-I is cleared, an output event is broadcast to all processors in the system. The event interface signals are also present at RN-I and RN-D nodes, for use by components such as a *System Memory Management Unit* (SMMU).

The logical operator OR is used to combine the **EVENT** signals, then the result is broadcast to the processors.

4.20 Quality of Service

CI-700 includes end-to-end QoS capabilities which support latency and bandwidth requirements for different types of devices.

The QoS device classes are:

Devices with bounded latency requirements

These devices are primarily real-time or isochronous that require some or all of their transactions complete within a specific time period to meet overall system requirements. These devices are typically highly latency-tolerant within the bounds of their maximum latency requirement. Examples of this class of device include networking I/O devices and display devices.

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Latency-sensitive devices

The response latency that the transactions of devices incur has a high impact on the performance of these devices. Processors are traditionally highly latency-sensitive devices, although a processor can also be a bandwidth-sensitive device depending on its workload.

Bandwidth-sensitive devices

These devices have a minimum bandwidth requirement to meet system requirements. An example of this class of device is a video codec engine, which requires a minimum bandwidth to sustain real-time video encode and decode throughput.

Bandwidth-hungry devices

These devices have significant bandwidth requirements and can use as much system bandwidth as is made available, to the limits of the system. These devices determine the overall scalability limits of a system, with the devices and system scaling until all available bandwidth is consumed.


Note

A device can be classified into one or more of these classes, depending on its workload requirements.

Support for these different types of devices and their resulting traffic is included in the AMBA® 5 CHI protocol and in the entirety of CI-700 microarchitecture. Each component in CI-700 contributes to the overall QoS microarchitecture.

4.20.1 Architectural QoS support

The AMBA 5 CHI protocol includes a 4-bit *QoS Priority Value* (QPV) with all message flits.

The QPV of the originating message must propagate for all messages in a transaction. The QPV is defined as higher values being higher priority and lower values being lower priority. All CI-700 components use the QPV to provide prioritized arbitration and to prevent Head-of-line blocking based on the QPV.

4.20.2 Microarchitectural QoS support

The QPV of RN requests must be modulated depending on how well or poorly their respective QoS requirements are met.

4.20.2.1 QoS regulators

CI-700 supports end-to-end *Quality-of-Service* (QoS) which guarantees using QoS mechanisms that are distributed throughout the system. QoS-modulation capability can be integrated into the RN. However CI-700 enables system designers to include non-QoS-aware devices in the CI-700

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system, but still have these devices meet the QoS-modulation requirements of the CI-700 QoS microarchitecture.

The QoS provision uses the QoS field in each RN request to influence arbitration priority at every QoS decision point. The QoS field is then propagated through all subsequent packets that are generated by the transaction. RNs must either:

- Self-modulate their QoS priority depending on how well their respective QoS requirements are met.
- Use the integrated QoS regulators at ingress points to CI-700.

It is possible to include non-QoS-aware devices in the system, but still have these devices meet the QoS modulation requirement of the QoS architecture. To meet this requirement, CI-700 includes inline regulators that perform the QoS functionality without the requesting device requiring any awareness of QoS. A *QoS Regulator* (QR) provides an interstitial layer between an RN and the interconnect. The QR monitors how the bandwidth and latency requirements of the RN are met, and does in-line replacement of the RN-provided QPV field. The QR adjusts the QPV field upwards for higher priority in the system and downwards for lower priority.

QoS regulators are present at each RN-I ACE-Lite interface and at each XP device port that is connected to an RN-F.

CI-700 QoS regulators have three operating modes:

- Pass-through
- Programmed QoS value
- Regulation

These operating modes are controlled through memory-mapped configuration registers.

4.20.2.2 QoS regulator operation

The values of the base QPV, **AxQOS** for AXI and ACE-Lite interfaces or **RXREQFLIT.QOS** for CHI ports, are inputs to the QoS subblock.

When latency regulation or period regulation is enabled, the values generated by the regulators replace the base QPV values. For an RN-F, a single QoS regulator monitors CHI transactions that return data to the RN-F such as reads, atomics, and snoop stash responses. The regulated QPV is applied to all CHI requests from that RN-F. For an RN-I or RN-D, separate QoS regulators exist for AR and AW channels.

The QoS regulators can operate in either latency regulation mode or period regulation mode. The registers to configure the QoS regulators exist in each RN-I, RN-D, and XP.

Latency regulation mode

When configured for latency regulation, the QoS regulator increases the QPV whenever actual transaction latency is higher than the target, and decreases the QPV when it is lower:

- For every cycle that the latency of a transaction is more than the target latency, the QPV increases by a fractional amount. The scale factor K_i determines this amount.

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- For every cycle that the latency of a transaction is less than the target latency, the QPV decreases by the same fractional amount. The scale factor K_i determines this amount.

The QoS Latency Target register specifies the target transaction latency in cycles.

The QoS Latency Scale register specifies the scale factor K_i. It is coded in powers of two, so that a programmed value of `0x0` = 2^{-3} and a programmed value of `0x7` = 2^{-10}.

The QoS regulator can be programmed to operate in latency regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to `0b1`.
- Set the lat_en bit to `0b1`.
- Set the reg_mode bit to `0b0`.
- Set the pqv_mode bit to `0b0`.

Period regulation mode for bandwidth regulation

When configured for period regulation, the QoS regulator increases the QPV whenever the period between transactions is larger than the target, and decreases the QPV when it is lower:

- For every cycle that the period between transactions (as measured at dispatch time) is more than the target period, the QPV increases the scale factor K_i by a fractional amount.
- For every cycle that the period between transactions is less than the target period, the QPV decreases the scale factor K_i by the same fractional amount.

The QoS Latency Target register specifies the target period in cycles.

The QoS Latency Scale register specifies the scale factor K_i. It is coded in powers of two, so that a programmed value of `0x0` = 2^{-3} and a programmed value of `0x7` = 2^{-10}.

The QoS regulator can be programmed to operate in period regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to `0b1`.
- Set the lat_en bit to `0b1`.
- Set the reg_mode bit to `0b1`.

There are two modes of period regulation:

Normal mode

The QPV does not increase or decrease when there are zero outstanding transactions.

Quiesce high mode

The QPV increases by a fractional amount, which the scale factor K_i determines, in every cycle where there are zero outstanding transactions.

The mode of period regulation can be selected by programming the pqv_mode bit in the QoS Control register.

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4.20.2.3 RN-I and RN-D bridge QoS support

In addition to the QoS regulators, the RN-I and RN-D bridge provides QoS-aware arbitration mechanisms.

To simplify arbitration logic, all transactions are split into two *QoS Priority Classes* (QPCs), high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.

Port multiplexer arbitration

An RN-I and RN-D bridge includes three ACE-Lite and ACE-Lite-with-DVM ports. The RN-I and RN-D bridge selects between these ports for allocation into its transaction tracker. This selection process makes the allocated transaction a candidate for issuing to a Home Node. The port multiplexer is arbitrated using the following strategy:

- High QPC first, then the low QPC.
- Round-robin arbitration among the AMBA ports within a QPC.

Tracker allocation

When transactions are allocated into the tracker, they are scheduled for issuance to a Home Node based on QPC. This strategy is the same strategy as port mux arbitration.

- High QPC first, then the low QPC.
- Round-robin arbitration in a QPC among the transactions for issue.

4.20.2.4 HN-F QoS support

The HN-F is a key shared system resource that is used for system caching and for communication with the memory controller for external memory access.

The HN-F includes the following QoS support mechanisms:

QoS decoding in HN-F

The HN-F interprets the 4-bit QPV at a coarser granularity, as the following table shows.

Table 4-56: QoS classes in HN-F

QoS value range	QoS class	Class mnemonic	Priority
15	HighHigh	HH	Highest
14-12	High	H	High
11-8	Med	M	Medium
7-0	Low	L	Low

QoS class and POCQ resource availability

The HN-F includes a 16-entry, 32-entry or 64-entry structure, the POCQ, from which all transaction ordering and scheduling is performed. The POCQ buffers are shared resources for all QoS classes, with one entry being reserved for internal use. The higher the QoS class, the higher the occupancy availability. As the following figure shows, the POCQ is partitioned so that higher

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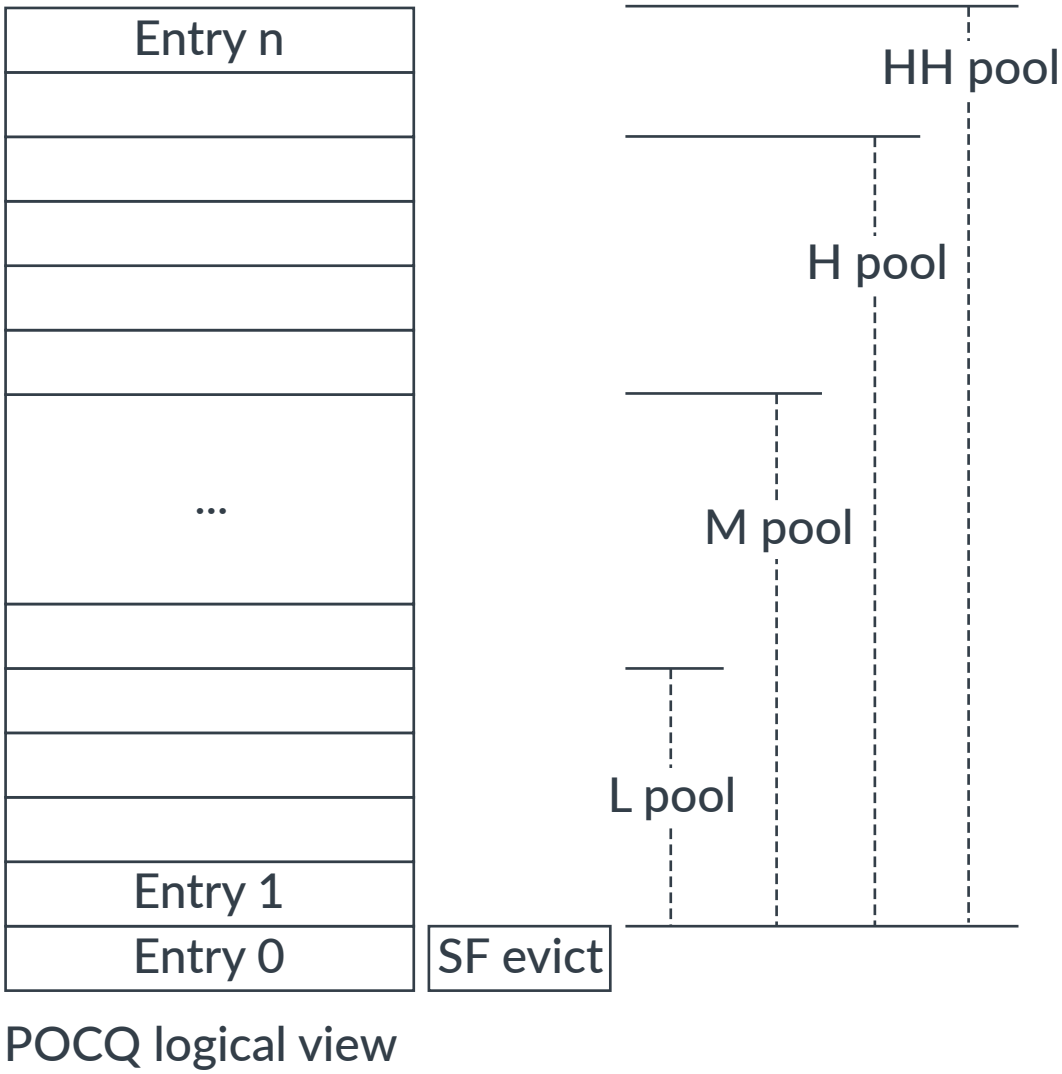
priority requests are able to use a larger percentage of the POCQ buffering. This partitioning ensures bandwidth and latency requirements of higher priority transactions are met.

The number of entries available for use by each QoS class is defined in the HN-F QoS Reservation register, and is software-programmable.

Figure 4-36: POCQ availability and QoS classes



The QoS pools are:

hh_pool	Available for HH class.
h_pool	Available for H class and HH class.
m_pool	Available for M class, H class, and HH class.
l_pool	Available for all classes.
seq	SF evictions only.

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Register fields must be programmed so that highhigh_qos_max_cnt > high_qos_max_cnt > med_qos_max_cnt > low_qos_max_cnt ≥ 2. The maximum value that is allowed for highhigh_qos_max_cnt = (`NUM_ENTRIES_POCQ` - seq_qos_max_cnt).

POCQ allocation policies

Allocation into POCQ entries can follow either of two paths:

- Immediate allocation on receipt of the initial request by the HN-F
- Allocation of a retried request after a protocol-layer retry of the initial request

The first case is the expected common case and is always the case in a reasonably uncongested system. If the POCQ has an available buffer corresponding to the QoS class of an arriving request, that request allocates in the POCQ.

However, consider a congested system and a POCQ entry with the QoS class of an arriving request is unavailable at the time of arrival. In this case, the AMBA® 5 CHI protocol requires that the arriving request receives a protocol-layer retry. The transaction flow in this case is as follows:

1. A request arrives at a congested HN-F.
2. The HN-F does not have an available POCQ buffer corresponding to the QoS class of the new transaction.
3. The HN-F increments a credit counter for the specific QoS class of the specific RN and sends a RetryAck response to the RN.
4. On receiving a RetryAck response, the RN then waits for a follow-on PCreditGrant response.
5. When a POCQ entry becomes available, the HN-F reserves that buffer for the highest-priority RN with a nonzero credit-counter. It also sends a PCreditGrant response to the selected RN.
6. On receiving a PCreditGrant, the RN re-issues the transaction, which is guaranteed to be allocated into the HN-F.

This mechanism serves as prioritized arbitration based on QoS values for requests that are sent to the HN-F.

POCQ scheduler policies

When transactions are allocated into the POCQ, they are scheduled for issuance based on the QPV as follows, in descending order of priority:

- Starved transactions. These transactions are lower-priority transactions that have made no progress for a specific number of cycles. The number of cycles is specified in the respective fields in the RN Starvation Register.
- Highest QoS class
- Round-robin arbitration within a QoS class among the issuable transactions

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4.20.2.5 HN-I, SBSX, and MTSX QoS support

The HN-I bridge provides QoS-aware arbitration mechanisms for static grants and AMBA requests.

To simplify arbitration logic, all transactions are split into two QPCs: high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.


Note

SBSX and MTSX QoS support is identical to that of the HN-I.

Dynamic credit tracker allocation

Requests allocate into the tracker until it is full. After it is full, requests are retried and the HN-I increments a credit counter for the affected RNs in an internal retry bank.

When a tracker entry is cleared, the HN-I checks the retry bank for any retried transactions. If any are present, the newly available tracker entry is reserved and a static credit grant is sent to an RN chosen using the following algorithm:

- Choose an RN marked as high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Scheduling to AMBA interface

When transactions are allocated into the tracker, they are scheduled for issue on the AMBA interface. The scheduling is based on QPC following a similar strategy to static credit allocation:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Write data buffers are also allocated based on QPC class. For write requests that are ready to issue:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

4.20.3 QoS configuration example

This example configuration demonstrates the QoS mechanisms and their contribution to the overall QoS solution.

It is the responsibility of the SoC designer and system programmer to configure CI-700 to meet the specific requirements of the system and expected workloads.

System operating conditions

The example QoS configuration assumes the following:

- Four processor clusters:

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- Bimodal operation. A processor cluster is latency-sensitive when bandwidth per cluster is ≤ 2GB/s, and bandwidth-hungry, and therefore latency-tolerant, when bandwidth per cluster is > 2GB/s.
- 16 outstanding combined reads and writes.
- 10GB/s maximum bandwidth per cluster.
- 25GB/s maximum aggregate bandwidth across all processor clusters.

- Four peripheral devices with bounded latency requirements:
  - Each device is the sole device that is connected to ACE-Lite interface 0 on four different RN-I bridges.
  - 1 microsecond maximum latency requirement.
  - 4GB/s maximum bandwidth per device.
  - 210GB/s maximum aggregate bandwidth across all devices.
- 14 peripheral bandwidth-hungry devices:
  - Connected to all remaining RN-I ACE-Lite interfaces.
  - 12GB/s read or write bandwidth per device, with a combined maximum of 24GB/s.
  - 60GB/s maximum aggregate bandwidth across all devices.
- All devices can be concurrently active.
- 80GB/s maximum aggregate bandwidth across all devices.

HN-F QoS classes

For the QoS ranges and class values in HN-F, refer to Table 4-56: QoS classes in HN-F on page 173.

QoS regulator settings

To meet the bandwidth and latency requirements of the described system configuration, CI-700 QoS regulators can be configured with the settings as described in the following table.

Table 4-57: QoS regulation settings

Device	Regulation type	Regulation parameter	QoS range	QoS scale
Processor	Latency	60ns max latency	11-13	8-9
Real-time peripheral	Override (constant value)	Constant	15	n/a
High-bandwidth peripheral	Override (constant value)	Constant	8	n/a

The latency specification for real-time peripherals must be sufficiently far below the maximum real-time constraint to allow the control loop in the QoS regulator to adjust based on achieved latency. However, the programmed latency must not violate the maximum latency requirement.

To meet the bandwidth and latency requirements of the described system configuration, HN-F QoS reservation values can be configured as summarized in the following table. The table is based on 32-entry POCQ with one entry for SF back invalidations.

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Table 4-58: QoS class and reservation value settings

QoS class	QoS reservation value
HighHigh	31
High	30
Medium	15
Low	5

These settings enable the following system functionality:

- Real-time devices are QPV-15, ensuring their transactions meet their bounded latency requirements.
- The processor QPV is higher than the bandwidth-hungry devices, second only to the real-time devices. Therefore the processor QPV generally achieves minimum latency, except when there is high-bandwidth real-time traffic.
- Real-time devices have all the HN-F POCQ buffering available to them, to prevent bandwidth limitations from impacting achieved latency.
- Real-time devices always have buffering available to them throughout the entirety of CI-700 preventing Head-of-line blocking from lower-priority or higher-latency transactions.

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5 Programmers model

This chapter describes the application-level registers and provides an overview for programming the CI-700 interconnect.

5.1 About the programmers model

A CI-700 interconnect consists of various components, such as XPs, RN-Is, or DTCs, that are accessed through memory mapped registers for configuration, topology, and status information.

The memory mapped registers are organized in a series of 64KB regions. They are accessed through CHI, AXI, or APB read and write commands. APB accesses to the registers occur through the CI-700 HN-D APB interface.

A full description of a CI-700 interconnect consists of:

- A list of components
- The compile-time configuration options for each component
- The connectivity between the components

Software can determine the full configuration of the CI-700 interconnect through a sequence of accesses to the configuration register space.

5.1.1 Node configuration register address mapping

All CI-700 configuration registers are mapped to a specific address range that is divided into sections for individual components.

The configuration register address space starts at PERIPHBASE. For a CI-700 mesh configuration, the configuration register address space has a maximum size of 256MB. For a single-MXP configuration, the configuration register address space has a maximum size of 8MB.

The **CFGM_PERIPHBASE** input signal controls the reset value of PERIPHBASE. Configuration register accesses through the HN-D APB interface use the same addressing scheme as the CHI and AXI interfaces. However, only 32 bits of the address are provided to the APB interface.

All configuration, information, and status registers in a CI-700 interconnect are grouped into 64KB regions each associated with a CI-700 component instance. The base address of each region can be determined at compile time, or determined at runtime through a software discovery mechanism.

Software discovery consists of steps:

1. Read information in the 64KB region at offset `0x0`. This information determines the number of XPs in CI-700 and the offset from PERIPHBASE for the 64KB region of each XP.

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2. Read information in the 64KB region that is associated with each XP. This information determines the components that are associated with that XP, topology information for those components, and the offset from PERIPHBASE for each component 64KB region.
3. Read information in the 64KB region that is associated with the component. This information determines the type of block and the configuration details of the component.

For more information on these steps, see 4.12.4 Discovery tree structure on page 133.

With this sequence, software can build a list of all components in the system and the addresses of their respective 64KB configuration regions.

5.1.2 Global configuration register region

The 64KB block at offset `0x0` contains global information and configuration for CI-700, and the first level of discovery information for components in the system.

Each XP Base Address register contains the offset from PERIPHBASE for a 64KB region that contains the information about one XP. The XP Base Address register also contains discovery information for components that are associated with that XP. The XP Base address refers to the relative address of the XP configuration registers. The first level of discovery points to each por_mxp_node_info register of the XPs.

For more register information, see 5.3.1 Configuration master register descriptions on page 207.

5.1.3 XP configuration register region

Each XP has a 64KB configuration register region with information about that XP and all associated components.

For more information, refer to 5.3.6 XP register descriptions on page 718.

5.1.4 Component configuration register region

Each non-XP component has a 64KB configuration register region. This region has programmable information, status, and configuration options for that component.

The following table lists the contents, including the number of 8B registers which fit in the space.

Table 5-1: Configuration register region values

Register sections	Relative offset	Absolute offset	Description
Discovery register section			
NODE INFO (node type, node ID)	`0x0`	`0x0`	Up to 16 registers
CHILD INFO (number of children, offset of the first child pointer register = `0x100`)	`0x80`	`0x80`	Up to 16 registers

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Register sections	Relative offset	Absolute offset	Description
CHILD POINTER registers	0x100	0x100	Up to 256 registers
UNIT REGISTER section	0x900	Unit-specific registers	
UNIT INFO	0x0	0x900	Up to 16 registers
UNIT SECURITY	0x80	0x980	Up to 16 registers
UNIT CTRL	0x100	0xA00	Up to 16 registers
UNIT QoS	0x180	0xA80	Up to 32 registers
UNIT DEBUG	0x280	0xB80	Up to 16 registers
UNIT OTHER	0x300	0xC00	Up to 128 registers
UNIT POWER	0x700	0x1000	4KB-aligned space – 512 registers
UNIT PMU	0x1700	0x2000	4KB-aligned space – 512 registers
UNIT RAS (Secure RAS registers)	0x2700	0x3000	4KB-aligned space – 512 registers
UNIT RAS (Non-secure RAS registers)	0x2800	0x3100	4KB-aligned space – 512 registers

5.1.5 Requirements of configuration register reads and writes

Reads and writes to the CI-700 configuration registers must meet certain requirements.

A dedicated APB slave port is provided for the access of all CI-700 configuration registers. The APB slave port has the following properties:

- APB only supports 32-bit accesses
- **PSTRB[3:0]** must be driven to `4'hF` for a write transaction
- Secure access requires setting **PPROT[1]** to 0

If the following requirements are not met, **UNPREDICTABLE** behavior can occur:

- All accesses must be of device type, either:
  - Device, strongly ordered
  - nGnRE, nGnRnE
- All accesses must have a data size of 32 bits or 64 bits
- All accesses must be natively aligned, that is:
  - 32-bit accesses must be aligned to a 32-bit boundary
  - 64-bit accesses must be aligned to a 64-bit boundary
- For configuration register writes, all bits, 32 or 64, must be written, that is, all byte lanes must be valid:
  - **WRSTB** must indicate that all byte lanes are valid if the write transaction is from an AMBA® AXI or ACE-Lite interface.

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- **BE** must indicate that all byte lanes are valid if the write transaction is sent from an AMBA® 5 CHI interface.

- Secure registers can only be accessed through a Secure access, that is, NS = 0. Non-secure registers can be accessed through either a Secure or Non-secure access.

For more information on error signal handling, see 4.17 Reliability, Availability, and Serviceability on page 141.

5.2 Register summary

The register summary tables list the registers in CI-700.

5.2.1 Configuration master register summary

This section lists the configuration master registers used in CI-700.

CFGM register summary

The following table shows the *CFGM* registers in offset order from the base memory address.


Note

Some offsets in this table are defined by specific types of base address in the component configuration register region. For more information about these base addresses, see Table 5-1: Configuration register region values on page 180.

Table 5-2: CFGM register summary

Offset	Name	Type	Description
0x0	por_cfgm_node_info	RO	5.3.1.1 por_cfgm_node_info on page 207
0x8	por_cfgm_periph_id_0_periph_id_1	RO	5.3.1.2 por_cfgm_periph_id_0_periph_id_1 on page 208
0x10	por_cfgm_periph_id_2_periph_id_3	RO	5.3.1.3 por_cfgm_periph_id_2_periph_id_3 on page 209
0x18	por_cfgm_periph_id_4_periph_id_5	RO	5.3.1.4 por_cfgm_periph_id_4_periph_id_5 on page 210
0x20	por_cfgm_periph_id_6_periph_id_7	RO	5.3.1.5 por_cfgm_periph_id_6_periph_id_7 on page 211
0x28	por_cfgm_component_id_0_component_id_1	RO	5.3.1.6 por_cfgm_component_id_0_component_id_1 on page 212
0x30	por_cfgm_component_id_2_component_id_3	RO	5.3.1.7 por_cfgm_component_id_2_component_id_3 on page 213
0x80	por_cfgm_child_info	RO	5.3.1.8 por_cfgm_child_info on page 214
0x980	por_cfgm_secure_access	RW	5.3.1.9 por_cfgm_secure_access on page 215

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Offset	Name	Type	Description
0x3000	por_cfgm_errgsr0	RO	5.3.1.10 por_cfgm_errgsr0 on page 217
0x3008	por_cfgm_errgsr1	RO	5.3.1.11 por_cfgm_errgsr1 on page 218
0x3010	por_cfgm_errgsr2	RO	5.3.1.12 por_cfgm_errgsr2 on page 219
0x3018	por_cfgm_errgsr3	RO	5.3.1.13 por_cfgm_errgsr3 on page 220
0x3020	por_cfgm_errgsr4	RO	5.3.1.14 por_cfgm_errgsr4 on page 221
0x3028	por_cfgm_errgsr5	RO	5.3.1.15 por_cfgm_errgsr5 on page 222
0x3080	por_cfgm_errgsr6	RO	5.3.1.16 por_cfgm_errgsr6 on page 223
0x3088	por_cfgm_errgsr7	RO	5.3.1.17 por_cfgm_errgsr7 on page 224
0x3090	por_cfgm_errgsr8	RO	5.3.1.18 por_cfgm_errgsr8 on page 225
0x3098	por_cfgm_errgsr9	RO	5.3.1.19 por_cfgm_errgsr9 on page 226
0x30A0	por_cfgm_errgsr10	RO	5.3.1.20 por_cfgm_errgsr10 on page 227
0x30A8	por_cfgm_errgsr11	RO	5.3.1.21 por_cfgm_errgsr11 on page 228
0x3100	por_cfgm_errgsr0_NS	RO	5.3.1.22 por_cfgm_errgsr0_NS on page 229
0x3108	por_cfgm_errgsr1_NS	RO	5.3.1.23 por_cfgm_errgsr1_NS on page 230
0x3110	por_cfgm_errgsr2_NS	RO	5.3.1.24 por_cfgm_errgsr2_NS on page 231
0x3118	por_cfgm_errgsr3_NS	RO	5.3.1.25 por_cfgm_errgsr3_NS on page 232
0x3120	por_cfgm_errgsr4_NS	RO	5.3.1.26 por_cfgm_errgsr4_NS on page 233
0x3128	por_cfgm_errgsr5_NS	RO	5.3.1.27 por_cfgm_errgsr5_NS on page 234
0x3180	por_cfgm_errgsr6_NS	RO	5.3.1.28 por_cfgm_errgsr6_NS on page 235
0x3188	por_cfgm_errgsr7_NS	RO	5.3.1.29 por_cfgm_errgsr7_NS on page 236
0x3190	por_cfgm_errgsr8_NS	RO	5.3.1.30 por_cfgm_errgsr8_NS on page 237
0x3198	por_cfgm_errgsr9_NS	RO	5.3.1.31 por_cfgm_errgsr9_NS on page 238
0x31A0	por_cfgm_errgsr10_NS	RO	5.3.1.32 por_cfgm_errgsr10_NS on page 239
0x31A8	por_cfgm_errgsr11_NS	RO	5.3.1.33 por_cfgm_errgsr11_NS on page 240
0x3FA8	por_cfgm_errdevaff	RO	5.3.1.34 por_cfgm_errdevaff on page 241
0x3FB8	por_cfgm_errdevarch	RO	5.3.1.35 por_cfgm_errdevarch on page 242
0x3FC8	por_cfgm_erridr	RO	5.3.1.36 por_cfgm_erridr on page 243
0x3FD0	por_cfgm_errpidr45	RO	5.3.1.37 por_cfgm_errpidr45 on page 244
0x3FD8	por_cfgm_errpidr67	RO	5.3.1.38 por_cfgm_errpidr67 on page 245
0x3FE0	por_cfgm_errpidr01	RO	5.3.1.39 por_cfgm_errpidr01 on page 246
0x3FE8	por_cfgm_errpidr23	RO	5.3.1.40 por_cfgm_errpidr23 on page 247
0x3FF0	por_cfgm_errcidr01	RO	5.3.1.41 por_cfgm_errcidr01 on page 248
0x3FF8	por_cfgm_errcidr23	RO	5.3.1.42 por_cfgm_errcidr23 on page 249
0x900	por_info_global	RO	5.3.1.43 por_info_global on page 250
0x1C00	por_ppu_int_enable	RW	5.3.1.44 por_ppu_int_enable on page 252
0x1C08	por_ppu_int_status	W1C	5.3.1.45 por_ppu_int_status on page 253
0x1C10	por_ppu_qactive_hyst	RW	5.3.1.46 por_ppu_qactive_hyst on page 254
0x1C18	por_mpam_s_err_int_status	W1C	5.3.1.47 por_mpam_s_err_int_status on page 255

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Offset	Name	Type	Description
0x1C20	por_mpam_ns_err_int_status	W1C	5.3.1.48 por_mpam_ns_err_int_status on page 256
0xCHILD_POINTER_BASE + 8 * $index	por_cfgm_child_pointer_$index	RO	5.3.1.49 por_cfgm_child_pointer_$index on page 257

5.2.2 DN register summary

This section lists the DN registers used in CI-700.

DN register summary

The following table shows the *DN* registers in offset order from the base memory address

Table 5-3: DN register summary

Offset	Name	Type	Description
0x0	por_dn_node_info	RO	5.3.2.1 por_dn_node_info on page 259
0x80	por_dn_child_info	RO	5.3.2.2 por_dn_child_info on page 260
0x900	por_dn_build_info	RO	5.3.2.3 por_dn_build_info on page 261
0x980	por_dn_secure_register_groups_override	RW	5.3.2.4 por_dn_secure_register_groups_override on page 262
0xA00	por_dn_cfg_ctl	RW	5.3.2.5 por_dn_cfg_ctl on page 263
0xA08	por_dn_aux_ctl	RW	5.3.2.6 por_dn_aux_ctl on page 264
0xC00	por_dn_vmf0_ctrl	RW	5.3.2.7 por_dn_vmf0_ctrl on page 265
0xC08	por_dn_vmf0_rnf0	RW	5.3.2.8 por_dn_vmf0_rnf0 on page 267
0xC10	por_dn_vmf0_rnd	RW	5.3.2.9 por_dn_vmf0_rnd on page 268
0xC18	por_dn_vmf0_cxra	RW	5.3.2.10 por_dn_vmf0_cxra on page 269
0xC20	por_dn_vmf1_ctrl	RW	5.3.2.11 por_dn_vmf1_ctrl on page 270
0xC28	por_dn_vmf1_rnf0	RW	5.3.2.12 por_dn_vmf1_rnf0 on page 272
0xC30	por_dn_vmf1_rnd	RW	5.3.2.13 por_dn_vmf1_rnd on page 273
0xC38	por_dn_vmf1_cxra	RW	5.3.2.14 por_dn_vmf1_cxra on page 274
0xC40	por_dn_vmf2_ctrl	RW	5.3.2.15 por_dn_vmf2_ctrl on page 275
0xC48	por_dn_vmf2_rnf0	RW	5.3.2.16 por_dn_vmf2_rnf0 on page 276
0xC50	por_dn_vmf2_rnd	RW	5.3.2.17 por_dn_vmf2_rnd on page 277
0xC58	por_dn_vmf2_cxra	RW	5.3.2.18 por_dn_vmf2_cxra on page 278
0xC60	por_dn_vmf3_ctrl	RW	5.3.2.19 por_dn_vmf3_ctrl on page 279
0xC68	por_dn_vmf3_rnf0	RW	5.3.2.20 por_dn_vmf3_rnf0 on page 281
0xC70	por_dn_vmf3_rnd	RW	5.3.2.21 por_dn_vmf3_rnd on page 282
0xC78	por_dn_vmf3_cxra	RW	5.3.2.22 por_dn_vmf3_cxra on page 283
0xC80	por_dn_vmf4_ctrl	RW	5.3.2.23 por_dn_vmf4_ctrl on page 284
0xC88	por_dn_vmf4_rnf0	RW	5.3.2.24 por_dn_vmf4_rnf0 on page 285
0xC90	por_dn_vmf4_rnd	RW	5.3.2.25 por_dn_vmf4_rnd on page 286
0xC98	por_dn_vmf4_cxra	RW	5.3.2.26 por_dn_vmf4_cxra on page 287

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Offset	Name	Type	Description
0xCA0	por_dn_vmf5_ctrl	RW	5.3.2.27 por_dn_vmf5_ctrl on page 288
0xCA8	por_dn_vmf5_rnf0	RW	5.3.2.28 por_dn_vmf5_rnf0 on page 290
0xCB0	por_dn_vmf5_rnd	RW	5.3.2.29 por_dn_vmf5_rnd on page 291
0xCB8	por_dn_vmf5_cxra	RW	5.3.2.30 por_dn_vmf5_cxra on page 292
0xCC0	por_dn_vmf6_ctrl	RW	5.3.2.31 por_dn_vmf6_ctrl on page 293
0xCC8	por_dn_vmf6_rnf0	RW	5.3.2.32 por_dn_vmf6_rnf0 on page 295
0xCD0	por_dn_vmf6_rnd	RW	5.3.2.33 por_dn_vmf6_rnd on page 296
0xCD8	por_dn_vmf6_cxra	RW	5.3.2.34 por_dn_vmf6_cxra on page 297
0xCE0	por_dn_vmf7_ctrl	RW	5.3.2.35 por_dn_vmf7_ctrl on page 298
0xCE8	por_dn_vmf7_rnf0	RW	5.3.2.36 por_dn_vmf7_rnf0 on page 299
0xCF0	por_dn_vmf7_rnd	RW	5.3.2.37 por_dn_vmf7_rnd on page 300
0xCF8	por_dn_vmf7_cxra	RW	5.3.2.38 por_dn_vmf7_cxra on page 301
0xD00	por_dn_vmf8_ctrl	RW	5.3.2.39 por_dn_vmf8_ctrl on page 302
0xD08	por_dn_vmf8_rnf0	RW	5.3.2.40 por_dn_vmf8_rnf0 on page 304
0xD10	por_dn_vmf8_rnd	RW	5.3.2.41 por_dn_vmf8_rnd on page 305
0xD18	por_dn_vmf8_cxra	RW	5.3.2.42 por_dn_vmf8_cxra on page 306
0xD20	por_dn_vmf9_ctrl	RW	5.3.2.43 por_dn_vmf9_ctrl on page 307
0xD28	por_dn_vmf9_rnf0	RW	5.3.2.44 por_dn_vmf9_rnf0 on page 308
0xD30	por_dn_vmf9_rnd	RW	5.3.2.45 por_dn_vmf9_rnd on page 309
0xD38	por_dn_vmf9_cxra	RW	5.3.2.46 por_dn_vmf9_cxra on page 310
0xD40	por_dn_vmf10_ctrl	RW	5.3.2.47 por_dn_vmf10_ctrl on page 311
0xD48	por_dn_vmf10_rnf0	RW	5.3.2.48 por_dn_vmf10_rnf0 on page 313
0xD50	por_dn_vmf10_rnd	RW	5.3.2.49 por_dn_vmf10_rnd on page 314
0xD58	por_dn_vmf10_cxra	RW	5.3.2.50 por_dn_vmf10_cxra on page 315
0xD60	por_dn_vmf11_ctrl	RW	5.3.2.51 por_dn_vmf11_ctrl on page 316
0xD68	por_dn_vmf11_rnf0	RW	5.3.2.52 por_dn_vmf11_rnf0 on page 318
0xD70	por_dn_vmf11_rnd	RW	5.3.2.53 por_dn_vmf11_rnd on page 319
0xD78	por_dn_vmf11_cxra	RW	5.3.2.54 por_dn_vmf11_cxra on page 320
0xD80	por_dn_vmf12_ctrl	RW	5.3.2.55 por_dn_vmf12_ctrl on page 321
0xD88	por_dn_vmf12_rnf0	RW	5.3.2.56 por_dn_vmf12_rnf0 on page 322
0xD90	por_dn_vmf12_rnd	RW	5.3.2.57 por_dn_vmf12_rnd on page 323
0xD98	por_dn_vmf12_cxra	RW	5.3.2.58 por_dn_vmf12_cxra on page 324
0xDA0	por_dn_vmf13_ctrl	RW	5.3.2.59 por_dn_vmf13_ctrl on page 325
0xDA8	por_dn_vmf13_rnf0	RW	5.3.2.60 por_dn_vmf13_rnf0 on page 327
0xDB0	por_dn_vmf13_rnd	RW	5.3.2.61 por_dn_vmf13_rnd on page 328
0xDB8	por_dn_vmf13_cxra	RW	5.3.2.62 por_dn_vmf13_cxra on page 329
0xDC0	por_dn_vmf14_ctrl	RW	5.3.2.63 por_dn_vmf14_ctrl on page 330
0xDC8	por_dn_vmf14_rnf0	RW	5.3.2.64 por_dn_vmf14_rnf0 on page 331
0xDD0	por_dn_vmf14_rnd	RW	5.3.2.65 por_dn_vmf14_rnd on page 332

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Offset	Name	Type	Description
0xDD8	por_dn_vmf14_cxra	RW	5.3.2.66 por_dn_vmf14_cxra on page 333
0xDE0	por_dn_vmf15_ctrl	RW	5.3.2.67 por_dn_vmf15_ctrl on page 334
0xDE8	por_dn_vmf15_rnf0	RW	5.3.2.68 por_dn_vmf15_rnf0 on page 336
0xDF0	por_dn_vmf15_rnd	RW	5.3.2.69 por_dn_vmf15_rnd on page 337
0xDF8	por_dn_vmf15_cxra	RW	5.3.2.70 por_dn_vmf15_cxra on page 338
0x2000	por_dn_pmu_event_sel	RW	5.3.2.71 por_dn_pmu_event_sel on page 339

5.2.3 Debug and trace register summary

This section lists the debug and trace registers used in CI-700.

DT register summary

The following table shows the *DT* registers in offset order from the base memory address

Table 5-4: DT register summary

Offset	Name	Type	Description
0x0	por_dt_node_info	RO	5.3.3.1 por_dt_node_info on page 341
0x80	por_dt_child_info	RO	5.3.3.2 por_dt_child_info on page 342
0x980	por_dt_secure_access	RW	5.3.3.3 por_dt_secure_access on page 343
0xA00	por_dt_dtc_ctl	RW	5.3.3.4 por_dt_dtc_ctl on page 345
0xA10	por_dt_trigger_status	RO	5.3.3.5 por_dt_trigger_status on page 346
0xA20	por_dt_trigger_status_clr	WO	5.3.3.6 por_dt_trigger_status_clr on page 347
0xA30	por_dt_trace_control	RW	5.3.3.7 por_dt_trace_control on page 348
0xA48	por_dt_traceid	RW	5.3.3.8 por_dt_traceid on page 349
0x2000	por_dt_pmevcntAB	RW	5.3.3.9 por_dt_pmevcntAB on page 350
0x2010	por_dt_pmevcntCD	RW	5.3.3.10 por_dt_pmevcntCD on page 351
0x2020	por_dt_pmevcntEF	RW	5.3.3.11 por_dt_pmevcntEF on page 352
0x2030	por_dt_pmevcntGH	RW	5.3.3.12 por_dt_pmevcntGH on page 353
0x2040	por_dt_pmccntr	RW	5.3.3.13 por_dt_pmccntr on page 354
0x2050	por_dt_pmevcntsrAB	RW	5.3.3.14 por_dt_pmevcntsrAB on page 355
0x2060	por_dt_pmevcntsrCD	RW	5.3.3.15 por_dt_pmevcntsrCD on page 356
0x2070	por_dt_pmevcntsrEF	RW	5.3.3.16 por_dt_pmevcntsrEF on page 357
0x2080	por_dt_pmevcntsrGH	RW	5.3.3.17 por_dt_pmevcntsrGH on page 358
0x2090	por_dt_pmccntrsr	RW	5.3.3.18 por_dt_pmccntrsr on page 359
0x2100	por_dt_pmcr	RW	5.3.3.19 por_dt_pmcr on page 360
0x2118	por_dt_pmovsr	RO	5.3.3.20 por_dt_pmovsr on page 362
0x2120	por_dt_pmovsr_clr	WO	5.3.3.21 por_dt_pmovsr_clr on page 363
0x2128	por_dt_pmssr	RO	5.3.3.22 por_dt_pmssr on page 364
0x2130	por_dt_pmsrr	WO	5.3.3.23 por_dt_pmsrr on page 365

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Offset	Name	Type	Description
0xFA0	por_dt_claim	RW	5.3.3.24 por_dt_claim on page 366
0xFA8	por_dt_devaff	RO	5.3.3.25 por_dt_devaff on page 367
0xFB0	por_dt_lsr	RO	5.3.3.26 por_dt_lsr on page 368
0xFB8	por_dt_authstatus_devarch	RO	5.3.3.27 por_dt_authstatus_devarch on page 369
0xFC0	por_dt_devid	RO	5.3.3.28 por_dt_devid on page 370
0xFC8	por_dt_devtype	RO	5.3.3.29 por_dt_devtype on page 371
0xFD0	por_dt_pidr45	RO	5.3.3.30 por_dt_pidr45 on page 373
0xFD8	por_dt_pidr67	RO	5.3.3.31 por_dt_pidr67 on page 374
0xFE0	por_dt_pidr01	RO	5.3.3.32 por_dt_pidr01 on page 375
0xFE8	por_dt_pidr23	RO	5.3.3.33 por_dt_pidr23 on page 376
0xFF0	por_dt_cidr01	RO	5.3.3.34 por_dt_cidr01 on page 377
0xFF8	por_dt_cidr23	RO	5.3.3.35 por_dt_cidr23 on page 378

5.2.4 HN-F register summary

This section lists the HN-F registers used in CI-700.

HNF register summary

The following table shows the *HNF* registers in offset order from the base memory address

Table 5-5: HNF register summary

Offset	Name	Type	Description
0x0	por_hnf_node_info	RO	5.3.4.1 por_hnf_node_info on page 379
0x80	por_hnf_child_info	RO	5.3.4.2 por_hnf_child_info on page 380
0x980	por_hnf_secure_register_groups_override	RW	5.3.4.3 por_hnf_secure_register_groups_override on page 381
0x900	por_hnf_unit_info	RO	5.3.4.4 por_hnf_unit_info on page 383
0xA00	por_hnf_cfg_ctl	RW	5.3.4.5 por_hnf_cfg_ctl on page 386
0xA08	por_hnf_aux_ctl	RW	5.3.4.6 por_hnf_aux_ctl on page 388
0xA10	por_hnf_r2_aux_ctl	RW	5.3.4.7 por_hnf_r2_aux_ctl on page 393
0xA18	por_hnf_cbusy_limit_ctl	RW	5.3.4.8 por_hnf_cbusy_limit_ctl on page 395
0x1C00	por_hnf_ppu_pwpr	RW	5.3.4.9 por_hnf_ppu_pwpr on page 396
0x1C08	por_hnf_ppu_pwsr	RO	5.3.4.10 por_hnf_ppu_pwsr on page 398
0x1C14	por_hnf_ppu_misr	RO	5.3.4.11 por_hnf_ppu_misr on page 399
0x2BB0	por_hnf_ppu_idr0	RO	5.3.4.12 por_hnf_ppu_idr0 on page 400
0x2BB4	por_hnf_ppu_idr1	RO	5.3.4.13 por_hnf_ppu_idr1 on page 402
0x2BC8	por_hnf_ppu_iidr	RO	5.3.4.14 por_hnf_ppu_iidr on page 403
0x2BCC	por_hnf_ppu_aidr	RO	5.3.4.15 por_hnf_ppu_aidr on page 403
0x1D00	por_hnf_ppu_dyn_ret_threshold	RW	5.3.4.16 por_hnf_ppu_dyn_ret_threshold on page 404
0xA80	por_hnf_qos_band	RO	5.3.4.17 por_hnf_qos_band on page 405

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Offset	Name	Type	Description
0xA88	por_hnf_qos_reservation	RW	5.3.4.18 por_hnf_qos_reservation on page 407
0xA90	por_hnf_rn_starvation	RW	5.3.4.19 por_hnf_rn_starvation on page 408
0x3000	por_hnf_errfr	RO	5.3.4.20 por_hnf_errfr on page 410
0x3008	por_hnf_errctlr	RW	5.3.4.21 por_hnf_errctlr on page 411
0x3010	por_hnf_errstatus	W1C	5.3.4.22 por_hnf_errstatus on page 412
0x3018	por_hnf_erraddr	RW	5.3.4.23 por_hnf_erraddr on page 414
0x3020	por_hnf_errmisc	RW	5.3.4.24 por_hnf_errmisc on page 416
0x3030	por_hnf_err_inj	RW	5.3.4.25 por_hnf_err_inj on page 418
0x3038	por_hnf_byte_par_err_inj	WO	5.3.4.26 por_hnf_byte_par_err_inj on page 419
0x3100	por_hnf_errfr_NS	RO	5.3.4.27 por_hnf_errfr_NS on page 420
0x3108	por_hnf_errctlr_NS	RW	5.3.4.28 por_hnf_errctlr_NS on page 422
0x3110	por_hnf_errstatus_NS	W1C	5.3.4.29 por_hnf_errstatus_NS on page 423
0x3118	por_hnf_erraddr_NS	RW	5.3.4.30 por_hnf_erraddr_NS on page 425
0x3120	por_hnf_errmisc_NS	RW	5.3.4.31 por_hnf_errmisc_NS on page 426
0xC00	por_hnf_slc_lock_ways	RW	5.3.4.32 por_hnf_slc_lock_ways on page 428
0xC08	por_hnf_slc_lock_base0	RW	5.3.4.33 por_hnf_slc_lock_base0 on page 430
0xC10	por_hnf_slc_lock_base1	RW	5.3.4.34 por_hnf_slc_lock_base1 on page 431
0xC18	por_hnf_slc_lock_base2	RW	5.3.4.35 por_hnf_slc_lock_base2 on page 432
0xC20	por_hnf_slc_lock_base3	RW	5.3.4.36 por_hnf_slc_lock_base3 on page 433
0xC28	por_hnf_rni_region_vec	RW	5.3.4.37 por_hnf_rni_region_vec on page 434
0xC30	por_hnf_rnd_region_vec	RW	5.3.4.38 por_hnf_rnd_region_vec on page 435
0xC38	por_hnf_rnf_region_vec	RW	5.3.4.39 por_hnf_rnf_region_vec on page 436
0xC40	por_hnf_rnf_region_vec1	RW	5.3.4.40 por_hnf_rnf_region_vec1 on page 437
0xC48	por_hnf_slcway_partition0_rnf_vec	RW	5.3.4.41 por_hnf_slcway_partition0_rnf_vec on page 439
0xC50	por_hnf_slcway_partition1_rnf_vec	RW	5.3.4.42 por_hnf_slcway_partition1_rnf_vec on page 440
0xC58	por_hnf_slcway_partition2_rnf_vec	RW	5.3.4.43 por_hnf_slcway_partition2_rnf_vec on page 441
0xC60	por_hnf_slcway_partition3_rnf_vec	RW	5.3.4.44 por_hnf_slcway_partition3_rnf_vec on page 442
0xCB0	por_hnf_slcway_partition0_rnf_vec1	RW	5.3.4.45 por_hnf_slcway_partition0_rnf_vec1 on page 443
0xCB8	por_hnf_slcway_partition1_rnf_vec1	RW	5.3.4.46 por_hnf_slcway_partition1_rnf_vec1 on page 444
0xCC0	por_hnf_slcway_partition2_rnf_vec1	RW	5.3.4.47 por_hnf_slcway_partition2_rnf_vec1 on page 445
0xCC8	por_hnf_slcway_partition3_rnf_vec1	RW	5.3.4.48 por_hnf_slcway_partition3_rnf_vec1 on page 446
0xC68	por_hnf_slcway_partition0_rni_vec	RW	5.3.4.49 por_hnf_slcway_partition0_rni_vec on page 447
0xC70	por_hnf_slcway_partition1_rni_vec	RW	5.3.4.50 por_hnf_slcway_partition1_rni_vec on page 448
0xC78	por_hnf_slcway_partition2_rni_vec	RW	5.3.4.51 por_hnf_slcway_partition2_rni_vec on page 449
0xC80	por_hnf_slcway_partition3_rni_vec	RW	5.3.4.52 por_hnf_slcway_partition3_rni_vec on page 450
0xC88	por_hnf_slcway_partition0_rnd_vec	RW	5.3.4.53 por_hnf_slcway_partition0_rnd_vec on page 451
0xC90	por_hnf_slcway_partition1_rnd_vec	RW	5.3.4.54 por_hnf_slcway_partition1_rnd_vec on page 452
0xC98	por_hnf_slcway_partition2_rnd_vec	RW	5.3.4.55 por_hnf_slcway_partition2_rnd_vec on page 453
0xCA0	por_hnf_slcway_partition3_rnd_vec	RW	5.3.4.56 por_hnf_slcway_partition3_rnd_vec on page 454

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Offset	Name	Type	Description
0xCA8	por_hnf_rn_region_lock	RW	5.3.4.57 por_hnf_rn_region_lock on page 455
0xCD0	por_hnf_sf_cxg_blocked_ways	RW	5.3.4.58 por_hnf_sf_cxg_blocked_ways on page 456
0xCF0	hn_sam_hash_addr_mask_reg	RW	5.3.4.59 hn_sam_hash_addr_mask_reg on page 457
0xCF8	hn_sam_region_cmp_addr_mask_reg	RW	5.3.4.60 hn_sam_region_cmp_addr_mask_reg on page 458
0xD00	por_hnf_sam_control	RW	5.3.4.61 por_hnf_sam_control on page 460
0xD08	por_hnf_sam_memregion0	RW	5.3.4.62 por_hnf_sam_memregion0 on page 461
0xD10	por_hnf_sam_memregion1	RW	5.3.4.63 por_hnf_sam_memregion1 on page 463
0xD18	por_hnf_sam_sn_properties	RW	5.3.4.64 por_hnf_sam_sn_properties on page 465
0xD20	por_hnf_sam_6sn_nodeid	RW	5.3.4.65 por_hnf_sam_6sn_nodeid on page 469
0xCE8	por_hnf_sam_sn_properties1	RW	5.3.4.66 por_hnf_sam_sn_properties1 on page 470
0xD28	por_hnf_rn_phys_id0	RW	5.3.4.67 por_hnf_rn_phys_id0 on page 473
0xD30	por_hnf_rn_phys_id1	RW	5.3.4.68 por_hnf_rn_phys_id1 on page 475
0xD38	por_hnf_rn_phys_id2	RW	5.3.4.69 por_hnf_rn_phys_id2 on page 477
0xD40	por_hnf_rn_phys_id3	RW	5.3.4.70 por_hnf_rn_phys_id3 on page 480
0xD48	por_hnf_rn_phys_id4	RW	5.3.4.71 por_hnf_rn_phys_id4 on page 482
0xD50	por_hnf_rn_phys_id5	RW	5.3.4.72 por_hnf_rn_phys_id5 on page 484
0xD58	por_hnf_rn_phys_id6	RW	5.3.4.73 por_hnf_rn_phys_id6 on page 487
0xD60	por_hnf_rn_phys_id7	RW	5.3.4.74 por_hnf_rn_phys_id7 on page 489
0xD68	por_hnf_rn_phys_id8	RW	5.3.4.75 por_hnf_rn_phys_id8 on page 492
0xD70	por_hnf_rn_phys_id9	RW	5.3.4.76 por_hnf_rn_phys_id9 on page 494
0xD78	por_hnf_rn_phys_id10	RW	5.3.4.77 por_hnf_rn_phys_id10 on page 497
0xD80	por_hnf_rn_phys_id11	RW	5.3.4.78 por_hnf_rn_phys_id11 on page 499
0xD88	por_hnf_rn_phys_id12	RW	5.3.4.79 por_hnf_rn_phys_id12 on page 502
0xD90	por_hnf_rn_phys_id13	RW	5.3.4.80 por_hnf_rn_phys_id13 on page 504
0xD98	por_hnf_rn_phys_id14	RW	5.3.4.81 por_hnf_rn_phys_id14 on page 507
0xDA0	por_hnf_rn_phys_id15	RW	5.3.4.82 por_hnf_rn_phys_id15 on page 509
0xDA8	por_hnf_rn_phys_id16	RW	5.3.4.83 por_hnf_rn_phys_id16 on page 512
0xDB0	por_hnf_rn_phys_id17	RW	5.3.4.84 por_hnf_rn_phys_id17 on page 514
0xDB8	por_hnf_rn_phys_id18	RW	5.3.4.85 por_hnf_rn_phys_id18 on page 517
0xDC0	por_hnf_rn_phys_id19	RW	5.3.4.86 por_hnf_rn_phys_id19 on page 519
0xDC8	por_hnf_rn_phys_id20	RW	5.3.4.87 por_hnf_rn_phys_id20 on page 522
0xDD0	por_hnf_rn_phys_id21	RW	5.3.4.88 por_hnf_rn_phys_id21 on page 524
0xDD8	por_hnf_rn_phys_id22	RW	5.3.4.89 por_hnf_rn_phys_id22 on page 527
0xDE0	por_hnf_rn_phys_id23	RW	5.3.4.90 por_hnf_rn_phys_id23 on page 529
0xDE8	por_hnf_rn_phys_id24	RW	5.3.4.91 por_hnf_rn_phys_id24 on page 532
0xDF0	por_hnf_rn_phys_id25	RW	5.3.4.92 por_hnf_rn_phys_id25 on page 534
0xDF8	por_hnf_rn_phys_id26	RW	5.3.4.93 por_hnf_rn_phys_id26 on page 537
0xE00	por_hnf_rn_phys_id27	RW	5.3.4.94 por_hnf_rn_phys_id27 on page 539
0xE08	por_hnf_rn_phys_id28	RW	5.3.4.95 por_hnf_rn_phys_id28 on page 542

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Offset	Name	Type	Description
0xE10	por_hnf_rn_phys_id29	RW	5.3.4.96 por_hnf_rn_phys_id29 on page 544
0xE18	por_hnf_rn_phys_id30	RW	5.3.4.97 por_hnf_rn_phys_id30 on page 547
0xE20	por_hnf_rn_phys_id31	RW	5.3.4.98 por_hnf_rn_phys_id31 on page 549
0xE28	por_hnf_rn_phys_id32	RW	5.3.4.99 por_hnf_rn_phys_id32 on page 552
0xE30	por_hnf_rn_phys_id33	RW	5.3.4.100 por_hnf_rn_phys_id33 on page 554
0xE38	por_hnf_rn_phys_id34	RW	5.3.4.101 por_hnf_rn_phys_id34 on page 557
0xE40	por_hnf_rn_phys_id35	RW	5.3.4.102 por_hnf_rn_phys_id35 on page 559
0xE48	por_hnf_rn_phys_id36	RW	5.3.4.103 por_hnf_rn_phys_id36 on page 562
0xE50	por_hnf_rn_phys_id37	RW	5.3.4.104 por_hnf_rn_phys_id37 on page 564
0xE58	por_hnf_rn_phys_id38	RW	5.3.4.105 por_hnf_rn_phys_id38 on page 567
0xE60	por_hnf_rn_phys_id39	RW	5.3.4.106 por_hnf_rn_phys_id39 on page 569
0xE68	por_hnf_rn_phys_id40	RW	5.3.4.107 por_hnf_rn_phys_id40 on page 572
0xE70	por_hnf_rn_phys_id41	RW	5.3.4.108 por_hnf_rn_phys_id41 on page 574
0xE78	por_hnf_rn_phys_id42	RW	5.3.4.109 por_hnf_rn_phys_id42 on page 577
0xE80	por_hnf_rn_phys_id43	RW	5.3.4.110 por_hnf_rn_phys_id43 on page 579
0xE88	por_hnf_rn_phys_id44	RW	5.3.4.111 por_hnf_rn_phys_id44 on page 582
0xE90	por_hnf_rn_phys_id45	RW	5.3.4.112 por_hnf_rn_phys_id45 on page 584
0xE98	por_hnf_rn_phys_id46	RW	5.3.4.113 por_hnf_rn_phys_id46 on page 587
0xEA0	por_hnf_rn_phys_id47	RW	5.3.4.114 por_hnf_rn_phys_id47 on page 589
0xEA8	por_hnf_rn_phys_id48	RW	5.3.4.115 por_hnf_rn_phys_id48 on page 592
0xEB0	por_hnf_rn_phys_id49	RW	5.3.4.116 por_hnf_rn_phys_id49 on page 594
0xEB8	por_hnf_rn_phys_id50	RW	5.3.4.117 por_hnf_rn_phys_id50 on page 597
0xEC0	por_hnf_rn_phys_id51	RW	5.3.4.118 por_hnf_rn_phys_id51 on page 599
0xEC8	por_hnf_rn_phys_id52	RW	5.3.4.119 por_hnf_rn_phys_id52 on page 602
0xED0	por_hnf_rn_phys_id53	RW	5.3.4.120 por_hnf_rn_phys_id53 on page 604
0xED8	por_hnf_rn_phys_id54	RW	5.3.4.121 por_hnf_rn_phys_id54 on page 607
0xEE0	por_hnf_rn_phys_id55	RW	5.3.4.122 por_hnf_rn_phys_id55 on page 609
0xEE8	por_hnf_rn_phys_id56	RW	5.3.4.123 por_hnf_rn_phys_id56 on page 612
0xEF0	por_hnf_rn_phys_id57	RW	5.3.4.124 por_hnf_rn_phys_id57 on page 614
0xEF8	por_hnf_rn_phys_id58	RW	5.3.4.125 por_hnf_rn_phys_id58 on page 617
0xF00	por_hnf_rn_phys_id59	RW	5.3.4.126 por_hnf_rn_phys_id59 on page 619
0xF08	por_hnf_rn_phys_id60	RW	5.3.4.127 por_hnf_rn_phys_id60 on page 622
0xF10	por_hnf_rn_phys_id61	RW	5.3.4.128 por_hnf_rn_phys_id61 on page 624
0xF18	por_hnf_rn_phys_id62	RW	5.3.4.129 por_hnf_rn_phys_id62 on page 627
0xF20	por_hnf_rn_phys_id63	RW	5.3.4.130 por_hnf_rn_phys_id63 on page 629
0xF28	por_hnf_ldid_map_table_reg0	RW	5.3.4.131 por_hnf_ldid_map_table_reg0 on page 632
0xF30	por_hnf_ldid_map_table_reg1	RW	5.3.4.132 por_hnf_ldid_map_table_reg1 on page 633
0xF38	por_hnf_ldid_map_table_reg2	RW	5.3.4.133 por_hnf_ldid_map_table_reg2 on page 635
0xF40	por_hnf_ldid_map_table_reg3	RW	5.3.4.134 por_hnf_ldid_map_table_reg3 on page 636

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Offset	Name	Type	Description
0xF48	por_hnf_ldid_map_table_reg4	RW	5.3.4.135 por_hnf_ldid_map_table_reg4 on page 637
0xF80	por_hnf_cml_port_aggr_grp0_add_mask	RW	5.3.4.136 por_hnf_cml_port_aggr_grp0_add_mask on page 639
0xF88	por_hnf_cml_port_aggr_grp1_add_mask	RW	5.3.4.137 por_hnf_cml_port_aggr_grp1_add_mask on page 640
0xF90	por_hnf_cml_port_aggr_grp2_add_mask	RW	5.3.4.138 por_hnf_cml_port_aggr_grp2_add_mask on page 641
0xF98	por_hnf_cml_port_aggr_grp3_add_mask	RW	5.3.4.139 por_hnf_cml_port_aggr_grp3_add_mask on page 642
0xFA0	por_hnf_cml_port_aggr_grp4_add_mask	RW	5.3.4.140 por_hnf_cml_port_aggr_grp4_add_mask on page 644
0xFB0	por_hnf_cml_port_aggr_grp_reg0	RW	5.3.4.141 por_hnf_cml_port_aggr_grp_reg0 on page 645
0xFB8	por_hnf_cml_port_aggr_grp_reg1	RW	5.3.4.142 por_hnf_cml_port_aggr_grp_reg1 on page 646
0xFD0	por_hnf_cml_port_aggr_ctrl_reg	RW	5.3.4.143 por_hnf_cml_port_aggr_ctrl_reg on page 648
0xF50	por_hnf_abf_lo_addr	RW	5.3.4.144 por_hnf_abf_lo_addr on page 650
0xF58	por_hnf_abf_hi_addr	RW	5.3.4.145 por_hnf_abf_hi_addr on page 651
0xF60	por_hnf_abf_pr	RW	5.3.4.146 por_hnf_abf_pr on page 652
0xF68	por_hnf_abf_sr	RO	5.3.4.147 por_hnf_abf_sr on page 654
0x1000	por_hnf_cbusy_write_limit_ctl	RW	5.3.4.148 por_hnf_cbusy_write_limit_ctl on page 655
0x1008	por_hnf_cbusy_resp_ctl	RW	5.3.4.149 por_hnf_cbusy_resp_ctl on page 656
0x1010	por_hnf_cbusy_sn_ctl	RW	5.3.4.150 por_hnf_cbusy_sn_ctl on page 658
0xFE0	por_hnf_partner_scratch_reg0	RW	5.3.4.151 por_hnf_partner_scratch_reg0 on page 659
0xFE8	por_hnf_partner_scratch_reg1	RW	5.3.4.152 por_hnf_partner_scratch_reg1 on page 660
0xB80	por_hnf_cfg_slcsf_dbgrd	WO	5.3.4.153 por_hnf_cfg_slcsf_dbgrd on page 661
0xB88	por_hnf_slc_cache_access_slc_tag	RO	5.3.4.154 por_hnf_slc_cache_access_slc_tag on page 662
0xB90	por_hnf_slc_cache_access_slc_tag1	RO	5.3.4.155 por_hnf_slc_cache_access_slc_tag1 on page 663
0xB98	por_hnf_slc_cache_access_slc_data	RO	5.3.4.156 por_hnf_slc_cache_access_slc_data on page 664
0xBC0	por_hnf_slc_cache_access_slc_mte_tag	RO	5.3.4.157 por_hnf_slc_cache_access_slc_mte_tag on page 665
0xBA0	por_hnf_slc_cache_access_sf_tag	RO	5.3.4.158 por_hnf_slc_cache_access_sf_tag on page 666
0xBA8	por_hnf_slc_cache_access_sf_tag1	RO	5.3.4.159 por_hnf_slc_cache_access_sf_tag1 on page 667
0xBB0	por_hnf_slc_cache_access_sf_tag2	RO	5.3.4.160 por_hnf_slc_cache_access_sf_tag2 on page 668
0x2000	por_hnf_pmu_event_sel	RW	5.3.4.161 por_hnf_pmu_event_sel on page 669
0x2008	por_hnf_pmu_mpam_sel	RW	5.3.4.162 por_hnf_pmu_mpam_sel on page 673
0x2010	por_hnf_pmu_mpam_pardid_mask0	RW	5.3.4.163 por_hnf_pmu_mpam_pardid_mask0 on page 675
0x2018	por_hnf_pmu_mpam_pardid_mask1	RW	5.3.4.164 por_hnf_pmu_mpam_pardid_mask1 on page 676
0x2020	por_hnf_pmu_mpam_pardid_mask2	RW	5.3.4.165 por_hnf_pmu_mpam_pardid_mask2 on page 677
0x2028	por_hnf_pmu_mpam_pardid_mask3	RW	5.3.4.166 por_hnf_pmu_mpam_pardid_mask3 on page 678
0x2030	por_hnf_pmu_mpam_pardid_mask4	RW	5.3.4.167 por_hnf_pmu_mpam_pardid_mask4 on page 680
0x2038	por_hnf_pmu_mpam_pardid_mask5	RW	5.3.4.168 por_hnf_pmu_mpam_pardid_mask5 on page 681
0x2040	por_hnf_pmu_mpam_pardid_mask6	RW	5.3.4.169 por_hnf_pmu_mpam_pardid_mask6 on page 682
0x2048	por_hnf_pmu_mpam_pardid_mask7	RW	5.3.4.170 por_hnf_pmu_mpam_pardid_mask7 on page 683

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5.2.5 HN-I register summary

This section lists the HN-I registers used in CI-700.

HNI register summary

The following table shows the *HNI* registers in offset order from the base memory address

Table 5-6: HNI register summary

Offset	Name	Type	Description
0x0	por_hni_node_info	RO	5.3.5.1 por_hni_node_info on page 685
0x80	por_hni_child_info	RO	5.3.5.2 por_hni_child_info on page 686
0x980	por_hni_secure_register_groups_override	RW	5.3.5.3 por_hni_secure_register_groups_override on page 687
0x900	por_hni_unit_info	RO	5.3.5.4 por_hni_unit_info on page 688
0xC00	por_hni_sam_addrregion0_cfg	RW	5.3.5.5 por_hni_sam_addrregion0_cfg on page 690
0xC08	por_hni_sam_addrregion1_cfg	RW	5.3.5.6 por_hni_sam_addrregion1_cfg on page 691
0xC10	por_hni_sam_addrregion2_cfg	RW	5.3.5.7 por_hni_sam_addrregion2_cfg on page 693
0xC18	por_hni_sam_addrregion3_cfg	RW	5.3.5.8 por_hni_sam_addrregion3_cfg on page 695
0xA00	por_hni_cfg_ctl	RW	5.3.5.9 por_hni_cfg_ctl on page 697
0xA08	por_hni_aux_ctl	RW	5.3.5.10 por_hni_aux_ctl on page 698
0x3000	por_hni_errfr	RO	5.3.5.11 por_hni_errfr on page 699
0x3008	por_hni_errctlr	RW	5.3.5.12 por_hni_errctlr on page 701
0x3010	por_hni_errstatus	W1C	5.3.5.13 por_hni_errstatus on page 702
0x3018	por_hni_erraddr	RW	5.3.5.14 por_hni_erraddr on page 704
0x3020	por_hni_errmisc	RW	5.3.5.15 por_hni_errmisc on page 705
0x3100	por_hni_errfr_NS	RO	5.3.5.16 por_hni_errfr_NS on page 708
0x3108	por_hni_errctlr_NS	RW	5.3.5.17 por_hni_errctlr_NS on page 709
0x3110	por_hni_errstatus_NS	W1C	5.3.5.18 por_hni_errstatus_NS on page 711
0x3118	por_hni_erraddr_NS	RW	5.3.5.19 por_hni_erraddr_NS on page 713
0x3120	por_hni_errmisc_NS	RW	5.3.5.20 por_hni_errmisc_NS on page 714
0x2000	por_hni_pmu_event_sel	RW	5.3.5.21 por_hni_pmu_event_sel on page 716

5.2.6 XP register summary

This section lists the XP registers used in CI-700.

MXP register summary

The following table shows the *MXP* registers in offset order from the base memory address

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Note

Some offsets in this table are defined by specific types of base address in the component configuration register region. For more information about these base addresses, see Table 5-1: Configuration register region values on page 180.

Table 5-7: MXP register summary

Offset	Name	Type	Description
0x0	por_mxp_node_info	RO	5.3.6.1 por_mxp_node_info on page 718
0x8	por_mxp_device_port_connect_info_p0	RO	5.3.6.2 por_mxp_device_port_connect_info_p0 on page 720
0x10	por_mxp_device_port_connect_info_p1	RO	5.3.6.3 por_mxp_device_port_connect_info_p1 on page 723
0x18	por_mxp_mesh_port_connect_info_east	RO	5.3.6.4 por_mxp_mesh_port_connect_info_east on page 726
0x20	por_mxp_mesh_port_connect_info_north	RO	5.3.6.5 por_mxp_mesh_port_connect_info_north on page 727
0xNODE_TYPE_BASE + 16'h28 + (8 * ($index-2))	por_mxp_device_port_connect_info_p $index	RO	5.3.6.6 por_mxp_device_port_connect_info_p $index on page 728
0x80	por_mxp_child_info	RO	5.3.6.7 por_mxp_child_info on page 731
0xCHILD_POINTER_BASE + 16'h0 + (8 * $index)	por_mxp_child_pointer_$index	RO	5.3.6.8 por_mxp_child_pointer_$index on page 732
0xCHILD_POINTER_BASE + 16'h0 + (8 * $index)	por_mxp_child_pointer_$index	RO	5.3.6.9 por_mxp_child_pointer_$index on page 733
0x900	por_mxp_p0_info	RO	5.3.6.10 por_mxp_p0_info on page 734
0x908	por_mxp_p1_info	RO	5.3.6.11 por_mxp_p1_info on page 735
0x910	por_dtm_unit_info	RO	5.3.6.12 por_dtm_unit_info on page 737
0xUNIT_REGISTER_BASE + UNIT_INFO_BASE + 16'h18 + (8 * ($index-1))	por_dtm_unit_info_dt$index	RO	5.3.6.13 por_dtm_unit_info_dt$index on page 738
0xUNIT_REGISTER_BASE + UNIT_INFO_BASE + 16'h28 + (8 * ($index-2))	por_mxp_p$index_info	RO	5.3.6.14 por_mxp_p$index_info on page 739
0x980	por_mxp_secure_register_groups_override	RW	5.3.6.15 por_mxp_secure_register_groups_override on page 741
0xA00	por_mxp_aux_ctl	RW	5.3.6.16 por_mxp_aux_ctl on page 742
0xUNIT_REGISTER_BASE + UNIT_CTRL_BASE + 16'h08 + (8 * $index)	por_mxp_p$index_mpam_override	RW	5.3.6.17 por_mxp_p $index_mpam_override on page 743

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Offset	Name	Type	Description
0xUNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h000 + (32 * $index)	por_mxp_p$index_qos_control	RW	5.3.6.18 por_mxp_p$index_qos_control on page 744
0xUNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h008 + (32 * $index)	por_mxp_p$index_qos_lat_tgt	RW	5.3.6.19 por_mxp_p$index_qos_lat_tgt on page 746
0xUNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h010 + (32 * $index)	por_mxp_p$index_qos_lat_scale	RW	5.3.6.20 por_mxp_p$index_qos_lat_scale on page 747
0xUNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h018 + (32 * $index)	por_mxp_p$index_qos_lat_range	RW	5.3.6.21 por_mxp_p$index_qos_lat_range on page 748
0x2000	por_mxp_pmu_event_sel	RW	5.3.6.22 por_mxp_pmu_event_sel on page 750
0x3000	por_mxp_errfr	RO	5.3.6.23 por_mxp_errfr on page 752
0x3008	por_mxp_errctlr	RW	5.3.6.24 por_mxp_errctlr on page 754
0x3010	por_mxp_errstatus	W1C	5.3.6.25 por_mxp_errstatus on page 755
0x3028	por_mxp_errmisc	RW	5.3.6.26 por_mxp_errmisc on page 757
0xUNIT_REGISTER_BASE + UNIT_S_ERROR_BASE + 16'h030 + (8 * $index)	por_mxp_p$index_byte_par_err_inj	WO	5.3.6.27 por_mxp_p $index_byte_par_err_inj on page 759
0x3100	por_mxp_errfr_NS	RO	5.3.6.28 por_mxp_errfr_NS on page 760
0x3108	por_mxp_errctlr_NS	RW	5.3.6.29 por_mxp_errctlr_NS on page 761
0x3110	por_mxp_errstatus_NS	W1C	5.3.6.30 por_mxp_errstatus_NS on page 763
0x3128	por_mxp_errmisc_NS	RW	5.3.6.31 por_mxp_errmisc_NS on page 765
0xUNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h0 + (8 * $index)	por_mxp_p$index_syscoreq_ctl	RW	5.3.6.32 por_mxp_p$index_syscoreq_ctl on page 767
0xUNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h10 + (8 * $index)	por_mxp_p$index_syscoack_status	RO	5.3.6.33 por_mxp_p $index_syscoack_status on page 768
0xUNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h20 + (8 * ($index-2))	por_mxp_p$index_syscoreq_ctl	RW	5.3.6.34 por_mxp_p$index_syscoreq_ctl on page 770
0xUNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h40 + (8 * ($index-2))	por_mxp_p$index_syscoack_status	RO	5.3.6.35 por_mxp_p $index_syscoack_status on page 771
0x2100	por_dtm_control	RW	5.3.6.36 por_dtm_control on page 772
0x2118	por_dtm_fifo_entry_ready	W1C	5.3.6.37 por_dtm_fifo_entry_ready on page 774
0x2120	por_dtm_fifo_entry0_0	RO	5.3.6.38 por_dtm_fifo_entry0_0 on page 775

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Offset	Name	Type	Description
0x2128	por_dtm_fifo_entry0_1	RO	5.3.6.39 por_dtm_fifo_entry0_1 on page 776
0x2130	por_dtm_fifo_entry0_2	RO	5.3.6.40 por_dtm_fifo_entry0_2 on page 777
0x2138	por_dtm_fifo_entry1_0	RO	5.3.6.41 por_dtm_fifo_entry1_0 on page 778
0x2140	por_dtm_fifo_entry1_1	RO	5.3.6.42 por_dtm_fifo_entry1_1 on page 779
0x2148	por_dtm_fifo_entry1_2	RO	5.3.6.43 por_dtm_fifo_entry1_2 on page 780
0x2150	por_dtm_fifo_entry2_0	RO	5.3.6.44 por_dtm_fifo_entry2_0 on page 781
0x2158	por_dtm_fifo_entry2_1	RO	5.3.6.45 por_dtm_fifo_entry2_1 on page 782
0x2160	por_dtm_fifo_entry2_2	RO	5.3.6.46 por_dtm_fifo_entry2_2 on page 783
0x2168	por_dtm_fifo_entry3_0	RO	5.3.6.47 por_dtm_fifo_entry3_0 on page 784
0x2170	por_dtm_fifo_entry3_1	RO	5.3.6.48 por_dtm_fifo_entry3_1 on page 785
0x2178	por_dtm_fifo_entry3_2	RO	5.3.6.49 por_dtm_fifo_entry3_2 on page 786
0x21A0	por_dtm_wp0_config	RW	5.3.6.50 por_dtm_wp0_config on page 787
0x21A8	por_dtm_wp0_val	RW	5.3.6.51 por_dtm_wp0_val on page 790
0x21B0	por_dtm_wp0_mask	RW	5.3.6.52 por_dtm_wp0_mask on page 791
0x21B8	por_dtm_wp1_config	RW	5.3.6.53 por_dtm_wp1_config on page 792
0x21C0	por_dtm_wp1_val	RW	5.3.6.54 por_dtm_wp1_val on page 794
0x21C8	por_dtm_wp1_mask	RW	5.3.6.55 por_dtm_wp1_mask on page 795
0x21D0	por_dtm_wp2_config	RW	5.3.6.56 por_dtm_wp2_config on page 796
0x21D8	por_dtm_wp2_val	RW	5.3.6.57 por_dtm_wp2_val on page 799
0x21E0	por_dtm_wp2_mask	RW	5.3.6.58 por_dtm_wp2_mask on page 800
0x21E8	por_dtm_wp3_config	RW	5.3.6.59 por_dtm_wp3_config on page 801
0x21F0	por_dtm_wp3_val	RW	5.3.6.60 por_dtm_wp3_val on page 803
0x21F8	por_dtm_wp3_mask	RW	5.3.6.61 por_dtm_wp3_mask on page 804

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Offset	Name	Type	Description
0x2200	por_dtm_pmsicr	RW	5.3.6.62 por_dtm_pmsicr on page 805
0x2208	por_dtm_pmsirr	RW	5.3.6.63 por_dtm_pmsirr on page 806
0x2210	por_dtm_pmu_config	RW	5.3.6.64 por_dtm_pmu_config on page 807
0x2220	por_dtm_pmevcnt	RW	5.3.6.65 por_dtm_pmevcnt on page 814
0x2240	por_dtm_pmevcntsr	RW	5.3.6.66 por_dtm_pmevcntsr on page 815
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h000 + (512 * $index)	por_dtm_control_dt$index	RW	5.3.6.67 por_dtm_control_dt$index on page 816
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h018 + (512 * $index)	por_dtm_fifo_entry_ready_dt$index	W1C	5.3.6.68 por_dtm_fifo_entry_ready_dt$index on page 818
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h020 + (512 * $index)	por_dtm_fifo_entry0_0_dt$index	RO	5.3.6.69 por_dtm_fifo_entry0_0_dt$index on page 819
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h028 + (512 * $index)	por_dtm_fifo_entry0_1_dt$index	RO	5.3.6.70 por_dtm_fifo_entry0_1_dt$index on page 820
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h030 + (512 * $index)	por_dtm_fifo_entry0_2_dt$index	RO	5.3.6.71 por_dtm_fifo_entry0_2_dt$index on page 821
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h038 + (512 * $index)	por_dtm_fifo_entry1_0_dt$index	RO	5.3.6.72 por_dtm_fifo_entry1_0_dt$index on page 822
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h040 + (512 * $index)	por_dtm_fifo_entry1_1_dt$index	RO	5.3.6.73 por_dtm_fifo_entry1_1_dt$index on page 823
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h048 + (512 * $index)	por_dtm_fifo_entry1_2_dt$index	RO	5.3.6.74 por_dtm_fifo_entry1_2_dt$index on page 824
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h050 + (512 * $index)	por_dtm_fifo_entry2_0_dt$index	RO	5.3.6.75 por_dtm_fifo_entry2_0_dt$index on page 825
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h058 + (512 * $index)	por_dtm_fifo_entry2_1_dt$index	RO	5.3.6.76 por_dtm_fifo_entry2_1_dt$index on page 826
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h060 + (512 * $index)	por_dtm_fifo_entry2_2_dt$index	RO	5.3.6.77 por_dtm_fifo_entry2_2_dt$index on page 827
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h068 + (512 * $index)	por_dtm_fifo_entry3_0_dt$index	RO	5.3.6.78 por_dtm_fifo_entry3_0_dt$index on page 828
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h070 + (512 * $index)	por_dtm_fifo_entry3_1_dt$index	RO	5.3.6.79 por_dtm_fifo_entry3_1_dt$index on page 829

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Offset	Name	Type	Description
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h078 + (512 * $index)	por_dtm_fifo_entry3_2_dt$index	RO	5.3.6.80 por_dtm_fifo_entry3_2_dt$index on page 830
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0a0 + (512 * $index)	por_dtm_wp0_config_dt$index	RW	5.3.6.81 por_dtm_wp0_config_dt$index on page 831
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0a8 + (512 * $index)	por_dtm_wp0_val_dt$index	RW	5.3.6.82 por_dtm_wp0_val_dt$index on page 834
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0b0 + (512 * $index)	por_dtm_wp0_mask_dt$index	RW	5.3.6.83 por_dtm_wp0_mask_dt$index on page 835
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0b8 + (512 * $index)	por_dtm_wp1_config_dt$index	RW	5.3.6.84 por_dtm_wp1_config_dt$index on page 836
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0c0 + (512 * $index)	por_dtm_wp1_val_dt$index	RW	5.3.6.85 por_dtm_wp1_val_dt$index on page 838
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0c8 + (512 * $index)	por_dtm_wp1_mask_dt$index	RW	5.3.6.86 por_dtm_wp1_mask_dt$index on page 839
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0d0 + (512 * $index)	por_dtm_wp2_config_dt$index	RW	5.3.6.87 por_dtm_wp2_config_dt$index on page 840
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0d8 + (512 * $index)	por_dtm_wp2_val_dt$index	RW	5.3.6.88 por_dtm_wp2_val_dt$index on page 843
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0e0 + (512 * $index)	por_dtm_wp2_mask_dt$index	RW	5.3.6.89 por_dtm_wp2_mask_dt$index on page 844
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0e8 + (512 * $index)	por_dtm_wp3_config_dt$index	RW	5.3.6.90 por_dtm_wp3_config_dt$index on page 845
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0f0 + (512 * $index)	por_dtm_wp3_val_dt$index	RW	5.3.6.91 por_dtm_wp3_val_dt$index on page 847
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0f8 + (512 * $index)	por_dtm_wp3_mask_dt$index	RW	5.3.6.92 por_dtm_wp3_mask_dt$index on page 848
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h100 + (512 * $index)	por_dtm_pmsicr_dt$index	RW	5.3.6.93 por_dtm_pmsicr_dt$index on page 849
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h108 + (512 * $index)	por_dtm_pmsirr_dt$index	RW	5.3.6.94 por_dtm_pmsirr_dt$index on page 850
0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h110 + (512 * $index)	por_dtm_pmu_config_dt$index	RW	5.3.6.95 por_dtm_pmu_config_dt$index on page 851

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Offset	Name	Type	Description
`0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h120 + (512 * $index)`	por_dtm_pmevcnt_dt$index	RW	5.3.6.96 por_dtm_pmevcnt_dt$index on page 855
`0xUNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h140 + (512 * $index)`	por_dtm_pmevcntsr_dt$index	RW	5.3.6.97 por_dtm_pmevcntsr_dt$index on page 856
`0xC90`	por_mxp_xy_override_sel_0	RW	5.3.6.98 por_mxp_xy_override_sel_0 on page 858
`0xC98`	por_mxp_xy_override_sel_1	RW	5.3.6.99 por_mxp_xy_override_sel_1 on page 859
`0xCA0`	por_mxp_xy_override_sel_2	RW	5.3.6.100 por_mxp_xy_override_sel_2 on page 861
`0xCA8`	por_mxp_xy_override_sel_3	RW	5.3.6.101 por_mxp_xy_override_sel_3 on page 863
`0xCB0`	por_mxp_xy_override_sel_4	RW	5.3.6.102 por_mxp_xy_override_sel_4 on page 864
`0xCB8`	por_mxp_xy_override_sel_5	RW	5.3.6.103 por_mxp_xy_override_sel_5 on page 866
`0xCC0`	por_mxp_xy_override_sel_6	RW	5.3.6.104 por_mxp_xy_override_sel_6 on page 868
`0xCC8`	por_mxp_xy_override_sel_7	RW	5.3.6.105 por_mxp_xy_override_sel_7 on page 869

5.2.7 RN-D register summary

This section lists the RN-D registers used in CI-700.

RND register summary

The following table shows the *RND* registers in offset order from the base memory address

Table 5-8: RND register summary

Offset	Name	Type	Description
`0x0`	por_rnd_node_info	RO	5.3.7.1 por_rnd_node_info on page 871
`0x80`	por_rnd_child_info	RO	5.3.7.2 por_rnd_child_info on page 872
`0x980`	por_rnd_secure_register_groups_override	RW	5.3.7.3 por_rnd_secure_register_groups_override on page 873
`0x900`	por_rnd_unit_info	RO	5.3.7.4 por_rnd_unit_info on page 874
`0x908`	por_rnd_unit_info2	RO	5.3.7.5 por_rnd_unit_info2 on page 876
`0xA00`	por_rnd_cfg_ctl	RW	5.3.7.6 por_rnd_cfg_ctl on page 877
`0xA08`	por_rnd_aux_ctl	RW	5.3.7.7 por_rnd_aux_ctl on page 880
`0xA10`	por_rnd_s0_port_control	RW	5.3.7.8 por_rnd_s0_port_control on page 882
`0xA18`	por_rnd_s1_port_control	RW	5.3.7.9 por_rnd_s1_port_control on page 883
`0xA20`	por_rnd_s2_port_control	RW	5.3.7.10 por_rnd_s2_port_control on page 884
`0xA28`	por_rnd_s0_mpam_control	RW	5.3.7.11 por_rnd_s0_mpam_control on page 885

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Offset	Name	Type	Description
0xA30	por_rnd_s1_mpam_control	RW	5.3.7.12 por_rnd_s1_mpam_control on page 887
0xA38	por_rnd_s2_mpam_control	RW	5.3.7.13 por_rnd_s2_mpam_control on page 888
0xA80	por_rnd_s0_qos_control	RW	5.3.7.14 por_rnd_s0_qos_control on page 890
0xA88	por_rnd_s0_qos_lat_tgt	RW	5.3.7.15 por_rnd_s0_qos_lat_tgt on page 892
0xA90	por_rnd_s0_qos_lat_scale	RW	5.3.7.16 por_rnd_s0_qos_lat_scale on page 893
0xA98	por_rnd_s0_qos_lat_range	RW	5.3.7.17 por_rnd_s0_qos_lat_range on page 895
0xAA0	por_rnd_s1_qos_control	RW	5.3.7.18 por_rnd_s1_qos_control on page 896
0xAA8	por_rnd_s1_qos_lat_tgt	RW	5.3.7.19 por_rnd_s1_qos_lat_tgt on page 898
0xAB0	por_rnd_s1_qos_lat_scale	RW	5.3.7.20 por_rnd_s1_qos_lat_scale on page 899
0xAB8	por_rnd_s1_qos_lat_range	RW	5.3.7.21 por_rnd_s1_qos_lat_range on page 901
0xAC0	por_rnd_s2_qos_control	RW	5.3.7.22 por_rnd_s2_qos_control on page 903
0xAC8	por_rnd_s2_qos_lat_tgt	RW	5.3.7.23 por_rnd_s2_qos_lat_tgt on page 905
0xAD0	por_rnd_s2_qos_lat_scale	RW	5.3.7.24 por_rnd_s2_qos_lat_scale on page 906
0xAD8	por_rnd_s2_qos_lat_range	RW	5.3.7.25 por_rnd_s2_qos_lat_range on page 908
0x2000	por_rnd_pmu_event_sel	RW	5.3.7.26 por_rnd_pmu_event_sel on page 909
0x1C00	por_rnd_syscoreq_ctl	RW	5.3.7.27 por_rnd_syscoreq_ctl on page 911
0x1C08	por_rnd_syscoack_status	RO	5.3.7.28 por_rnd_syscoack_status on page 913

5.2.8 RN-I register summary

This section lists the RN-I registers used in CI-700.

RNI register summary

The following table shows the *RNI* registers in offset order from the base memory address

Table 5-9: RNI register summary

Offset	Name	Type	Description
0x0	por_rni_node_info	RO	5.3.8.1 por_rni_node_info on page 914
0x80	por_rni_child_info	RO	5.3.8.2 por_rni_child_info on page 915
0x980	por_rni_secure_register_groups_override	RW	5.3.8.3 por_rni_secure_register_groups_override on page 916
0x900	por_rni_unit_info	RO	5.3.8.4 por_rni_unit_info on page 917
0x908	por_rni_unit_info2	RO	5.3.8.5 por_rni_unit_info2 on page 919
0xA00	por_rni_cfg_ctl	RW	5.3.8.6 por_rni_cfg_ctl on page 920
0xA08	por_rni_aux_ctl	RW	5.3.8.7 por_rni_aux_ctl on page 922
0xA10	por_rni_s0_port_control	RW	5.3.8.8 por_rni_s0_port_control on page 924
0xA18	por_rni_s1_port_control	RW	5.3.8.9 por_rni_s1_port_control on page 925
0xA20	por_rni_s2_port_control	RW	5.3.8.10 por_rni_s2_port_control on page 926
0xA28	por_rni_s0_mpam_control	RW	5.3.8.11 por_rni_s0_mpam_control on page 928
0xA30	por_rni_s1_mpam_control	RW	5.3.8.12 por_rni_s1_mpam_control on page 929

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Offset	Name	Type	Description
0xA38	por_rni_s2_mpam_control	RW	5.3.8.13 por_rni_s2_mpam_control on page 931
0xA80	por_rni_s0_qos_control	RW	5.3.8.14 por_rni_s0_qos_control on page 932
0xA88	por_rni_s0_qos_lat_tgt	RW	5.3.8.15 por_rni_s0_qos_lat_tgt on page 934
0xA90	por_rni_s0_qos_lat_scale	RW	5.3.8.16 por_rni_s0_qos_lat_scale on page 935
0xA98	por_rni_s0_qos_lat_range	RW	5.3.8.17 por_rni_s0_qos_lat_range on page 937
0xAA0	por_rni_s1_qos_control	RW	5.3.8.18 por_rni_s1_qos_control on page 939
0xAA8	por_rni_s1_qos_lat_tgt	RW	5.3.8.19 por_rni_s1_qos_lat_tgt on page 941
0xAB0	por_rni_s1_qos_lat_scale	RW	5.3.8.20 por_rni_s1_qos_lat_scale on page 942
0xAB8	por_rni_s1_qos_lat_range	RW	5.3.8.21 por_rni_s1_qos_lat_range on page 944
0xAC0	por_rni_s2_qos_control	RW	5.3.8.22 por_rni_s2_qos_control on page 945
0xAC8	por_rni_s2_qos_lat_tgt	RW	5.3.8.23 por_rni_s2_qos_lat_tgt on page 947
0xAD0	por_rni_s2_qos_lat_scale	RW	5.3.8.24 por_rni_s2_qos_lat_scale on page 948
0xAD8	por_rni_s2_qos_lat_range	RW	5.3.8.25 por_rni_s2_qos_lat_range on page 950
0x2000	por_rni_pmu_event_sel	RW	5.3.8.26 por_rni_pmu_event_sel on page 952

5.2.9 RN SAM register summary

This section lists the RN SAM registers used in CI-700.

RNSAM register summary

The following table shows the *RNSAM* registers in offset order from the base memory address

Table 5-10: RNSAM register summary

Offset	Name	Type	Description
0x0	por_rnsam_node_info	RO	5.3.9.1 por_rnsam_node_info on page 955
0x80	por_rnsam_child_info	RO	5.3.9.2 por_rnsam_child_info on page 956
0x980	por_rnsam_secure_register_groups_override	RW	5.3.9.3 por_rnsam_secure_register_groups_override on page 957
0x900	por_rnsam_unit_info	RO	5.3.9.4 por_rnsam_unit_info on page 958
0xC00	non_hash_mem_region_reg0	RW	5.3.9.5 non_hash_mem_region_reg0 on page 959
0xC08	non_hash_mem_region_reg1	RW	5.3.9.6 non_hash_mem_region_reg1 on page 961
0xC10	non_hash_mem_region_reg2	RW	5.3.9.7 non_hash_mem_region_reg2 on page 962
0xC18	non_hash_mem_region_reg3	RW	5.3.9.8 non_hash_mem_region_reg3 on page 964
0xC20	non_hash_mem_region_reg4	RW	5.3.9.9 non_hash_mem_region_reg4 on page 966
0xC28	non_hash_mem_region_reg5	RW	5.3.9.10 non_hash_mem_region_reg5 on page 968
0xC30	non_hash_mem_region_reg6	RW	5.3.9.11 non_hash_mem_region_reg6 on page 970
0xC38	non_hash_mem_region_reg7	RW	5.3.9.12 non_hash_mem_region_reg7 on page 971
0xC40	non_hash_mem_region_reg8	RW	5.3.9.13 non_hash_mem_region_reg8 on page 973
0xC48	non_hash_mem_region_reg9	RW	5.3.9.14 non_hash_mem_region_reg9 on page 975
0xC50	non_hash_mem_region_reg10	RW	5.3.9.15 non_hash_mem_region_reg10 on page 977

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Offset	Name	Type	Description
0xC58	non_hash_mem_region_reg11	RW	5.3.9.16 non_hash_mem_region_reg11 on page 979
0xC60	non_hash_mem_region_reg12	RW	5.3.9.17 non_hash_mem_region_reg12 on page 980
0xC68	non_hash_mem_region_reg13	RW	5.3.9.18 non_hash_mem_region_reg13 on page 982
0xC70	non_hash_mem_region_reg14	RW	5.3.9.19 non_hash_mem_region_reg14 on page 984
0xC78	non_hash_mem_region_reg15	RW	5.3.9.20 non_hash_mem_region_reg15 on page 986
0xC80	non_hash_mem_region_reg16	RW	5.3.9.21 non_hash_mem_region_reg16 on page 988
0xC88	non_hash_mem_region_reg17	RW	5.3.9.22 non_hash_mem_region_reg17 on page 989
0xC90	non_hash_mem_region_reg18	RW	5.3.9.23 non_hash_mem_region_reg18 on page 991
0xC98	non_hash_mem_region_reg19	RW	5.3.9.24 non_hash_mem_region_reg19 on page 993
0xD80	non_hash_tgt_nodeid0	RW	5.3.9.25 non_hash_tgt_nodeid0 on page 995
0xD88	non_hash_tgt_nodeid1	RW	5.3.9.26 non_hash_tgt_nodeid1 on page 996
0xD90	non_hash_tgt_nodeid2	RW	5.3.9.27 non_hash_tgt_nodeid2 on page 997
0xD98	non_hash_tgt_nodeid3	RW	5.3.9.28 non_hash_tgt_nodeid3 on page 999
0xDA0	non_hash_tgt_nodeid4	RW	5.3.9.29 non_hash_tgt_nodeid4 on page 1000
0xE00	sys_cache_grp_region0	RW	5.3.9.30 sys_cache_grp_region0 on page 1001
0xE08	sys_cache_grp_region1	RW	5.3.9.31 sys_cache_grp_region1 on page 1003
0xE10	sys_cache_grp_region2	RW	5.3.9.32 sys_cache_grp_region2 on page 1005
0xE18	sys_cache_grp_region3	RW	5.3.9.33 sys_cache_grp_region3 on page 1007
0xE40	sys_cache_grp_secondary_reg0	RW	5.3.9.34 sys_cache_grp_secondary_reg0 on page 1009
0xE48	sys_cache_grp_secondary_reg1	RW	5.3.9.35 sys_cache_grp_secondary_reg1 on page 1010
0xE50	sys_cache_grp_secondary_reg2	RW	5.3.9.36 sys_cache_grp_secondary_reg2 on page 1012
0xE58	sys_cache_grp_secondary_reg3	RW	5.3.9.37 sys_cache_grp_secondary_reg3 on page 1014
0xE80	rnsam_hash_addr_mask_reg	RW	5.3.9.38 rnsam_hash_addr_mask_reg on page 1016
0xE90	rnsam_region_cmp_addr_mask_reg	RW	5.3.9.39 rnsam_region_cmp_addr_mask_reg on page 1017
0xEA0	sys_cache_group_hn_count	RW	5.3.9.40 sys_cache_group_hn_count on page 1018
0xEB0	sys_cache_grp_sn_attr	RW	5.3.9.41 sys_cache_grp_sn_attr on page 1019
0xEC0	sys_cache_grp_nonhash_nodeid	RW	5.3.9.42 sys_cache_grp_nonhash_nodeid on page 1022
0xF00	sys_cache_grp_hn_nodeid_reg0	RW	5.3.9.43 sys_cache_grp_hn_nodeid_reg0 on page 1023
0xF08	sys_cache_grp_hn_nodeid_reg1	RW	5.3.9.44 sys_cache_grp_hn_nodeid_reg1 on page 1024
0xF10	sys_cache_grp_hn_nodeid_reg2	RW	5.3.9.45 sys_cache_grp_hn_nodeid_reg2 on page 1026
0xF18	sys_cache_grp_hn_nodeid_reg3	RW	5.3.9.46 sys_cache_grp_hn_nodeid_reg3 on page 1027
0xF20	sys_cache_grp_hn_nodeid_reg4	RW	5.3.9.47 sys_cache_grp_hn_nodeid_reg4 on page 1028
0xF28	sys_cache_grp_hn_nodeid_reg5	RW	5.3.9.48 sys_cache_grp_hn_nodeid_reg5 on page 1030
0xF30	sys_cache_grp_hn_nodeid_reg6	RW	5.3.9.49 sys_cache_grp_hn_nodeid_reg6 on page 1031
0xF38	sys_cache_grp_hn_nodeid_reg7	RW	5.3.9.50 sys_cache_grp_hn_nodeid_reg7 on page 1032
0xF40	sys_cache_grp_hn_nodeid_reg8	RW	5.3.9.51 sys_cache_grp_hn_nodeid_reg8 on page 1034
0xF48	sys_cache_grp_hn_nodeid_reg9	RW	5.3.9.52 sys_cache_grp_hn_nodeid_reg9 on page 1035
0xF50	sys_cache_grp_hn_nodeid_reg10	RW	5.3.9.53 sys_cache_grp_hn_nodeid_reg10 on page 1036
0xF58	sys_cache_grp_hn_nodeid_reg11	RW	5.3.9.54 sys_cache_grp_hn_nodeid_reg11 on page 1038

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Offset	Name	Type	Description
0xF60	sys_cache_grp_hn_nodeid_reg12	RW	5.3.9.55 sys_cache_grp_hn_nodeid_reg12 on page 1039
0xF68	sys_cache_grp_hn_nodeid_reg13	RW	5.3.9.56 sys_cache_grp_hn_nodeid_reg13 on page 1040
0xF70	sys_cache_grp_hn_nodeid_reg14	RW	5.3.9.57 sys_cache_grp_hn_nodeid_reg14 on page 1042
0xF78	sys_cache_grp_hn_nodeid_reg15	RW	5.3.9.58 sys_cache_grp_hn_nodeid_reg15 on page 1043
0x1000	sys_cache_grp_sn_nodeid_reg0	RW	5.3.9.59 sys_cache_grp_sn_nodeid_reg0 on page 1044
0x1008	sys_cache_grp_sn_nodeid_reg1	RW	5.3.9.60 sys_cache_grp_sn_nodeid_reg1 on page 1046
0x1010	sys_cache_grp_sn_nodeid_reg2	RW	5.3.9.61 sys_cache_grp_sn_nodeid_reg2 on page 1047
0x1018	sys_cache_grp_sn_nodeid_reg3	RW	5.3.9.62 sys_cache_grp_sn_nodeid_reg3 on page 1048
0x1020	sys_cache_grp_sn_nodeid_reg4	RW	5.3.9.63 sys_cache_grp_sn_nodeid_reg4 on page 1050
0x1028	sys_cache_grp_sn_nodeid_reg5	RW	5.3.9.64 sys_cache_grp_sn_nodeid_reg5 on page 1051
0x1030	sys_cache_grp_sn_nodeid_reg6	RW	5.3.9.65 sys_cache_grp_sn_nodeid_reg6 on page 1052
0x1038	sys_cache_grp_sn_nodeid_reg7	RW	5.3.9.66 sys_cache_grp_sn_nodeid_reg7 on page 1054
0x1040	sys_cache_grp_sn_nodeid_reg8	RW	5.3.9.67 sys_cache_grp_sn_nodeid_reg8 on page 1055
0x1048	sys_cache_grp_sn_nodeid_reg9	RW	5.3.9.68 sys_cache_grp_sn_nodeid_reg9 on page 1056
0x1050	sys_cache_grp_sn_nodeid_reg10	RW	5.3.9.69 sys_cache_grp_sn_nodeid_reg10 on page 1058
0x1058	sys_cache_grp_sn_nodeid_reg11	RW	5.3.9.70 sys_cache_grp_sn_nodeid_reg11 on page 1059
0x1060	sys_cache_grp_sn_nodeid_reg12	RW	5.3.9.71 sys_cache_grp_sn_nodeid_reg12 on page 1060
0x1068	sys_cache_grp_sn_nodeid_reg13	RW	5.3.9.72 sys_cache_grp_sn_nodeid_reg13 on page 1062
0x1070	sys_cache_grp_sn_nodeid_reg14	RW	5.3.9.73 sys_cache_grp_sn_nodeid_reg14 on page 1063
0x1078	sys_cache_grp_sn_nodeid_reg15	RW	5.3.9.74 sys_cache_grp_sn_nodeid_reg15 on page 1064
0x1100	rnsam_status	RW	5.3.9.75 rnsam_status on page 1066
0x1108	gic_mem_region_reg	RW	5.3.9.76 gic_mem_region_reg on page 1067
0x1120	sys_cache_grp_cal_mode_reg	RW	5.3.9.77 sys_cache_grp_cal_mode_reg on page 1069
0x1140	sys_cache_grp_sn_sam_cfg0	RW	5.3.9.78 sys_cache_grp_sn_sam_cfg0 on page 1070
0x1148	sys_cache_grp_sn_sam_cfg1	RW	5.3.9.79 sys_cache_grp_sn_sam_cfg1 on page 1072
0x1180	sys_cache_grp_hn_cpa_en_reg	RW	5.3.9.80 sys_cache_grp_hn_cpa_en_reg on page 1074
0x1190	sys_cache_grp_hn_cpa_grp_reg	RW	5.3.9.81 sys_cache_grp_hn_cpa_grp_reg on page 1075
0x11A0	cml_port_aggr_mode_ctrl_reg	RW	5.3.9.82 cml_port_aggr_mode_ctrl_reg on page 1077
0x11A8	cml_port_aggr_mode_ctrl_reg1	RW	5.3.9.83 cml_port_aggr_mode_ctrl_reg1 on page 1081
0x11C0	cml_port_aggr_grp0_add_mask	RW	5.3.9.84 cml_port_aggr_grp0_add_mask on page 1086
0x11C8	cml_port_aggr_grp1_add_mask	RW	5.3.9.85 cml_port_aggr_grp1_add_mask on page 1087
0x11D0	cml_port_aggr_grp2_add_mask	RW	5.3.9.86 cml_port_aggr_grp2_add_mask on page 1088
0x11D8	cml_port_aggr_grp3_add_mask	RW	5.3.9.87 cml_port_aggr_grp3_add_mask on page 1089
0x11E0	cml_port_aggr_grp4_add_mask	RW	5.3.9.88 cml_port_aggr_grp4_add_mask on page 1090
0x11F0	cml_port_aggr_grp_reg0	RW	5.3.9.89 cml_port_aggr_grp_reg0 on page 1091
0x11F8	cml_port_aggr_grp_reg1	RW	5.3.9.90 cml_port_aggr_grp_reg1 on page 1093
0x1208	cml_port_aggr_ctrl_reg	RW	5.3.9.91 cml_port_aggr_ctrl_reg on page 1094
0x1280	sam_qos_mem_region_reg0	RW	5.3.9.92 sam_qos_mem_region_reg0 on page 1097
0x1288	sam_qos_mem_region_reg1	RW	5.3.9.93 sam_qos_mem_region_reg1 on page 1098

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Offset	Name	Type	Description
0x1290	sam_qos_mem_region_reg2	RW	5.3.9.94 sam_qos_mem_region_reg2 on page 1100
0x1298	sam_qos_mem_region_reg3	RW	5.3.9.95 sam_qos_mem_region_reg3 on page 1102
0x12A0	sam_qos_mem_region_reg4	RW	5.3.9.96 sam_qos_mem_region_reg4 on page 1104
0x12A8	sam_qos_mem_region_reg5	RW	5.3.9.97 sam_qos_mem_region_reg5 on page 1105
0x12B0	sam_qos_mem_region_reg6	RW	5.3.9.98 sam_qos_mem_region_reg6 on page 1107
0x12B8	sam_qos_mem_region_reg7	RW	5.3.9.99 sam_qos_mem_region_reg7 on page 1109
0x1600	sam_generic_regs0	RW	5.3.9.100 sam_generic_regs0 on page 1111

5.2.10 SBSX register summary

This section lists the SBSX registers used in CI-700.

SBSX register summary

The following table shows the *SBSX* registers in offset order from the base memory address

Table 5-11: SBSX register summary

Offset	Name	Type	Description
0x0	por_sbsx_node_info	RO	5.3.10.1 por_sbsx_node_info on page 1112
0x80	por_sbsx_child_info	RO	5.3.10.2 por_sbsx_child_info on page 1113
0x980	por_sbsx_secure_register_groups_override	RW	5.3.10.3 por_sbsx_secure_register_groups_override on page 1114
0x900	por_sbsx_unit_info	RO	5.3.10.4 por_sbsx_unit_info on page 1115
0xA00	por_sbsx_cfg_ctl	RW	5.3.10.5 por_sbsx_cfg_ctl on page 1117
0xA08	por_sbsx_aux_ctl	RW	5.3.10.6 por_sbsx_aux_ctl on page 1118
0xA18	por_sbsx_cbusy_limit_ctl	RW	5.3.10.7 por_sbsx_cbusy_limit_ctl on page 1119
0x3000	por_sbsx_errfr	RO	5.3.10.8 por_sbsx_errfr on page 1120
0x3008	por_sbsx_errctlr	RW	5.3.10.9 por_sbsx_errctlr on page 1122
0x3010	por_sbsx_errstatus	W1C	5.3.10.10 por_sbsx_errstatus on page 1123
0x3018	por_sbsx_erraddr	RW	5.3.10.11 por_sbsx_erraddr on page 1125
0x3020	por_sbsx_errmisc	RW	5.3.10.12 por_sbsx_errmisc on page 1126
0x3100	por_sbsx_errfr_NS	RO	5.3.10.13 por_sbsx_errfr_NS on page 1128
0x3108	por_sbsx_errctlr_NS	RW	5.3.10.14 por_sbsx_errctlr_NS on page 1129
0x3110	por_sbsx_errstatus_NS	W1C	5.3.10.15 por_sbsx_errstatus_NS on page 1130
0x3118	por_sbsx_erraddr_NS	RW	5.3.10.16 por_sbsx_erraddr_NS on page 1132
0x3120	por_sbsx_errmisc_NS	RW	5.3.10.17 por_sbsx_errmisc_NS on page 1134
0x2000	por_sbsx_pmu_event_sel	RW	5.3.10.18 por_sbsx_pmu_event_sel on page 1135

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5.2.11 HN-F MPAM_NS register summary

This section lists the HN-F MPAM_NS registers used in CI-700.

HNF_MPAM_NS register summary

The following table shows the *HNF_MPAM_NS* registers in offset order from the base memory address

Table 5-12: HNF_MPAM_NS register summary

Offset	Name	Type	Description
0x0	por_hnf_mpam_ns_node_info	RO	5.3.11.1 por_hnf_mpam_ns_node_info on page 1137
0x80	por_hnf_mpam_ns_child_info	RO	5.3.11.2 por_hnf_mpam_ns_child_info on page 1139
0x1000	por_hnf_mpam_idr	RO	5.3.11.3 por_hnf_mpam_idr on page 1140
0x1018	por_hnf_mpam_iidr	RO	5.3.11.4 por_hnf_mpam_iidr on page 1141
0x1020	por_hnf_mpam_aidr	RO	5.3.11.5 por_hnf_mpam_aidr on page 1143
0x1028	por_hnf_mpam_impl_idr	RO	5.3.11.6 por_hnf_mpam_impl_idr on page 1144
0x1030	por_hnf_mpam_cpor_idr	RO	5.3.11.7 por_hnf_mpam_cpor_idr on page 1145
0x1038	por_hnf_mpam_ccap_idr	RO	5.3.11.8 por_hnf_mpam_ccap_idr on page 1146
0x1040	por_hnf_mpam_mbw_idr	RO	5.3.11.9 por_hnf_mpam_mbw_idr on page 1147
0x1048	por_hnf_mpam_pri_idr	RO	5.3.11.10 por_hnf_mpam_pri_idr on page 1149
0x1050	por_hnf_mpam_partid_nrw_idr	RO	5.3.11.11 por_hnf_mpam_partid_nrw_idr on page 1150
0x1080	por_hnf_mpam_msmon_idr	RO	5.3.11.12 por_hnf_mpam_msmon_idr on page 1151
0x1088	por_hnf_mpam_csumon_idr	RO	5.3.11.13 por_hnf_mpam_csumon_idr on page 1153
0x1090	por_hnf_mpam_mbwumon_idr	RO	5.3.11.14 por_hnf_mpam_mbwumon_idr on page 1154
0x10F0	por_hnf_ns_mpam_ecr	RW	5.3.11.15 por_hnf_ns_mpam_ecr on page 1155
0x10F8	por_hnf_ns_mpam_esr	RW	5.3.11.16 por_hnf_ns_mpam_esr on page 1156
0x1100	por_hnf_ns_mpamcfg_part_sel	RW	5.3.11.17 por_hnf_ns_mpamcfg_part_sel on page 1158
0x1108	por_hnf_ns_mpamcfg_cmax	RW	5.3.11.18 por_hnf_ns_mpamcfg_cmax on page 1159
0x1200	por_hnf_ns_mpamcfg_mbw_min	RW	5.3.11.19 por_hnf_ns_mpamcfg_mbw_min on page 1160
0x1208	por_hnf_ns_mpamcfg_mbw_max	RW	5.3.11.20 por_hnf_ns_mpamcfg_mbw_max on page 1161
0x1220	por_hnf_ns_mpamcfg_mbw_winwd	RW	5.3.11.21 por_hnf_ns_mpamcfg_mbw_winwd on page 1162
0x1400	por_hnf_ns_mpamcfg_pri	RW	5.3.11.22 por_hnf_ns_mpamcfg_pri on page 1163
0x1500	por_hnf_ns_mpamcfg_mbw_prop	RW	5.3.11.23 por_hnf_ns_mpamcfg_mbw_prop on page 1165
0x1600	por_hnf_ns_mpamcfg_intpartid	RW	5.3.11.24 por_hnf_ns_mpamcfg_intpartid on page 1166
0x1800	por_hnf_ns_msmon_cfg_mon_sel	RW	5.3.11.25 por_hnf_ns_msmon_cfg_mon_sel on page 1167
0x1808	por_hnf_ns_msmon_capt_evnt	RW	5.3.11.26 por_hnf_ns_msmon_capt_evnt on page 1168
0x1810	por_hnf_ns_msmon_cfg_csu_flt	RW	5.3.11.27 por_hnf_ns_msmon_cfg_csu_flt on page 1169
0x1818	por_hnf_ns_msmon_cfg_csu_ctl	RW	5.3.11.28 por_hnf_ns_msmon_cfg_csu_ctl on page 1170
0x1820	por_hnf_ns_msmon_cfg_mbwu_flt	RW	5.3.11.29 por_hnf_ns_msmon_cfg_mbwu_flt on page 1173
0x1828	por_hnf_ns_msmon_cfg_mbwu_ctl	RW	5.3.11.30 por_hnf_ns_msmon_cfg_mbwu_ctl on page 1174
0x1840	por_hnf_ns_msmon_csu	RW	5.3.11.31 por_hnf_ns_msmon_csu on page 1176

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Offset	Name	Type	Description
0x1848	por_hnf_ns_msmon_csu_capture	RW	5.3.11.32 por_hnf_ns_msmon_csu_capture on page 1177
0x1860	por_hnf_ns_msmon_mbwu	RW	5.3.11.33 por_hnf_ns_msmon_mbwu on page 1178
0x1868	por_hnf_ns_msmon_mbwu_capture	RW	5.3.11.34 por_hnf_ns_msmon_mbwu_capture on page 1179
0x2000	por_hnf_ns_mpamcfg_cpbm	RW	5.3.11.35 por_hnf_ns_mpamcfg_cpbm on page 1180

5.2.12 HN-F MPAM_S register summary

This section lists the HN-F MPAM_S registers used in CI-700.

HNF_MPAM_S register summary

The following table shows the *HNF_MPAM_S* registers in offset order from the base memory address

Table 5-13: HNF_MPAM_S register summary

Offset	Name	Type	Description
0x0	por_hnf_mpam_s_node_info	RO	5.3.12.1 por_hnf_mpam_s_node_info on page 1182
0x80	por_hnf_mpam_s_child_info	RO	5.3.12.2 por_hnf_mpam_s_child_info on page 1183
0x980	por_hnf_mpam_s_secure_register_groups_override	RW	5.3.12.3 por_hnf_mpam_s_secure_register_groups_override on page 1184
0x1008	por_hnf_mpam_sidr	RO	5.3.12.4 por_hnf_mpam_sidr on page 1185
0x10F0	por_hnf_s_mpam_ecr	RW	5.3.12.5 por_hnf_s_mpam_ecr on page 1186
0x10F8	por_hnf_s_mpam_esr	RW	5.3.12.6 por_hnf_s_mpam_esr on page 1187
0x1100	por_hnf_s_mpamcfg_part_sel	RW	5.3.12.7 por_hnf_s_mpamcfg_part_sel on page 1189
0x1108	por_hnf_s_mpamcfg_cmax	RW	5.3.12.8 por_hnf_s_mpamcfg_cmax on page 1190
0x1200	por_hnf_s_mpamcfg_mbw_min	RW	5.3.12.9 por_hnf_s_mpamcfg_mbw_min on page 1191
0x1208	por_hnf_s_mpamcfg_mbw_max	RW	5.3.12.10 por_hnf_s_mpamcfg_mbw_max on page 1192
0x1220	por_hnf_s_mpamcfg_mbw_winwd	RW	5.3.12.11 por_hnf_s_mpamcfg_mbw_winwd on page 1193
0x1400	por_hnf_s_mpamcfg_pri	RW	5.3.12.12 por_hnf_s_mpamcfg_pri on page 1194
0x1500	por_hnf_s_mpamcfg_mbw_prop	RW	5.3.12.13 por_hnf_s_mpamcfg_mbw_prop on page 1196
0x1600	por_hnf_s_mpamcfg_intpartid	RW	5.3.12.14 por_hnf_s_mpamcfg_intpartid on page 1197
0x1800	por_hnf_s_msmon_cfg_mon_sel	RW	5.3.12.15 por_hnf_s_msmon_cfg_mon_sel on page 1198
0x1808	por_hnf_s_msmon_capt_evnt	RW	5.3.12.16 por_hnf_s_msmon_capt_evnt on page 1199
0x1810	por_hnf_s_msmon_cfg_csu_flt	RW	5.3.12.17 por_hnf_s_msmon_cfg_csu_flt on page 1200
0x1818	por_hnf_s_msmon_cfg_csu_ctl	RW	5.3.12.18 por_hnf_s_msmon_cfg_csu_ctl on page 1202
0x1820	por_hnf_s_msmon_cfg_mbwu_flt	RW	5.3.12.19 por_hnf_s_msmon_cfg_mbwu_flt on page 1204
0x1828	por_hnf_s_msmon_cfg_mbwu_ctl	RW	5.3.12.20 por_hnf_s_msmon_cfg_mbwu_ctl on page 1205
0x1840	por_hnf_s_msmon_csu	RW	5.3.12.21 por_hnf_s_msmon_csu on page 1207
0x1848	por_hnf_s_msmon_csu_capture	RW	5.3.12.22 por_hnf_s_msmon_csu_capture on page 1208
0x1860	por_hnf_s_msmon_mbwu	RW	5.3.12.23 por_hnf_s_msmon_mbwu on page 1210
0x1868	por_hnf_s_msmon_mbwu_capture	RW	5.3.12.24 por_hnf_s_msmon_mbwu_capture on page 1211

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Offset	Name	Type	Description
0x2000	por_hnf_s_mpamcfg_cpbm	RW	5.3.12.25 por_hnf_s_mpamcfg_cpbm on page 1212

5.2.13 MTU register summary

This section lists the MTU registers used in CI-700.

MTU register summary

The following table shows the *MTU* registers in offset order from the base memory address

Table 5-14: MTU register summary

Offset	Name	Type	Description
0x0	por_mtu_node_info	RO	5.3.13.1 por_mtu_node_info on page 1213
0x80	por_mtu_child_info	RO	5.3.13.2 por_mtu_child_info on page 1214
0x980	por_mtu_secure_register_groups_override	RW	5.3.13.3 por_mtu_secure_register_groups_override on page 1215
0x900	por_mtu_unit_info	RO	5.3.13.4 por_mtu_unit_info on page 1217
0xA00	por_mtu_cfg_ctl	RW	5.3.13.5 por_mtu_cfg_ctl on page 1218
0xA08	por_mtu_aux_ctl	RW	5.3.13.6 por_mtu_aux_ctl on page 1220
0xA30	por_mtu_tc_flush_pr	RW	5.3.13.7 por_mtu_tc_flush_pr on page 1221
0xA38	por_mtu_tc_flush_sr	RO	5.3.13.8 por_mtu_tc_flush_sr on page 1222
0xA40	por_mtu_tag_addr_ctl	RW	5.3.13.9 por_mtu_tag_addr_ctl on page 1223
0xA48	por_mtu_tag_addr_base	RW	5.3.13.10 por_mtu_tag_addr_base on page 1224
0xA50	por_mtu_tag_addr_shutter0	RW	5.3.13.11 por_mtu_tag_addr_shutter0 on page 1225
0xA58	por_mtu_tag_addr_shutter1	RW	5.3.13.12 por_mtu_tag_addr_shutter1 on page 1235
0xA60	por_mtu_tag_addr_shutter2	RW	5.3.13.13 por_mtu_tag_addr_shutter2 on page 1244
0x3000	por_mtu_errfr	RO	5.3.13.14 por_mtu_errfr on page 1252
0x3008	por_mtu_errctlr	RW	5.3.13.15 por_mtu_errctlr on page 1254
0x3010	por_mtu_errstatus	W1C	5.3.13.16 por_mtu_errstatus on page 1255
0x3018	por_mtu_erraddr	RW	5.3.13.17 por_mtu_erraddr on page 1257
0x3020	por_mtu_errmisc	RW	5.3.13.18 por_mtu_errmisc on page 1259
0x3100	por_mtu_errfr_NS	RO	5.3.13.19 por_mtu_errfr_NS on page 1261
0x3108	por_mtu_errctlr_NS	RW	5.3.13.20 por_mtu_errctlr_NS on page 1263
0x3110	por_mtu_errstatus_NS	W1C	5.3.13.21 por_mtu_errstatus_NS on page 1264
0x3118	por_mtu_erraddr_NS	RW	5.3.13.22 por_mtu_erraddr_NS on page 1266
0x3120	por_mtu_errmisc_NS	RW	5.3.13.23 por_mtu_errmisc_NS on page 1267
0x3030	por_mtu_err_inj	RW	5.3.13.24 por_mtu_err_inj on page 1269
0xB80	por_mtu_cfg_tc_dbgrd	WO	5.3.13.25 por_mtu_cfg_tc_dbgrd on page 1270
0xB88	por_mtu_tc_cache_access_tc_ctl	RO	5.3.13.26 por_mtu_tc_cache_access_tc_ctl on page 1272
0xB98	por_mtu_tc_cache_access_tc_data	RO	5.3.13.27 por_mtu_tc_cache_access_tc_data on page 1273
0x2000	por_mtu_pmu_event_sel	RW	5.3.13.28 por_mtu_pmu_event_sel on page 1274

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5.3 Register descriptions

This section contains register descriptions.

5.3.1 Configuration master register descriptions

This section lists the configuration registers.

5.3.1.1 por_cfgm_node_info

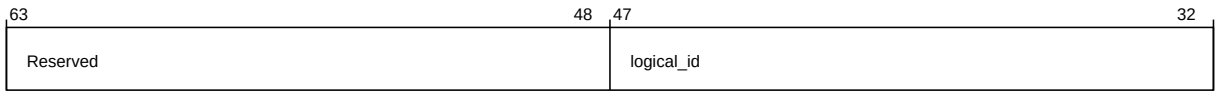
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1: por_cfgm_por_cfgm_node_info (high)



The following table shows the por_cfgm_node_info higher register bit assignments.

Table 5-15: por_cfgm_por_cfgm_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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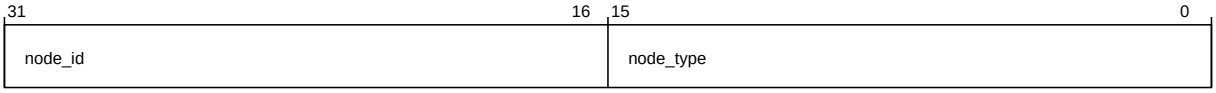
Figure 5-2: por_cfgm_por_cfgm_node_info (low)



The following table shows the por_cfgm_node_info lower register bit assignments.

Table 5-16: por_cfgm_por_cfgm_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0002

5.3.1.2 por_cfgm_periph_id_0_periph_id_1

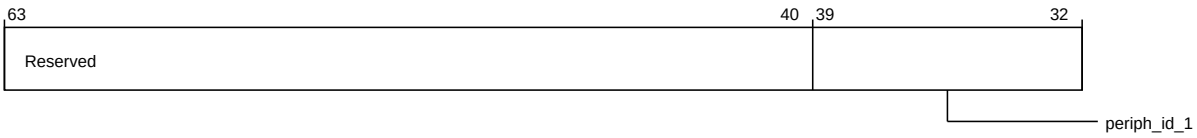
Functions as the peripheral ID 0 and peripheral ID 1 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-3: por_cfgm_por_cfgm_periph_id_0_periph_id_1 (high)



The following table shows the por_cfgm_periph_id_0_periph_id_1 higher register bit assignments.

Table 5-17: por_cfgm_por_cfgm_periph_id_0_periph_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_1	Peripheral ID 1	RO	8'b10110100

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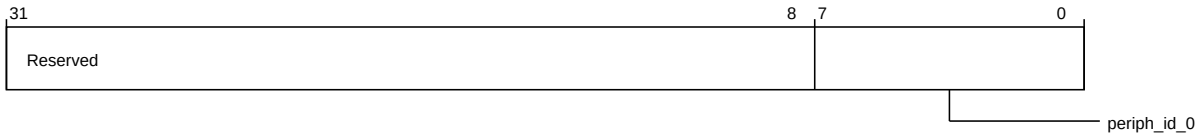
The following figure shows the lower register bit assignments.

Figure 5-4: por_cfgm_por_cfgm_periph_id_0_periph_id_1 (low)



The following table shows the por_cfgm_periph_id_0_periph_id_1 lower register bit assignments.

Table 5-18: por_cfgm_por_cfgm_periph_id_0_periph_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_0	Peripheral ID 0	RO	Configuration dependent

5.3.1.3 por_cfgm_periph_id_2_periph_id_3

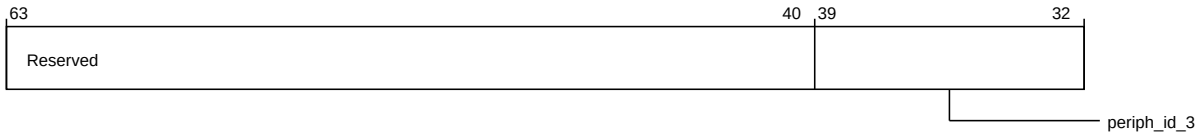
Functions as the peripheral ID 2 and peripheral ID 3 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h10
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-5: por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)



The following table shows the por_cfgm_periph_id_2_periph_id_3 higher register bit assignments.

Table 5-19: por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-

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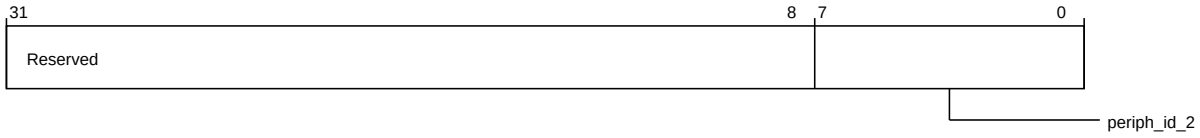
Bits	Field name	Description	Type	Reset
39:32	periph_id_3	Peripheral ID 3	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-6: por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)



The following table shows the por_cfgm_periph_id_2_periph_id_3 lower register bit assignments.

Table 5-20: por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_2	Peripheral ID 2 [7:4] indicates revision: 0x0 r0p0 0x1 r1p0 0x2 r2p0 [3] JEDEC JEP106 identity code, 1'b1 [2:0] JEP106 identity code [6:4], 0'b011	RO	Configuration dependent

5.3.1.4 por_cfgm_periph_id_4_periph_id_5

Functions as the peripheral ID 4 and peripheral ID 5 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h18
Register reset 64'b011000100
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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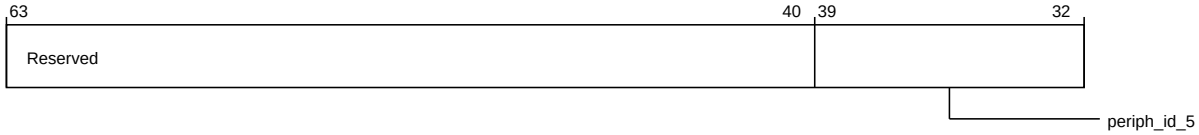
Figure 5-7: por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)



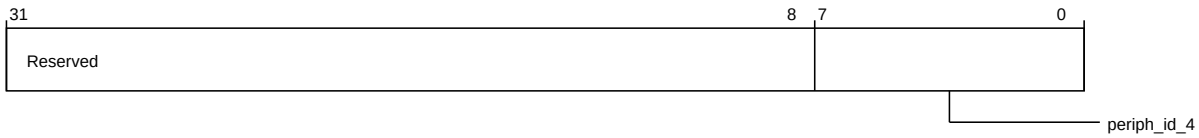
The following table shows the por_cfgm_periph_id_4_periph_id_5 higher register bit assignments.

Table 5-21: por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_5	Peripheral ID 5	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-8: por_cfgm_por_cfgm_periph_id_4_periph_id_5 (low)



The following table shows the por_cfgm_periph_id_4_periph_id_5 lower register bit assignments.

Table 5-22: por_cfgm_por_cfgm_periph_id_4_periph_id_5 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_4	Peripheral ID 4	RO	8'b11000100

5.3.1.5 por_cfgm_periph_id_6_periph_id_7

Functions as the peripheral ID 6 and peripheral ID 7 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h20
Register reset 64'b0
Usage constraints There are no usage constraints.

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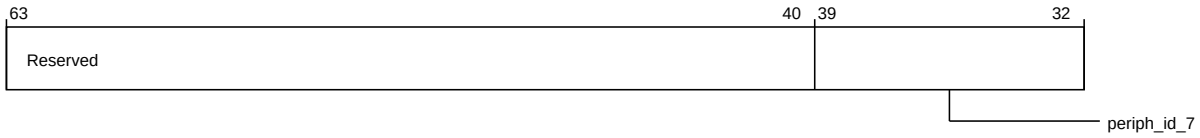
The following figure shows the higher register bit assignments.

Figure 5-9: por_cfgm_por_cfgm_periph_id_6_periph_id_7 (high)



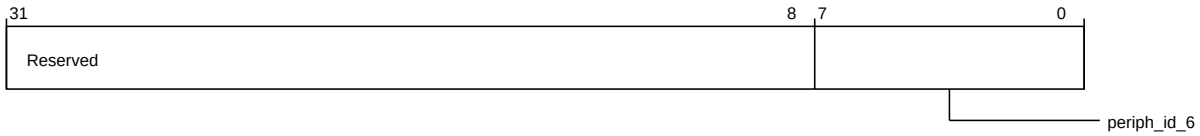
The following table shows the por_cfgm_periph_id_6_periph_id_7 higher register bit assignments.

Table 5-23: por_cfgm_por_cfgm_periph_id_6_periph_id_7 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_7	Peripheral ID 7	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-10: por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)



The following table shows the por_cfgm_periph_id_6_periph_id_7 lower register bit assignments.

Table 5-24: por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_6	Peripheral ID 6	RO	8'b0

5.3.1.6 por_cfgm_component_id_0_component_id_1

Functions as the component ID 0 and component ID 1 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h28
Register reset 64'b1111000000001101

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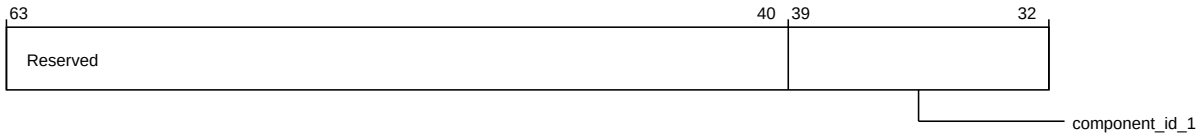
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-11: por_cfgm_por_cfgm_component_id_0_component_id_1 (high)



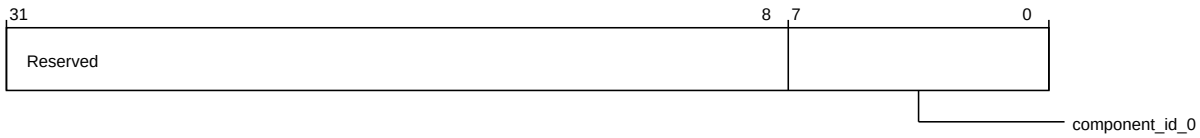
The following table shows the por_cfgm_component_id_0_component_id_1 higher register bit assignments.

Table 5-25: por_cfgm_por_cfgm_component_id_0_component_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_1	Component ID 1	RO	8'b11110000

The following figure shows the lower register bit assignments.

Figure 5-12: por_cfgm_por_cfgm_component_id_0_component_id_1 (low)



The following table shows the por_cfgm_component_id_0_component_id_1 lower register bit assignments.

Table 5-26: por_cfgm_por_cfgm_component_id_0_component_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_0	Component ID 0	RO	8'b00001101

5.3.1.7 por_cfgm_component_id_2_component_id_3

Functions as the component ID 2 and component ID 3 register.

Its characteristics are:

Type RO

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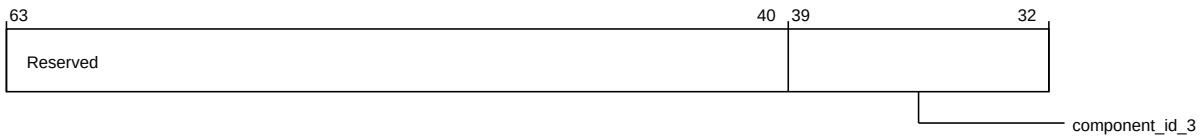
Register width (Bits) 64
Address offset 16'h30
Register reset 64'b1011000100000101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-13: por_cfgm_por_cfgm_component_id_2_component_id_3 (high)



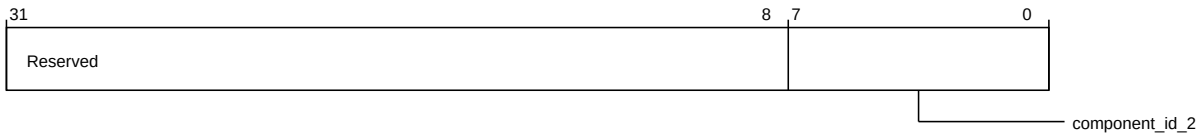
The following table shows the por_cfgm_component_id_2_component_id_3 higher register bit assignments.

Table 5-27: por_cfgm_por_cfgm_component_id_2_component_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_3	Component ID 3	RO	8'b10110001

The following figure shows the lower register bit assignments.

Figure 5-14: por_cfgm_por_cfgm_component_id_2_component_id_3 (low)



The following table shows the por_cfgm_component_id_2_component_id_3 lower register bit assignments.

Table 5-28: por_cfgm_por_cfgm_component_id_2_component_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_2	Component ID 2	RO	8'b00000101

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5.3.1.8 por_cfgm_child_info

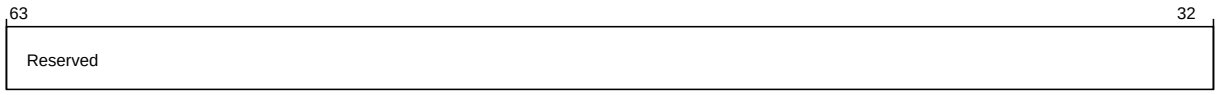
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-15: por_cfgm_por_cfgm_child_info (high)



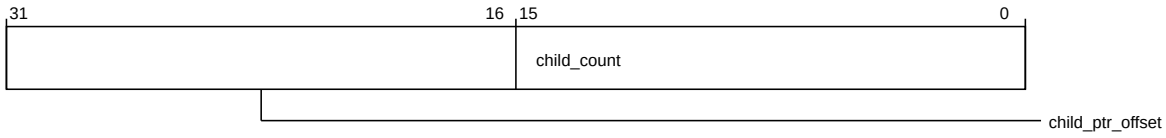
The following table shows the por_cfgm_child_info higher register bit assignments.

Table 5-29: por_cfgm_por_cfgm_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-16: por_cfgm_por_cfgm_child_info (low)



The following table shows the por_cfgm_child_info lower register bit assignments.

Table 5-30: por_cfgm_por_cfgm_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

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5.3.1.9 por_cfgm_secure_access

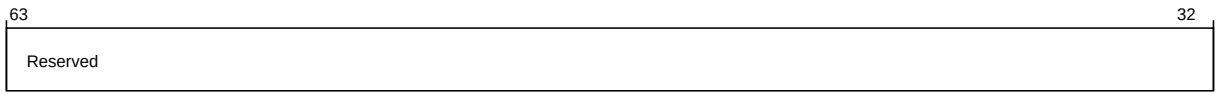
Functions as the Secure access control register. This register must be set up at boot time. Before initiating a write to this register, software must ensure that no other configuration accesses are in flight. Once this write is initiated, no other configuration accesses are initiated until complete.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-17: por_cfgm_por_cfgm_secure_access (high)



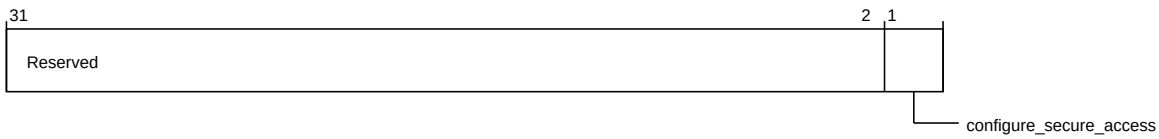
The following table shows the por_cfgm_secure_access higher register bit assignments.

Table 5-31: por_cfgm_por_cfgm_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-18: por_cfgm_por_cfgm_secure_access (low)



The following table shows the por_cfgm_secure_access lower register bit assignments.

Table 5-32: por_cfgm_por_cfgm_secure_access (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
1:0	configure_secure_access	Secure access mode 2'b00: Default operation 2'b01: Allows Non-secure access to Secure registers 2'b10: Allows Secure access only to any configuration register regardless of its security status 2'b11: Undefined behavior	RW	2'b0

5.3.1.10 por_cfgm_errgsr0

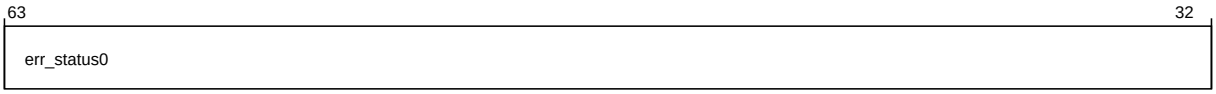
Provides the XP <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3000
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-19: por_cfgm_por_cfgm_errgsr0 (high)



The following table shows the por_cfgm_errgsr0 higher register bit assignments.

Table 5-33: por_cfgm_por_cfgm_errgsr0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status0	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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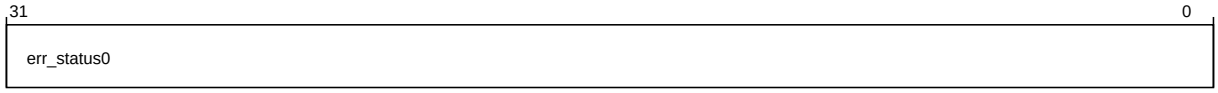
Figure 5-20: por_cfgm_por_cfgm_errgsr0 (low)



The following table shows the por_cfgm_errgsr0 lower register bit assignments.

Table 5-34: por_cfgm_por_cfgm_errgsr0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0	Read-only copy of por_mxp_err<n>status	RO	64'h0

5.3.1.11 por_cfgm_errgsr1

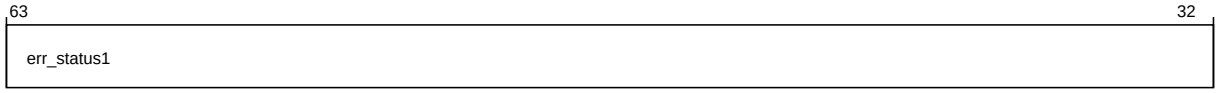
Provides the HN-I <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-21: por_cfgm_por_cfgm_errgsr1 (high)



The following table shows the por_cfgm_errgsr1 higher register bit assignments.

Table 5-35: por_cfgm_por_cfgm_errgsr1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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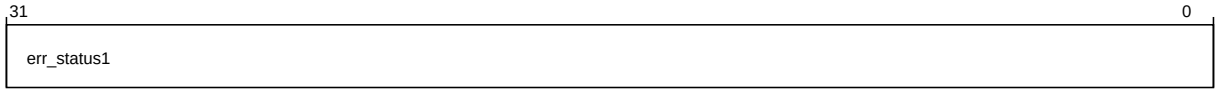
Figure 5-22: por_cfgm_por_cfgm_errgsr1 (low)



The following table shows the por_cfgm_errgsr1 lower register bit assignments.

Table 5-36: por_cfgm_por_cfgm_errgsr1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

5.3.1.12 por_cfgm_errgsr2

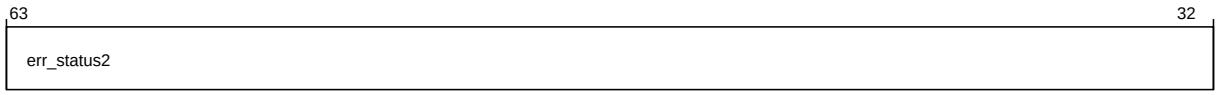
Provides the HN-F <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-23: por_cfgm_por_cfgm_errgsr2 (high)



The following table shows the por_cfgm_errgsr2 higher register bit assignments.

Table 5-37: por_cfgm_por_cfgm_errgsr2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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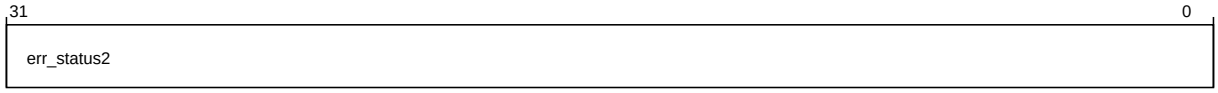
Figure 5-24: por_cfgm_por_cfgm_errgsr2 (low)



The following table shows the por_cfgm_errgsr2 lower register bit assignments.

Table 5-38: por_cfgm_por_cfgm_errgsr2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

5.3.1.13 por_cfgm_errgsr3

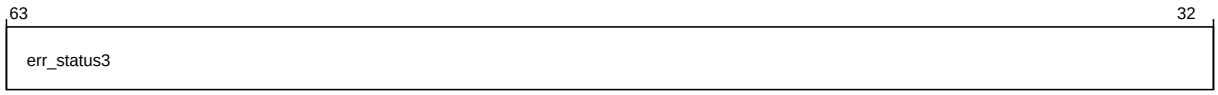
Provides the SBSX <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-25: por_cfgm_por_cfgm_errgsr3 (high)



The following table shows the por_cfgm_errgsr3 higher register bit assignments.

Table 5-39: por_cfgm_por_cfgm_errgsr3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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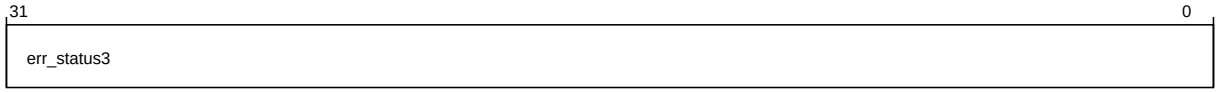
Figure 5-26: por_cfgm_por_cfgm_errgsr3 (low)



The following table shows the por_cfgm_errgsr3 lower register bit assignments.

Table 5-40: por_cfgm_por_cfgm_errgsr3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

5.3.1.14 por_cfgm_errgsr4

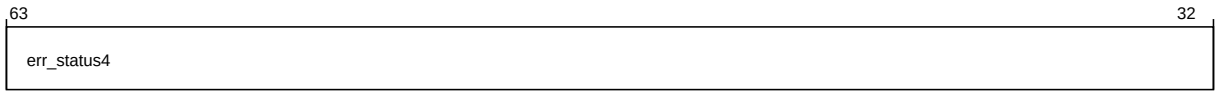
Provides the CXG <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-27: por_cfgm_por_cfgm_errgsr4 (high)



The following table shows the por_cfgm_errgsr4 higher register bit assignments.

Table 5-41: por_cfgm_por_cfgm_errgsr4 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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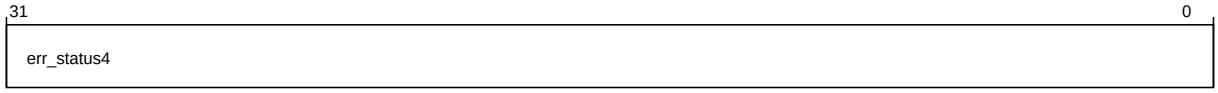
Figure 5-28: por_cfgm_por_cfgm_errgsr4 (low)



The following table shows the por_cfgm_errgsr4 lower register bit assignments.

Table 5-42: por_cfgm_por_cfgm_errgsr4 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

5.3.1.15 por_cfgm_errgsr5

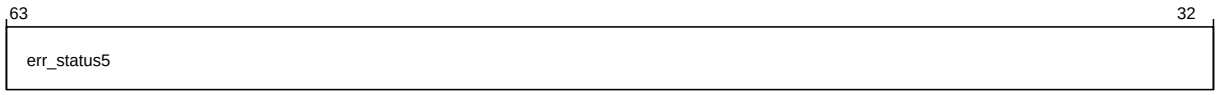
Provides the MTSX <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3028
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-29: por_cfgm_por_cfgm_errgsr5 (high)



The following table shows the por_cfgm_errgsr5 higher register bit assignments.

Table 5-43: por_cfgm_por_cfgm_errgsr5 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5	Read-only copy of por_mtsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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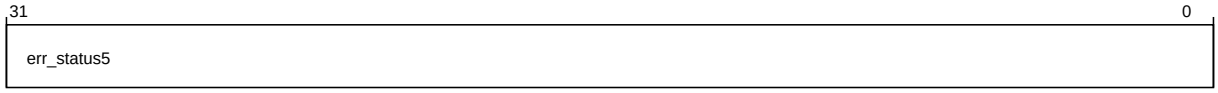
Figure 5-30: por_cfgm_por_cfgm_errgsr5 (low)



The following table shows the por_cfgm_errgsr5 lower register bit assignments.

Table 5-44: por_cfgm_por_cfgm_errgsr5 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5	Read-only copy of por_mtsx_err<n>status	RO	64'h0

5.3.1.16 por_cfgm_errgsr6

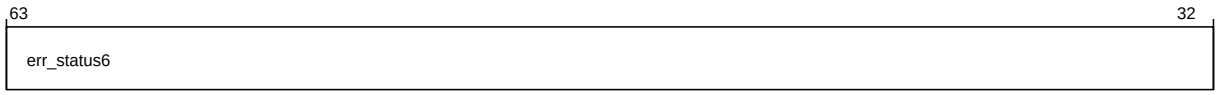
Provides the XP <n> Secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3080
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-31: por_cfgm_por_cfgm_errgsr6 (high)



The following table shows the por_cfgm_errgsr6 higher register bit assignments.

Table 5-45: por_cfgm_por_cfgm_errgsr6 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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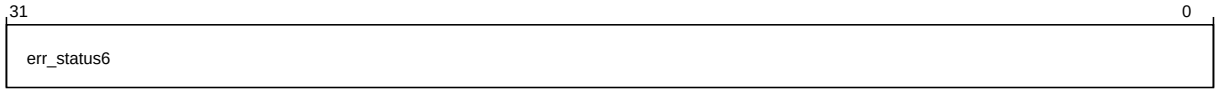
Figure 5-32: por_cfgm_por_cfgm_errgsr6 (low)



The following table shows the por_cfgm_errgsr6 lower register bit assignments.

Table 5-46: por_cfgm_por_cfgm_errgsr6 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6	Read-only copy of por_mxp_err<n>status	RO	64'h0

5.3.1.17 por_cfgm_errgsr7

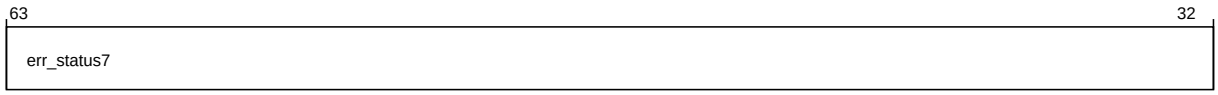
Provides the HN-I <n> Secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3088
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-33: por_cfgm_por_cfgm_errgsr7 (high)



The following table shows the por_cfgm_errgsr7 higher register bit assignments.

Table 5-47: por_cfgm_por_cfgm_errgsr7 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status7	Read-only copy of por_hni_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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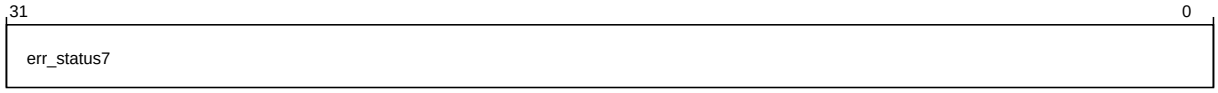
Figure 5-34: por_cfgm_por_cfgm_errgsr7 (low)



The following table shows the por_cfgm_errgsr7 lower register bit assignments.

Table 5-48: por_cfgm_por_cfgm_errgsr7 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status7	Read-only copy of por_hni_err<n>status	RO	64'h0

5.3.1.18 por_cfgm_errgsr8

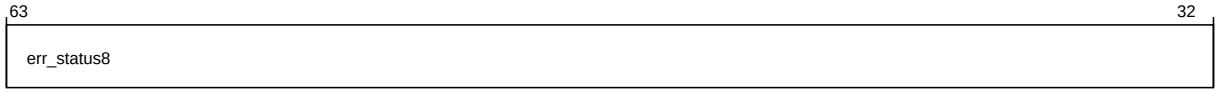
Provides the HN-F <n> Secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3090
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-35: por_cfgm_por_cfgm_errgsr8 (high)



The following table shows the por_cfgm_errgsr8 higher register bit assignments.

Table 5-49: por_cfgm_por_cfgm_errgsr8 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status8	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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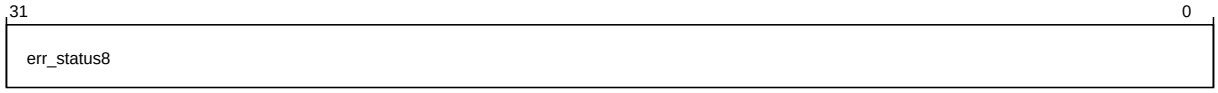
Figure 5-36: por_cfgm_por_cfgm_errgsr8 (low)



The following table shows the por_cfgm_errgsr8 lower register bit assignments.

Table 5-50: por_cfgm_por_cfgm_errgsr8 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8	Read-only copy of por_hnf_err<n>status	RO	64'h0

5.3.1.19 por_cfgm_errgsr9

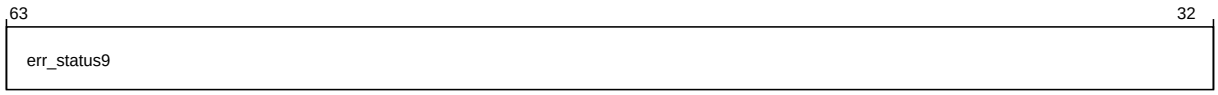
Provides the SBSX <n> Secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3098
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-37: por_cfgm_por_cfgm_errgsr9 (high)



The following table shows the por_cfgm_errgsr9 higher register bit assignments.

Table 5-51: por_cfgm_por_cfgm_errgsr9 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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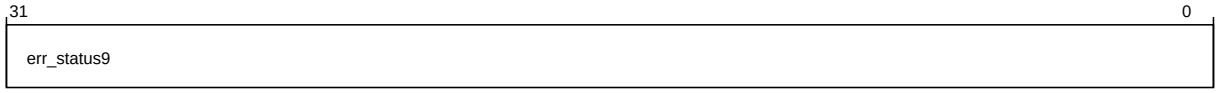
Figure 5-38: por_cfgm_por_cfgm_errgsr9 (low)



The following table shows the por_cfgm_errgsr9 lower register bit assignments.

Table 5-52: por_cfgm_por_cfgm_errgsr9 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9	Read-only copy of por_sbsx_err<n>status	RO	64'h0

5.3.1.20 por_cfgm_errgsr10

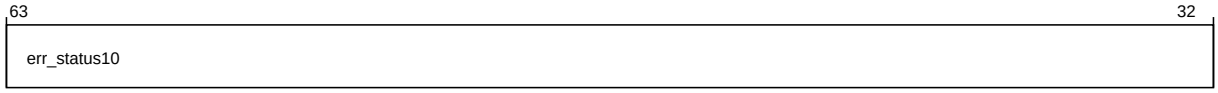
Provides the CXG <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h30A0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-39: por_cfgm_por_cfgm_errgsr10 (high)



The following table shows the por_cfgm_errgsr10 higher register bit assignments.

Table 5-53: por_cfgm_por_cfgm_errgsr10 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status10	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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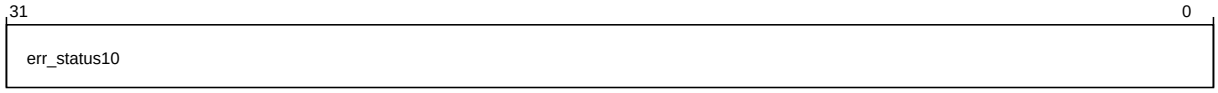
Figure 5-40: por_cfgm_por_cfgm_errgsr10 (low)



The following table shows the por_cfgm_errgsr10 lower register bit assignments.

Table 5-54: por_cfgm_por_cfgm_errgsr10 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status10	Read-only copy of por_cxg_err<n>status	RO	64'h0

5.3.1.21 por_cfgm_errgsr11

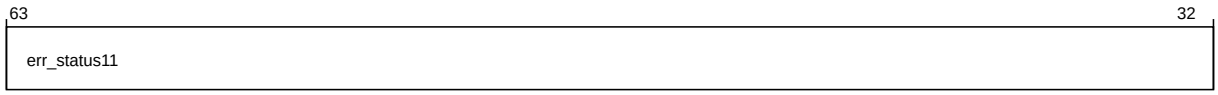
Provides the MTSX <n> Secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h30A8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-41: por_cfgm_por_cfgm_errgsr11 (high)



The following table shows the por_cfgm_errgsr11 higher register bit assignments.

Table 5-55: por_cfgm_por_cfgm_errgsr11 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status11	Read-only copy of por_mtsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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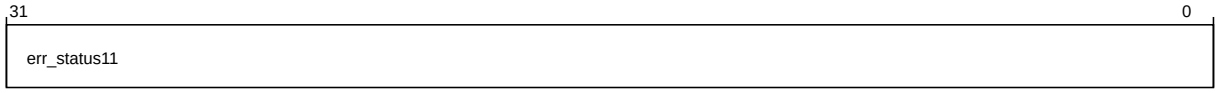
Figure 5-42: por_cfgm_por_cfgm_errgsr11 (low)



The following table shows the por_cfgm_errgsr11 lower register bit assignments.

Table 5-56: por_cfgm_por_cfgm_errgsr11 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status11	Read-only copy of por_mtsx_err<n>status	RO	64'h0

5.3.1.22 por_cfgm_errgsr0_NS

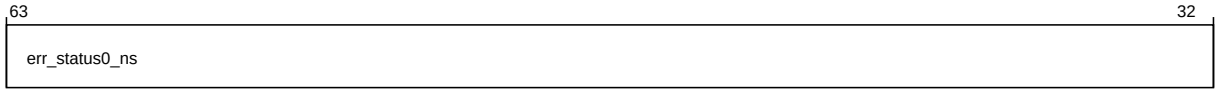
Provides the XP <n> Non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-43: por_cfgm_por_cfgm_errgsr0_ns (high)



The following table shows the por_cfgm_errgsr0_NS higher register bit assignments.

Table 5-57: por_cfgm_por_cfgm_errgsr0_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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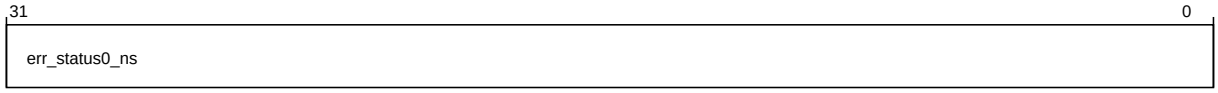
Figure 5-44: por_cfgm_por_cfgm_errgsr0_ns (low)



The following table shows the por_cfgm_errgsr0_NS lower register bit assignments.

Table 5-58: por_cfgm_por_cfgm_errgsr0_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

5.3.1.23 por_cfgm_errgsr1_NS

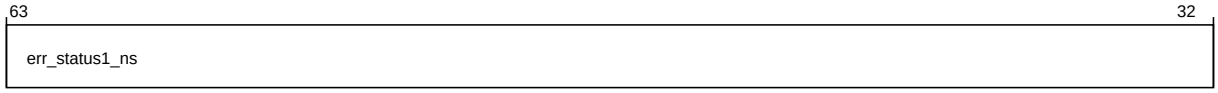
Provides the HN-I <n> Non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-45: por_cfgm_por_cfgm_errgsr1_ns (high)



The following table shows the por_cfgm_errgsr1_NS higher register bit assignments.

Table 5-59: por_cfgm_por_cfgm_errgsr1_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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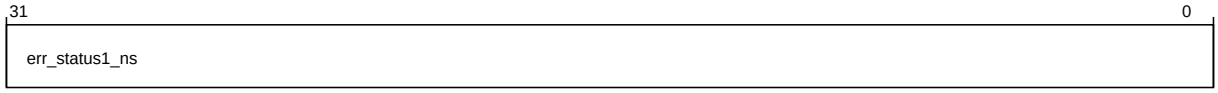
Figure 5-46: por_cfgm_por_cfgm_errgsr1_ns (low)



The following table shows the por_cfgm_errgsr1_NS lower register bit assignments.

Table 5-60: por_cfgm_por_cfgm_errgsr1_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

5.3.1.24 por_cfgm_errgsr2_NS

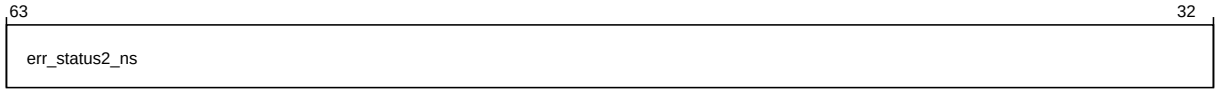
Provides the HN-F <n> Non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-47: por_cfgm_por_cfgm_errgsr2_ns (high)



The following table shows the por_cfgm_errgsr2_NS higher register bit assignments.

Table 5-61: por_cfgm_por_cfgm_errgsr2_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

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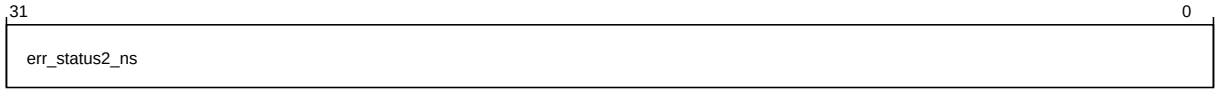
Figure 5-48: por_cfgm_por_cfgm_errgsr2_ns (low)



The following table shows the por_cfgm_errgsr2_NS lower register bit assignments.

Table 5-62: por_cfgm_por_cfgm_errgsr2_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

5.3.1.25 por_cfgm_errgsr3_NS

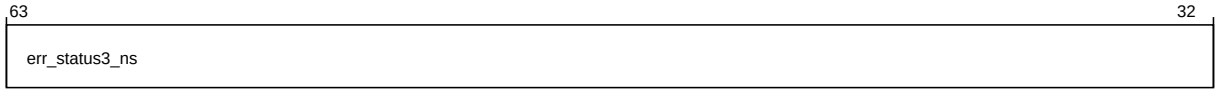
Provides the SBSX <n> Non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-49: por_cfgm_por_cfgm_errgsr3_ns (high)



The following table shows the por_cfgm_errgsr3_NS higher register bit assignments.

Table 5-63: por_cfgm_por_cfgm_errgsr3_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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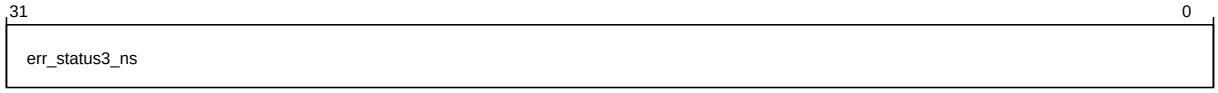
Figure 5-50: por_cfgm_por_cfgm_errgsr3_ns (low)



The following table shows the por_cfgm_errgsr3_NS lower register bit assignments.

Table 5-64: por_cfgm_por_cfgm_errgsr3_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

5.3.1.26 por_cfgm_errgsr4_NS

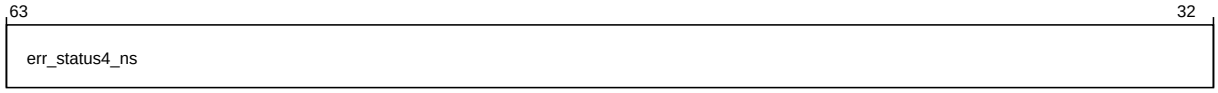
Provides the CXG <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3120
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-51: por_cfgm_por_cfgm_errgsr4_ns (high)



The following table shows the por_cfgm_errgsr4_NS higher register bit assignments.

Table 5-65: por_cfgm_por_cfgm_errgsr4_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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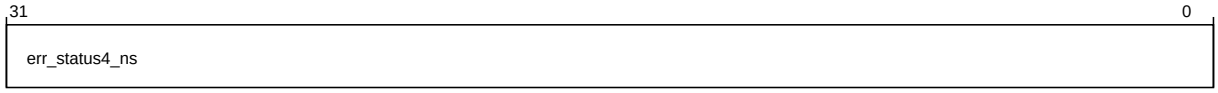
Figure 5-52: por_cfgm_por_cfgm_errgsr4_ns (low)



The following table shows the por_cfgm_errgsr4_NS lower register bit assignments.

Table 5-66: por_cfgm_por_cfgm_errgsr4_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

5.3.1.27 por_cfgm_errgsr5_NS

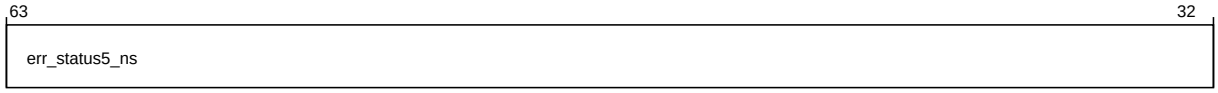
Provides the MTSX <n> Non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-53: por_cfgm_por_cfgm_errgsr5_ns (high)



The following table shows the por_cfgm_errgsr5_NS higher register bit assignments.

Table 5-67: por_cfgm_por_cfgm_errgsr5_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5_ns	Read-only copy of por_mtsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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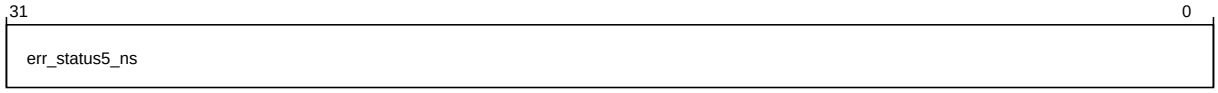
Figure 5-54: por_cfgm_por_cfgm_errgsr5_ns (low)



The following table shows the por_cfgm_errgsr5_NS lower register bit assignments.

Table 5-68: por_cfgm_por_cfgm_errgsr5_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5_ns	Read-only copy of por_mtsx_err<n>status	RO	64'h0

5.3.1.28 por_cfgm_errgsr6_NS

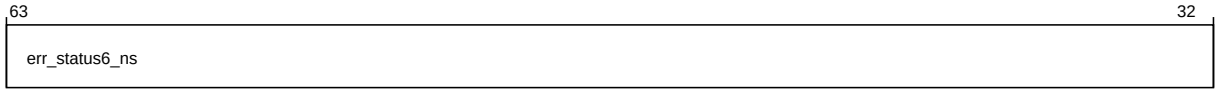
Provides the XP <n> Non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3180
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-55: por_cfgm_por_cfgm_errgsr6_ns (high)



The following table shows the por_cfgm_errgsr6_NS higher register bit assignments.

Table 5-69: por_cfgm_por_cfgm_errgsr6_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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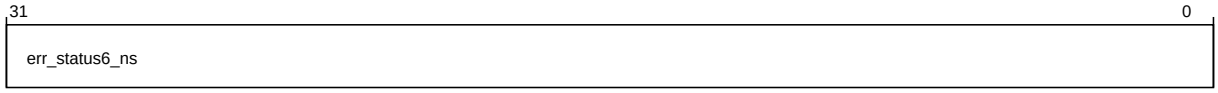
Figure 5-56: por_cfgm_por_cfgm_errgsr6_ns (low)



The following table shows the por_cfgm_errgsr6_NS lower register bit assignments.

Table 5-70: por_cfgm_por_cfgm_errgsr6_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

5.3.1.29 por_cfgm_errgsr7_NS

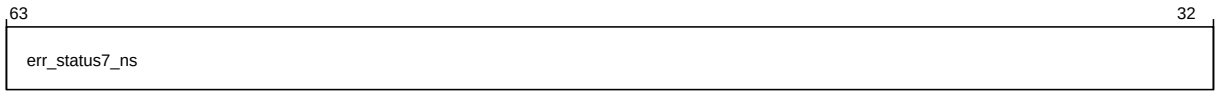
Provides the HN-I <n> Non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3188
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-57: por_cfgm_por_cfgm_errgsr7_ns (high)



The following table shows the por_cfgm_errgsr7_NS higher register bit assignments.

Table 5-71: por_cfgm_por_cfgm_errgsr7_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status7_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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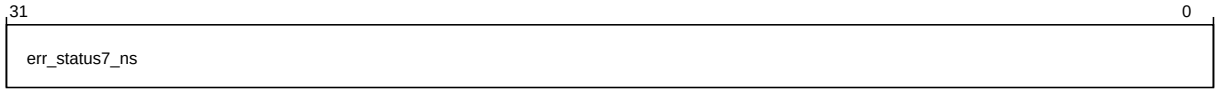
Figure 5-58: por_cfgm_por_cfgm_errgsr7_ns (low)



The following table shows the por_cfgm_errgsr7_NS lower register bit assignments.

Table 5-72: por_cfgm_por_cfgm_errgsr7_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status7_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

5.3.1.30 por_cfgm_errgsr8_NS

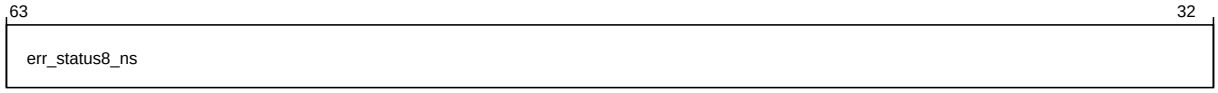
Provides the HN-F <n> Non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3190
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-59: por_cfgm_por_cfgm_errgsr8_ns (high)



The following table shows the por_cfgm_errgsr8_NS higher register bit assignments.

Table 5-73: por_cfgm_por_cfgm_errgsr8_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status8_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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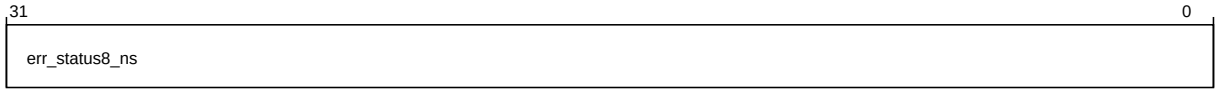
Figure 5-60: por_cfgm_por_cfgm_errgsr8_ns (low)



The following table shows the por_cfgm_errgsr8_NS lower register bit assignments.

Table 5-74: por_cfgm_por_cfgm_errgsr8_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

5.3.1.31 por_cfgm_errgsr9_NS

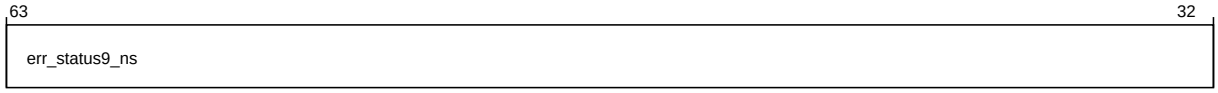
Provides the SBSX <n> Non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3198
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-61: por_cfgm_por_cfgm_errgsr9_ns (high)



The following table shows the por_cfgm_errgsr9_NS higher register bit assignments.

Table 5-75: por_cfgm_por_cfgm_errgsr9_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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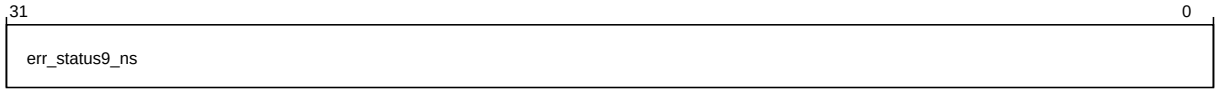
Figure 5-62: por_cfgm_por_cfgm_errgsr9_ns (low)



The following table shows the por_cfgm_errgsr9_NS lower register bit assignments.

Table 5-76: por_cfgm_por_cfgm_errgsr9_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

5.3.1.32 por_cfgm_errgsr10_NS

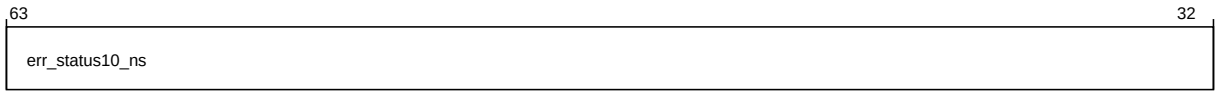
Provides the CXG <n> Secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h31A0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-63: por_cfgm_por_cfgm_errgsr10_ns (high)



The following table shows the por_cfgm_errgsr10_NS higher register bit assignments.

Table 5-77: por_cfgm_por_cfgm_errgsr10_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status10_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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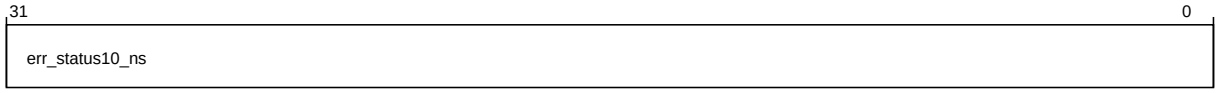
Figure 5-64: por_cfgm_por_cfgm_errgsr10_ns (low)



The following table shows the por_cfgm_errgsr10_NS lower register bit assignments.

Table 5-78: por_cfgm_por_cfgm_errgsr10_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status10_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

5.3.1.33 por_cfgm_errgsr11_NS

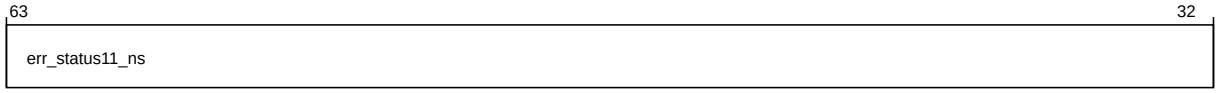
Provides the MTSX <n> Non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h31A8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-65: por_cfgm_por_cfgm_errgsr11_ns (high)



The following table shows the por_cfgm_errgsr11_NS higher register bit assignments.

Table 5-79: por_cfgm_por_cfgm_errgsr11_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status11_ns	Read-only copy of por_mtsx_err<n>status	RO	64'h0

The following figure shows the lower register bit assignments.

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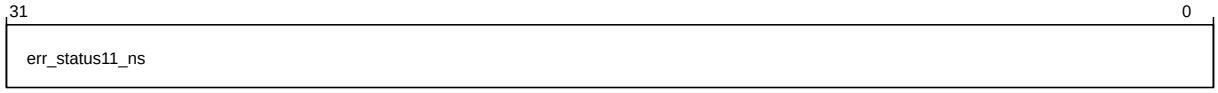
Figure 5-66: por_cfgm_por_cfgm_errgsr11_ns (low)



The following table shows the por_cfgm_errgsr11_NS lower register bit assignments.

Table 5-80: por_cfgm_por_cfgm_errgsr11_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status11_ns	Read-only copy of por_mtsx_err<n>status	RO	64'h0

5.3.1.34 por_cfgm_errdevaff

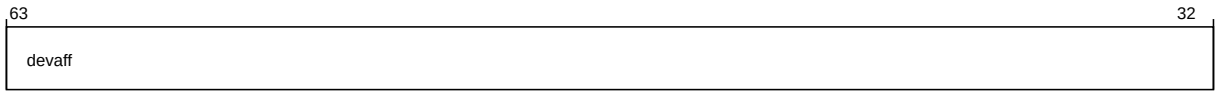
Functions as the device affinity register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FA8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-67: por_cfgm_por_cfgm_errdevaff (high)



The following table shows the por_cfgm_errdevaff higher register bit assignments.

Table 5-81: por_cfgm_por_cfgm_errdevaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following figure shows the lower register bit assignments.

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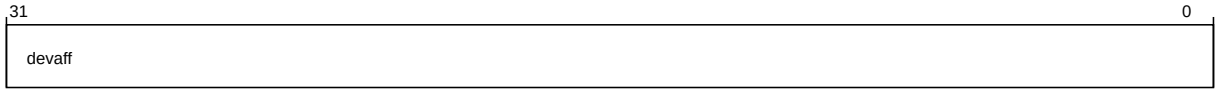
Figure 5-68: por_cfgm_por_cfgm_errdevaff (low)



The following table shows the por_cfgm_errdevaff lower register bit assignments.

Table 5-82: por_cfgm_por_cfgm_errdevaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

5.3.1.35 por_cfgm_errdevarch

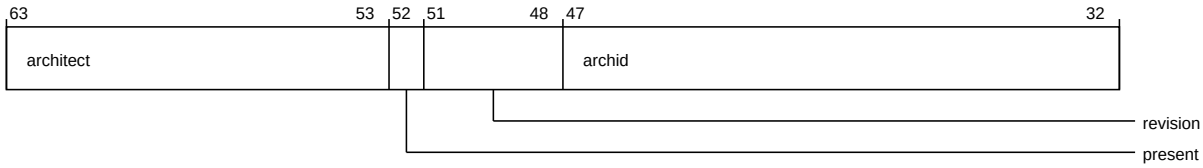
Functions as the device architecture register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FB8
Register reset 64'b00010111011100000000000101000
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-69: por_cfgm_por_cfgm_errdevarch (high)



The following table shows the por_cfgm_errdevarch higher register bit assignments.

Table 5-83: por_cfgm_por_cfgm_errdevarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'h23B
52	present	Present	RO	1'b1

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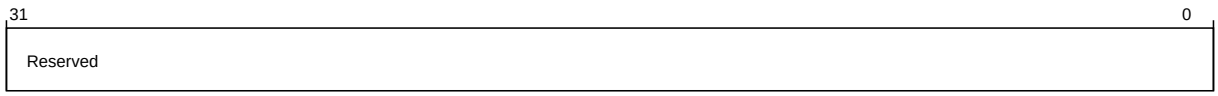
Bits	Field name	Description	Type	Reset
51:48	revision	Architecture revision	RO	4'b0
47:32	archid	Architecture ID	RO	16'h0A00

The following figure shows the lower register bit assignments.

Figure 5-70: por_cfgm_por_cfgm_errdevarch (low)



The following table shows the por_cfgm_errdevarch lower register bit assignments.

Table 5-84: por_cfgm_por_cfgm_errdevarch (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

5.3.1.36 por_cfgm_erridr

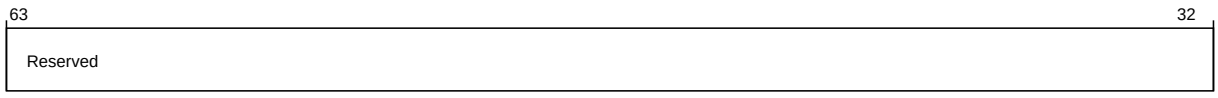
Contains the number of error records.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FC8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-71: por_cfgm_por_cfgm_erridr (high)



The following table shows the por_cfgm_erridr higher register bit assignments.

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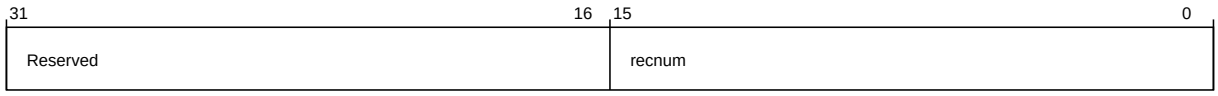
Table 5-85: por_cfgm_por_cfgm_erridr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-72: por_cfgm_por_cfgm_erridr (low)



The following table shows the por_cfgm_erridr lower register bit assignments.

Table 5-86: por_cfgm_por_cfgm_erridr (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	recnum	Number of error records; equal to 2*(number of logical devices)	RO	Configuration dependent

5.3.1.37 por_cfgm_errpidr45

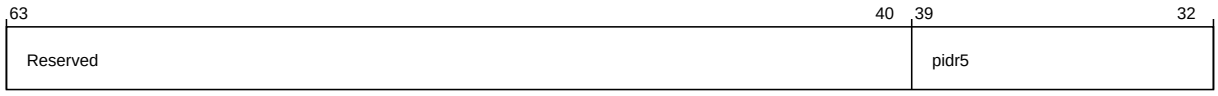
Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FD0
Register reset 64'b000000100
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-73: por_cfgm_por_cfgm_errpidr45 (high)



The following table shows the por_cfgm_errpidr45 higher register bit assignments.

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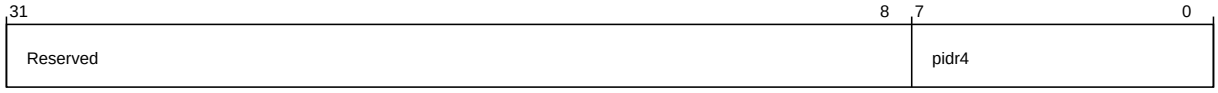
Table 5-87: por_cfgm_por_cfgm_errpidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-74: por_cfgm_por_cfgm_errpidr45 (low)



The following table shows the por_cfgm_errpidr45 lower register bit assignments.

Table 5-88: por_cfgm_por_cfgm_errpidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

5.3.1.38 por_cfgm_errpidr67

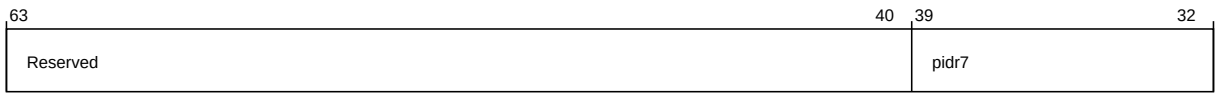
Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FD8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-75: por_cfgm_por_cfgm_errpidr67 (high)



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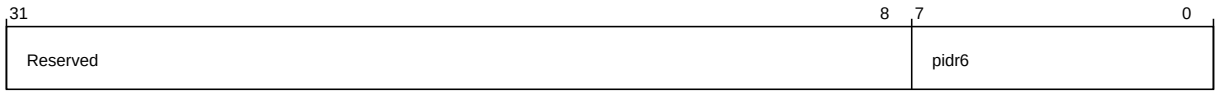
The following table shows the por_cfgm_errpidr67 higher register bit assignments.

Table 5-89: por_cfgm_por_cfgm_errpidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-76: por_cfgm_por_cfgm_errpidr67 (low)



The following table shows the por_cfgm_errpidr67 lower register bit assignments.

Table 5-90: por_cfgm_por_cfgm_errpidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

5.3.1.39 por_cfgm_errpidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FE0
Register reset 64'b0101110000011100
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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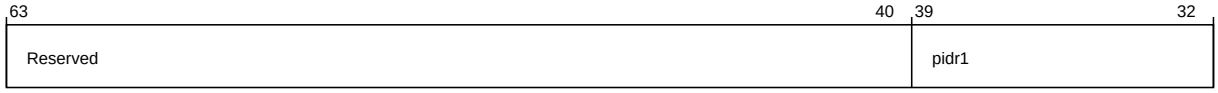
Figure 5-77: por_cfgm_por_cfgm_errpidr01 (high)



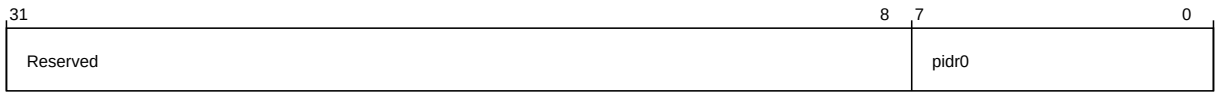
The following table shows the por_cfgm_errpidr01 higher register bit assignments.

Table 5-91: por_cfgm_por_cfgm_errpidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

The following figure shows the lower register bit assignments.

Figure 5-78: por_cfgm_por_cfgm_errpidr01 (low)



The following table shows the por_cfgm_errpidr01 lower register bit assignments.

Table 5-92: por_cfgm_por_cfgm_errpidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

5.3.1.40 por_cfgm_errpidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FE8
Register reset 64'b000000111
Usage constraints There are no usage constraints.

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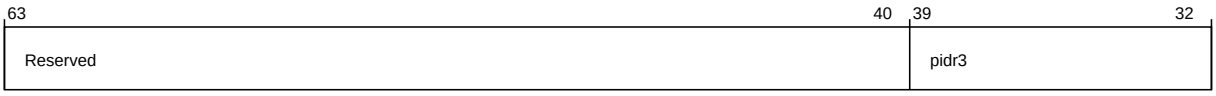
The following figure shows the higher register bit assignments.

Figure 5-79: por_cfgm_por_cfgm_errpidr23 (high)



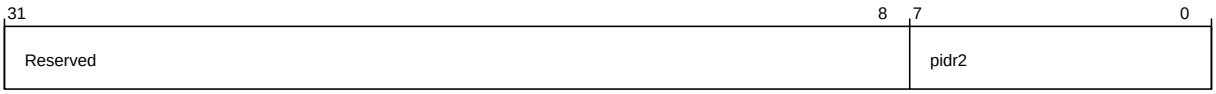
The following table shows the por_cfgm_errpidr23 higher register bit assignments.

Table 5-93: por_cfgm_por_cfgm_errpidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-80: por_cfgm_por_cfgm_errpidr23 (low)



The following table shows the por_cfgm_errpidr23 lower register bit assignments.

Table 5-94: por_cfgm_por_cfgm_errpidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

5.3.1.41 por_cfgm_errcidr01

Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3FF0
Register reset 64'b1111111100001101

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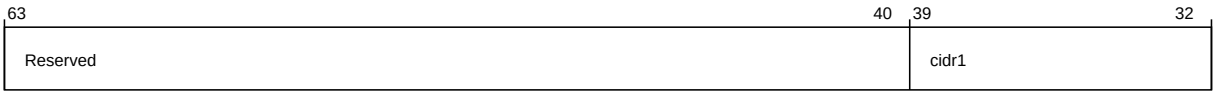
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-81: por_cfgm_por_cfgm_errcidr01 (high)



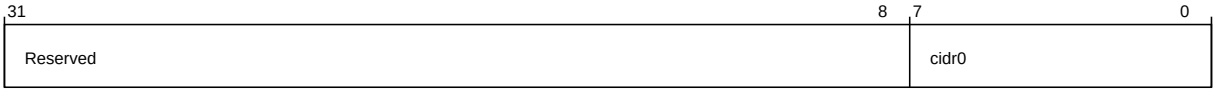
The following table shows the por_cfgm_errcidr01 higher register bit assignments.

Table 5-95: por_cfgm_por_cfgm_errcidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr1	Component ID 1	RO	8'hff

The following figure shows the lower register bit assignments.

Figure 5-82: por_cfgm_por_cfgm_errcidr01 (low)



The following table shows the por_cfgm_errcidr01 lower register bit assignments.

Table 5-96: por_cfgm_por_cfgm_errcidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr0	Component ID 0	RO	8'hd

5.3.1.42 por_cfgm_errcidr23

Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64

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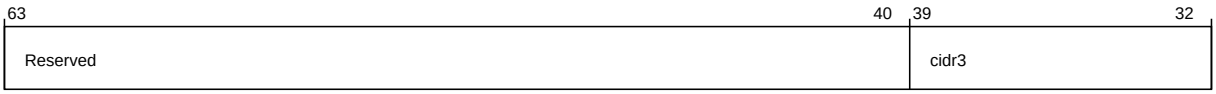
Address offset 16'h3FF8
Register reset 64'b0001011100000101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-83: por_cfgm_por_cfgm_errcidr23 (high)



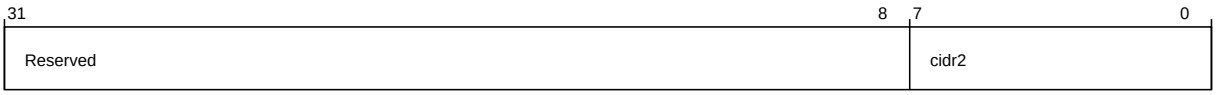
The following table shows the por_cfgm_errcidr23 higher register bit assignments.

Table 5-97: por_cfgm_por_cfgm_errcidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr3	Component ID 3	RO	8'hb1

The following figure shows the lower register bit assignments.

Figure 5-84: por_cfgm_por_cfgm_errcidr23 (low)



The following table shows the por_cfgm_errcidr23 lower register bit assignments.

Table 5-98: por_cfgm_por_cfgm_errcidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

5.3.1.43 por_info_global

Contains user-specified values of build-time global configuration parameters.

Its characteristics are:

Type RO

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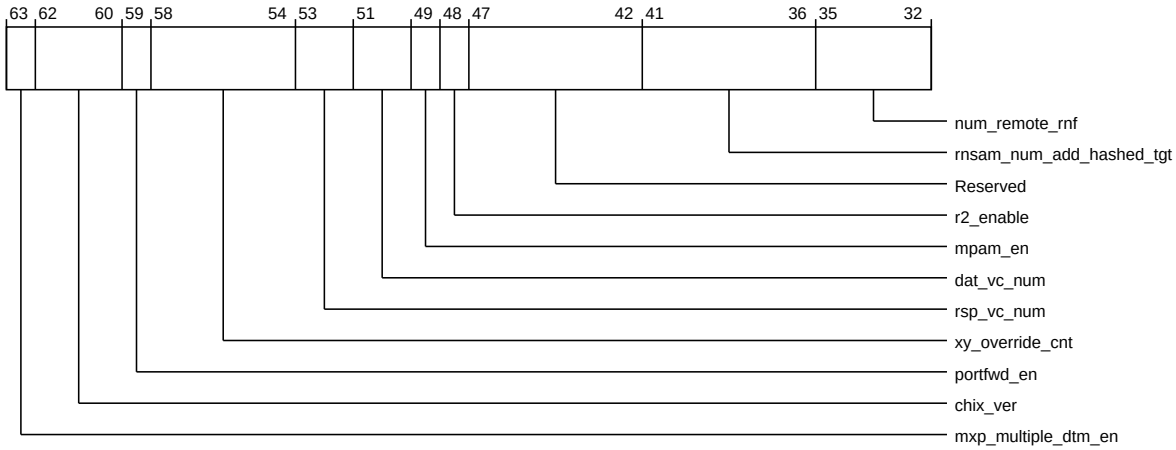
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-85: por_cfgm_por_info_global (high)



The following table shows the por_info_global higher register bit assignments.

Table 5-99: por_cfgm_por_info_global (high)

Bits	Field name	Description	Type	Reset
63	mxp_multiple_dtm_en	Multiple DTMs feature enable. This is used if number of device ports on the XP is > 2	RO	Configuration dependent
62:60	chix_ver	CHIX Version Parameter: 2 -> CHIB, 3 -> CHIC, 4 -> CHID, 5 -> CHIE	RO	Configuration dependent
59	portfwd_en	CCIX Port to Port Forwarding feature enable	RO	Configuration dependent
58:54	xy_override_cnt	Number of Src-Tgt pairs whose XY route path can be overriden	RO	Configuration dependent
53:52	rsp_vc_num	Number of additional RSP channels internal to MXP. For inreased bandwidth, this parameter need to be set to 2	RO	Configuration dependent
51:50	dat_vc_num	Number of additional DAT channels internal to MXP. For inreased bandwidth, this parameter need to be set to 2	RO	Configuration dependent
49	mpam_en	MPAM enable	RO	Configuration dependent
48	r2_enable	CMN R2 feature enable	RO	Configuration dependent
47:42	Reserved	Reserved	RO	-

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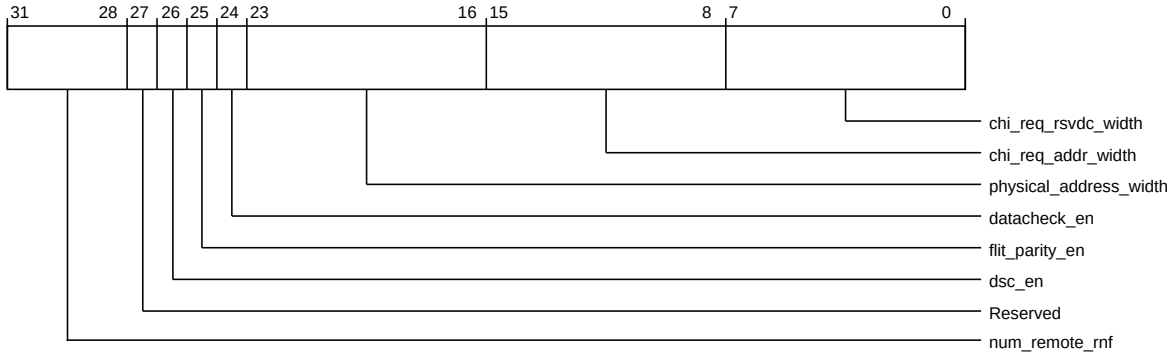
Bits	Field name	Description	Type	Reset
41:36	rnsam_num_add_hashed_tgt	Number of additional hashed target ID's supported by the RN SAM, beyond the local HNF count	RO	Configuration dependent
35:32	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-86: por_cfgm_por_info_global (low)



The following table shows the por_info_global lower register bit assignments.

Table 5-100: por_cfgm_por_info_global (low)

Bits	Field name	Description	Type	Reset
31:28	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent
27	Reserved	Reserved	RO	-
26	dsc_en	DSC Enable	RO	Configuration dependent
25	flit_parity_en	Indicates whether parity checking is enabled in the transport layer on all flits sent on the interconnect	RO	Configuration dependent
24	datacheck_en	Indicates whether datacheck feature is enabled for CHI DAT flit	RO	Configuration dependent
23:16	physical_address_width	Physical address width	RO	Configuration dependent
15:8	chi_req_addr_width	REQ address width	RO	Configuration dependent
7:0	chi_req_rsvdc_width	RSVDC field width in CHI REQ flit	RO	Configuration dependent

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5.3.1.44 por_ppu_int_enable

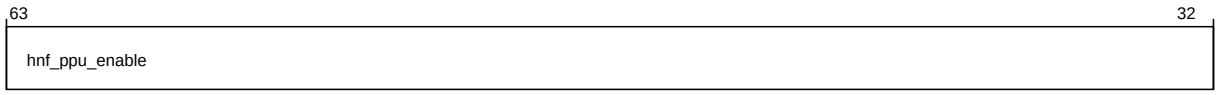
Configures the HN-F PPU event interrupt. Contains the interrupt mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1C00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-87: por_cfgm_por_ppu_int_enable (high)



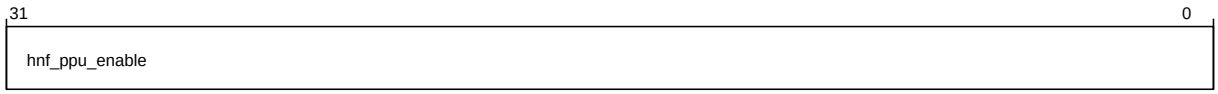
The following table shows the por_ppu_int_enable higher register bit assignments.

Table 5-101: por_cfgm_por_ppu_int_enable (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_enable	Interrupt mask	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-88: por_cfgm_por_ppu_int_enable (low)



The following table shows the por_ppu_int_enable lower register bit assignments.

Table 5-102: por_cfgm_por_ppu_int_enable (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_enable	Interrupt mask	RW	64'b0

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5.3.1.45 por_ppu_int_status

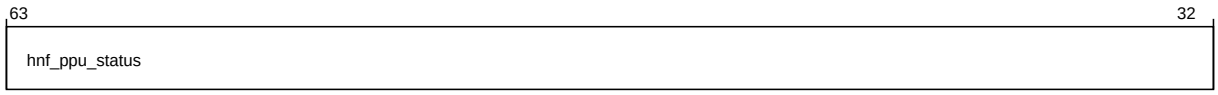
Provides HN-F PPU event interrupt status.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h1C08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-89: por_cfgm_por_ppu_int_status (high)



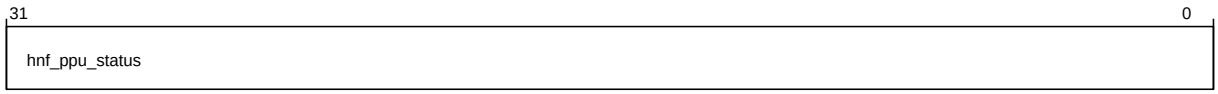
The following table shows the por_ppu_int_status higher register bit assignments.

Table 5-103: por_cfgm_por_ppu_int_status (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_status	Interrupt status	W1C	64'b0

The following figure shows the lower register bit assignments.

Figure 5-90: por_cfgm_por_ppu_int_status (low)



The following table shows the por_ppu_int_status lower register bit assignments.

Table 5-104: por_cfgm_por_ppu_int_status (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_status	Interrupt status	W1C	64'b0

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5.3.1.46 por_ppu_qactive_hyst

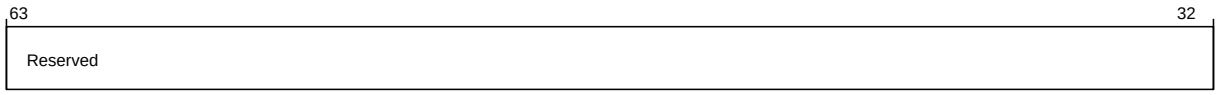
Number of hysteresis clock cycles to retain QACTIVE assertion

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1C10
Register reset 64'b0000000000000010
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-91: por_cfgm_por_ppu_qactive_hyst (high)



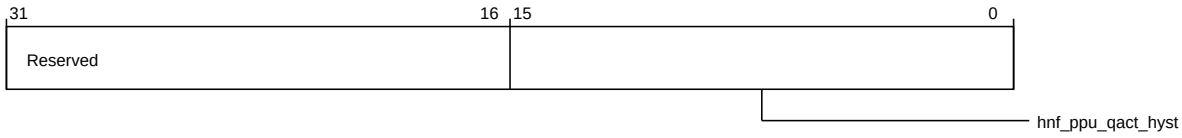
The following table shows the por_ppu_qactive_hyst higher register bit assignments.

Table 5-105: por_cfgm_por_ppu_qactive_hyst (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-92: por_cfgm_por_ppu_qactive_hyst (low)



The following table shows the por_ppu_qactive_hyst lower register bit assignments.

Table 5-106: por_cfgm_por_ppu_qactive_hyst (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_ppu_qact_hyst	QACTIVE hysteresis	RW	16'h10

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5.3.1.47 por_mpam_s_err_int_status

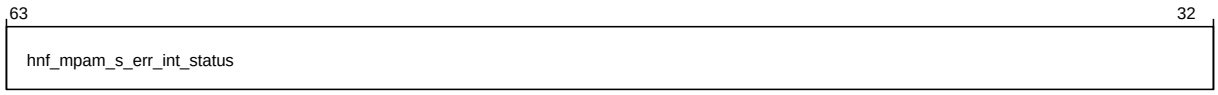
Provides HN-F MPAM Secure Error interrupt status.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h1C18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-93: por_cfgm_por_mpam_s_err_int_status (high)



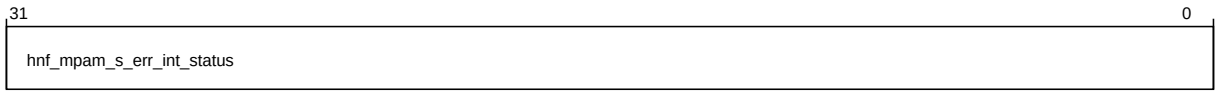
The following table shows the por_mpam_s_err_int_status higher register bit assignments.

Table 5-107: por_cfgm_por_mpam_s_err_int_status (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_mpam_s_err_int_status	MPAM S Interrupt status	W1C	64'b0

The following figure shows the lower register bit assignments.

Figure 5-94: por_cfgm_por_mpam_s_err_int_status (low)



The following table shows the por_mpam_s_err_int_status lower register bit assignments.

Table 5-108: por_cfgm_por_mpam_s_err_int_status (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_mpam_s_err_int_status	MPAM S Interrupt status	W1C	64'b0

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5.3.1.48 por_mpam_ns_err_int_status

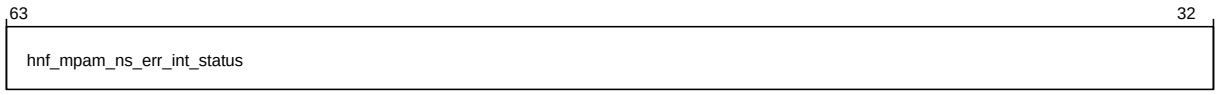
Provides HN-F MPAM Non-Secure Error interrupt status.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h1C20
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-95: por_cfgm_por_mpam_ns_err_int_status (high)



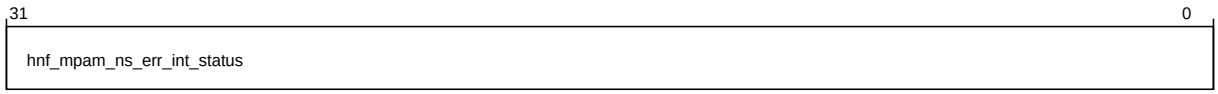
The following table shows the por_mpam_ns_err_int_status higher register bit assignments.

Table 5-109: por_cfgm_por_mpam_ns_err_int_status (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_mpam_ns_err_int_status	MPAM NS Interrupt status	W1C	64'b0

The following figure shows the lower register bit assignments.

Figure 5-96: por_cfgm_por_mpam_ns_err_int_status (low)



The following table shows the por_mpam_ns_err_int_status lower register bit assignments.

Table 5-110: por_cfgm_por_mpam_ns_err_int_status (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_mpam_ns_err_int_status	MPAM NS Interrupt status	W1C	64'b0

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5.3.1.49 por_cfgm_child_pointer_$index

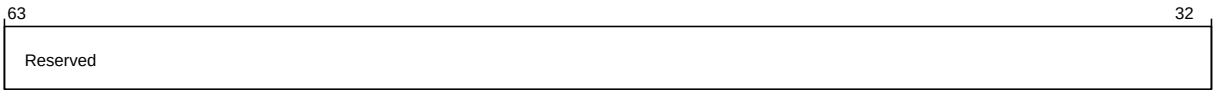
This register repeats 255 times. It is parameterized by the $index from 0 to 255. Contains base address of child configuration node. NOTE: There will be as many child pointer registers in the Global Config Unit as the number of XP's on the chip. Each successive child pointer register will be at the next 8 byte address boundary. Each successive child pointer register will be named with the suffix corresponding to the register number. For example por_cfgm_child_pointer_<0:255>.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset CHILD_POINTER_BASE + 8 * $index
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-97: por_cfgm_por_cfgm_child_pointer_$index (high)



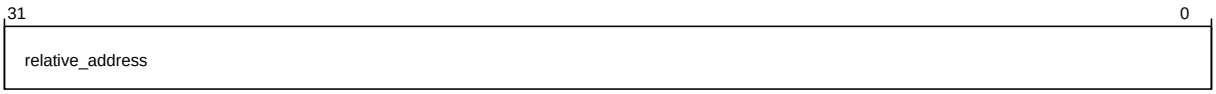
The following table shows the por_cfgm_child_pointer_$index higher register bit assignments.

Table 5-111: por_cfgm_por_cfgm_child_pointer_$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-98: por_cfgm_por_cfgm_child_pointer_$index (low)



The following table shows the por_cfgm_child_pointer_$index lower register bit assignments.

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Table 5-112: por_cfgm_por_cfgm_child_pointer_$index (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address	Bit 31: External or internal child node 1'b1: Indicates child pointer points to a configuration node that is external to CI-700 1'b0: Indicates child pointer points to a configuration node that is internal to CI-700 Bits [30]: Set to 1'b0 Bits [29:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

5.3.2 DN register descriptions

This section lists the DN registers.

5.3.2.1 por_dn_node_info

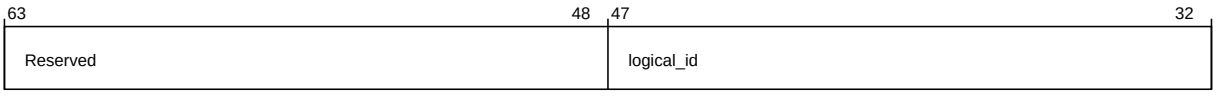
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-99: por_dn_por_dn_node_info (high)



The following table shows the por_dn_node_info higher register bit assignments.

Table 5-113: por_dn_por_dn_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

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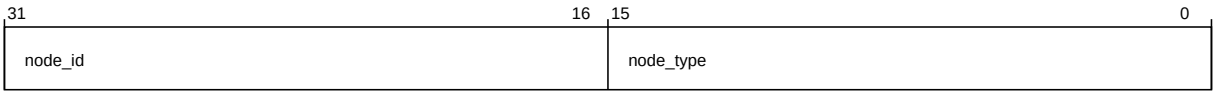
The following figure shows the lower register bit assignments.

Figure 5-100: por_dn_por_dn_node_info (low)



The following table shows the por_dn_node_info lower register bit assignments.

Table 5-114: por_dn_por_dn_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0001

5.3.2.2 por_dn_child_info

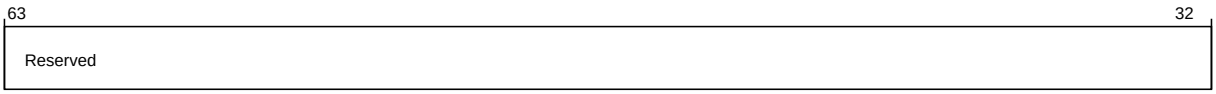
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-101: por_dn_por_dn_child_info (high)



The following table shows the por_dn_child_info higher register bit assignments.

Table 5-115: por_dn_por_dn_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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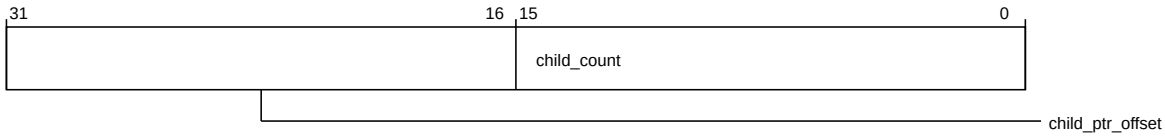
The following figure shows the lower register bit assignments.

Figure 5-102: por_dn_por_dn_child_info (low)



The following table shows the por_dn_child_info lower register bit assignments.

Table 5-116: por_dn_por_dn_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

5.3.2.3 por_dn_build_info

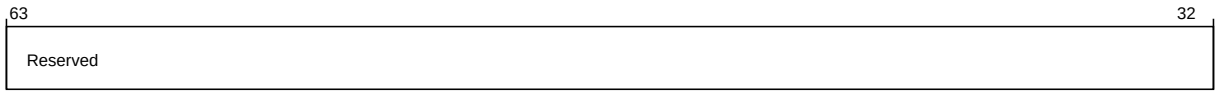
Contains the configuration parameter values. Indicates the specific DN configuration.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset 64'b1
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-103: por_dn_por_dn_build_info (high)



The following table shows the por_dn_build_info higher register bit assignments.

Table 5-117: por_dn_por_dn_build_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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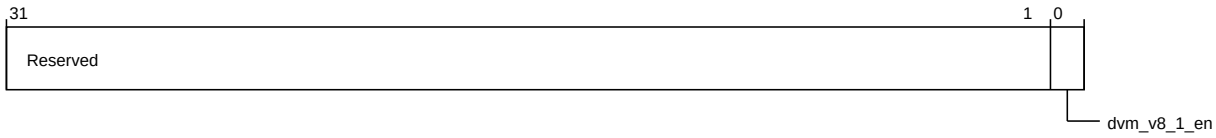
The following figure shows the lower register bit assignments.

Figure 5-104: por_dn_por_dn_build_info (low)



The following table shows the por_dn_build_info lower register bit assignments.

Table 5-118: por_dn_por_dn_build_info (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	dvm_v8_1_en	Determines whether all nodes receiving DVM snoops support DVM v8.1 operations; must be set to 0 if not supported by all nodes, therefore allowing the node to perform demotion before sending out the DVM snoop	RO	1'b1

5.3.2.4 por_dn_secure_register_groups_override

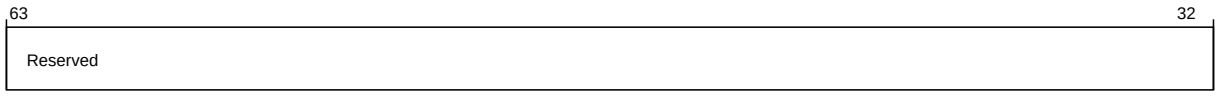
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-105: por_dn_por_dn_secure_register_groups_override (high)



The following table shows the por_dn_secure_register_groups_override higher register bit assignments.

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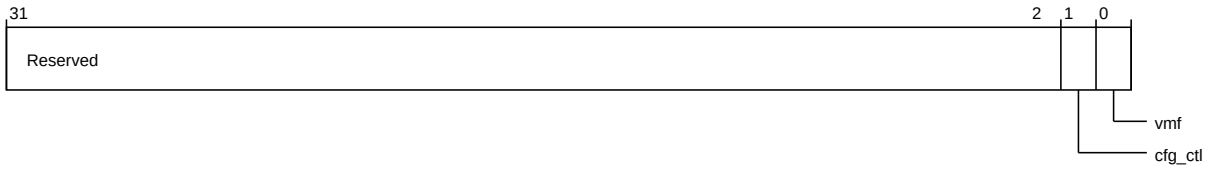
Table 5-119: por_dn_por_dn_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-106: por_dn_por_dn_secure_register_groups_override (low)



The following table shows the por_dn_secure_register_groups_override lower register bit assignments.

Table 5-120: por_dn_por_dn_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_dn_cfg_ctl)	RW	1'b0
0	vmf	Allows Non-secure access to Secure VMF registers	RW	1'b0

5.3.2.5 por_dn_cfg_ctl

Functions as the configuration control register for DVM Node.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_dn_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

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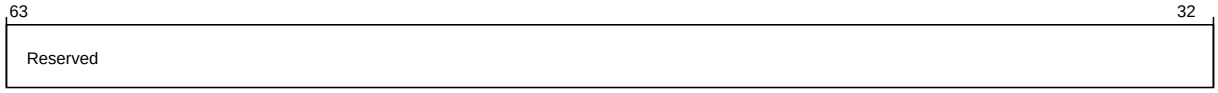
Figure 5-107: por_dn_por_dn_cfg_ctl (high)



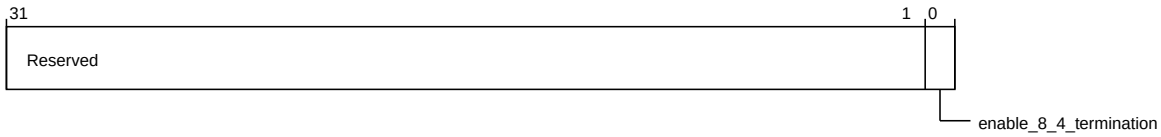
The following table shows the por_dn_cfg_ctl higher register bit assignments.

Table 5-121: por_dn_por_dn_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-108: por_dn_por_dn_cfg_ctl (low)



The following table shows the por_dn_cfg_ctl lower register bit assignments.

Table 5-122: por_dn_por_dn_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	enable_8_4_termination	Enables termination of 8.4 DVMOps in DN.	RW	1'b0

5.3.2.6 por_dn_aux_ctl

Functions as the auxiliary control register for DN.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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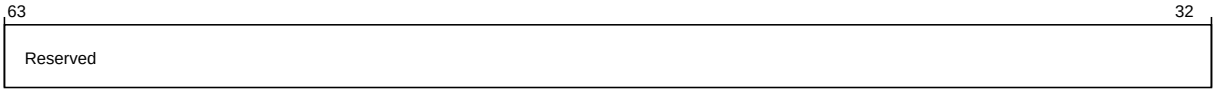
Figure 5-109: por_dn_por_dn_aux_ctl (high)



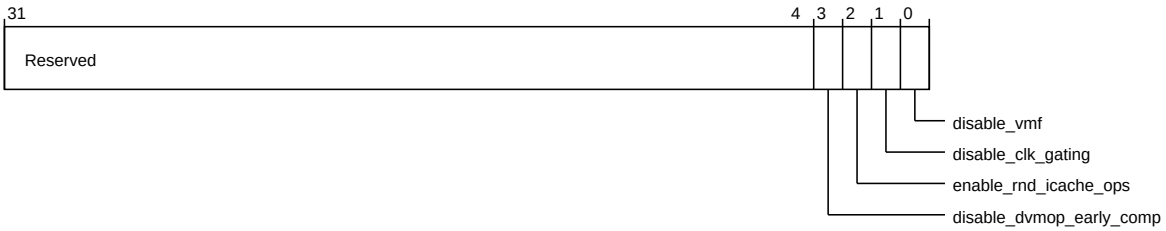
The following table shows the por_dn_aux_ctl higher register bit assignments.

Table 5-123: por_dn_por_dn_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-110: por_dn_por_dn_aux_ctl (low)



The following table shows the por_dn_aux_ctl lower register bit assignments.

Table 5-124: por_dn_por_dn_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	disable_dvmop_early_comp	Disables Early Comp (CompDBID) for DVMOps	RW	1'b0
2	enable_rnd_icache_ops	Filters out BPI and VICI/PICI Snps to RNDs when set	RW	Configuration dependent
1	disable_clk_gating	Disables autonomous clock gating when set	RW	1'b0
0	disable_vmf	This bit is currently not supported. Software must not program this bit.	RW	Configuration dependent

5.3.2.7 por_dn_vmf0_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

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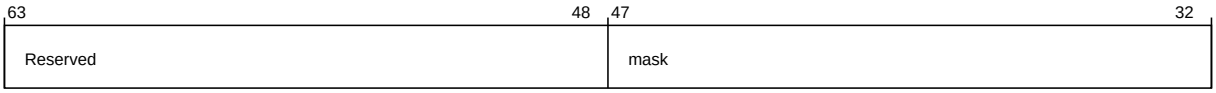
Register width (Bits) 64
Address offset 16'hC00
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-111: por_dn_por_dn_vmf0_ctrl (high)



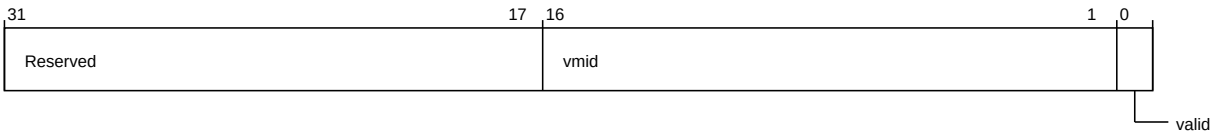
The following table shows the por_dn_vmf0_ctrl higher register bit assignments.

Table 5-125: por_dn_por_dn_vmf0_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf0_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-112: por_dn_por_dn_vmf0_ctrl (low)



The following table shows the por_dn_vmf0_ctrl lower register bit assignments.

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Table 5-126: por_dn_por_dn_vmf0_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.8 por_dn_vmf0_rnf0

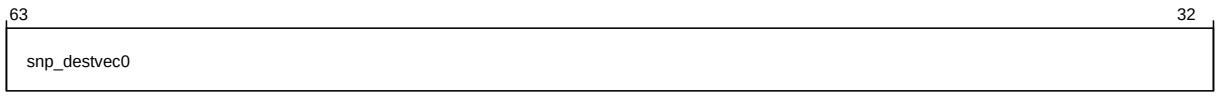
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-113: por_dn_por_dn_vmf0_rnf0 (high)



The following table shows the por_dn_vmf0_rnf0 higher register bit assignments.

Table 5-127: por_dn_por_dn_vmf0_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

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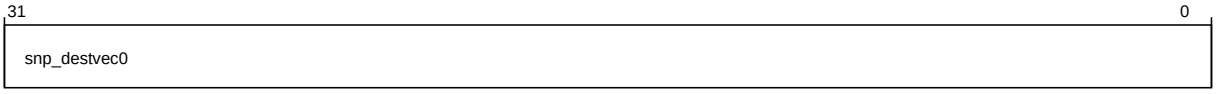
The following figure shows the lower register bit assignments.

Figure 5-114: por_dn_por_dn_vmf0_rnf0 (low)



The following table shows the por_dn_vmf0_rnf0 lower register bit assignments.

Table 5-128: por_dn_por_dn_vmf0_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

5.3.2.9 por_dn_vmf0_rnd

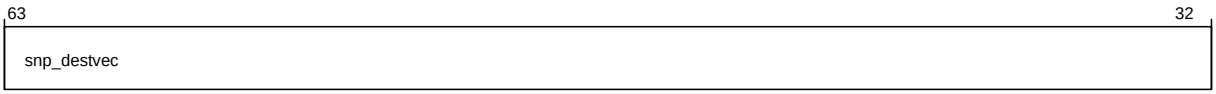
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-115: por_dn_por_dn_vmf0_rnd (high)



The following table shows the por_dn_vmf0_rnd higher register bit assignments.

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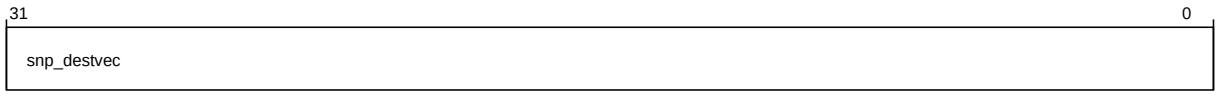
Table 5-129: por_dn_por_dn_vmf0_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-116: por_dn_por_dn_vmf0_rnd (low)



The following table shows the por_dn_vmf0_rnd lower register bit assignments.

Table 5-130: por_dn_por_dn_vmf0_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

5.3.2.10 por_dn_vmf0_cxra

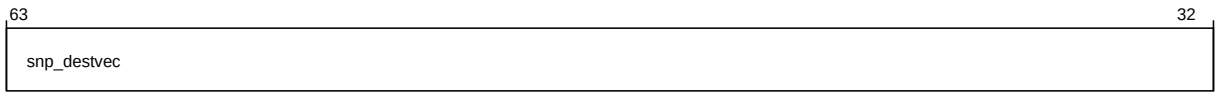
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-117: por_dn_por_dn_vmf0_cxra (high)



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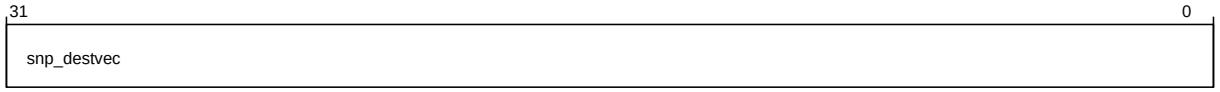
The following table shows the por_dn_vmf0_cxra higher register bit assignments.

Table 5-131: por_dn_por_dn_vmf0_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-118: por_dn_por_dn_vmf0_cxra (low)



The following table shows the por_dn_vmf0_cxra lower register bit assignments.

Table 5-132: por_dn_por_dn_vmf0_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

5.3.2.11 por_dn_vmf1_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC20
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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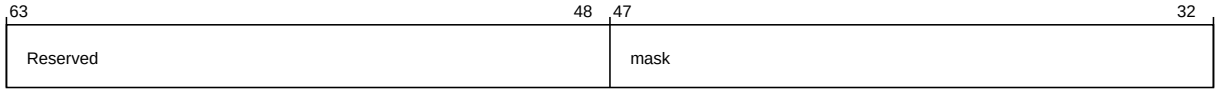
Figure 5-119: por_dn_por_dn_vmf1_ctrl (high)



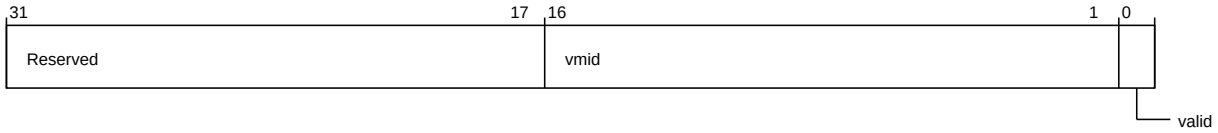
The following table shows the por_dn_vmf1_ctrl higher register bit assignments.

Table 5-133: por_dn_por_dn_vmf1_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf1_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-120: por_dn_por_dn_vmf1_ctrl (low)



The following table shows the por_dn_vmf1_ctrl lower register bit assignments.

Table 5-134: por_dn_por_dn_vmf1_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

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5.3.2.12 por_dn_vmf1_rnf0

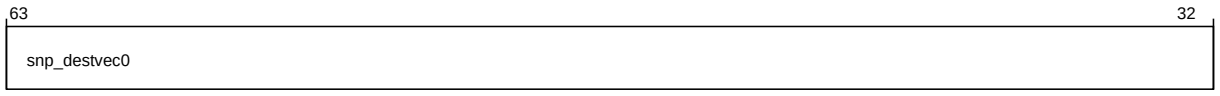
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-121: por_dn_por_dn_vmf1_rnf0 (high)



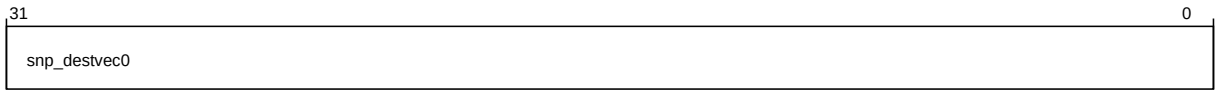
The following table shows the por_dn_vmf1_rnf0 higher register bit assignments.

Table 5-135: por_dn_por_dn_vmf1_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-122: por_dn_por_dn_vmf1_rnf0 (low)



The following table shows the por_dn_vmf1_rnf0 lower register bit assignments.

Table 5-136: por_dn_por_dn_vmf1_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

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5.3.2.13 por_dn_vmf1_rnd

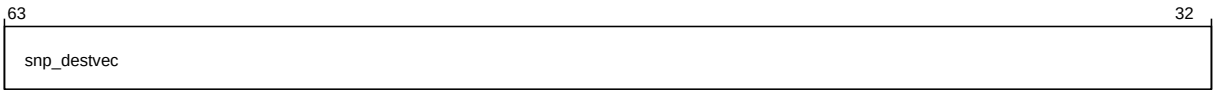
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-123: por_dn_por_dn_vmf1_rnd (high)



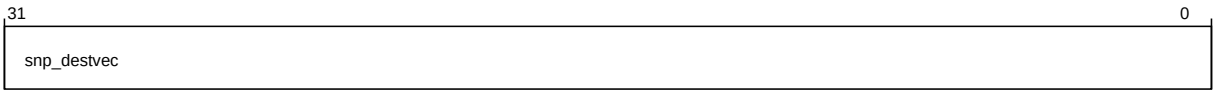
The following table shows the por_dn_vmf1_rnd higher register bit assignments.

Table 5-137: por_dn_por_dn_vmf1_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-124: por_dn_por_dn_vmf1_rnd (low)



The following table shows the por_dn_vmf1_rnd lower register bit assignments.

Table 5-138: por_dn_por_dn_vmf1_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

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5.3.2.14 por_dn_vmf1_cxra

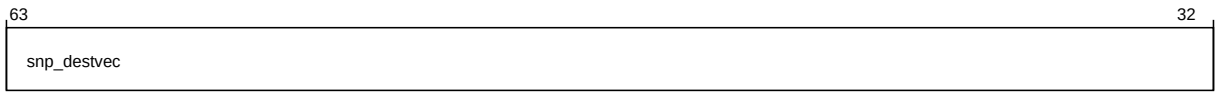
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-125: por_dn_por_dn_vmf1_cxra (high)



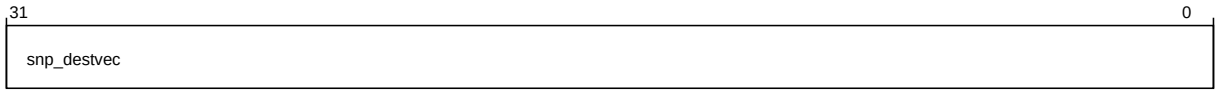
The following table shows the por_dn_vmf1_cxra higher register bit assignments.

Table 5-139: por_dn_por_dn_vmf1_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-126: por_dn_por_dn_vmf1_cxra (low)



The following table shows the por_dn_vmf1_cxra lower register bit assignments.

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Table 5-140: por_dn_por_dn_vmf1_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

5.3.2.15 por_dn_vmf2_ctrl

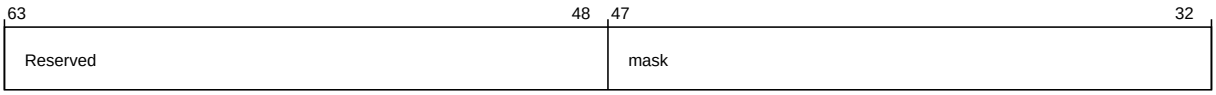
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC40
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-127: por_dn_por_dn_vmf2_ctrl (high)



The following table shows the por_dn_vmf2_ctrl higher register bit assignments.

Table 5-141: por_dn_por_dn_vmf2_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf2_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

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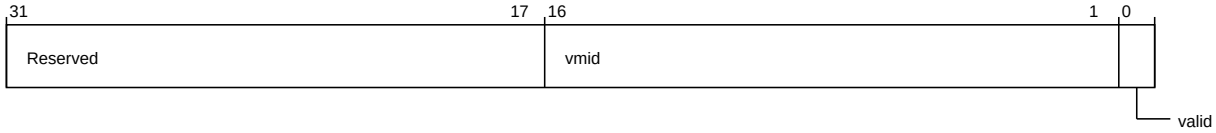
Figure 5-128: por_dn_por_dn_vmf2_ctrl (low)



The following table shows the por_dn_vmf2_ctrl lower register bit assignments.

Table 5-142: por_dn_por_dn_vmf2_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.16 por_dn_vmf2_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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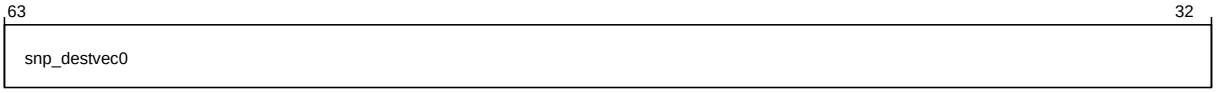
Figure 5-129: por_dn_por_dn_vmf2_rnf0 (high)



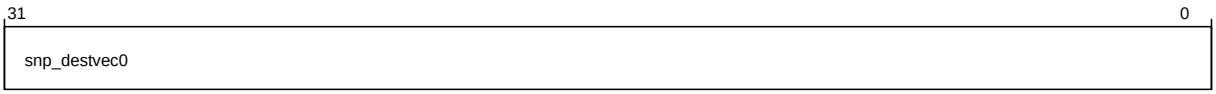
The following table shows the por_dn_vmf2_rnf0 higher register bit assignments.

Table 5-143: por_dn_por_dn_vmf2_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-130: por_dn_por_dn_vmf2_rnf0 (low)



The following table shows the por_dn_vmf2_rnf0 lower register bit assignments.

Table 5-144: por_dn_por_dn_vmf2_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

5.3.2.17 por_dn_vmf2_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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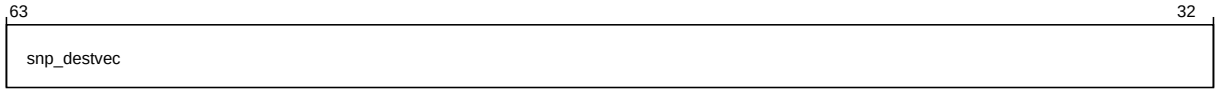
Figure 5-131: por_dn_por_dn_vmf2_rnd (high)



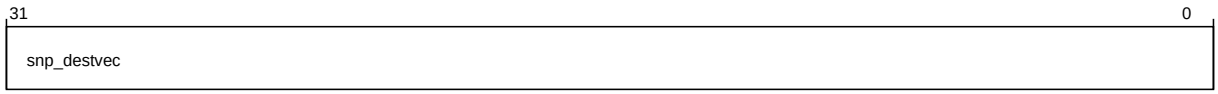
The following table shows the por_dn_vmf2_rnd higher register bit assignments.

Table 5-145: por_dn_por_dn_vmf2_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-132: por_dn_por_dn_vmf2_rnd (low)



The following table shows the por_dn_vmf2_rnd lower register bit assignments.

Table 5-146: por_dn_por_dn_vmf2_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

5.3.2.18 por_dn_vmf2_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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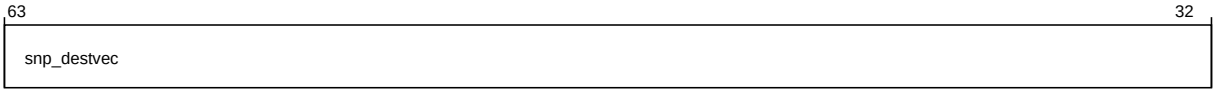
The following figure shows the higher register bit assignments.

Figure 5-133: por_dn_por_dn_vmf2_cxra (high)



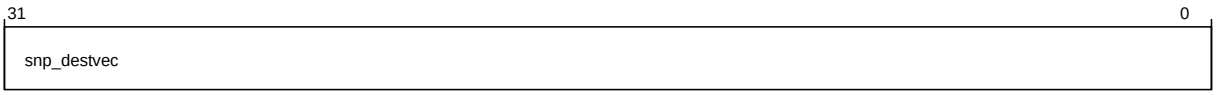
The following table shows the por_dn_vmf2_cxra higher register bit assignments.

Table 5-147: por_dn_por_dn_vmf2_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-134: por_dn_por_dn_vmf2_cxra (low)



The following table shows the por_dn_vmf2_cxra lower register bit assignments.

Table 5-148: por_dn_por_dn_vmf2_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

5.3.2.19 por_dn_vmf3_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC60
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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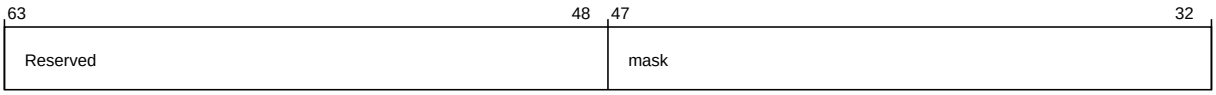
The following figure shows the higher register bit assignments.

Figure 5-135: por_dn_por_dn_vmf3_ctrl (high)



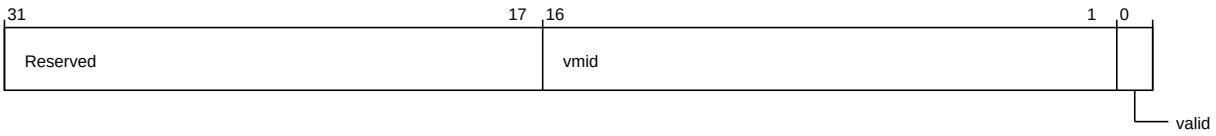
The following table shows the por_dn_vmf3_ctrl higher register bit assignments.

Table 5-149: por_dn_por_dn_vmf3_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf3_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-136: por_dn_por_dn_vmf3_ctrl (low)



The following table shows the por_dn_vmf3_ctrl lower register bit assignments.

Table 5-150: por_dn_por_dn_vmf3_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000

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Bits	Field name	Description	Type	Reset
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.20 por_dn_vmf3_rnf0

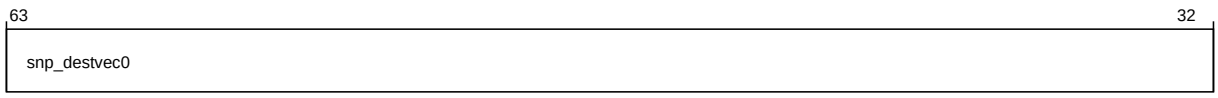
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC68
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-137: por_dn_por_dn_vmf3_rnf0 (high)



The following table shows the por_dn_vmf3_rnf0 higher register bit assignments.

Table 5-151: por_dn_por_dn_vmf3_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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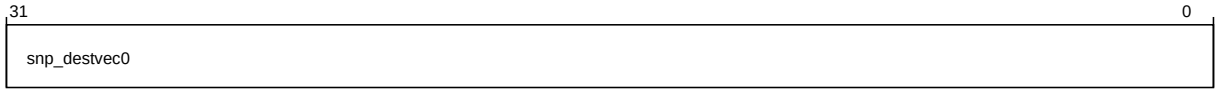
Figure 5-138: por_dn_por_dn_vmf3_rnf0 (low)



The following table shows the por_dn_vmf3_rnf0 lower register bit assignments.

Table 5-152: por_dn_por_dn_vmf3_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

5.3.2.21 por_dn_vmf3_rnd

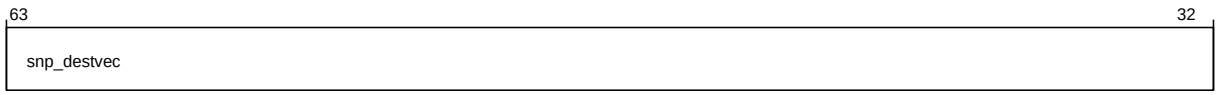
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-139: por_dn_por_dn_vmf3_rnd (high)



The following table shows the por_dn_vmf3_rnd higher register bit assignments.

Table 5-153: por_dn_por_dn_vmf3_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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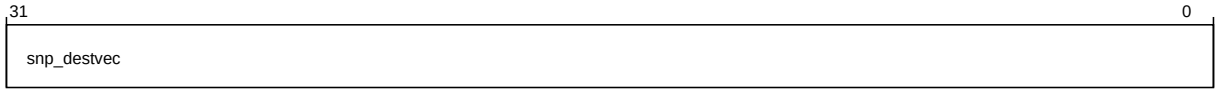
Figure 5-140: por_dn_por_dn_vmf3_rnd (low)



The following table shows the por_dn_vmf3_rnd lower register bit assignments.

Table 5-154: por_dn_por_dn_vmf3_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

5.3.2.22 por_dn_vmf3_cxra

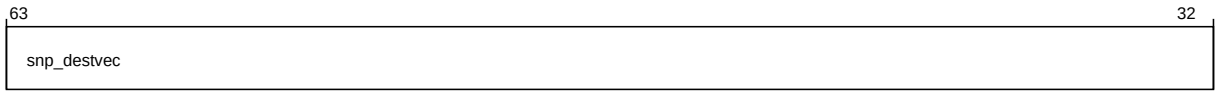
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-141: por_dn_por_dn_vmf3_cxra (high)



The following table shows the por_dn_vmf3_cxra higher register bit assignments.

Table 5-155: por_dn_por_dn_vmf3_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

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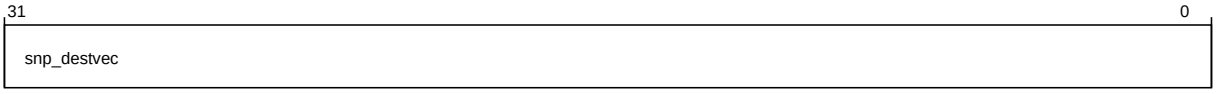
The following figure shows the lower register bit assignments.

Figure 5-142: por_dn_por_dn_vmf3_cxra (low)



The following table shows the por_dn_vmf3_cxra lower register bit assignments.

Table 5-156: por_dn_por_dn_vmf3_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

5.3.2.23 por_dn_vmf4_ctrl

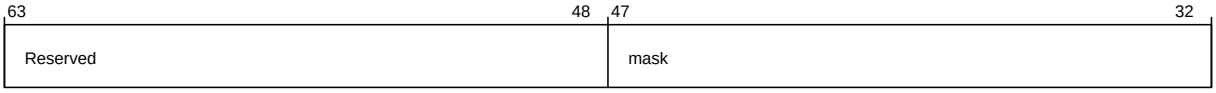
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC80
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-143: por_dn_por_dn_vmf4_ctrl (high)



The following table shows the por_dn_vmf4_ctrl higher register bit assignments.

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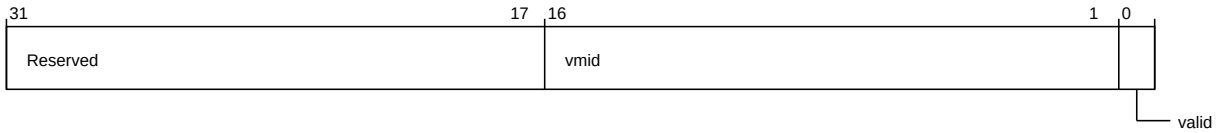
Table 5-157: por_dn_por_dn_vmf4_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf4_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-144: por_dn_por_dn_vmf4_ctrl (low)



The following table shows the por_dn_vmf4_ctrl lower register bit assignments.

Table 5-158: por_dn_por_dn_vmf4_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.24 por_dn_vmf4_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64

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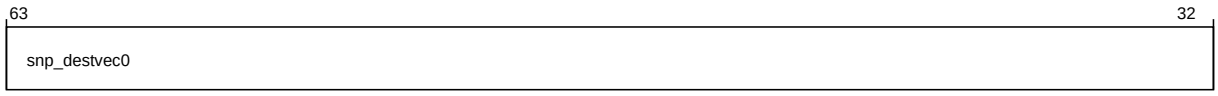
Address offset 16'hC88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-145: por_dn_por_dn_vmf4_rnf0 (high)



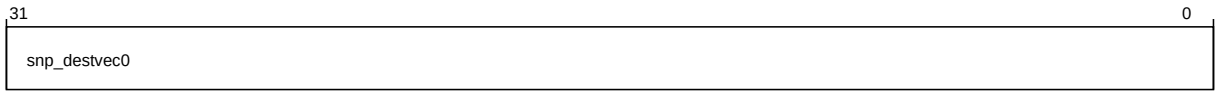
The following table shows the por_dn_vmf4_rnf0 higher register bit assignments.

Table 5-159: por_dn_por_dn_vmf4_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-146: por_dn_por_dn_vmf4_rnf0 (low)



The following table shows the por_dn_vmf4_rnf0 lower register bit assignments.

Table 5-160: por_dn_por_dn_vmf4_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

5.3.2.25 por_dn_vmf4_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

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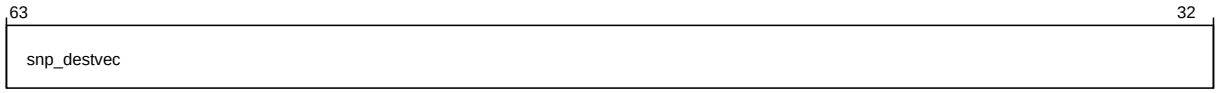
Register width (Bits) 64
Address offset 16'hC90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-147: por_dn_por_dn_vmf4_rnd (high)



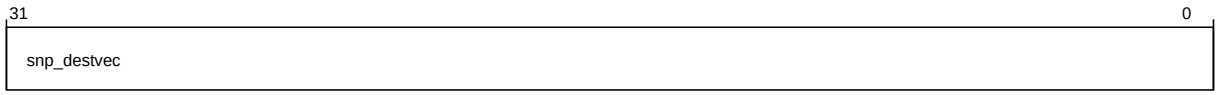
The following table shows the por_dn_vmf4_rnd higher register bit assignments.

Table 5-161: por_dn_por_dn_vmf4_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-148: por_dn_por_dn_vmf4_rnd (low)



The following table shows the por_dn_vmf4_rnd lower register bit assignments.

Table 5-162: por_dn_por_dn_vmf4_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

5.3.2.26 por_dn_vmf4_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

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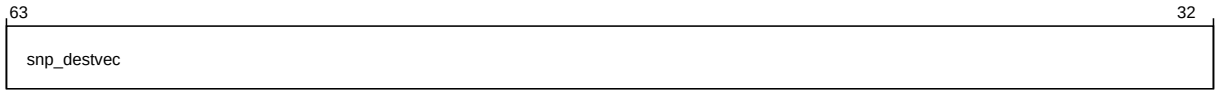
Type RW
Register width (Bits) 64
Address offset 16'hC98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-149: por_dn_por_dn_vmf4_cxra (high)



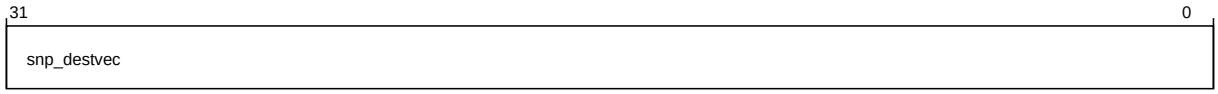
The following table shows the por_dn_vmf4_cxra higher register bit assignments.

Table 5-163: por_dn_por_dn_vmf4_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-150: por_dn_por_dn_vmf4_cxra (low)



The following table shows the por_dn_vmf4_cxra lower register bit assignments.

Table 5-164: por_dn_por_dn_vmf4_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

5.3.2.27 por_dn_vmf5_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

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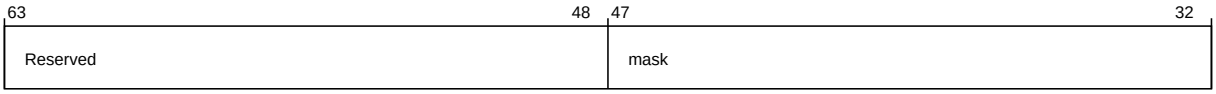
Type RW
Register width (Bits) 64
Address offset 16'hCA0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-151: por_dn_por_dn_vmf5_ctrl (high)



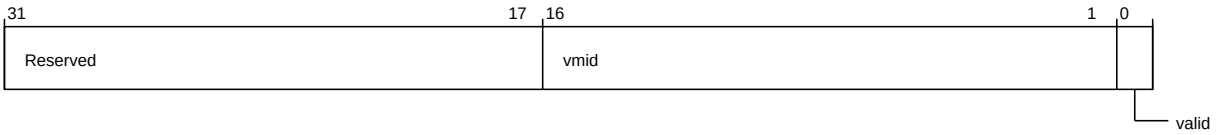
The following table shows the por_dn_vmf5_ctrl higher register bit assignments.

Table 5-165: por_dn_por_dn_vmf5_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf5_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-152: por_dn_por_dn_vmf5_ctrl (low)



The following table shows the por_dn_vmf5_ctrl lower register bit assignments.

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Table 5-166: por_dn_por_dn_vmf5_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.28 por_dn_vmf5_rnf0

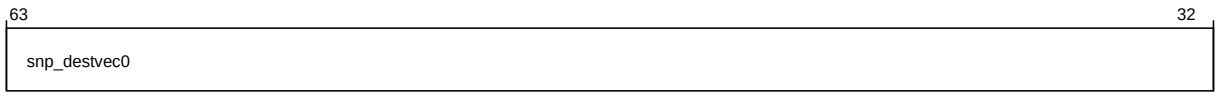
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-153: por_dn_por_dn_vmf5_rnf0 (high)



The following table shows the por_dn_vmf5_rnf0 higher register bit assignments.

Table 5-167: por_dn_por_dn_vmf5_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

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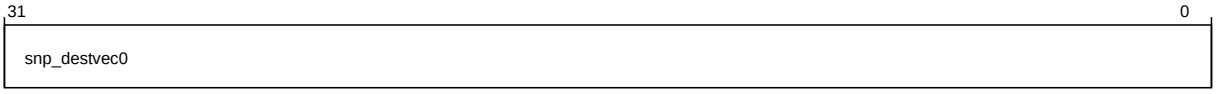
The following figure shows the lower register bit assignments.

Figure 5-154: por_dn_por_dn_vmf5_rnf0 (low)



The following table shows the por_dn_vmf5_rnf0 lower register bit assignments.

Table 5-168: por_dn_por_dn_vmf5_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

5.3.2.29 por_dn_vmf5_rnd

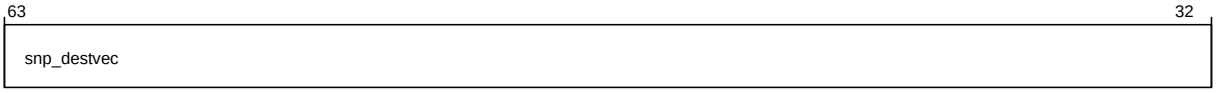
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-155: por_dn_por_dn_vmf5_rnd (high)



The following table shows the por_dn_vmf5_rnd higher register bit assignments.

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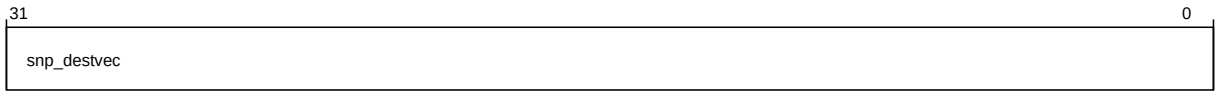
Table 5-169: por_dn_por_dn_vmf5_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-156: por_dn_por_dn_vmf5_rnd (low)



The following table shows the por_dn_vmf5_rnd lower register bit assignments.

Table 5-170: por_dn_por_dn_vmf5_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

5.3.2.30 por_dn_vmf5_cxra

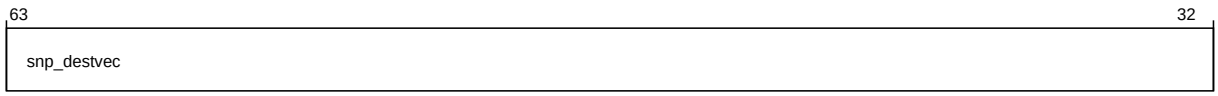
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-157: por_dn_por_dn_vmf5_cxra (high)



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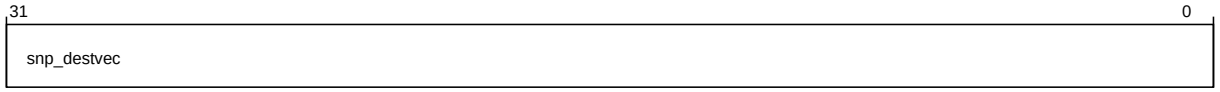
The following table shows the por_dn_vmf5_cxra higher register bit assignments.

Table 5-171: por_dn_por_dn_vmf5_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-158: por_dn_por_dn_vmf5_cxra (low)



The following table shows the por_dn_vmf5_cxra lower register bit assignments.

Table 5-172: por_dn_por_dn_vmf5_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

5.3.2.31 por_dn_vmf6_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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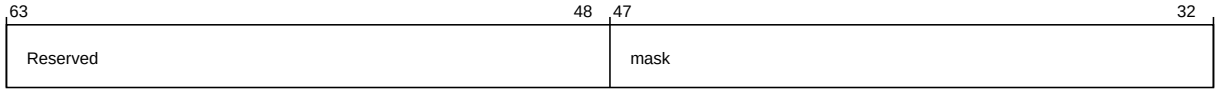
Figure 5-159: por_dn_por_dn_vmf6_ctrl (high)



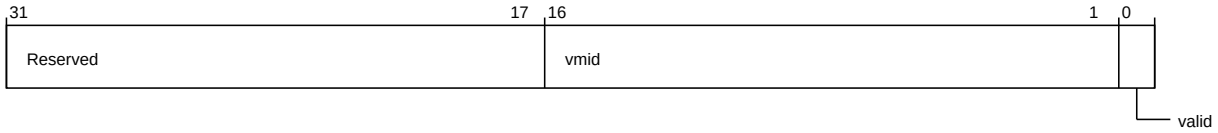
The following table shows the por_dn_vmf6_ctrl higher register bit assignments.

Table 5-173: por_dn_por_dn_vmf6_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf6_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-160: por_dn_por_dn_vmf6_ctrl (low)



The following table shows the por_dn_vmf6_ctrl lower register bit assignments.

Table 5-174: por_dn_por_dn_vmf6_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

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5.3.2.32 por_dn_vmf6_rnf0

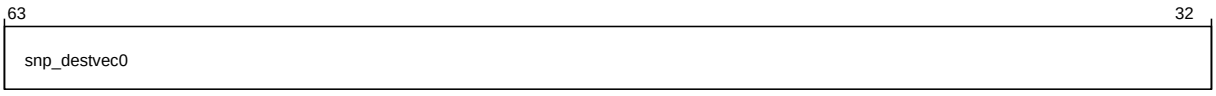
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-161: por_dn_por_dn_vmf6_rnf0 (high)



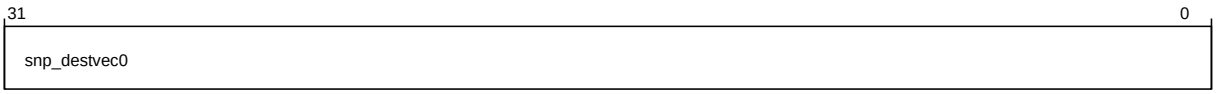
The following table shows the por_dn_vmf6_rnf0 higher register bit assignments.

Table 5-175: por_dn_por_dn_vmf6_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-162: por_dn_por_dn_vmf6_rnf0 (low)



The following table shows the por_dn_vmf6_rnf0 lower register bit assignments.

Table 5-176: por_dn_por_dn_vmf6_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

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5.3.2.33 por_dn_vmf6_rnd

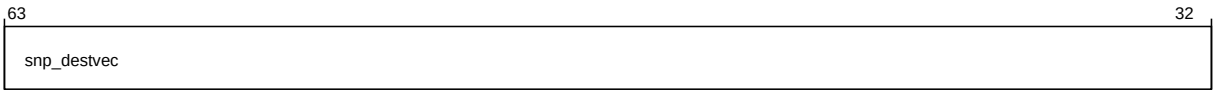
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-163: por_dn_por_dn_vmf6_rnd (high)



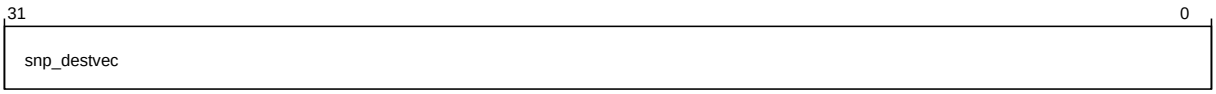
The following table shows the por_dn_vmf6_rnd higher register bit assignments.

Table 5-177: por_dn_por_dn_vmf6_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-164: por_dn_por_dn_vmf6_rnd (low)



The following table shows the por_dn_vmf6_rnd lower register bit assignments.

Table 5-178: por_dn_por_dn_vmf6_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

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5.3.2.34 por_dn_vmf6_cxra

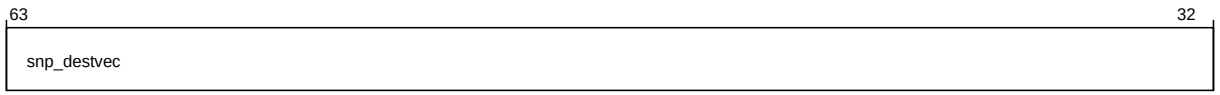
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCD8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-165: por_dn_por_dn_vmf6_cxra (high)



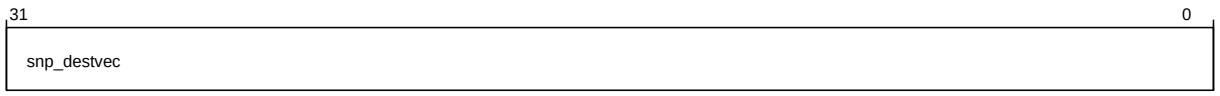
The following table shows the por_dn_vmf6_cxra higher register bit assignments.

Table 5-179: por_dn_por_dn_vmf6_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-166: por_dn_por_dn_vmf6_cxra (low)



The following table shows the por_dn_vmf6_cxra lower register bit assignments.

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Table 5-180: por_dn_por_dn_vmf6_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

5.3.2.35 por_dn_vmf7_ctrl

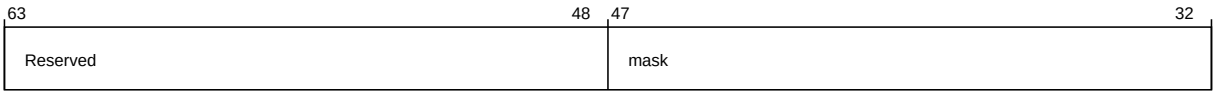
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCE0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-167: por_dn_por_dn_vmf7_ctrl (high)



The following table shows the por_dn_vmf7_ctrl higher register bit assignments.

Table 5-181: por_dn_por_dn_vmf7_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf7_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

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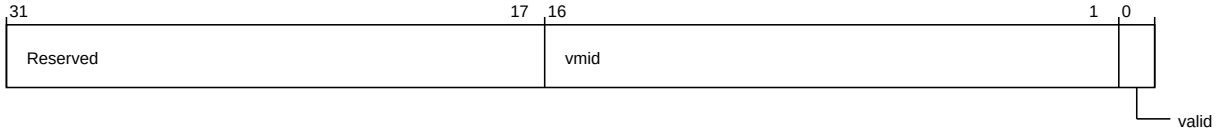
Figure 5-168: por_dn_por_dn_vmf7_ctrl (low)



The following table shows the por_dn_vmf7_ctrl lower register bit assignments.

Table 5-182: por_dn_por_dn_vmf7_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.36 por_dn_vmf7_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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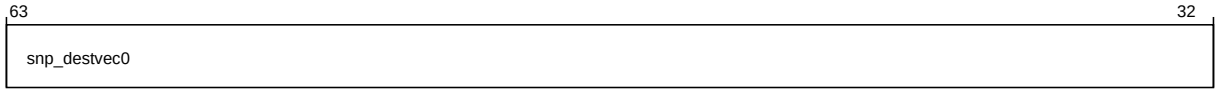
Figure 5-169: por_dn_por_dn_vmf7_rnf0 (high)



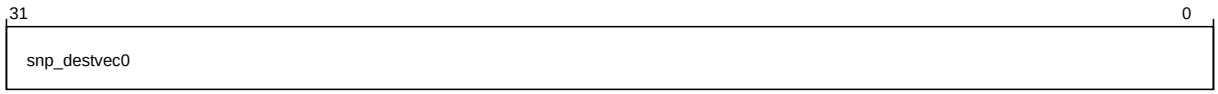
The following table shows the por_dn_vmf7_rnf0 higher register bit assignments.

Table 5-183: por_dn_por_dn_vmf7_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-170: por_dn_por_dn_vmf7_rnf0 (low)



The following table shows the por_dn_vmf7_rnf0 lower register bit assignments.

Table 5-184: por_dn_por_dn_vmf7_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

5.3.2.37 por_dn_vmf7_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCF0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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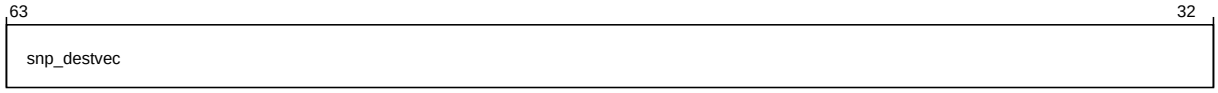
Figure 5-171: por_dn_por_dn_vmf7_rnd (high)



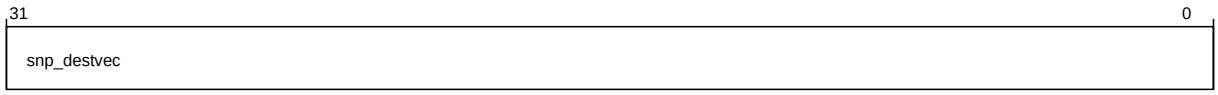
The following table shows the por_dn_vmf7_rnd higher register bit assignments.

Table 5-185: por_dn_por_dn_vmf7_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-172: por_dn_por_dn_vmf7_rnd (low)



The following table shows the por_dn_vmf7_rnd lower register bit assignments.

Table 5-186: por_dn_por_dn_vmf7_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

5.3.2.38 por_dn_vmf7_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCF8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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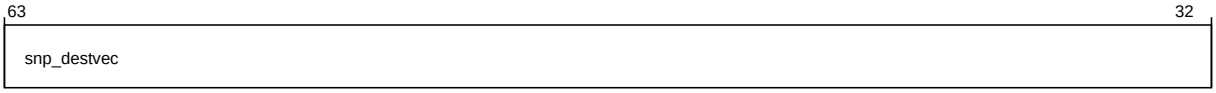
The following figure shows the higher register bit assignments.

Figure 5-173: por_dn_por_dn_vmf7_cxra (high)



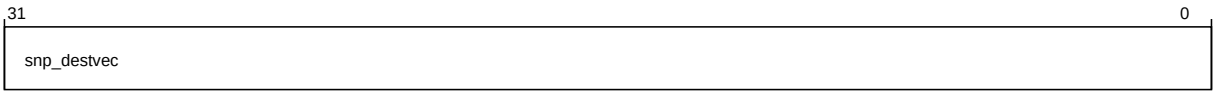
The following table shows the por_dn_vmf7_cxra higher register bit assignments.

Table 5-187: por_dn_por_dn_vmf7_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-174: por_dn_por_dn_vmf7_cxra (low)



The following table shows the por_dn_vmf7_cxra lower register bit assignments.

Table 5-188: por_dn_por_dn_vmf7_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

5.3.2.39 por_dn_vmf8_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD00
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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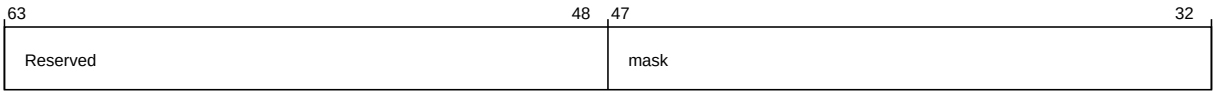
The following figure shows the higher register bit assignments.

Figure 5-175: por_dn_por_dn_vmf8_ctrl (high)



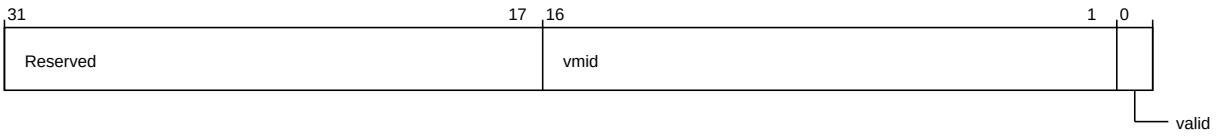
The following table shows the por_dn_vmf8_ctrl higher register bit assignments.

Table 5-189: por_dn_por_dn_vmf8_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf8_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-176: por_dn_por_dn_vmf8_ctrl (low)



The following table shows the por_dn_vmf8_ctrl lower register bit assignments.

Table 5-190: por_dn_por_dn_vmf8_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000

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Bits	Field name	Description	Type	Reset
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.40 por_dn_vmf8_rnf0

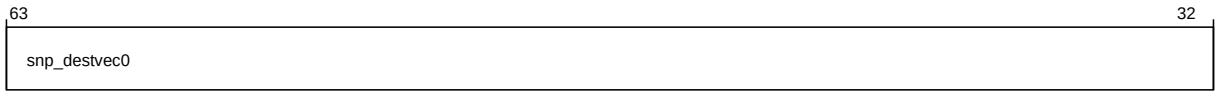
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-177: por_dn_por_dn_vmf8_rnf0 (high)



The following table shows the por_dn_vmf8_rnf0 higher register bit assignments.

Table 5-191: por_dn_por_dn_vmf8_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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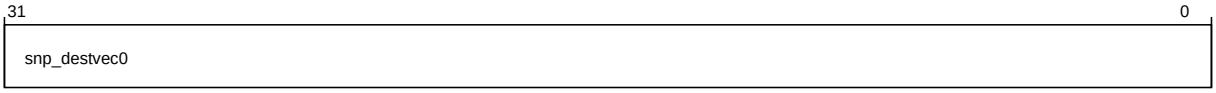
Figure 5-178: por_dn_por_dn_vmf8_rnf0 (low)



The following table shows the por_dn_vmf8_rnf0 lower register bit assignments.

Table 5-192: por_dn_por_dn_vmf8_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

5.3.2.41 por_dn_vmf8_rnd

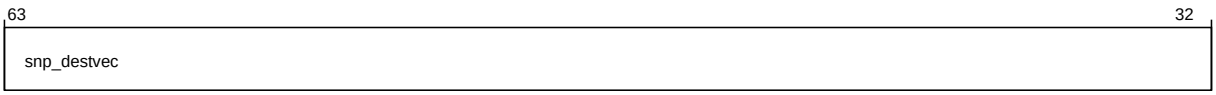
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-179: por_dn_por_dn_vmf8_rnd (high)



The following table shows the por_dn_vmf8_rnd higher register bit assignments.

Table 5-193: por_dn_por_dn_vmf8_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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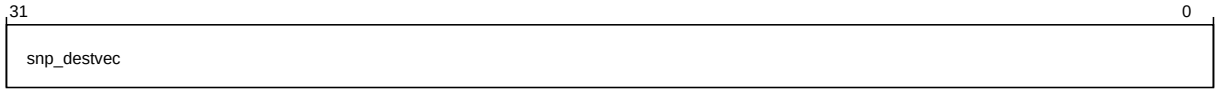
Figure 5-180: por_dn_por_dn_vmf8_rnd (low)



The following table shows the por_dn_vmf8_rnd lower register bit assignments.

Table 5-194: por_dn_por_dn_vmf8_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

5.3.2.42 por_dn_vmf8_cxra

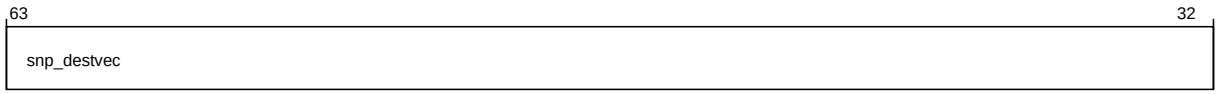
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-181: por_dn_por_dn_vmf8_cxra (high)



The following table shows the por_dn_vmf8_cxra higher register bit assignments.

Table 5-195: por_dn_por_dn_vmf8_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

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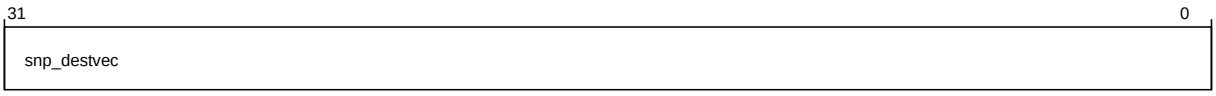
The following figure shows the lower register bit assignments.

Figure 5-182: por_dn_por_dn_vmf8_cxra (low)



The following table shows the por_dn_vmf8_cxra lower register bit assignments.

Table 5-196: por_dn_por_dn_vmf8_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

5.3.2.43 por_dn_vmf9_ctrl

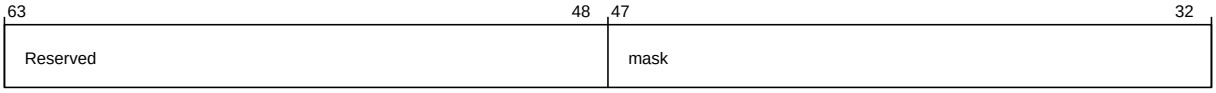
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD20
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-183: por_dn_por_dn_vmf9_ctrl (high)



The following table shows the por_dn_vmf9_ctrl higher register bit assignments.

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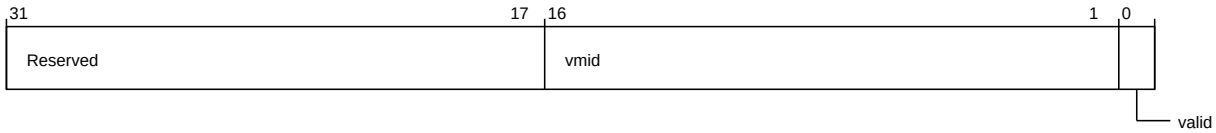
Table 5-197: por_dn_por_dn_vmf9_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf9_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-184: por_dn_por_dn_vmf9_ctrl (low)



The following table shows the por_dn_vmf9_ctrl lower register bit assignments.

Table 5-198: por_dn_por_dn_vmf9_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.44 por_dn_vmf9_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64

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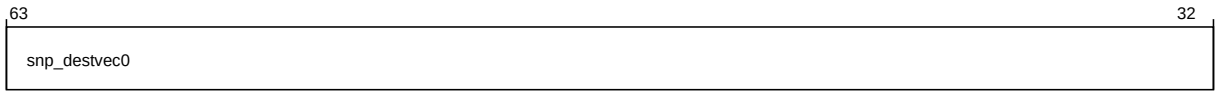
Address offset 16'hD28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-185: por_dn_por_dn_vmf9_rnf0 (high)



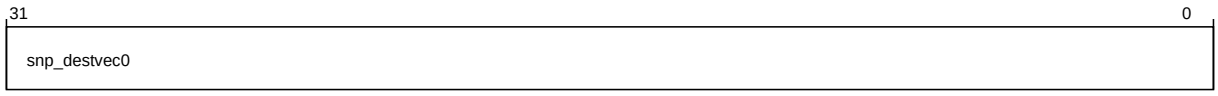
The following table shows the por_dn_vmf9_rnf0 higher register bit assignments.

Table 5-199: por_dn_por_dn_vmf9_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-186: por_dn_por_dn_vmf9_rnf0 (low)



The following table shows the por_dn_vmf9_rnf0 lower register bit assignments.

Table 5-200: por_dn_por_dn_vmf9_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

5.3.2.45 por_dn_vmf9_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

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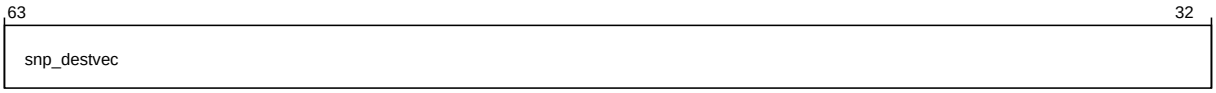
Register width (Bits) 64
Address offset 16'hD30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-187: por_dn_por_dn_vmf9_rnd (high)



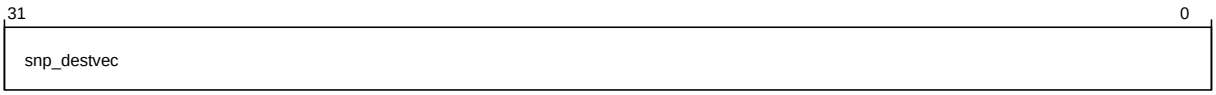
The following table shows the por_dn_vmf9_rnd higher register bit assignments.

Table 5-201: por_dn_por_dn_vmf9_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-188: por_dn_por_dn_vmf9_rnd (low)



The following table shows the por_dn_vmf9_rnd lower register bit assignments.

Table 5-202: por_dn_por_dn_vmf9_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

5.3.2.46 por_dn_vmf9_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

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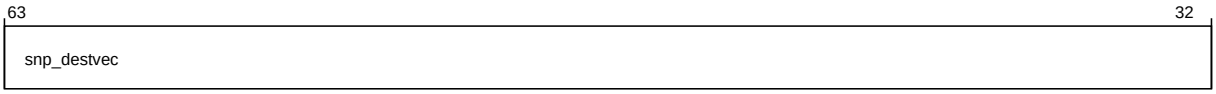
Type RW
Register width (Bits) 64
Address offset 16'hD38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-189: por_dn_por_dn_vmf9_cxra (high)



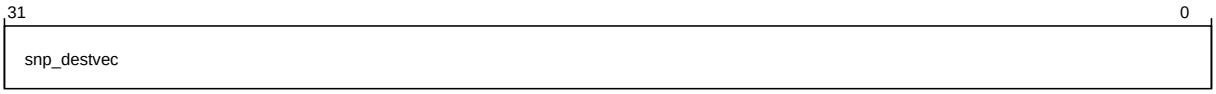
The following table shows the por_dn_vmf9_cxra higher register bit assignments.

Table 5-203: por_dn_por_dn_vmf9_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-190: por_dn_por_dn_vmf9_cxra (low)



The following table shows the por_dn_vmf9_cxra lower register bit assignments.

Table 5-204: por_dn_por_dn_vmf9_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

5.3.2.47 por_dn_vmf10_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

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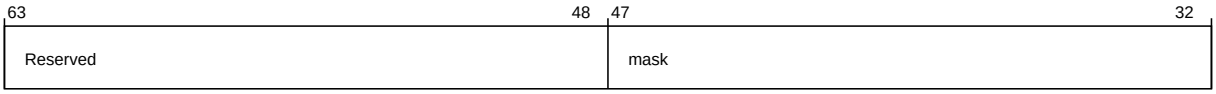
Type RW
Register width (Bits) 64
Address offset 16'hD40
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-191: por_dn_por_dn_vmf10_ctrl (high)



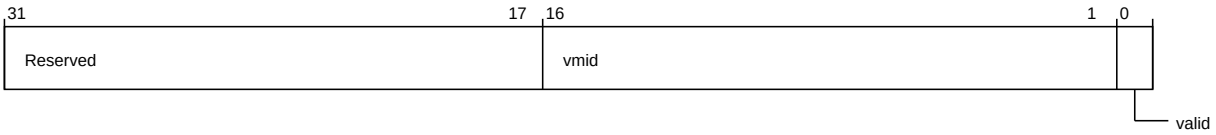
The following table shows the por_dn_vmf10_ctrl higher register bit assignments.

Table 5-205: por_dn_por_dn_vmf10_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf10_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-192: por_dn_por_dn_vmf10_ctrl (low)



The following table shows the por_dn_vmf10_ctrl lower register bit assignments.

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Table 5-206: por_dn_por_dn_vmf10_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.48 por_dn_vmf10_rnf0

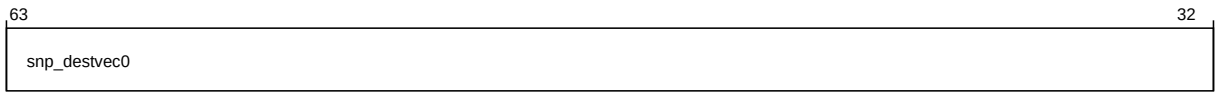
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-193: por_dn_por_dn_vmf10_rnf0 (high)



The following table shows the por_dn_vmf10_rnf0 higher register bit assignments.

Table 5-207: por_dn_por_dn_vmf10_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

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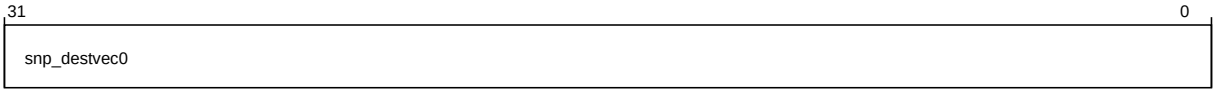
The following figure shows the lower register bit assignments.

Figure 5-194: por_dn_por_dn_vmf10_rnf0 (low)



The following table shows the por_dn_vmf10_rnf0 lower register bit assignments.

Table 5-208: por_dn_por_dn_vmf10_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

5.3.2.49 por_dn_vmf10_rnd

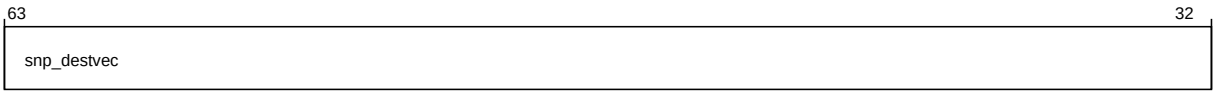
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-195: por_dn_por_dn_vmf10_rnd (high)



The following table shows the por_dn_vmf10_rnd higher register bit assignments.

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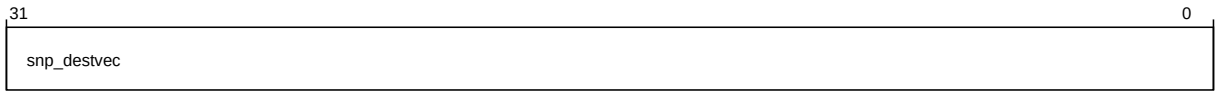
Table 5-209: por_dn_por_dn_vmf10_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-196: por_dn_por_dn_vmf10_rnd (low)



The following table shows the por_dn_vmf10_rnd lower register bit assignments.

Table 5-210: por_dn_por_dn_vmf10_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

5.3.2.50 por_dn_vmf10_cxra

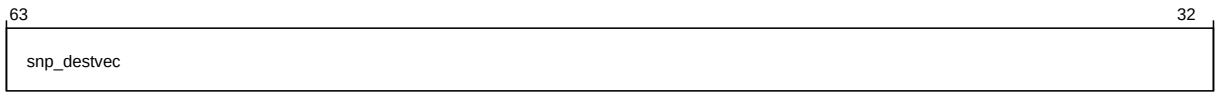
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-197: por_dn_por_dn_vmf10_cxra (high)



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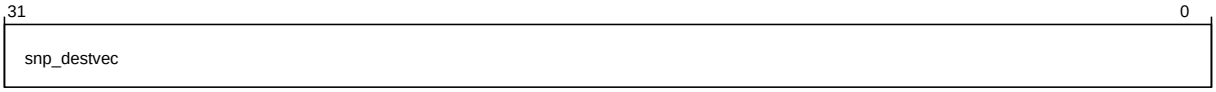
The following table shows the por_dn_vmf10_cxra higher register bit assignments.

Table 5-211: por_dn_por_dn_vmf10_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-198: por_dn_por_dn_vmf10_cxra (low)



The following table shows the por_dn_vmf10_cxra lower register bit assignments.

Table 5-212: por_dn_por_dn_vmf10_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

5.3.2.51 por_dn_vmf11_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD60
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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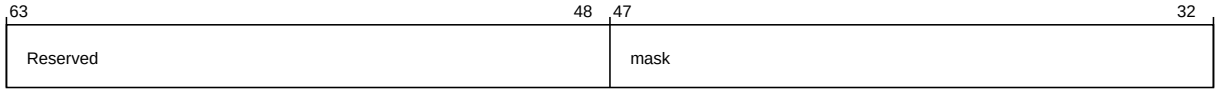
Figure 5-199: por_dn_por_dn_vmf11_ctrl (high)



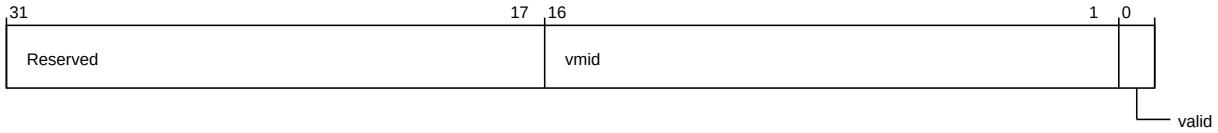
The following table shows the por_dn_vmf11_ctrl higher register bit assignments.

Table 5-213: por_dn_por_dn_vmf11_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf11_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-200: por_dn_por_dn_vmf11_ctrl (low)



The following table shows the por_dn_vmf11_ctrl lower register bit assignments.

Table 5-214: por_dn_por_dn_vmf11_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

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5.3.2.52 por_dn_vmf11_rnf0

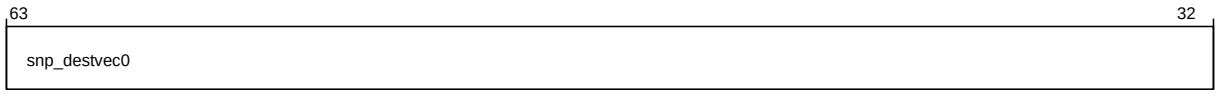
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD68
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-201: por_dn_por_dn_vmf11_rnf0 (high)



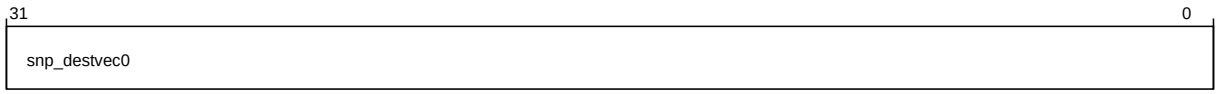
The following table shows the por_dn_vmf11_rnf0 higher register bit assignments.

Table 5-215: por_dn_por_dn_vmf11_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-202: por_dn_por_dn_vmf11_rnf0 (low)



The following table shows the por_dn_vmf11_rnf0 lower register bit assignments.

Table 5-216: por_dn_por_dn_vmf11_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

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5.3.2.53 por_dn_vmf11_rnd

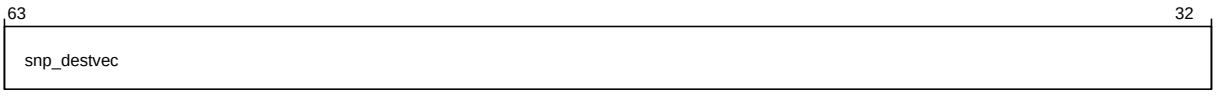
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-203: por_dn_por_dn_vmf11_rnd (high)



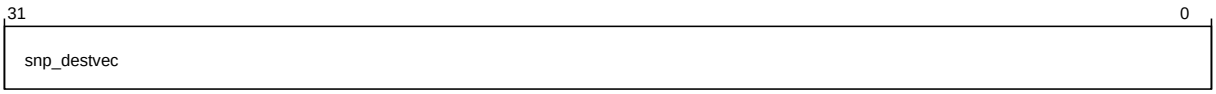
The following table shows the por_dn_vmf11_rnd higher register bit assignments.

Table 5-217: por_dn_por_dn_vmf11_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-204: por_dn_por_dn_vmf11_rnd (low)



The following table shows the por_dn_vmf11_rnd lower register bit assignments.

Table 5-218: por_dn_por_dn_vmf11_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

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5.3.2.54 por_dn_vmf11_cxra

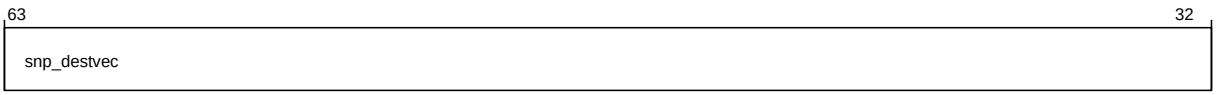
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-205: por_dn_por_dn_vmf11_cxra (high)



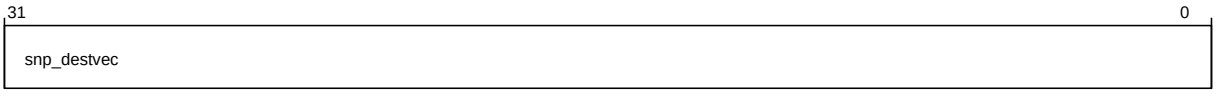
The following table shows the por_dn_vmf11_cxra higher register bit assignments.

Table 5-219: por_dn_por_dn_vmf11_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-206: por_dn_por_dn_vmf11_cxra (low)



The following table shows the por_dn_vmf11_cxra lower register bit assignments.

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Table 5-220: por_dn_por_dn_vmf11_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

5.3.2.55 por_dn_vmf12_ctrl

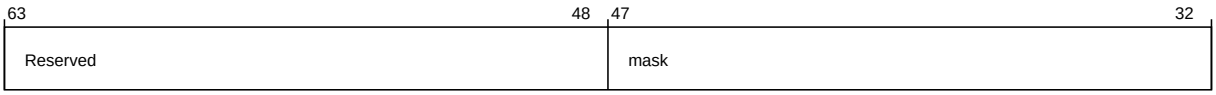
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD80
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-207: por_dn_por_dn_vmf12_ctrl (high)



The following table shows the por_dn_vmf12_ctrl higher register bit assignments.

Table 5-221: por_dn_por_dn_vmf12_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf12_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

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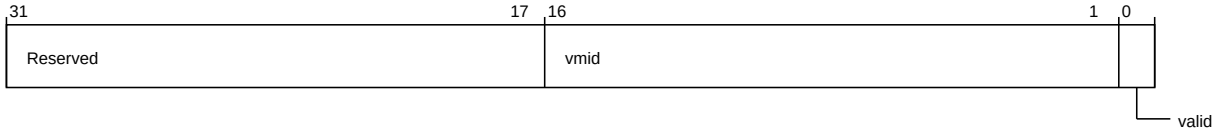
Figure 5-208: por_dn_por_dn_vmf12_ctrl (low)



The following table shows the por_dn_vmf12_ctrl lower register bit assignments.

Table 5-222: por_dn_por_dn_vmf12_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.56 por_dn_vmf12_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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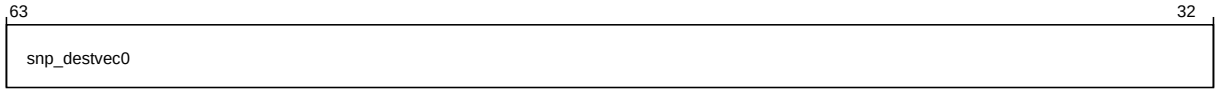
Figure 5-209: por_dn_por_dn_vmf12_rnf0 (high)



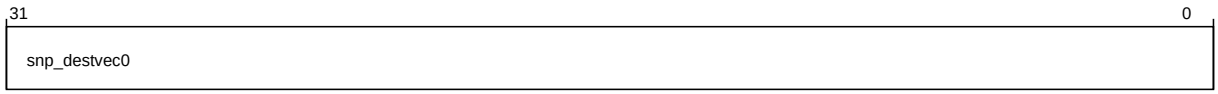
The following table shows the por_dn_vmf12_rnf0 higher register bit assignments.

Table 5-223: por_dn_por_dn_vmf12_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-210: por_dn_por_dn_vmf12_rnf0 (low)



The following table shows the por_dn_vmf12_rnf0 lower register bit assignments.

Table 5-224: por_dn_por_dn_vmf12_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

5.3.2.57 por_dn_vmf12_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

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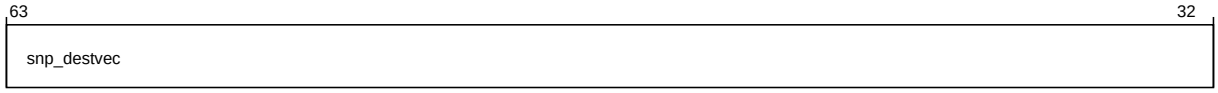
Figure 5-211: por_dn_por_dn_vmf12_rnd (high)



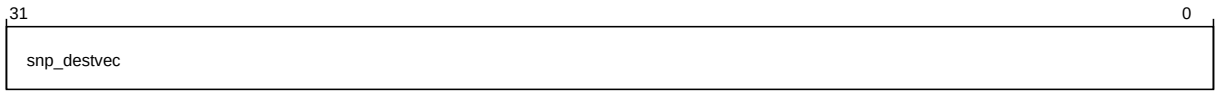
The following table shows the por_dn_vmf12_rnd higher register bit assignments.

Table 5-225: por_dn_por_dn_vmf12_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-212: por_dn_por_dn_vmf12_rnd (low)



The following table shows the por_dn_vmf12_rnd lower register bit assignments.

Table 5-226: por_dn_por_dn_vmf12_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

5.3.2.58 por_dn_vmf12_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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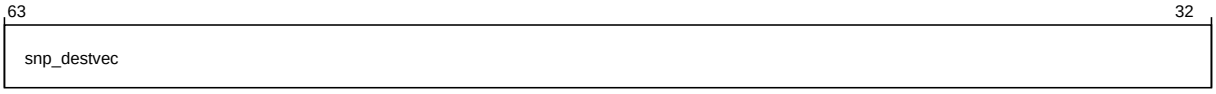
The following figure shows the higher register bit assignments.

Figure 5-213: por_dn_por_dn_vmf12_cxra (high)



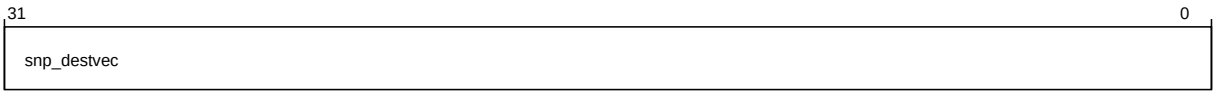
The following table shows the por_dn_vmf12_cxra higher register bit assignments.

Table 5-227: por_dn_por_dn_vmf12_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-214: por_dn_por_dn_vmf12_cxra (low)



The following table shows the por_dn_vmf12_cxra lower register bit assignments.

Table 5-228: por_dn_por_dn_vmf12_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

5.3.2.59 por_dn_vmf13_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDA0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

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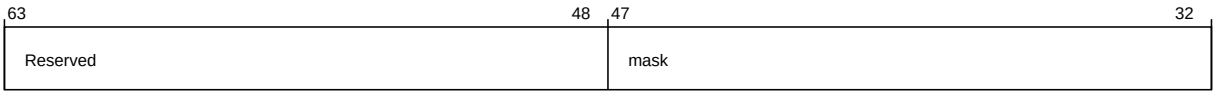
The following figure shows the higher register bit assignments.

Figure 5-215: por_dn_por_dn_vmf13_ctrl (high)



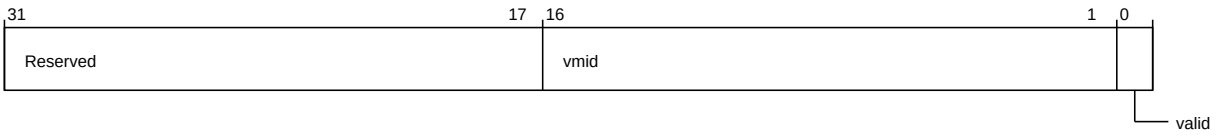
The following table shows the por_dn_vmf13_ctrl higher register bit assignments.

Table 5-229: por_dn_por_dn_vmf13_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf13_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-216: por_dn_por_dn_vmf13_ctrl (low)



The following table shows the por_dn_vmf13_ctrl lower register bit assignments.

Table 5-230: por_dn_por_dn_vmf13_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000

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Bits	Field name	Description	Type	Reset
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.60 por_dn_vmf13_rnf0

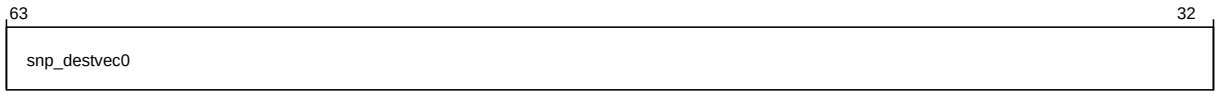
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-217: por_dn_por_dn_vmf13_rnf0 (high)



The following table shows the por_dn_vmf13_rnf0 higher register bit assignments.

Table 5-231: por_dn_por_dn_vmf13_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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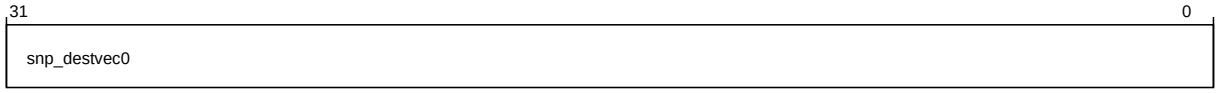
Figure 5-218: por_dn_por_dn_vmf13_rnf0 (low)



The following table shows the por_dn_vmf13_rnf0 lower register bit assignments.

Table 5-232: por_dn_por_dn_vmf13_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

5.3.2.61 por_dn_vmf13_rnd

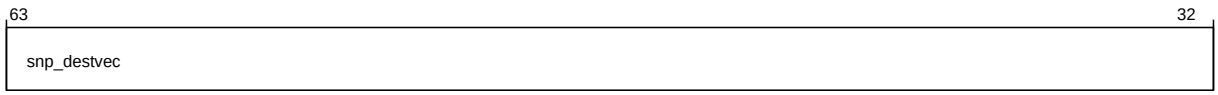
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-219: por_dn_por_dn_vmf13_rnd (high)



The following table shows the por_dn_vmf13_rnd higher register bit assignments.

Table 5-233: por_dn_por_dn_vmf13_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

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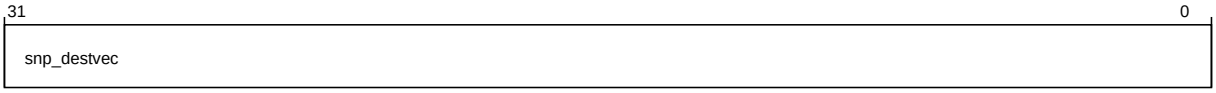
Figure 5-220: por_dn_por_dn_vmf13_rnd (low)



The following table shows the por_dn_vmf13_rnd lower register bit assignments.

Table 5-234: por_dn_por_dn_vmf13_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

5.3.2.62 por_dn_vmf13_cxra

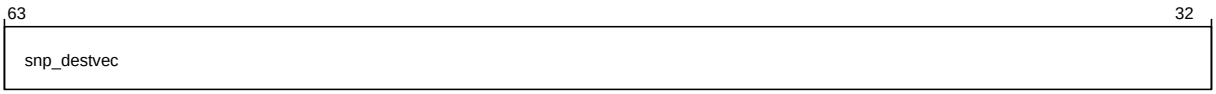
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-221: por_dn_por_dn_vmf13_cxra (high)



The following table shows the por_dn_vmf13_cxra higher register bit assignments.

Table 5-235: por_dn_por_dn_vmf13_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

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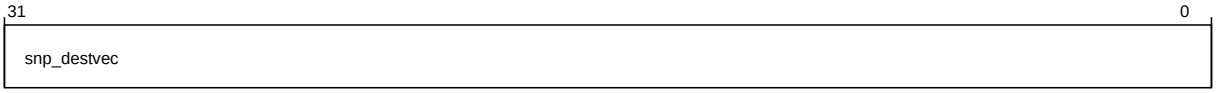
The following figure shows the lower register bit assignments.

Figure 5-222: por_dn_por_dn_vmf13_cxra (low)



The following table shows the por_dn_vmf13_cxra lower register bit assignments.

Table 5-236: por_dn_por_dn_vmf13_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

5.3.2.63 por_dn_vmf14_ctrl

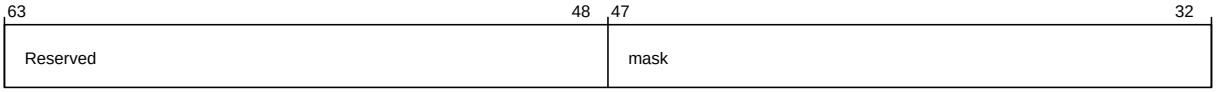
Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDC0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-223: por_dn_por_dn_vmf14_ctrl (high)



The following table shows the por_dn_vmf14_ctrl higher register bit assignments.

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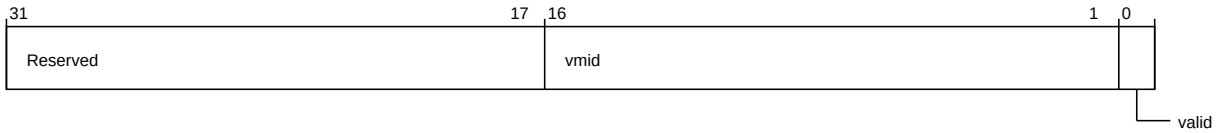
Table 5-237: por_dn_por_dn_vmf14_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf14_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-224: por_dn_por_dn_vmf14_ctrl (low)



The following table shows the por_dn_vmf14_ctrl lower register bit assignments.

Table 5-238: por_dn_por_dn_vmf14_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.64 por_dn_vmf14_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64

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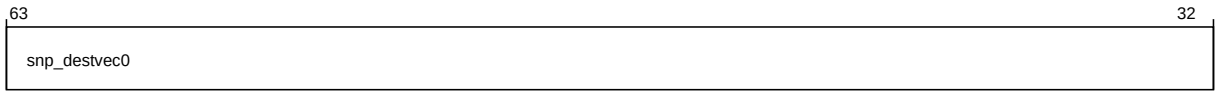
Address offset 16'hDC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-225: por_dn_por_dn_vmf14_rnf0 (high)



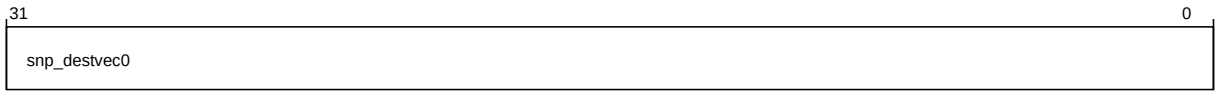
The following table shows the por_dn_vmf14_rnf0 higher register bit assignments.

Table 5-239: por_dn_por_dn_vmf14_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-226: por_dn_por_dn_vmf14_rnf0 (low)



The following table shows the por_dn_vmf14_rnf0 lower register bit assignments.

Table 5-240: por_dn_por_dn_vmf14_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

5.3.2.65 por_dn_vmf14_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

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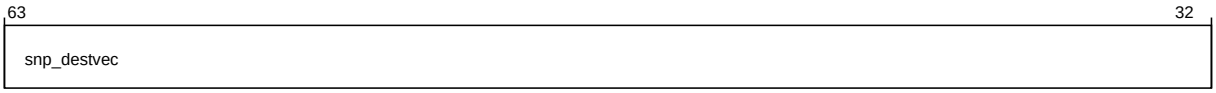
Register width (Bits) 64
Address offset 16'hDD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-227: por_dn_por_dn_vmf14_rnd (high)



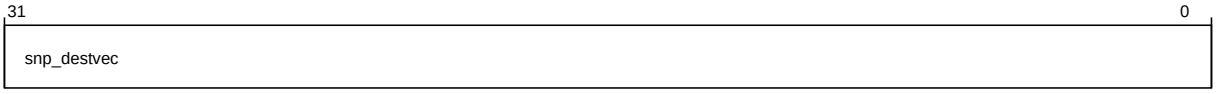
The following table shows the por_dn_vmf14_rnd higher register bit assignments.

Table 5-241: por_dn_por_dn_vmf14_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-228: por_dn_por_dn_vmf14_rnd (low)



The following table shows the por_dn_vmf14_rnd lower register bit assignments.

Table 5-242: por_dn_por_dn_vmf14_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

5.3.2.66 por_dn_vmf14_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

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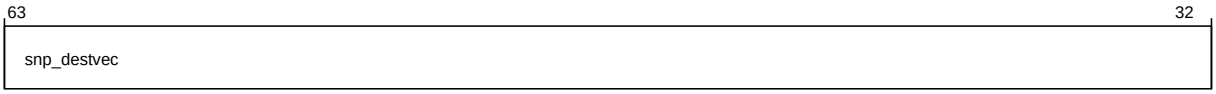
Type RW
Register width (Bits) 64
Address offset 16'hDD8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-229: por_dn_por_dn_vmf14_cxra (high)



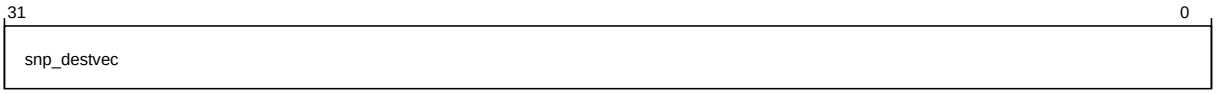
The following table shows the por_dn_vmf14_cxra higher register bit assignments.

Table 5-243: por_dn_por_dn_vmf14_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-230: por_dn_por_dn_vmf14_cxra (low)



The following table shows the por_dn_vmf14_cxra lower register bit assignments.

Table 5-244: por_dn_por_dn_vmf14_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

5.3.2.67 por_dn_vmf15_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

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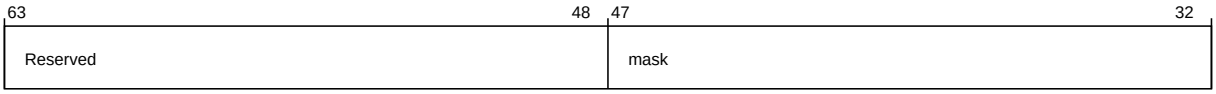
Type RW
Register width (Bits) 64
Address offset 16'hDE0
Register reset 64'b1111111111111111000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-231: por_dn_por_dn_vmf15_ctrl (high)



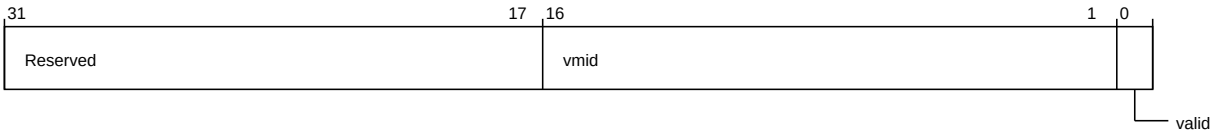
The following table shows the por_dn_vmf15_ctrl higher register bit assignments.

Table 5-245: por_dn_por_dn_vmf15_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf15_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following figure shows the lower register bit assignments.

Figure 5-232: por_dn_por_dn_vmf15_ctrl (low)



The following table shows the por_dn_vmf15_ctrl lower register bit assignments.

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Table 5-246: por_dn_por_dn_vmf15_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

5.3.2.68 por_dn_vmf15_rnf0

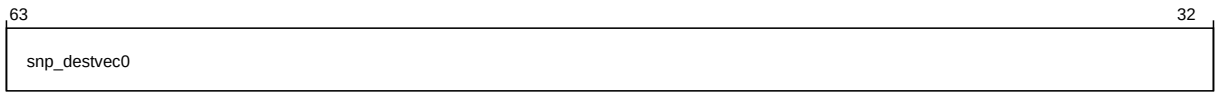
Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-233: por_dn_por_dn_vmf15_rnf0 (high)



The following table shows the por_dn_vmf15_rnf0 higher register bit assignments.

Table 5-247: por_dn_por_dn_vmf15_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

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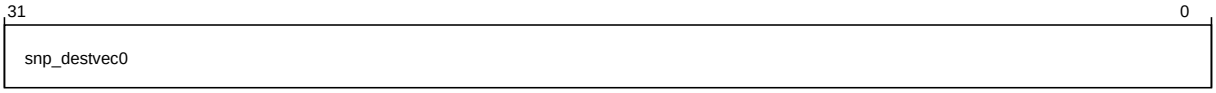
The following figure shows the lower register bit assignments.

Figure 5-234: por_dn_por_dn_vmf15_rnf0 (low)



The following table shows the por_dn_vmf15_rnf0 lower register bit assignments.

Table 5-248: por_dn_por_dn_vmf15_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

5.3.2.69 por_dn_vmf15_rnd

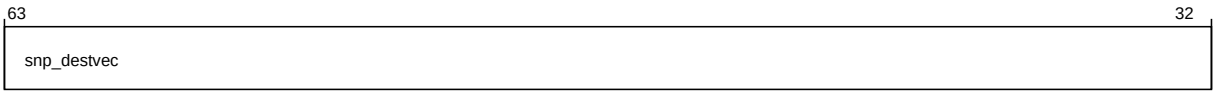
Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDF0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-235: por_dn_por_dn_vmf15_rnd (high)



The following table shows the por_dn_vmf15_rnd higher register bit assignments.

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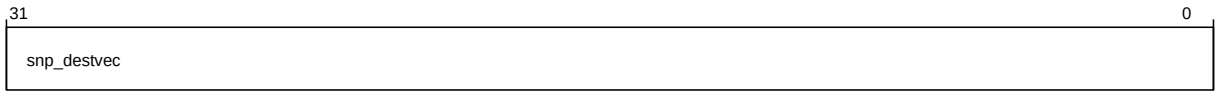
Table 5-249: por_dn_por_dn_vmf15_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-236: por_dn_por_dn_vmf15_rnd (low)



The following table shows the por_dn_vmf15_rnd lower register bit assignments.

Table 5-250: por_dn_por_dn_vmf15_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

5.3.2.70 por_dn_vmf15_cxra

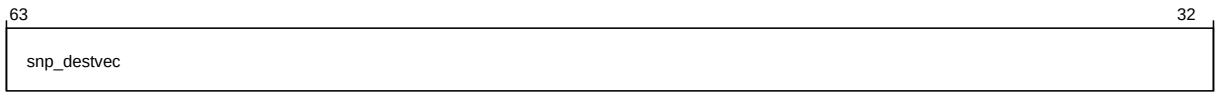
Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CI-700 system. Does not have any effect.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDF8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_dn_secure_register_groups_override.vmf

The following figure shows the higher register bit assignments.

Figure 5-237: por_dn_por_dn_vmf15_cxra (high)



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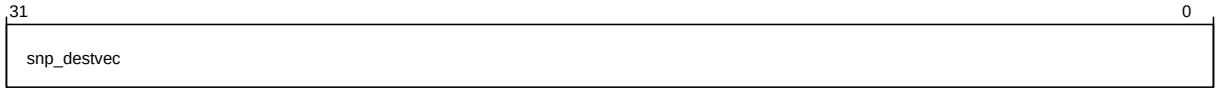
The following table shows the por_dn_vmf15_cxra higher register bit assignments.

Table 5-251: por_dn_por_dn_vmf15_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-238: por_dn_por_dn_vmf15_cxra (low)



The following table shows the por_dn_vmf15_cxra lower register bit assignments.

Table 5-252: por_dn_por_dn_vmf15_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

5.3.2.71 por_dn_pmu_event_sel

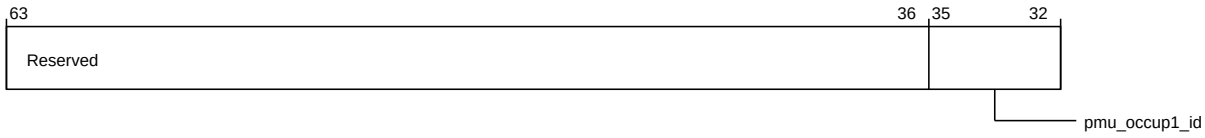
Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-239: por_dn_por_dn_pmu_event_sel (high)



The following table shows the por_dn_pmu_event_sel higher register bit assignments.

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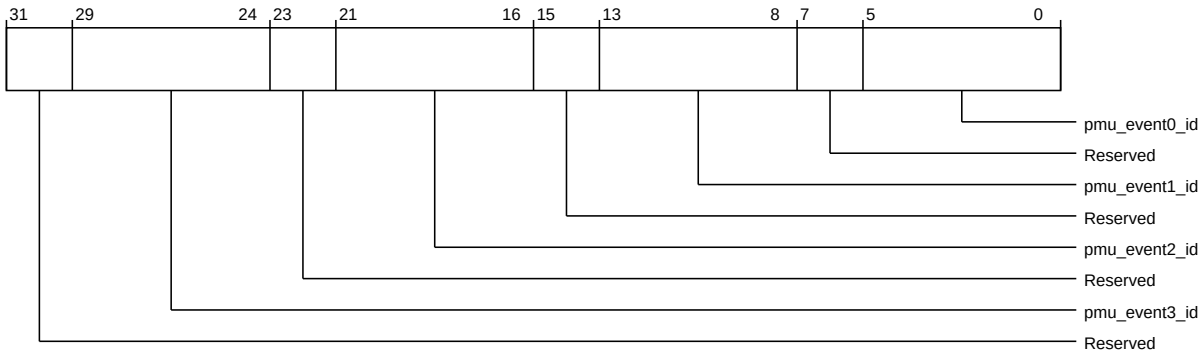
Table 5-253: por_dn_por_dn_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	PMU occupancy event selector ID 4'b0000: All 4'b0001: DVM ops 4'b0010: DVM syncs	RW	4'b0

The following figure shows the lower register bit assignments.

Figure 5-240: por_dn_por_dn_pmu_event_sel (low)



The following table shows the por_dn_pmu_event_sel lower register bit assignments.

Table 5-254: por_dn_por_dn_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	PMU Event 0 ID 6'h00: No event 6'h01: Number of TLBI DVM op requests 6'h02: Number of BPI DVM op requests 6'h03: Number of PICI DVM op requests 6'h04: Number of VICI DVM op requests 6'h05: Number of DVM sync requests 6'h06: Number of DVM op requests that were filtered using VMID filtering 6'h07: Number of DVM op requests to RNDs, BPI or PICI/VICI, that were filtered 6'h08: Number of retried REQ 6'h09: Number of SNPs sent to RNs 6'h0a: Number of SNPs stalled to RNs due to lack of Crds 6'h0b: DVM tracker full counter 6'h0c: DVM tracker occupancy counter	RW	5'b0

5.3.3 Debug and trace register descriptions

This section lists the debug and trace registers.

5.3.3.1 por_dt_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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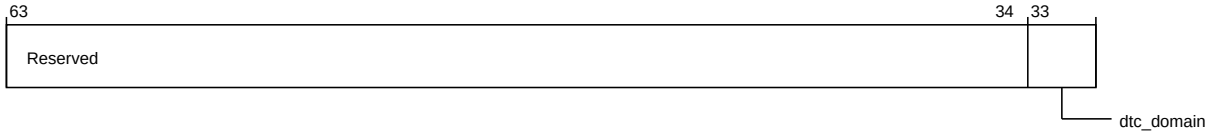
Figure 5-241: por_dt_por_dt_node_info (high)



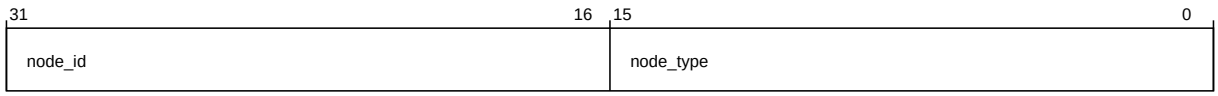
The following table shows the por_dt_node_info higher register bit assignments.

Table 5-255: por_dt_por_dt_node_info (high)

Bits	Field name	Description	Type	Reset
63:34	Reserved	Reserved	RO	-
33:32	dtc_domain	DTC domain number	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-242: por_dt_por_dt_node_info (low)



The following table shows the por_dt_node_info lower register bit assignments.

Table 5-256: por_dt_por_dt_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h3

5.3.3.2 por_dt_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

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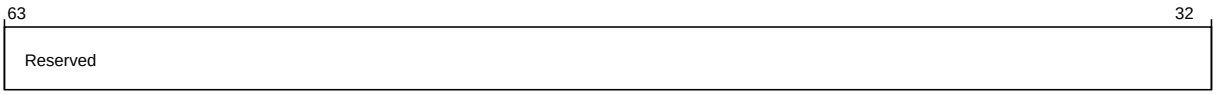
The following figure shows the higher register bit assignments.

Figure 5-243: por_dt_por_dt_child_info (high)



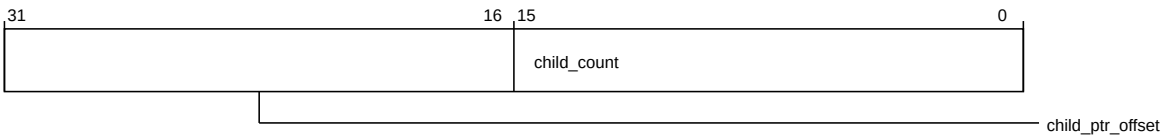
The following table shows the por_dt_child_info higher register bit assignments.

Table 5-257: por_dt_por_dt_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-244: por_dt_por_dt_child_info (low)



The following table shows the por_dt_child_info lower register bit assignments.

Table 5-258: por_dt_por_dt_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0000
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.3.3 por_dt_secure_access

Functions as the Secure access control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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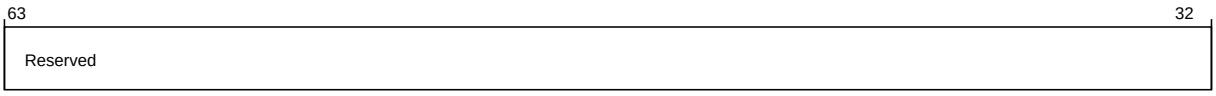
The following figure shows the higher register bit assignments.

Figure 5-245: por_dt_por_dt_secure_access (high)



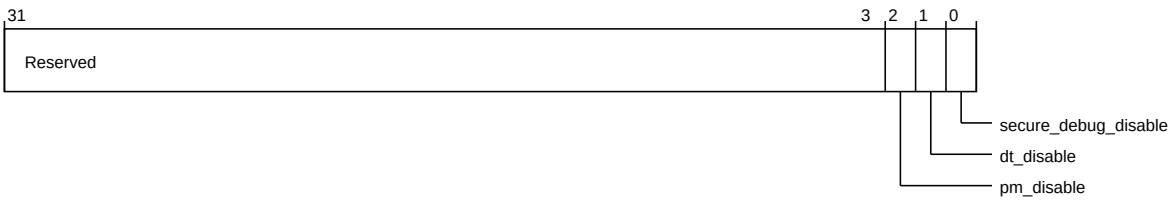
The following table shows the por_dt_secure_access higher register bit assignments.

Table 5-259: por_dt_por_dt_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-246: por_dt_por_dt_secure_access (low)



The following table shows the por_dt_secure_access lower register bit assignments.

Table 5-260: por_dt_por_dt_secure_access (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	pm_disable	PMU disable 1'b0: PMU function is not affected 1'b1: PMU function is disabled.	RW	1'b0
1	dt_disable	Debug disable 1'b0: DT function is not affected 1'b1: DT function is disabled.	RW	1'b0
0	secure_debug_disable	Secure debug disable 1'b0: Secure events are monitored by the PMU 1'b1: Secure events are only monitored by the PMU if SPNIDEN is set to 1	RW	1'b0

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5.3.3.4 por_dt_dtc_ctl

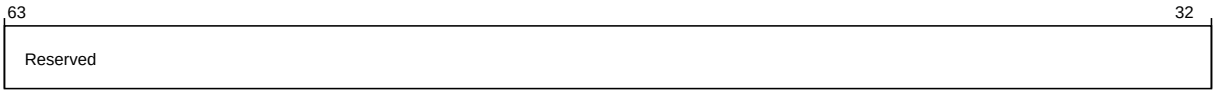
Functions as the debug trace control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-247: por_dt_por_dt_dtc_ctl (high)



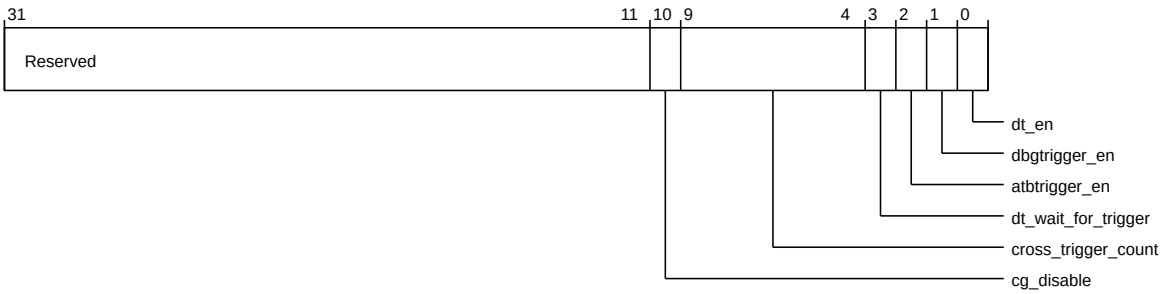
The following table shows the por_dt_dtc_ctl higher register bit assignments.

Table 5-261: por_dt_por_dt_dtc_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-248: por_dt_por_dt_dtc_ctl (low)



The following table shows the por_dt_dtc_ctl lower register bit assignments.

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Table 5-262: por_dt_por_dt_dtc_ctl (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	cg_disable	Disables DT architectural clock gates	RW	1'b0
9:4	cross_trigger_count	Number of cross triggers received before trace enable NOTE: Only applicable if dt_wait_for_trigger is set to 1.	RW	6'b0
3	dt_wait_for_trigger	Enables waiting for cross trigger before trace enable	RW	1'b0
2	atbtrigger_en	ATB trigger enable	RW	1'b0
1	dbgtrigger_en	DBGWATCHTRIG enable	RW	1'b0
0	dt_en	Enables debug, trace, and PMU features	RW	1'b0

5.3.3.5 por_dt_trigger_status

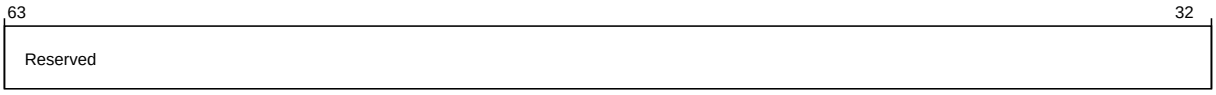
Provides the trigger status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hA10
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-249: por_dt_por_dt_trigger_status (high)



The following table shows the por_dt_trigger_status higher register bit assignments.

Table 5-263: por_dt_por_dt_trigger_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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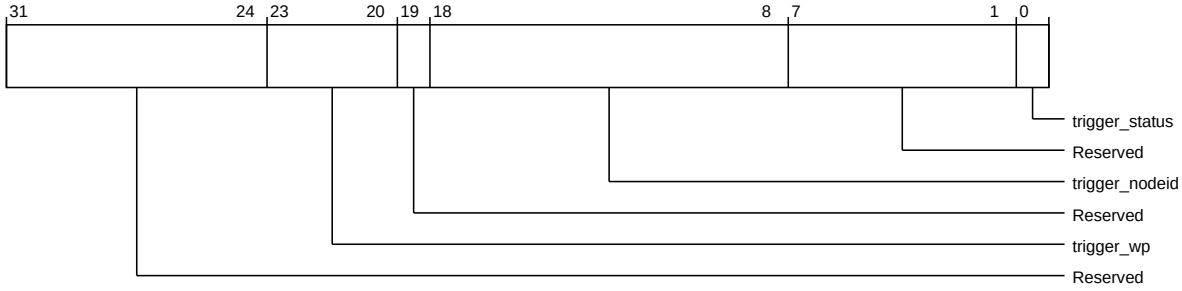
Figure 5-250: por_dt_por_dt_trigger_status (low)



The following table shows the por_dt_trigger_status lower register bit assignments.

Table 5-264: por_dt_por_dt_trigger_status (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	trigger_wp	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by watchpoint	RO	1'h0
19	Reserved	Reserved	RO	-
18:8	trigger_nodeid	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by node ID	RO	11'h0
7:1	Reserved	Reserved	RO	-
0	trigger_status	Indicates DBGWATCHTRIGREQ assertion and/or ATB trigger	RO	1'h0

5.3.3.6 por_dt_trigger_status_clr

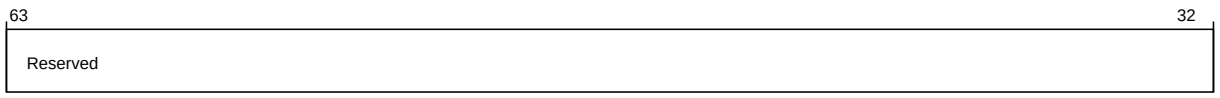
Clears the trigger status.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'hA20
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-251: por_dt_por_dt_trigger_status_clr (high)



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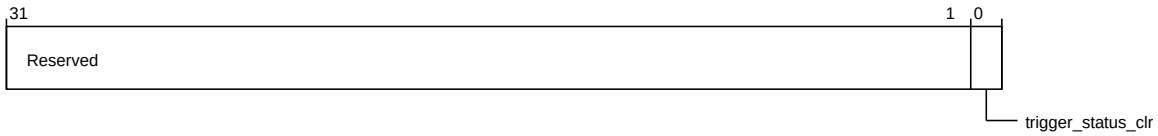
The following table shows the por_dt_trigger_status_clr higher register bit assignments.

Table 5-265: por_dt_por_dt_trigger_status_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-252: por_dt_por_dt_trigger_status_clr (low)



The following table shows the por_dt_trigger_status_clr lower register bit assignments.

Table 5-266: por_dt_por_dt_trigger_status_clr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	trigger_status_clr	Write a 1 to clear por_dt_trigger_status.trigger_status	WO	1'b0

5.3.3.7 por_dt_trace_control

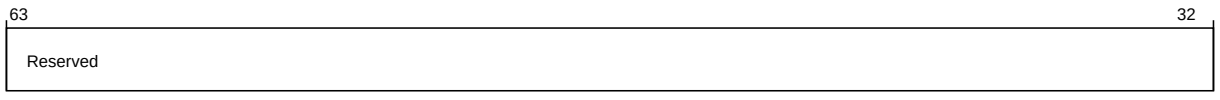
Functions as the trace control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA30
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-253: por_dt_por_dt_trace_control (high)



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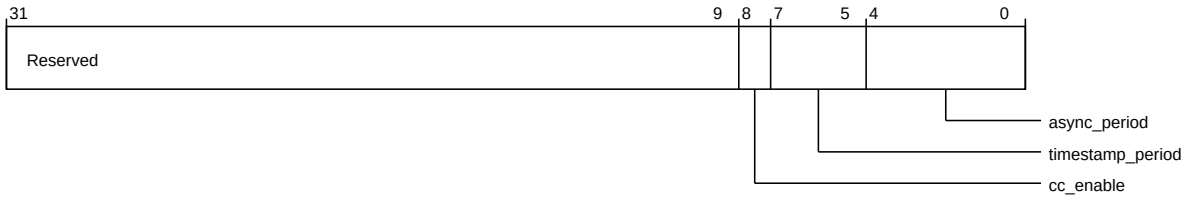
The following table shows the por_dt_trace_control higher register bit assignments.

Table 5-267: por_dt_por_dt_trace_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-254: por_dt_por_dt_trace_control (low)



The following table shows the por_dt_trace_control lower register bit assignments.

Table 5-268: por_dt_por_dt_trace_control (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	cc_enable	Cycle count enable	RW	1'b0
7:5	timestamp_period	Time stamp packet insertion period 3'b000: Time stamp disabled 3'b011: Time stamp every 8K clock cycles 3'b100: Time stamp every 16K clock cycles 3'b101: Time stamp every 32K clock cycles 3'b110: Time stamp every 64K clock cycles	RW	3'b0
4:0	async_period	Alignment sync packet insertion period 5'h00: Alignment sync disabled 5'h08: Alignment sync inserted after 256B of trace 5'h09: Alignment sync inserted after 512B of trace 5'h14: Alignment sync inserted after 1048576B of trace NOTE: All other values are reserved.	RW	5'b0

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5.3.3.8 por_dt_traceid

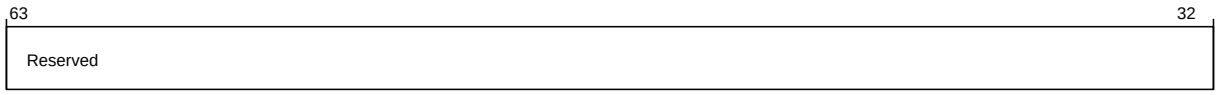
Contains the ATB ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA48
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-255: por_dt_por_dt_traceid (high)



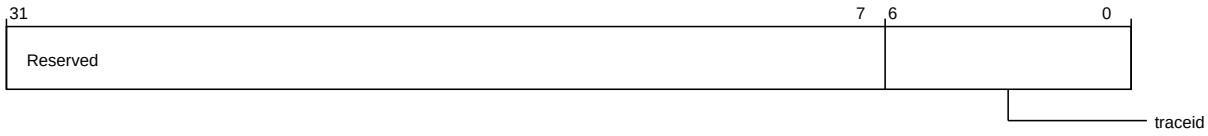
The following table shows the por_dt_traceid higher register bit assignments.

Table 5-269: por_dt_por_dt_traceid (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-256: por_dt_por_dt_traceid (low)



The following table shows the por_dt_traceid lower register bit assignments.

Table 5-270: por_dt_por_dt_traceid (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6:0	traceid	ATB ID	RW	7'h0

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5.3.3.9 por_dt_pmevcntAB

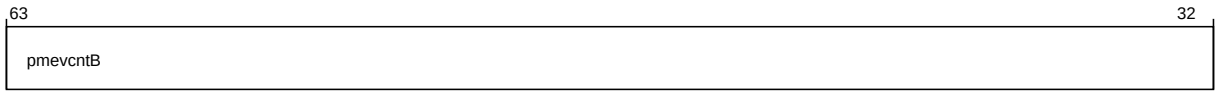
Contains the PMU event counters A and B.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-257: por_dt_por_dt_pmevcntab (high)



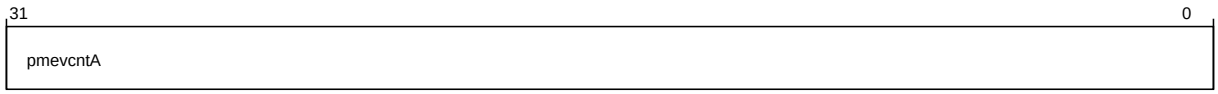
The following table shows the por_dt_pmevcntAB higher register bit assignments.

Table 5-271: por_dt_por_dt_pmevcntab (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntB	PMU counter B	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-258: por_dt_por_dt_pmevcntab (low)



The following table shows the por_dt_pmevcntAB lower register bit assignments.

Table 5-272: por_dt_por_dt_pmevcntab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntA	PMU counter A	RW	32'h0000

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5.3.3.10 por_dt_pmevcntCD

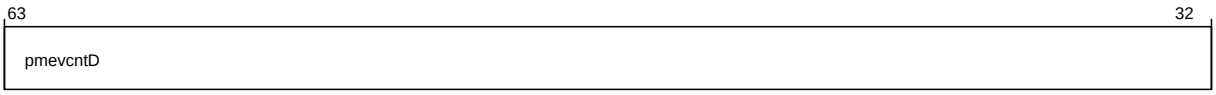
Contains the PMU event counters C and D.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2010
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-259: por_dt_por_dt_pmevcntcd (high)



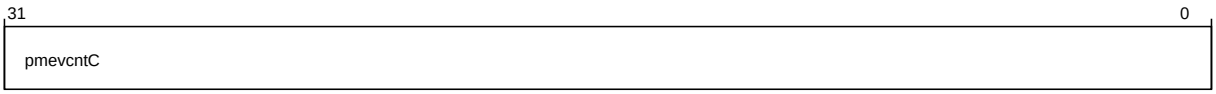
The following table shows the por_dt_pmevcntCD higher register bit assignments.

Table 5-273: por_dt_por_dt_pmevcntcd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntD	PMU counter D	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-260: por_dt_por_dt_pmevcntcd (low)



The following table shows the por_dt_pmevcntCD lower register bit assignments.

Table 5-274: por_dt_por_dt_pmevcntcd (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntC	PMU counter C	RW	32'h0000

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5.3.3.11 por_dt_pmevcntEF

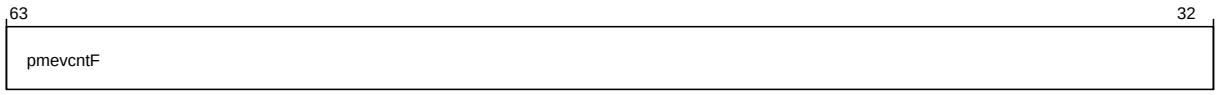
Contains the PMU event counters E and F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2020
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-261: por_dt_por_dt_pmevcntef (high)



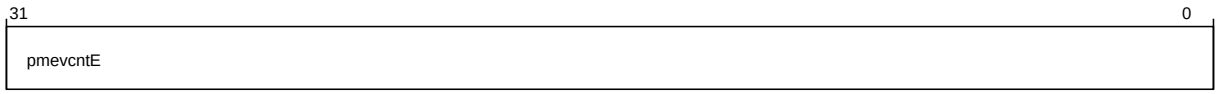
The following table shows the por_dt_pmevcntEF higher register bit assignments.

Table 5-275: por_dt_por_dt_pmevcntef (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntF	PMU counter F	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-262: por_dt_por_dt_pmevcntef (low)



The following table shows the por_dt_pmevcntEF lower register bit assignments.

Table 5-276: por_dt_por_dt_pmevcntef (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntE	PMU counter E	RW	32'h0000

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5.3.3.12 por_dt_pmevcntGH

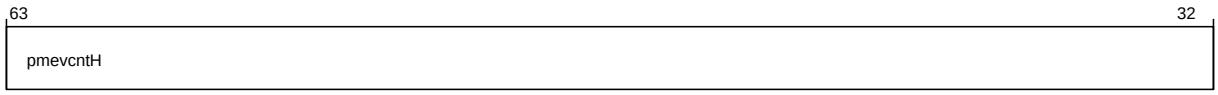
Contains the PMU event counters G and H.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2030
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-263: por_dt_por_dt_pmevcntgh (high)



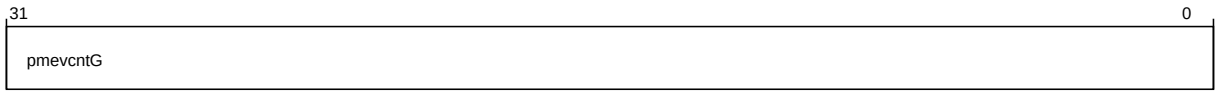
The following table shows the por_dt_pmevcntGH higher register bit assignments.

Table 5-277: por_dt_por_dt_pmevcntgh (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntH	PMU counter H	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-264: por_dt_por_dt_pmevcntgh (low)



The following table shows the por_dt_pmevcntGH lower register bit assignments.

Table 5-278: por_dt_por_dt_pmevcntgh (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntG	PMU counter G	RW	32'h0000

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5.3.3.13 por_dt_pmccntr

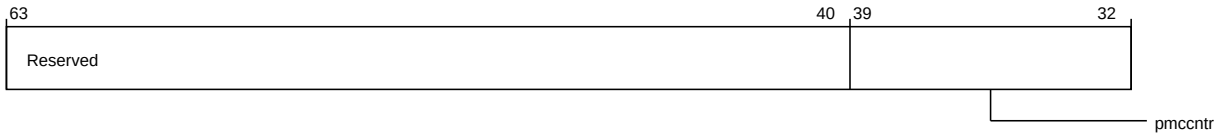
Contains the PMU cycle counter.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2040
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-265: por_dt_por_dt_pmccntr (high)



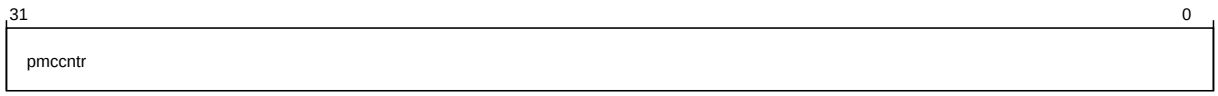
The following table shows the por_dt_pmccntr higher register bit assignments.

Table 5-279: por_dt_por_dt_pmccntr (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pmccntr	PMU cycle counter	RW	40'h0

The following figure shows the lower register bit assignments.

Figure 5-266: por_dt_por_dt_pmccntr (low)



The following table shows the por_dt_pmccntr lower register bit assignments.

Table 5-280: por_dt_por_dt_pmccntr (low)

Bits	Field name	Description	Type	Reset
31:0	pmccntr	PMU cycle counter	RW	40'h0

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5.3.3.14 por_dt_pmevcntsrAB

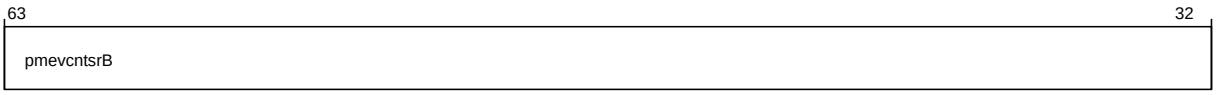
Contains the PMU event counter shadow registers A and B.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2050
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-267: por_dt_por_dt_pmevcntsrab (high)



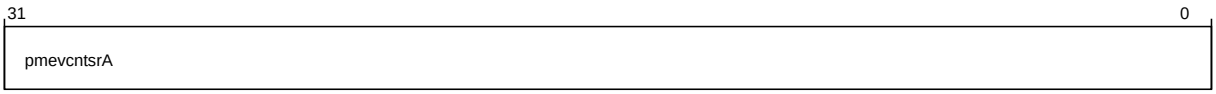
The following table shows the por_dt_pmevcntsrAB higher register bit assignments.

Table 5-281: por_dt_por_dt_pmevcntsrab (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrB	PMU counter B shadow register	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-268: por_dt_por_dt_pmevcntsrab (low)



The following table shows the por_dt_pmevcntsrAB lower register bit assignments.

Table 5-282: por_dt_por_dt_pmevcntsrab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrA	PMU counter A shadow register	RW	32'h0000

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5.3.3.15 por_dt_pmevcntsrCD

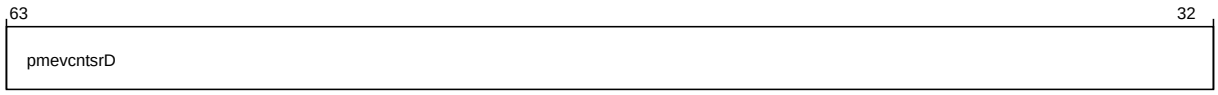
Contains the PMU event counter shadow registers C and D.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2060
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-269: por_dt_por_dt_pmevcntsrcd (high)



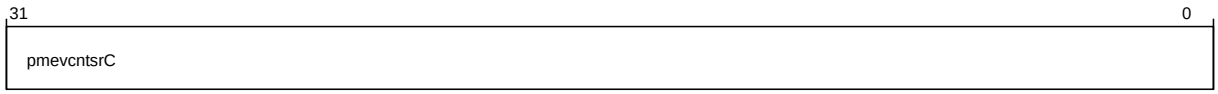
The following table shows the por_dt_pmevcntsrCD higher register bit assignments.

Table 5-283: por_dt_por_dt_pmevcntsrcd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrD	PMU counter D shadow register	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-270: por_dt_por_dt_pmevcntsrcd (low)



The following table shows the por_dt_pmevcntsrCD lower register bit assignments.

Table 5-284: por_dt_por_dt_pmevcntsrcd (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrC	PMU counter C shadow register	RW	32'h0000

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5.3.3.16 por_dt_pmevcntsrEF

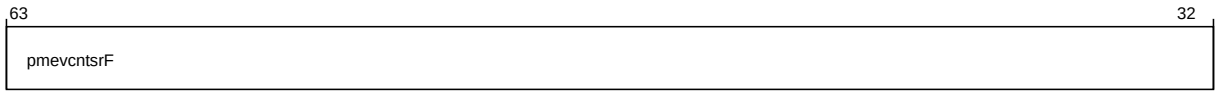
Contains the PMU event counter shadow registers E and F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2070
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-271: por_dt_por_dt_pmevcntsref (high)



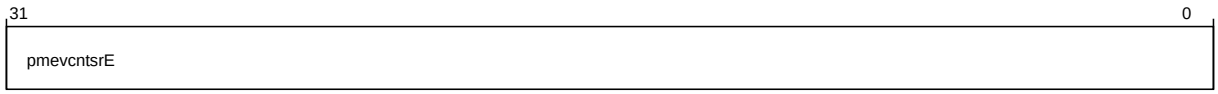
The following table shows the por_dt_pmevcntsrEF higher register bit assignments.

Table 5-285: por_dt_por_dt_pmevcntsref (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrF	PMU counter F shadow register	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-272: por_dt_por_dt_pmevcntsref (low)



The following table shows the por_dt_pmevcntsrEF lower register bit assignments.

Table 5-286: por_dt_por_dt_pmevcntsref (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrE	PMU counter E shadow register	RW	32'h0000

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5.3.3.17 por_dt_pmevcntsrGH

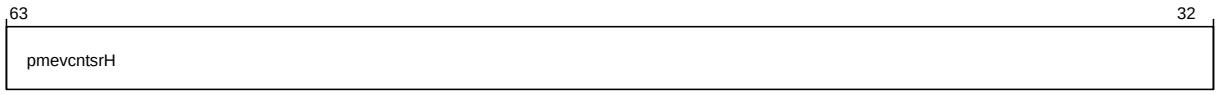
Contains the PMU event counter shadow registers G and H.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2080
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-273: por_dt_por_dt_pmevcntsrgh (high)



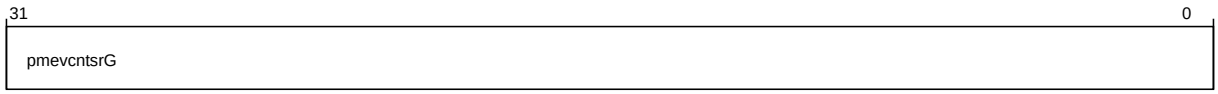
The following table shows the por_dt_pmevcntsrGH higher register bit assignments.

Table 5-287: por_dt_por_dt_pmevcntsrgh (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrH	PMU counter H shadow register	RW	32'h0000

The following figure shows the lower register bit assignments.

Figure 5-274: por_dt_por_dt_pmevcntsrgh (low)



The following table shows the por_dt_pmevcntsrGH lower register bit assignments.

Table 5-288: por_dt_por_dt_pmevcntsrgh (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrG	PMU counter G shadow register	RW	32'h0000

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5.3.3.18 por_dt_pmccntrsr

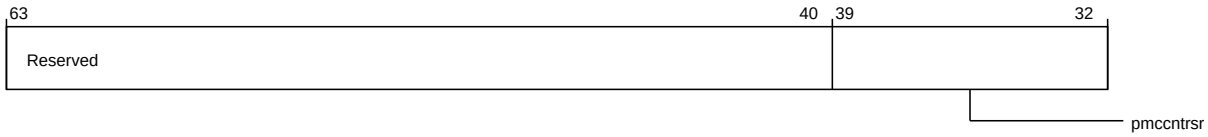
Contains the PMU cycle counter shadow register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2090
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-275: por_dt_por_dt_pmccntrsr (high)



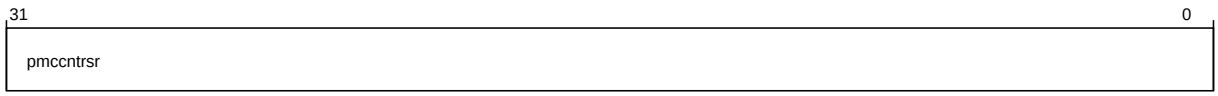
The following table shows the por_dt_pmccntrsr higher register bit assignments.

Table 5-289: por_dt_por_dt_pmccntrsr (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

The following figure shows the lower register bit assignments.

Figure 5-276: por_dt_por_dt_pmccntrsr (low)



The following table shows the por_dt_pmccntrsr lower register bit assignments.

Table 5-290: por_dt_por_dt_pmccntrsr (low)

Bits	Field name	Description	Type	Reset
31:0	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

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5.3.3.19 por_dt_pmcr

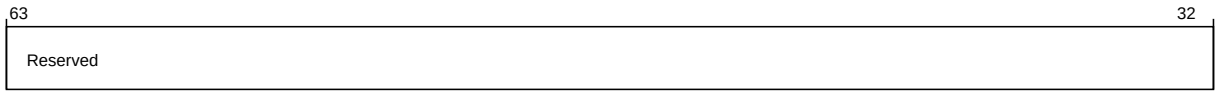
Functions as the PMU control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-277: por_dt_por_dt_pmcr (high)



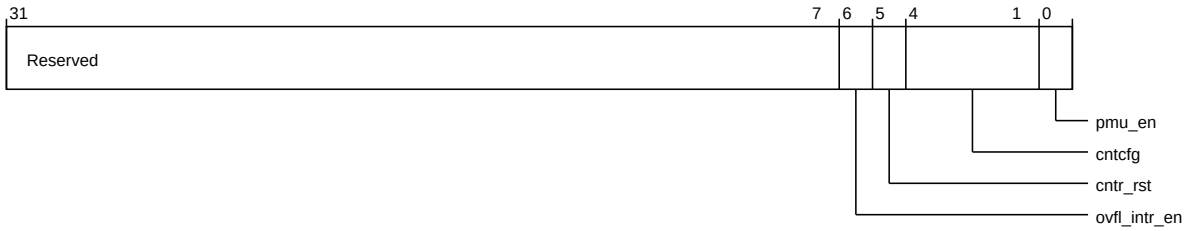
The following table shows the por_dt_pmcr higher register bit assignments.

Table 5-291: por_dt_por_dt_pmcr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-278: por_dt_por_dt_pmcr (low)



The following table shows the por_dt_pmcr lower register bit assignments.

Table 5-292: por_dt_por_dt_pmcr (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
6	ovfl_intr_en	Enables INTREQPMU assertion on PMU counter overflow	RW	1'h0
5	cntr_rst	Enables clearing of live counters upon assertion of por_dt_pmsrr.ss_req or PMUSNAPSHOTREQ	RW	1'h0
4:1	cntcfg	Groups adjacent 32-bit registers into a 64-bit register	RW	4'h0
0	pmu_en	Enables PMU features	RW	1'b0

5.3.3.20 por_dt_pmovsr

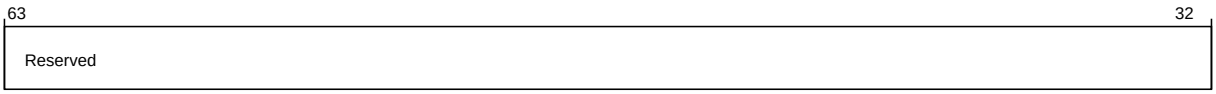
Provides the PMU overflow status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-279: por_dt_por_dt_pmovsr (high)



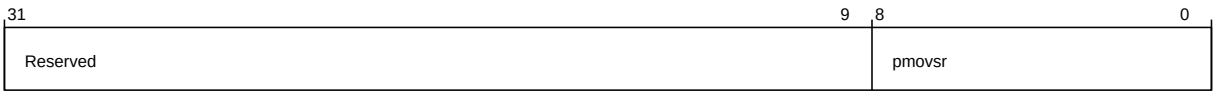
The following table shows the por_dt_pmovsr higher register bit assignments.

Table 5-293: por_dt_por_dt_pmovsr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-280: por_dt_por_dt_pmovsr (low)



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The following table shows the por_dt_pmovsr lower register bit assignments.

Table 5-294: por_dt_por_dt_pmovsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr	PMU overflow status Bit 8: Indicates overflow from cycle counter Bits [7:0]: Indicates overflow from counters 7 to 0	RO	9'h0

5.3.3.21 por_dt_pmovsr_clr

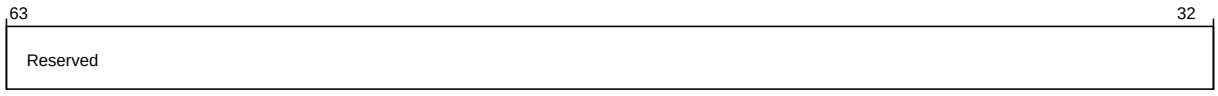
Clears the PMU overflow status.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'h2120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-281: por_dt_por_dt_pmovsr_clr (high)



The following table shows the por_dt_pmovsr_clr higher register bit assignments.

Table 5-295: por_dt_por_dt_pmovsr_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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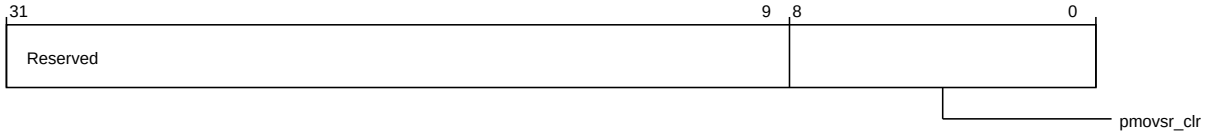
Figure 5-282: por_dt_por_dt_pmovsr_clr (low)



The following table shows the por_dt_pmovsr_clr lower register bit assignments.

Table 5-296: por_dt_por_dt_pmovsr_clr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr_clr	Write a 1 to clear the corresponding bit in por_dt_pmovsr.pmovsr	WO	9'b0

5.3.3.22 por_dt_pmssr

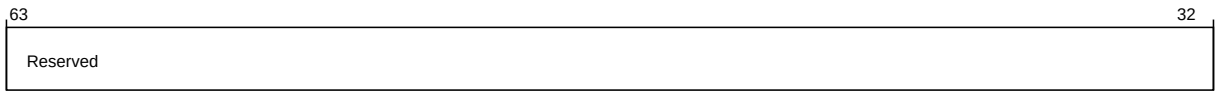
Provides the PMU snapshot status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-283: por_dt_por_dt_pmssr (high)



The following table shows the por_dt_pmssr higher register bit assignments.

Table 5-297: por_dt_por_dt_pmssr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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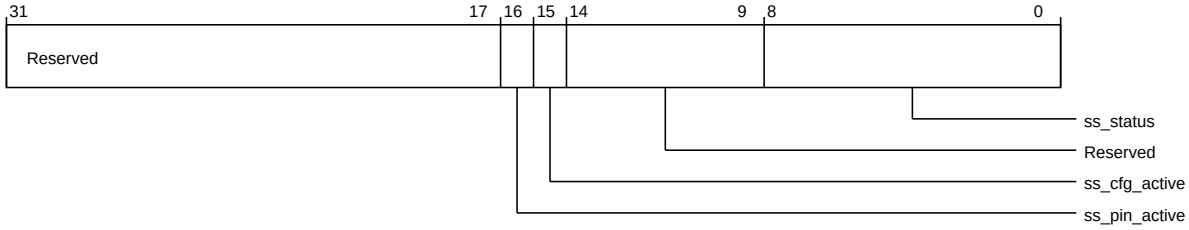
Figure 5-284: por_dt_por_dt_pmssr (low)



The following table shows the por_dt_pmssr lower register bit assignments.

Table 5-298: por_dt_por_dt_pmssr (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	ss_pin_active	Activates PMU snapshot from PMUSNAPSHOTREQ	RO	1'b0
15	ss_cfg_active	PMU snapshot activated from configuration write	RO	1'b0
14:9	Reserved	Reserved	RO	-
8:0	ss_status	PMU snapshot status Bit 8: Indicates snapshot status for cycle counter Bits [7:0]: Indicates snapshot status for counters 7 to 0	RO	9'b0

5.3.3.23 por_dt_pmsrr

Sends PMU snapshot requests.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'h2130
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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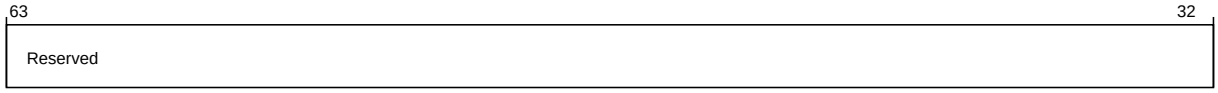
Figure 5-285: por_dt_por_dt_pmsrr (high)



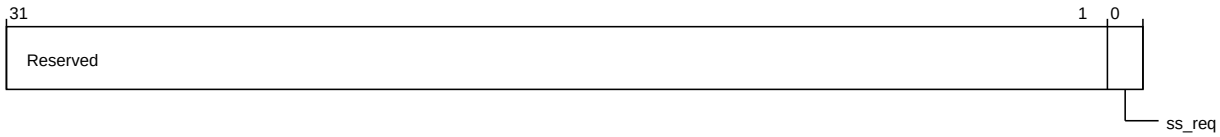
The following table shows the por_dt_pmsrr higher register bit assignments.

Table 5-299: por_dt_por_dt_pmsrr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-286: por_dt_por_dt_pmsrr (low)



The following table shows the por_dt_pmsrr lower register bit assignments.

Table 5-300: por_dt_por_dt_pmsrr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	ss_req	Write a 1 to request PMU snapshot	WO	1'b0

5.3.3.24 por_dt_claim

Functions as the claim tag set register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFA0
Register reset 64'b0111111111111111111111111111111111
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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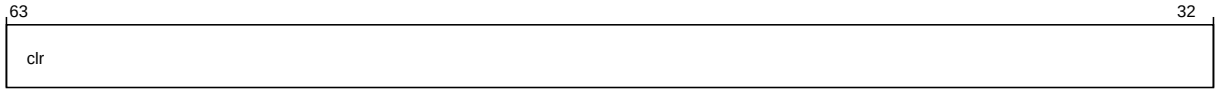
Figure 5-287: por_dt_por_dt_claim (high)



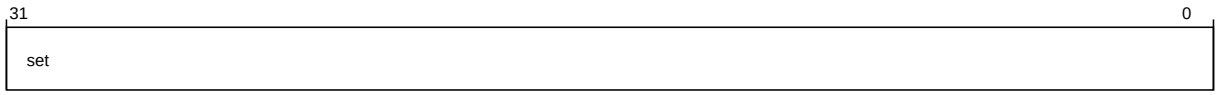
The following table shows the por_dt_claim higher register bit assignments.

Table 5-301: por_dt_por_dt_claim (high)

Bits	Field name	Description	Type	Reset
63:32	clr	Upper half of the claim tag value; enables individual bits to be cleared (write) and returns the current claim tag value (read)	RW	32'b0

The following figure shows the lower register bit assignments.

Figure 5-288: por_dt_por_dt_claim (low)



The following table shows the por_dt_claim lower register bit assignments.

Table 5-302: por_dt_por_dt_claim (low)

Bits	Field name	Description	Type	Reset
31:0	set	Lower half of the claim tag value; allows individual bits to be set (write) and returns the number of bits that can be set (read)	RW	32'hffffffff

5.3.3.25 por_dt_devaff

Functions as the device affinity register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFA8
Register reset 64'b0
Usage constraints There are no usage constraints.

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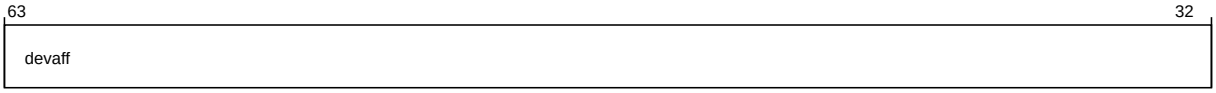
The following figure shows the higher register bit assignments.

Figure 5-289: por_dt_por_dt_devaff (high)



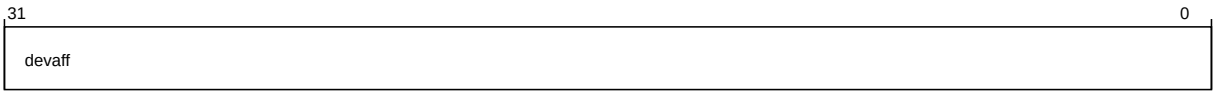
The following table shows the por_dt_devaff higher register bit assignments.

Table 5-303: por_dt_por_dt_devaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-290: por_dt_por_dt_devaff (low)



The following table shows the por_dt_devaff lower register bit assignments.

Table 5-304: por_dt_por_dt_devaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

5.3.3.26 por_dt_lsr

Functions as the lock status register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFB0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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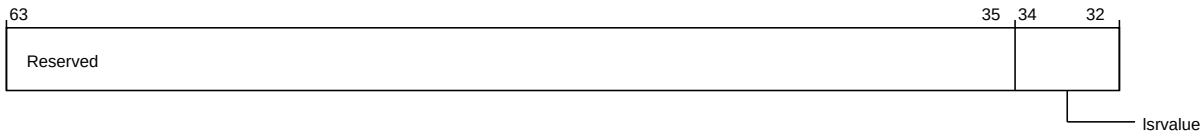
Figure 5-291: por_dt_por_dt_lsr (high)



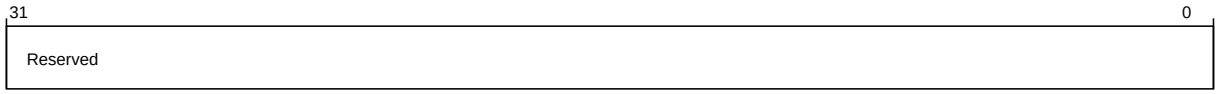
The following table shows the por_dt_lsr higher register bit assignments.

Table 5-305: por_dt_por_dt_lsr (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	lsrvalue	Lock status value	RO	3'b0

The following figure shows the lower register bit assignments.

Figure 5-292: por_dt_por_dt_lsr (low)



The following table shows the por_dt_lsr lower register bit assignments.

Table 5-306: por_dt_por_dt_lsr (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

5.3.3.27 por_dt_authstatus_devarch

Functions as the authentication status register and the device architecture register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFB8
Register reset 64'b01001010
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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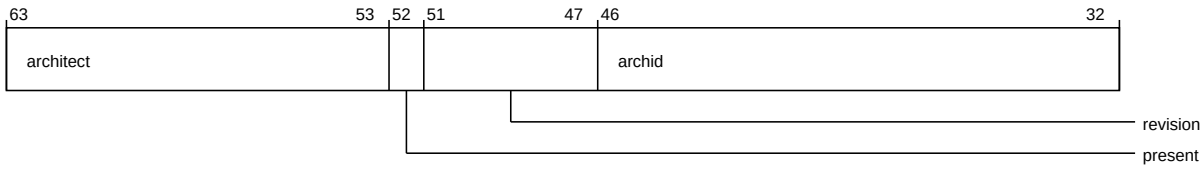
Figure 5-293: por_dt_por_dt_authstatus_devarch (high)



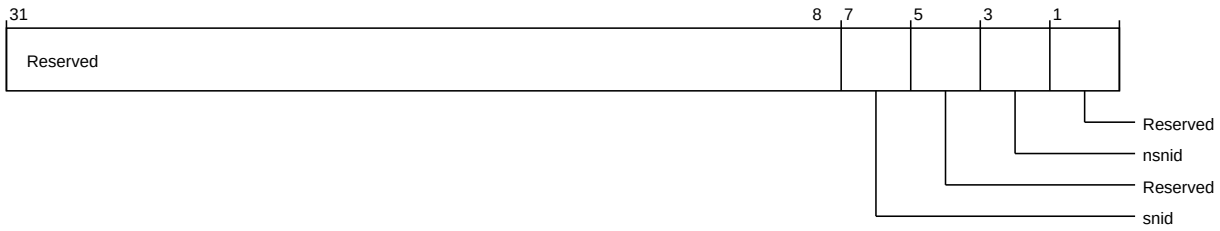
The following table shows the por_dt_authstatus_devarch higher register bit assignments.

Table 5-307: por_dt_por_dt_authstatus_devarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'b0
52	present	Present	RO	1'b1
51:47	revision	Architecture revision	RO	6'b0
46:32	archid	Architecture ID	RO	16'b0

The following figure shows the lower register bit assignments.

Figure 5-294: por_dt_por_dt_authstatus_devarch (low)



The following table shows the por_dt_authstatus_devarch lower register bit assignments.

Table 5-308: por_dt_por_dt_authstatus_devarch (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	snid	Secure non-invasive debug	RO	2'b10
5:4	Reserved	Reserved	RO	-
3:2	nsnid	Non-secure non-invasive debug	RO	2'b10
1:0	Reserved	Reserved	RO	-

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5.3.3.28 por_dt_devid

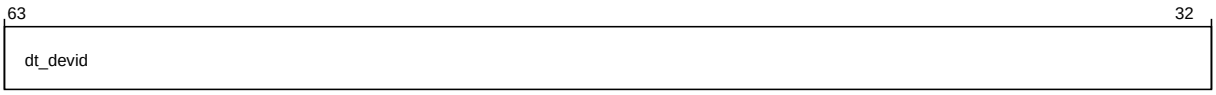
Functions as the device configuration register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFC0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-295: por_dt_por_dt_devid (high)



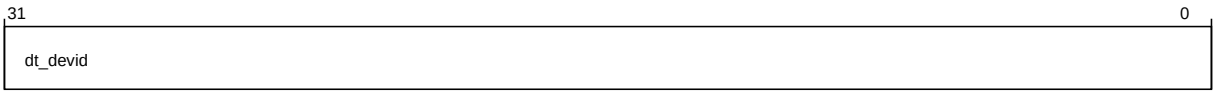
The following table shows the por_dt_devid higher register bit assignments.

Table 5-309: por_dt_por_dt_devid (high)

Bits	Field name	Description	Type	Reset
63:32	dt_devid	Device ID	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-296: por_dt_por_dt_devid (low)



The following table shows the por_dt_devid lower register bit assignments.

Table 5-310: por_dt_por_dt_devid (low)

Bits	Field name	Description	Type	Reset
31:0	dt_devid	Device ID	RO	64'b0

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5.3.3.29 por_dt_devtype

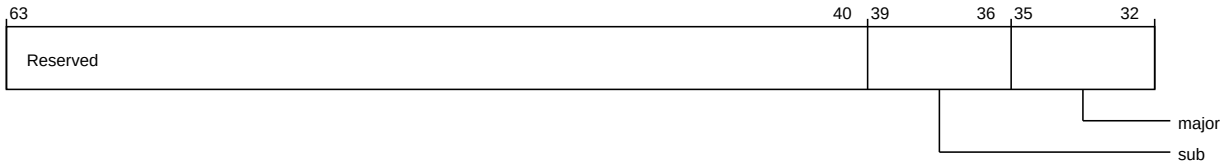
Functions as the device type identifier register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFC8
Register reset 64'b01000011
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-297: por_dt_por_dt_devtype (high)



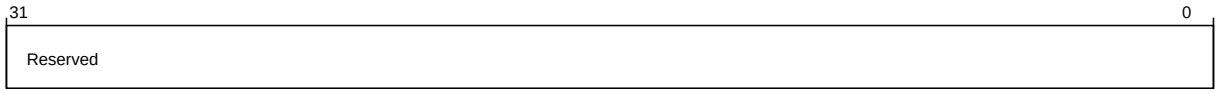
The following table shows the por_dt_devtype higher register bit assignments.

Table 5-311: por_dt_por_dt_devtype (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:36	sub	Sub type	RO	4'h4
35:32	major	Major type	RO	4'h3

The following figure shows the lower register bit assignments.

Figure 5-298: por_dt_por_dt_devtype (low)



The following table shows the por_dt_devtype lower register bit assignments.

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Table 5-312: por_dt_por_dt_devtype (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

5.3.3.30 por_dt_pidr45

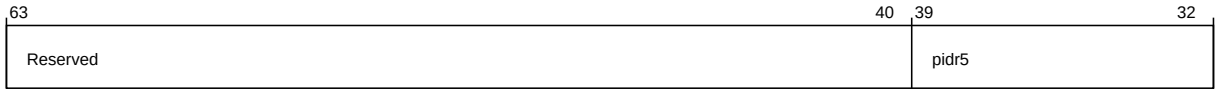
Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFD0
Register reset 64'b000000100
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-299: por_dt_por_dt_pidr45 (high)



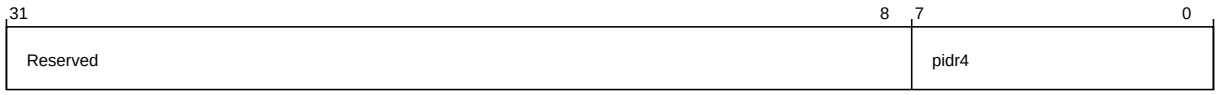
The following table shows the por_dt_pidr45 higher register bit assignments.

Table 5-313: por_dt_por_dt_pidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-300: por_dt_por_dt_pidr45 (low)



The following table shows the por_dt_pidr45 lower register bit assignments.

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Table 5-314: por_dt_por_dt_pidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

5.3.3.31 por_dt_pidr67

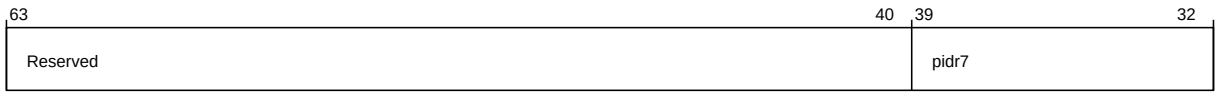
Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFD8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-301: por_dt_por_dt_pidr67 (high)



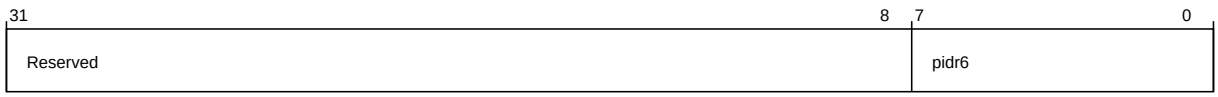
The following table shows the por_dt_pidr67 higher register bit assignments.

Table 5-315: por_dt_por_dt_pidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following figure shows the lower register bit assignments.

Figure 5-302: por_dt_por_dt_pidr67 (low)



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The following table shows the por_dt_pidr67 lower register bit assignments.

Table 5-316: por_dt_por_dt_pidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

5.3.3.32 por_dt_pidr01

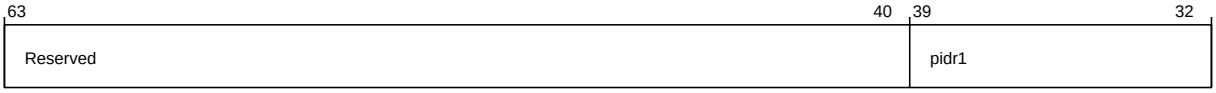
Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFE0
Register reset 64'b0101110000011100
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-303: por_dt_por_dt_pidr01 (high)



The following table shows the por_dt_pidr01 higher register bit assignments.

Table 5-317: por_dt_por_dt_pidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

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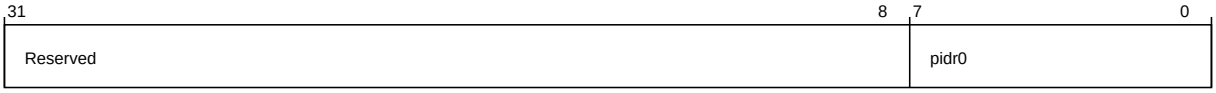
Figure 5-304: por_dt_por_dt_pidr01 (low)



The following table shows the por_dt_pidr01 lower register bit assignments.

Table 5-318: por_dt_por_dt_pidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

5.3.3.33 por_dt_pidr23

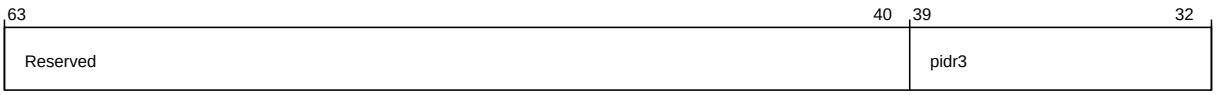
Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFE8
Register reset 64'b000000111
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-305: por_dt_por_dt_pidr23 (high)



The following table shows the por_dt_pidr23 higher register bit assignments.

Table 5-319: por_dt_por_dt_pidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

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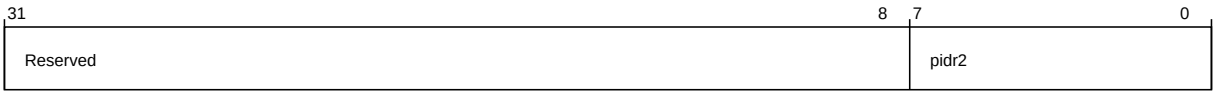
The following figure shows the lower register bit assignments.

Figure 5-306: por_dt_por_dt_pidr23 (low)



The following table shows the por_dt_pidr23 lower register bit assignments.

Table 5-320: por_dt_por_dt_pidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

5.3.3.34 por_dt_cidr01

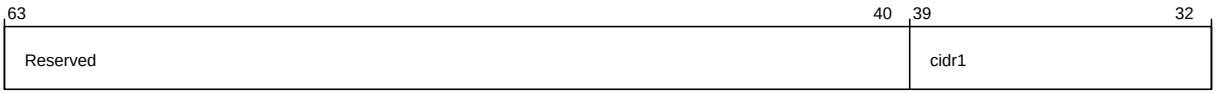
Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFF0
Register reset 64'b1001111100001101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-307: por_dt_por_dt_cidr01 (high)



The following table shows the por_dt_cidr01 higher register bit assignments.

Table 5-321: por_dt_por_dt_cidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-

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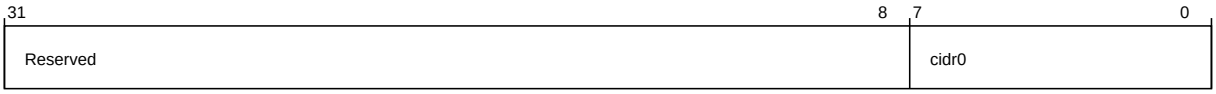
Bits	Field name	Description	Type	Reset
39:32	cidr1	Component ID 1	RO	8'h9f

The following figure shows the lower register bit assignments.

Figure 5-308: por_dt_por_dt_cidr01 (low)



The following table shows the por_dt_cidr01 lower register bit assignments.

Table 5-322: por_dt_por_dt_cidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr0	Component ID 0	RO	8'hd

5.3.3.35 por_dt_cidr23

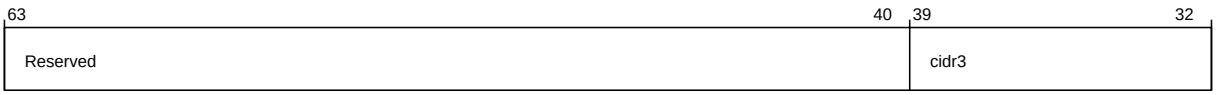
Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hFF8
Register reset 64'b0001011100000101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-309: por_dt_por_dt_cidr23 (high)



The following table shows the por_dt_cidr23 higher register bit assignments.

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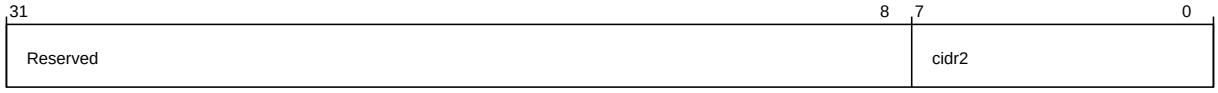
Table 5-323: por_dt_por_dt_cidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr3	Component ID 3	RO	8'hb1

The following figure shows the lower register bit assignments.

Figure 5-310: por_dt_por_dt_cidr23 (low)



The following table shows the por_dt_cidr23 lower register bit assignments.

Table 5-324: por_dt_por_dt_cidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

5.3.4 HN-F register descriptions

This section lists the HN-F registers.

5.3.4.1 por_hnf_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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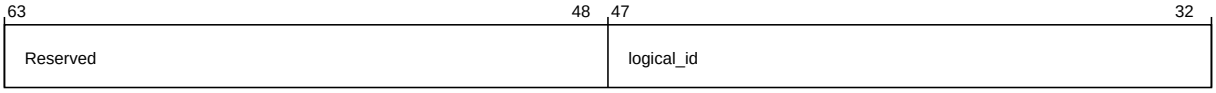
Figure 5-311: por_hnf_por_hnf_node_info (high)



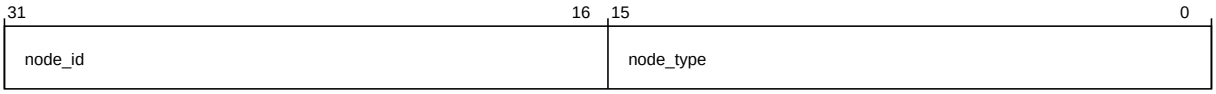
The following table shows the por_hnf_node_info higher register bit assignments.

Table 5-325: por_hnf_por_hnf_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-312: por_hnf_por_hnf_node_info (low)



The following table shows the por_hnf_node_info lower register bit assignments.

Table 5-326: por_hnf_por_hnf_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0005

5.3.4.2 por_hnf_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

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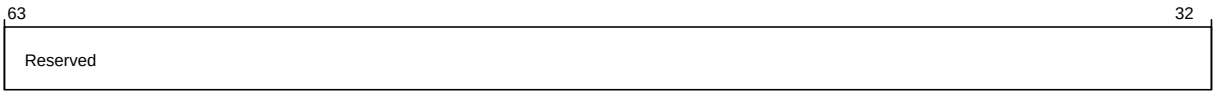
The following figure shows the higher register bit assignments.

Figure 5-313: por_hnf_por_hnf_child_info (high)



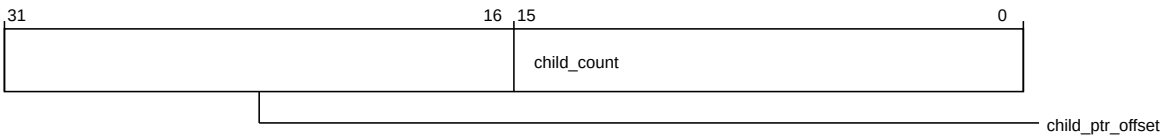
The following table shows the por_hnf_child_info higher register bit assignments.

Table 5-327: por_hnf_por_hnf_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-314: por_hnf_por_hnf_child_info (low)



The following table shows the por_hnf_child_info lower register bit assignments.

Table 5-328: por_hnf_por_hnf_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.4.3 por_hnf_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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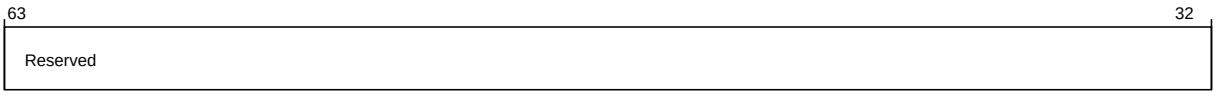
The following figure shows the higher register bit assignments.

Figure 5-315: por_hnf_por_hnf_secure_register_groups_override (high)



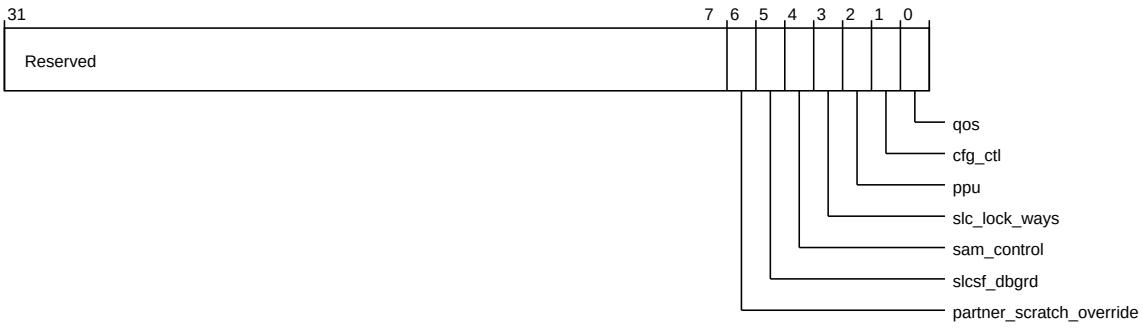
The following table shows the por_hnf_secure_register_groups_override higher register bit assignments.

Table 5-329: por_hnf_por_hnf_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-316: por_hnf_por_hnf_secure_register_groups_override (low)



The following table shows the por_hnf_secure_register_groups_override lower register bit assignments.

Table 5-330: por_hnf_por_hnf_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6	partner_scratch_override	Allows Non-secure access to Secure Partenr scratch registers	RW	1'b0
5	slcsf_dbgrd	Allows Non-secure access to Secure SLC/SF debug read registers	RW	1'b0
4	sam_control	Allows Non-secure access to Secure HN-F SAM control registers	RW	1'b0
3	slc_lock_ways	Allows Non-secure access to Secure cache way locking registers	RW	1'b0
2	ppu	Allows Non-secure access to Secure power policy registers	RW	1'b0
1	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_hnf_cfg_ctl)	RW	1'b0
0	qos	Allows Non-secure access to Secure QoS registers	RW	1'b0

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5.3.4.4 por_hnf_unit_info

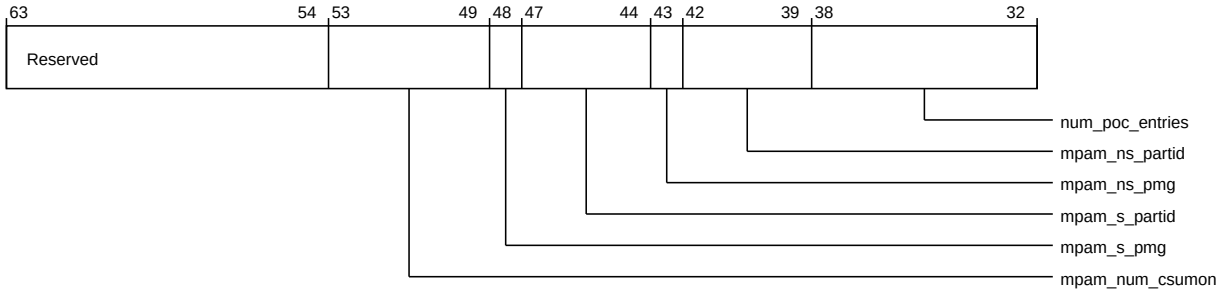
Provides component identification information for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-317: por_hnf_por_hnf_unit_info (high)



The following table shows the por_hnf_unit_info higher register bit assignments.

Table 5-331: por_hnf_por_hnf_unit_info (high)

Bits	Field name	Description	Type	Reset
63:54	Reserved	Reserved	RO	-
53:49	mpam_num_csumon	Number of Cache Storage Usage Monitors for MPAM	RO	Configuration dependent
48	mpam_s_pmg	MPAM Secure supported PMGs 1'b0: 1 S PMG 1'b1: 2 S PMG	RO	-

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Bits	Field name	Description	Type	Reset
47:44	mpam_s_partid	MPAM Secure supported PARTIDs 4'b0000: 1 S PARTID 4'b0001: 2 S PARTID 4'b0010: 4 S PARTID 4'b0011: 8 S PARTID 4'b0100: 16 S PARTID 4'b0101: 32 S PARTID 4'b0110: 64 S PARTID 4'b0111: 128 S PARTID 4'b1000: 256 S PARTID 4'b1001: 512 S PARTID	RO	-
43	mpam_ns_pmg	MPAM Non-Secure supported PMGs 1'b0: 1 NS PMG 1'b1: 2 NS PMG	RO	-
42:39	mpam_ns_partid	MPAM Non-Secure supported PARTIDs 4'b0000: 1 NS PARTID 4'b0001: 2 NS PARTID 4'b0010: 4 NS PARTID 4'b0011: 8 NS PARTID 4'b0100: 16 NS PARTID 4'b0101: 32 NS PARTID 4'b0110: 64 NS PARTID 4'b0111: 128 NS PARTID 4'b1000: 256 NS PARTID 4'b1001: 512 NS PARTID	RO	-
38:32	num_poc_entries	Number of POCQ entries	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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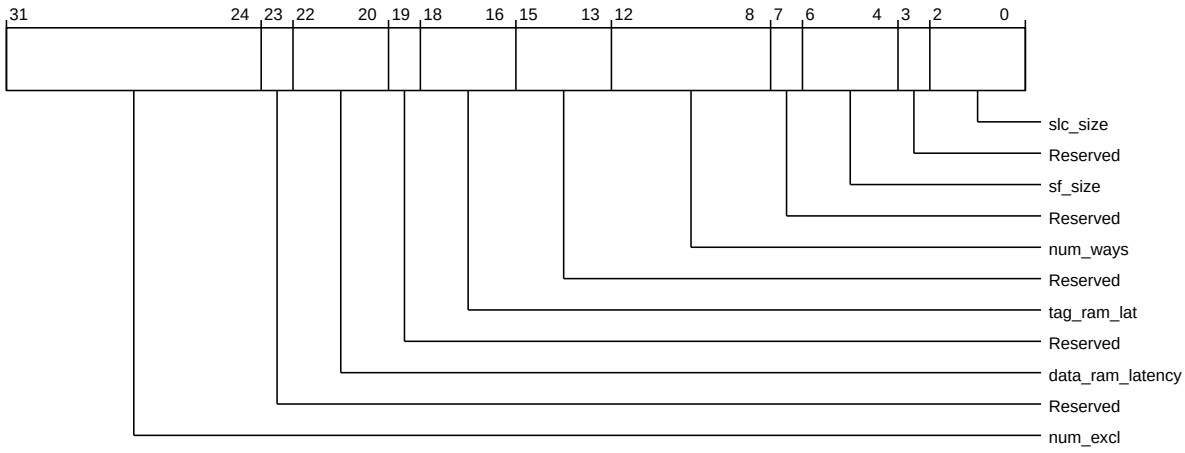
Figure 5-318: por_hnf_por_hnf_unit_info (low)



The following table shows the por_hnf_unit_info lower register bit assignments.

Table 5-332: por_hnf_por_hnf_unit_info (low)

Bits	Field name	Description	Type	Reset
31:24	num_excl	Number of exclusive monitors	RO	-
23	Reserved	Reserved	RO	-
22:20	data_ram_latency	SLC data RAM latency (in cycles)	RO	-
19	Reserved	Reserved	RO	-
18:16	tag_ram_lat	SLC tag RAM latency (in cycles)	RO	-
15:13	Reserved	Reserved	RO	-
12:8	num_ways	Number of cache ways in the SLC	RO	-
7	Reserved	Reserved	RO	-
6:4	sf_size	SF size 3'b000: 512KB 3'b001: 1MB 3'b010: 2MB 3'b011: 4MB 3'b100: 8MB	RO	-
3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	slc_size	SLC size 3'b000: No SLC 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1MB 3'b101: 2MB 3'b110: 3MB 3'b111: 4MB	RO	-

5.3.4.5 por_hnf_cfg_ctl

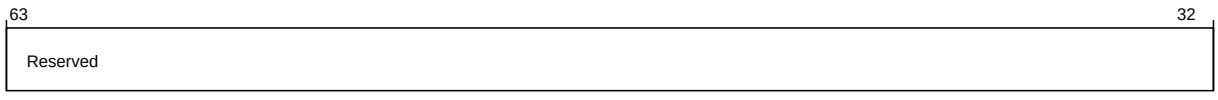
Functions as the configuration control register for HN-F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

Figure 5-319: por_hnf_por_hnf_cfg_ctl (high)



The following table shows the por_hnf_cfg_ctl higher register bit assignments.

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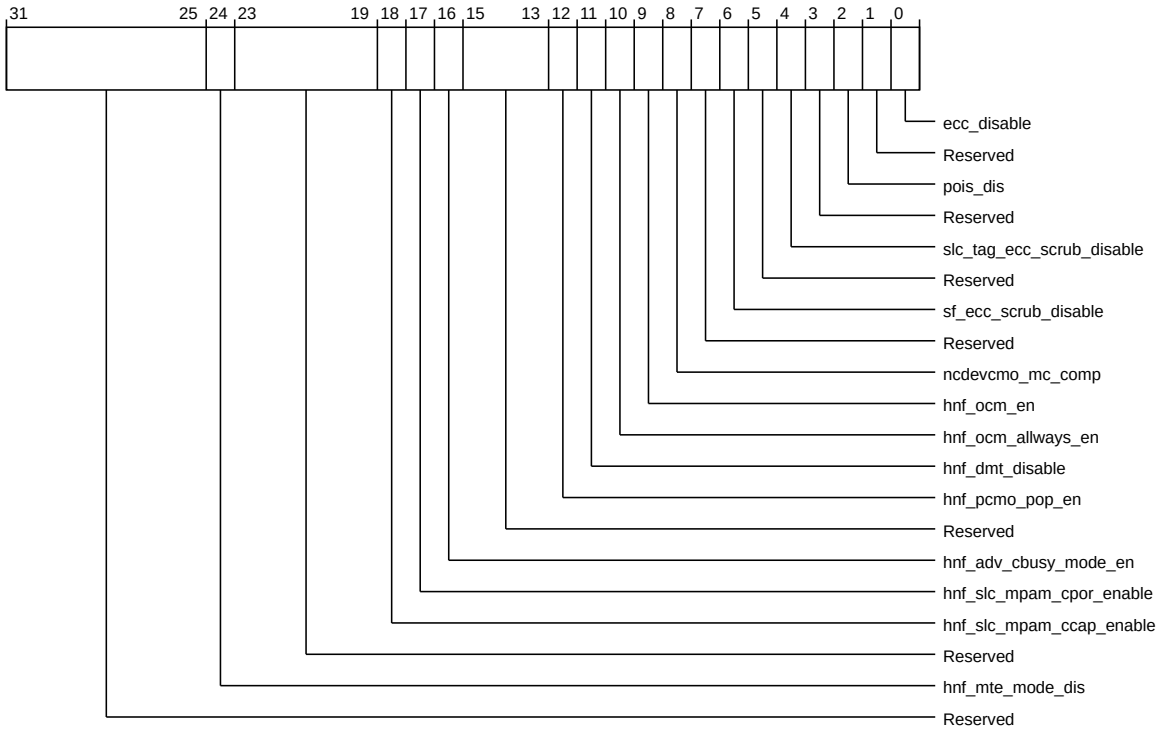
Table 5-333: por_hnf_por_hnf_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-320: por_hnf_por_hnf_cfg_ctl (low)



The following table shows the por_hnf_cfg_ctl lower register bit assignments.

Table 5-334: por_hnf_por_hnf_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	hnf_mte_mode_dis	Disables the MTE features in HNF when set to 1'b1	RW	1'b0
23:19	Reserved	Reserved	RO	-
18	hnf_slc_mpam_ccap_enable	Enable MPAM Cache Capacity Partitioning for SLC 1'b1: Cache Capacity Partitioning is enabled if supported in Hardware. 1'b0: Cache Capacity Partitioning is disabled for SLC. NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0

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Bits	Field name	Description	Type	Reset
17	hnf_slc_mpam_cpor_enable	Enable MPAM Cache Portion Partitioning for SLC 1'b1: Cache Portion Partitioning is enabled if supported in Hardware. 1'b0: Cache Portion Partitioning is disabled for SLC. NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0
16	hnf_adv_cbusy_mode_en	Enables the advanced features of HNF CBusy handling	RW	1'b0
15:13	Reserved	Reserved	RO	-
12	hnf_pcmo_pop_en	Terminates PCMO in HNF when this bit is set to 1'b1	RW	1'b0
11	hnf_dmt_disable	Disables DMT when set	RW	1'b0
10	hnf_ocm_allways_en	Enables all SLC ways with OCM	RW	1'b0
9	hnf_ocm_en	Enables region locking with OCM support	RW	1'b0
8	ncdevcmo_mc_comp	Disables HN-F completion when set NOTE: When set, HN-F sends completion for the following transactions received after completion from SN: 1. Non-cacheable WriteNoSnp 2. Device WriteNoSnp 3. CMO (cache maintenance operations)	RW	1'b0
7	Reserved	Reserved	RO	-
6	sf_ecc_scrub_disable	Disables SF tag single-bit ECC error scrubbing when set	RW	1'b0
5	Reserved	Reserved	RO	-
4	slc_tag_ecc_scrub_disable	Disables SLC tag single-bit ECC error scrubbing when set	RW	1'b0
3	Reserved	Reserved	RO	-
2	pois_dis	Disables parity error data poison when set	RW	1'b0
1	Reserved	Reserved	RO	-
0	ecc_disable	Disables SLC and SF ECC generation/detection when set	RW	1'b0

5.3.4.6 por_hnf_aux_ctl

Functions as the auxiliary control register for HN-F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

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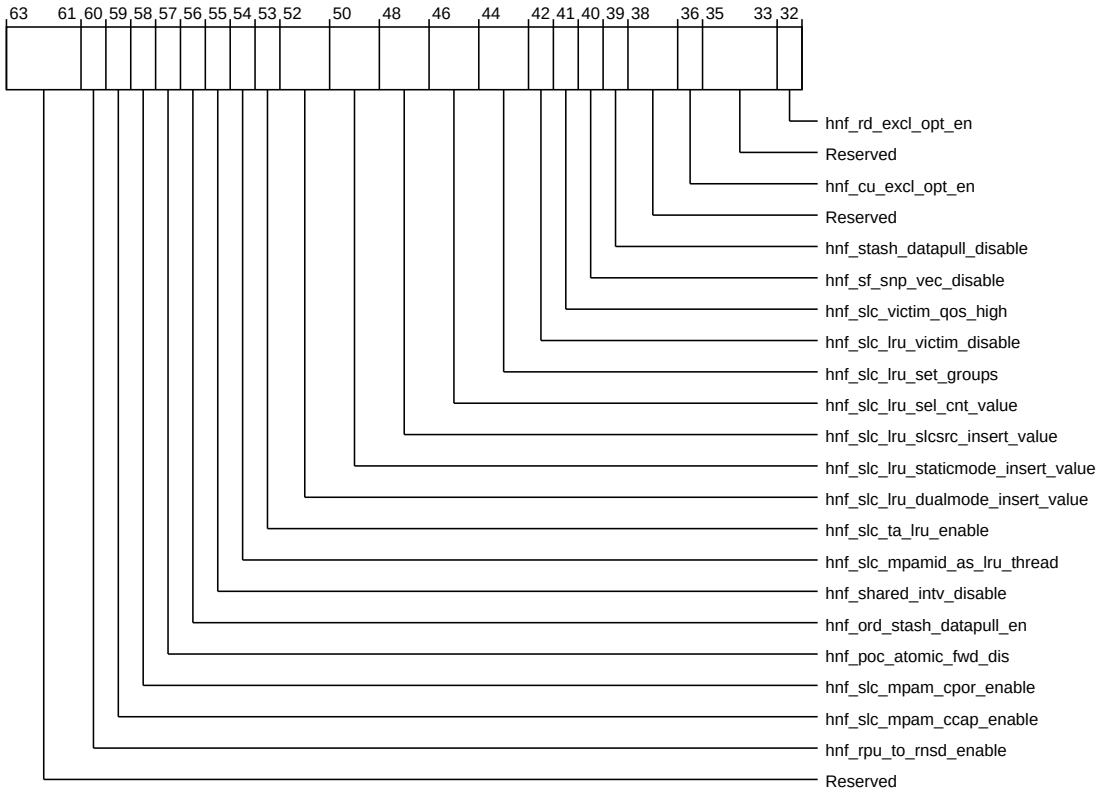
The following figure shows the higher register bit assignments.

Figure 5-321: por_hnf_por_hnf_aux_ctl (high)



The following table shows the por_hnf_aux_ctl higher register bit assignments.

Table 5-335: por_hnf_por_hnf_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:61	Reserved	Reserved	RO	-
60	hnf_rpu_to_rnsd_enable	Enables HN-F to treat ReadPrefUnique ops as ReadNotSharedDirty	RW	1'b0
59	hnf_slc_mpam_ccap_enable	Enable MPAM Cache Capacity Partitioning for SLC 1'b1: Cache Capacity Partitioning is enabled if supported in Hardware. 1'b0: Cache Capacity Partitioning is disabled for SLC. NOTE: This bit moved to cfg_ctl and will be removed in future version of ICN. NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0

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Bits	Field name	Description	Type	Reset
58	hnf_slc_mpam_cpor_enable	Enable MPAM Cache Portion Partitioning for SLC 1'b1: Cache Portion Partitioning is enabled if supported in Hardware. 1'b0: Cache Portion Partitioning is disabled for SLC. NOTE: This bit moved to cfg_ctl and will be removed in future version of ICN. NOTE: If MPAM is disabled at build time, this bit has no meaning.	RW	1'b0
57	hnf_poc_atomic_fwd_dis	Disable the atomic data forwarding in POCQ	RW	1'b0
56	hnf_ord_stash_datapull_en	Enables stash datapull for ordered write stash requests	RW	Configuration dependent
55	hnf_shared_intv_disable	Disables snoop requests to CHIB RN-F with shared copy	RW	Configuration dependent
54	hnf_slc_mpamid_as_lru_thread	Use MPAM PARTID as ThreadID for Thread Aware eLRU 1'b0: ThreadID is based on LPID+LID for Thread Aware eLRU. 1'b1: ThreadID is based on MPAM PARTID+NS for Thread Aware eLRU. Note: MPAM PARTID is used only if MPAM is enabled.	RW	1'b0
53	hnf_slc_ta_lru_enable	Thread Aware eLRU enable 1'b0: ThreadID used for eLRU is zero. 1'b1: ThreadID used for eLRU is based on MPAMID or LPID+LID. Note: If SLC size is less than 256KB, this bit is ignore.	RW	1'b0
52:51	hnf_slc_lru_dualmode_insert_value	Insertion value for Dual mode eLRU NOTE: Default is 2'b11.	RW	2'b11
50:49	hnf_slc_lru_staticmode_insert_value	Insertion value for Static mode eLRU NOTE: Default is 2'b10.	RW	2'b10
48:47	hnf_slc_lru_slcsrc_insert_value	Insertion value if SLC source bit is set NOTE: Default is 2'b00.	RW	2'b00

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Bits	Field name	Description	Type	Reset
46:45	hnf_slc_lru_sel_cnt_value	Selection counter value for eLRU to determine which group policy is more effective 2'b00: Sel counter is like an 8-bit range; upper limit is 255; middle point is 128 2'b01: Sel counter is like a 9-bit range; upper limit is 511; middle point is 256 2'b10: Sel counter is like a 10-bit range; upper limit is 1023; middle point is 512 2'b11: Sel counter is like an 11-bit range; upper limit is 2047; middle point is 1024 NOTE: Default is 10-bit with counter reset to a value of 512.	RW	2'b10
44:43	hnf_slc_lru_set_groups	Number of sets in monitor group for enhance LRU 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 128 NOTE: Default is 32 sets per monitor group. If cache size is small (128KB or less), there would be only one set per group.	RW	2'b01
42	hnf_slc_lru_victim_disable	Disable enhanced LRU based victim selection for SLC 1'b0: SLC victim selection is based on eLRU. 1'b1: SLC victim selection is based on LFSR. NOTE: Victim selection for SF is always LFSR-based.	RW	1'b1
41	hnf_slc_victim_qos_high	SLC victim QoS behavior for SN write request 1'b0: Each victim inherits the QoS value of the request which caused it 1'b1: All victims use high QoS class (14)	RW	1'b0
40	hnf_sf_snp_vec_disable	Disables SF snoop vector when set	RW	1'b0
39	hnf_stash_datapull_disable	Disables HN-F stash data pull support when set	RW	1'b0
38:37	Reserved	Reserved	RO	-
36	hnf_cu_excl_opt_en	CleanUnique exclusive optimization enable	RW	Configuration dependent
35:33	Reserved	Reserved	RO	-
32	hnf_rd_excl_opt_en	ReadNotSharedDirty exclusive optimization enable	RW	1'b0

The following figure shows the lower register bit assignments.

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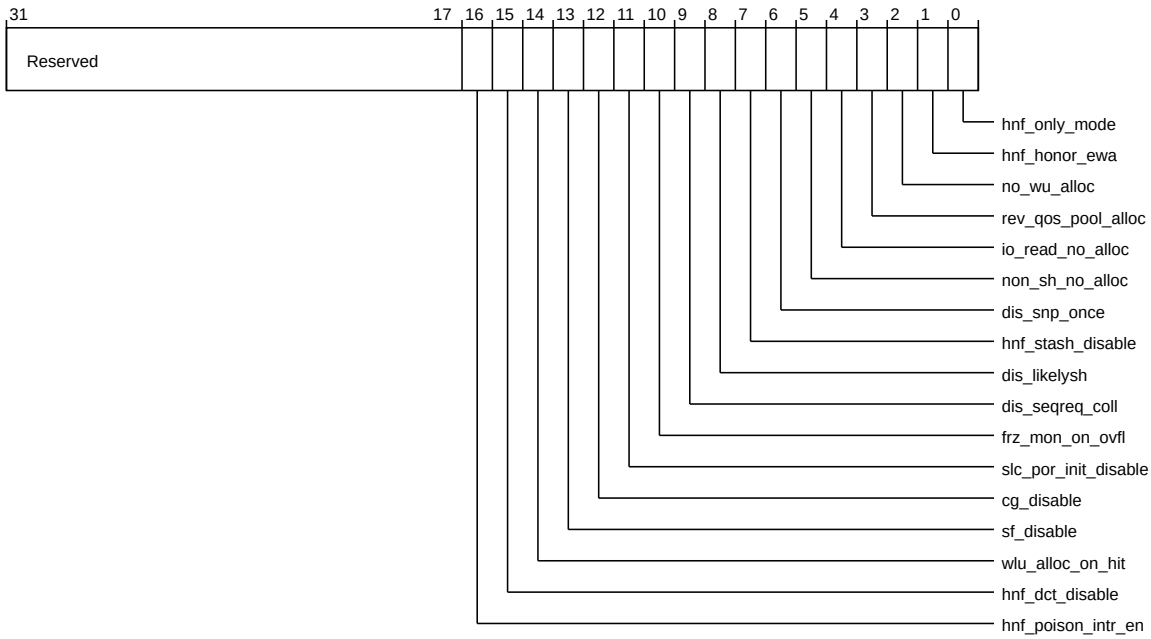
Figure 5-322: por_hnf_por_hnf_aux_ctl (low)



The following table shows the por_hnf_aux_ctl lower register bit assignments.

Table 5-336: por_hnf_por_hnf_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	hnf_poison_intr_en	Enables reporting an interrupt by HN-F when poison is detected at SLC	RW	Configuration dependent
15	hnf_dct_disable	Disables DCT when set	RW	Configuration dependent
14	wlu_alloc_on_hit	Forces WLU requests to allocate if the line hit in SLC	RW	1'b0
13	sf_disable	Disables SF	RW	1'b0
12	cg_disable	Disables HN-F architectural clock gates	RW	1'b0
11	slc_por_init_disable	Disables SLC and SF initialization on Reset	RW	1'b0
10	frz_mon_on_ovfl	Freezes the exclusive monitors	RW	1'b0
9	dis_seqreq_coll		RW	1'b0
8	dis_likelysh	Disables Likely Shared based allocations	RW	1'b0
7	hnf_stash_disable	Disables HN-F stash support	RW	Configuration dependent
6	dis_snp_once	When set, disables SnpOnce and converts to SnpShared	RW	Configuration dependent
5	non_sh_no_alloc	Disables SLC allocation for non-shareable cacheable transactions when set	RW	1'b0
4	io_read_no_alloc	When set, disables ReadOnce and ReadNoSnp allocation in SLC from RN-Is	RW	1'b0
3	rev_qos_pool_alloc	Reverses QoS pool allocation algorithm	RW	1'b0

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Bits	Field name	Description	Type	Reset
2	no_wu_alloc	Disables WriteUnique/WriteLineUnique allocations in SLC when set	RW	1'b0
1	hnf_honor_ewa	When set, postpones completion for writes where EWA=0 in the request until HN-F receives completion from MC or SBSX	RW	1'b1
0	hnf_only_mode	Enables HN-F only mode; disables SLC and SF when set	RW	1'b0

5.3.4.7 por_hnf_r2_aux_ctl

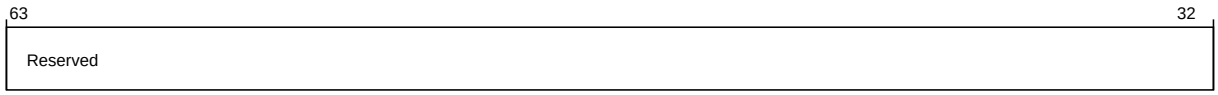
Functions as the auxiliary control register for HN-F for CI-700 R2 features.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA10
Register reset 64'b010010000
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-323: por_hnf_por_hnf_r2_aux_ctl (high)



The following table shows the por_hnf_r2_aux_ctl higher register bit assignments.

Table 5-337: por_hnf_por_hnf_r2_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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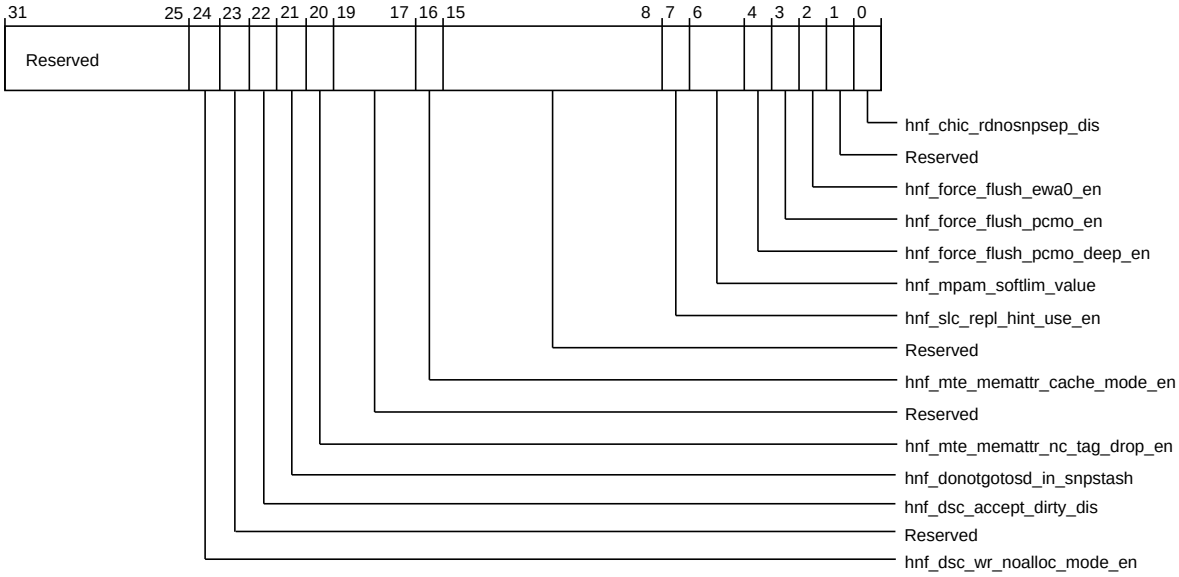
Figure 5-324: por_hnf_por_hnf_r2_aux_ctl (low)



The following table shows the por_hnf_r2_aux_ctl lower register bit assignments.

Table 5-338: por_hnf_por_hnf_r2_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	hnf_dsc_wr_noalloc_mode_en	Enables HNF to mark DSC writes as no-alloc if RNF also retains a copy of the cache line	RW	1'b0
23	Reserved	Reserved	RO	-
22	hnf_dsc_accept_dirty_dis	In DSC mode, disable accepting data from DSC	RW	1'b0
21	hnf_donotgotosd_in_snpstash	Sets the value of DoNotGoToSD bit on SnpStash	RW	1'b0
20	hnf_mte_mematttr_nc_tag_drop_en	Enables HNF to drop any dirty tags for Non-Cacheable memory, when set to 1'b1	RW	1'b0
19:17	Reserved	Reserved	RO	-
16	hnf_mte_mematttr_cache_mode_en	When set to 1'b1, it enables HNF to convert Non-cacheable requests to cacheable if MTE tags are required	RW	1'b1
15:8	Reserved	Reserved	RO	-
7	hnf_slc_repl_hint_use_en	1'b0: Interconnect generated SLC Replacement hints are used for eLRU. 1'b1: RN-F provided SLC Replacement hints are used for eLRU.	RW	1'b0

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Bits	Field name	Description	Type	Reset
6:5	hnf_mpam_softlim_value	Soft Limit value for MPAM capacity partitioning. 2'b00: Soft limit is 0% below hardlimit. 2'b01: Soft limit is 3.13% (1/32) below hardlimit 2'b10: Soft limit is 6.25% (1/16) below hardlimit 2'b11: Soft limit is 9.38% (3/32) below hardlimit NOTE: Default is 3.13% below hardlimit. If CMAX value set is at or below 12.5%, soft limit is ignored.	RW	2'b01
4	hnf_force_flush_pcmo_deep_en	Make PCMO request for SLC and SF flush generated SN writes as Deep PCMO. CONSTRAINT: hnf_force_flush_pcmo_deep_en is valid only if hnf_force_flush_pcmo_en bit is set. CONSTRAINT: This bit can be set only if ALL SNs in the system support deep attribute.	RW	1'b0
3	hnf_force_flush_pcmo_en	Generate PCMO request for SLC and SF flush generated SN writes	RW	1'b0
2	hnf_force_flush_ewa0_en	Force SLC and SF flush to use EWA 0 for SN writes	RW	1'b0
1	Reserved	Reserved	RO	-
0	hnf_chic_rdnosnpsep_dis	Disables separation of Data and Comp in CHIC mode	RW	1'b0

5.3.4.8 por_hnf_cbusy_limit_ctl

Cbusy threshold limits for POCQ entries.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA18
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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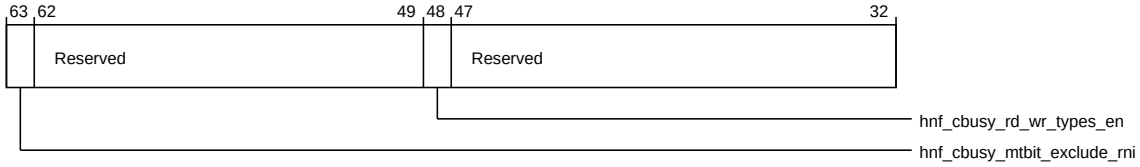
Figure 5-325: por_hnf_por_hnf_cbusy_limit_ctl (high)



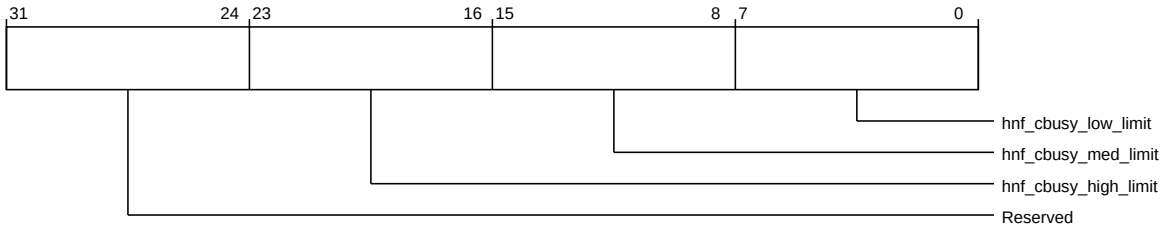
The following table shows the por_hnf_cbusy_limit_ctl higher register bit assignments.

Table 5-339: por_hnf_por_hnf_cbusy_limit_ctl (high)

Bits	Field name	Description	Type	Reset
63	hnf_cbusy_mtbit_exclude_rni	Exclude RNI sources in multi-source mode	RW	1'b0
62:49	Reserved	Reserved	RO	-
48	hnf_cbusy_rd_wr_types_en	When set, CBusy for Reads and Writes are handled independently. The thresholds specified in this register are used for Read request types in POCQ	RW	1'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-326: por_hnf_por_hnf_cbusy_limit_ctl (low)



The following table shows the por_hnf_cbusy_limit_ctl lower register bit assignments.

Table 5-340: por_hnf_por_hnf_cbusy_limit_ctl (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_cbusy_high_limit	POCQ limit for CBusy High	RW	Configuration dependent
15:8	hnf_cbusy_med_limit	POCQ limit for CBusy Med	RW	Configuration dependent
7:0	hnf_cbusy_low_limit	POCQ limit for CBusy Low	RW	Configuration dependent

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5.3.4.9 por_hnf_ppu_pwpr

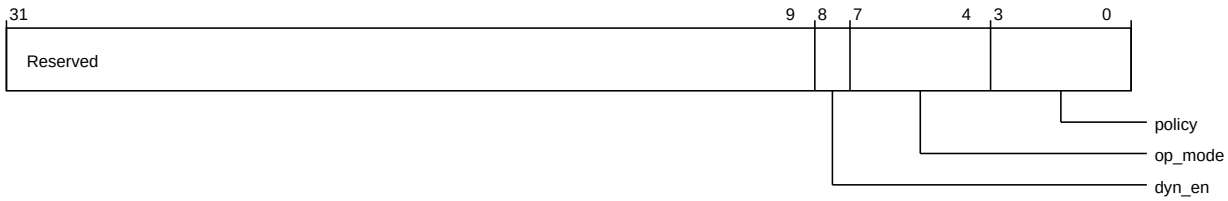
Functions as the power policy register for HN-F.

Its characteristics are:

Type RW
Register width (Bits) 32
Address offset 16'h1C00
Register reset 32'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.ppu

The following figure shows the lower register bit assignments.

Figure 5-327: por_hnf_por_hnf_ppu_pwpr



The following table shows the por_hnf_ppu_pwpr register bit assignments.

Table 5-341: por_hnf_por_hnf_ppu_pwpr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	dyn_en	Dynamic transition enable	RW	1'b0
7:4	op_mode	HN-F operational power mode 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RW	4'b0

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Bits	Field name	Description	Type	Reset
3:0	policy	HN-F power mode policy 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RW	4'b0

5.3.4.10 por_hnf_ppu_pwsr

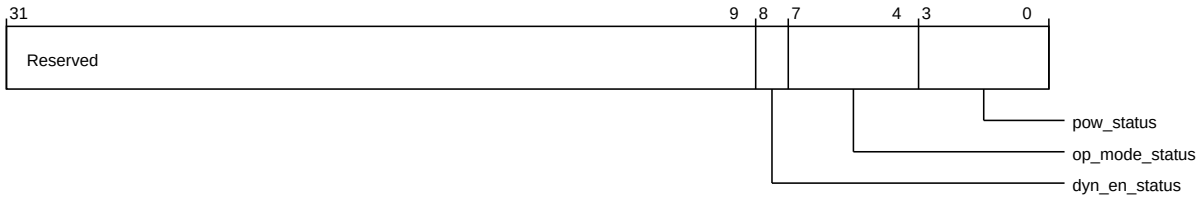
Provides power status information for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h1C08
Register reset 32'b0
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

Figure 5-328: por_hnf_por_hnf_ppu_pwsr



The following table shows the por_hnf_ppu_pwsr register bit assignments.

Table 5-342: por_hnf_por_hnf_ppu_pwsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	dyn_en_status	Dynamic transition status	RO	1'b0

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Bits	Field name	Description	Type	Reset
7:4	op_mode_status	HN-F operational mode status 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RO	4'b0
3:0	pow_status	HN-F power mode status 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RO	4'b0

5.3.4.11 por_hnf_ppu_misr

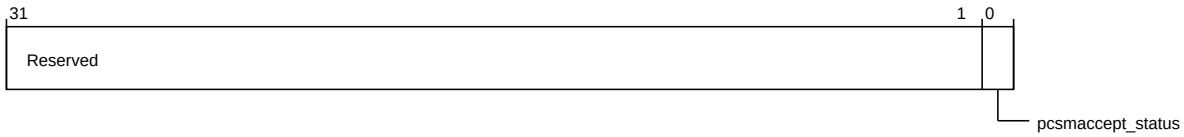
Functions as the power miscellaneous input current status register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h1C14
Register reset 32'b0
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

Figure 5-329: por_hnf_por_hnf_ppu_misr



The following table shows the por_hnf_ppu_misr register bit assignments.

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Table 5-343: por_hnf_por_hnf_ppu_misr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	pcsmaccept_status	HN-F RAM PCSMACCEPT status	RO	1'b0

5.3.4.12 por_hnf_ppu_idr0

Provides identification information for the HN-F PPU.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h2BB0
Register reset 32'b00100000000011010010101000
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

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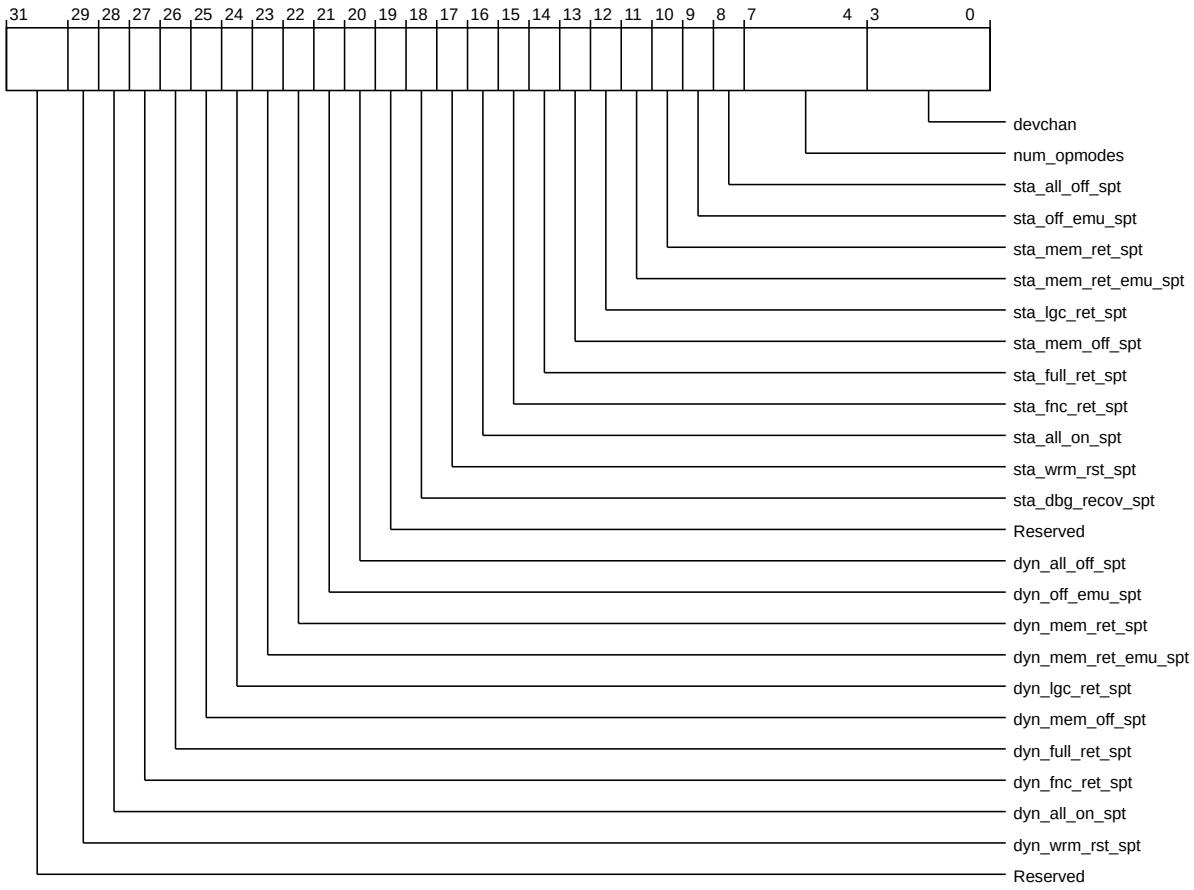
Figure 5-330: por_hnf_por_hnf_ppu_idr0



The following table shows the por_hnf_ppu_idr0 register bit assignments.

Table 5-344: por_hnf_por_hnf_ppu_idr0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29	dyn_wrm_rst_spt	Dynamic warm_rst support	RO	1'b0
28	dyn_all_on_spt	Dynamic on support	RO	1'b0
27	dyn_fnc_ret_spt	Dynamic func_ret support	RO	1'b1
26	dyn_full_ret_spt	Dynamic full_ret support	RO	1'b0
25	dyn_mem_off_spt	Dynamic mem_off support	RO	1'b0
24	dyn_lgc_ret_spt	Dynamic logic_ret support	RO	1'b0
23	dyn_mem_ret_emu_spt	Dynamic mem_ret_emu support	RO	1'b0
22	dyn_mem_ret_spt	Dynamic mem_ret support	RO	1'b0
21	dyn_off_emu_spt	Dynamic off_emu support	RO	1'b0
20	dyn_all_off_spt	Dynamic off support	RO	1'b0
19	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
18	sta_dbg_recov_spt	Static dbg_recov support	RO	1'b0
17	sta_wrm_rst_spt	Static warm_rst support	RO	1'b0
16	sta_all_on_spt	Static on support	RO	1'b1
15	sta_fnc_ret_spt	Static func_ret support	RO	1'b1
14	sta_full_ret_spt	Static full_ret support	RO	1'b0
13	sta_mem_off_spt	Static mem_off support	RO	1'b1
12	sta_lgc_ret_spt	Static logic_ret support	RO	1'b0
11	sta_mem_ret_emu_spt	Static mem_ret_emu support	RO	1'b0
10	sta_mem_ret_spt	Static mem_ret support	RO	1'b1
9	sta_off_emu_spt	Static off_emu support	RO	1'b0
8	sta_all_off_spt	Static off support	RO	1'b1
7:4	num_opmodes	Number of operational modes	RO	4'b0100
3:0	devchan	Number of device interface channels	RO	1'b0

5.3.4.13 por_hnf_ppu_idr1

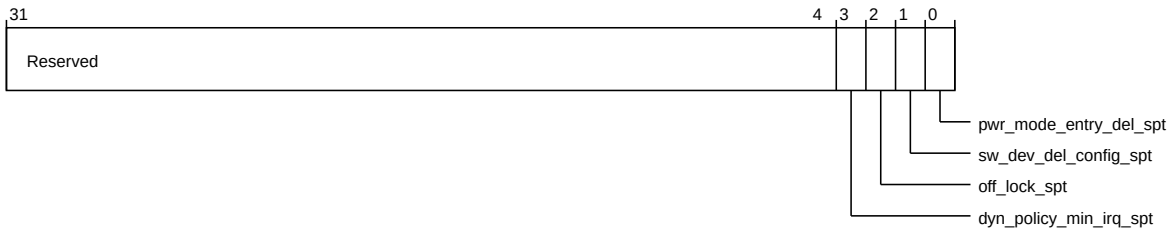
Provides identification information for the HN-F PPU.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h2BB4
Register reset 32'b0
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

Figure 5-331: por_hnf_por_hnf_ppu_idr1



The following table shows the por_hnf_ppu_idr1 register bit assignments.

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Table 5-345: por_hnf_por_hnf_ppu_idr1 (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	dyn_policy_min_irq_spt	Dynamic minimum policy interrupt support	RO	1'b0
2	off_lock_spt	Off and mem_ret lock support	RO	1'b0
1	sw_dev_del_config_spt	Software device delay control configuration support	RO	1'b0
0	pwr_mode_entry_del_spt	Power mode entry delay support	RO	1'b0

5.3.4.14 por_hnf_ppu_iidr

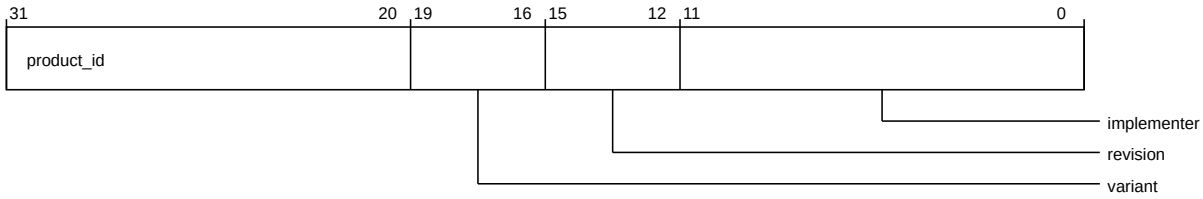
Functions as the power implementation identification register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h2BC8
Register reset 32'b00001001110000000000000100111011
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

Figure 5-332: por_hnf_por_hnf_ppu_iidr



The following table shows the por_hnf_ppu_iidr register bit assignments.

Table 5-346: por_hnf_por_hnf_ppu_iidr (low)

Bits	Field name	Description	Type	Reset
31:20	product_id	Implementation identifier	RO	12'h434
19:16	variant	Implementation variant	RO	4'h0
15:12	revision	Implementation revision	RO	4'h0
11:0	implementer	Arm implementation	RO	12'h43B

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5.3.4.15 por_hnf_ppu_aidr

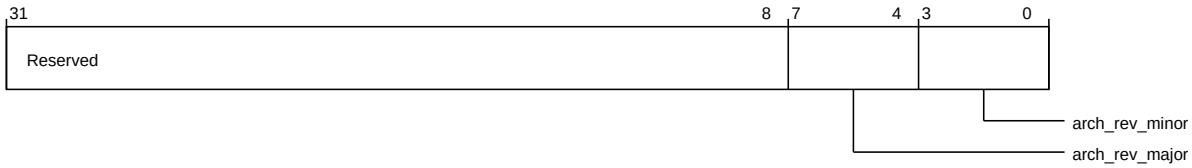
Functions as the power architecture identification register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 16'h2BCC
Register reset 32'b00010001
Usage constraints There are no usage constraints.

The following figure shows the lower register bit assignments.

Figure 5-333: por_hnf_por_hnf_ppu_aidr



The following table shows the por_hnf_ppu_aidr register bit assignments.

Table 5-347: por_hnf_por_hnf_ppu_aidr (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:4	arch_rev_major	PPU architecture major revision	RO	4'h1
3:0	arch_rev_minor	PPU architecture minor revision	RO	4'h1

5.3.4.16 por_hnf_ppu_dyn_ret_threshold

Configures the dynamic retention threshold for SLC and SF RAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1D00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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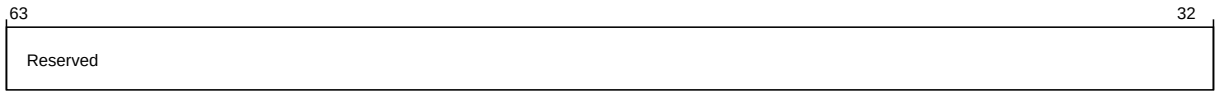
Secure group override por_hnf_secure_register_groups_override.ppu

The following figure shows the higher register bit assignments.

Figure 5-334: por_hnf_por_hnf_ppu_dyn_ret_threshold (high)



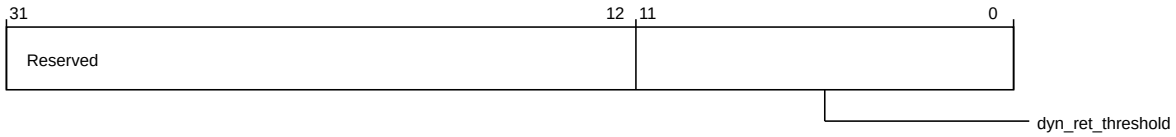
The following table shows the por_hnf_ppu_dyn_ret_threshold higher register bit assignments.

Table 5-348: por_hnf_por_hnf_ppu_dyn_ret_threshold (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-335: por_hnf_por_hnf_ppu_dyn_ret_threshold (low)



The following table shows the por_hnf_ppu_dyn_ret_threshold lower register bit assignments.

Table 5-349: por_hnf_por_hnf_ppu_dyn_ret_threshold (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	dyn_ret_threshold	HN-F RAM idle cycle count threshold	RW	32'b0

5.3.4.17 por_hnf_qos_band

Provides QoS classifications based on the QoS value ranges.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hA80
Register reset 64'b1111111111101100101110000011100000

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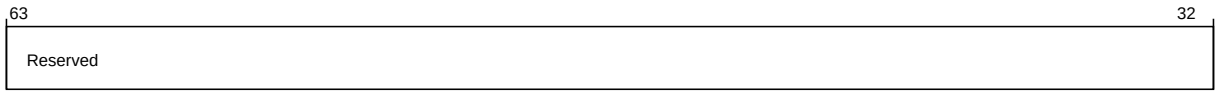
Usage constraints Only accessible by Secure accesses.

Secure group override por_hnf_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

Figure 5-336: por_hnf_por_hnf_qos_band (high)



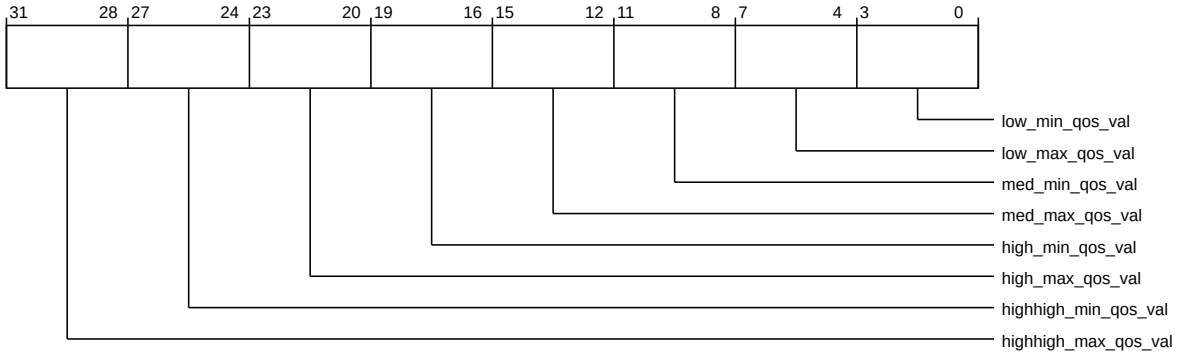
The following table shows the por_hnf_qos_band higher register bit assignments.

Table 5-350: por_hnf_por_hnf_qos_band (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-337: por_hnf_por_hnf_qos_band (low)



The following table shows the por_hnf_qos_band lower register bit assignments.

Table 5-351: por_hnf_por_hnf_qos_band (low)

Bits	Field name	Description	Type	Reset
31:28	highhigh_max_qos_val	Maximum value for HighHigh QoS class	RO	4'hF
27:24	highhigh_min_qos_val	Minimum value for HighHigh QoS class	RO	4'hF
23:20	high_max_qos_val	Maximum value for High QoS class	RO	4'hE
19:16	high_min_qos_val	Minimum value for High QoS class	RO	4'hC
15:12	med_max_qos_val	Maximum value for Medium QoS class	RO	4'hB
11:8	med_min_qos_val	Minimum value for Medium QoS class	RO	4'h8

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Bits	Field name	Description	Type	Reset
7:4	low_max_qos_val	Maximum value for Low QoS class	RO	4'h7
3:0	low_min_qos_val	Minimum value for Low QoS class	RO	4'h0

5.3.4.18 por_hnf_qos_reservation

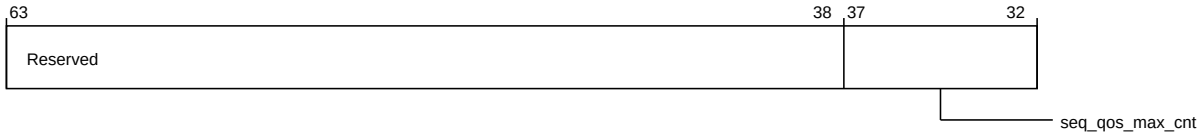
Controls POCQ maximum occupancy counts for each QoS class (HighHigh, High, Medium, and Low).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA88
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

Figure 5-338: por_hnf_por_hnf_qos_reservation (high)



The following table shows the por_hnf_qos_reservation higher register bit assignments.

Table 5-352: por_hnf_por_hnf_qos_reservation (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	seq_qos_max_cnt	Number of entries reserved for SF evictions in POCQ CONSTRAINT: Maximum number is 2 entries.	RW	6'h1

The following figure shows the lower register bit assignments.

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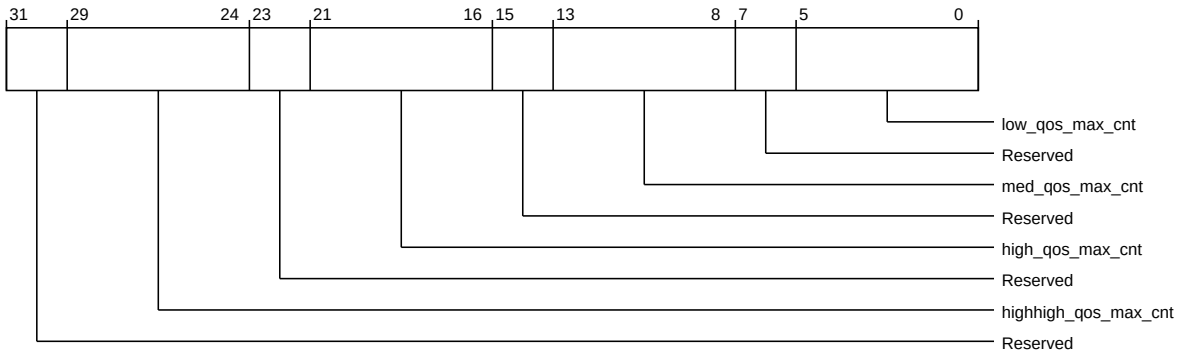
Figure 5-339: por_hnf_por_hnf_qos_reservation (low)



The following table shows the por_hnf_qos_reservation lower register bit assignments.

Table 5-353: por_hnf_por_hnf_qos_reservation (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	highhigh_qos_max_cnt	Maximum number of HighHigh QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
23:22	Reserved	Reserved	RO	-
21:16	high_qos_max_cnt	Maximum number of High QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:8	med_qos_max_cnt	Maximum number of Medium QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
7:6	Reserved	Reserved	RO	-
5:0	low_qos_max_cnt	Maximum number of Low QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent

5.3.4.19 por_hnf_rn_starvation

Controls starvation counts for each QoS class. Determines static credit grantee selection.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA90
Register reset 64'b1111111111111111011111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.qos

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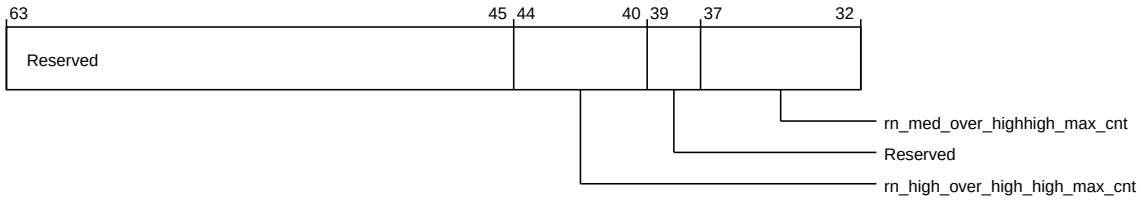
The following figure shows the higher register bit assignments.

Figure 5-340: por_hnf_por_hnf_rn_starvation (high)



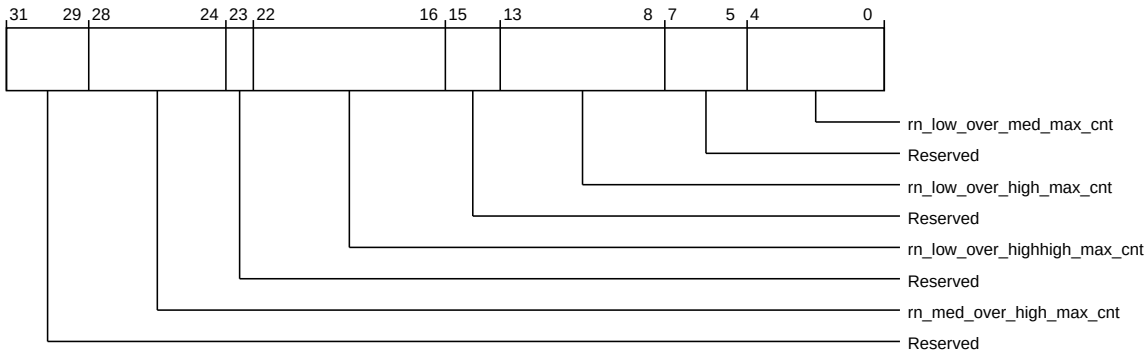
The following table shows the por_hnf_rn_starvation higher register bit assignments.

Table 5-354: por_hnf_por_hnf_rn_starvation (high)

Bits	Field name	Description	Type	Reset
63:45	Reserved	Reserved	RO	-
44:40	rn_high_over_high_high_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over High QoS class	RW	5'h1F
39:38	Reserved	Reserved	RO	-
37:32	rn_med_over_highhigh_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over Medium QoS class	RW	6'h3F

The following figure shows the lower register bit assignments.

Figure 5-341: por_hnf_por_hnf_rn_starvation (low)



The following table shows the por_hnf_rn_starvation lower register bit assignments.

Table 5-355: por_hnf_por_hnf_rn_starvation (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	rn_med_over_high_max_cnt	Maximum number of consecutive instances where High QoS class wins priority over Medium QoS class	RW	5'h1F
23	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
22:16	rn_low_over_highhigh_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over Low QoS class	RW	7'h3F
15:14	Reserved	Reserved	RO	-
13:8	rn_low_over_high_max_cnt	Maximum number of consecutive instances where High QoS class wins priority over Low QoS class	RW	6'h3F
7:5	Reserved	Reserved	RO	-
4:0	rn_low_over_med_max_cnt	Maximum number of consecutive instances where Medium QoS class wins priority over Low QoS class	RW	5'h1F

5.3.4.20 por_hnf_errfr

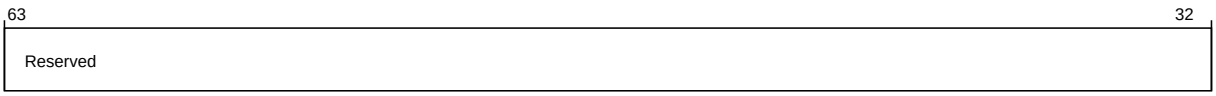
Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3000
Register reset 64'b1001010100101
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-342: por_hnf_por_hnf_errfr (high)



The following table shows the por_hnf_errfr higher register bit assignments.

Table 5-356: por_hnf_por_hnf_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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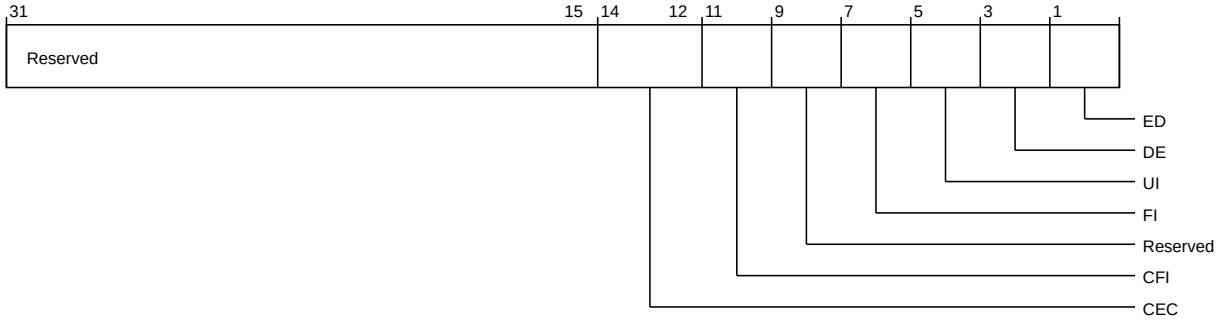
Figure 5-343: por_hnf_por_hnf_errfr (low)



The following table shows the por_hnf_errfr lower register bit assignments.

Table 5-357: por_hnf_por_hnf_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_hnf_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_hnf_errmisc[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

5.3.4.21 por_hnf_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0

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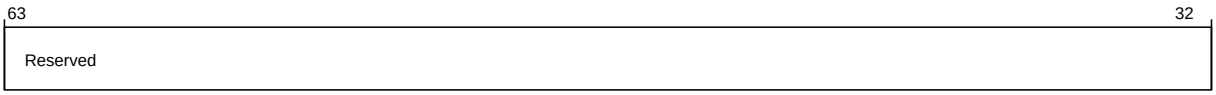
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-344: por_hnf_por_hnf_errctlr (high)



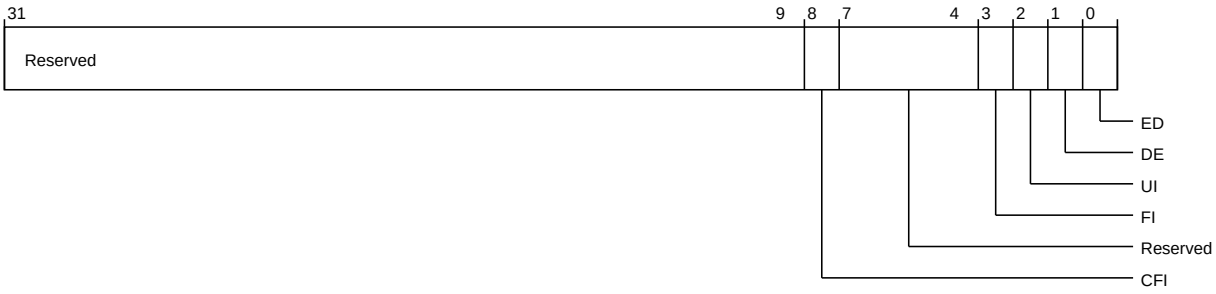
The following table shows the por_hnf_errctlr higher register bit assignments.

Table 5-358: por_hnf_por_hnf_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-345: por_hnf_por_hnf_errctlr (low)



The following table shows the por_hnf_errctlr lower register bit assignments.

Table 5-359: por_hnf_por_hnf_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hnf_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hnf_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hnf_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hnf_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hnf_errfr.ED	RW	1'b0

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5.3.4.22 por_hnf_errstatus

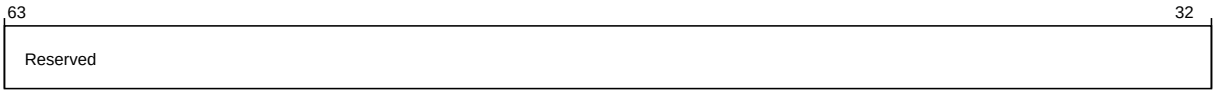
Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-346: por_hnf_por_hnf_errstatus (high)



The following table shows the por_hnf_errstatus higher register bit assignments.

Table 5-360: por_hnf_por_hnf_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-347: por_hnf_por_hnf_errstatus (low)



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The following table shows the por_hnf_errstatus lower register bit assignments.

Table 5-361: por_hnf_por_hnf_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hnf_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hnf_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

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5.3.4.23 por_hnf_erraddr

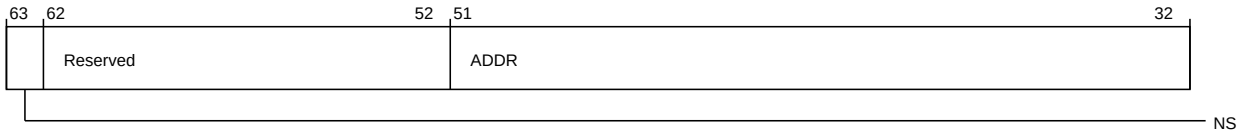
Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-348: por_hnf_por_hnf_erraddr (high)



The following table shows the por_hnf_erraddr higher register bit assignments.

Table 5-362: por_hnf_por_hnf_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hnf_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

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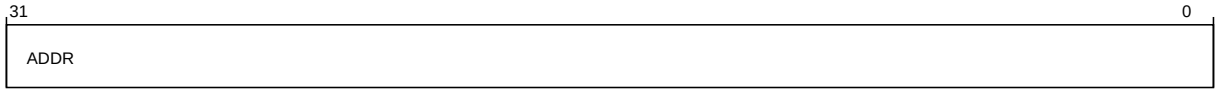
Figure 5-349: por_hnf_por_hnf_erraddr (low)



The following table shows the por_hnf_erraddr lower register bit assignments.

Table 5-363: por_hnf_por_hnf_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

5.3.4.24 por_hnf_errmisc

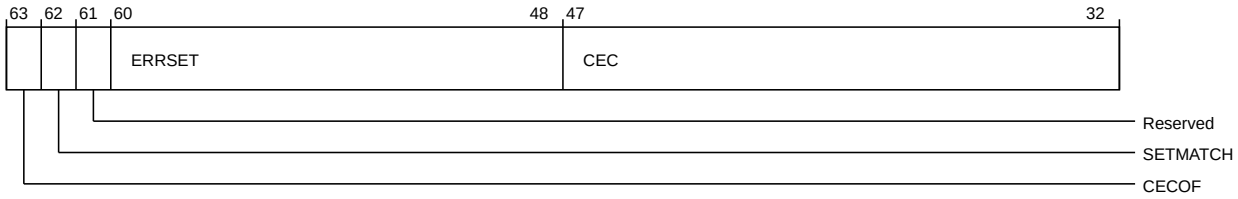
Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-350: por_hnf_por_hnf_errmisc (high)



The following table shows the por_hnf_errmisc higher register bit assignments.

Table 5-364: por_hnf_por_hnf_errmisc (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0

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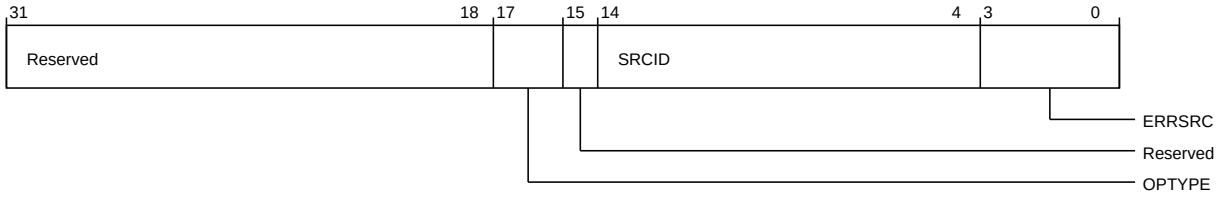
Bits	Field name	Description	Type	Reset
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following figure shows the lower register bit assignments.

Figure 5-351: por_hnf_por_hnf_errmisc (low)



The following table shows the por_hnf_errmisc lower register bit assignments.

Table 5-365: por_hnf_por_hnf_errmisc (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0

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Bits	Field name	Description	Type	Reset
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

5.3.4.25 por_hnf_err_inj

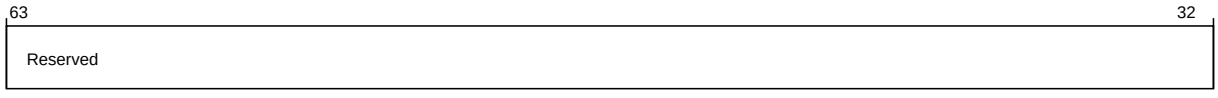
Enables error injection and setup. When enabled for a given source ID and logic processor ID, HN-F returns a slave error and reports an error interrupt. This error interrupt emulates a SLC double-bit data ECC error. This feature enables software to test the error handler. The slave error is reported for cacheable read access for which SLC hit is the data source. No slave error or error interrupt is reported for cacheable read access in which SLC miss is the data source.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3030
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-352: por_hnf_por_hnf_err_inj (high)



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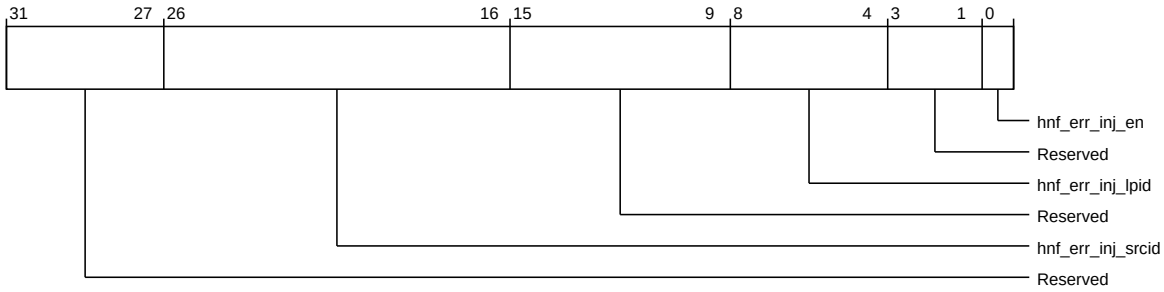
The following table shows the por_hnf_err_inj higher register bit assignments.

Table 5-366: por_hnf_por_hnf_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-353: por_hnf_por_hnf_err_inj (low)



The following table shows the por_hnf_err_inj lower register bit assignments.

Table 5-367: por_hnf_por_hnf_err_inj (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	hnf_err_inj_srcid	RN source ID for read access which results in a SLC miss; does not report slave error or error to match error injection	RW	11'h0
15:9	Reserved	Reserved	RO	-
8:4	hnf_err_inj_lpid	LPID used to match for error injection	RW	5'h0
3:1	Reserved	Reserved	RO	-
0	hnf_err_inj_en	Enables error injection and report	RW	1'b0

5.3.4.26 por_hnf_byte_par_err_inj

Functions as the byte parity error injection register for HN-F.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'h3038
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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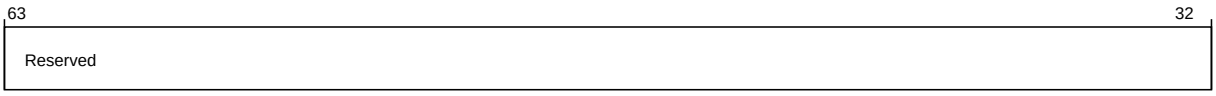
The following figure shows the higher register bit assignments.

Figure 5-354: por_hnf_por_hnf_byte_par_err_inj (high)



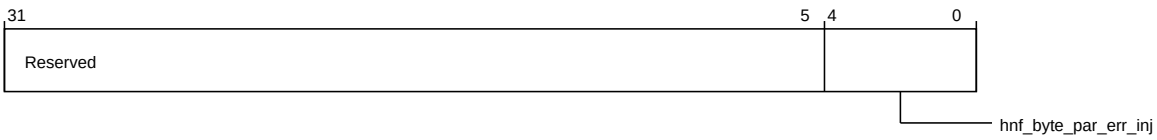
The following table shows the por_hnf_byte_par_err_inj higher register bit assignments.

Table 5-368: por_hnf_por_hnf_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-355: por_hnf_por_hnf_byte_par_err_inj (low)



The following table shows the por_hnf_byte_par_err_inj lower register bit assignments.

Table 5-369: por_hnf_por_hnf_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	hnf_byte_par_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next SLC hit; the error will be injected in all data flits on specified byte (0 to 31)	WO	5'h0

5.3.4.27 por_hnf_errfr_NS

Functions as the Non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b1001010100101
Usage constraints There are no usage constraints.

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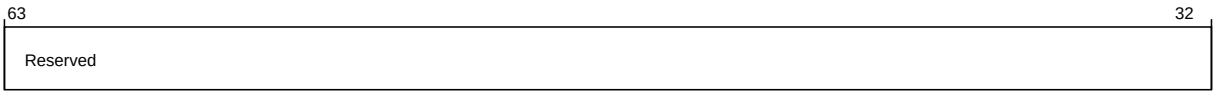
The following figure shows the higher register bit assignments.

Figure 5-356: por_hnf_por_hnf_errfr_ns (high)



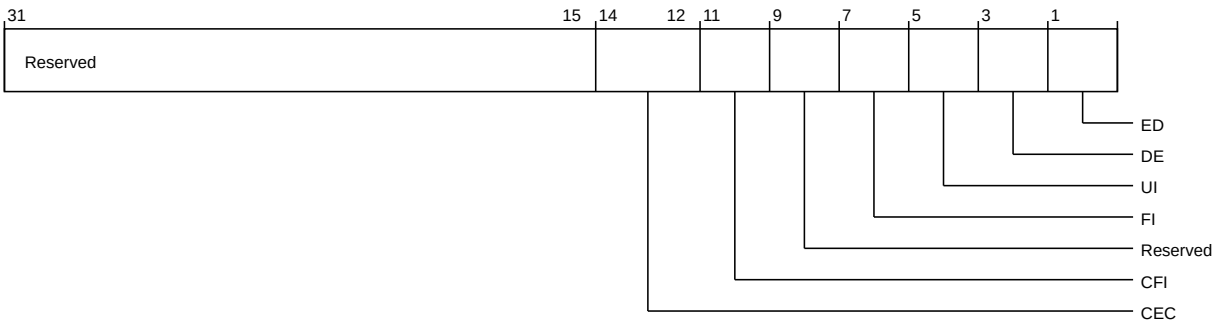
The following table shows the por_hnf_errfr_NS higher register bit assignments.

Table 5-370: por_hnf_por_hnf_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-357: por_hnf_por_hnf_errfr_ns (low)



The following table shows the por_hnf_errfr_NS lower register bit assignments.

Table 5-371: por_hnf_por_hnf_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_hnf_errmisc_NS[39:32] 3'b100: Implements 16-bit error counter in por_hnf_errmisc_NS[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10

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Bits	Field name	Description	Type	Reset
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

5.3.4.28 por_hnf_errctlr_NS

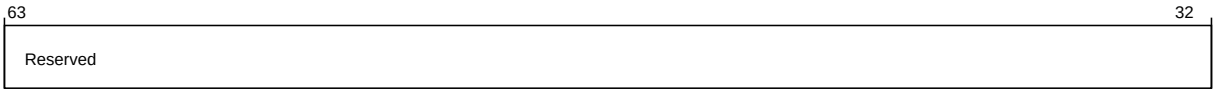
Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-358: por_hnf_por_hnf_errctlr_ns (high)



The following table shows the por_hnf_errctlr_NS higher register bit assignments.

Table 5-372: por_hnf_por_hnf_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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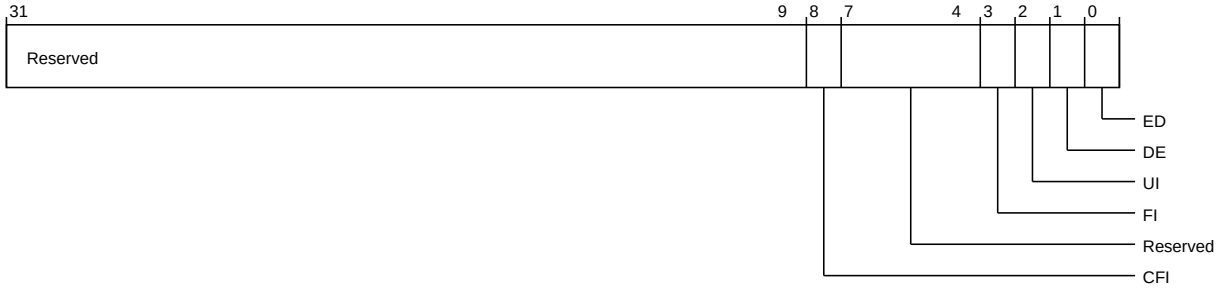
Figure 5-359: por_hnf_por_hnf_errctlr_ns (low)



The following table shows the por_hnf_errctlr_NS lower register bit assignments.

Table 5-373: por_hnf_por_hnf_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hnf_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hnf_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hnf_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hnf_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hnf_errfr_NS.ED	RW	1'b0

5.3.4.29 por_hnf_errstatus_NS

Functions as the Non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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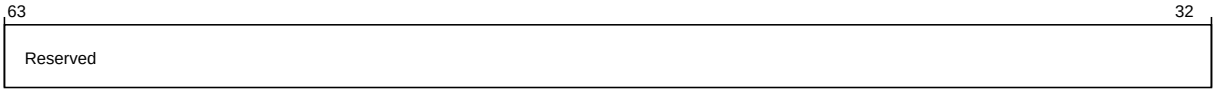
Figure 5-360: por_hnf_por_hnf_errstatus_ns (high)



The following table shows the por_hnf_errstatus_NS higher register bit assignments.

Table 5-374: por_hnf_por_hnf_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-361: por_hnf_por_hnf_errstatus_ns (low)



The following table shows the por_hnf_errstatus_NS lower register bit assignments.

Table 5-375: por_hnf_por_hnf_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hnf_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0

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Bits	Field name	Description	Type	Reset
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hnf_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.4.30 por_hnf_erraddr_NS

Contains the Non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

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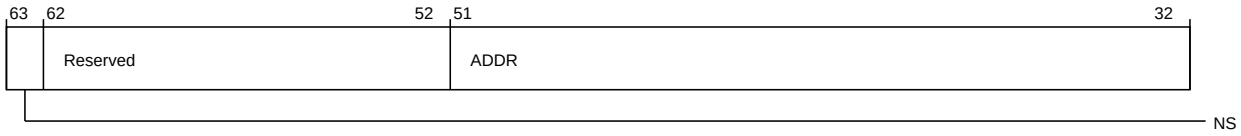
The following figure shows the higher register bit assignments.

Figure 5-362: por_hnf_por_hnf_erraddr_ns (high)



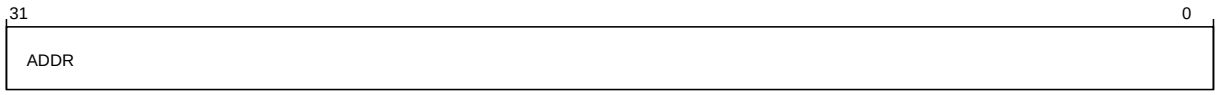
The following table shows the por_hnf_erraddr_NS higher register bit assignments.

Table 5-376: por_hnf_por_hnf_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hnf_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-363: por_hnf_por_hnf_erraddr_ns (low)



The following table shows the por_hnf_erraddr_NS lower register bit assignments.

Table 5-377: por_hnf_por_hnf_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

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5.3.4.31 por_hnf_errmisc_NS

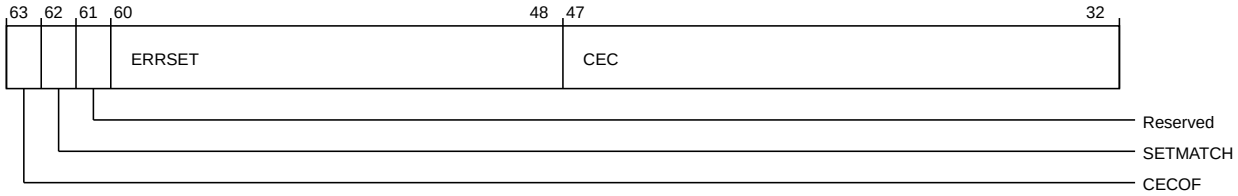
Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-364: por_hnf_por_hnf_errmisc_ns (high)



The following table shows the por_hnf_errmisc_NS higher register bit assignments.

Table 5-378: por_hnf_por_hnf_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following figure shows the lower register bit assignments.

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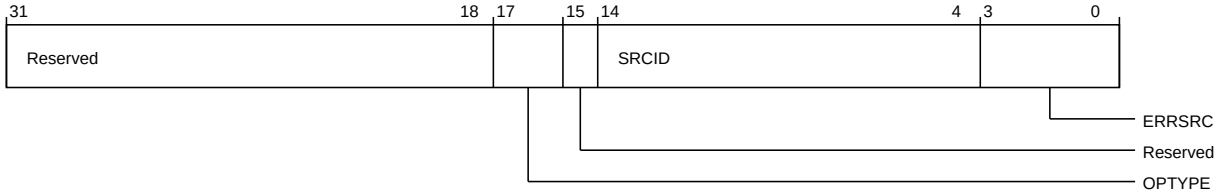
Figure 5-365: por_hnf_por_hnf_errmisc_ns (low)



The following table shows the por_hnf_errmisc_NS lower register bit assignments.

Table 5-379: por_hnf_por_hnf_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

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5.3.4.32 por_hnf_slc_lock_ways

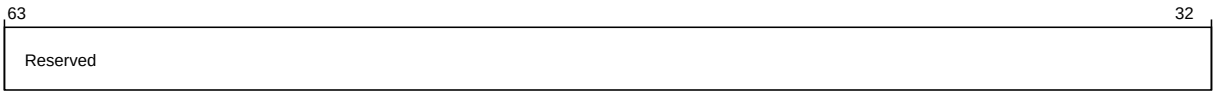
Controls SLC way lock settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC00
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-366: por_hnf_por_hnf_slc_lock_ways (high)



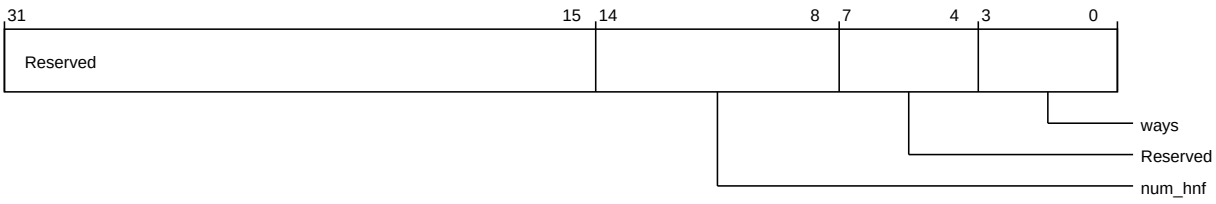
The following table shows the por_hnf_slc_lock_ways higher register bit assignments.

Table 5-380: por_hnf_por_hnf_slc_lock_ways (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-367: por_hnf_por_hnf_slc_lock_ways (low)



The following table shows the por_hnf_slc_lock_ways lower register bit assignments.

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Table 5-381: por_hnf_por_hnf_slc_lock_ways (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:8	num_hnf	Number of HN-Fs in NUMA (non-uniform memory access) region	RW	Configuration dependent
7:4	Reserved	Reserved	RO	-
3:0	ways	Number of SLC ways locked (1, 2, 4, 8, 12)	RW	4'b0

5.3.4.33 por_hnf_slc_lock_base0

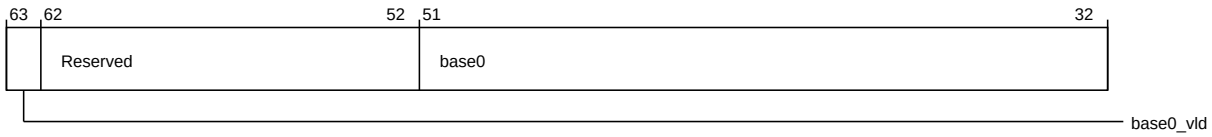
Functions as the base register for lock region 0 [47:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-368: por_hnf_por_hnf_slc_lock_base0 (high)



The following table shows the por_hnf_slc_lock_base0 higher register bit assignments.

Table 5-382: por_hnf_por_hnf_slc_lock_base0 (high)

Bits	Field name	Description	Type	Reset
63	base0_vld	Lock region 0 base valid	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	base0	Lock region 0 base address	RW	52'b0

The following figure shows the lower register bit assignments.

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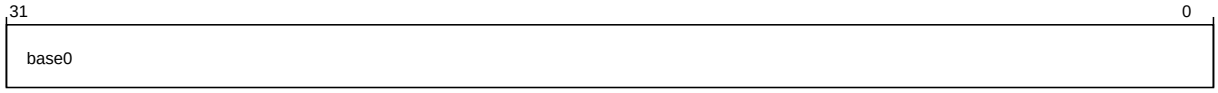
Figure 5-369: por_hnf_por_hnf_slc_lock_base0 (low)



The following table shows the por_hnf_slc_lock_base0 lower register bit assignments.

Table 5-383: por_hnf_por_hnf_slc_lock_base0 (low)

Bits	Field name	Description	Type	Reset
31:0	base0	Lock region 0 base address	RW	52'b0

5.3.4.34 por_hnf_slc_lock_base1

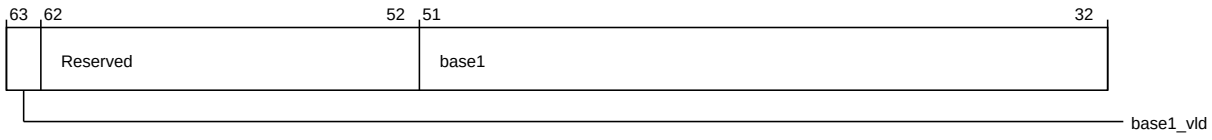
Functions as the base register for lock region 1 [47:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-370: por_hnf_por_hnf_slc_lock_base1 (high)



The following table shows the por_hnf_slc_lock_base1 higher register bit assignments.

Table 5-384: por_hnf_por_hnf_slc_lock_base1 (high)

Bits	Field name	Description	Type	Reset
63	base1_vld	Lock region 1 base valid	RW	1'b0

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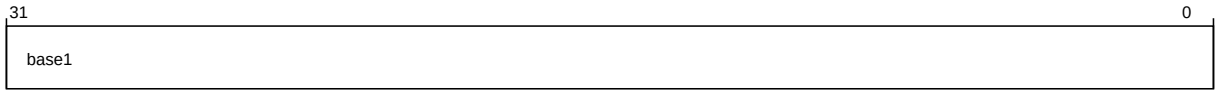
Bits	Field name	Description	Type	Reset
62:52	Reserved	Reserved	RO	-
51:32	base1	Lock region 1 base address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-371: por_hnf_por_hnf_slc_lock_base1 (low)



The following table shows the por_hnf_slc_lock_base1 lower register bit assignments.

Table 5-385: por_hnf_por_hnf_slc_lock_base1 (low)

Bits	Field name	Description	Type	Reset
31:0	base1	Lock region 1 base address	RW	52'b0

5.3.4.35 por_hnf_slc_lock_base2

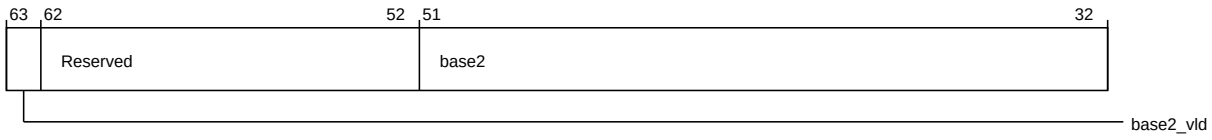
Functions as the base register for lock region 2 [47:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-372: por_hnf_por_hnf_slc_lock_base2 (high)



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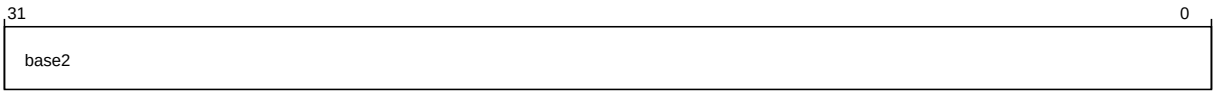
The following table shows the por_hnf_slc_lock_base2 higher register bit assignments.

Table 5-386: por_hnf_por_hnf_slc_lock_base2 (high)

Bits	Field name	Description	Type	Reset
63	base2_vld	Lock region 2 base valid	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	base2	Lock region 2 base address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-373: por_hnf_por_hnf_slc_lock_base2 (low)



The following table shows the por_hnf_slc_lock_base2 lower register bit assignments.

Table 5-387: por_hnf_por_hnf_slc_lock_base2 (low)

Bits	Field name	Description	Type	Reset
31:0	base2	Lock region 2 base address	RW	52'b0

5.3.4.36 por_hnf_slc_lock_base3

Functions as the base register for lock region 3 [47:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

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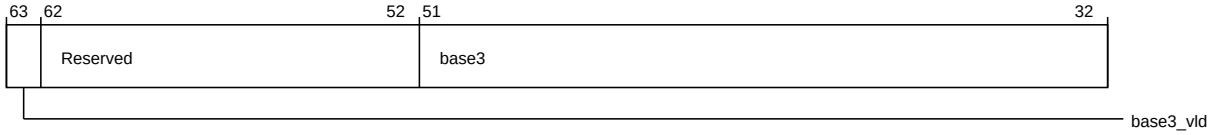
Figure 5-374: por_hnf_por_hnf_slc_lock_base3 (high)



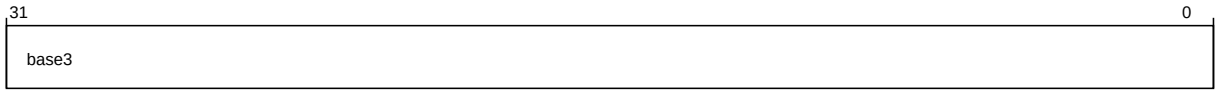
The following table shows the por_hnf_slc_lock_base3 higher register bit assignments.

Table 5-388: por_hnf_por_hnf_slc_lock_base3 (high)

Bits	Field name	Description	Type	Reset
63	base3_vld	Lock region 3 base valid	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	base3	Lock region 3 base address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-375: por_hnf_por_hnf_slc_lock_base3 (low)



The following table shows the por_hnf_slc_lock_base3 lower register bit assignments.

Table 5-389: por_hnf_por_hnf_slc_lock_base3 (low)

Bits	Field name	Description	Type	Reset
31:0	base3	Lock region 3 base address	RW	52'b0

5.3.4.37 por_hnf_rni_region_vec

Functions as the control register for RN-I source SLC way allocation.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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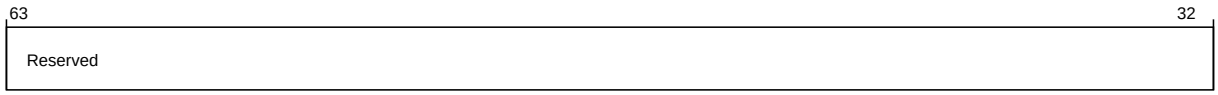
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-376: por_hnf_por_hnf_rni_region_vec (high)



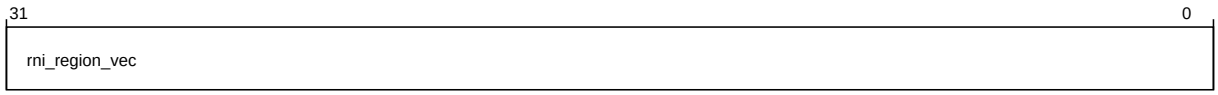
The following table shows the por_hnf_rni_region_vec higher register bit assignments.

Table 5-390: por_hnf_por_hnf_rni_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-377: por_hnf_por_hnf_rni_region_vec (low)



The following table shows the por_hnf_rni_region_vec lower register bit assignments.

Table 5-391: por_hnf_por_hnf_rni_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_region_vec	Bit vector mask; identifies which logical IDs of the RN-Is to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

5.3.4.38 por_hnf_rnd_region_vec

Functions as the control register for RN-D source SLC way allocation.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC30
Register reset 64'b0

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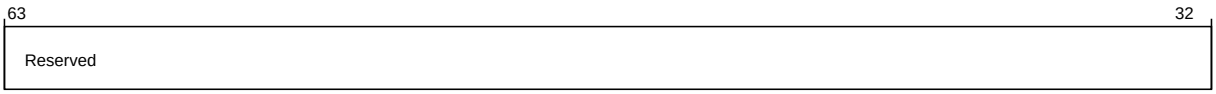
Usage constraints Only accessible by Secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-378: por_hnf_por_hnf_rnd_region_vec (high)



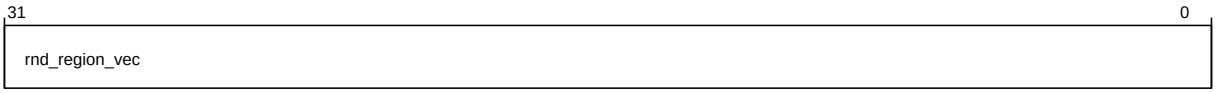
The following table shows the por_hnf_rnd_region_vec higher register bit assignments.

Table 5-392: por_hnf_por_hnf_rnd_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-379: por_hnf_por_hnf_rnd_region_vec (low)



The following table shows the por_hnf_rnd_region_vec lower register bit assignments.

Table 5-393: por_hnf_por_hnf_rnd_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_region_vec	Bit vector mask; identifies which logical IDs of the RN-Ds to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

5.3.4.39 por_hnf_rnf_region_vec

Functions as the control register for RN-F source SLC way allocation.

Its characteristics are:

Type RW
Register width (Bits) 64

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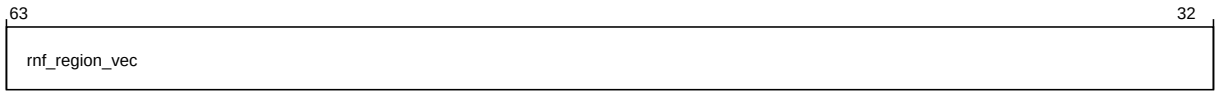
Address offset 16'hC38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-380: por_hnf_por_hnf_rnf_region_vec (high)



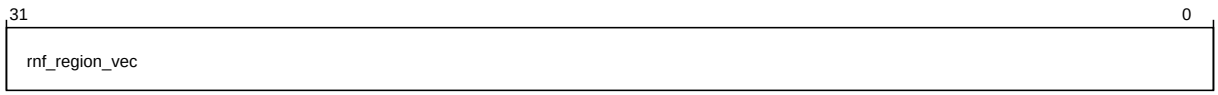
The following table shows the por_hnf_rnf_region_vec higher register bit assignments.

Table 5-394: por_hnf_por_hnf_rnf_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-381: por_hnf_por_hnf_rnf_region_vec (low)



The following table shows the por_hnf_rnf_region_vec lower register bit assignments.

Table 5-395: por_hnf_por_hnf_rnf_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

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5.3.4.40 por_hnf_rnf_region_vec1

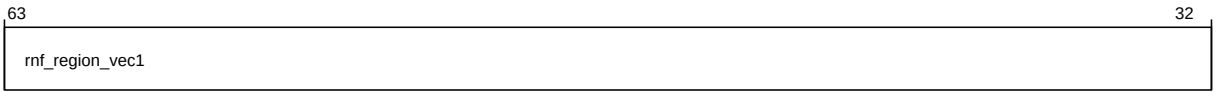
Functions as the control register for RN-F source SLC way allocation for logical IDs 64 through 127.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-382: por_hnf_por_hnf_rnf_region_vec1 (high)



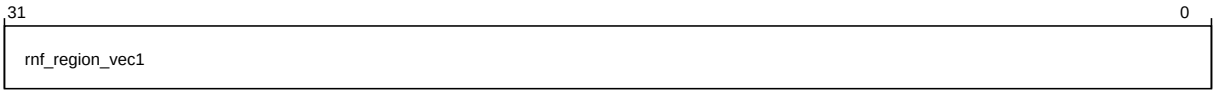
The following table shows the por_hnf_rnf_region_vec1 higher register bit assignments.

Table 5-396: por_hnf_por_hnf_rnf_region_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-383: por_hnf_por_hnf_rnf_region_vec1 (low)



The following table shows the por_hnf_rnf_region_vec1 lower register bit assignments.

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Table 5-397: por_hnf_por_hnf_rnf_region_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

5.3.4.41 por_hnf_slcway_partition0_rnf_vec

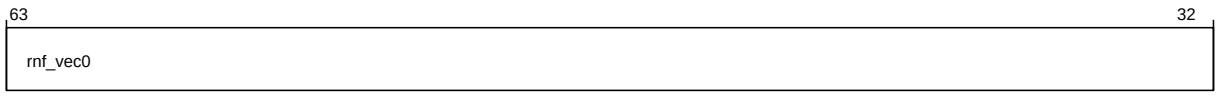
Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC48
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-384: por_hnf_por_hnf_slcway_partition0_rnf_vec (high)



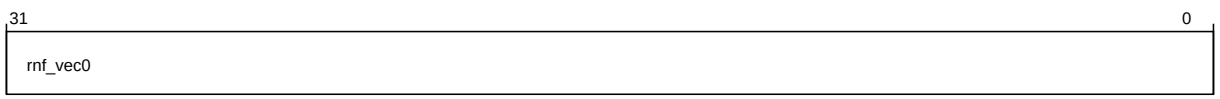
The following table shows the por_hnf_slcway_partition0_rnf_vec higher register bit assignments.

Table 5-398: por_hnf_por_hnf_slcway_partition0_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-385: por_hnf_por_hnf_slcway_partition0_rnf_vec (low)



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The following table shows the por_hnf_slcway_partition0_rnf_vec lower register bit assignments.

Table 5-399: por_hnf_por_hnf_slcway_partition0_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.42 por_hnf_slcway_partition1_rnf_vec

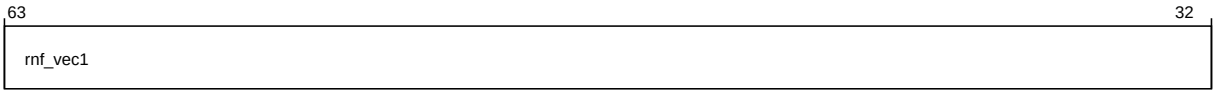
Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC50
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-386: por_hnf_por_hnf_slcway_partition1_rnf_vec (high)



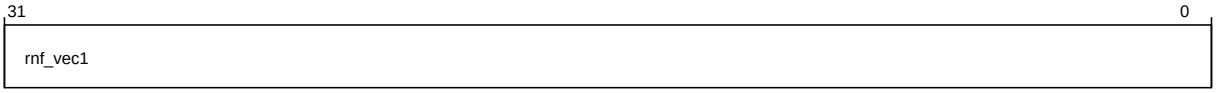
The following table shows the por_hnf_slcway_partition1_rnf_vec higher register bit assignments.

Table 5-400: por_hnf_por_hnf_slcway_partition1_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-387: por_hnf_por_hnf_slcway_partition1_rnf_vec (low)



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The following table shows the por_hnf_slcway_partition1_rnf_vec lower register bit assignments.

Table 5-401: por_hnf_por_hnf_slcway_partition1_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.43 por_hnf_slcway_partition2_rnf_vec

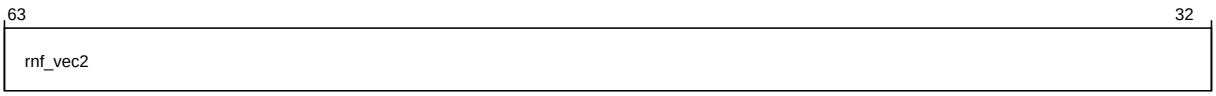
Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC58
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-388: por_hnf_por_hnf_slcway_partition2_rnf_vec (high)



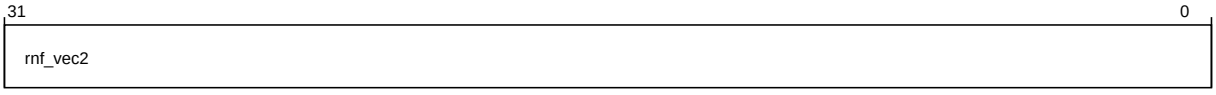
The following table shows the por_hnf_slcway_partition2_rnf_vec higher register bit assignments.

Table 5-402: por_hnf_por_hnf_slcway_partition2_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-389: por_hnf_por_hnf_slcway_partition2_rnf_vec (low)



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The following table shows the por_hnf_slcway_partition2_rnf_vec lower register bit assignments.

Table 5-403: por_hnf_por_hnf_slcway_partition2_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.44 por_hnf_slcway_partition3_rnf_vec

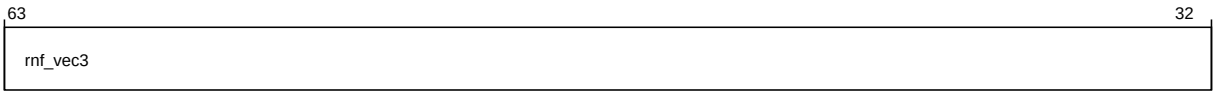
Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC60
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-390: por_hnf_por_hnf_slcway_partition3_rnf_vec (high)



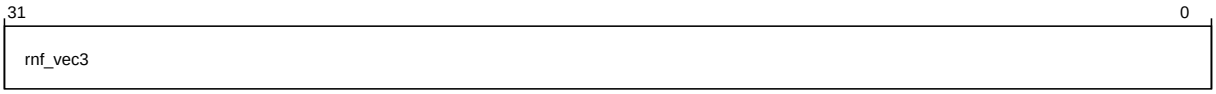
The following table shows the por_hnf_slcway_partition3_rnf_vec higher register bit assignments.

Table 5-404: por_hnf_por_hnf_slcway_partition3_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-391: por_hnf_por_hnf_slcway_partition3_rnf_vec (low)



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The following table shows the por_hnf_slcway_partition3_rnf_vec lower register bit assignments.

Table 5-405: por_hnf_por_hnf_slcway_partition3_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.45 por_hnf_slcway_partition0_rnf_vec1

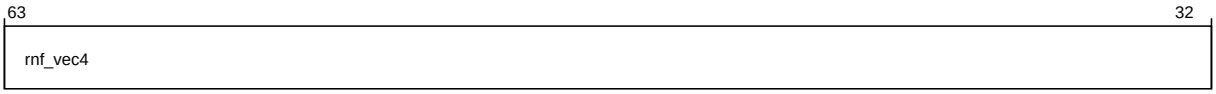
Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB0
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-392: por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)



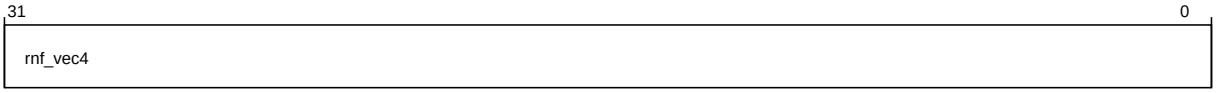
The following table shows the por_hnf_slcway_partition0_rnf_vec1 higher register bit assignments.

Table 5-406: por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-393: por_hnf_por_hnf_slcway_partition0_rnf_vec1 (low)



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The following table shows the por_hnf_slcway_partition0_rnf_vec1 lower register bit assignments.

Table 5-407: por_hnf_por_hnf_slcway_partition0_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.46 por_hnf_slcway_partition1_rnf_vec1

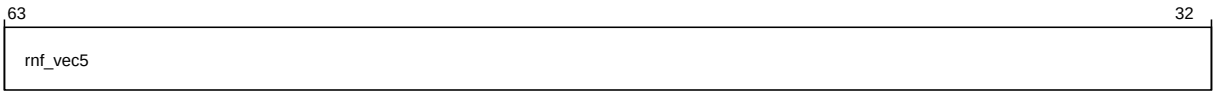
Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB8
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-394: por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)



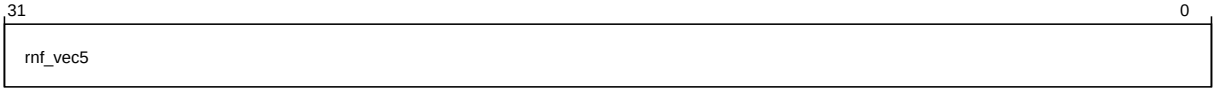
The following table shows the por_hnf_slcway_partition1_rnf_vec1 higher register bit assignments.

Table 5-408: por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-395: por_hnf_por_hnf_slcway_partition1_rnf_vec1 (low)



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The following table shows the por_hnf_slcway_partition1_rnf_vec1 lower register bit assignments.

Table 5-409: por_hnf_por_hnf_slcway_partition1_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.47 por_hnf_slcway_partition2_rnf_vec1

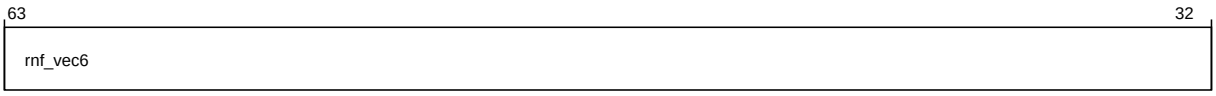
Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC0
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-396: por_hnf_por_hnf_slcway_partition2_rnf_vec1 (high)



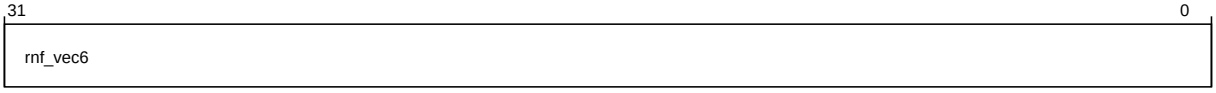
The following table shows the por_hnf_slcway_partition2_rnf_vec1 higher register bit assignments.

Table 5-410: por_hnf_por_hnf_slcway_partition2_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-397: por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)



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The following table shows the por_hnf_slcway_partition2_rnf_vec1 lower register bit assignments.

Table 5-411: por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.48 por_hnf_slcway_partition3_rnf_vec1

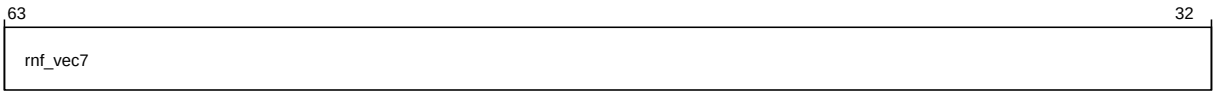
Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15) for Logical RNF IDs 64 to 127.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC8
Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-398: por_hnf_por_hnf_slcway_partition3_rnf_vec1 (high)



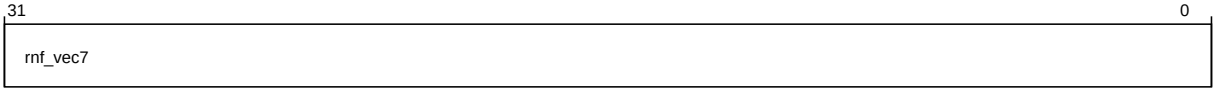
The following table shows the por_hnf_slcway_partition3_rnf_vec1 higher register bit assignments.

Table 5-412: por_hnf_por_hnf_slcway_partition3_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-399: por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)



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The following table shows the por_hnf_slcway_partition3_rnf_vec1 lower register bit assignments.

Table 5-413: por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

5.3.4.49 por_hnf_slcway_partition0_rni_vec

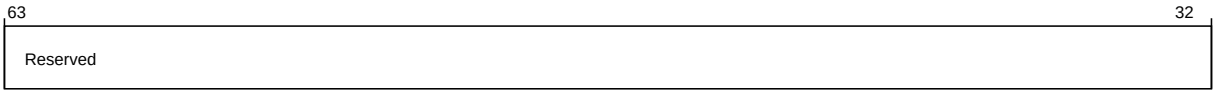
Functions as the control register for RN-Is that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC68
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-400: por_hnf_por_hnf_slcway_partition0_rni_vec (high)



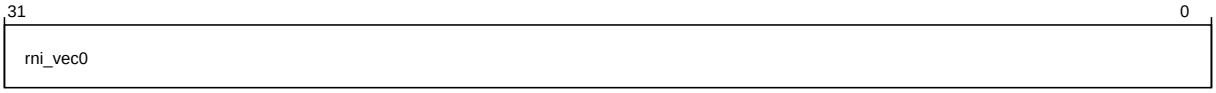
The following table shows the por_hnf_slcway_partition0_rni_vec higher register bit assignments.

Table 5-414: por_hnf_por_hnf_slcway_partition0_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-401: por_hnf_por_hnf_slcway_partition0_rni_vec (low)



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The following table shows the por_hnf_slcway_partition0_rni_vec lower register bit assignments.

Table 5-415: por_hnf_por_hnf_slcway_partition0_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.50 por_hnf_slcway_partition1_rni_vec

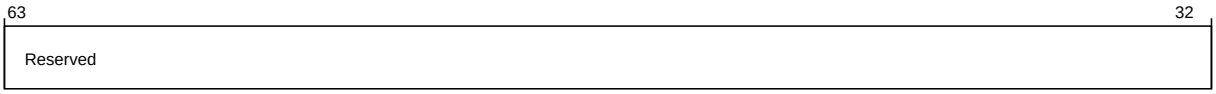
Functions as the control register for RN-Is that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC70
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-402: por_hnf_por_hnf_slcway_partition1_rni_vec (high)



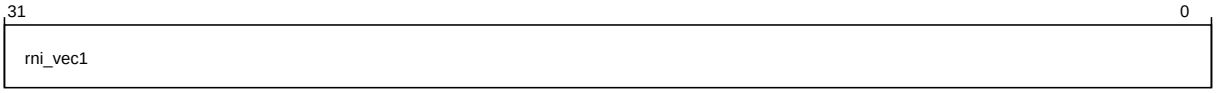
The following table shows the por_hnf_slcway_partition1_rni_vec higher register bit assignments.

Table 5-416: por_hnf_por_hnf_slcway_partition1_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-403: por_hnf_por_hnf_slcway_partition1_rni_vec (low)



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The following table shows the por_hnf_slcway_partition1_rni_vec lower register bit assignments.

Table 5-417: por_hnf_por_hnf_slcway_partition1_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.51 por_hnf_slcway_partition2_rni_vec

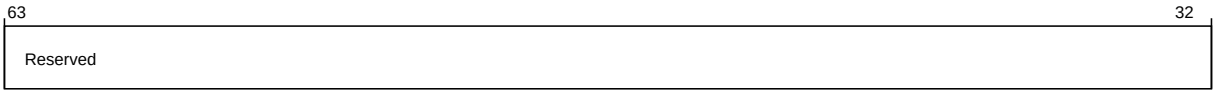
Functions as the control register for RN-Is that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC78
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-404: por_hnf_por_hnf_slcway_partition2_rni_vec (high)



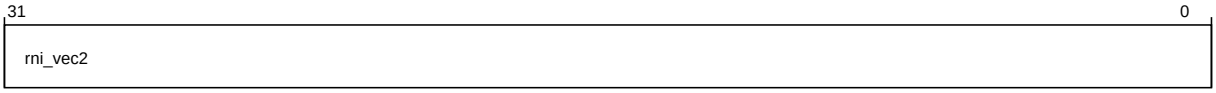
The following table shows the por_hnf_slcway_partition2_rni_vec higher register bit assignments.

Table 5-418: por_hnf_por_hnf_slcway_partition2_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-405: por_hnf_por_hnf_slcway_partition2_rni_vec (low)



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The following table shows the por_hnf_slcway_partition2_rni_vec lower register bit assignments.

Table 5-419: por_hnf_por_hnf_slcway_partition2_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.52 por_hnf_slcway_partition3_rni_vec

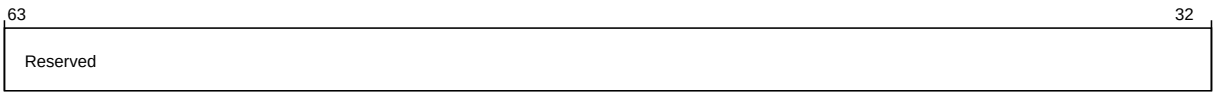
Functions as the control register for RN-Is that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC80
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-406: por_hnf_por_hnf_slcway_partition3_rni_vec (high)



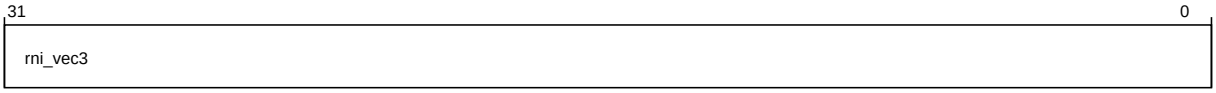
The following table shows the por_hnf_slcway_partition3_rni_vec higher register bit assignments.

Table 5-420: por_hnf_por_hnf_slcway_partition3_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-407: por_hnf_por_hnf_slcway_partition3_rni_vec (low)



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The following table shows the por_hnf_slcway_partition3_rni_vec lower register bit assignments.

Table 5-421: por_hnf_por_hnf_slcway_partition3_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.53 por_hnf_slcway_partition0_rnd_vec

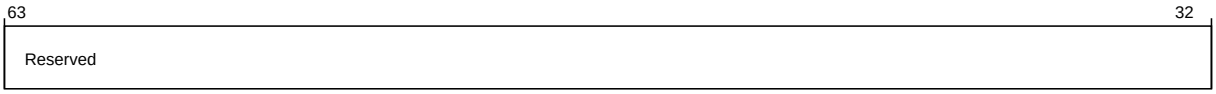
Functions as the control register for RN-Ds that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC88
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-408: por_hnf_por_hnf_slcway_partition0_rnd_vec (high)



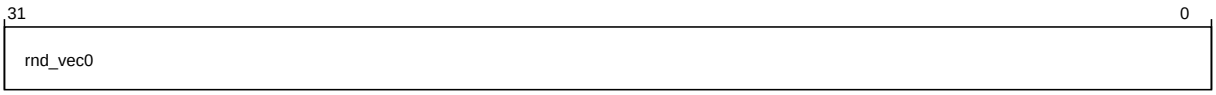
The following table shows the por_hnf_slcway_partition0_rnd_vec higher register bit assignments.

Table 5-422: por_hnf_por_hnf_slcway_partition0_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-409: por_hnf_por_hnf_slcway_partition0_rnd_vec (low)



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The following table shows the por_hnf_slcway_partition0_rnd_vec lower register bit assignments.

Table 5-423: por_hnf_por_hnf_slcway_partition0_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.54 por_hnf_slcway_partition1_rnd_vec

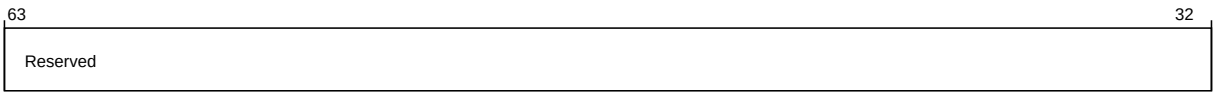
Functions as the control register for RN-Ds that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC90
Register reset 64'b1111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-410: por_hnf_por_hnf_slcway_partition1_rnd_vec (high)



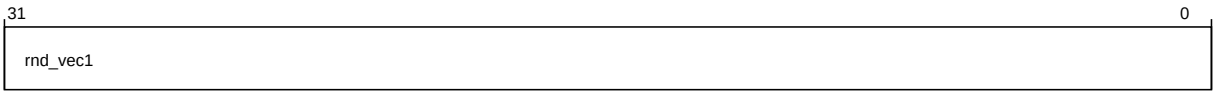
The following table shows the por_hnf_slcway_partition1_rnd_vec higher register bit assignments.

Table 5-424: por_hnf_por_hnf_slcway_partition1_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-411: por_hnf_por_hnf_slcway_partition1_rnd_vec (low)



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The following table shows the por_hnf_slcway_partition1_rnd_vec lower register bit assignments.

Table 5-425: por_hnf_por_hnf_slcway_partition1_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.55 por_hnf_slcway_partition2_rnd_vec

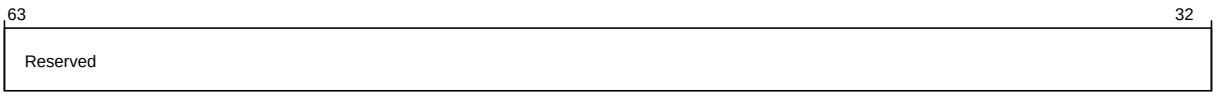
Functions as the control register for RN-Ds that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC98
Register reset 64'b1111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-412: por_hnf_por_hnf_slcway_partition2_rnd_vec (high)



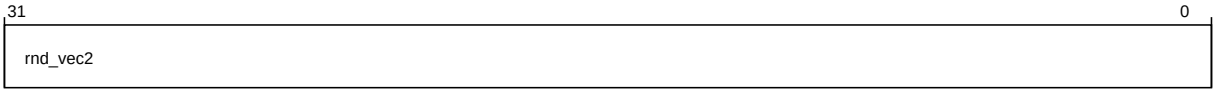
The following table shows the por_hnf_slcway_partition2_rnd_vec higher register bit assignments.

Table 5-426: por_hnf_por_hnf_slcway_partition2_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-413: por_hnf_por_hnf_slcway_partition2_rnd_vec (low)



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The following table shows the por_hnf_slcway_partition2_rnd_vec lower register bit assignments.

Table 5-427: por_hnf_por_hnf_slcway_partition2_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.56 por_hnf_slcway_partition3_rnd_vec

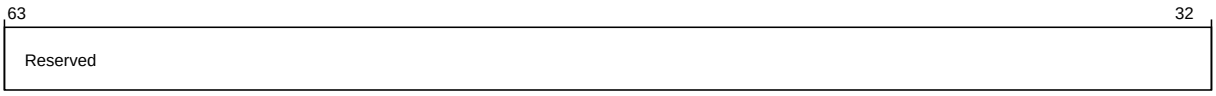
Functions as the control register for RN-Ds that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCA0
Register reset 64'b1111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-414: por_hnf_por_hnf_slcway_partition3_rnd_vec (high)



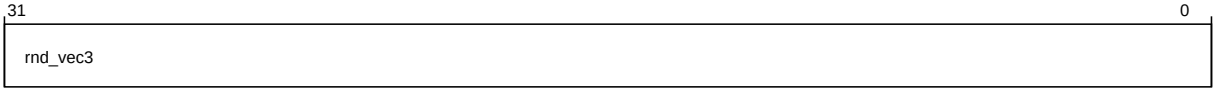
The following table shows the por_hnf_slcway_partition3_rnd_vec higher register bit assignments.

Table 5-428: por_hnf_por_hnf_slcway_partition3_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-415: por_hnf_por_hnf_slcway_partition3_rnd_vec (low)



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The following table shows the por_hnf_slcway_partition3_rnd_vec lower register bit assignments.

Table 5-429: por_hnf_por_hnf_slcway_partition3_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

5.3.4.57 por_hnf_rn_region_lock

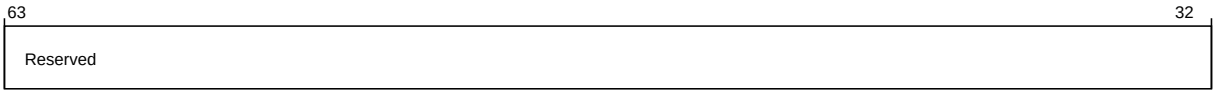
Functions as the enable register for source-based SLC way allocation.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following figure shows the higher register bit assignments.

Figure 5-416: por_hnf_por_hnf_rn_region_lock (high)



The following table shows the por_hnf_rn_region_lock higher register bit assignments.

Table 5-430: por_hnf_por_hnf_rn_region_lock (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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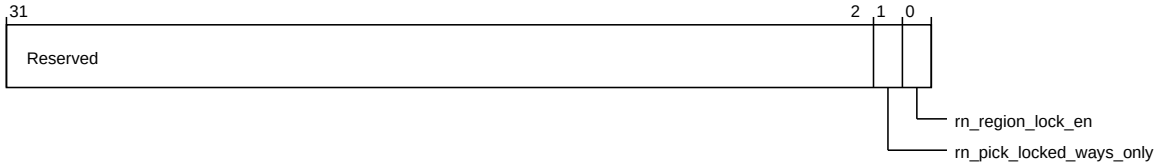
Figure 5-417: por_hnf_por_hnf_rn_region_lock (low)



The following table shows the por_hnf_rn_region_lock lower register bit assignments.

Table 5-431: por_hnf_por_hnf_rn_region_lock (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	rn_pick_locked_ways_only	Specifies which ways the programmed RNs can allocate new cache lines to 1'b0: Programmed RN will choose all ways including locked 1'b1: Programmed RN will only allocate in locked ways	RW	1'b0
0	rn_region_lock_en	Enables SRC-based region locking 1'b0: SRC based way locking is disabled 1'b1: SRC based way locking is enabled	RW	1'b0

5.3.4.58 por_hnf_sf_cxg_blocked_ways

Specifies the SF ways that are blocked for remote chip to use in CML mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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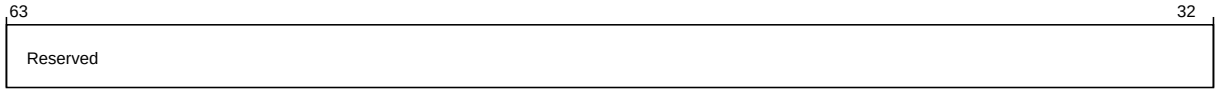
Figure 5-418: por_hnf_por_hnf_sf_cxg_blocked_ways (high)



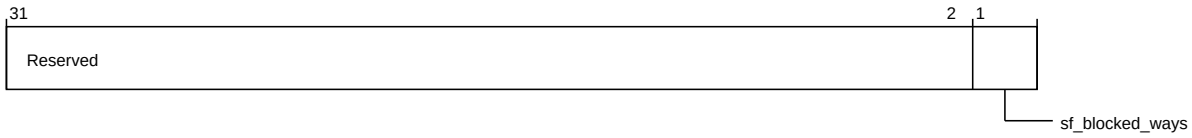
The following table shows the por_hnf_sf_cxg_blocked_ways higher register bit assignments.

Table 5-432: por_hnf_por_hnf_sf_cxg_blocked_ways (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-419: por_hnf_por_hnf_sf_cxg_blocked_ways (low)



The following table shows the por_hnf_sf_cxg_blocked_ways lower register bit assignments.

Table 5-433: por_hnf_por_hnf_sf_cxg_blocked_ways (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	sf_blocked_ways	Number of SF ways blocked for remote chips to use in CML mode (0, 4, 8, or 12) 2'b00: No ways are blocked; all 16 SF ways could be used by local or remote RN-Fs 2'b01: Lower 4 ways are blocked from remote RN-Fs; ways 3:0 for local RN-Fs only; ways 15:4 for local and remote RN-Fs 2'b10: Lower 8 ways are blocked from remote RN-Fs; ways 7:0 for local RN-Fs only; ways 15:8 for local and remote RN-Fs 2'b11: Lower 12 ways are blocked from remote RN-Fs; ways 11:0 for local RN-Fs only; ways 15:12 for local and remote RN-Fs	RW	2'b00

5.3.4.59 hn_sam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

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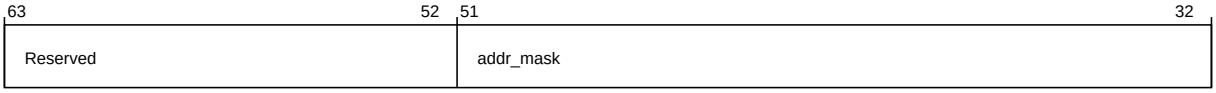
Type RW
Register width (Bits) 64
Address offset 16'hCF0
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-420: por_hnf_hn_sam_hash_addr_mask_reg (high)



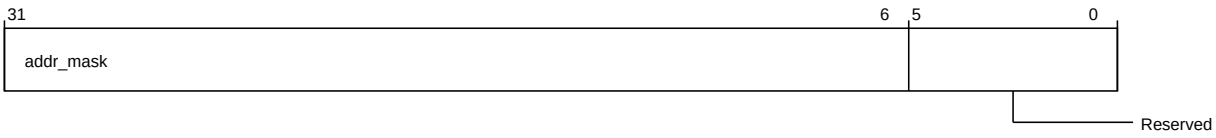
The following table shows the hn_sam_hash_addr_mask_reg higher register bit assignments.

Table 5-434: por_hnf_hn_sam_hash_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-421: por_hnf_hn_sam_hash_addr_mask_reg (low)



The following table shows the hn_sam_hash_addr_mask_reg lower register bit assignments.

Table 5-435: por_hnf_hn_sam_hash_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFFF
5:0	Reserved	Reserved	RO	-

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5.3.4.60 hn_sam_region_cmp_addr_mask_reg

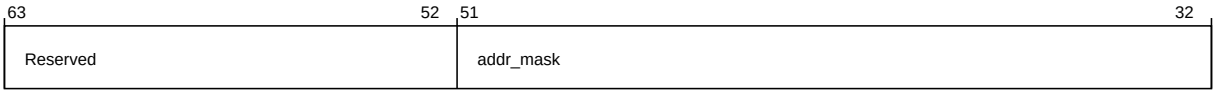
Configures the address mask that is applied before memory region compare.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCF8
Register reset 64'b1111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-422: por_hnf_hn_sam_region_cmp_addr_mask_reg (high)



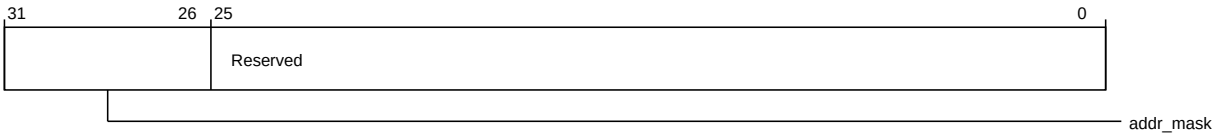
The following table shows the hn_sam_region_cmp_addr_mask_reg higher register bit assignments.

Table 5-436: por_hnf_hn_sam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask applied before memory region compare	RW	26'h3FFFFF

The following figure shows the lower register bit assignments.

Figure 5-423: por_hnf_hn_sam_region_cmp_addr_mask_reg (low)



The following table shows the hn_sam_region_cmp_addr_mask_reg lower register bit assignments.

Table 5-437: por_hnf_hn_sam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:26	addr_mask	Address mask applied before memory region compare	RW	26'h3FFFFF

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Bits	Field name	Description	Type	Reset
25:0	Reserved	Reserved	RO	-

5.3.4.61 por_hnf_sam_control

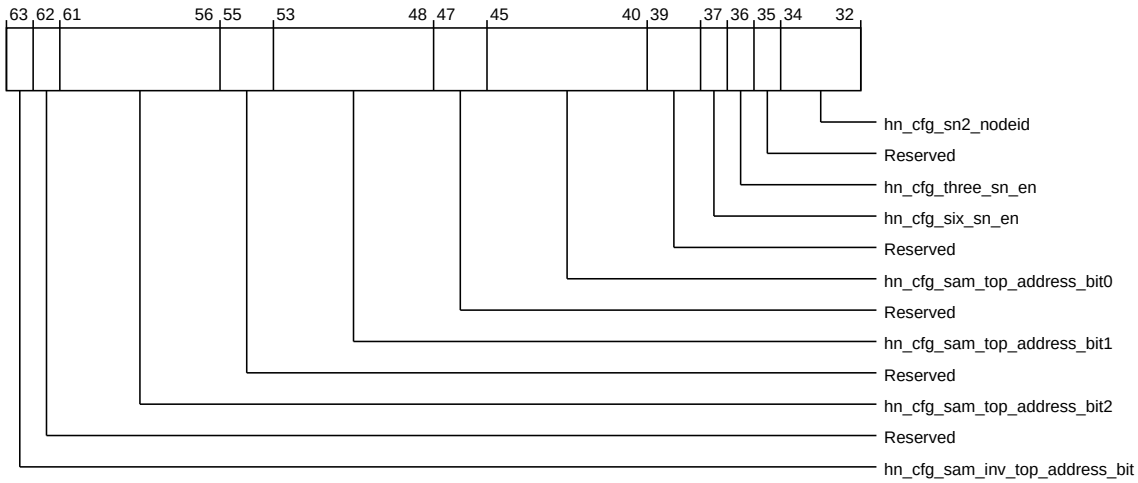
Configures HN-F SAM. All top_address_bit fields must be between bits 47 and 28 of the address. top_address_bit2 > top_address_bit1 > top_address_bit0. Must be configured to match corresponding por_rnsam_sys_cache_grp_sn_sam_cfgN register in the RN SAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-424: por_hnf_por_hnf_sam_control (high)



The following table shows the por_hnf_sam_control higher register bit assignments.

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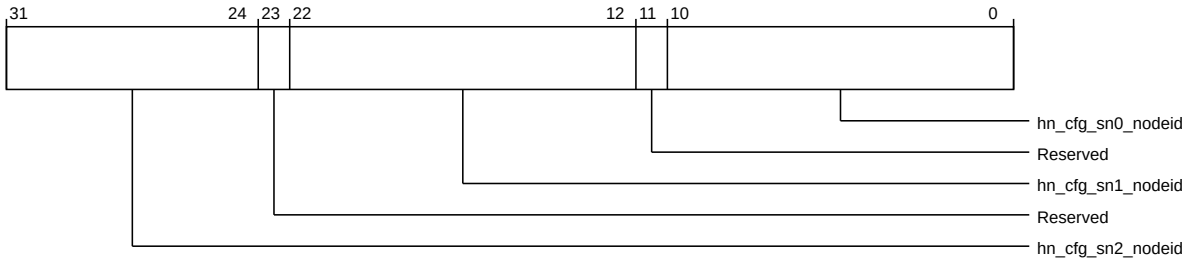
Table 5-438: por_hnf_por_hnf_sam_control (high)

Bits	Field name	Description	Type	Reset
63	hn_cfg_sam_inv_top_address_bit	Inverts the top address bit (hn_cfg_sam_top_address_bit1 if 3-SN, hn_cfg_sam_top_address_bit2 if 6-SN) NOTE: Can only be used when the address map does not have unique address bit combinations.	RW	1'h0
62	Reserved	Reserved	RO	-
61:56	hn_cfg_sam_top_address_bit2	Bit position of top_address_bit2; used for address hashing in 6-SN configuration	RW	6'h00
55:54	Reserved	Reserved	RO	-
53:48	hn_cfg_sam_top_address_bit1	Bit position of top_address_bit1; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
47:46	Reserved	Reserved	RO	-
45:40	hn_cfg_sam_top_address_bit0	Bit position of top_address_bit0; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
39:38	Reserved	Reserved	RO	-
37	hn_cfg_six_sn_en	Enables 6-SN configuration	RW	1'b0
36	hn_cfg_three_sn_en	Enables 3-SN configuration	RW	1'b0
35	Reserved	Reserved	RO	-
34:32	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-425: por_hnf_por_hnf_sam_control (low)



The following table shows the por_hnf_sam_control lower register bit assignments.

Table 5-439: por_hnf_por_hnf_sam_control (low)

Bits	Field name	Description	Type	Reset
31:24	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0
23	Reserved	Reserved	RO	-
22:12	hn_cfg_sn1_nodeid	SN 1 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	hn_cfg_sn0_nodeid	SN 0 node ID	RW	11'h0

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5.3.4.62 por_hnf_sam_memregion0

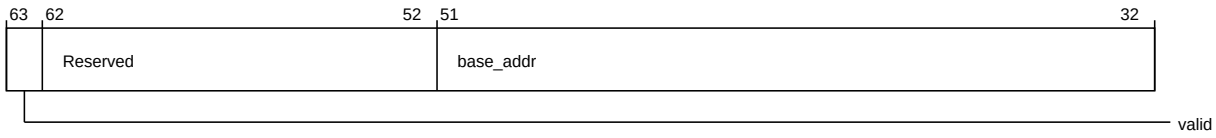
Configures range-based memory region 0 in HN-F SAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-426: por_hnf_por_hnf_sam_memregion0 (high)



The following table shows the por_hnf_sam_memregion0 higher register bit assignments.

Table 5-440: por_hnf_por_hnf_sam_memregion0 (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:52	Reserved	Reserved	RO	-
51:32	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	26'h0

The following figure shows the lower register bit assignments.

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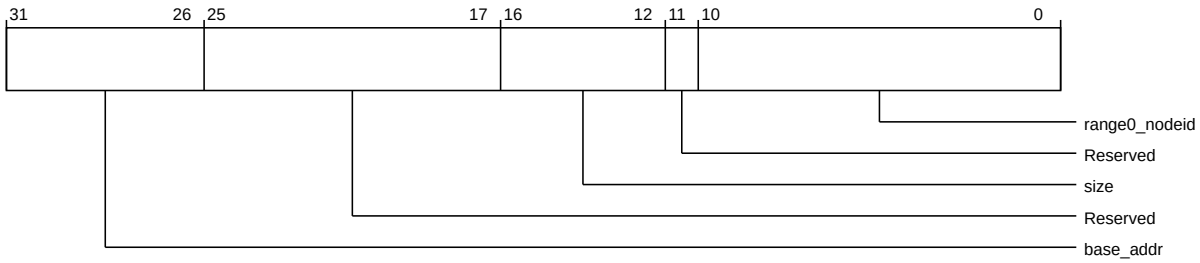
Figure 5-427: por_hnf_por_hnf_sam_memregion0 (low)



The following table shows the por_hnf_sam_memregion0 lower register bit assignments.

Table 5-441: por_hnf_por_hnf_sam_memregion0 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	26'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'h0
11	Reserved	Reserved	RO	-
10:0	range0_nodeid	Memory region 0 target node ID	RW	11'h0

5.3.4.63 por_hnf_sam_memregion1

Configures range-based memory region 1 in HN-F SAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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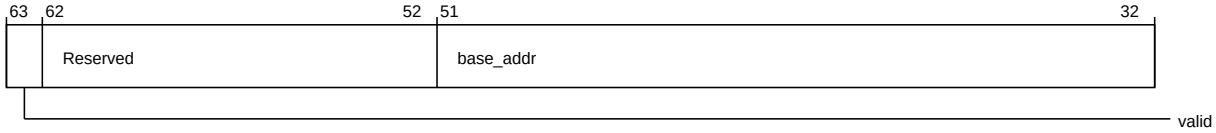
Figure 5-428: por_hnf_por_hnf_sam_memregion1 (high)



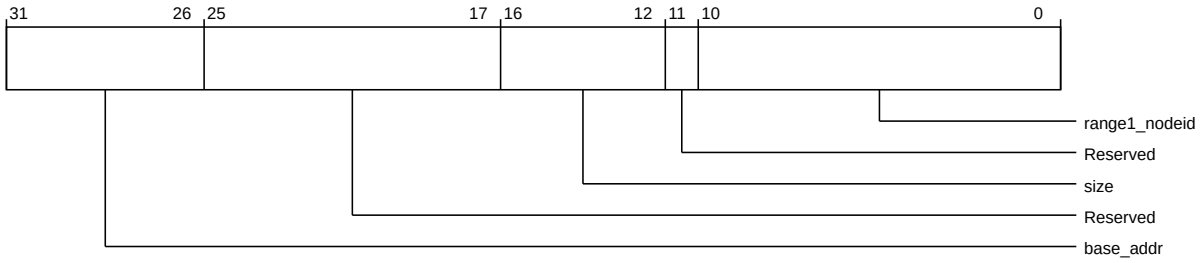
The following table shows the por_hnf_sam_memregion1 higher register bit assignments.

Table 5-442: por_hnf_por_hnf_sam_memregion1 (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:52	Reserved	Reserved	RO	-
51:32	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	26'h0

The following figure shows the lower register bit assignments.

Figure 5-429: por_hnf_por_hnf_sam_memregion1 (low)



The following table shows the por_hnf_sam_memregion1 lower register bit assignments.

Table 5-443: por_hnf_por_hnf_sam_memregion1 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	26'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'h0

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Bits	Field name	Description	Type	Reset
11	Reserved	Reserved	RO	-
10:0	range1_nodeid	Memory region 1 target node ID	RW	11'h0

5.3.4.64 por_hnf_sam_sn_properties

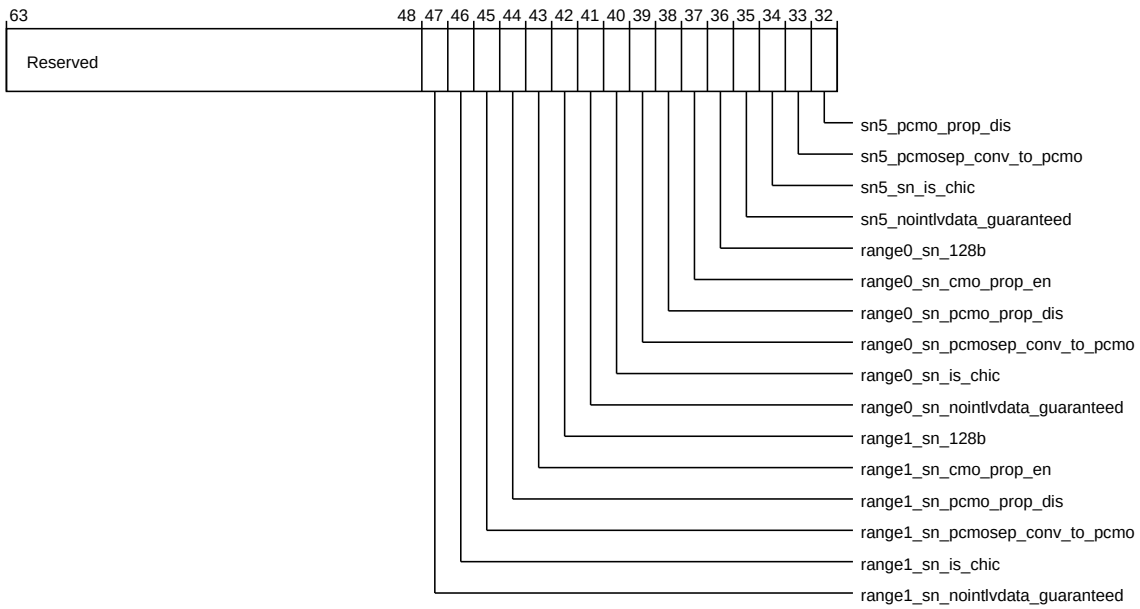
Configures properties for all six SN targets and two range-based SN targets.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-430: por_hnf_por_hnf_sam_sn_properties (high)



The following table shows the por_hnf_sam_sn_properties higher register bit assignments.

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Table 5-444: por_hnf_por_hnf_sam_sn_properties (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47	range1_sn_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
46	range1_sn_is_chic	Indicates that the range 1 SN is a CHI-C SN when set	RW	1'b0
45	range1_sn_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for range 1 SN when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
44	range1_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 1 SN when set	RW	1'b0
43	range1_sn_cmo_prop_en	Enables CMO propagation for range 1 SN	RW	1'b0
42	range1_sn_128b	Data width of range 1 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
41	range0_sn_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
40	range0_sn_is_chic	Indicates that the range 0 SN is a CHI-C SN when set	RW	1'b0
39	range0_sn_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for range 0 SN when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
38	range0_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 0 SN when set	RW	1'b0
37	range0_sn_cmo_prop_en	Enables CMO propagation for range 0 SN	RW	1'b0
36	range0_sn_128b	Data width of range 0 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
35	sn5_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
34	sn5_sn_is_chic	Indicates that SN5 is a CHI-C SN when set	RW	1'b0
33	sn5_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 5 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
32	sn5_pcmo_prop_dis	Disables PCMO propagation for SN 5 when set	RW	1'b0

The following figure shows the lower register bit assignments.

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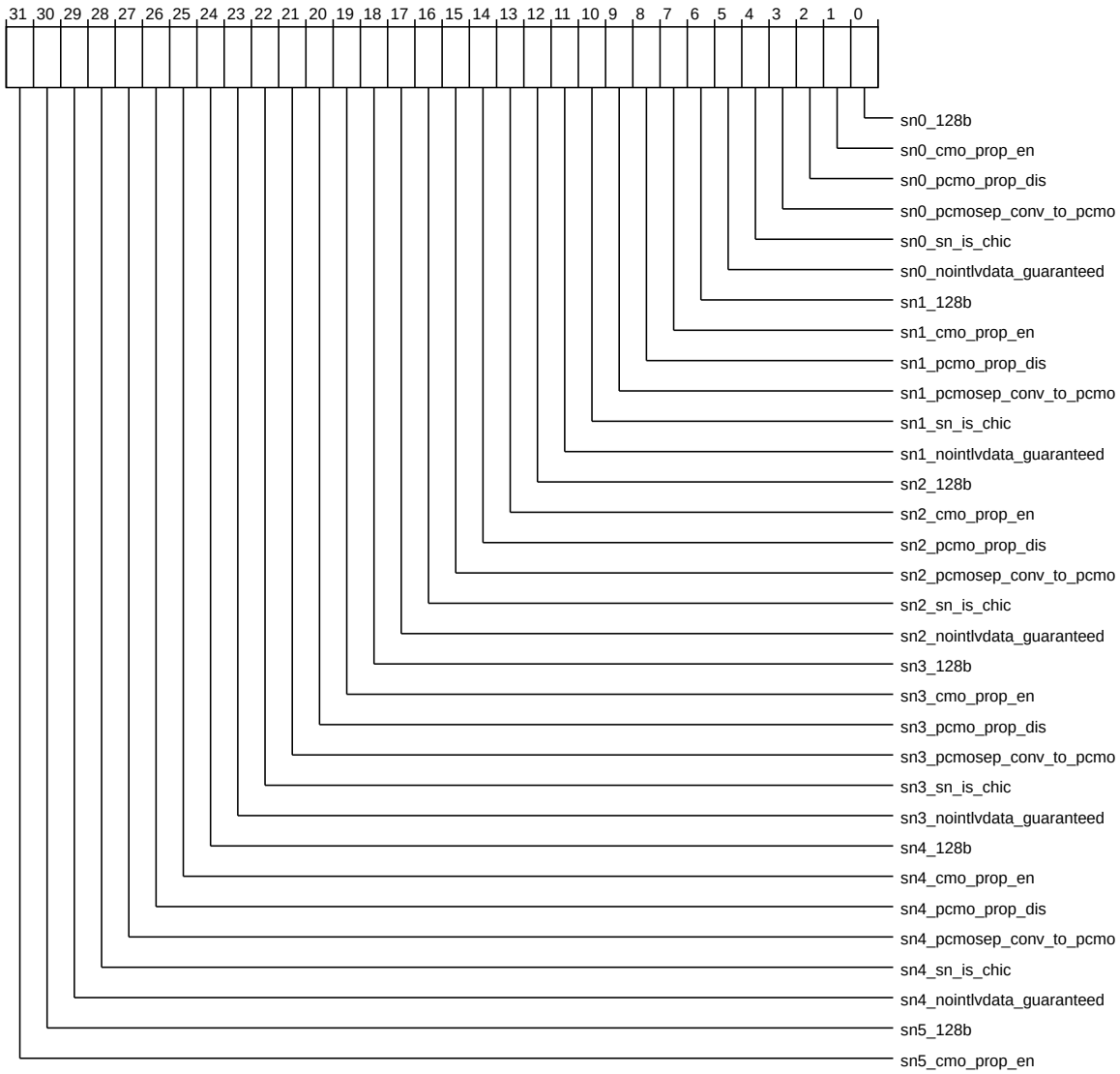
Figure 5-431: por_hnf_por_hnf_sam_sn_properties (low)



The following table shows the por_hnf_sam_sn_properties lower register bit assignments.

Table 5-445: por_hnf_por_hnf_sam_sn_properties (low)

Bits	Field name	Description	Type	Reset
31	sn5_cmo_prop_en	Enables CMO propagation for SN 5 when set	RW	1'b0
30	sn5_128b	Data width of SN 5 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
29	sn4_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
28	sn4_sn_is_chic	Indicates that SN4 is a CHI-C SN when set	RW	1'b0

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Bits	Field name	Description	Type	Reset
27	sn4_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 4 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
26	sn4_pcmo_prop_dis	Disables PCMO propagation for SN 4 when set	RW	1'b0
25	sn4_cmo_prop_en	Enables CMO propagation for SN 4 when set	RW	1'b0
24	sn4_128b	Data width of SN 4 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
23	sn3_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
22	sn3_sn_is_chic	Indicates that SN3 is a CHI-C SN when set	RW	1'b0
21	sn3_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 3 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
20	sn3_pcmo_prop_dis	Disables PCMO propagation for SN 3 when set	RW	1'b0
19	sn3_cmo_prop_en	Enables CMO propagation for SN 3 when set	RW	1'b0
18	sn3_128b	Data width of SN 3 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
17	sn2_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
16	sn2_sn_is_chic	Indicates that SN2 is a CHI-C SN when set	RW	1'b0
15	sn2_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 2 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
14	sn2_pcmo_prop_dis	Disables PCMO propagation for SN 2 when set	RW	1'b0
13	sn2_cmo_prop_en	Enables CMO propagation for SN 2 when set	RW	1'b0
12	sn2_128b	Data width of SN 2 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
11	sn1_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
10	sn1_sn_is_chic	Indicates that SN1 is a CHI-C SN when set	RW	1'b0
9	sn1_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 1 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
8	sn1_pcmo_prop_dis	Disables PCMO propagation for SN 1 when set	RW	1'b0
7	sn1_cmo_prop_en	Enables CMO propagation for SN 1 when set	RW	1'b0
6	sn1_128b	Data width of SN 1 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0

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Bits	Field name	Description	Type	Reset
5	sn0_nointlvdata_guaranteed	SN guaratees the return data will not be interleaved	RW	1'b0
4	sn0_sn_is_chic	Indicates that SN0 is a CHI-C SN when set	RW	1'b0
3	sn0_pcmosep_conv_to_pcmo	Convert CleanSharedPersistSep to CleanSharedPersist for SN 0 when set CONSTRAINT: Should not be enabled when sn_pcmo_prop_dis bit is set to 1	RW	1'b0
2	sn0_pcmo_prop_dis	Disables PCMO propagation for SN 0 when set	RW	1'b0
1	sn0_cmo_prop_en	Enables CMO propagation for SN 0 when set	RW	1'b0
0	sn0_128b	Data width of SN 0 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0

5.3.4.65 por_hnf_sam_6sn_nodeid

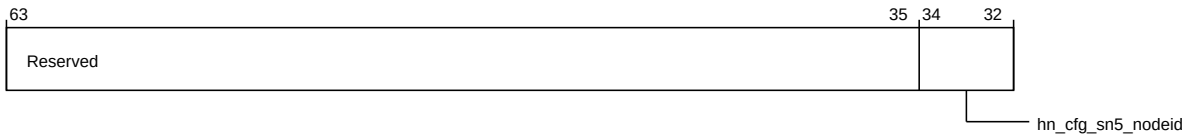
Configures node IDs for slave nodes 3 to 5 in 6-SN configuration mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-432: por_hnf_por_hnf_sam_6sn_nodeid (high)



The following table shows the por_hnf_sam_6sn_nodeid higher register bit assignments.

Table 5-446: por_hnf_por_hnf_sam_6sn_nodeid (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	hn_cfg_sn5_nodeid	SN 5 node ID	RW	11'h0

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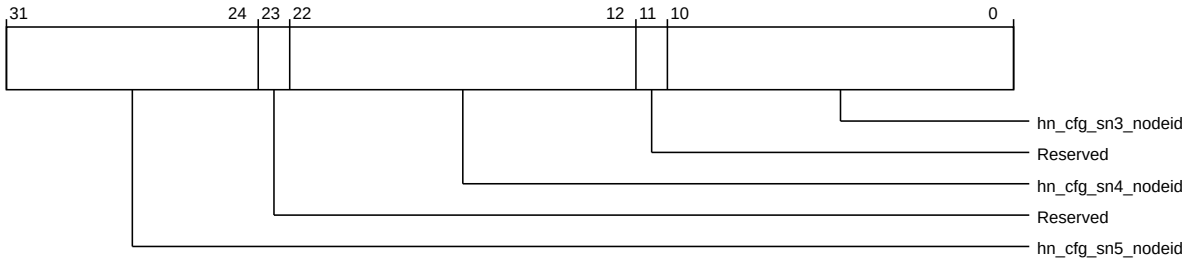
The following figure shows the lower register bit assignments.

Figure 5-433: por_hnf_por_hnf_sam_6sn_nodeid (low)



The following table shows the por_hnf_sam_6sn_nodeid lower register bit assignments.

Table 5-447: por_hnf_por_hnf_sam_6sn_nodeid (low)

Bits	Field name	Description	Type	Reset
31:24	hn_cfg_sn5_nodeid	SN 5 node ID	RW	11'h0
23	Reserved	Reserved	RO	-
22:12	hn_cfg_sn4_nodeid	SN 4 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	hn_cfg_sn3_nodeid	SN 3 node ID	RW	11'h0

5.3.4.66 por_hnf_sam_sn_properties1

Configures additional properties for all six SN targets and two range-based SN targets.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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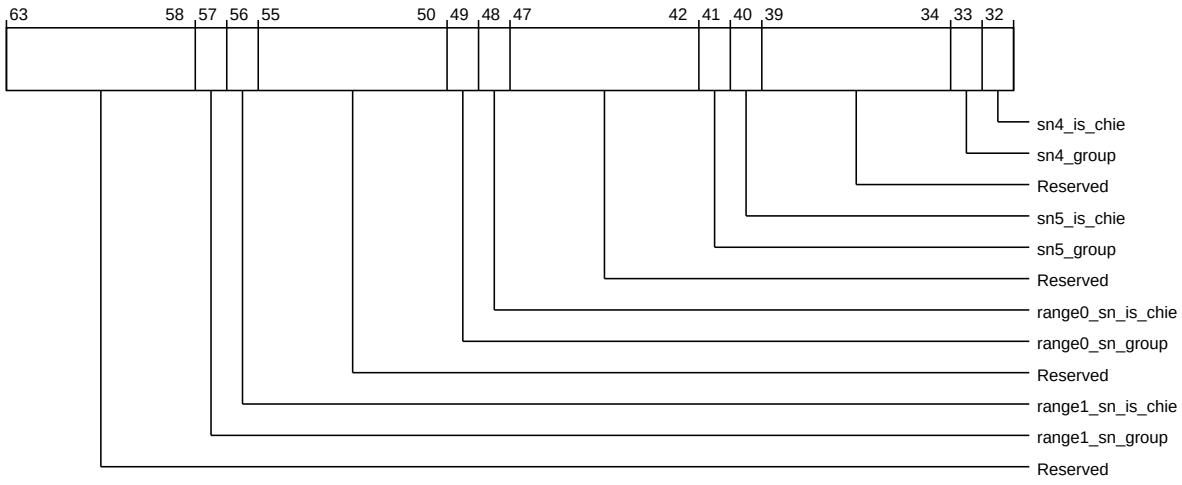
Figure 5-434: por_hnf_por_hnf_sam_sn_properties1 (high)



The following table shows the por_hnf_sam_sn_properties1 higher register bit assignments.

Table 5-448: por_hnf_por_hnf_sam_sn_properties1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57	range1_sn_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
56	range1_sn_is_chie	Range 1 SN supports CHI-E	RW	1'b0
55:50	Reserved	Reserved	RO	-
49	range0_sn_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
48	range0_sn_is_chie	Range 0 SN supports CHI-E	RW	1'b0
47:42	Reserved	Reserved	RO	-
41	sn5_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
40	sn5_is_chie	SN 5 supports CHI-E	RW	1'b0
39:34	Reserved	Reserved	RO	-

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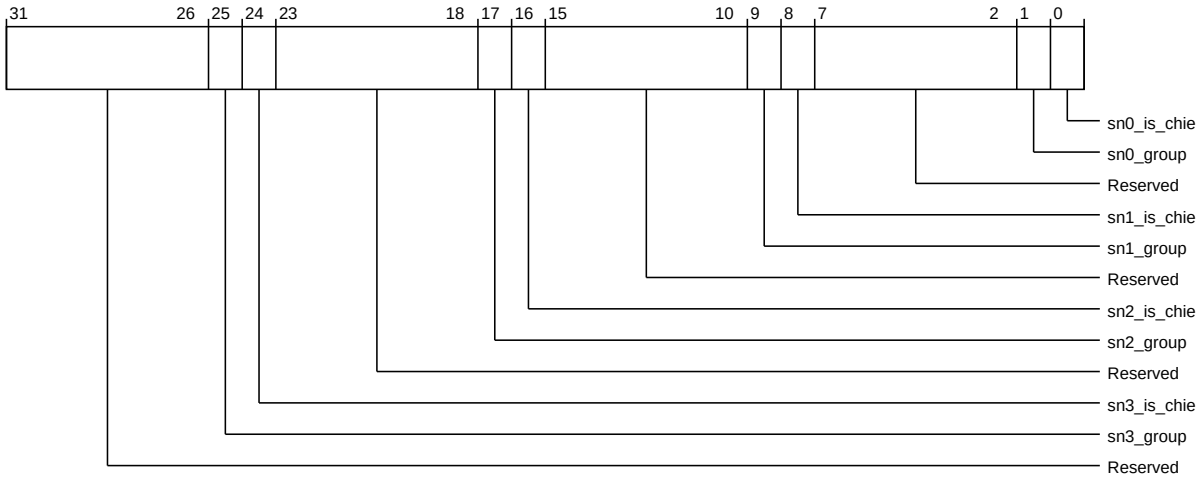
Bits	Field name	Description	Type	Reset
33	sn4_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
32	sn4_is_chie	SN 4 supports CHI-E	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-435: por_hnf_por_hnf_sam_sn_properties1 (low)



The following table shows the por_hnf_sam_sn_properties1 lower register bit assignments.

Table 5-449: por_hnf_por_hnf_sam_sn_properties1 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25	sn3_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
24	sn3_is_chie	SN 3 supports CHI-E	RW	1'b0
23:18	Reserved	Reserved	RO	-
17	sn2_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
16	sn2_is_chie	SN 2 supports CHI-E	RW	1'b0
15:10	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
9	sn1_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
8	sn1_is_chie	SN 1 supports CHI-E	RW	1'b0
7:2	Reserved	Reserved	RO	-
1	sn0_group	Specifies the SN-F grouping 1'b0: Group A 1'b1: Group B	RW	1'b0
0	sn0_is_chie	SN 0 supports CHI-E	RW	1'b0

5.3.4.67 por_hnf_rn_phys_id0

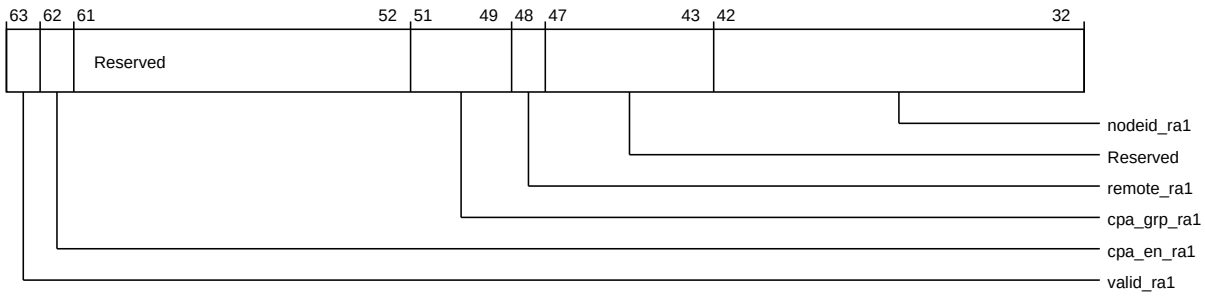
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-436: por_hnf_por_hnf_rn_phys_id0 (high)



The following table shows the por_hnf_rn_phys_id0 higher register bit assignments.

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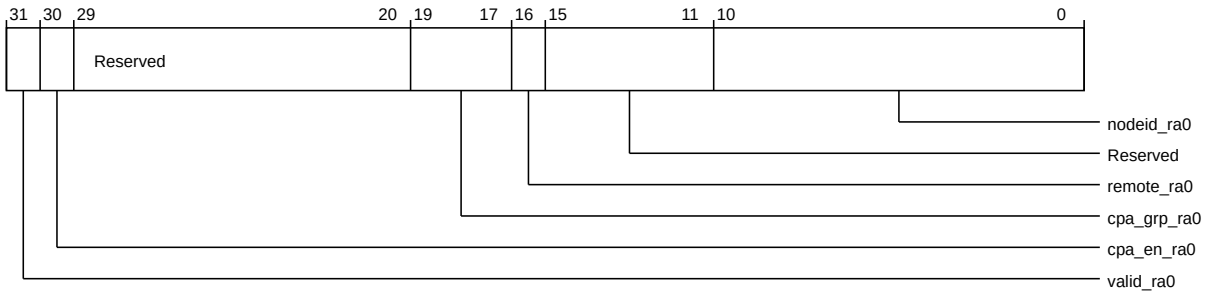
Table 5-450: por_hnf_por_hnf_rn_phys_id0 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra1	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra1	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra1	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra1	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra1	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-437: por_hnf_por_hnf_rn_phys_id0 (low)



The following table shows the por_hnf_rn_phys_id0 lower register bit assignments.

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Table 5-451: por_hnf_por_hnf_rn_phys_id0 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra0	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra0	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra0	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra0	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra0	Specifies the node ID	RW	11'h0

5.3.4.68 por_hnf_rn_phys_id1

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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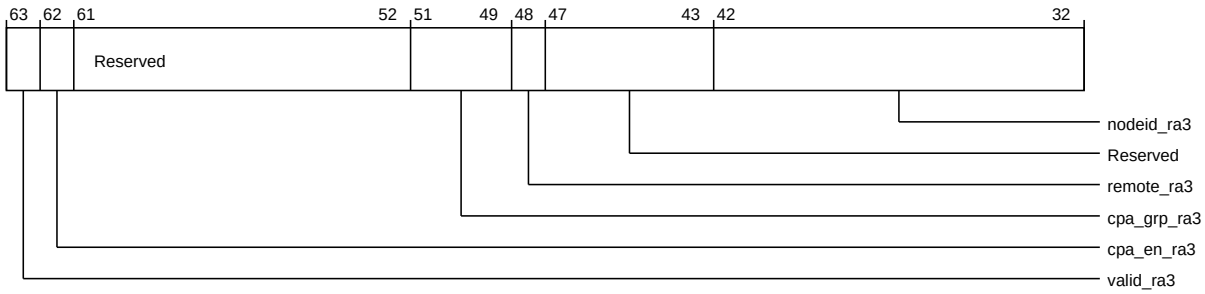
Figure 5-438: por_hnf_por_hnf_rn_phys_id1 (high)



The following table shows the por_hnf_rn_phys_id1 higher register bit assignments.

Table 5-452: por_hnf_por_hnf_rn_phys_id1 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra3	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra3	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra3	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra3	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra3	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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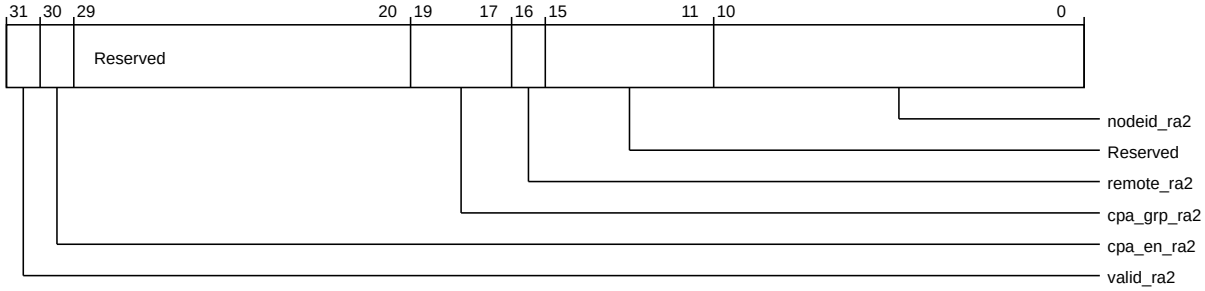
Figure 5-439: por_hnf_por_hnf_rn_phys_id1 (low)



The following table shows the por_hnf_rn_phys_id1 lower register bit assignments.

Table 5-453: por_hnf_por_hnf_rn_phys_id1 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra2	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra2	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra2	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra2	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra2	Specifies the node ID	RW	11'h0

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5.3.4.69 por_hnf_rn_phys_id2

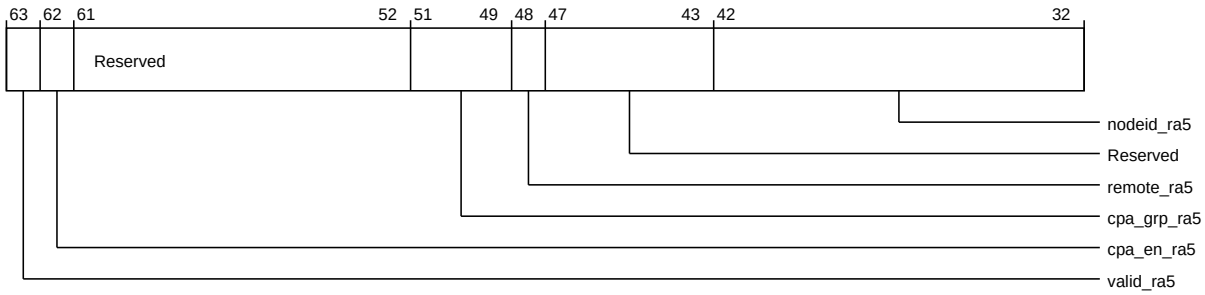
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-440: por_hnf_por_hnf_rn_phys_id2 (high)



The following table shows the por_hnf_rn_phys_id2 higher register bit assignments.

Table 5-454: por_hnf_por_hnf_rn_phys_id2 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra5	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra5	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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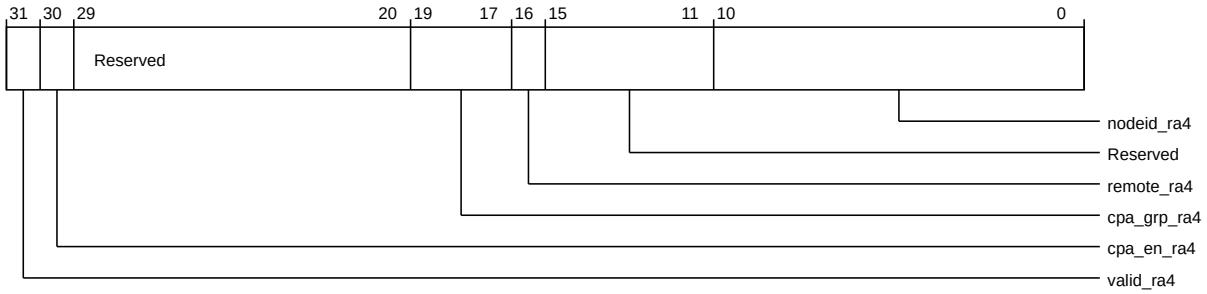
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra5	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 2'b11: Reserved	RW	3'h0
48	remote_ra5	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra5	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-441: por_hnf_por_hnf_rn_phys_id2 (low)



The following table shows the por_hnf_rn_phys_id2 lower register bit assignments.

Table 5-455: por_hnf_por_hnf_rn_phys_id2 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra4	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra4	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra4	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 2'b11: Reserved	RW	3'h0
16	remote_ra4	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra4	Specifies the node ID	RW	11'h0

5.3.4.70 por_hnf_rn_phys_id3

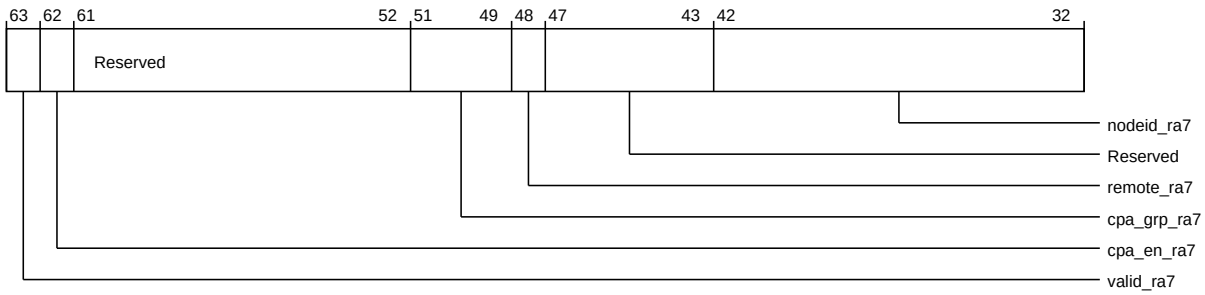
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-442: por_hnf_por_hnf_rn_phys_id3 (high)



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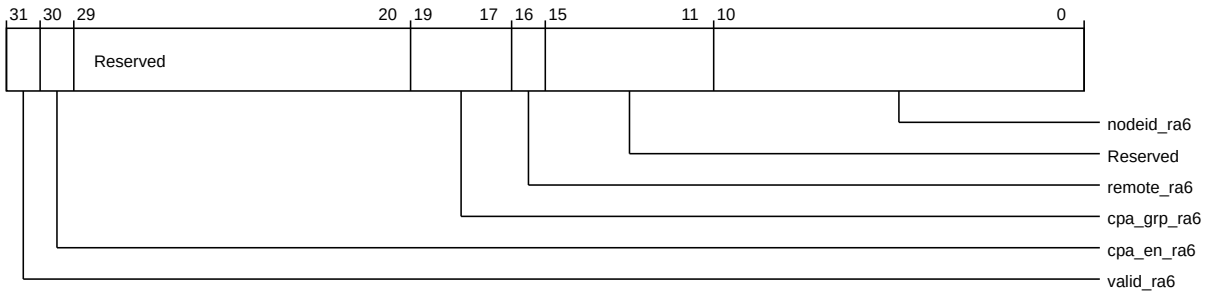
The following table shows the por_hnf_rn_phys_id3 higher register bit assignments.

Table 5-456: por_hnf_por_hnf_rn_phys_id3 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra7	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra7	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra7	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 2'b11: Reserved	RW	3'h0
48	remote_ra7	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra7	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-443: por_hnf_por_hnf_rn_phys_id3 (low)



The following table shows the por_hnf_rn_phys_id3 lower register bit assignments.

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Table 5-457: por_hnf_por_hnf_rn_phys_id3 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra6	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra6	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra6	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 2'b11: Reserved	RW	3'h0
16	remote_ra6	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra6	Specifies the node ID	RW	11'h0

5.3.4.71 por_hnf_rn_phys_id4

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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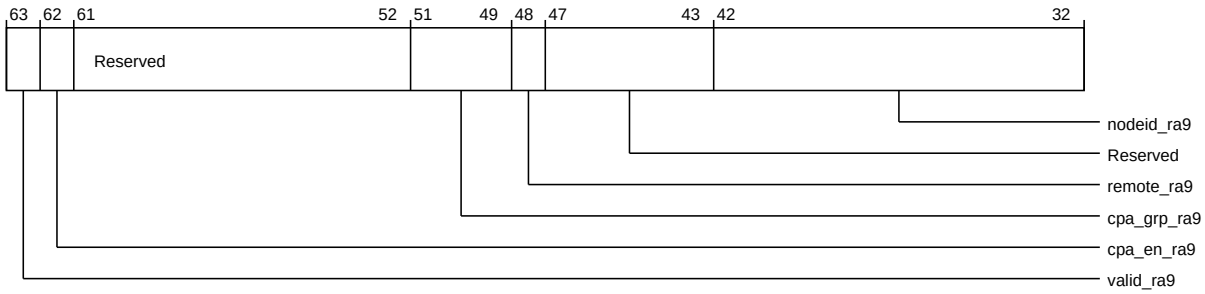
Figure 5-444: por_hnf_por_hnf_rn_phys_id4 (high)



The following table shows the por_hnf_rn_phys_id4 higher register bit assignments.

Table 5-458: por_hnf_por_hnf_rn_phys_id4 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra9	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra9	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra9	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra9	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra9	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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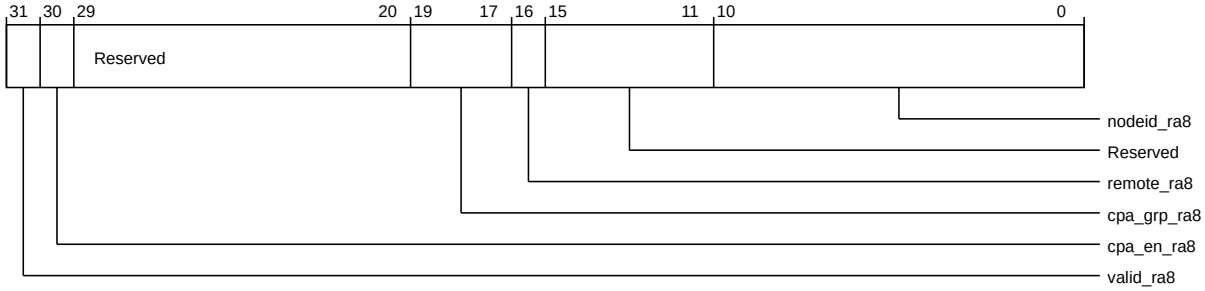
Figure 5-445: por_hnf_por_hnf_rn_phys_id4 (low)



The following table shows the por_hnf_rn_phys_id4 lower register bit assignments.

Table 5-459: por_hnf_por_hnf_rn_phys_id4 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra8	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra8	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra8	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 2'b11: Reserved	RW	3'h0
16	remote_ra8	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra8	Specifies the node ID	RW	11'h0

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5.3.4.72 por_hnf_rn_phys_id5

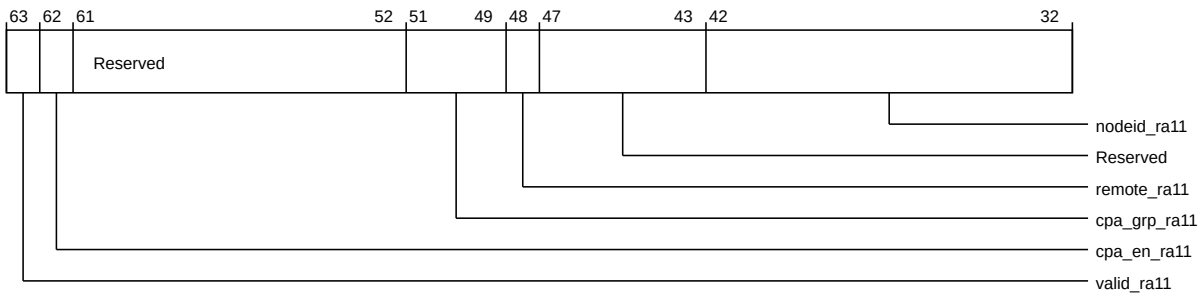
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-446: por_hnf_por_hnf_rn_phys_id5 (high)



The following table shows the por_hnf_rn_phys_id5 higher register bit assignments.

Table 5-460: por_hnf_por_hnf_rn_phys_id5 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra11	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra11	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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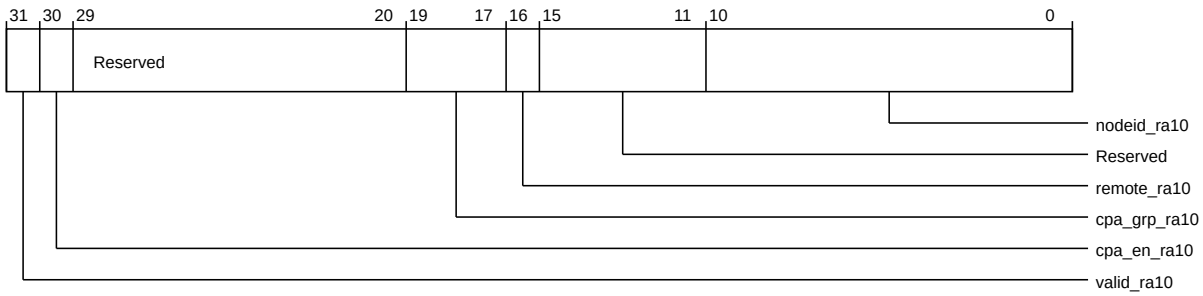
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra11	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra11	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra11	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-447: por_hnf_por_hnf_rn_phys_id5 (low)



The following table shows the por_hnf_rn_phys_id5 lower register bit assignments.

Table 5-461: por_hnf_por_hnf_rn_phys_id5 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra10	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra10	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra10	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra10	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra10	Specifies the node ID	RW	11'h0

5.3.4.73 por_hnf_rn_phys_id6

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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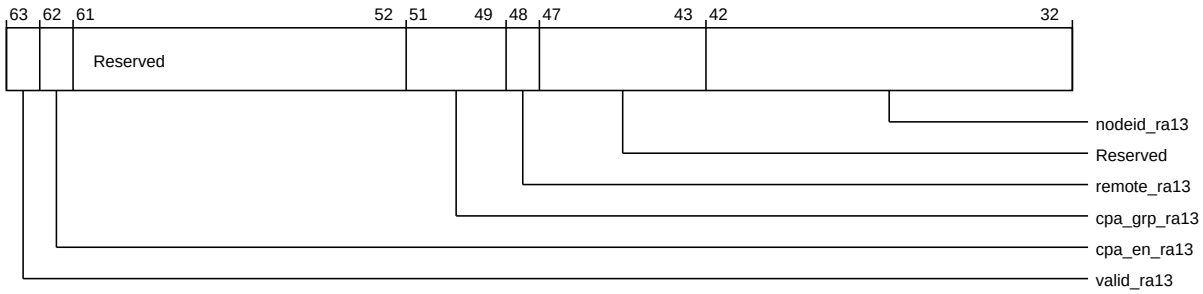
Figure 5-448: por_hnf_por_hnf_rn_phys_id6 (high)



The following table shows the por_hnf_rn_phys_id6 higher register bit assignments.

Table 5-462: por_hnf_por_hnf_rn_phys_id6 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra13	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra13	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra13	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra13	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra13	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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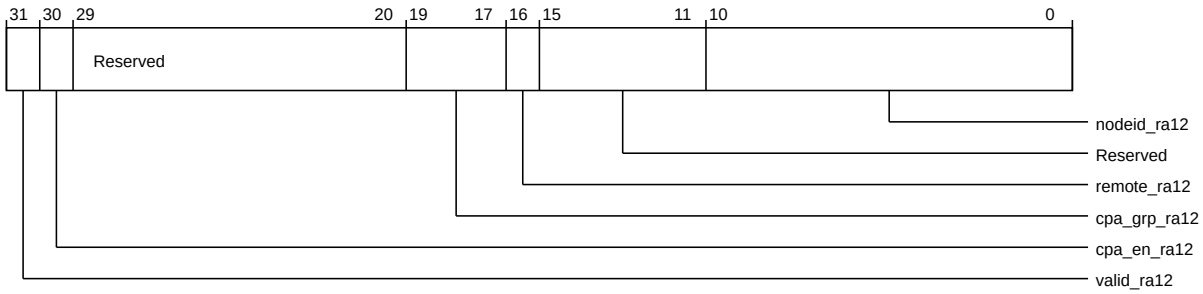
Figure 5-449: por_hnf_por_hnf_rn_phys_id6 (low)



The following table shows the por_hnf_rn_phys_id6 lower register bit assignments.

Table 5-463: por_hnf_por_hnf_rn_phys_id6 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra12	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra12	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra12	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra12	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra12	Specifies the node ID	RW	11'h0

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5.3.4.74 por_hnf_rn_phys_id7

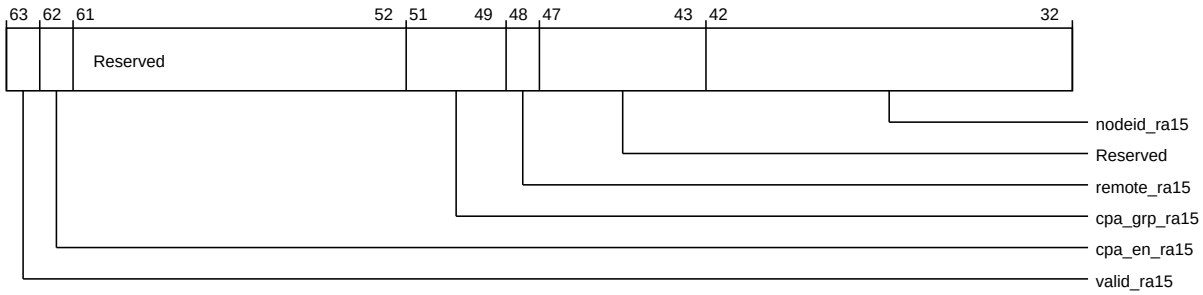
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-450: por_hnf_por_hnf_rn_phys_id7 (high)



The following table shows the por_hnf_rn_phys_id7 higher register bit assignments.

Table 5-464: por_hnf_por_hnf_rn_phys_id7 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra15	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra15	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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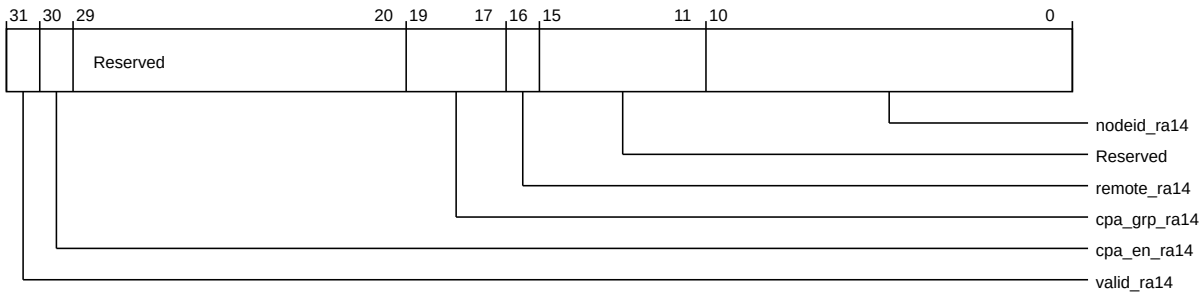
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra15	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra15	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra15	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-451: por_hnf_por_hnf_rn_phys_id7 (low)



The following table shows the por_hnf_rn_phys_id7 lower register bit assignments.

Table 5-465: por_hnf_por_hnf_rn_phys_id7 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra14	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra14	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra14	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra14	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra14	Specifies the node ID	RW	11'h0

5.3.4.75 por_hnf_rn_phys_id8

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD68
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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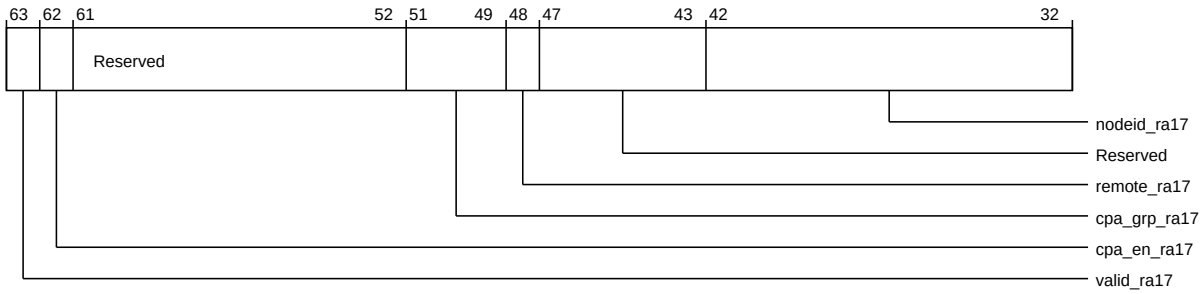
Figure 5-452: por_hnf_por_hnf_rn_phys_id8 (high)



The following table shows the por_hnf_rn_phys_id8 higher register bit assignments.

Table 5-466: por_hnf_por_hnf_rn_phys_id8 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra17	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra17	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra17	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra17	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra17	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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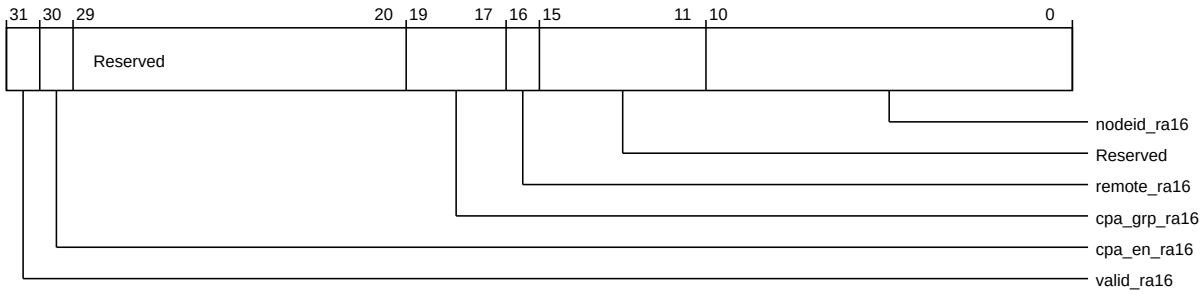
Figure 5-453: por_hnf_por_hnf_rn_phys_id8 (low)



The following table shows the por_hnf_rn_phys_id8 lower register bit assignments.

Table 5-467: por_hnf_por_hnf_rn_phys_id8 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra16	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra16	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra16	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra16	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra16	Specifies the node ID	RW	11'h0

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5.3.4.76 por_hnf_rn_phys_id9

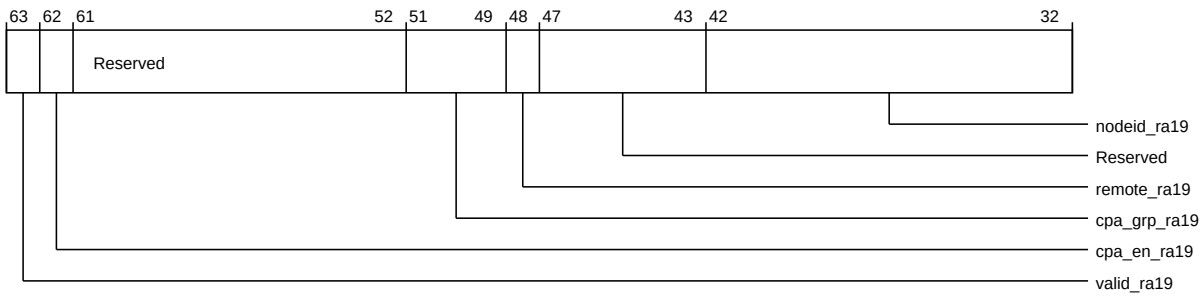
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-454: por_hnf_por_hnf_rn_phys_id9 (high)



The following table shows the por_hnf_rn_phys_id9 higher register bit assignments.

Table 5-468: por_hnf_por_hnf_rn_phys_id9 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra19	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra19	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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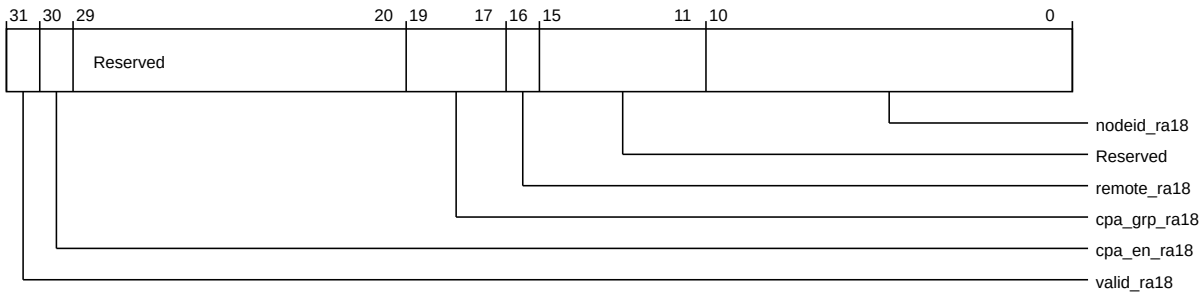
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra19	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra19	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra19	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-455: por_hnf_por_hnf_rn_phys_id9 (low)



The following table shows the por_hnf_rn_phys_id9 lower register bit assignments.

Table 5-469: por_hnf_por_hnf_rn_phys_id9 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra18	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra18	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra18	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra18	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra18	Specifies the node ID	RW	11'h0

5.3.4.77 por_hnf_rn_phys_id10

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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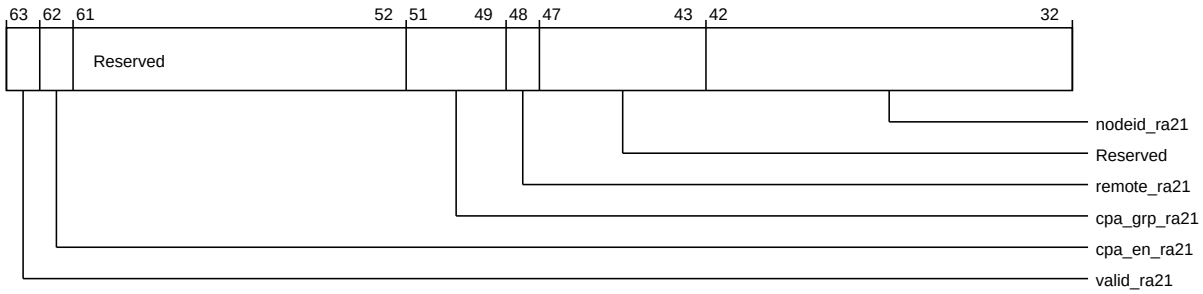
Figure 5-456: por_hnf_por_hnf_rn_phys_id10 (high)



The following table shows the por_hnf_rn_phys_id10 higher register bit assignments.

Table 5-470: por_hnf_por_hnf_rn_phys_id10 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra21	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra21	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra21	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra21	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra21	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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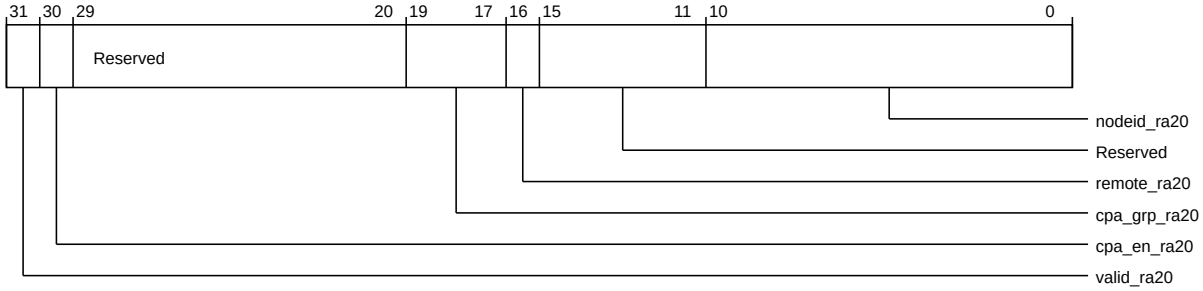
Figure 5-457: por_hnf_por_hnf_rn_phys_id10 (low)



The following table shows the por_hnf_rn_phys_id10 lower register bit assignments.

Table 5-471: por_hnf_por_hnf_rn_phys_id10 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra20	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra20	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra20	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra20	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra20	Specifies the node ID	RW	11'h0

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5.3.4.78 por_hnf_rn_phys_id11

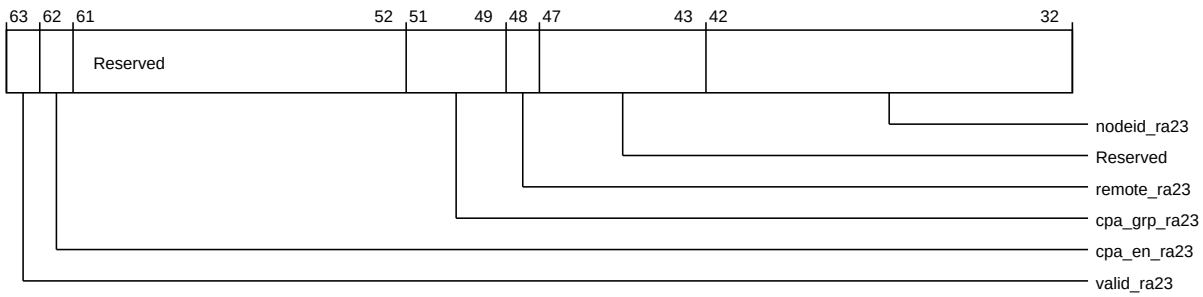
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-458: por_hnf_por_hnf_rn_phys_id11 (high)



The following table shows the por_hnf_rn_phys_id11 higher register bit assignments.

Table 5-472: por_hnf_por_hnf_rn_phys_id11 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra23	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra23	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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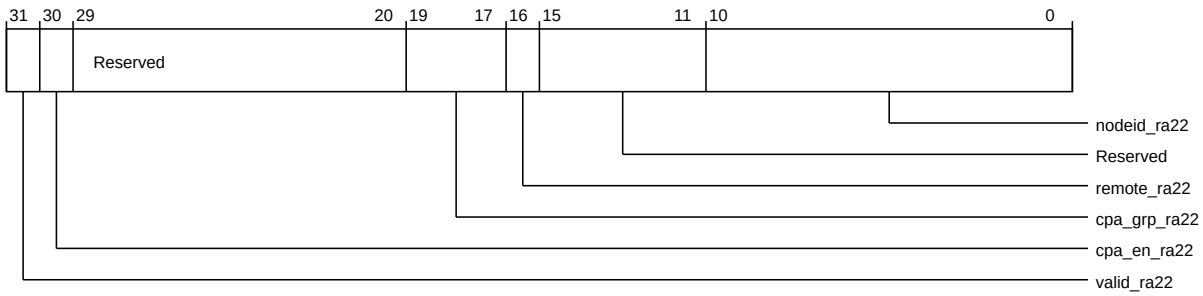
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra23	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra23	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra23	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-459: por_hnf_por_hnf_rn_phys_id11 (low)



The following table shows the por_hnf_rn_phys_id11 lower register bit assignments.

Table 5-473: por_hnf_por_hnf_rn_phys_id11 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra22	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra22	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra22	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra22	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra22	Specifies the node ID	RW	11'h0

5.3.4.79 por_hnf_rn_phys_id12

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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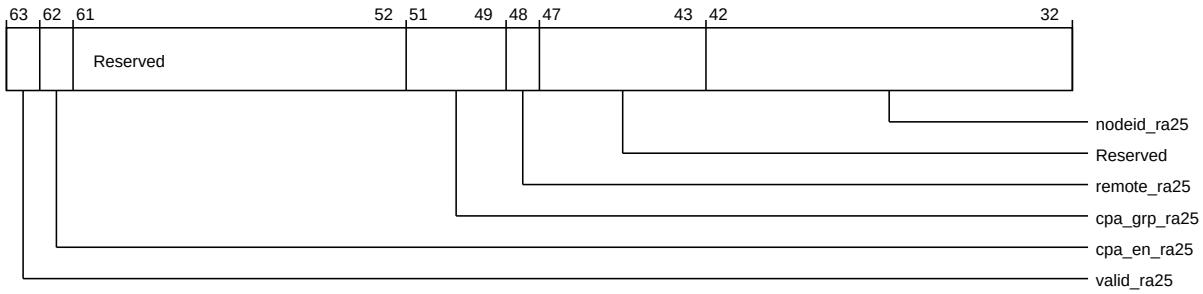
Figure 5-460: por_hnf_por_hnf_rn_phys_id12 (high)



The following table shows the por_hnf_rn_phys_id12 higher register bit assignments.

Table 5-474: por_hnf_por_hnf_rn_phys_id12 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra25	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra25	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra25	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra25	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra25	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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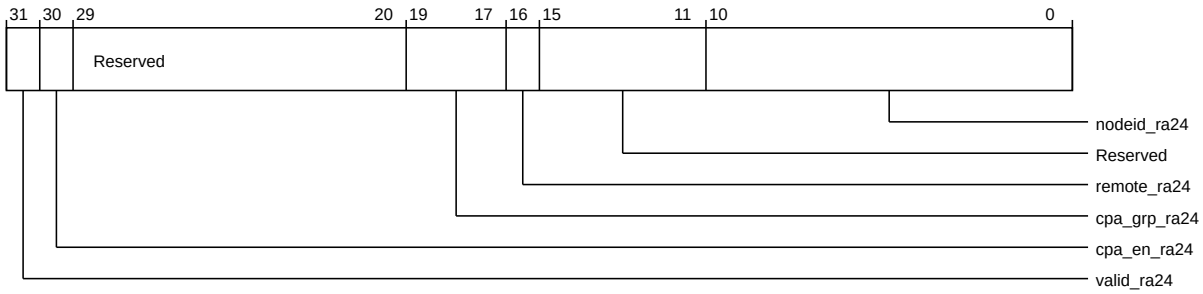
Figure 5-461: por_hnf_por_hnf_rn_phys_id12 (low)



The following table shows the por_hnf_rn_phys_id12 lower register bit assignments.

Table 5-475: por_hnf_por_hnf_rn_phys_id12 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra24	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra24	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra24	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra24	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra24	Specifies the node ID	RW	11'h0

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5.3.4.80 por_hnf_rn_phys_id13

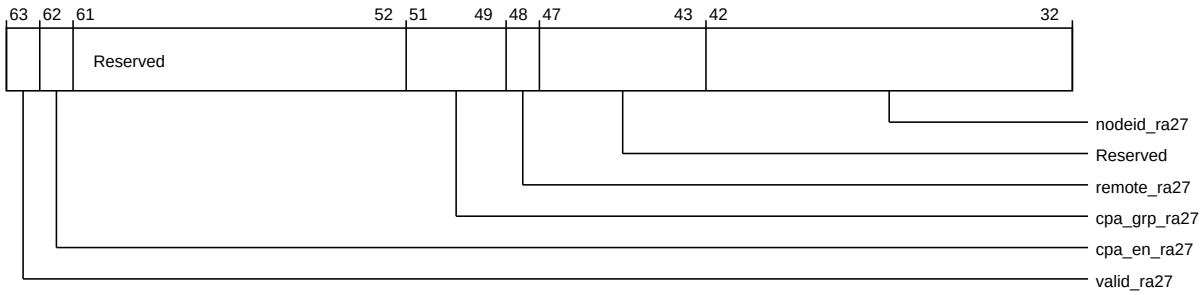
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-462: por_hnf_por_hnf_rn_phys_id13 (high)



The following table shows the por_hnf_rn_phys_id13 higher register bit assignments.

Table 5-476: por_hnf_por_hnf_rn_phys_id13 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra27	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra27	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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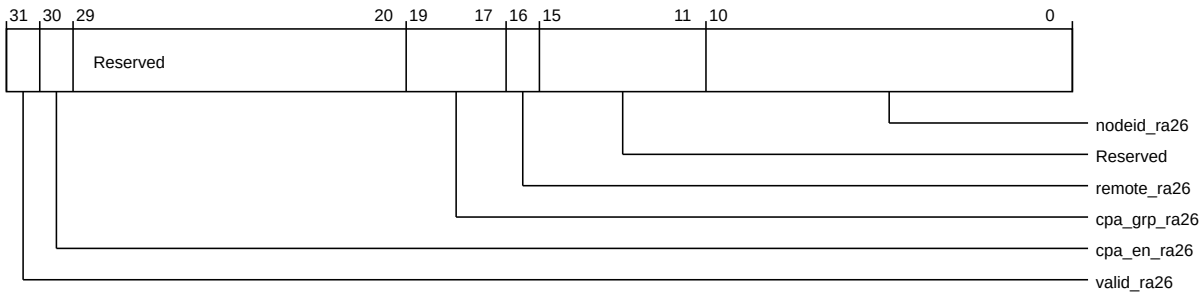
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra27	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra27	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra27	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-463: por_hnf_por_hnf_rn_phys_id13 (low)



The following table shows the por_hnf_rn_phys_id13 lower register bit assignments.

Table 5-477: por_hnf_por_hnf_rn_phys_id13 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra26	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra26	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra26	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra26	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra26	Specifies the node ID	RW	11'h0

5.3.4.81 por_hnf_rn_phys_id14

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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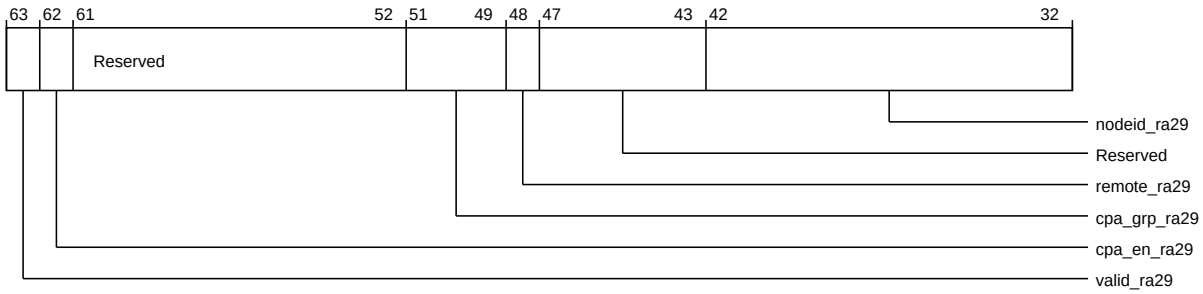
Figure 5-464: por_hnf_por_hnf_rn_phys_id14 (high)



The following table shows the por_hnf_rn_phys_id14 higher register bit assignments.

Table 5-478: por_hnf_por_hnf_rn_phys_id14 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra29	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra29	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra29	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra29	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra29	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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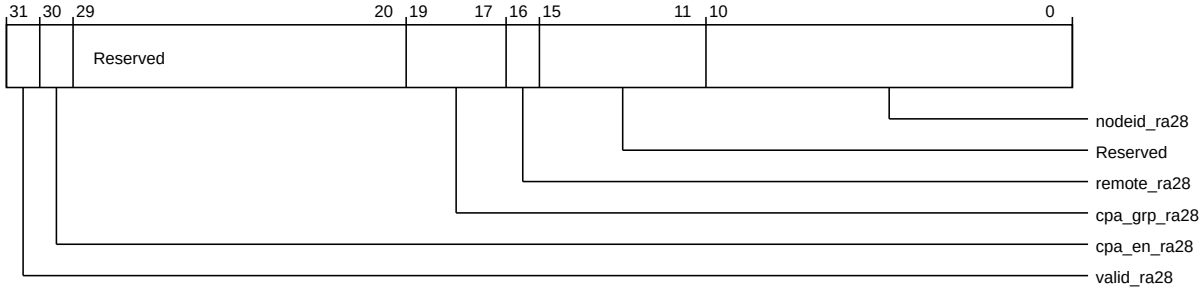
Figure 5-465: por_hnf_por_hnf_rn_phys_id14 (low)



The following table shows the por_hnf_rn_phys_id14 lower register bit assignments.

Table 5-479: por_hnf_por_hnf_rn_phys_id14 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra28	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra28	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra28	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra28	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra28	Specifies the node ID	RW	11'h0

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5.3.4.82 por_hnf_rn_phys_id15

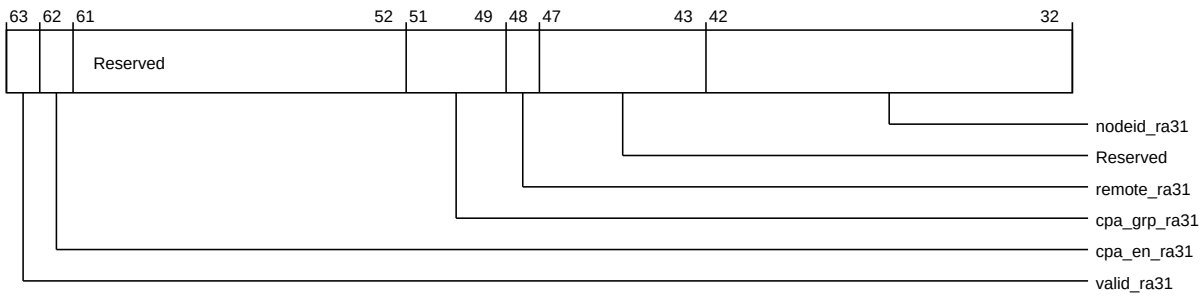
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-466: por_hnf_por_hnf_rn_phys_id15 (high)



The following table shows the por_hnf_rn_phys_id15 higher register bit assignments.

Table 5-480: por_hnf_por_hnf_rn_phys_id15 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra31	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra31	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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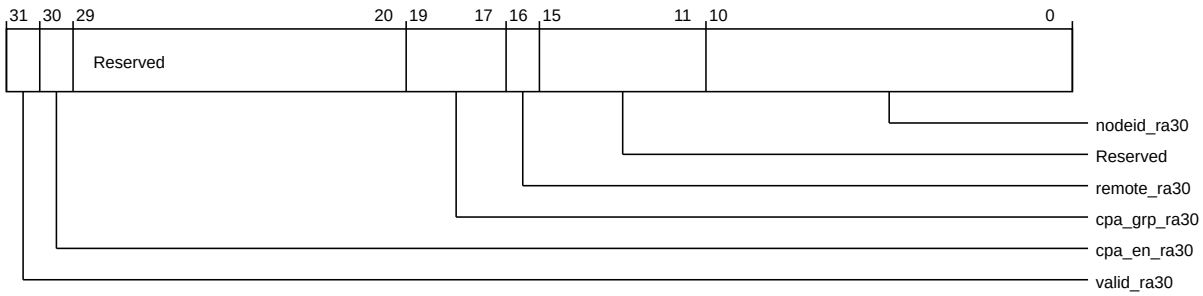
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra31	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra31	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra31	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-467: por_hnf_por_hnf_rn_phys_id15 (low)



The following table shows the por_hnf_rn_phys_id15 lower register bit assignments.

Table 5-481: por_hnf_por_hnf_rn_phys_id15 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra30	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra30	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra30	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra30	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra30	Specifies the node ID	RW	11'h0

5.3.4.83 por_hnf_rn_phys_id16

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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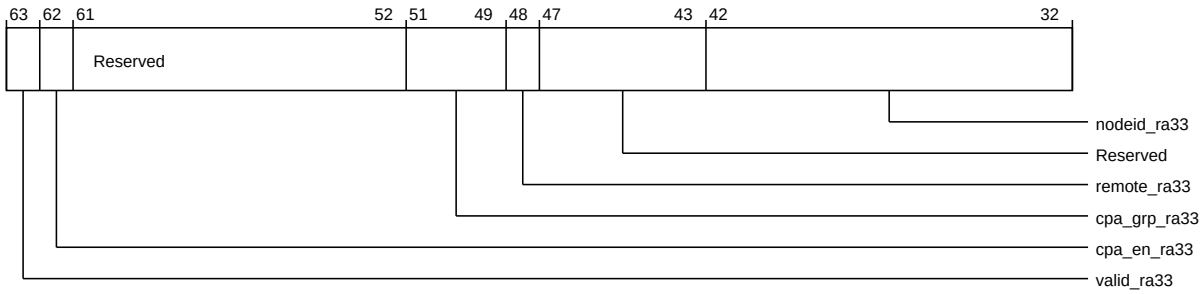
Figure 5-468: por_hnf_por_hnf_rn_phys_id16 (high)



The following table shows the por_hnf_rn_phys_id16 higher register bit assignments.

Table 5-482: por_hnf_por_hnf_rn_phys_id16 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra33	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra33	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra33	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra33	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra33	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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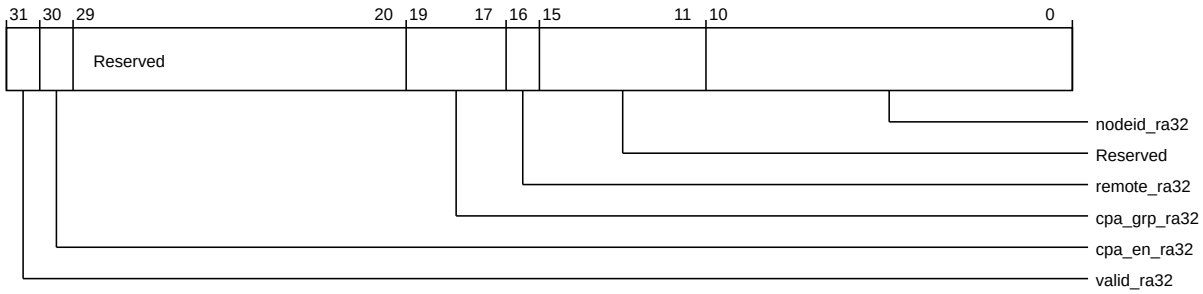
Figure 5-469: por_hnf_por_hnf_rn_phys_id16 (low)



The following table shows the por_hnf_rn_phys_id16 lower register bit assignments.

Table 5-483: por_hnf_por_hnf_rn_phys_id16 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra32	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra32	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra32	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra32	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra32	Specifies the node ID	RW	11'h0

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5.3.4.84 por_hnf_rn_phys_id17

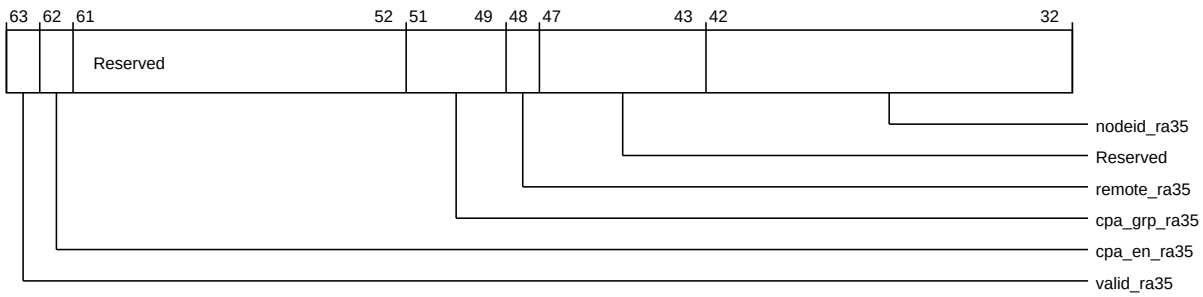
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-470: por_hnf_por_hnf_rn_phys_id17 (high)



The following table shows the por_hnf_rn_phys_id17 higher register bit assignments.

Table 5-484: por_hnf_por_hnf_rn_phys_id17 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra35	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra35	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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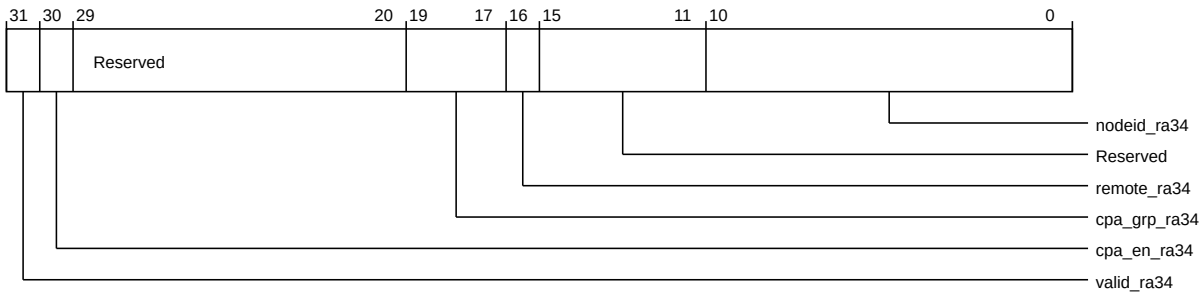
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra35	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra35	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra35	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-471: por_hnf_por_hnf_rn_phys_id17 (low)



The following table shows the por_hnf_rn_phys_id17 lower register bit assignments.

Table 5-485: por_hnf_por_hnf_rn_phys_id17 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra34	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra34	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra34	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra34	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra34	Specifies the node ID	RW	11'h0

5.3.4.85 por_hnf_rn_phys_id18

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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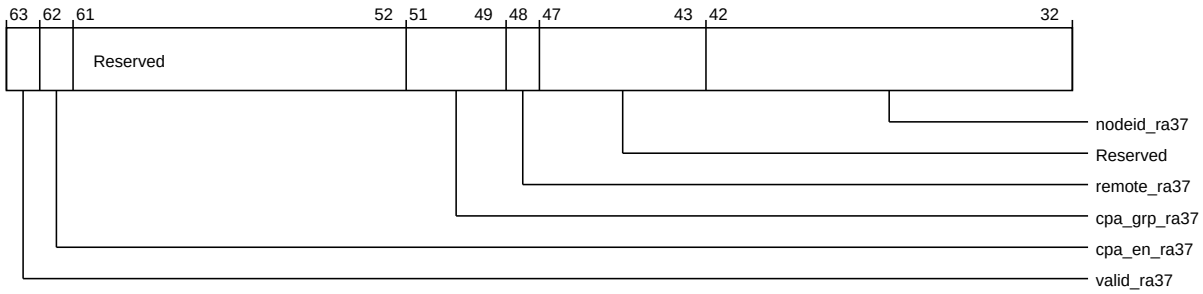
Figure 5-472: por_hnf_por_hnf_rn_phys_id18 (high)



The following table shows the por_hnf_rn_phys_id18 higher register bit assignments.

Table 5-486: por_hnf_por_hnf_rn_phys_id18 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra37	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra37	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra37	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra37	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra37	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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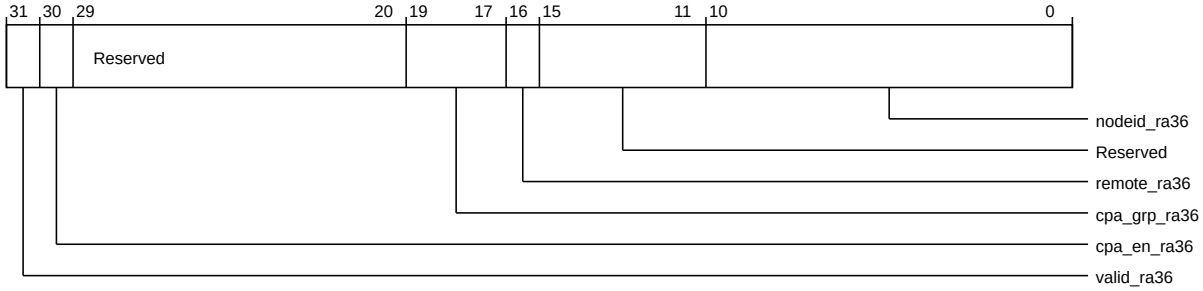
Figure 5-473: por_hnf_por_hnf_rn_phys_id18 (low)



The following table shows the por_hnf_rn_phys_id18 lower register bit assignments.

Table 5-487: por_hnf_por_hnf_rn_phys_id18 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra36	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra36	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra36	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra36	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra36	Specifies the node ID	RW	11'h0

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5.3.4.86 por_hnf_rn_phys_id19

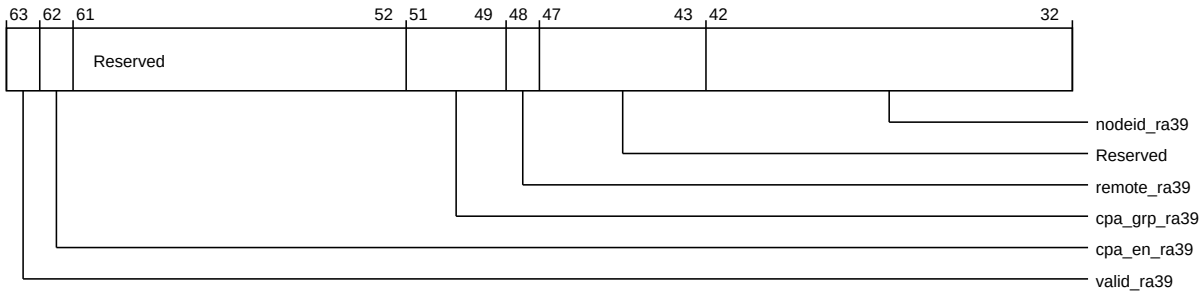
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-474: por_hnf_por_hnf_rn_phys_id19 (high)



The following table shows the por_hnf_rn_phys_id19 higher register bit assignments.

Table 5-488: por_hnf_por_hnf_rn_phys_id19 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra39	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra39	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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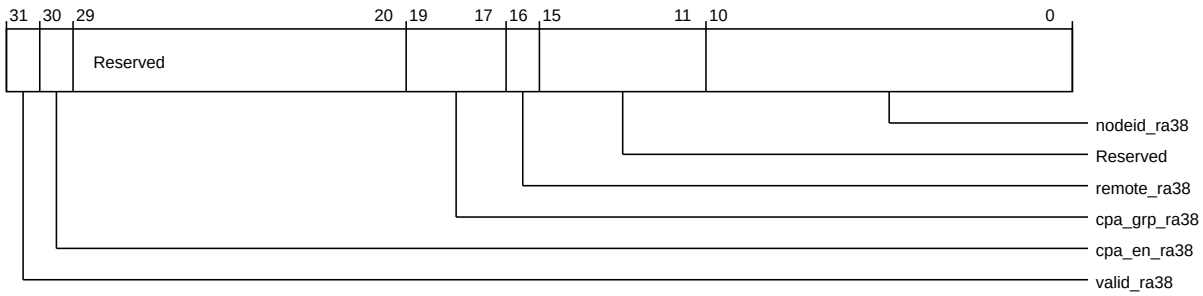
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra39	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra39	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra39	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-475: por_hnf_por_hnf_rn_phys_id19 (low)



The following table shows the por_hnf_rn_phys_id19 lower register bit assignments.

Table 5-489: por_hnf_por_hnf_rn_phys_id19 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra38	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra38	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra38	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra38	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra38	Specifies the node ID	RW	11'h0

5.3.4.87 por_hnf_rn_phys_id20

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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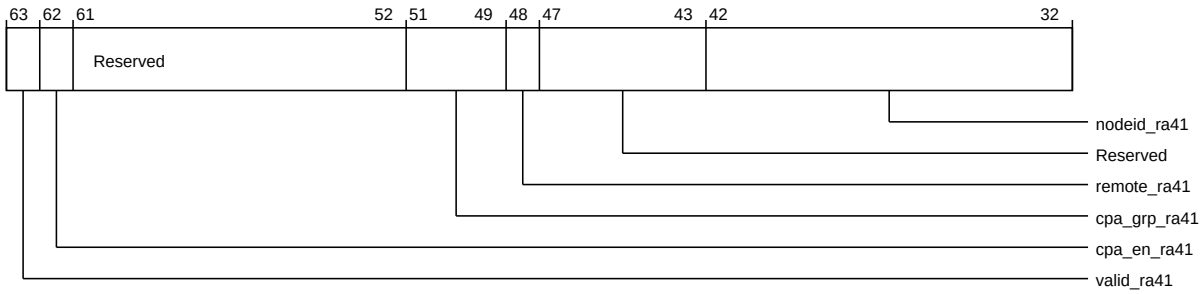
Figure 5-476: por_hnf_por_hnf_rn_phys_id20 (high)



The following table shows the por_hnf_rn_phys_id20 higher register bit assignments.

Table 5-490: por_hnf_por_hnf_rn_phys_id20 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra41	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra41	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra41	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra41	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra41	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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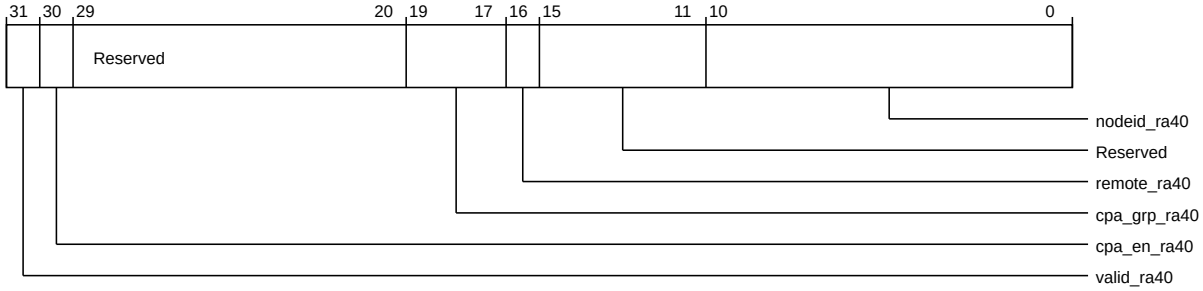
Figure 5-477: por_hnf_por_hnf_rn_phys_id20 (low)



The following table shows the por_hnf_rn_phys_id20 lower register bit assignments.

Table 5-491: por_hnf_por_hnf_rn_phys_id20 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra40	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra40	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra40	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra40	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra40	Specifies the node ID	RW	11'h0

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5.3.4.88 por_hnf_rn_phys_id21

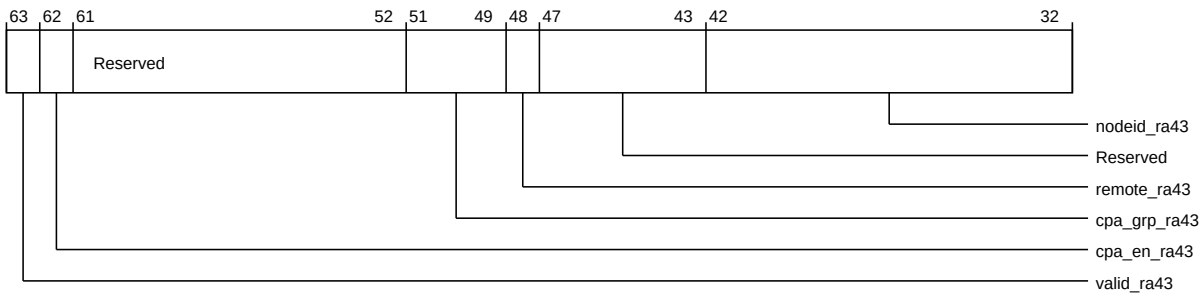
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-478: por_hnf_por_hnf_rn_phys_id21 (high)



The following table shows the por_hnf_rn_phys_id21 higher register bit assignments.

Table 5-492: por_hnf_por_hnf_rn_phys_id21 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra43	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra43	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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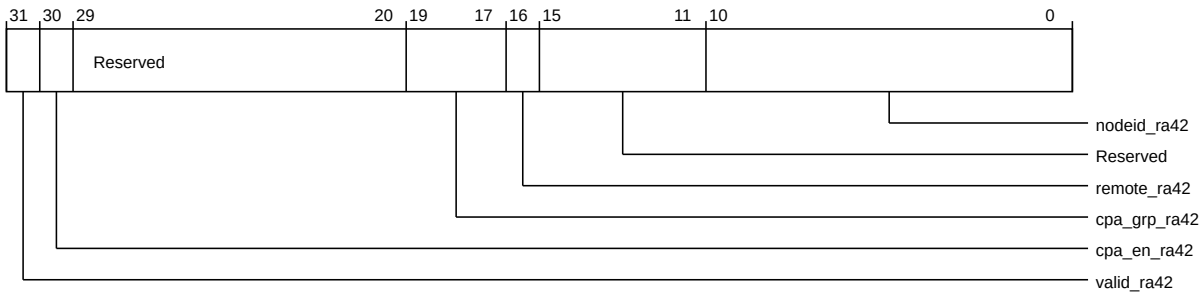
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra43	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra43	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra43	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-479: por_hnf_por_hnf_rn_phys_id21 (low)



The following table shows the por_hnf_rn_phys_id21 lower register bit assignments.

Table 5-493: por_hnf_por_hnf_rn_phys_id21 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra42	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra42	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra42	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra42	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra42	Specifies the node ID	RW	11'h0

5.3.4.89 por_hnf_rn_phys_id22

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDD8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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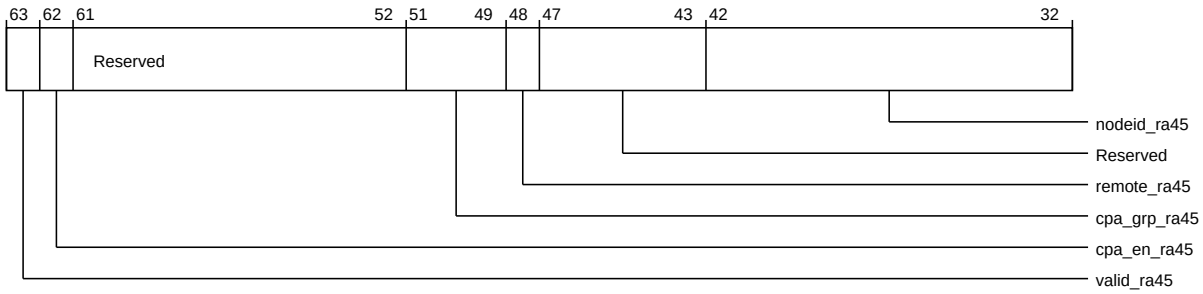
Figure 5-480: por_hnf_por_hnf_rn_phys_id22 (high)



The following table shows the por_hnf_rn_phys_id22 higher register bit assignments.

Table 5-494: por_hnf_por_hnf_rn_phys_id22 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra45	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra45	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra45	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra45	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra45	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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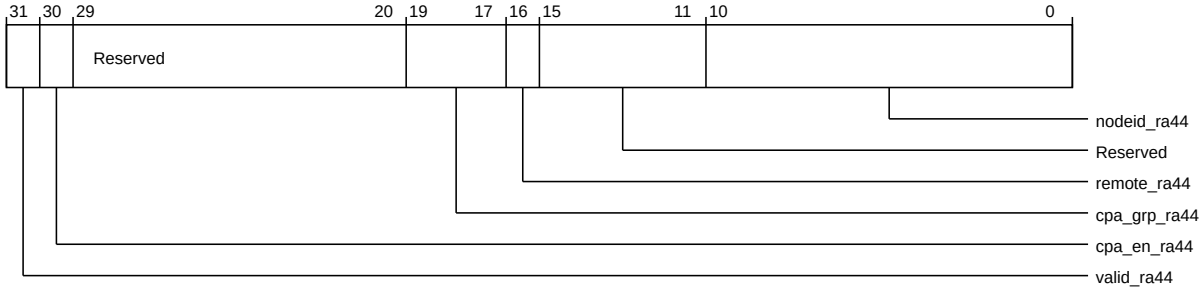
Figure 5-481: por_hnf_por_hnf_rn_phys_id22 (low)



The following table shows the por_hnf_rn_phys_id22 lower register bit assignments.

Table 5-495: por_hnf_por_hnf_rn_phys_id22 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra44	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra44	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra44	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra44	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra44	Specifies the node ID	RW	11'h0

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5.3.4.90 por_hnf_rn_phys_id23

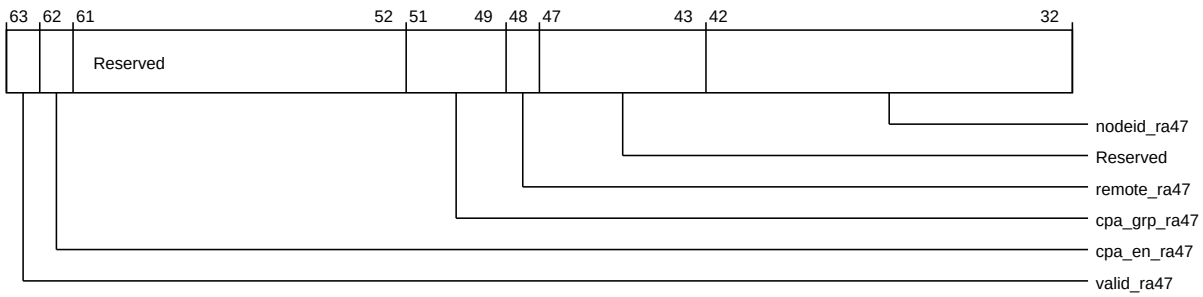
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDE0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-482: por_hnf_por_hnf_rn_phys_id23 (high)



The following table shows the por_hnf_rn_phys_id23 higher register bit assignments.

Table 5-496: por_hnf_por_hnf_rn_phys_id23 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra47	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra47	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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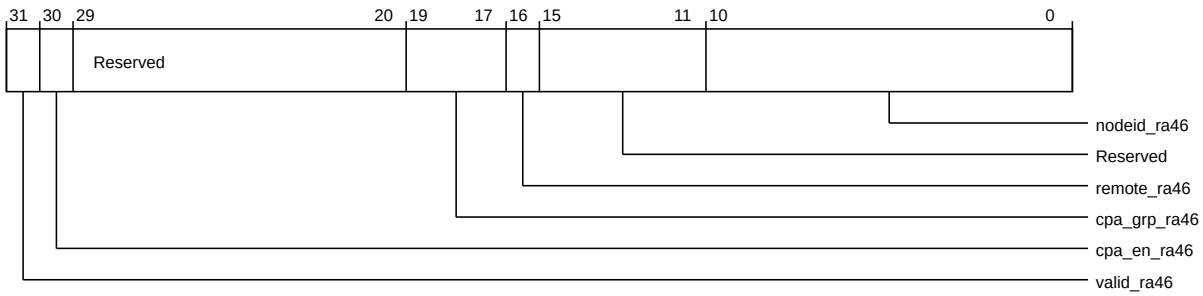
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra47	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra47	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra47	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-483: por_hnf_por_hnf_rn_phys_id23 (low)



The following table shows the por_hnf_rn_phys_id23 lower register bit assignments.

Table 5-497: por_hnf_por_hnf_rn_phys_id23 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra46	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra46	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra46	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra46	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra46	Specifies the node ID	RW	11'h0

5.3.4.91 por_hnf_rn_phys_id24

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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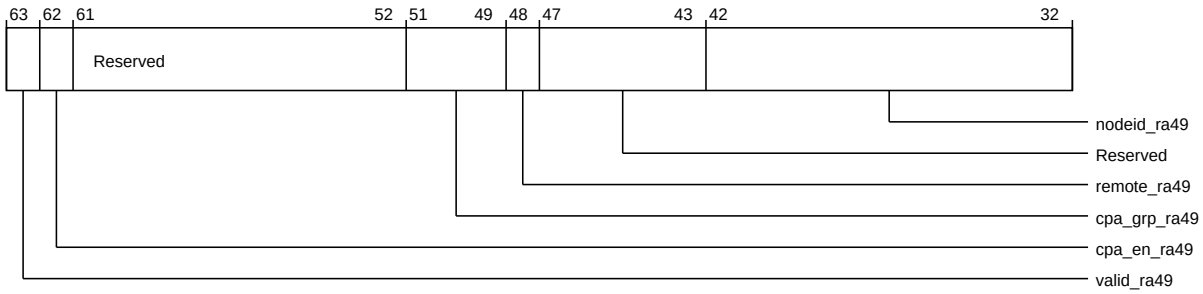
Figure 5-484: por_hnf_por_hnf_rn_phys_id24 (high)



The following table shows the por_hnf_rn_phys_id24 higher register bit assignments.

Table 5-498: por_hnf_por_hnf_rn_phys_id24 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra49	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra49	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra49	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra49	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra49	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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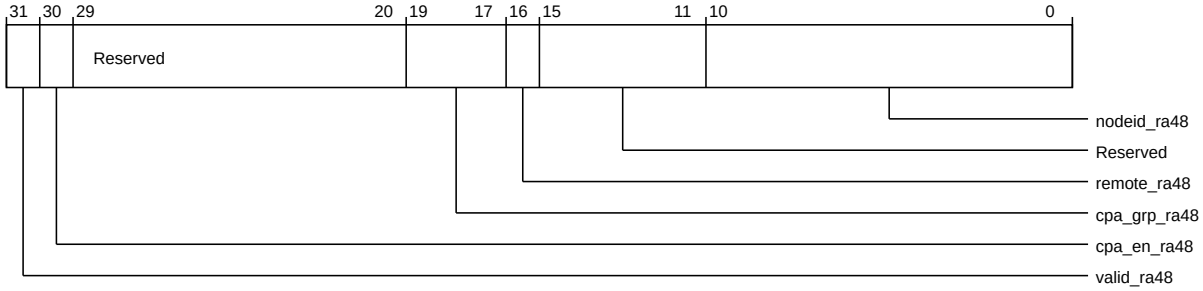
Figure 5-485: por_hnf_por_hnf_rn_phys_id24 (low)



The following table shows the por_hnf_rn_phys_id24 lower register bit assignments.

Table 5-499: por_hnf_por_hnf_rn_phys_id24 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra48	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra48	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra48	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra48	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra48	Specifies the node ID	RW	11'h0

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5.3.4.92 por_hnf_rn_phys_id25

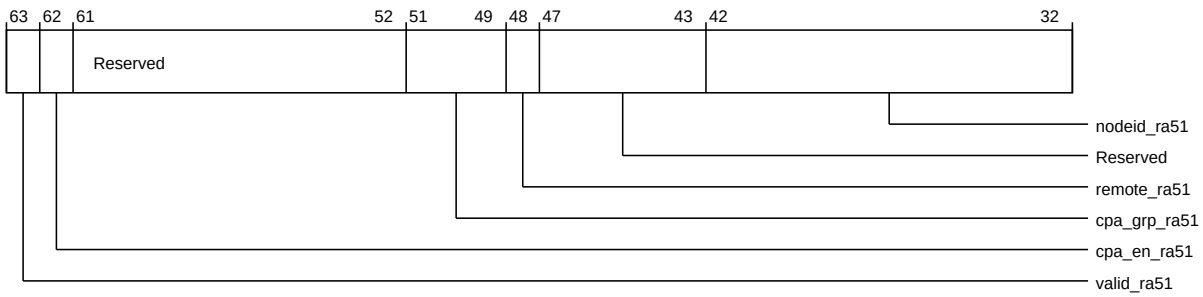
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDF0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-486: por_hnf_por_hnf_rn_phys_id25 (high)



The following table shows the por_hnf_rn_phys_id25 higher register bit assignments.

Table 5-500: por_hnf_por_hnf_rn_phys_id25 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra51	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra51	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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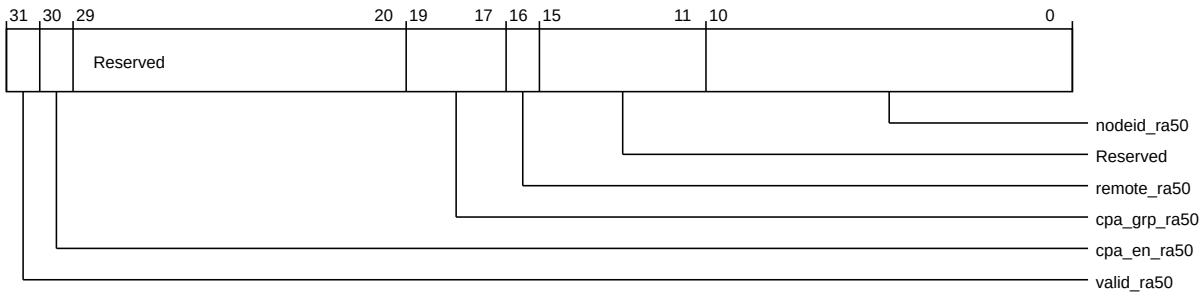
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra51	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra51	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra51	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-487: por_hnf_por_hnf_rn_phys_id25 (low)



The following table shows the por_hnf_rn_phys_id25 lower register bit assignments.

Table 5-501: por_hnf_por_hnf_rn_phys_id25 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra50	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra50	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra50	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra50	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra50	Specifies the node ID	RW	11'h0

5.3.4.93 por_hnf_rn_phys_id26

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDF8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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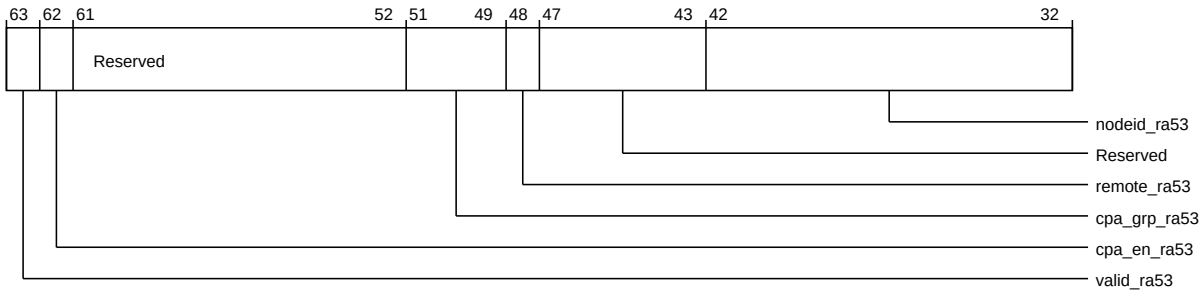
Figure 5-488: por_hnf_por_hnf_rn_phys_id26 (high)



The following table shows the por_hnf_rn_phys_id26 higher register bit assignments.

Table 5-502: por_hnf_por_hnf_rn_phys_id26 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra53	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra53	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra53	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra53	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra53	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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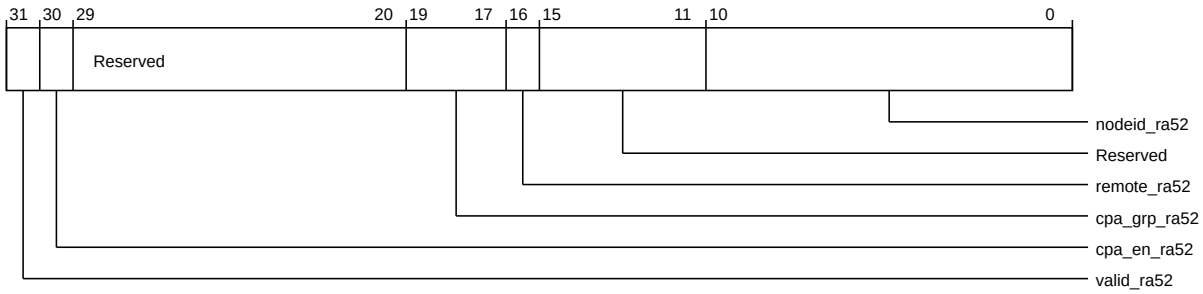
Figure 5-489: por_hnf_por_hnf_rn_phys_id26 (low)



The following table shows the por_hnf_rn_phys_id26 lower register bit assignments.

Table 5-503: por_hnf_por_hnf_rn_phys_id26 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra52	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra52	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra52	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra52	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra52	Specifies the node ID	RW	11'h0

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5.3.4.94 por_hnf_rn_phys_id27

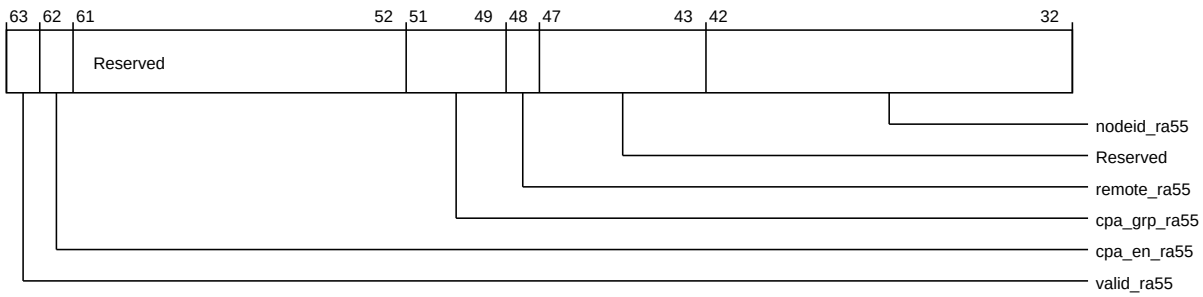
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-490: por_hnf_por_hnf_rn_phys_id27 (high)



The following table shows the por_hnf_rn_phys_id27 higher register bit assignments.

Table 5-504: por_hnf_por_hnf_rn_phys_id27 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra55	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra55	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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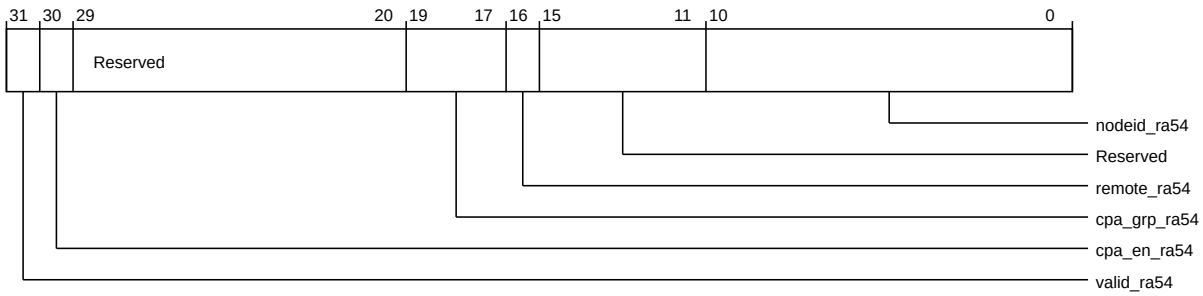
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra55	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra55	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra55	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-491: por_hnf_por_hnf_rn_phys_id27 (low)



The following table shows the por_hnf_rn_phys_id27 lower register bit assignments.

Table 5-505: por_hnf_por_hnf_rn_phys_id27 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra54	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra54	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra54	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra54	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra54	Specifies the node ID	RW	11'h0

5.3.4.95 por_hnf_rn_phys_id28

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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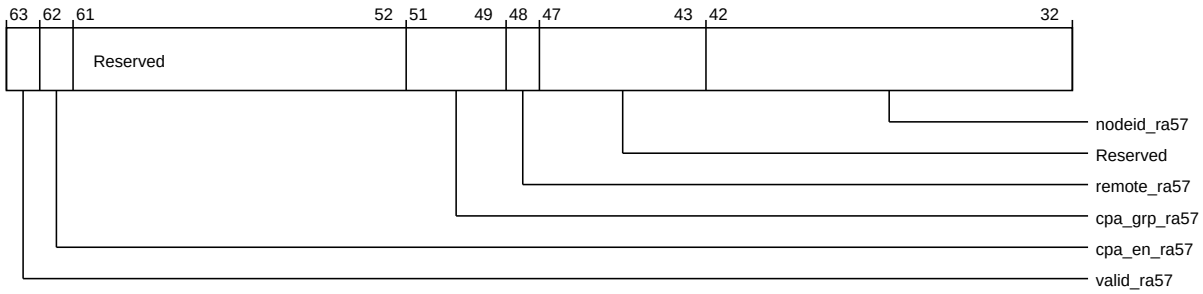
Figure 5-492: por_hnf_por_hnf_rn_phys_id28 (high)



The following table shows the por_hnf_rn_phys_id28 higher register bit assignments.

Table 5-506: por_hnf_por_hnf_rn_phys_id28 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra57	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra57	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra57	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra57	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra57	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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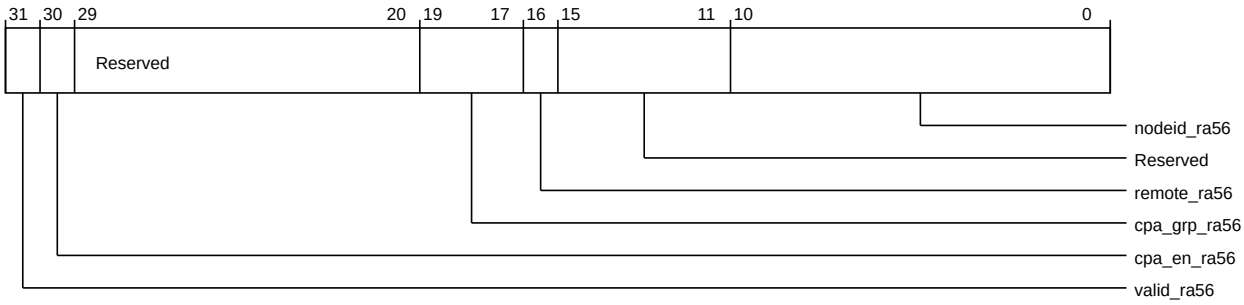
Figure 5-493: por_hnf_por_hnf_rn_phys_id28 (low)



The following table shows the por_hnf_rn_phys_id28 lower register bit assignments.

Table 5-507: por_hnf_por_hnf_rn_phys_id28 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra56	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra56	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra56	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra56	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra56	Specifies the node ID	RW	11'h0

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5.3.4.96 por_hnf_rn_phys_id29

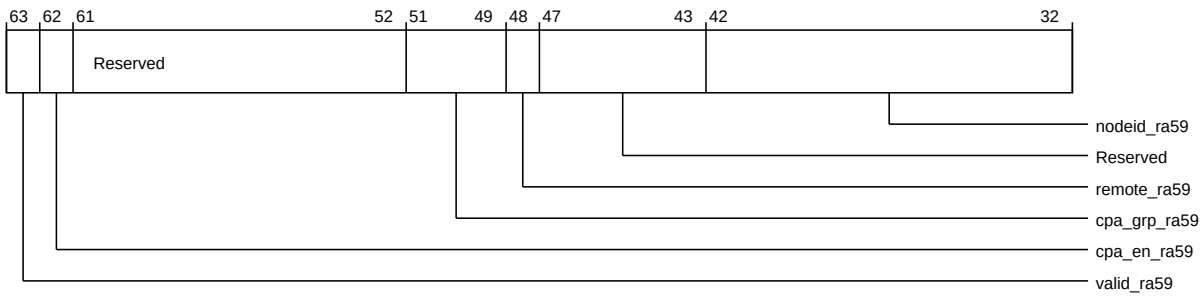
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-494: por_hnf_por_hnf_rn_phys_id29 (high)



The following table shows the por_hnf_rn_phys_id29 higher register bit assignments.

Table 5-508: por_hnf_por_hnf_rn_phys_id29 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra59	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra59	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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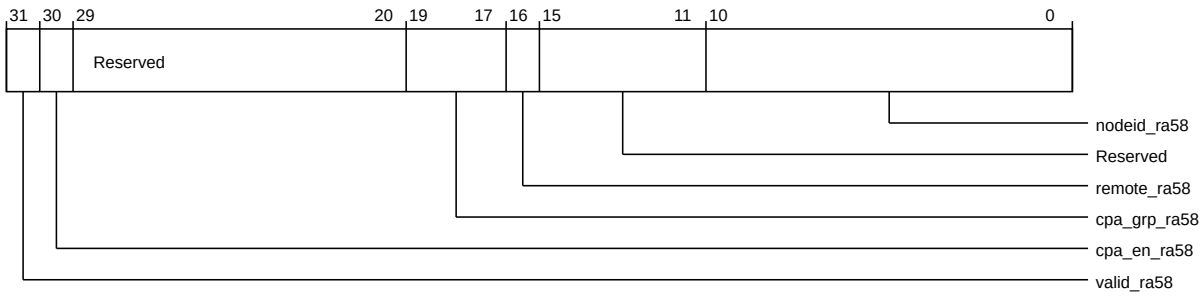
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra59	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra59	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra59	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-495: por_hnf_por_hnf_rn_phys_id29 (low)



The following table shows the por_hnf_rn_phys_id29 lower register bit assignments.

Table 5-509: por_hnf_por_hnf_rn_phys_id29 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra58	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra58	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra58	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra58	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra58	Specifies the node ID	RW	11'h0

5.3.4.97 por_hnf_rn_phys_id30

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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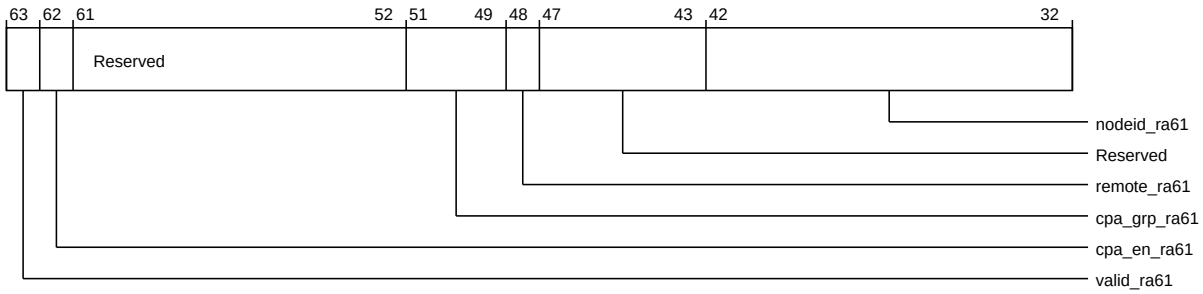
Figure 5-496: por_hnf_por_hnf_rn_phys_id30 (high)



The following table shows the por_hnf_rn_phys_id30 higher register bit assignments.

Table 5-510: por_hnf_por_hnf_rn_phys_id30 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra61	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra61	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra61	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra61	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra61	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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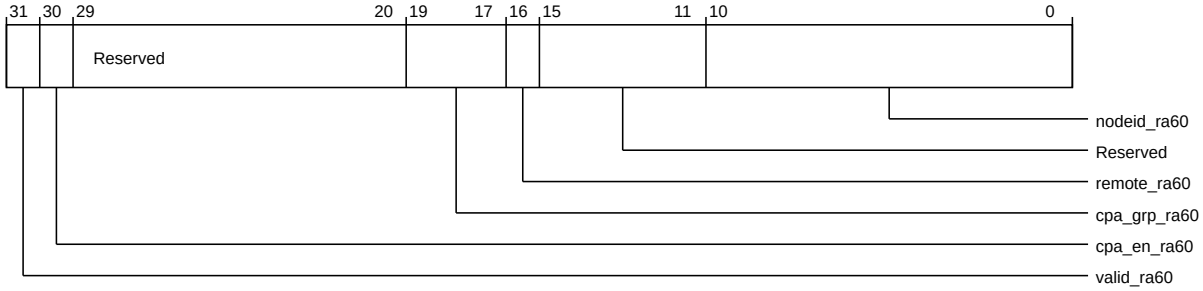
Figure 5-497: por_hnf_por_hnf_rn_phys_id30 (low)



The following table shows the por_hnf_rn_phys_id30 lower register bit assignments.

Table 5-511: por_hnf_por_hnf_rn_phys_id30 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra60	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra60	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra60	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra60	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra60	Specifies the node ID	RW	11'h0

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5.3.4.98 por_hnf_rn_phys_id31

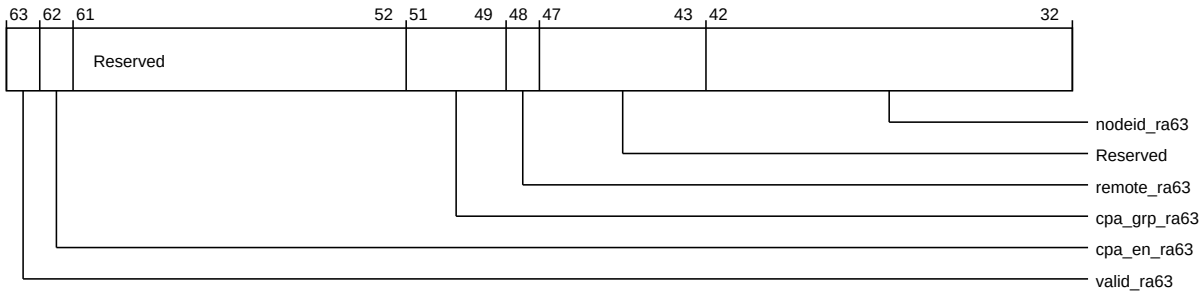
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-498: por_hnf_por_hnf_rn_phys_id31 (high)



The following table shows the por_hnf_rn_phys_id31 higher register bit assignments.

Table 5-512: por_hnf_por_hnf_rn_phys_id31 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra63	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra63	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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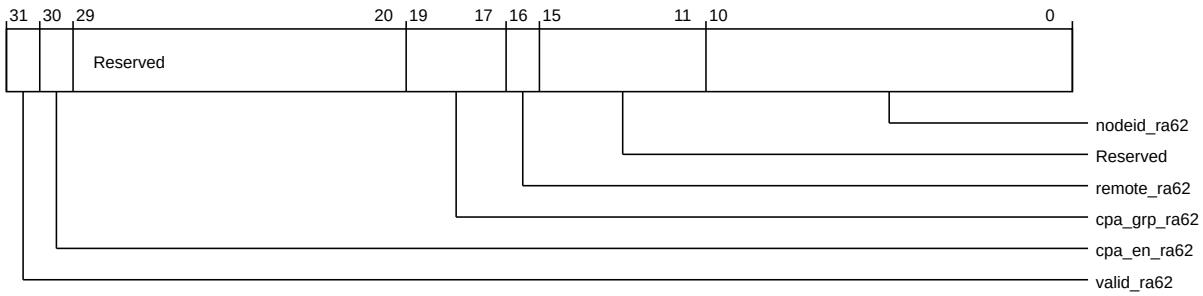
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra63	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra63	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra63	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-499: por_hnf_por_hnf_rn_phys_id31 (low)



The following table shows the por_hnf_rn_phys_id31 lower register bit assignments.

Table 5-513: por_hnf_por_hnf_rn_phys_id31 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra62	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra62	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra62	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra62	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra62	Specifies the node ID	RW	11'h0

5.3.4.99 por_hnf_rn_phys_id32

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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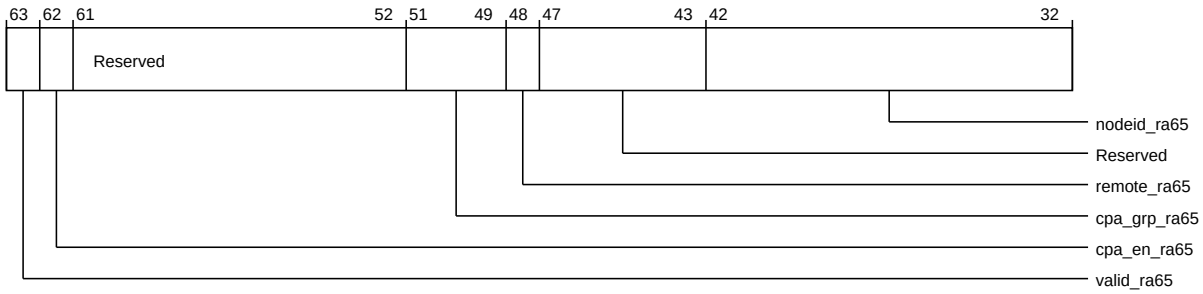
Figure 5-500: por_hnf_por_hnf_rn_phys_id32 (high)



The following table shows the por_hnf_rn_phys_id32 higher register bit assignments.

Table 5-514: por_hnf_por_hnf_rn_phys_id32 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra65	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra65	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra65	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra65	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra65	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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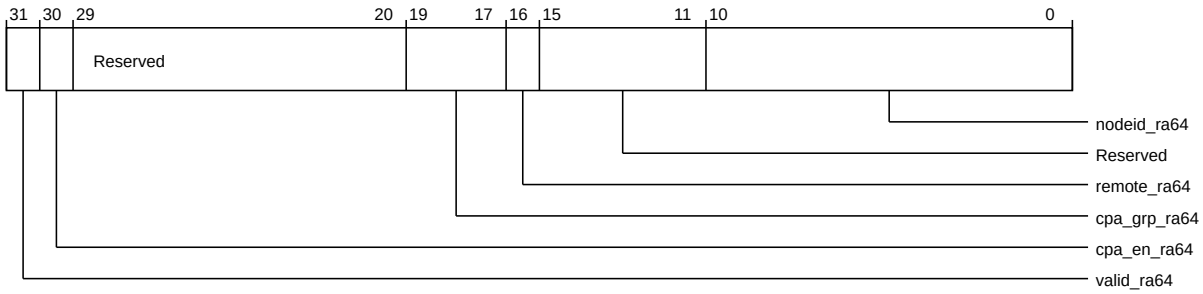
Figure 5-501: por_hnf_por_hnf_rn_phys_id32 (low)



The following table shows the por_hnf_rn_phys_id32 lower register bit assignments.

Table 5-515: por_hnf_por_hnf_rn_phys_id32 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra64	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra64	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra64	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra64	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra64	Specifies the node ID	RW	11'h0

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5.3.4.100 por_hnf_rn_phys_id33

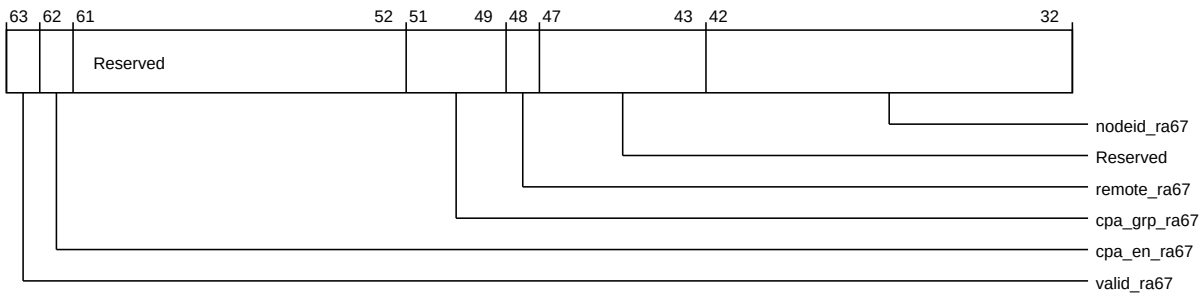
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-502: por_hnf_por_hnf_rn_phys_id33 (high)



The following table shows the por_hnf_rn_phys_id33 higher register bit assignments.

Table 5-516: por_hnf_por_hnf_rn_phys_id33 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra67	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra67	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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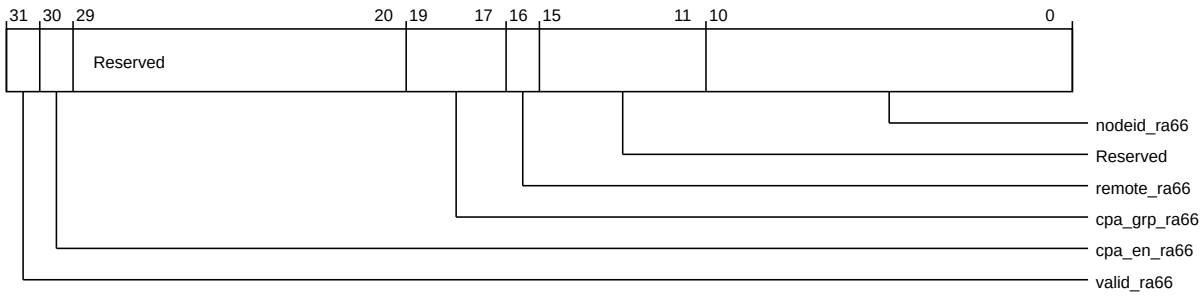
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra67	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra67	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra67	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-503: por_hnf_por_hnf_rn_phys_id33 (low)



The following table shows the por_hnf_rn_phys_id33 lower register bit assignments.

Table 5-517: por_hnf_por_hnf_rn_phys_id33 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra66	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra66	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra66	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra66	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra66	Specifies the node ID	RW	11'h0

5.3.4.101 por_hnf_rn_phys_id34

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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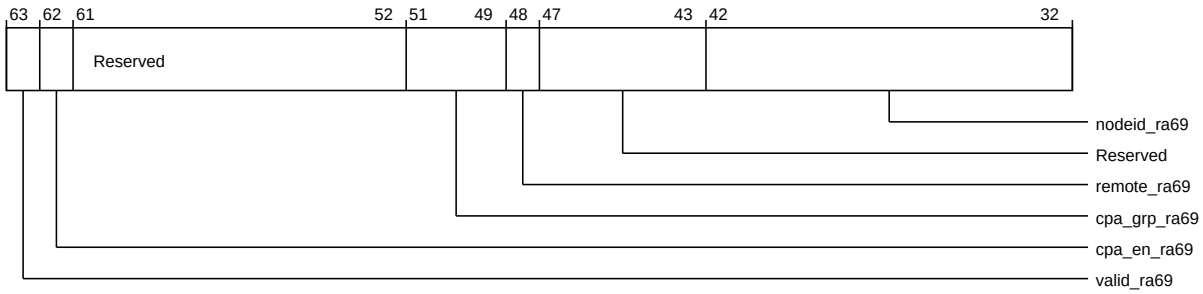
Figure 5-504: por_hnf_por_hnf_rn_phys_id34 (high)



The following table shows the por_hnf_rn_phys_id34 higher register bit assignments.

Table 5-518: por_hnf_por_hnf_rn_phys_id34 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra69	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra69	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra69	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra69	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra69	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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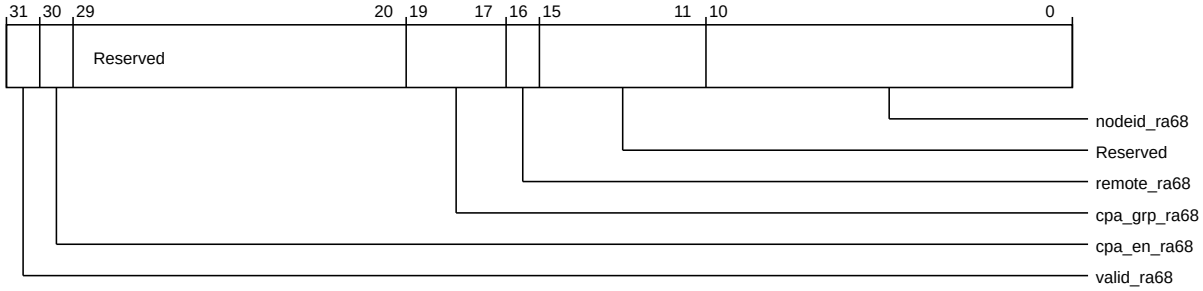
Figure 5-505: por_hnf_por_hnf_rn_phys_id34 (low)



The following table shows the por_hnf_rn_phys_id34 lower register bit assignments.

Table 5-519: por_hnf_por_hnf_rn_phys_id34 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra68	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra68	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra68	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra68	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra68	Specifies the node ID	RW	11'h0

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5.3.4.102 por_hnf_rn_phys_id35

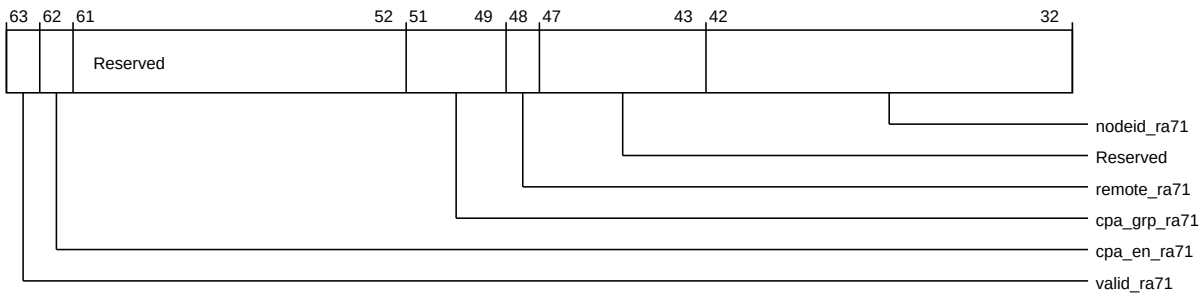
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-506: por_hnf_por_hnf_rn_phys_id35 (high)



The following table shows the por_hnf_rn_phys_id35 higher register bit assignments.

Table 5-520: por_hnf_por_hnf_rn_phys_id35 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra71	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra71	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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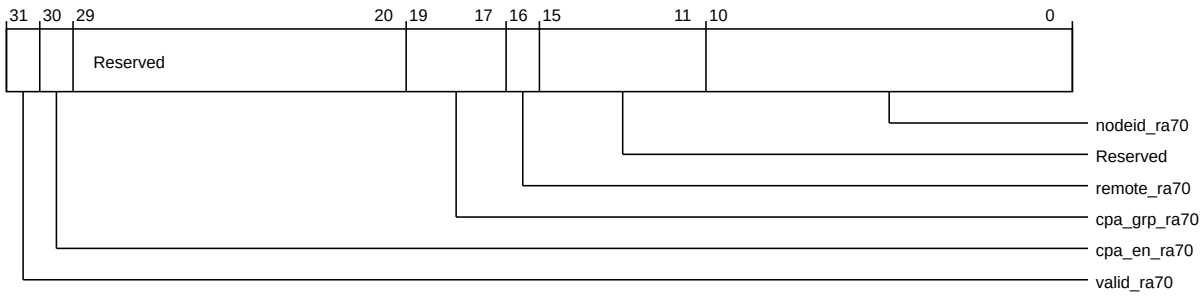
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra71	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra71	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra71	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-507: por_hnf_por_hnf_rn_phys_id35 (low)



The following table shows the por_hnf_rn_phys_id35 lower register bit assignments.

Table 5-521: por_hnf_por_hnf_rn_phys_id35 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra70	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra70	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra70	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra70	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra70	Specifies the node ID	RW	11'h0

5.3.4.103 por_hnf_rn_phys_id36

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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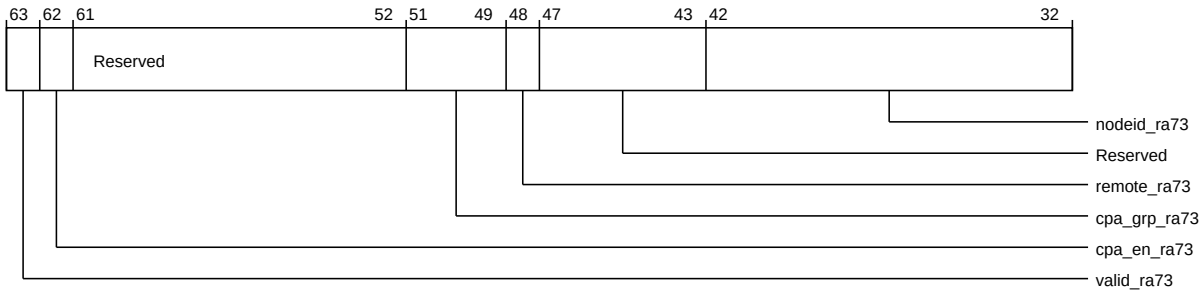
Figure 5-508: por_hnf_por_hnf_rn_phys_id36 (high)



The following table shows the por_hnf_rn_phys_id36 higher register bit assignments.

Table 5-522: por_hnf_por_hnf_rn_phys_id36 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra73	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra73	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra73	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra73	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra73	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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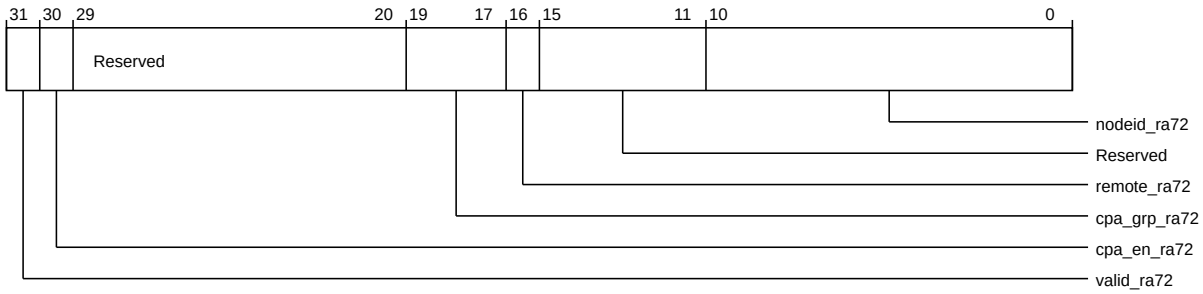
Figure 5-509: por_hnf_por_hnf_rn_phys_id36 (low)



The following table shows the por_hnf_rn_phys_id36 lower register bit assignments.

Table 5-523: por_hnf_por_hnf_rn_phys_id36 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra72	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra72	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra72	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra72	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra72	Specifies the node ID	RW	11'h0

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5.3.4.104 por_hnf_rn_phys_id37

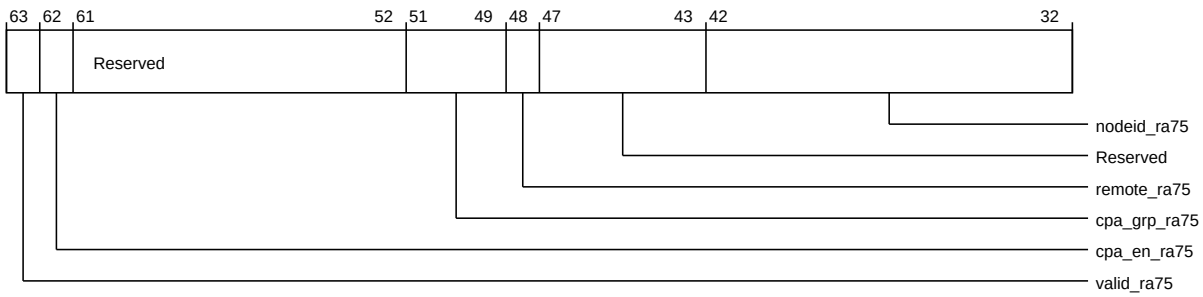
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-510: por_hnf_por_hnf_rn_phys_id37 (high)



The following table shows the por_hnf_rn_phys_id37 higher register bit assignments.

Table 5-524: por_hnf_por_hnf_rn_phys_id37 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra75	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra75	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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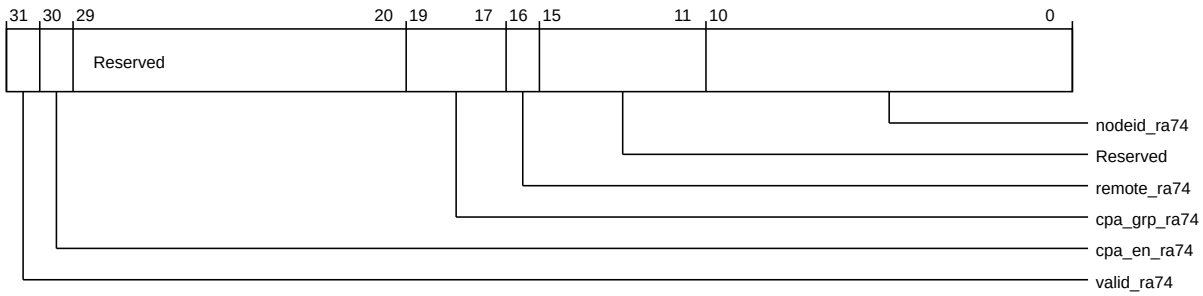
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra75	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra75	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra75	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-511: por_hnf_por_hnf_rn_phys_id37 (low)



The following table shows the por_hnf_rn_phys_id37 lower register bit assignments.

Table 5-525: por_hnf_por_hnf_rn_phys_id37 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra74	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra74	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra74	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra74	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra74	Specifies the node ID	RW	11'h0

5.3.4.105 por_hnf_rn_phys_id38

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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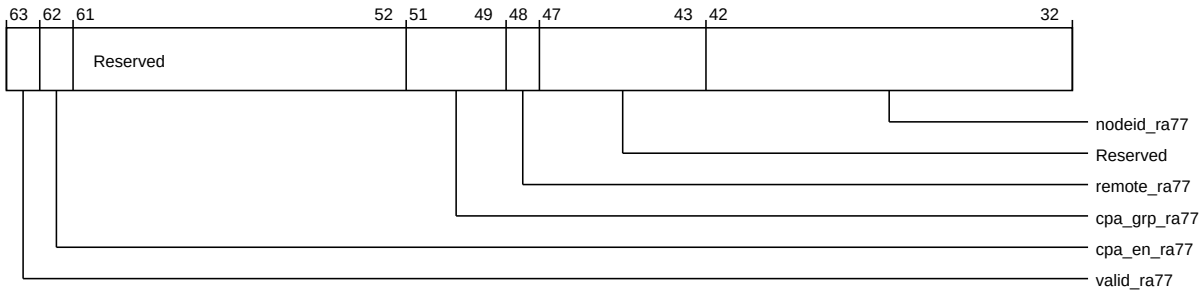
Figure 5-512: por_hnf_por_hnf_rn_phys_id38 (high)



The following table shows the por_hnf_rn_phys_id38 higher register bit assignments.

Table 5-526: por_hnf_por_hnf_rn_phys_id38 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra77	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra77	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra77	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra77	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra77	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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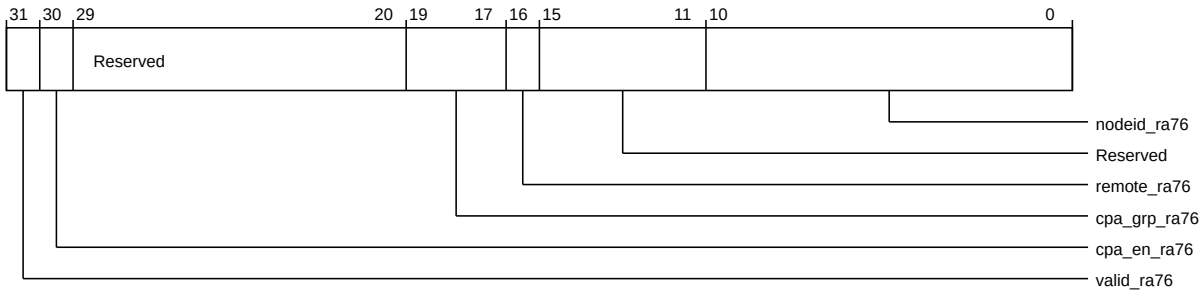
Figure 5-513: por_hnf_por_hnf_rn_phys_id38 (low)



The following table shows the por_hnf_rn_phys_id38 lower register bit assignments.

Table 5-527: por_hnf_por_hnf_rn_phys_id38 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra76	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra76	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra76	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra76	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra76	Specifies the node ID	RW	11'h0

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5.3.4.106 por_hnf_rn_phys_id39

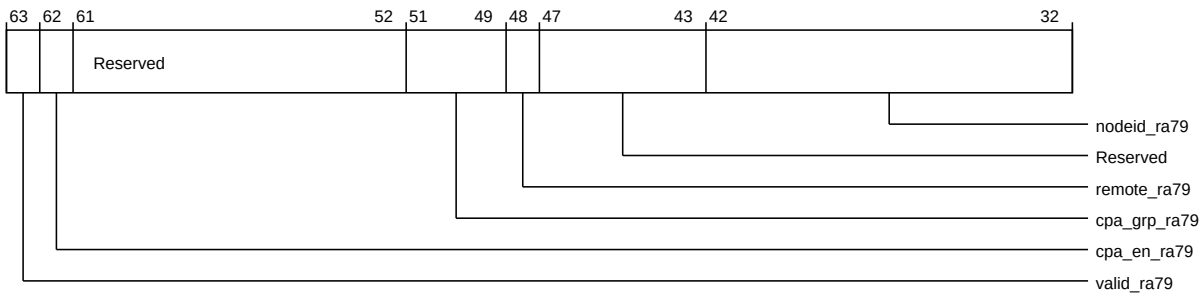
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-514: por_hnf_por_hnf_rn_phys_id39 (high)



The following table shows the por_hnf_rn_phys_id39 higher register bit assignments.

Table 5-528: por_hnf_por_hnf_rn_phys_id39 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra79	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra79	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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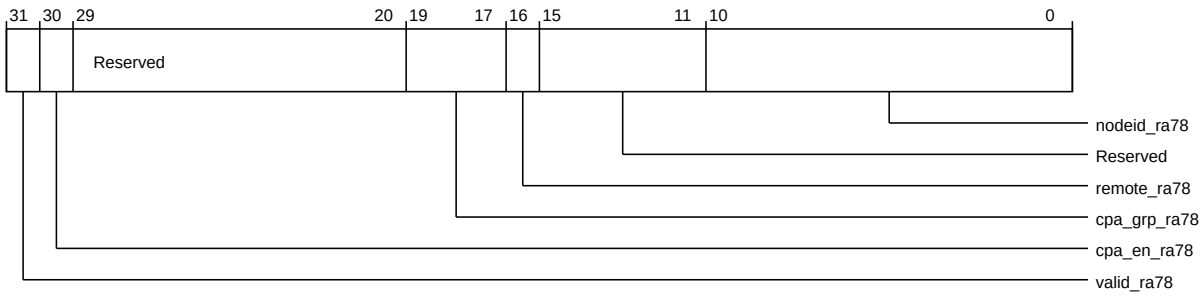
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra79	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra79	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra79	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-515: por_hnf_por_hnf_rn_phys_id39 (low)



The following table shows the por_hnf_rn_phys_id39 lower register bit assignments.

Table 5-529: por_hnf_por_hnf_rn_phys_id39 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra78	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra78	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra78	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra78	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra78	Specifies the node ID	RW	11'h0

5.3.4.107 por_hnf_rn_phys_id40

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE68
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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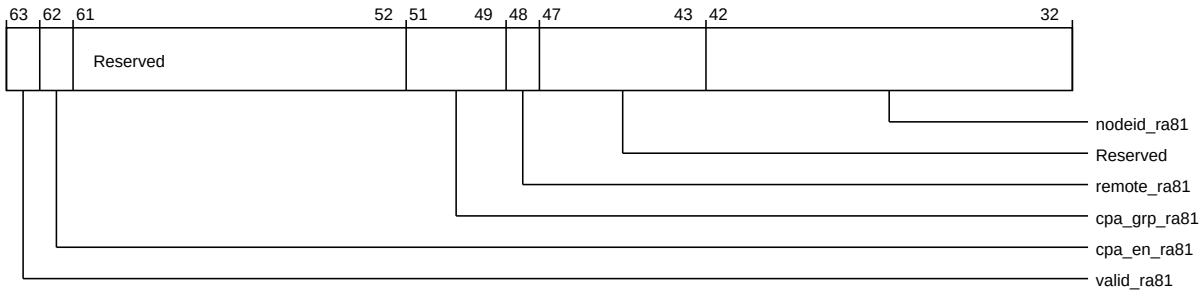
Figure 5-516: por_hnf_por_hnf_rn_phys_id40 (high)



The following table shows the por_hnf_rn_phys_id40 higher register bit assignments.

Table 5-530: por_hnf_por_hnf_rn_phys_id40 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra81	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra81	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra81	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra81	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra81	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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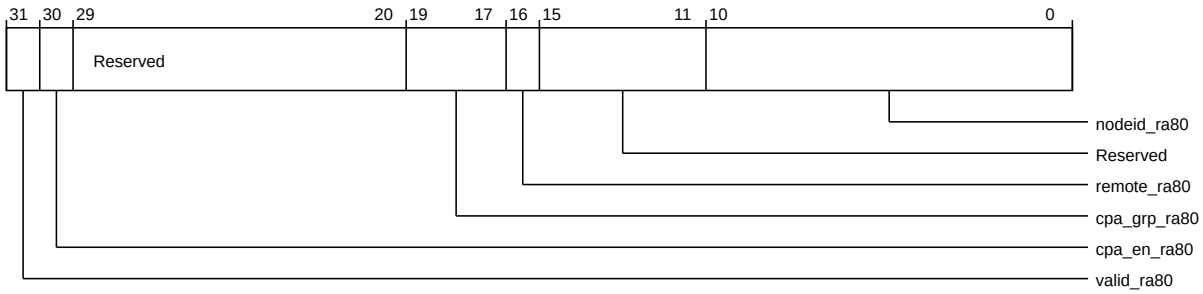
Figure 5-517: por_hnf_por_hnf_rn_phys_id40 (low)



The following table shows the por_hnf_rn_phys_id40 lower register bit assignments.

Table 5-531: por_hnf_por_hnf_rn_phys_id40 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra80	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra80	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra80	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra80	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra80	Specifies the node ID	RW	11'h0

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5.3.4.108 por_hnf_rn_phys_id41

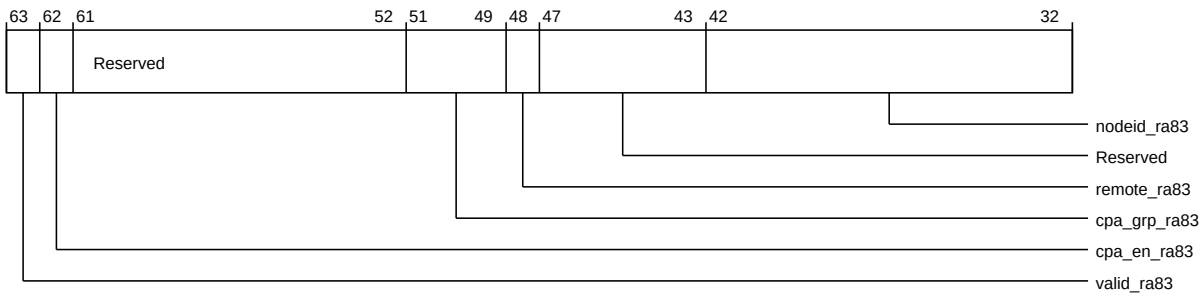
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-518: por_hnf_por_hnf_rn_phys_id41 (high)



The following table shows the por_hnf_rn_phys_id41 higher register bit assignments.

Table 5-532: por_hnf_por_hnf_rn_phys_id41 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra83	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra83	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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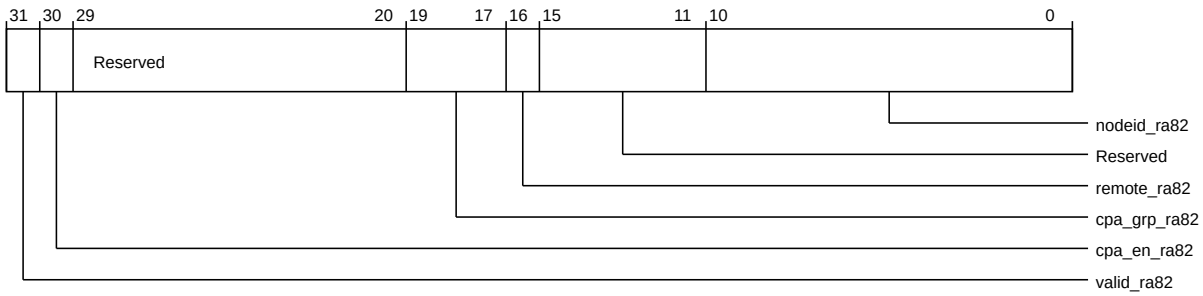
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra83	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra83	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra83	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-519: por_hnf_por_hnf_rn_phys_id41 (low)



The following table shows the por_hnf_rn_phys_id41 lower register bit assignments.

Table 5-533: por_hnf_por_hnf_rn_phys_id41 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra82	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra82	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra82	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra82	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra82	Specifies the node ID	RW	11'h0

5.3.4.109 por_hnf_rn_phys_id42

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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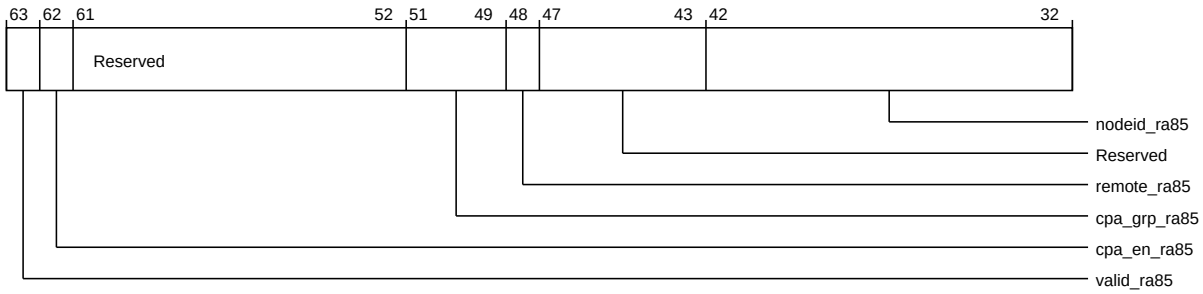
Figure 5-520: por_hnf_por_hnf_rn_phys_id42 (high)



The following table shows the por_hnf_rn_phys_id42 higher register bit assignments.

Table 5-534: por_hnf_por_hnf_rn_phys_id42 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra85	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra85	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra85	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra85	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra85	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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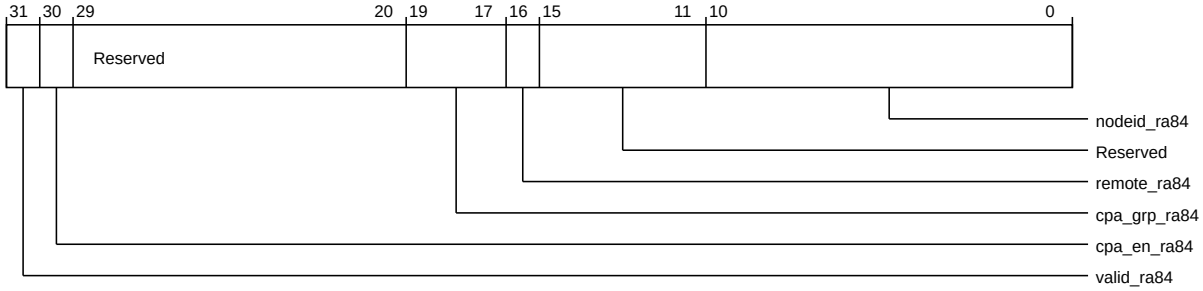
Figure 5-521: por_hnf_por_hnf_rn_phys_id42 (low)



The following table shows the por_hnf_rn_phys_id42 lower register bit assignments.

Table 5-535: por_hnf_por_hnf_rn_phys_id42 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra84	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra84	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra84	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra84	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra84	Specifies the node ID	RW	11'h0

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5.3.4.110 por_hnf_rn_phys_id43

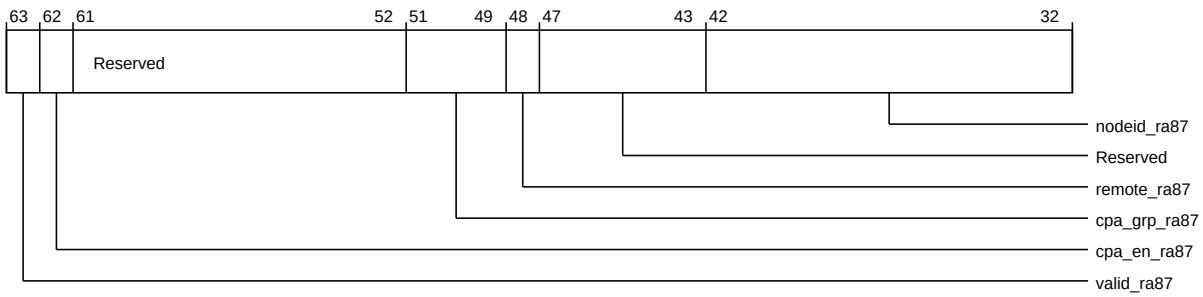
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-522: por_hnf_por_hnf_rn_phys_id43 (high)



The following table shows the por_hnf_rn_phys_id43 higher register bit assignments.

Table 5-536: por_hnf_por_hnf_rn_phys_id43 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra87	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra87	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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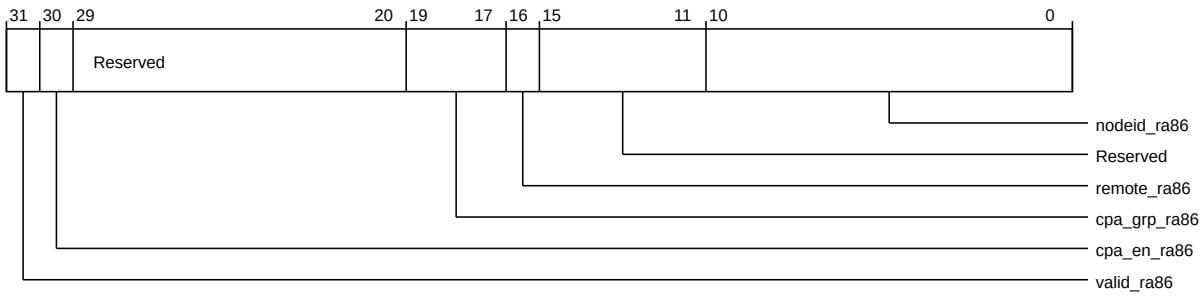
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra87	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra87	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra87	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-523: por_hnf_por_hnf_rn_phys_id43 (low)



The following table shows the por_hnf_rn_phys_id43 lower register bit assignments.

Table 5-537: por_hnf_por_hnf_rn_phys_id43 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra86	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra86	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra86	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra86	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra86	Specifies the node ID	RW	11'h0

5.3.4.111 por_hnf_rn_phys_id44

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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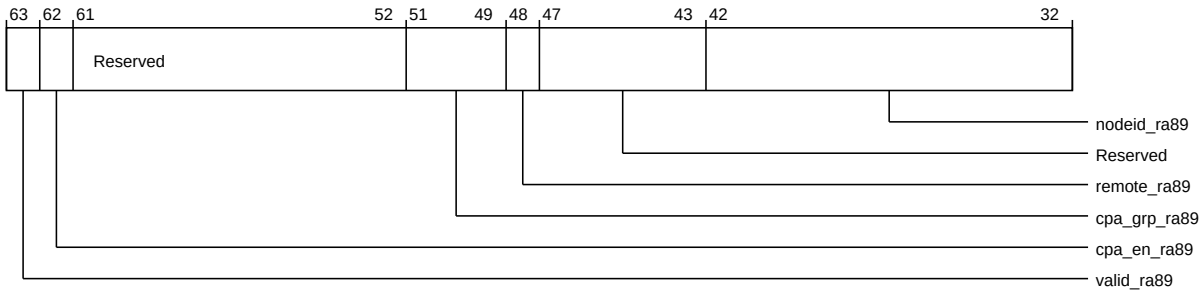
Figure 5-524: por_hnf_por_hnf_rn_phys_id44 (high)



The following table shows the por_hnf_rn_phys_id44 higher register bit assignments.

Table 5-538: por_hnf_por_hnf_rn_phys_id44 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra89	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra89	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra89	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra89	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra89	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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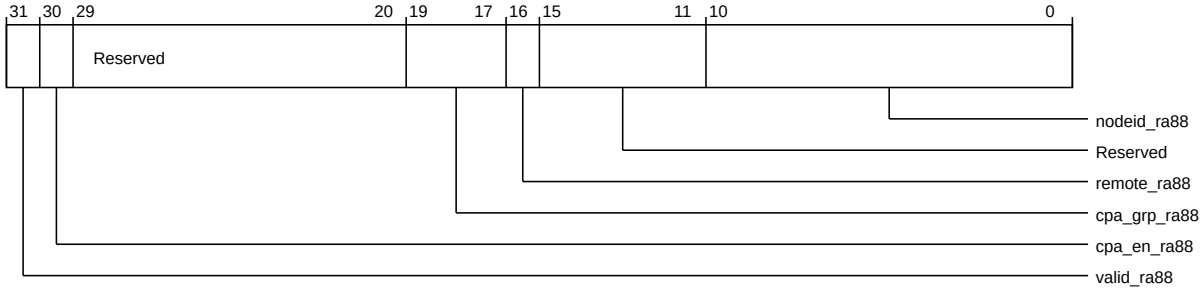
Figure 5-525: por_hnf_por_hnf_rn_phys_id44 (low)



The following table shows the por_hnf_rn_phys_id44 lower register bit assignments.

Table 5-539: por_hnf_por_hnf_rn_phys_id44 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra88	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra88	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra88	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra88	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra88	Specifies the node ID	RW	11'h0

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5.3.4.112 por_hnf_rn_phys_id45

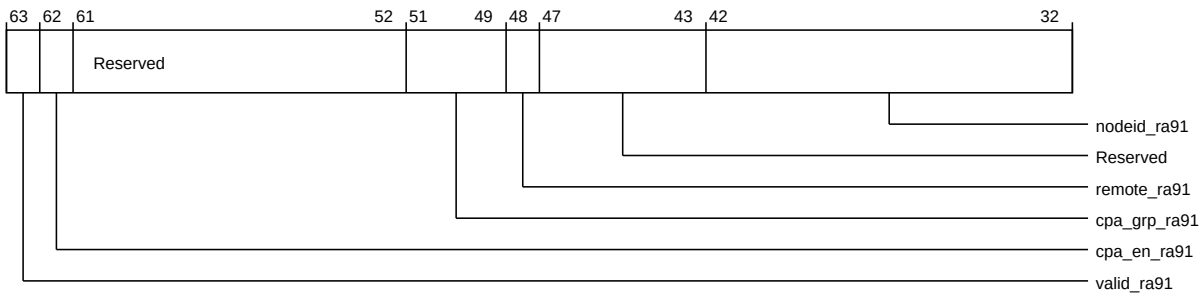
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-526: por_hnf_por_hnf_rn_phys_id45 (high)



The following table shows the por_hnf_rn_phys_id45 higher register bit assignments.

Table 5-540: por_hnf_por_hnf_rn_phys_id45 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra91	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra91	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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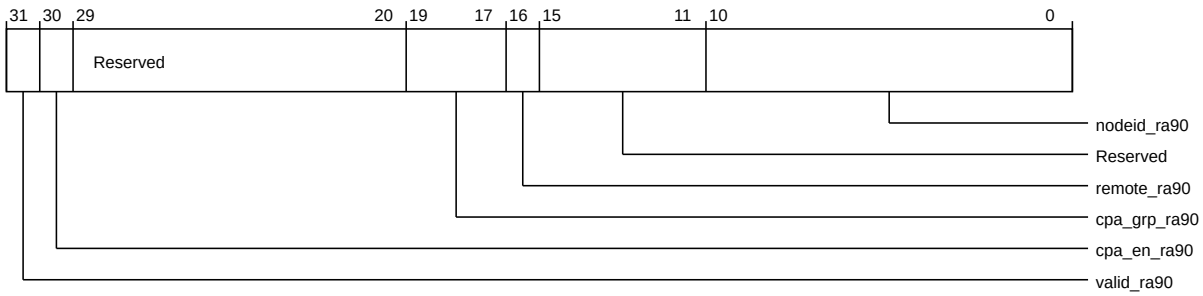
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra91	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra91	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra91	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-527: por_hnf_por_hnf_rn_phys_id45 (low)



The following table shows the por_hnf_rn_phys_id45 lower register bit assignments.

Table 5-541: por_hnf_por_hnf_rn_phys_id45 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra90	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra90	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra90	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra90	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra90	Specifies the node ID	RW	11'h0

5.3.4.113 por_hnf_rn_phys_id46

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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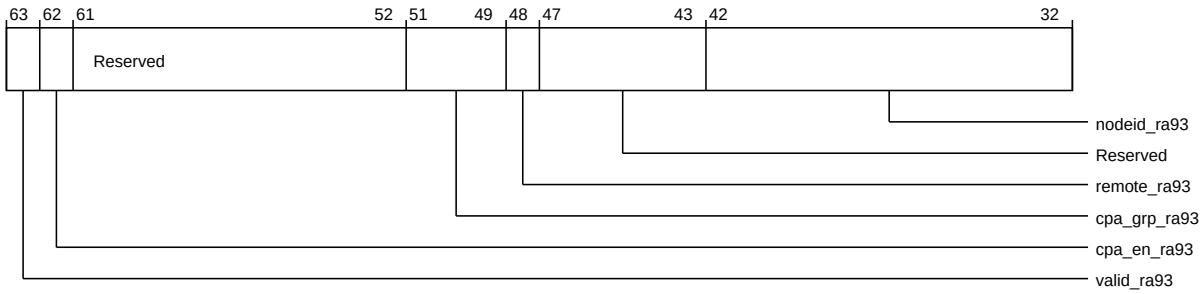
Figure 5-528: por_hnf_por_hnf_rn_phys_id46 (high)



The following table shows the por_hnf_rn_phys_id46 higher register bit assignments.

Table 5-542: por_hnf_por_hnf_rn_phys_id46 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra93	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra93	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra93	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra93	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra93	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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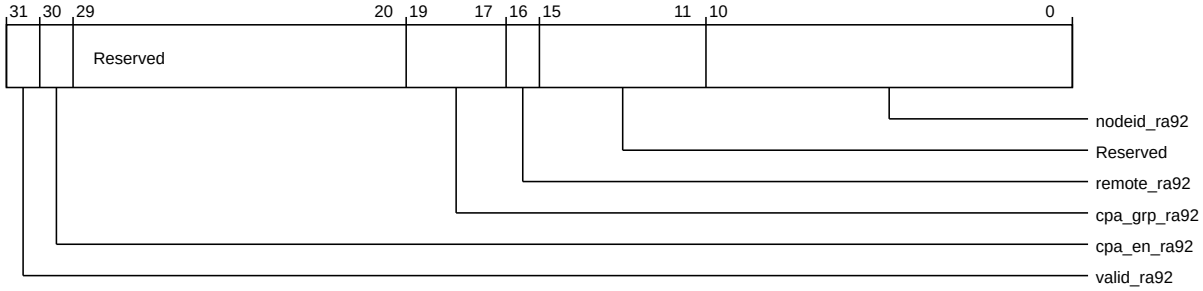
Figure 5-529: por_hnf_por_hnf_rn_phys_id46 (low)



The following table shows the por_hnf_rn_phys_id46 lower register bit assignments.

Table 5-543: por_hnf_por_hnf_rn_phys_id46 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra92	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra92	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra92	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra92	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra92	Specifies the node ID	RW	11'h0

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5.3.4.114 por_hnf_rn_phys_id47

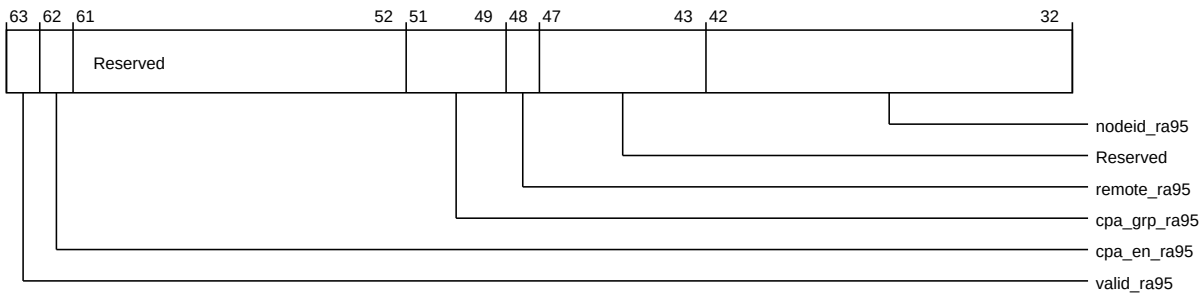
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-530: por_hnf_por_hnf_rn_phys_id47 (high)



The following table shows the por_hnf_rn_phys_id47 higher register bit assignments.

Table 5-544: por_hnf_por_hnf_rn_phys_id47 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra95	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra95	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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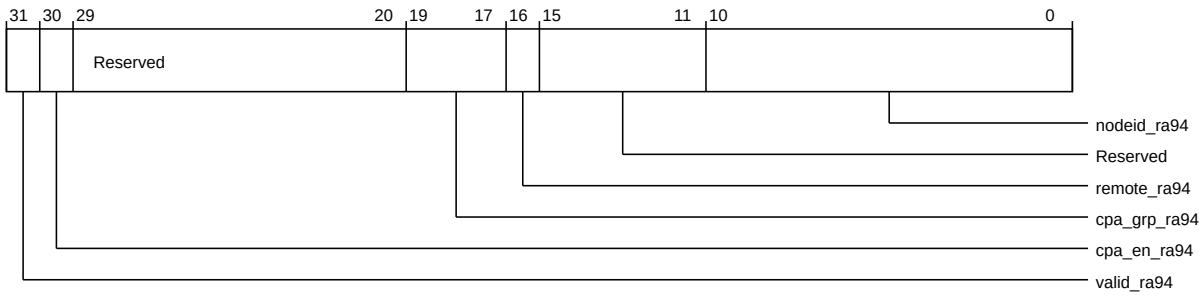
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra95	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra95	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra95	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-531: por_hnf_por_hnf_rn_phys_id47 (low)



The following table shows the por_hnf_rn_phys_id47 lower register bit assignments.

Table 5-545: por_hnf_por_hnf_rn_phys_id47 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra94	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra94	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra94	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra94	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra94	Specifies the node ID	RW	11'h0

5.3.4.115 por_hnf_rn_phys_id48

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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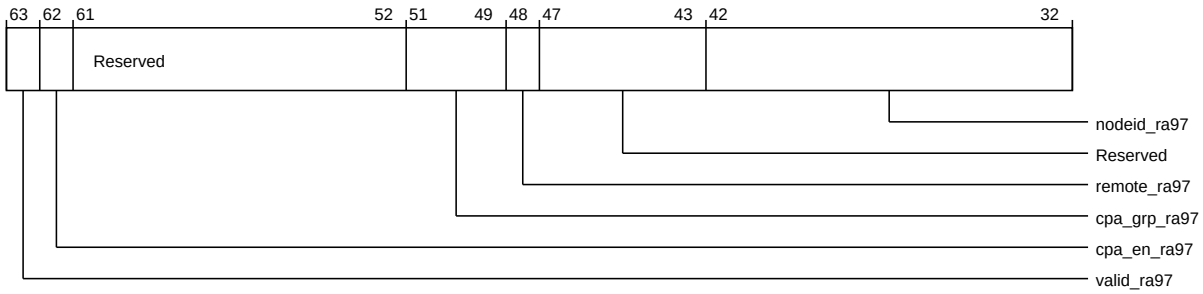
Figure 5-532: por_hnf_por_hnf_rn_phys_id48 (high)



The following table shows the por_hnf_rn_phys_id48 higher register bit assignments.

Table 5-546: por_hnf_por_hnf_rn_phys_id48 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra97	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra97	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra97	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra97	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra97	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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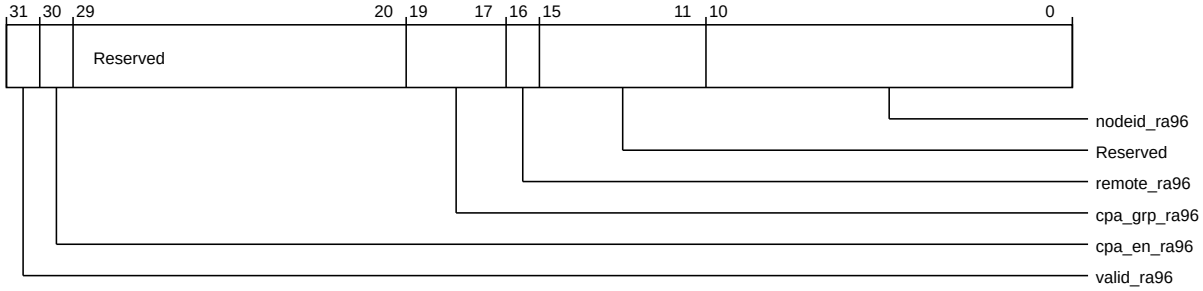
Figure 5-533: por_hnf_por_hnf_rn_phys_id48 (low)



The following table shows the por_hnf_rn_phys_id48 lower register bit assignments.

Table 5-547: por_hnf_por_hnf_rn_phys_id48 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra96	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra96	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra96	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra96	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra96	Specifies the node ID	RW	11'h0

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5.3.4.116 por_hnf_rn_phys_id49

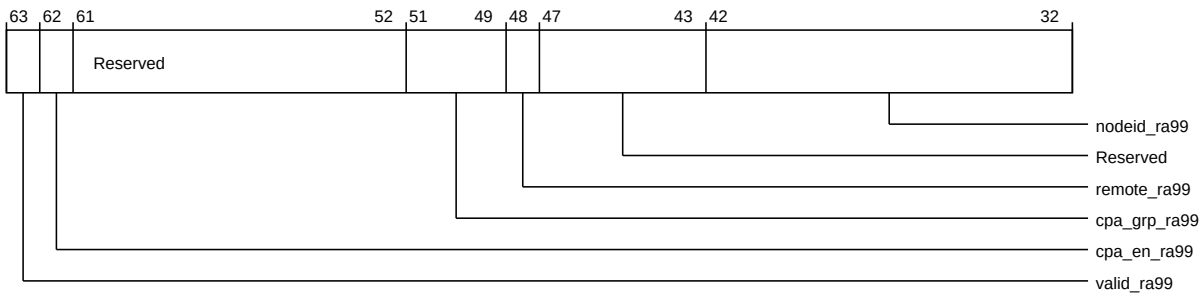
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-534: por_hnf_por_hnf_rn_phys_id49 (high)



The following table shows the por_hnf_rn_phys_id49 higher register bit assignments.

Table 5-548: por_hnf_por_hnf_rn_phys_id49 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra99	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra99	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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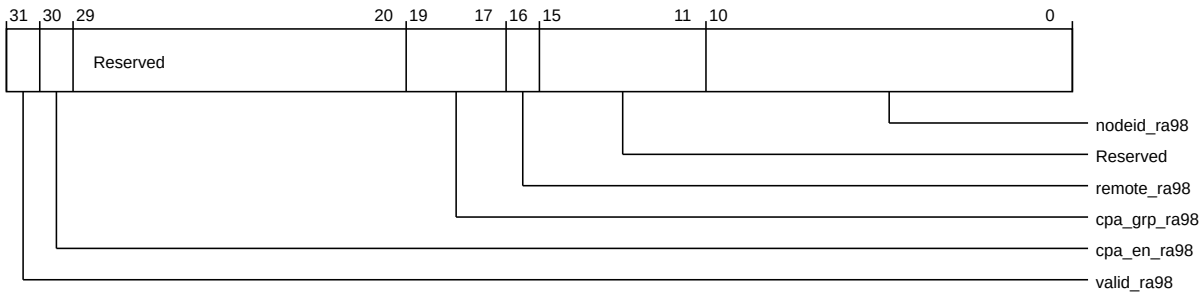
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra99	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra99	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra99	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-535: por_hnf_por_hnf_rn_phys_id49 (low)



The following table shows the por_hnf_rn_phys_id49 lower register bit assignments.

Table 5-549: por_hnf_por_hnf_rn_phys_id49 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra98	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra98	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra98	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra98	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra98	Specifies the node ID	RW	11'h0

5.3.4.117 por_hnf_rn_phys_id50

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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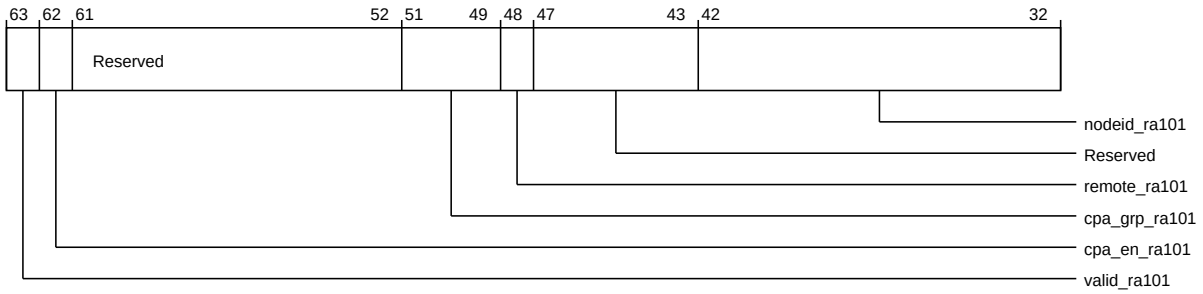
Figure 5-536: por_hnf_por_hnf_rn_phys_id50 (high)



The following table shows the por_hnf_rn_phys_id50 higher register bit assignments.

Table 5-550: por_hnf_por_hnf_rn_phys_id50 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra101	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra101	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra101	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra101	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra101	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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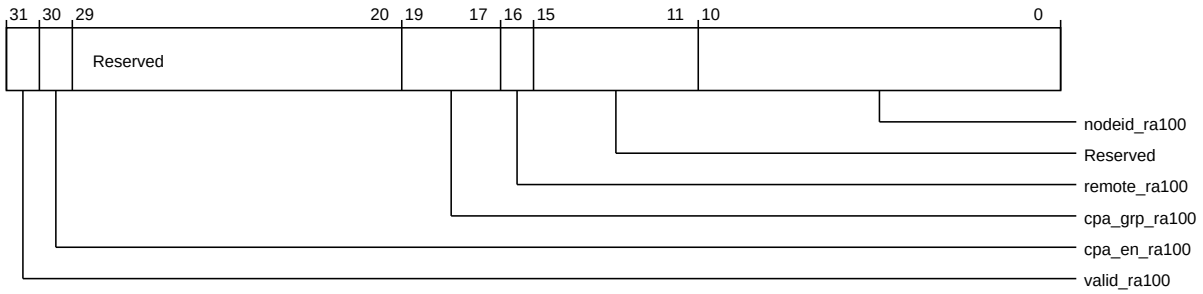
Figure 5-537: por_hnf_por_hnf_rn_phys_id50 (low)



The following table shows the por_hnf_rn_phys_id50 lower register bit assignments.

Table 5-551: por_hnf_por_hnf_rn_phys_id50 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra100	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra100	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra100	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra100	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra100	Specifies the node ID	RW	11'h0

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5.3.4.118 por_hnf_rn_phys_id51

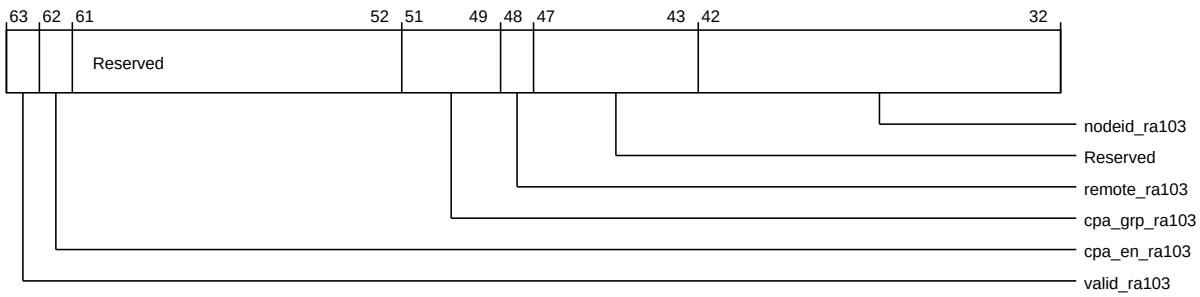
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-538: por_hnf_por_hnf_rn_phys_id51 (high)



The following table shows the por_hnf_rn_phys_id51 higher register bit assignments.

Table 5-552: por_hnf_por_hnf_rn_phys_id51 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra103	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra103	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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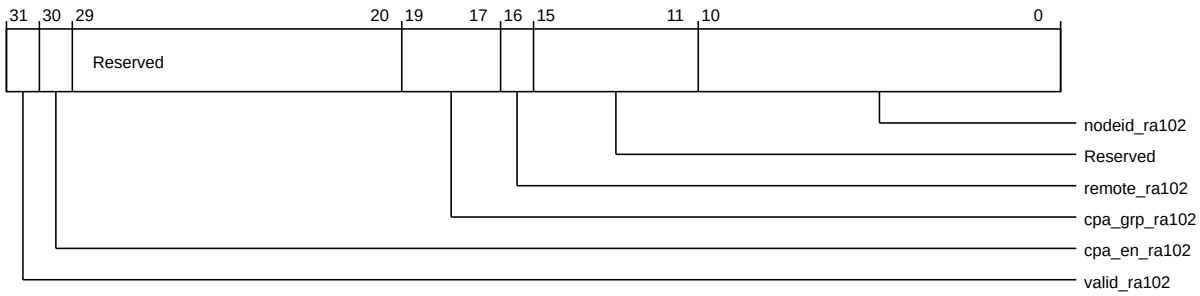
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra103	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra103	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra103	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-539: por_hnf_por_hnf_rn_phys_id51 (low)



The following table shows the por_hnf_rn_phys_id51 lower register bit assignments.

Table 5-553: por_hnf_por_hnf_rn_phys_id51 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra102	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra102	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra102	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra102	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra102	Specifies the node ID	RW	11'h0

5.3.4.119 por_hnf_rn_phys_id52

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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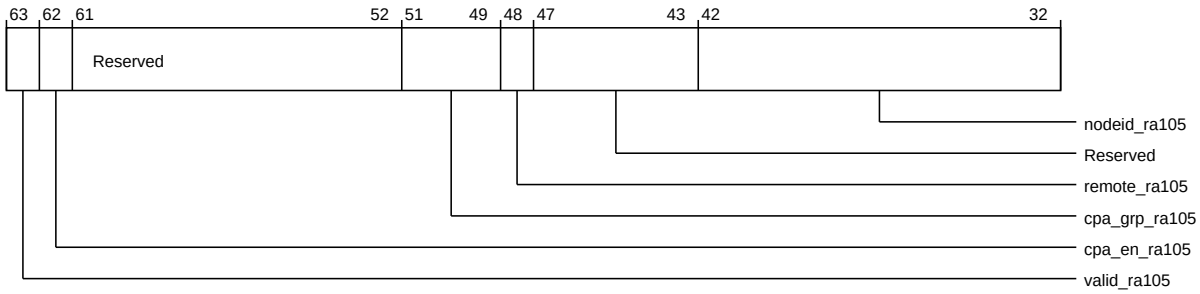
Figure 5-540: por_hnf_por_hnf_rn_phys_id52 (high)



The following table shows the por_hnf_rn_phys_id52 higher register bit assignments.

Table 5-554: por_hnf_por_hnf_rn_phys_id52 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra105	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra105	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra105	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra105	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra105	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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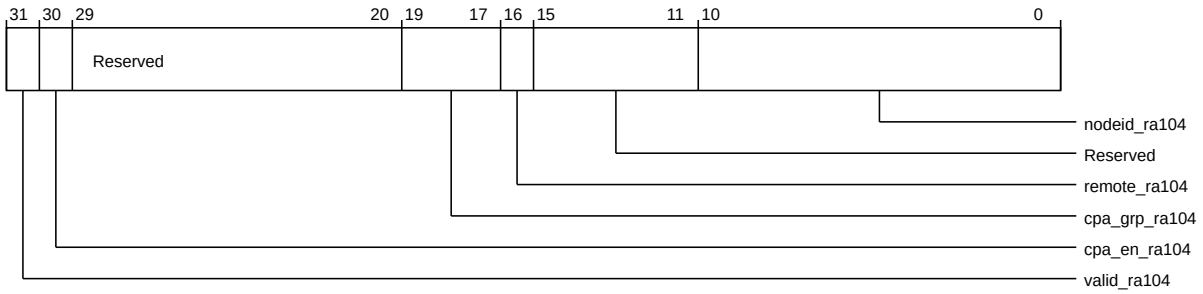
Figure 5-541: por_hnf_por_hnf_rn_phys_id52 (low)



The following table shows the por_hnf_rn_phys_id52 lower register bit assignments.

Table 5-555: por_hnf_por_hnf_rn_phys_id52 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra104	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra104	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra104	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra104	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra104	Specifies the node ID	RW	11'h0

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5.3.4.120 por_hnf_rn_phys_id53

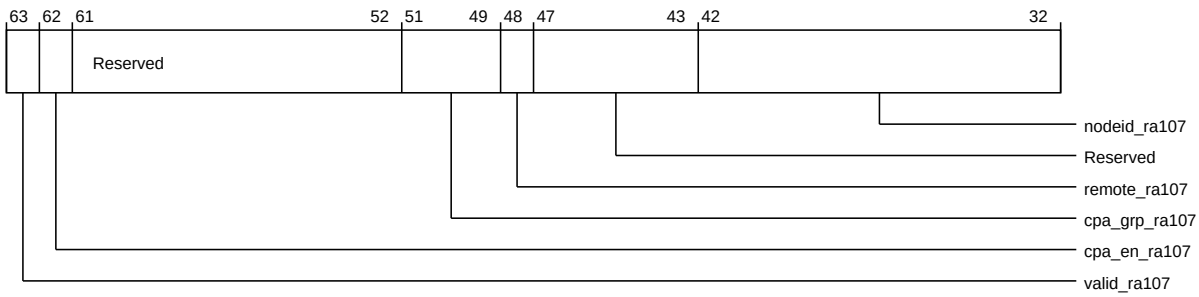
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hED0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-542: por_hnf_por_hnf_rn_phys_id53 (high)



The following table shows the por_hnf_rn_phys_id53 higher register bit assignments.

Table 5-556: por_hnf_por_hnf_rn_phys_id53 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra107	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra107	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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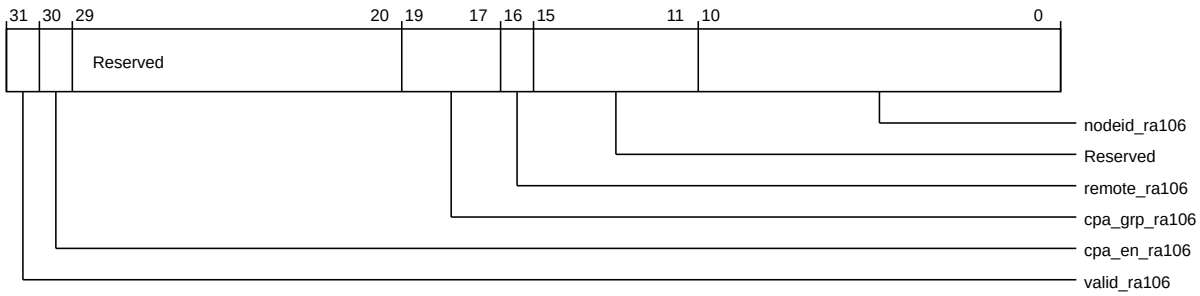
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra107	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra107	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra107	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-543: por_hnf_por_hnf_rn_phys_id53 (low)



The following table shows the por_hnf_rn_phys_id53 lower register bit assignments.

Table 5-557: por_hnf_por_hnf_rn_phys_id53 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra106	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra106	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra106	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra106	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra106	Specifies the node ID	RW	11'h0

5.3.4.121 por_hnf_rn_phys_id54

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hED8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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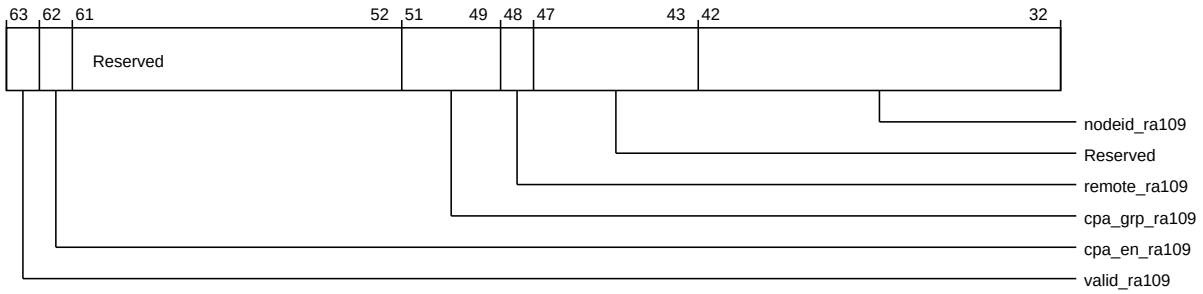
Figure 5-544: por_hnf_por_hnf_rn_phys_id54 (high)



The following table shows the por_hnf_rn_phys_id54 higher register bit assignments.

Table 5-558: por_hnf_por_hnf_rn_phys_id54 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra109	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra109	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra109	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra109	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra109	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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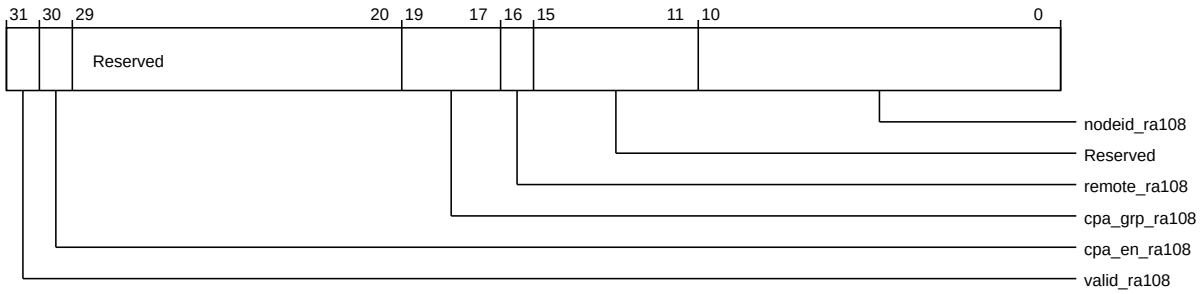
Figure 5-545: por_hnf_por_hnf_rn_phys_id54 (low)



The following table shows the por_hnf_rn_phys_id54 lower register bit assignments.

Table 5-559: por_hnf_por_hnf_rn_phys_id54 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra108	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra108	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra108	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra108	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra108	Specifies the node ID	RW	11'h0

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5.3.4.122 por_hnf_rn_phys_id55

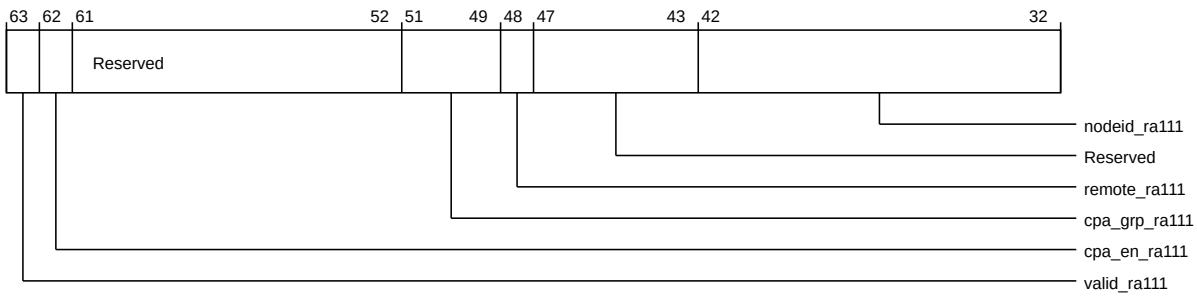
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEE0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-546: por_hnf_por_hnf_rn_phys_id55 (high)



The following table shows the por_hnf_rn_phys_id55 higher register bit assignments.

Table 5-560: por_hnf_por_hnf_rn_phys_id55 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra111	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra111	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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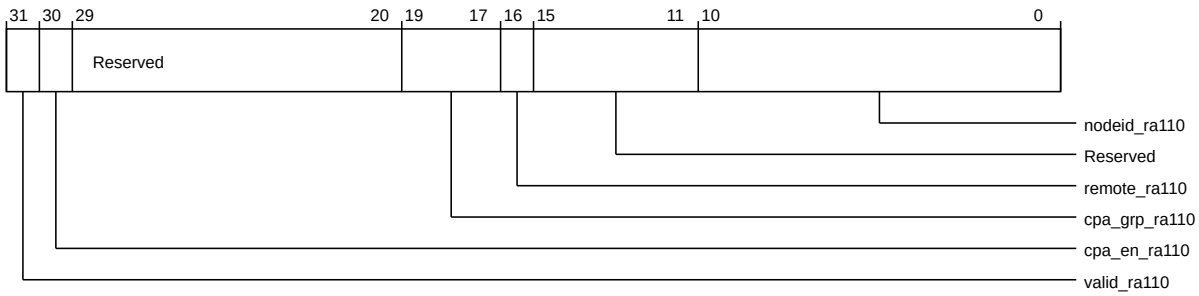
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra111	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra111	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra111	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-547: por_hnf_por_hnf_rn_phys_id55 (low)



The following table shows the por_hnf_rn_phys_id55 lower register bit assignments.

Table 5-561: por_hnf_por_hnf_rn_phys_id55 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra110	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra110	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra110	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra110	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra110	Specifies the node ID	RW	11'h0

5.3.4.123 por_hnf_rn_phys_id56

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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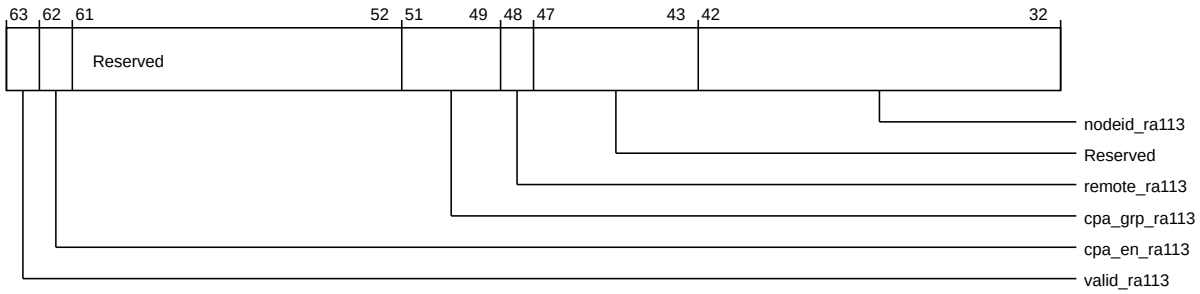
Figure 5-548: por_hnf_por_hnf_rn_phys_id56 (high)



The following table shows the por_hnf_rn_phys_id56 higher register bit assignments.

Table 5-562: por_hnf_por_hnf_rn_phys_id56 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra113	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra113	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra113	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra113	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra113	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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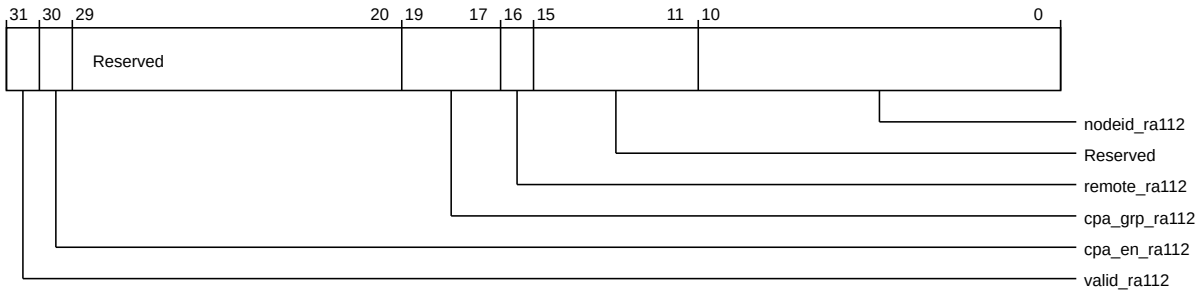
Figure 5-549: por_hnf_por_hnf_rn_phys_id56 (low)



The following table shows the por_hnf_rn_phys_id56 lower register bit assignments.

Table 5-563: por_hnf_por_hnf_rn_phys_id56 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra112	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra112	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra112	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra112	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra112	Specifies the node ID	RW	11'h0

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5.3.4.124 por_hnf_rn_phys_id57

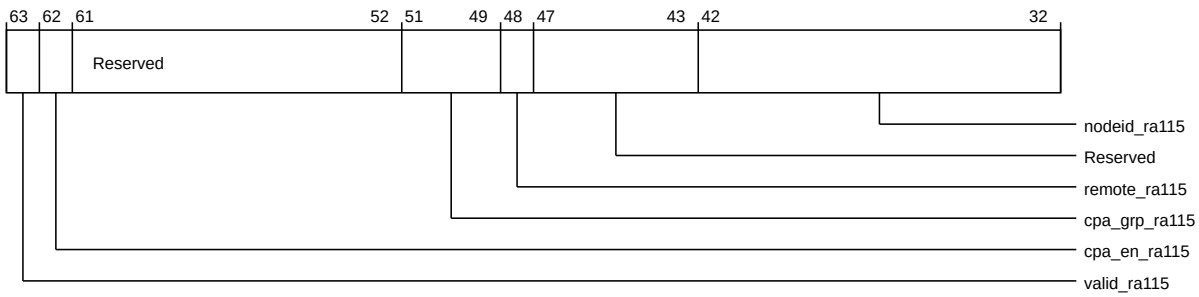
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEF0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-550: por_hnf_por_hnf_rn_phys_id57 (high)



The following table shows the por_hnf_rn_phys_id57 higher register bit assignments.

Table 5-564: por_hnf_por_hnf_rn_phys_id57 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra115	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra115	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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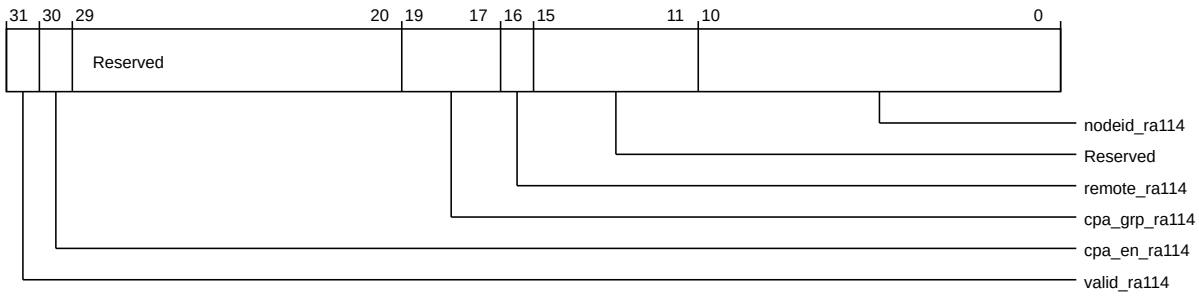
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra115	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra115	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra115	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-551: por_hnf_por_hnf_rn_phys_id57 (low)



The following table shows the por_hnf_rn_phys_id57 lower register bit assignments.

Table 5-565: por_hnf_por_hnf_rn_phys_id57 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra114	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra114	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra114	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra114	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra114	Specifies the node ID	RW	11'h0

5.3.4.125 por_hnf_rn_phys_id58

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEF8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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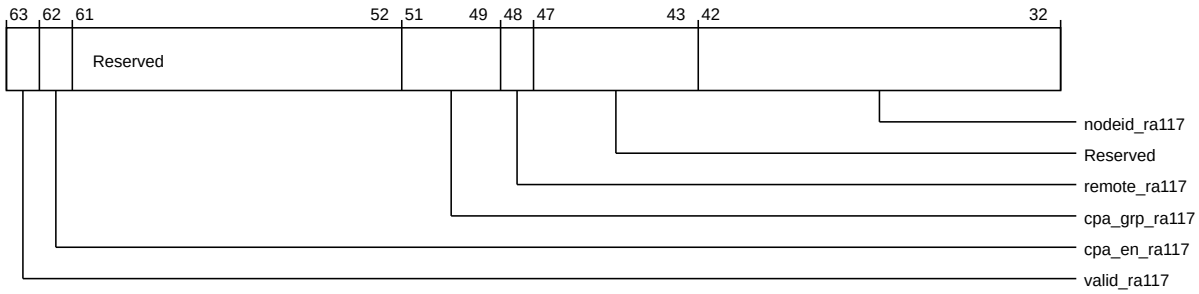
Figure 5-552: por_hnf_por_hnf_rn_phys_id58 (high)



The following table shows the por_hnf_rn_phys_id58 higher register bit assignments.

Table 5-566: por_hnf_por_hnf_rn_phys_id58 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra117	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra117	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra117	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra117	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra117	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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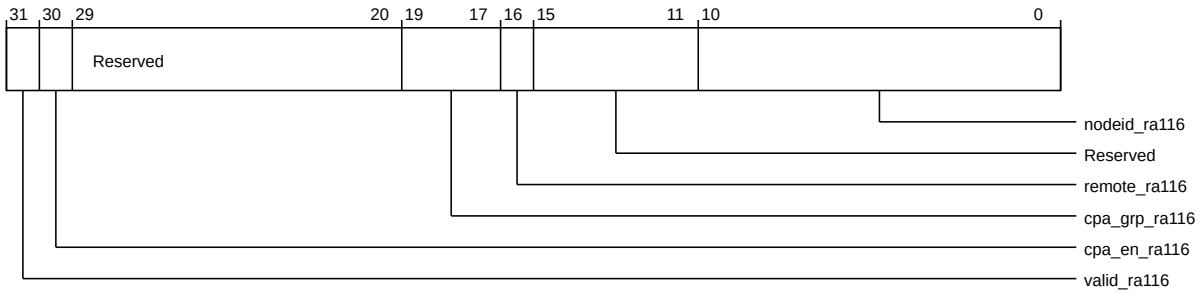
Figure 5-553: por_hnf_por_hnf_rn_phys_id58 (low)



The following table shows the por_hnf_rn_phys_id58 lower register bit assignments.

Table 5-567: por_hnf_por_hnf_rn_phys_id58 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra116	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra116	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra116	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra116	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra116	Specifies the node ID	RW	11'h0

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5.3.4.126 por_hnf_rn_phys_id59

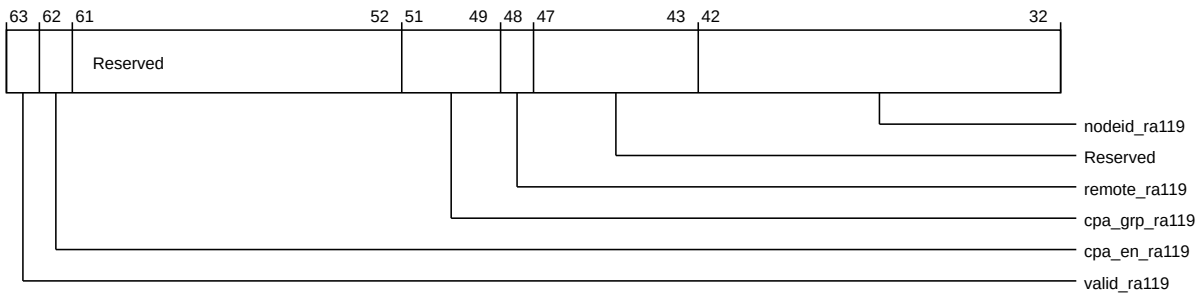
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-554: por_hnf_por_hnf_rn_phys_id59 (high)



The following table shows the por_hnf_rn_phys_id59 higher register bit assignments.

Table 5-568: por_hnf_por_hnf_rn_phys_id59 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra119	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra119	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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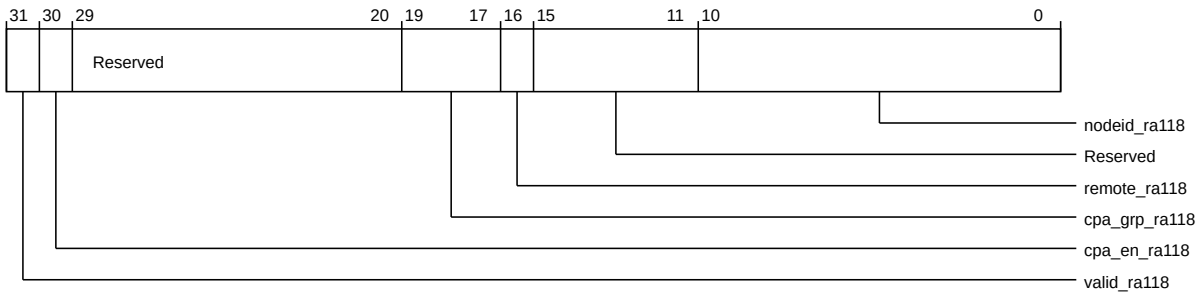
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra119	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra119	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra119	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-555: por_hnf_por_hnf_rn_phys_id59 (low)



The following table shows the por_hnf_rn_phys_id59 lower register bit assignments.

Table 5-569: por_hnf_por_hnf_rn_phys_id59 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra118	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra118	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra118	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra118	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra118	Specifies the node ID	RW	11'h0

5.3.4.127 por_hnf_rn_phys_id60

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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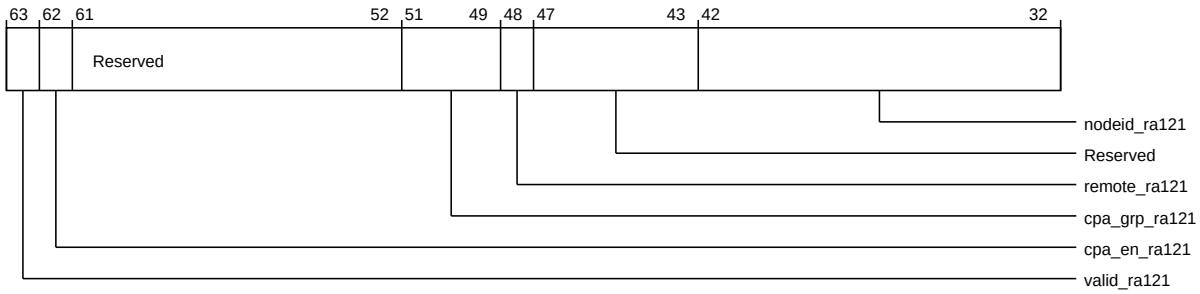
Figure 5-556: por_hnf_por_hnf_rn_phys_id60 (high)



The following table shows the por_hnf_rn_phys_id60 higher register bit assignments.

Table 5-570: por_hnf_por_hnf_rn_phys_id60 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra121	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra121	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra121	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra121	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra121	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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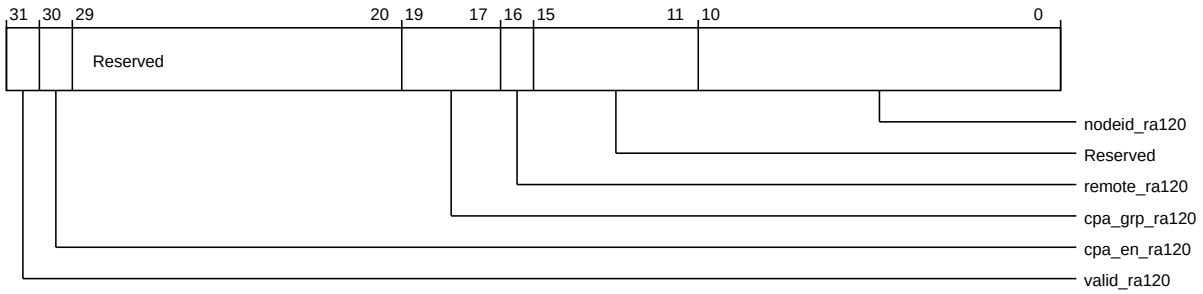
Figure 5-557: por_hnf_por_hnf_rn_phys_id60 (low)



The following table shows the por_hnf_rn_phys_id60 lower register bit assignments.

Table 5-571: por_hnf_por_hnf_rn_phys_id60 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra120	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra120	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra120	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra120	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra120	Specifies the node ID	RW	11'h0

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5.3.4.128 por_hnf_rn_phys_id61

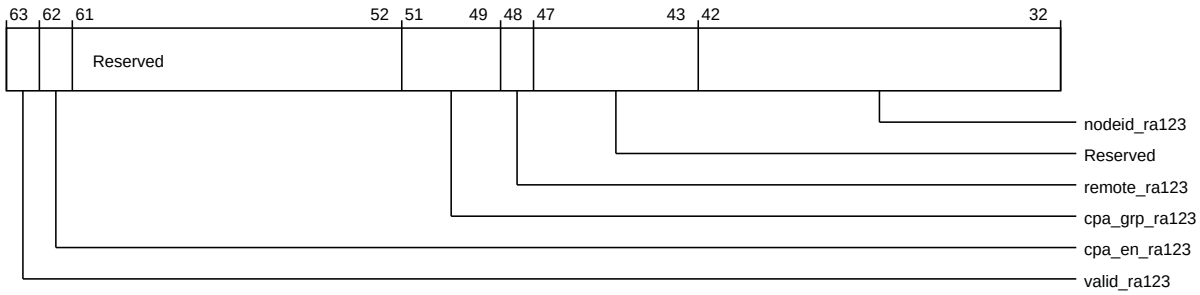
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-558: por_hnf_por_hnf_rn_phys_id61 (high)



The following table shows the por_hnf_rn_phys_id61 higher register bit assignments.

Table 5-572: por_hnf_por_hnf_rn_phys_id61 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra123	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra123	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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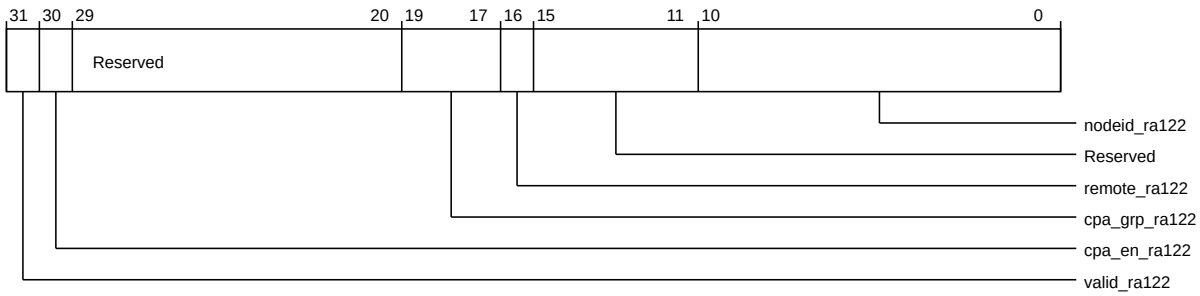
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra123	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra123	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra123	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-559: por_hnf_por_hnf_rn_phys_id61 (low)



The following table shows the por_hnf_rn_phys_id61 lower register bit assignments.

Table 5-573: por_hnf_por_hnf_rn_phys_id61 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra122	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra122	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra122	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra122	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra122	Specifies the node ID	RW	11'h0

5.3.4.129 por_hnf_rn_phys_id62

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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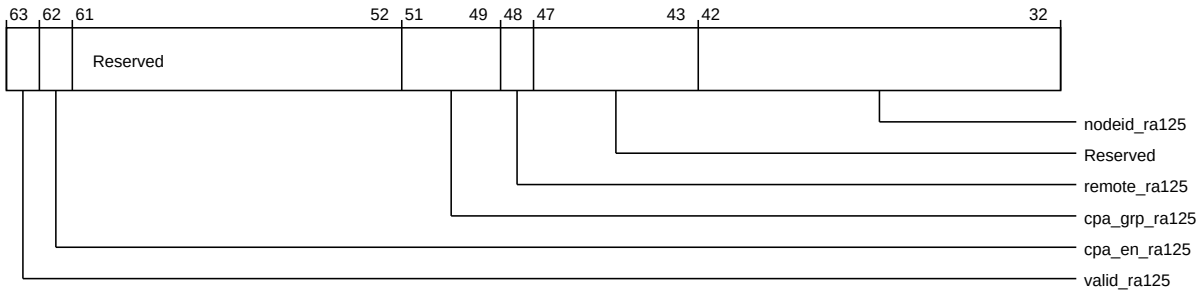
Figure 5-560: por_hnf_por_hnf_rn_phys_id62 (high)



The following table shows the por_hnf_rn_phys_id62 higher register bit assignments.

Table 5-574: por_hnf_por_hnf_rn_phys_id62 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra125	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra125	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-
51:49	cpa_grp_ra125	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra125	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra125	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

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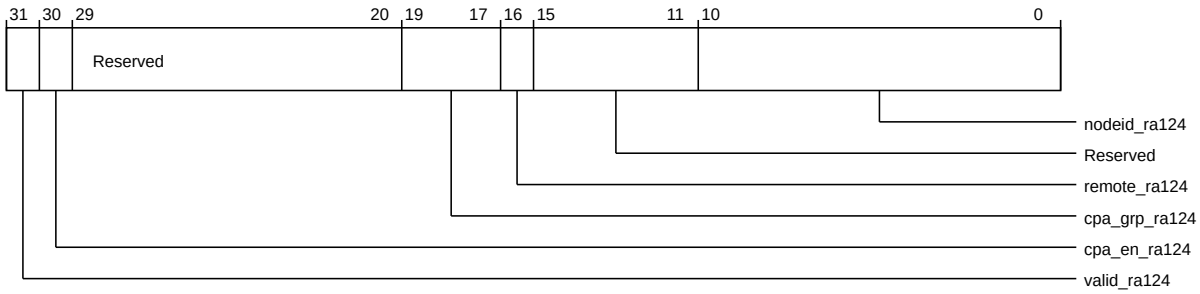
Figure 5-561: por_hnf_por_hnf_rn_phys_id62 (low)



The following table shows the por_hnf_rn_phys_id62 lower register bit assignments.

Table 5-575: por_hnf_por_hnf_rn_phys_id62 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra124	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra124	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-
19:17	cpa_grp_ra124	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra124	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra124	Specifies the node ID	RW	11'h0

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5.3.4.130 por_hnf_rn_phys_id63

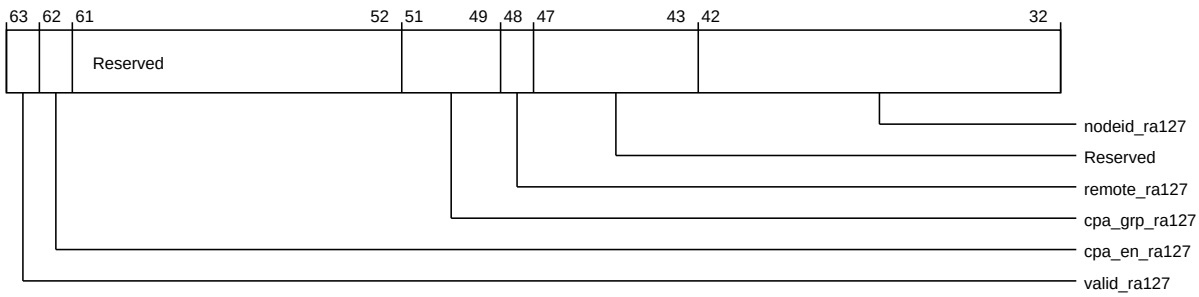
Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-562: por_hnf_por_hnf_rn_phys_id63 (high)



The following table shows the por_hnf_rn_phys_id63 higher register bit assignments.

Table 5-576: por_hnf_por_hnf_rn_phys_id63 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra127	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra127	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:52	Reserved	Reserved	RO	-

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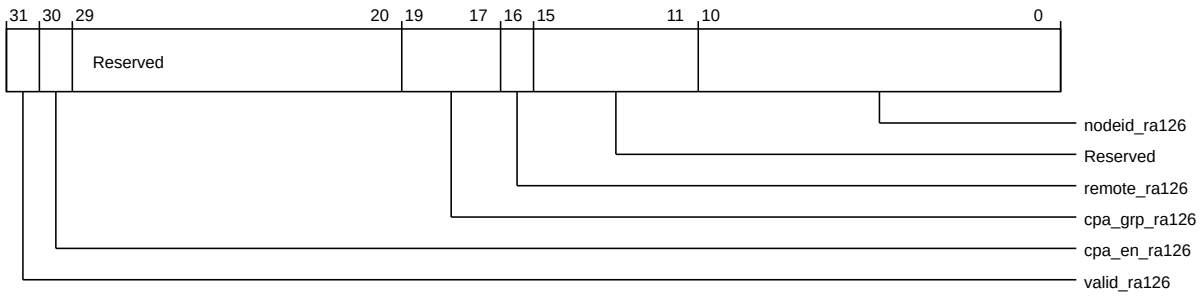
Bits	Field name	Description	Type	Reset
51:49	cpa_grp_ra127	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	remote_ra127	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra127	Specifies the node ID	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-563: por_hnf_por_hnf_rn_phys_id63 (low)



The following table shows the por_hnf_rn_phys_id63 lower register bit assignments.

Table 5-577: por_hnf_por_hnf_rn_phys_id63 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra126	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra126	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:17	cpa_grp_ra126	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
16	remote_ra126	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra126	Specifies the node ID	RW	11'h0

5.3.4.131 por_hnf_ldid_map_table_reg0

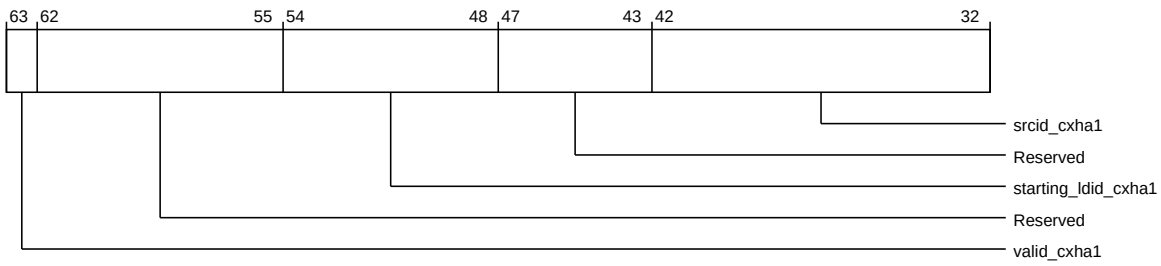
Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-564: por_hnf_por_hnf_ldid_map_table_reg0 (high)



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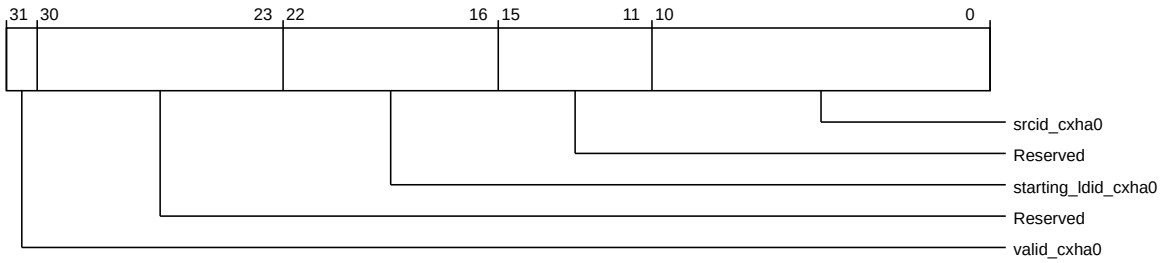
The following table shows the por_hnf_ldid_map_table_reg0 higher register bit assignments.

Table 5-578: por_hnf_por_hnf_ldid_map_table_reg0 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha1	Specifies CXHA 1 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha1	Specifies the starting LDID for RN-F's behind CXHA 1	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha1	Specifies the node ID for CXHA 1	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-565: por_hnf_por_hnf_ldid_map_table_reg0 (low)



The following table shows the por_hnf_ldid_map_table_reg0 lower register bit assignments.

Table 5-579: por_hnf_por_hnf_ldid_map_table_reg0 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha0	Specifies CXHA 0 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha0	Specifies the starting LDID for RN-F's behind CXHA 0	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha0	Specifies the node ID for CXHA 0	RW	11'h0

5.3.4.132 por_hnf_ldid_map_table_reg1

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF30
Register reset 64'b0

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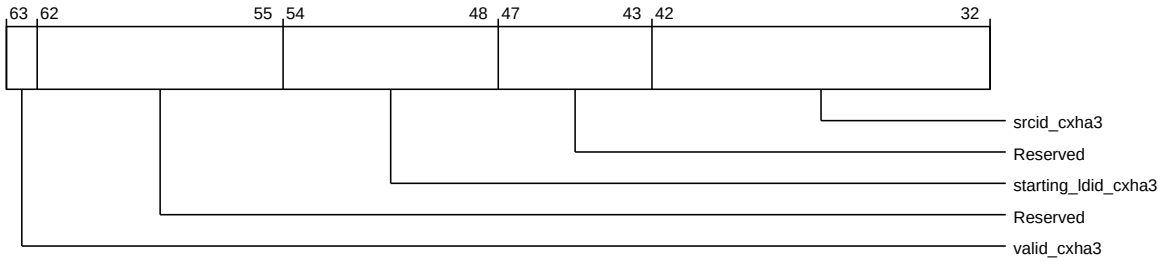
Usage constraints Only accessible by Secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-566: por_hnf_por_hnf_ldid_map_table_reg1 (high)



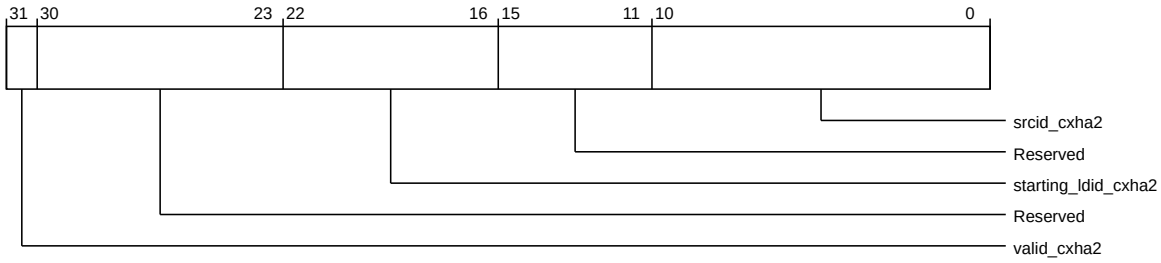
The following table shows the por_hnf_ldid_map_table_reg1 higher register bit assignments.

Table 5-580: por_hnf_por_hnf_ldid_map_table_reg1 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha3	Specifies CXHA 3 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha3	Specifies the starting LDID for RN-F's behind CXHA 3	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha3	Specifies the node ID for CXHA 3	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-567: por_hnf_por_hnf_ldid_map_table_reg1 (low)



The following table shows the por_hnf_ldid_map_table_reg1 lower register bit assignments.

Table 5-581: por_hnf_por_hnf_ldid_map_table_reg1 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha2	Specifies CXHA 2 programming is valid	RW	1'h0

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Bits	Field name	Description	Type	Reset
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha2	Specifies the starting LDID for RN-F's behind CXHA 2	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha2	Specifies the node ID for CXHA 2	RW	11'h0

5.3.4.133 por_hnf_ldid_map_table_reg2

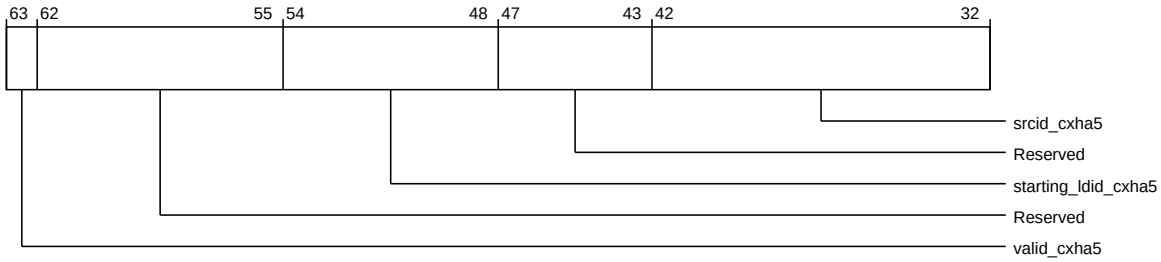
Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-568: por_hnf_por_hnf_ldid_map_table_reg2 (high)



The following table shows the por_hnf_ldid_map_table_reg2 higher register bit assignments.

Table 5-582: por_hnf_por_hnf_ldid_map_table_reg2 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha5	Specifies CXHA 5 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha5	Specifies the starting LDID for RN-F's behind CXHA 5	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha5	Specifies the node ID for CXHA 5	RW	11'h0

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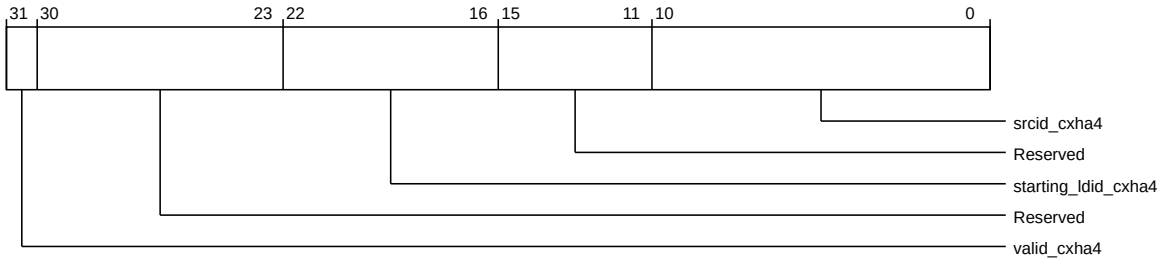
The following figure shows the lower register bit assignments.

Figure 5-569: por_hnf_por_hnf_ldid_map_table_reg2 (low)



The following table shows the por_hnf_ldid_map_table_reg2 lower register bit assignments.

Table 5-583: por_hnf_por_hnf_ldid_map_table_reg2 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha4	Specifies CXHA 4 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha4	Specifies the starting LDID for RN-F's behind CXHA 4	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha4	Specifies the node ID for CXHA 4	RW	11'h0

5.3.4.134 por_hnf_ldid_map_table_reg3

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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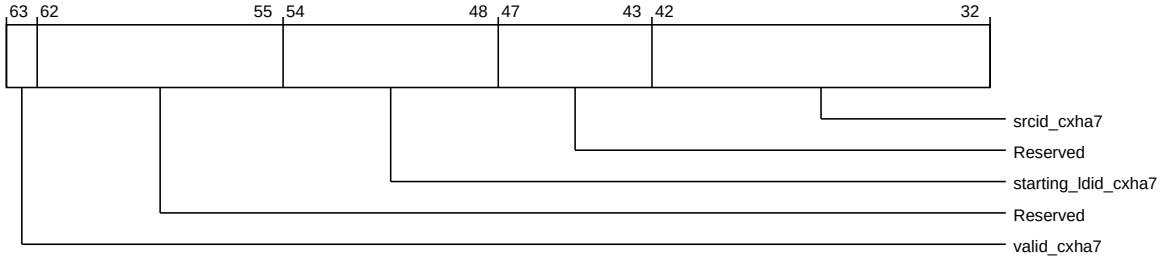
Figure 5-570: por_hnf_por_hnf_ldid_map_table_reg3 (high)



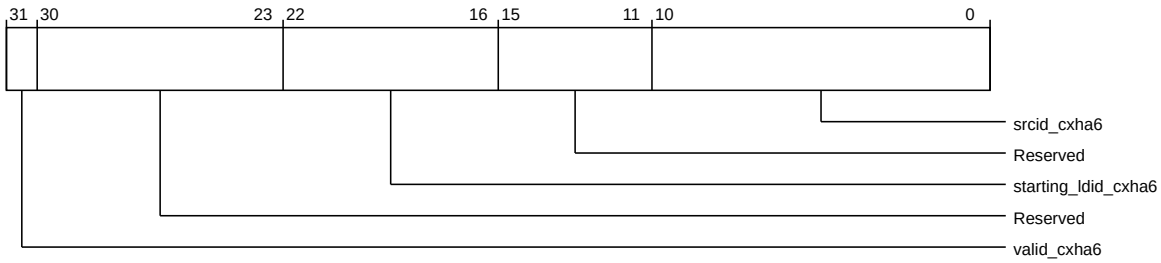
The following table shows the por_hnf_ldid_map_table_reg3 higher register bit assignments.

Table 5-584: por_hnf_por_hnf_ldid_map_table_reg3 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha7	Specifies CXHA 7 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha7	Specifies the starting LDID for RN-F's behind CXHA 7	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha7	Specifies the node ID for CXHA 7	RW	11'h0

The following figure shows the lower register bit assignments.

Figure 5-571: por_hnf_por_hnf_ldid_map_table_reg3 (low)



The following table shows the por_hnf_ldid_map_table_reg3 lower register bit assignments.

Table 5-585: por_hnf_por_hnf_ldid_map_table_reg3 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha6	Specifies CXHA 6 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha6	Specifies the starting LDID for RN-F's behind CXHA 6	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha6	Specifies the node ID for CXHA 6	RW	11'h0

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5.3.4.135 por_hnf_ldid_map_table_reg4

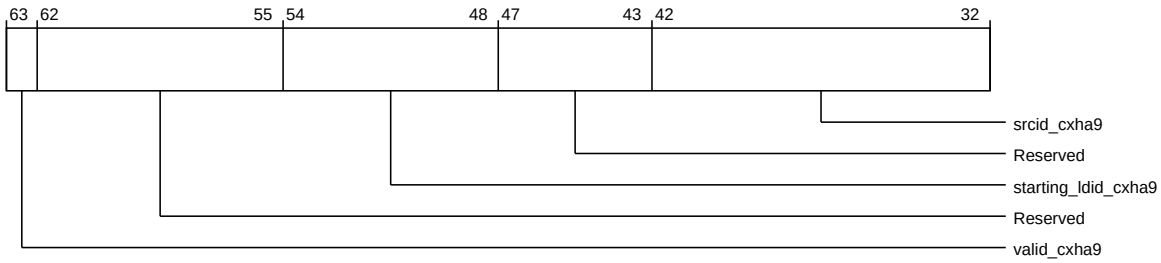
Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-572: por_hnf_por_hnf_ldid_map_table_reg4 (high)



The following table shows the por_hnf_ldid_map_table_reg4 higher register bit assignments.

Table 5-586: por_hnf_por_hnf_ldid_map_table_reg4 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha9	Specifies CXHA 9 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha9	Specifies the starting LDID for RN-F's behind CXHA 9	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha9	Specifies the node ID for CXHA 9	RW	11'h0

The following figure shows the lower register bit assignments.

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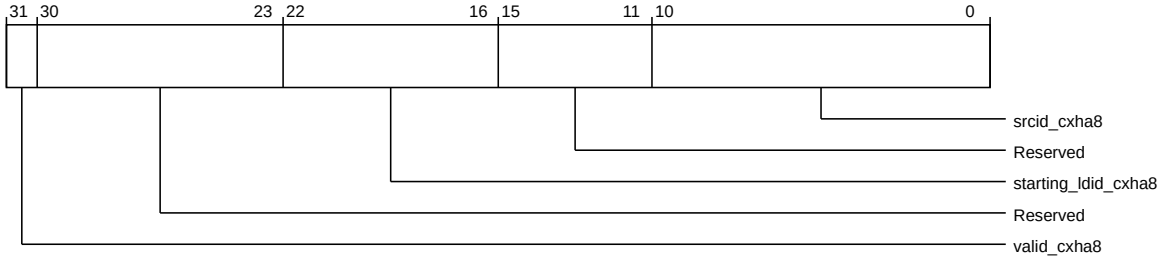
Figure 5-573: por_hnf_por_hnf_ldid_map_table_reg4 (low)



The following table shows the por_hnf_ldid_map_table_reg4 lower register bit assignments.

Table 5-587: por_hnf_por_hnf_ldid_map_table_reg4 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha8	Specifies CXHA 8 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha8	Specifies the starting LDID for RN-F's behind CXHA 8	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha8	Specifies the node ID for CXHA 8	RW	11'h0

5.3.4.136 por_hnf_cml_port_aggr_grp0_add_mask

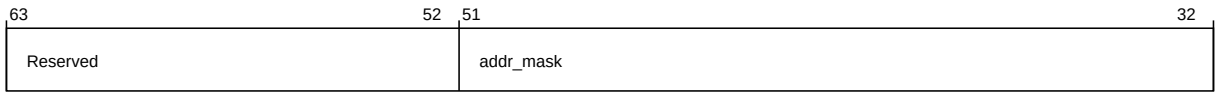
Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF80
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-574: por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)



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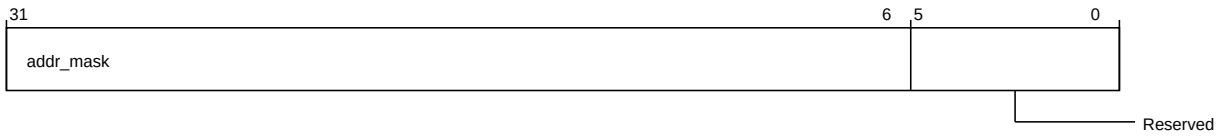
The following table shows the por_hnf_cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 5-588: por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-575: por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)



The following table shows the por_hnf_cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 5-589: por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.4.137 por_hnf_cml_port_aggr_grp1_add_mask

Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF88
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

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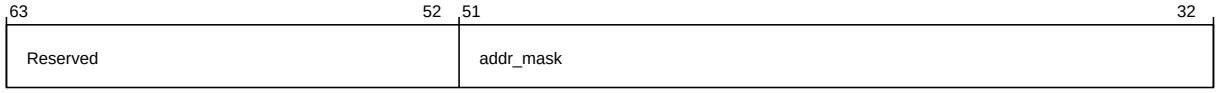
Figure 5-576: por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)



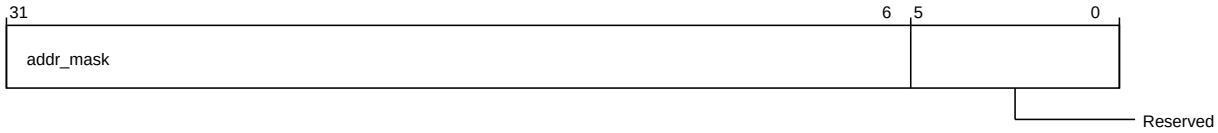
The following table shows the por_hnf_cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 5-590: por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-577: por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)



The following table shows the por_hnf_cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 5-591: por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.4.138 por_hnf_cml_port_aggr_grp2_add_mask

Configures the CCIX port aggregation address mask for group 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF90
Register reset 64'b1111111111111111111111111111111111111111111111111111

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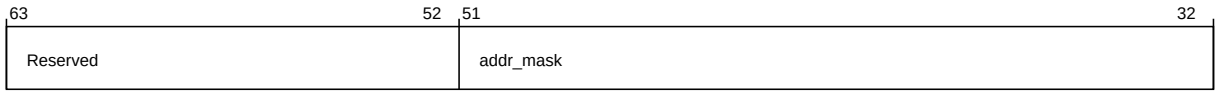
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-578: por_hnf_por_hnf_cml_port_aggr_grp2_add_mask (high)



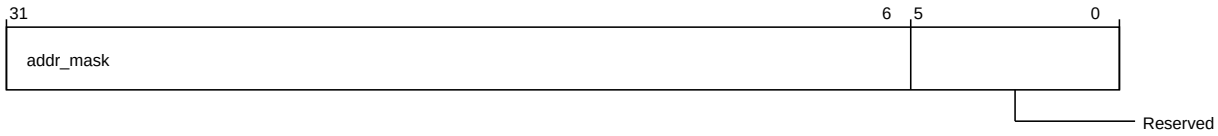
The following table shows the por_hnf_cml_port_aggr_grp2_add_mask higher register bit assignments.

Table 5-592: por_hnf_por_hnf_cml_port_aggr_grp2_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-579: por_hnf_por_hnf_cml_port_aggr_grp2_add_mask (low)



The following table shows the por_hnf_cml_port_aggr_grp2_add_mask lower register bit assignments.

Table 5-593: por_hnf_por_hnf_cml_port_aggr_grp2_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

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5.3.4.139 por_hnf_cml_port_aggr_grp3_add_mask

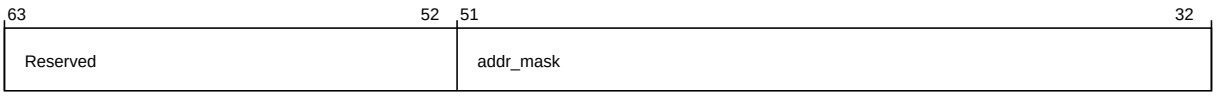
Configures the CCIX port aggregation address mask for group 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF98
Register reset 64'b111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-580: por_hnf_por_hnf_cml_port_aggr_grp3_add_mask (high)



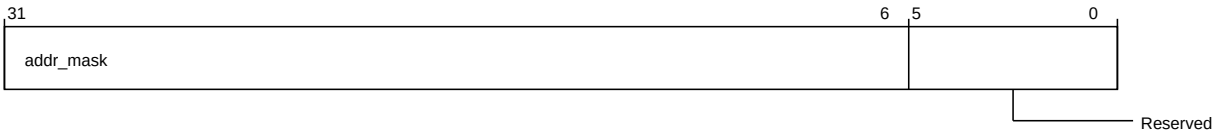
The following table shows the por_hnf_cml_port_aggr_grp3_add_mask higher register bit assignments.

Table 5-594: por_hnf_por_hnf_cml_port_aggr_grp3_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-581: por_hnf_por_hnf_cml_port_aggr_grp3_add_mask (low)



The following table shows the por_hnf_cml_port_aggr_grp3_add_mask lower register bit assignments.

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Table 5-595: por_hnf_por_hnf_cml_port_aggr_grp3_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.4.140 por_hnf_cml_port_aggr_grp4_add_mask

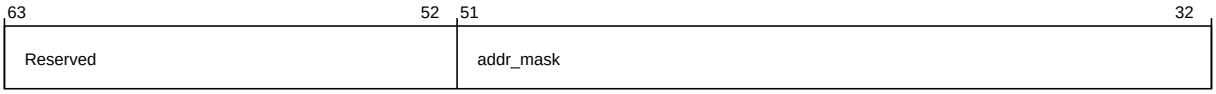
Configures the CCIX port aggregation address mask for group 4.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFA0
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-582: por_hnf_por_hnf_cml_port_aggr_grp4_add_mask (high)



The following table shows the por_hnf_cml_port_aggr_grp4_add_mask higher register bit assignments.

Table 5-596: por_hnf_por_hnf_cml_port_aggr_grp4_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF

The following figure shows the lower register bit assignments.

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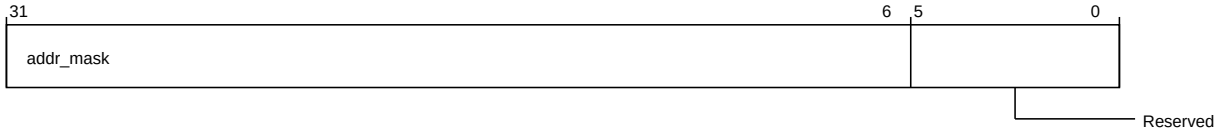
Figure 5-583: por_hnf_por_hnf_cml_port_aggr_grp4_add_mask (low)



The following table shows the por_hnf_cml_port_aggr_grp4_add_mask lower register bit assignments.

Table 5-597: por_hnf_por_hnf_cml_port_aggr_grp4_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.4.141 por_hnf_cml_port_aggr_grp_reg0

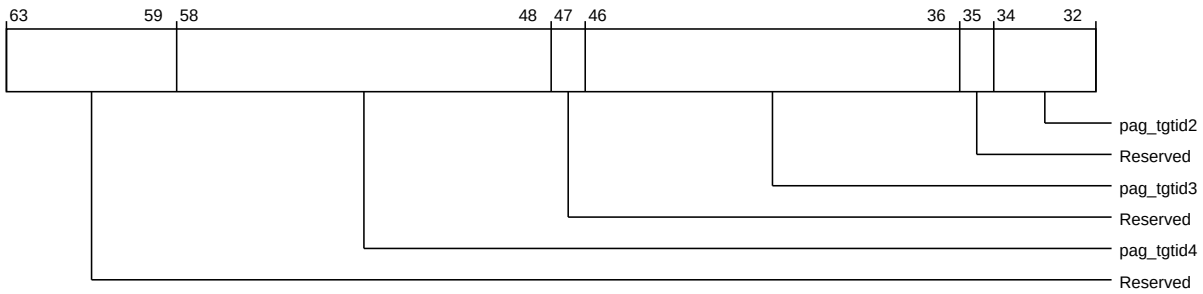
Configures the CCIX port aggregation port Node IDs.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-584: por_hnf_por_hnf_cml_port_aggr_grp_reg0 (high)



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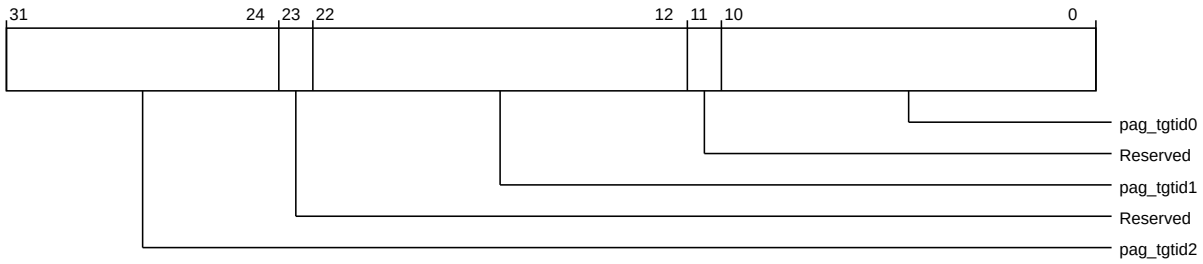
The following table shows the por_hnf_cml_port_aggr_grp_reg0 higher register bit assignments.

Table 5-598: por_hnf_por_hnf_cml_port_aggr_grp_reg0 (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	pag_tgtid4	Specifies the target ID 4 for CPAG	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	pag_tgtid3	Specifies the target ID 3 for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag_tgtid2	Specifies the target ID 2 for CPAG	RW	11'b0

The following figure shows the lower register bit assignments.

Figure 5-585: por_hnf_por_hnf_cml_port_aggr_grp_reg0 (low)



The following table shows the por_hnf_cml_port_aggr_grp_reg0 lower register bit assignments.

Table 5-599: por_hnf_por_hnf_cml_port_aggr_grp_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	pag_tgtid2	Specifies the target ID 2 for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag_tgtid1	Specifies the target ID 1 for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag_tgtid0	Specifies the target ID 0 for CPAG	RW	11'b0

5.3.4.142 por_hnf_cml_port_aggr_grp_reg1

Configures the CCIX port aggregation port Node IDs.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFB8
Register reset 64'b0

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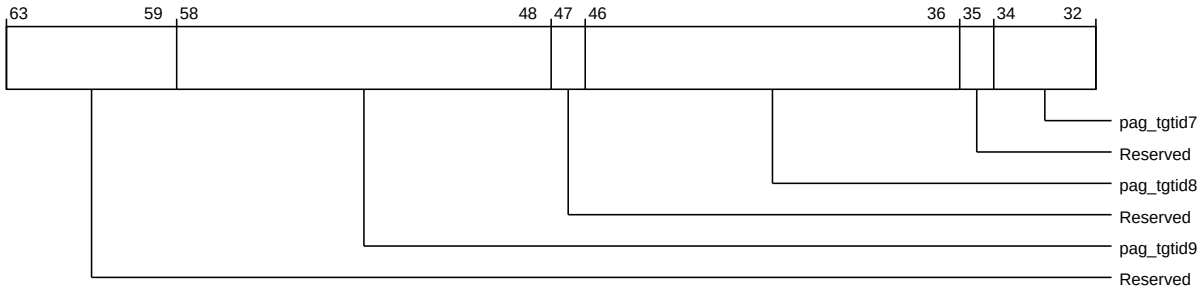
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-586: por_hnf_por_hnf_cml_port_aggr_grp_reg1 (high)



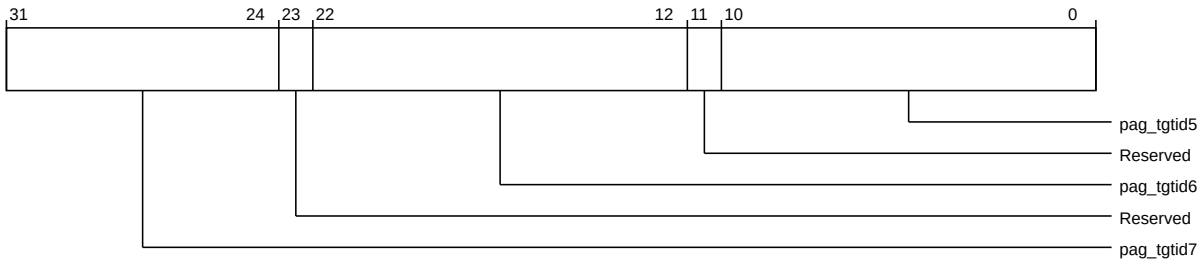
The following table shows the por_hnf_cml_port_aggr_grp_reg1 higher register bit assignments.

Table 5-600: por_hnf_por_hnf_cml_port_aggr_grp_reg1 (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	pag_tgtid9	Specifies the target ID 9 for CPAG	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	pag_tgtid8	Specifies the target ID 8 for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag_tgtid7	Specifies the target ID 7 for CPAG	RW	11'b0

The following figure shows the lower register bit assignments.

Figure 5-587: por_hnf_por_hnf_cml_port_aggr_grp_reg1 (low)



The following table shows the por_hnf_cml_port_aggr_grp_reg1 lower register bit assignments.

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Table 5-601: por_hnf_por_hnf_cml_port_aggr_grp_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	pag_tgtid7	Specifies the target ID 7 for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag_tgtid6	Specifies the target ID 6 for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag_tgtid5	Specifies the target ID 5 for CPAG	RW	11'b0

5.3.4.143 por_hnf_cml_port_aggr_ctrl_reg

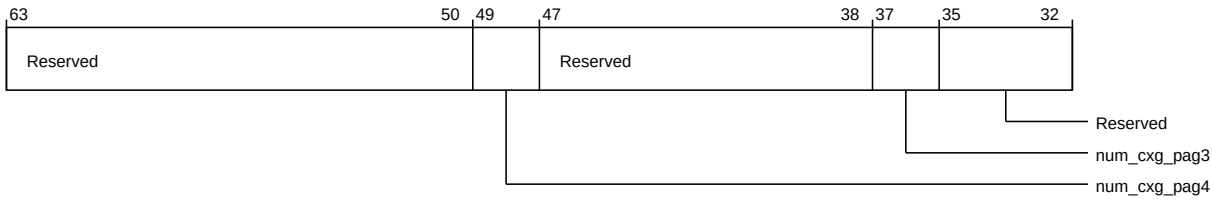
Configures the CCIX port aggregation port groups

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-588: por_hnf_por_hnf_cml_port_aggr_ctrl_reg (high)



The following table shows the por_hnf_cml_port_aggr_ctrl_reg higher register bit assignments.

Table 5-602: por_hnf_por_hnf_cml_port_aggr_ctrl_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-

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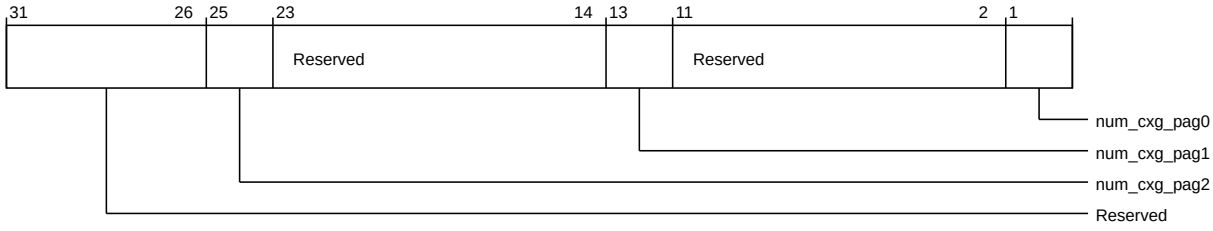
Bits	Field name	Description	Type	Reset
49:48	num_cxg_pag4	Specifies the number of CXRAs in CPAG4 Constraint: May use pag_tgtid8 through pag_tgtid9 of por_hnf_cml_port_aggr_grp_reg1 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
47:38	Reserved	Reserved	RO	-
37:36	num_cxg_pag3	Specifies the number of CXRAs in CPAG3 Constraint: May use pag_tgtid6 through pag_tgtid7 of por_hnf_cml_port_aggr_grp_reg1 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
35:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-589: por_hnf_por_hnf_cml_port_aggr_ctrl_reg (low)



The following table shows the por_hnf_cml_port_aggr_ctrl_reg lower register bit assignments.

Table 5-603: por_hnf_por_hnf_cml_port_aggr_ctrl_reg (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
25:24	num_cxg_pag2	Specifies the number of CXRAs in CPAG2 Constraint: May use pag_tgtid4 through pag_tgtid7 of por_hnf_cml_port_aggr_grp_reg[0,1] 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
23:14	Reserved	Reserved	RO	-
13:12	num_cxg_pag1	Specifies the number of CXRAs in CPAG1 Constraint: May use pag_tgtid2 through pag_tgtid3 of por_hnf_cml_port_aggr_grp_reg0 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
11:2	Reserved	Reserved	RO	-
1:0	num_cxg_pag0	Specifies the number of CXRAs in CPAG0 Constraint: May use pag_tgtid0 through pag_tgtid7 of por_hnf_cml_port_aggr_grp_reg[0,1] 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: 8 ports used	RW	2'b0

5.3.4.144 por_hnf_abf_lo_addr

Lower address range for Address Based Flush (ABF) [51:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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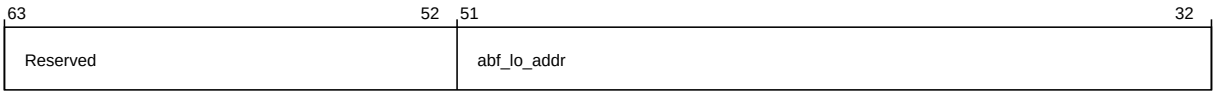
Secure group override por_hnf_secure_register_groups_override.ppu

The following figure shows the higher register bit assignments.

Figure 5-590: por_hnf_por_hnf_abf_lo_addr (high)



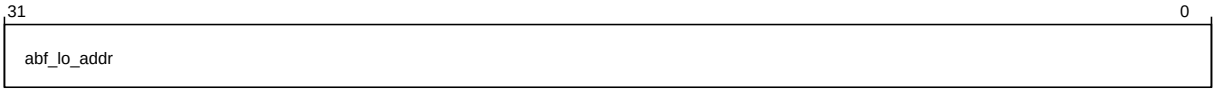
The following table shows the por_hnf_abf_lo_addr higher register bit assignments.

Table 5-604: por_hnf_por_hnf_abf_lo_addr (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	abf_lo_addr	Lower address range for ABF	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-591: por_hnf_por_hnf_abf_lo_addr (low)



The following table shows the por_hnf_abf_lo_addr lower register bit assignments.

Table 5-605: por_hnf_por_hnf_abf_lo_addr (low)

Bits	Field name	Description	Type	Reset
31:0	abf_lo_addr	Lower address range for ABF	RW	52'b0

5.3.4.145 por_hnf_abf_hi_addr

Upper address range for Address Based Flush (ABF) [51:0].

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF58
Register reset 64'b0

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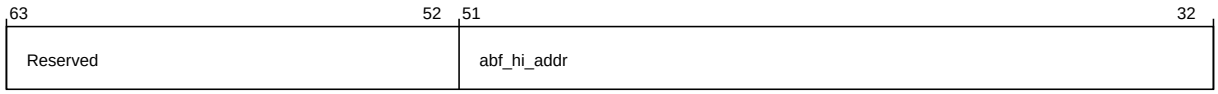
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.ppu

The following figure shows the higher register bit assignments.

Figure 5-592: por_hnf_por_hnf_abf_hi_addr (high)



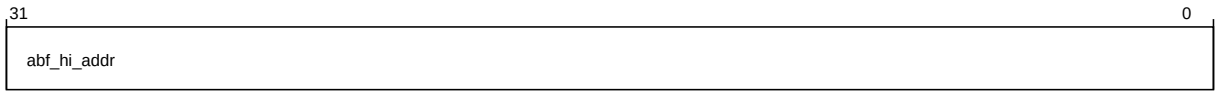
The following table shows the por_hnf_abf_hi_addr higher register bit assignments.

Table 5-606: por_hnf_por_hnf_abf_hi_addr (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	abf_hi_addr	Upper address range for ABF	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-593: por_hnf_por_hnf_abf_hi_addr (low)



The following table shows the por_hnf_abf_hi_addr lower register bit assignments.

Table 5-607: por_hnf_por_hnf_abf_hi_addr (low)

Bits	Field name	Description	Type	Reset
31:0	abf_hi_addr	Upper address range for ABF	RW	52'b0

5.3.4.146 por_hnf_abf_pr

Functions as the Address Based Flush (ABF) policy register.

Its characteristics are:

Type RW
Register width (Bits) 64

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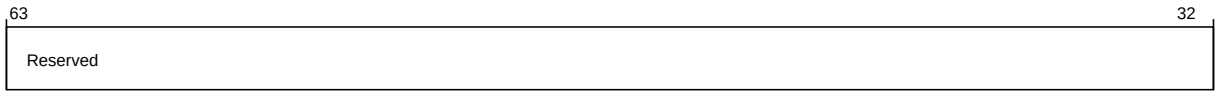
Address offset 16'hF60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hnf_secure_register_groups_override.ppu

The following figure shows the higher register bit assignments.

Figure 5-594: por_hnf_por_hnf_abf_pr (high)



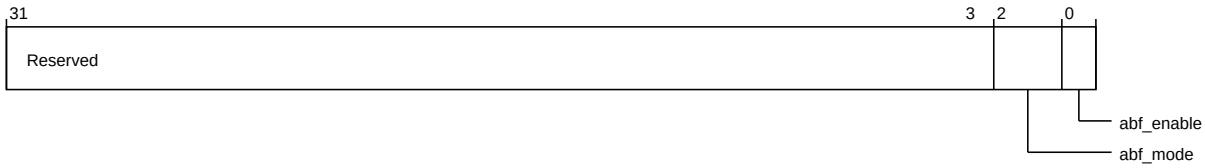
The following table shows the por_hnf_abf_pr higher register bit assignments.

Table 5-608: por_hnf_por_hnf_abf_pr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-595: por_hnf_por_hnf_abf_pr (low)



The following table shows the por_hnf_abf_pr lower register bit assignments.

Table 5-609: por_hnf_por_hnf_abf_pr (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:1	abf_mode	ABF mode 2'b00: Clean Invalidate; WB dirty data and invalidate local copy 2'b01: Make Invalidate; invalidate without writing back dirty data 2'b10: Clean Shared; WB dirty data and can keep clean copy 2'b11: Reserved	RW	2'b00

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Bits	Field name	Description	Type	Reset
0	abf_enable	Start Address Based Flushing based on high and low address ranges	RW	1'b0

5.3.4.147 por_hnf_abf_sr

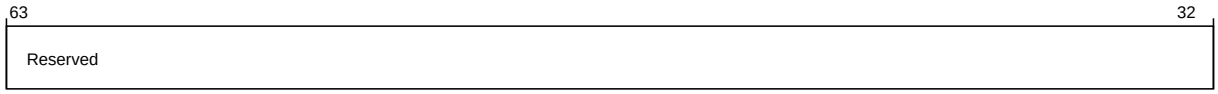
Functions as the Address Based Flush (ABF) status register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hF68
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-596: por_hnf_por_hnf_abf_sr (high)



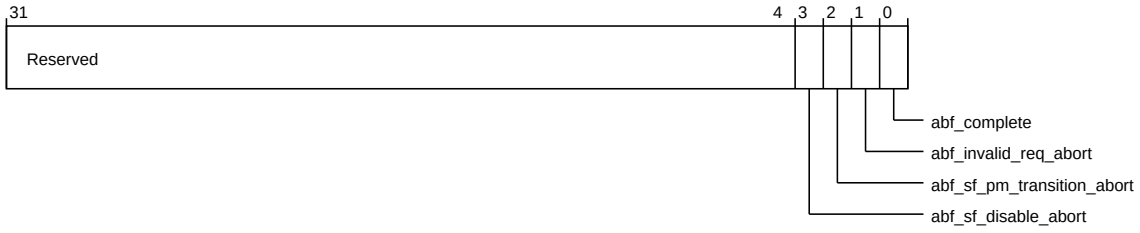
The following table shows the por_hnf_abf_sr higher register bit assignments.

Table 5-610: por_hnf_por_hnf_abf_sr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-597: por_hnf_por_hnf_abf_sr (low)



The following table shows the por_hnf_abf_sr lower register bit assignments.

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Table 5-611: por_hnf_por_hnf_abf_sr (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	abf_sf_disable_abort	ABF aborted due to SF not being enabled, either by configuration or double-bit ECC error	RO	1'b0
2	abf_sf_pm_transition_abort	ABF aborted due to PM transition while ABF in progress, or both PM and ABF requested at the same time	RO	1'b0
1	abf_invalid_req_abort	ABF request made while PM is not in FAM/HAM/SF_ONLY mode; request aborted in this case	RO	1'b0
0	abf_complete	ABF completed	RO	1'b0

5.3.4.148 por_hnf_cbusy_write_limit_ctl

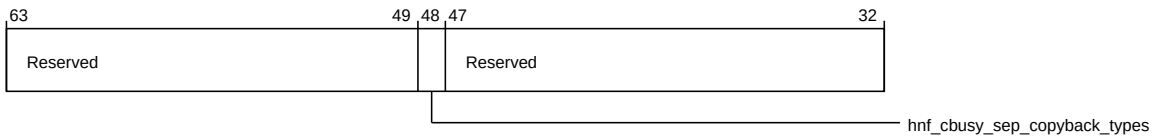
Cbusy threshold limits for POCQ write entries. CONSTRAINT: The hnf_adv_cbusy_mode_dis must be 1'b0 to use this feature.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1000
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-598: por_hnf_por_hnf_cbusy_write_limit_ctl (high)



The following table shows the por_hnf_cbusy_write_limit_ctl higher register bit assignments.

Table 5-612: por_hnf_por_hnf_cbusy_write_limit_ctl (high)

Bits	Field name	Description	Type	Reset
63:49	Reserved	Reserved	RO	-
48	hnf_cbusy_sep_copyback_types	Enables copyback and non-copyback write type separation in cbusy calculation	RW	1'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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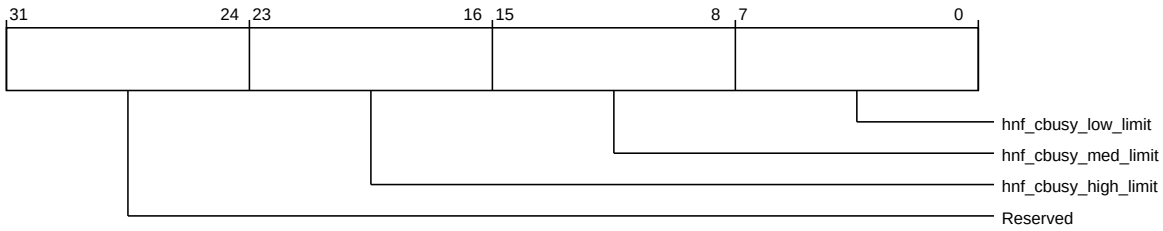
Figure 5-599: por_hnf_por_hnf_cbusy_write_limit_ctl (low)



The following table shows the por_hnf_cbusy_write_limit_ctl lower register bit assignments.

Table 5-613: por_hnf_por_hnf_cbusy_write_limit_ctl (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_cbusy_high_limit	POCQ limit for Write CBusy High	RW	Configuration dependent
15:8	hnf_cbusy_med_limit	POCQ limit for Write CBusy Med	RW	Configuration dependent
7:0	hnf_cbusy_low_limit	POCQ limit for Write CBusy Low	RW	Configuration dependent

5.3.4.149 por_hnf_cbusy_resp_ctl

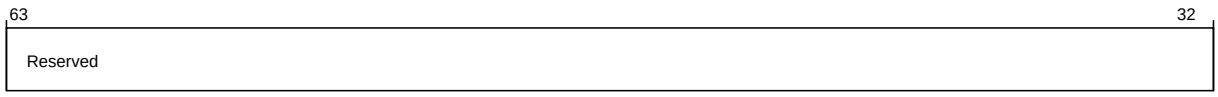
Contols the responses sent from HNF to RNF. CONSTRAINT: The hnf_adv_cbusy_mode_dis must be 1'b0 to use this feature.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1008
Register reset 64'b000100000
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-600: por_hnf_por_hnf_cbusy_resp_ctl (high)



The following table shows the por_hnf_cbusy_resp_ctl higher register bit assignments.

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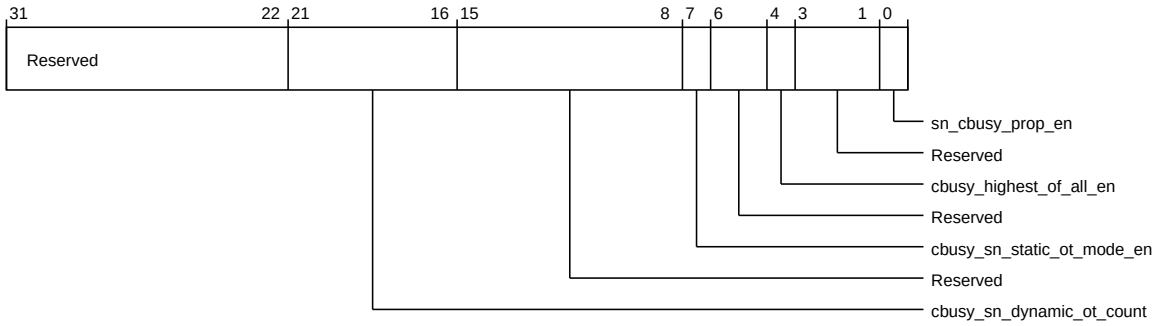
Table 5-614: por_hnf_por_hnf_cbusy_resp_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-601: por_hnf_por_hnf_cbusy_resp_ctl (low)



The following table shows the por_hnf_cbusy_resp_ctl lower register bit assignments.

Table 5-615: por_hnf_por_hnf_cbusy_resp_ctl (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	cbusy_sn_dynamic_ot_count	Specifies the granularity at which HN-F will dynamically throttle transactions to SN-F. CONSTRAINT: 2,4,8 are the the allowed values	RW	6'b000100
15:8	Reserved	Reserved	RO	-
7	cbusy_sn_static_ot_mode_en	Controls cbusy between HN-F and SN-F 1'b0: HN-F will dynamically throttle outstanding requests to SN-F 1'b1: HN-F will use fixed transactions count at each CBusy level at 1/4th POCQ granularity	RW	1'b0
6:5	Reserved	Reserved	RO	-
4	cbusy_highest_of_all_en	Controls cbusy between HN-F and SN-F 1'b0: Will send the HN-F or SN-F as configured 1'b1: Will select highest CBusy value between the SN-F and HN-F	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	sn_cbusy_prop_en	Controls HN-F and SN-F cbusy on responses to RN-F 1'b0: HN-F's POCQ Cbusy is sent 1'b1: SN-F's Cbusy is sent	RW	1'b0

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5.3.4.150 por_hnf_cbusy_sn_ctl

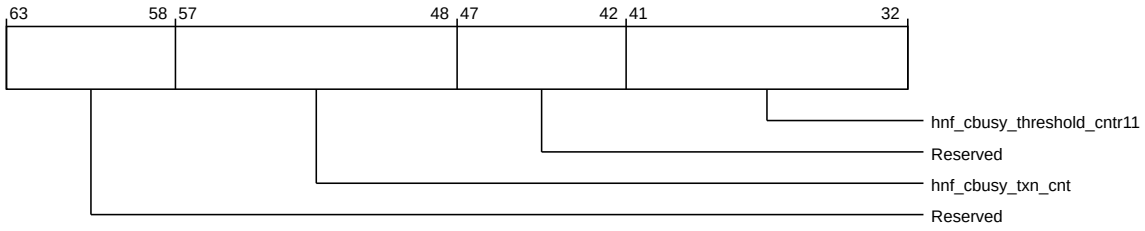
Controls the SN-F cbusy thresholds. CONSTRAINT: The hnf_adv_cbusy_mode_dis must be 1'b0 to use this feature.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1010
Register reset 64'b0100000000000001000000001000000001000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following figure shows the higher register bit assignments.

Figure 5-602: por_hnf_por_hnf_cbusy_sn_ctl (high)



The following table shows the por_hnf_cbusy_sn_ctl higher register bit assignments.

Table 5-616: por_hnf_por_hnf_cbusy_sn_ctl (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:48	hnf_cbusy_txn_cnt	Number of transactions over which the counters are tracked	RW	10'b0100000000
47:42	Reserved	Reserved	RO	-
41:32	hnf_cbusy_threshold_cntr11	CBusy threshold at which SN-F is considered busy for Counter_11	RW	10'b0000010000

The following figure shows the lower register bit assignments.

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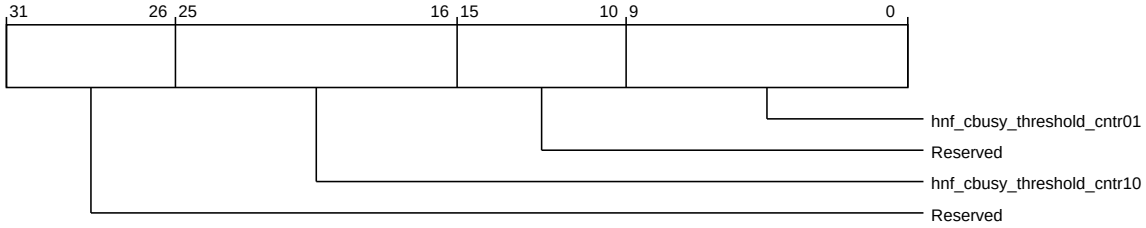
Figure 5-603: por_hnf_por_hnf_cbusy_sn_ctl (low)



The following table shows the por_hnf_cbusy_sn_ctl lower register bit assignments.

Table 5-617: por_hnf_por_hnf_cbusy_sn_ctl (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:16	hnf_cbusy_threshold_cntr10	CBusy threshold at which SN-F is considered busy for Counter_10	RW	10'b0000100000
15:10	Reserved	Reserved	RO	-
9:0	hnf_cbusy_threshold_cntr01	CBusy threshold at which SN-F is considered busy for Counter_01	RW	10'b0001000000

5.3.4.151 por_hnf_partner_scratch_reg0

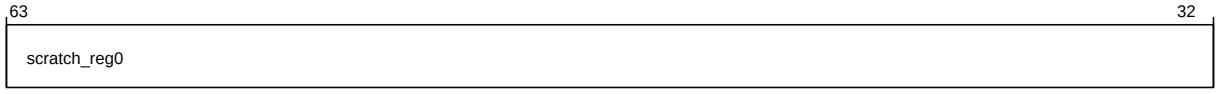
Partner scratch register 0

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFE0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.partner_scratch_override

The following figure shows the higher register bit assignments.

Figure 5-604: por_hnf_por_hnf_partner_scratch_reg0 (high)



The following table shows the por_hnf_partner_scratch_reg0 higher register bit assignments.

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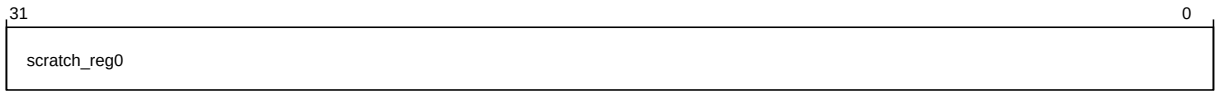
Table 5-618: por_hnf_por_hnf_partner_scratch_reg0 (high)

Bits	Field name	Description	Type	Reset
63:32	scratch_reg0	64 bit scratch register 0 wirh read/write access	RW	64'h00000000

The following figure shows the lower register bit assignments.

Figure 5-605: por_hnf_por_hnf_partner_scratch_reg0 (low)



The following table shows the por_hnf_partner_scratch_reg0 lower register bit assignments.

Table 5-619: por_hnf_por_hnf_partner_scratch_reg0 (low)

Bits	Field name	Description	Type	Reset
31:0	scratch_reg0	64 bit scratch register 0 wirh read/write access	RW	64'h00000000

5.3.4.152 por_hnf_partner_scratch_reg1

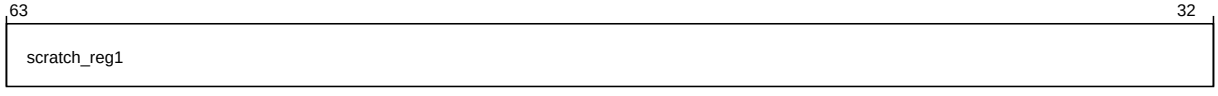
Partner scratch register 1

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hFE8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.partner_scratch_override

The following figure shows the higher register bit assignments.

Figure 5-606: por_hnf_por_hnf_partner_scratch_reg1 (high)



The following table shows the por_hnf_partner_scratch_reg1 higher register bit assignments.

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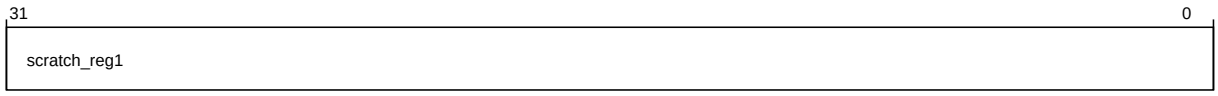
Table 5-620: por_hnf_por_hnf_partner_scratch_reg1 (high)

Bits	Field name	Description	Type	Reset
63:32	scratch_reg1	64 bit scratch register 1 wirh read/write access	RW	64'h00000000

The following figure shows the lower register bit assignments.

Figure 5-607: por_hnf_por_hnf_partner_scratch_reg1 (low)



The following table shows the por_hnf_partner_scratch_reg1 lower register bit assignments.

Table 5-621: por_hnf_por_hnf_partner_scratch_reg1 (low)

Bits	Field name	Description	Type	Reset
31:0	scratch_reg1	64 bit scratch register 1 wirh read/write access	RW	64'h00000000

5.3.4.153 por_hnf_cfg_slcsf_dbgrd

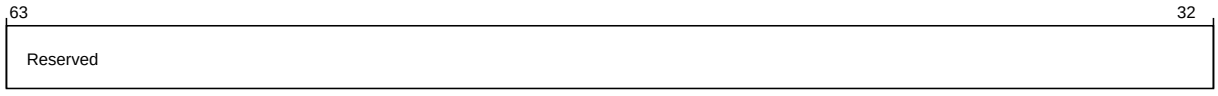
Controls access modes for SLC tasg, SLC data, and SF tag debug read.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'hB80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-608: por_hnf_por_hnf_cfg_slcsf_dbgrd (high)



The following table shows the por_hnf_cfg_slcsf_dbgrd higher register bit assignments.

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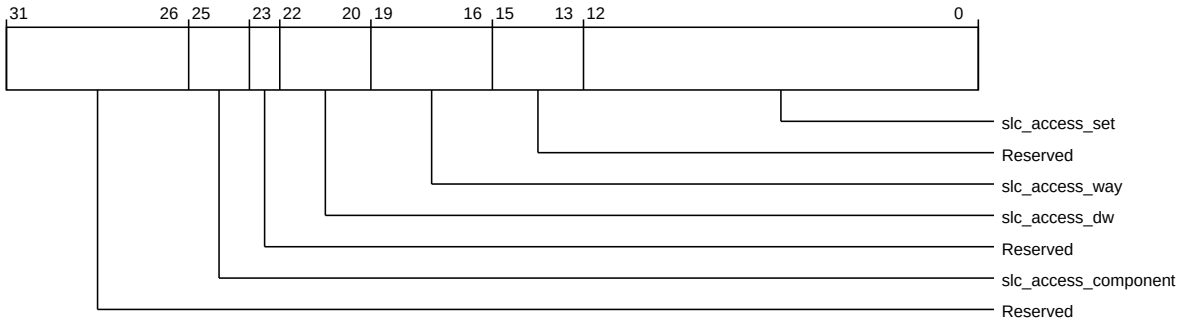
Table 5-622: por_hnf_por_hnf_cfg_slcsf_dbgrd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-609: por_hnf_por_hnf_cfg_slcsf_dbgrd (low)



The following table shows the por_hnf_cfg_slcsf_dbgrd lower register bit assignments.

Table 5-623: por_hnf_por_hnf_cfg_slcsf_dbgrd (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	slc_access_component	Specifies SLC/SF array debug read 2'b01: SLC data read 2'b10: SLC tag read 2'b11: SF tag read	WO	2'b00
23	Reserved	Reserved	RO	-
22:20	slc_access_dw	64-bit chunk address for SLC data debug read access	WO	3'h0
19:16	slc_access_way	Way address for SLC/SF debug read access	WO	4'h0
15:13	Reserved	Reserved	RO	-
12:0	slc_access_set	Set address for SLC/SF debug read access	WO	13'h0

5.3.4.154 por_hnf_slc_cache_access_slc_tag

Contains SLC tag debug read data bits [63:0]

Its characteristics are:

Type RO
Register width (Bits) 64

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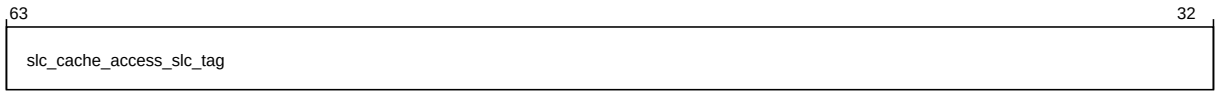
Address offset 16'hB88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-610: por_hnf_por_hnf_slc_cache_access_slc_tag (high)



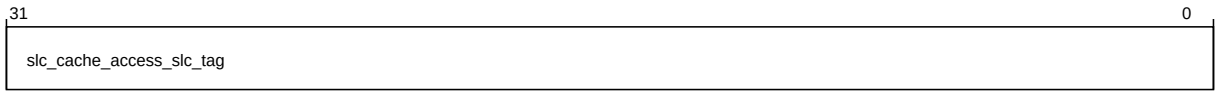
The following table shows the por_hnf_slc_cache_access_slc_tag higher register bit assignments.

Table 5-624: por_hnf_por_hnf_slc_cache_access_slc_tag (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_slc_tag	SLC tag debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-611: por_hnf_por_hnf_slc_cache_access_slc_tag (low)



The following table shows the por_hnf_slc_cache_access_slc_tag lower register bit assignments.

Table 5-625: por_hnf_por_hnf_slc_cache_access_slc_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_tag	SLC tag debug read data	RO	64'h0

5.3.4.155 por_hnf_slc_cache_access_slc_tag1

Contains SLC tag debug read data bits [127:64] when present

Its characteristics are:

Type RO
Register width (Bits) 64

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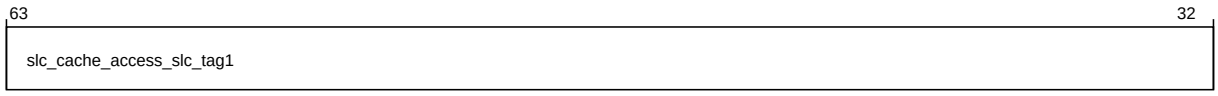
Address offset 16'hB90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-612: por_hnf_por_hnf_slc_cache_access_slc_tag1 (high)



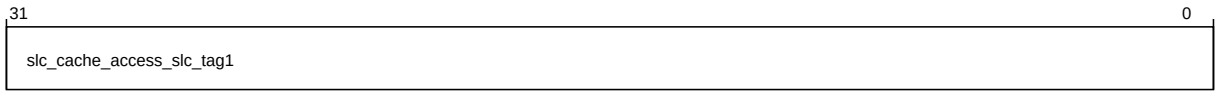
The following table shows the por_hnf_slc_cache_access_slc_tag1 higher register bit assignments.

Table 5-626: por_hnf_por_hnf_slc_cache_access_slc_tag1 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_slc_tag1	SLC tag debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-613: por_hnf_por_hnf_slc_cache_access_slc_tag1 (low)



The following table shows the por_hnf_slc_cache_access_slc_tag1 lower register bit assignments.

Table 5-627: por_hnf_por_hnf_slc_cache_access_slc_tag1 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_tag1	SLC tag debug read data	RO	64'h0

5.3.4.156 por_hnf_slc_cache_access_slc_data

Contains SLC data RAM debug read data.

Its characteristics are:

Type RO
Register width (Bits) 64

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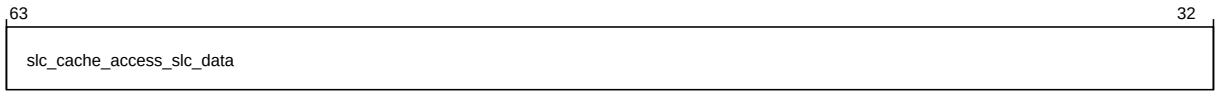
Address offset 16'hB98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-614: por_hnf_por_hnf_slc_cache_access_slc_data (high)



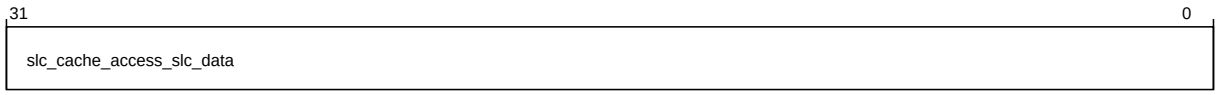
The following table shows the por_hnf_slc_cache_access_slc_data higher register bit assignments.

Table 5-628: por_hnf_por_hnf_slc_cache_access_slc_data (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-615: por_hnf_por_hnf_slc_cache_access_slc_data (low)



The following table shows the por_hnf_slc_cache_access_slc_data lower register bit assignments.

Table 5-629: por_hnf_por_hnf_slc_cache_access_slc_data (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

5.3.4.157 por_hnf_slc_cache_access_slc_mte_tag

Contains MTE Tag data for the corresponding SLC data RAM debug read.

Its characteristics are:

Type RO
Register width (Bits) 64

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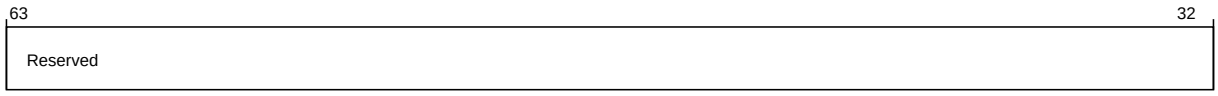
Address offset 16'hBC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-616: por_hnf_por_hnf_slc_cache_access_slc_mte_tag (high)



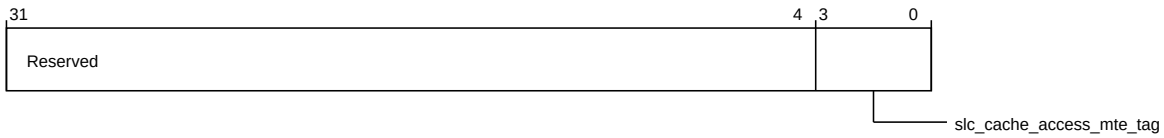
The following table shows the por_hnf_slc_cache_access_slc_mte_tag higher register bit assignments.

Table 5-630: por_hnf_por_hnf_slc_cache_access_slc_mte_tag (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-617: por_hnf_por_hnf_slc_cache_access_slc_mte_tag (low)



The following table shows the por_hnf_slc_cache_access_slc_mte_tag lower register bit assignments.

Table 5-631: por_hnf_por_hnf_slc_cache_access_slc_mte_tag (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	slc_cache_access_mte_tag	SLC MTE TAG corresponding to data RAM debug read data (128bit chunk of data)	RO	4'h0

5.3.4.158 por_hnf_slc_cache_access_sf_tag

Contains SF tag debug read data. Bits[63:0]

Its characteristics are:

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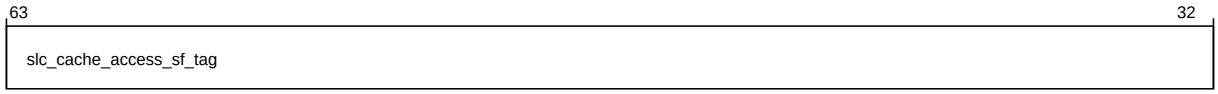
Type RO
Register width (Bits) 64
Address offset 16'hBA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-618: por_hnf_por_hnf_slc_cache_access_sf_tag (high)



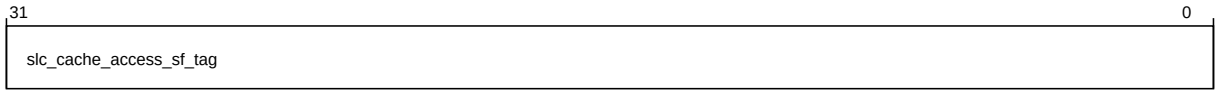
The following table shows the por_hnf_slc_cache_access_sf_tag higher register bit assignments.

Table 5-632: por_hnf_por_hnf_slc_cache_access_sf_tag (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-619: por_hnf_por_hnf_slc_cache_access_sf_tag (low)



The following table shows the por_hnf_slc_cache_access_sf_tag lower register bit assignments.

Table 5-633: por_hnf_por_hnf_slc_cache_access_sf_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

5.3.4.159 por_hnf_slc_cache_access_sf_tag1

Contains SF tag debug read data bits [127:64], when present in SF Tag

Its characteristics are:

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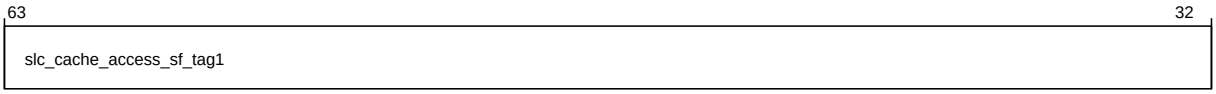
Type RO
Register width (Bits) 64
Address offset 16'hBA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-620: por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)



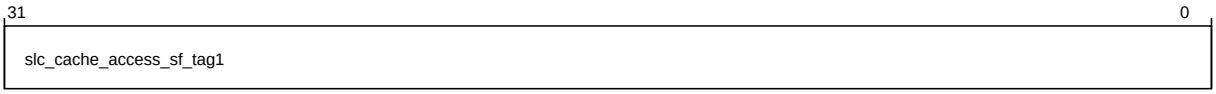
The following table shows the por_hnf_slc_cache_access_sf_tag1 higher register bit assignments.

Table 5-634: por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-621: por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)



The following table shows the por_hnf_slc_cache_access_sf_tag1 lower register bit assignments.

Table 5-635: por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

5.3.4.160 por_hnf_slc_cache_access_sf_tag2

Contains SF tag debug read data bits [128:191], when present in SF Tag

Its characteristics are:

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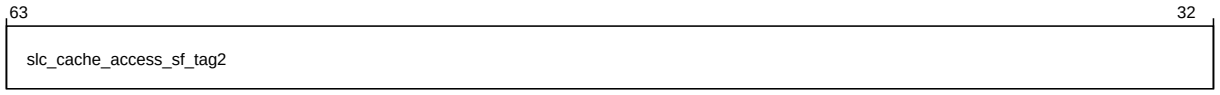
Type RO
Register width (Bits) 64
Address offset 16'hBB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-622: por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)



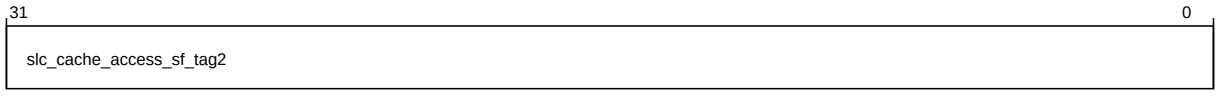
The following table shows the por_hnf_slc_cache_access_sf_tag2 higher register bit assignments.

Table 5-636: por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

The following figure shows the lower register bit assignments.

Figure 5-623: por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)



The following table shows the por_hnf_slc_cache_access_sf_tag2 lower register bit assignments.

Table 5-637: por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

5.3.4.161 por_hnf_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

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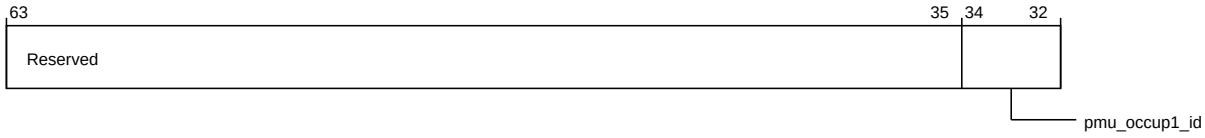
Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-624: por_hnf_por_hnf_pmu_event_sel (high)



The following table shows the por_hnf_pmu_event_sel higher register bit assignments.

Table 5-638: por_hnf_por_hnf_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	pmu_occup1_id	HN-F PMU occupancy 1 select 3'b000: All occupancy selected 3'b001: Read requests 3'b010: Write requests 3'b011: Atomic operation requests 3'b100: Stash requests	RW	3'h0

The following figure shows the lower register bit assignments.

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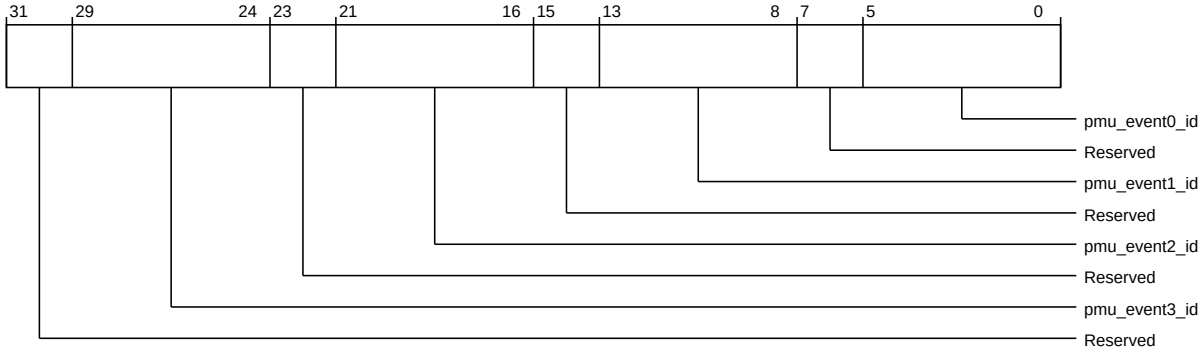
Figure 5-625: por_hnf_por_hnf_pmu_event_sel (low)



The following table shows the por_hnf_pmu_event_sel lower register bit assignments.

Table 5-639: por_hnf_por_hnf_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	HN-F PMU Event 3 select; see pmu_event0_id for encodings	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	HN-F PMU Event 2 select; see pmu_event0_id for encodings	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	HN-F PMU Event 1 select; see pmu_event0_id for encodings	RW	6'h00
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	HN-F PMU Event 0 select 6'h00: No event 6'h01: PMU_HN_CACHE_MISS_EVENT; counts total cache misses in first lookup result (high priority) 6'h02: PMU_HN_SLCSF_CACHE_ACCESS_EVENT; counts number of cache accesses in first access (high priority) 6'h03: PMU_HN_CACHE_FILL_EVENT; counts total allocations in HN SLC (all cache line allocations to SLC) 6'h04: PMU_HN_POCQ_RETRY_EVENT; counts number of retried requests 6'h05: PMU_HN_POCQ_REQS_RECVD_EVENT; counts number of requests received by HN 6'h06: PMU_HN_SF_HIT_EVENT; counts number of SF hits 6'h07: PMU_HN_SF_EVICTIONS_EVENT; counts number of SF eviction cache invalidations initiated 6'h08: PMU_HN_DIR_SNOOPS_SENT_EVENT; counts number of directed snoops sent (not including SF back invalidation) 6'h09: PMU_HN_BRD_SNOOPS_SENTEVENT; counts number of multicast snoops send (not including SF back invalidation) 6'h0A: PMU_HN_SLC_EVICTION_EVENT; counts number of SLC evictions (dirty only) 6'h0B: PMU_HN_SLC_FILL_INVALID_WAY_EVENT; counts number of SLC fills to an invalid way 6'h0C: PMU_HN_MC_RETRIES_EVENT; counts number of retried transactions by the MC 6'h0D: PMU_HN_MC_REQS_EVENT; counts number of requests sent to MC 6'h0E: PMU_HN_QOS_HH_RETRY_EVENT; counts number of times a HighHigh priority request is protocol retried at the HN-F 6'h0F: PMU_HN_POCQ_OCCUPANCY_EVENT; counts the POCQ occupancy in HN-F; occupancy filtering is programmed in pmu_occup1_id 6'h10: PMU_HN_POCQ_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation 6'h11: PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation for atomic operations 6'h12: PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT; counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations 6'h13: PMU_HN_CMP_ADQ_FULL_EVENT; counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations	RW	6'h00

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	6'h14: PMU_HN_TXDAT_STALL_EVENT; counts number of times HN-F has a pending TXDAT flit but no credits to upload 6'h15: PMU_HN_TXRSP_STALL_EVENT; counts number of times HN-F has a pending TXRSP flit but no credits to upload 6'h16: PMU_HN_SEQ_FULL_EVENT; counts number of times requests are replayed in SLC pipe due to SEQ being full 6'h17: PMU_HN_SEQ_HIT_EVENT; counts number of times a request in SLC hit a pending SF eviction in SEQ 6'h18: PMU_HN_SNP_SENT_EVENT; counts number of snoops sent including directed/multicast/ SF back invalidation 6'h19: PMU_HN_SFBI_DIR_SNP_SENT_EVENT; counts number of times directed snoops were sent due to SF back invalidation 6'h1a: PMU_HN_SFBI_BRD_SNP_SENT_EVENT; counts number of times multicast snoops were sent due to SF back invalidation 6'h1b: PMU_HN_SNP_SENT_UNTRK_EVENT; counts number of times snooped were sent due to untracked RN-Fs 6'h1c: PMU_HN_INTV_DIRTY_EVENT; counts number of times SF back invalidation resulted in dirty line intervention from the RN 6'h1d: PMU_HN_STASH_SNP_SENT_EVENT; counts number of times stash snoops sent 6'h1e: PMU_HN_STASH_DATA_PULL_EVENT; counts number of times stash snoops resulted in data pull from the RN 6'h1f: PMU_HN_SNP_FWDED_EVENT; counts number of times data forward snoops sent 6'h20: PMU_HN_ATOMIC_FWD_EVENT; counts number of times atomic data was forwarded between POC entries 6'h21: PMU_HN_MPAM_REQ_OVER_HARDLIM_EVENT; counts number of times write req can't allocate in SLC due to being over hardlimit 6'h22: PMU_HN_MPAM_REQ_OVER_SOFTLIM_EVENT; counts number of times write req is above soft limit	RW	6'h00

5.3.4.162 por_hnf_pmu_mpam_sel

Specifies details of MPAM event to be counted

Its characteristics are:

Type RW
Register width (Bits) 64

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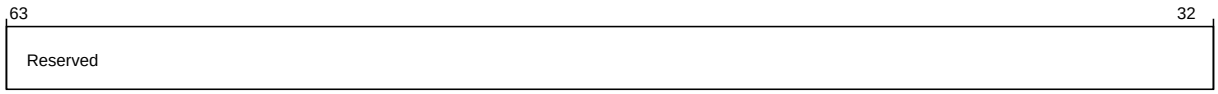
Address offset 16'h2008
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-626: por_hnf_por_hnf_pmu_mpam_sel (high)



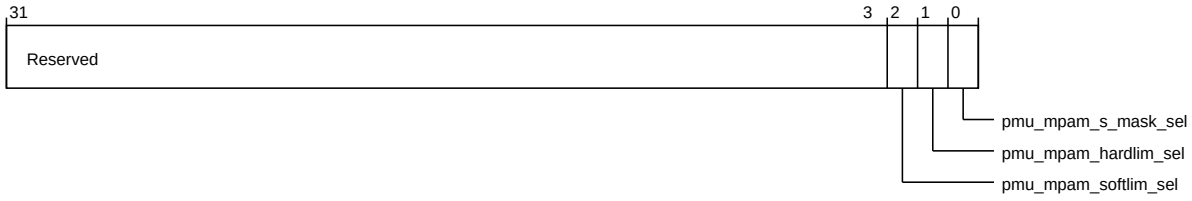
The following table shows the por_hnf_pmu_mpam_sel higher register bit assignments.

Table 5-640: por_hnf_por_hnf_pmu_mpam_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-627: por_hnf_por_hnf_pmu_mpam_sel (low)



The following table shows the por_hnf_pmu_mpam_sel lower register bit assignments.

Table 5-641: por_hnf_por_hnf_pmu_mpam_sel (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	pmu_mpam_softlim_sel	When set, HN-F PMU MPAM Softlimit count is filtered for specific PARTIDs 1'b0: PMU Softlimit count is total for all PARDIDs. 1'b1: PMU Softlimit count is only for PARDIDs indicated in fliter register	RW	1'b0
1	pmu_mpam_hardlim_sel	When set, HN-F PMU MPAM Hardlimit count is filtered for specific PARTIDs 1'b0: PMU Hardlimit count is total for all PARDIDs. 1'b1: PMU Hardlimit count is only for PARDIDs indicated in fliter register	RW	1'b0

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Bits	Field name	Description	Type	Reset
0	pmu_mpam_s_mask_sel	When set, PARTID Mask is used for Secure MPAM PARTID 1'b0: PMU MPAM mask is for Non-Secure MPAMID. 1'b1: PMU MPAM mask is for Secure MPAMID.	RW	1'b0

5.3.4.163 por_hnf_pmu_mpam_pardid_mask0

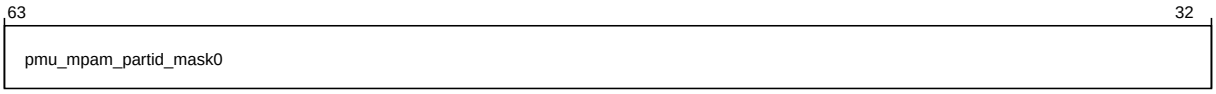
Functions as mask for PARTID[63:0] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2010
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-628: por_hnf_por_hnf_pmu_mpam_pardid_mask0 (high)



The following table shows the por_hnf_pmu_mpam_pardid_mask0 higher register bit assignments.

Table 5-642: por_hnf_por_hnf_pmu_mpam_pardid_mask0 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask0	MPAM PMU hardlimit and softlimit mask for PARTID [63:0] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

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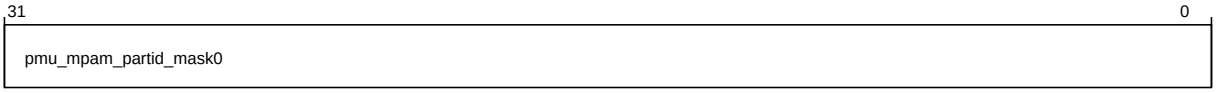
Figure 5-629: por_hnf_por_hnf_pmu_mpam_pardid_mask0 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask0 lower register bit assignments.

Table 5-643: por_hnf_por_hnf_pmu_mpam_pardid_mask0 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask0	MPAM PMU hardlimit and softlimit mask for PARTID [63:0] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.164 por_hnf_pmu_mpam_pardid_mask1

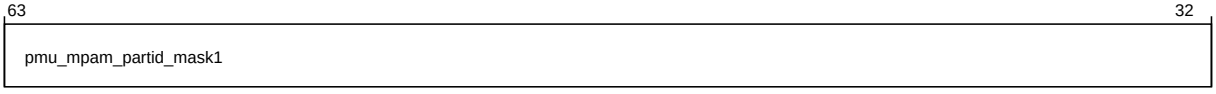
Functions as mask for PARTID[127:64] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2018
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-630: por_hnf_por_hnf_pmu_mpam_pardid_mask1 (high)



The following table shows the por_hnf_pmu_mpam_pardid_mask1 higher register bit assignments.

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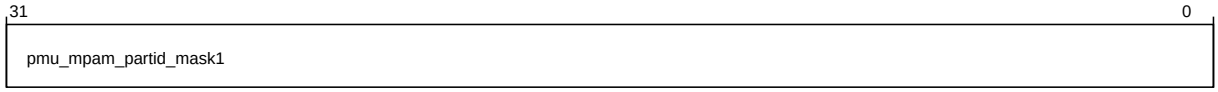
Table 5-644: por_hnf_por_hnf_pmu_mpam_pardid_mask1 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask1	MPAM PMU hardlimit and softlimit mask for PARTID [127:64] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-631: por_hnf_por_hnf_pmu_mpam_pardid_mask1 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask1 lower register bit assignments.

Table 5-645: por_hnf_por_hnf_pmu_mpam_pardid_mask1 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask1	MPAM PMU hardlimit and softlimit mask for PARTID [127:64] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.165 por_hnf_pmu_mpam_pardid_mask2

Functions as mask for PARTID[191:128] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2020
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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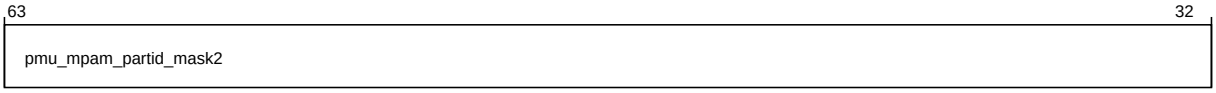
Figure 5-632: por_hnf_por_hnf_pmu_mpam_pardid_mask2 (high)



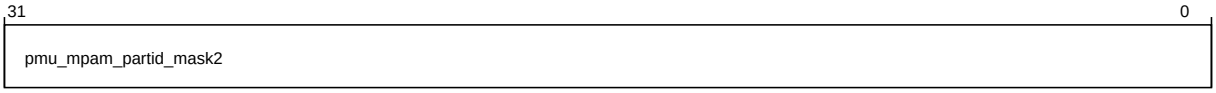
The following table shows the por_hnf_pmu_mpam_pardid_mask2 higher register bit assignments.

Table 5-646: por_hnf_por_hnf_pmu_mpam_pardid_mask2 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask2	MPAM PMU hardlimit and softlimit mask for PARTID [191:128] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-633: por_hnf_por_hnf_pmu_mpam_pardid_mask2 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask2 lower register bit assignments.

Table 5-647: por_hnf_por_hnf_pmu_mpam_pardid_mask2 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask2	MPAM PMU hardlimit and softlimit mask for PARTID [191:128] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.166 por_hnf_pmu_mpam_pardid_mask3

Functions as mask for PARTID[255:192] filter for MPM PMU events

Its characteristics are:

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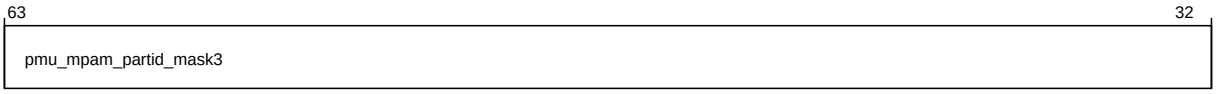
Type RW
Register width (Bits) 64
Address offset 16'h2028
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-634: por_hnf_por_hnf_pmu_mpam_pardid_mask3 (high)



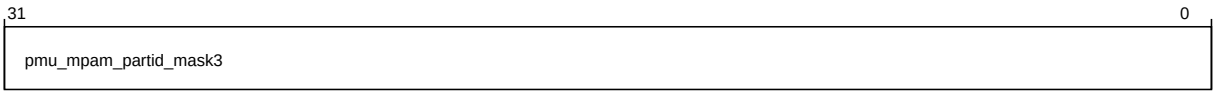
The following table shows the por_hnf_pmu_mpam_pardid_mask3 higher register bit assignments.

Table 5-648: por_hnf_por_hnf_pmu_mpam_pardid_mask3 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask3	MPAM PMU hardlimit and softlimit mask for PARTID [255:192] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-635: por_hnf_por_hnf_pmu_mpam_pardid_mask3 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask3 lower register bit assignments.

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Table 5-649: por_hnf_por_hnf_pmu_mpam_pardid_mask3 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask3	MPAM PMU hardlimit and softlimit mask for PARTID [255:192] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.167 por_hnf_pmu_mpam_pardid_mask4

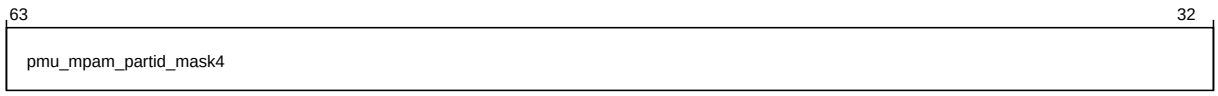
Functions as mask for PARTID[319:256] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2030
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-636: por_hnf_por_hnf_pmu_mpam_pardid_mask4 (high)



The following table shows the por_hnf_pmu_mpam_pardid_mask4 higher register bit assignments.

Table 5-650: por_hnf_por_hnf_pmu_mpam_pardid_mask4 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask4	MPAM PMU hardlimit and softlimit mask for PARTID [319:256] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

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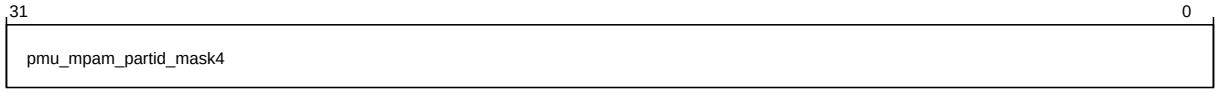
Figure 5-637: por_hnf_por_hnf_pmu_mpam_pardid_mask4 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask4 lower register bit assignments.

Table 5-651: por_hnf_por_hnf_pmu_mpam_pardid_mask4 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask4	MPAM PMU hardlimit and softlimit mask for PARTID [319:256] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.168 por_hnf_pmu_mpam_pardid_mask5

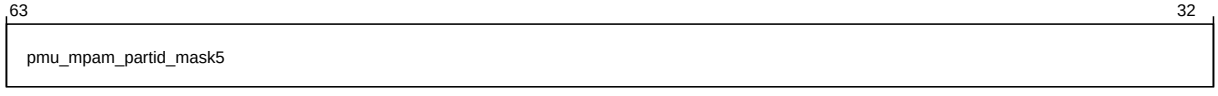
Functions as mask for PARTID[383:320] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2038
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-638: por_hnf_por_hnf_pmu_mpam_pardid_mask5 (high)



The following table shows the por_hnf_pmu_mpam_pardid_mask5 higher register bit assignments.

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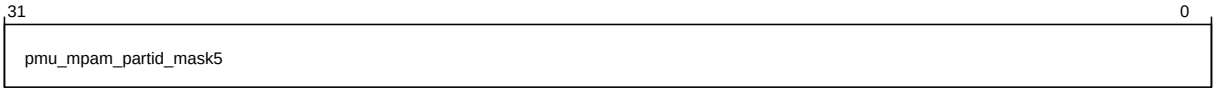
Table 5-652: por_hnf_por_hnf_pmu_mpam_pardid_mask5 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask5	MPAM PMU hardlimit and softlimit mask for PARTID [383:320] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-639: por_hnf_por_hnf_pmu_mpam_pardid_mask5 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask5 lower register bit assignments.

Table 5-653: por_hnf_por_hnf_pmu_mpam_pardid_mask5 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask5	MPAM PMU hardlimit and softlimit mask for PARTID [383:320] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.169 por_hnf_pmu_mpam_pardid_mask6

Functions as mask for PARTID[447:384] filter for MPM PMU events

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2040
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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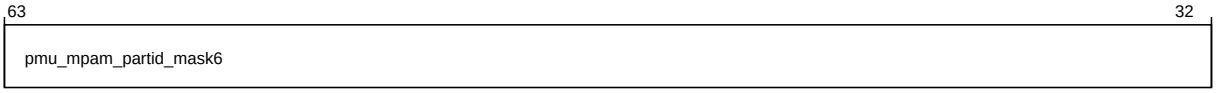
Figure 5-640: por_hnf_por_hnf_pmu_mpam_pardid_mask6 (high)



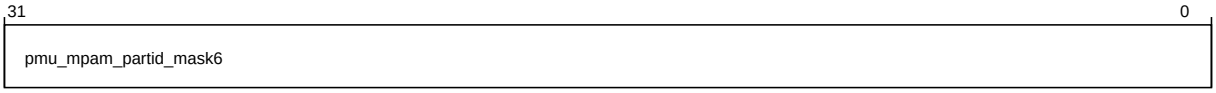
The following table shows the por_hnf_pmu_mpam_pardid_mask6 higher register bit assignments.

Table 5-654: por_hnf_por_hnf_pmu_mpam_pardid_mask6 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask6	MPAM PMU hardlimit and softlimit mask for PARTID [447:384] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-641: por_hnf_por_hnf_pmu_mpam_pardid_mask6 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask6 lower register bit assignments.

Table 5-655: por_hnf_por_hnf_pmu_mpam_pardid_mask6 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask6	MPAM PMU hardlimit and softlimit mask for PARTID [447:384] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.4.170 por_hnf_pmu_mpam_pardid_mask7

Functions as mask for PARTID[511:448] filter for MPM PMU events

Its characteristics are:

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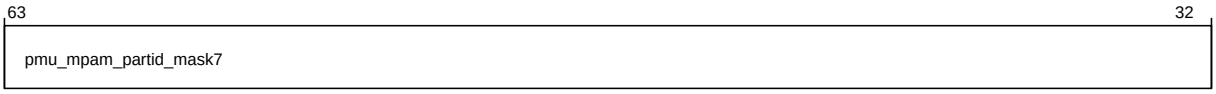
Type RW
Register width (Bits) 64
Address offset 16'h2048
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-642: por_hnf_por_hnf_pmu_mpam_pardid_mask7 (high)



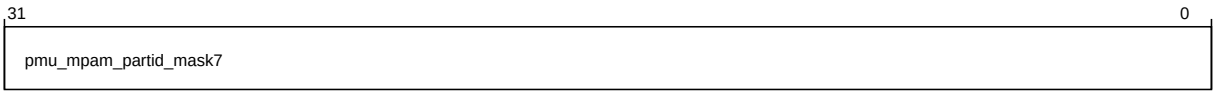
The following table shows the por_hnf_pmu_mpam_pardid_mask7 higher register bit assignments.

Table 5-656: por_hnf_por_hnf_pmu_mpam_pardid_mask7 (high)

Bits	Field name	Description	Type	Reset
63:32	pmu_mpam_partid_mask7	MPAM PMU hardlimit and softlimit mask for PARTID [511:448] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-643: por_hnf_por_hnf_pmu_mpam_pardid_mask7 (low)



The following table shows the por_hnf_pmu_mpam_pardid_mask7 lower register bit assignments.

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Table 5-657: por_hnf_por_hnf_pmu_mpam_pardid_mask7 (low)

Bits	Field name	Description	Type	Reset
31:0	pmu_mpam_partid_mask7	MPAM PMU hardlimit and softlimit mask for PARTID [511:448] 1'b0: PARTID specified is not counted in PMU count. 1'b1: PARTID specified is counted in PMU count. Note: This mask is used only when por_hnf_pmu_mpam_sel is set for PARTID based counting.	RW	64'b0

5.3.5 HN-I register descriptions

This section lists the HN-I registers.

5.3.5.1 por_hni_node_info

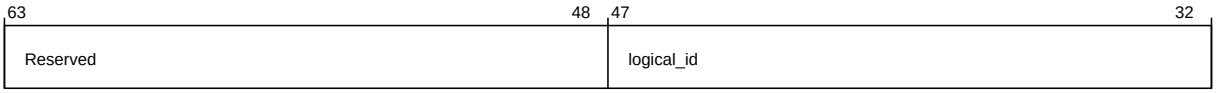
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-644: por_hni_por_hni_node_info (high)



The following table shows the por_hni_node_info higher register bit assignments.

Table 5-658: por_hni_por_hni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

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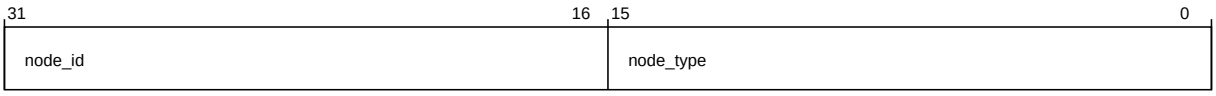
The following figure shows the lower register bit assignments.

Figure 5-645: por_hni_por_hni_node_info (low)



The following table shows the por_hni_node_info lower register bit assignments.

Table 5-659: por_hni_por_hni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0004

5.3.5.2 por_hni_child_info

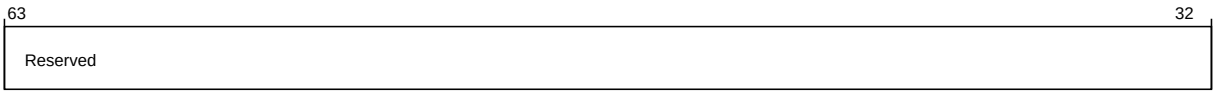
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-646: por_hni_por_hni_child_info (high)



The following table shows the por_hni_child_info higher register bit assignments.

Table 5-660: por_hni_por_hni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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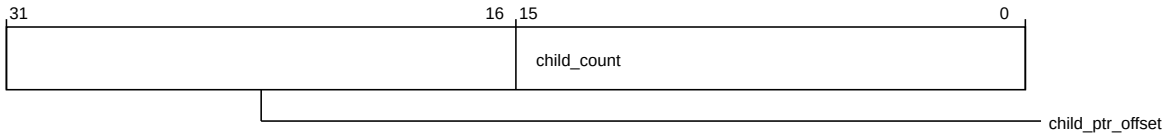
The following figure shows the lower register bit assignments.

Figure 5-647: por_hni_por_hni_child_info (low)



The following table shows the por_hni_child_info lower register bit assignments.

Table 5-661: por_hni_por_hni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.5.3 por_hni_secure_register_groups_override

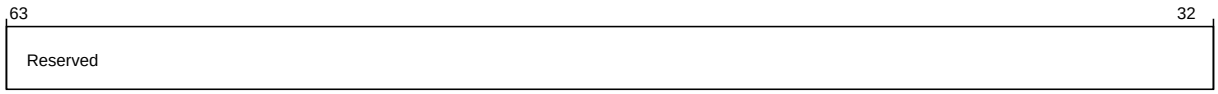
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-648: por_hni_por_hni_secure_register_groups_override (high)



The following table shows the por_hni_secure_register_groups_override higher register bit assignments.

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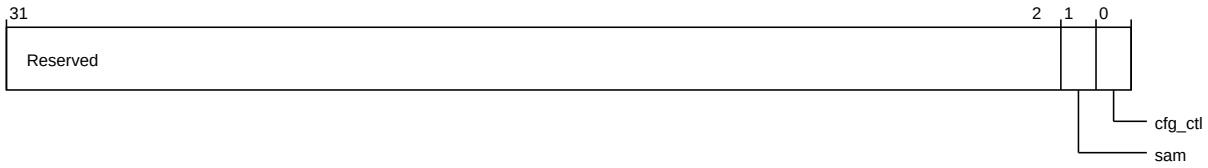
Table 5-662: por_hni_por_hni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-649: por_hni_por_hni_secure_register_groups_override (low)



The following table shows the por_hni_secure_register_groups_override lower register bit assignments.

Table 5-663: por_hni_por_hni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	sam	Allows Non-secure access to Secure SAM registers	RW	1'b0
0	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

5.3.5.4 por_hni_unit_info

Provides component identification information for HN-I.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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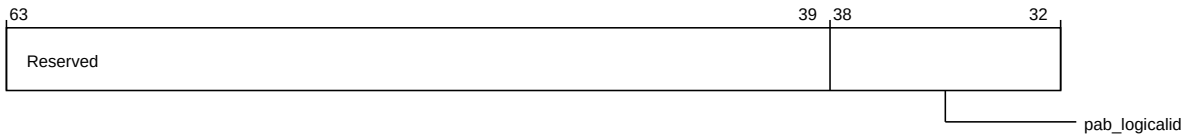
Figure 5-650: por_hni_por_hni_unit_info (high)



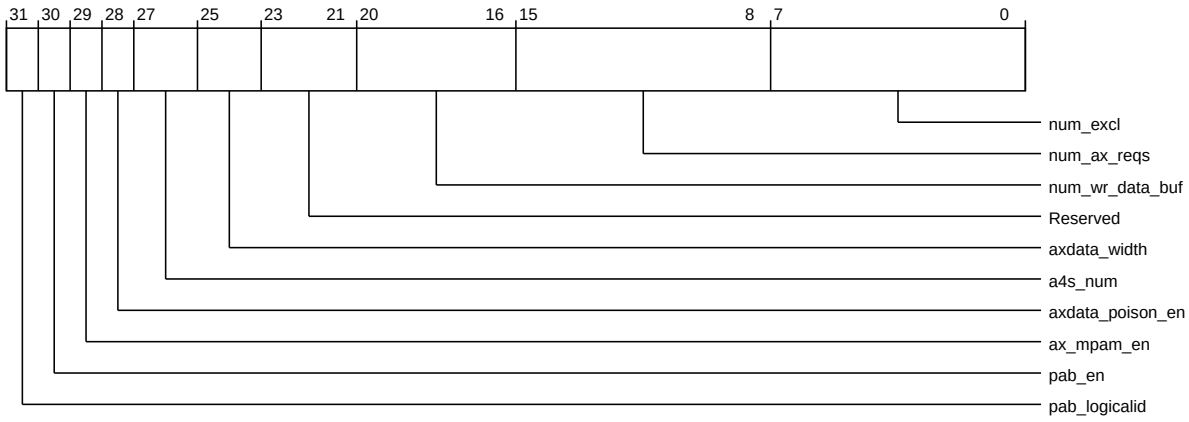
The following table shows the por_hni_unit_info higher register bit assignments.

Table 5-664: por_hni_por_hni_unit_info (high)

Bits	Field name	Description	Type	Reset
63:39	Reserved	Reserved	RO	-
38:32	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-651: por_hni_por_hni_unit_info (low)



The following table shows the por_hni_unit_info lower register bit assignments.

Table 5-665: por_hni_por_hni_unit_info (low)

Bits	Field name	Description	Type	Reset
31	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
30	pab_en	PUB AUB bridge enable 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
29	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
28	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent
27:26	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
25:24	axdata_width	Data width on ACE-Lite/AXI4 interface 2'b00: 128 bits 2'b01: 256 bits 2'b10: 512 bits	RO	Configuration dependent
23:21	Reserved	Reserved	RO	-
20:16	num_wr_data_buf	Number of write data buffers in HN-I	RO	Configuration dependent
15:8	num_ax_reqs	Maximum number of outstanding ACE-Lite/AXI4 requests	RO	Configuration dependent
7:0	num_excl	Number of exclusive monitors in HN-I	RO	Configuration dependent

5.3.5.5 por_hni_sam_addrregion0_cfg

Configures Address Region 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC00
Register reset 64'b11000111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hni_secure_register_groups_override.sam

The following figure shows the higher register bit assignments.

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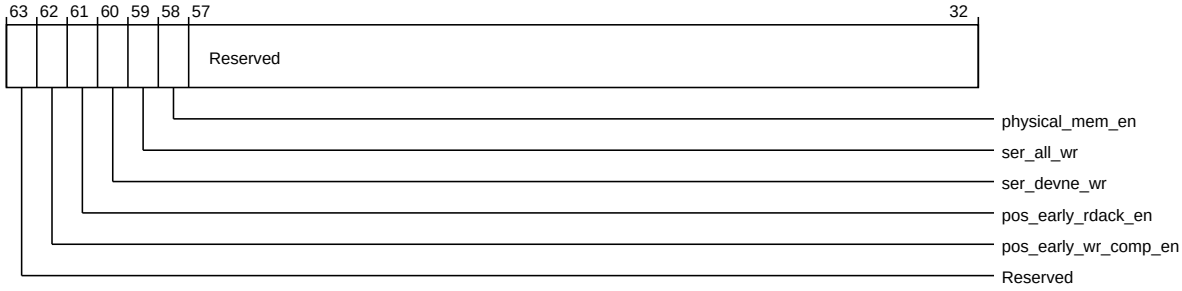
Figure 5-652: por_hni_por_hni_sam_addrregion0_cfg (high)



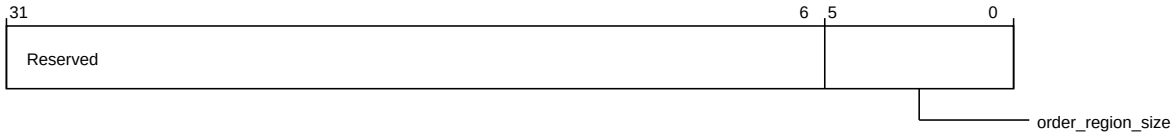
The following table shows the por_hni_sam_addrregion0_cfg higher register bit assignments.

Table 5-666: por_hni_por_hni_sam_addrregion0_cfg (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 0; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 0; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 0	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 0	RW	1'b0
58	physical_mem_en	Address Region 0 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-653: por_hni_por_hni_sam_addrregion0_cfg (low)



The following table shows the por_hni_sam_addrregion0_cfg lower register bit assignments.

Table 5-667: por_hni_por_hni_sam_addrregion0_cfg (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 0 size within Address Region 0 (2^n*4KB)	RW	6'b111111

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5.3.5.6 por_hni_sam_addrregion1_cfg

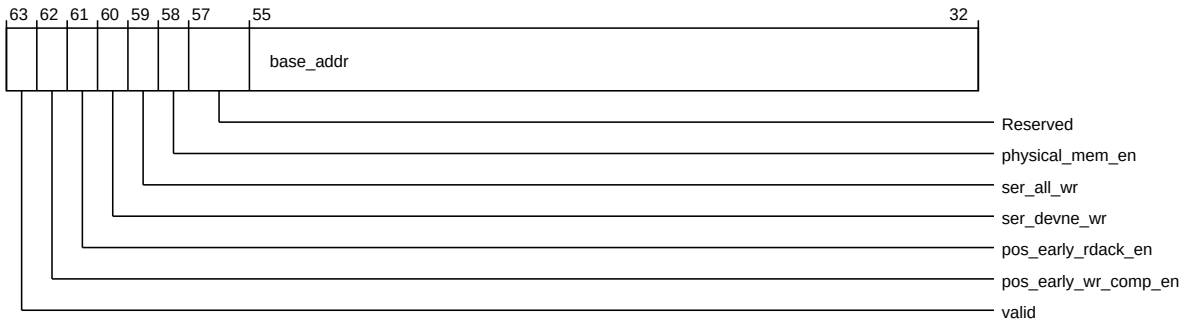
Configures Address Region 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC08
Register reset 64'b0110000000000000000000000000000000000000000000000000000000000000
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hni_secure_register_groups_override.sam

The following figure shows the higher register bit assignments.

Figure 5-654: por_hni_por_hni_sam_addrregion1_cfg (high)



The following table shows the por_hni_sam_addrregion1_cfg higher register bit assignments.

Table 5-668: por_hni_por_hni_sam_addrregion1_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Address Region 1 fields are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 1; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 1; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 1	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 1	RW	1'b0
58	physical_mem_en	Address Region 1 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-

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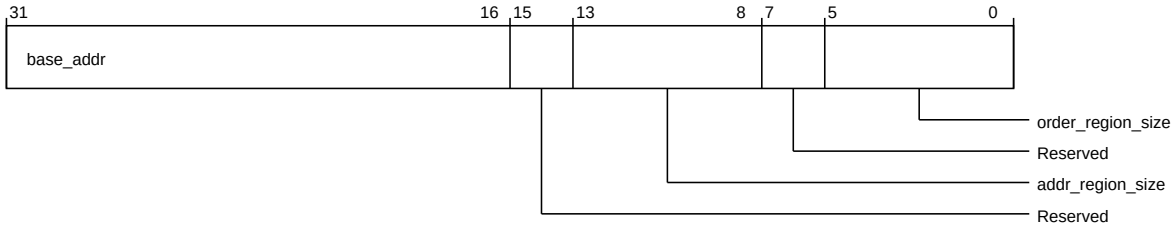
Bits	Field name	Description	Type	Reset
55:32	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	40'h0

The following figure shows the lower register bit assignments.

Figure 5-655: por_hni_por_hni_sam_addrregion1_cfg (low)



The following table shows the por_hni_sam_addrregion1_cfg lower register bit assignments.

Table 5-669: por_hni_por_hni_sam_addrregion1_cfg (low)

Bits	Field name	Description	Type	Reset
31:16	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	40'h0
15:14	Reserved	Reserved	RO	-
13:8	addr_region_size	<n>; used to calculate Address Region 1 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 1 size is less than or equal to 2^(address width).	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 1 size within Address Region 1 (2^n*4KB)	RW	6'h0

5.3.5.7 por_hni_sam_addrregion2_cfg

Configures Address Region 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC10
Register reset 64'b0110000000000000000000000000000000000000000000000000000000000000
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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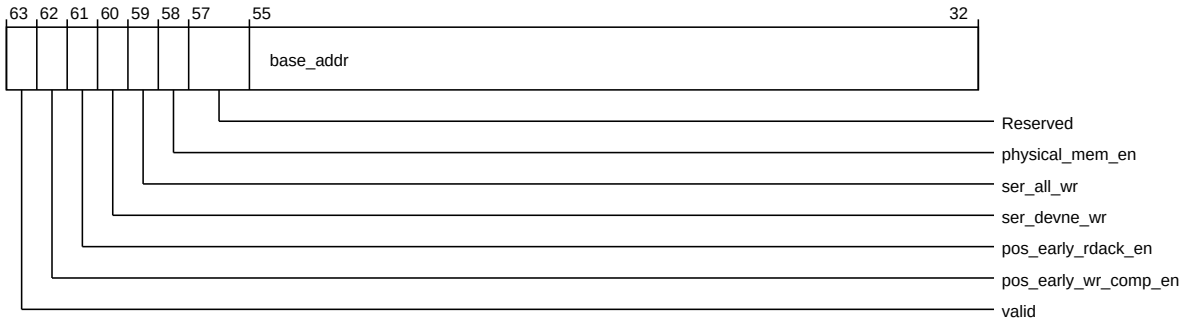
Secure group override por_hni_secure_register_groups_override.sam

The following figure shows the higher register bit assignments.

Figure 5-656: por_hni_por_hni_sam_addrregion2_cfg (high)



The following table shows the por_hni_sam_addrregion2_cfg higher register bit assignments.

Table 5-670: por_hni_por_hni_sam_addrregion2_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Address Region 2 fields are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 2; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 2; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 2	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 2	RW	1'b0
58	physical_mem_en	Address Region 2 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	40'h0

The following figure shows the lower register bit assignments.

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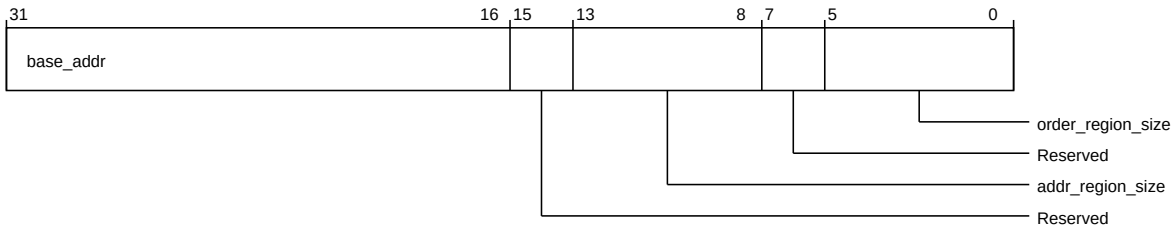
Figure 5-657: por_hni_por_hni_sam_addrregion2_cfg (low)



The following table shows the por_hni_sam_addrregion2_cfg lower register bit assignments.

Table 5-671: por_hni_por_hni_sam_addrregion2_cfg (low)

Bits	Field name	Description	Type	Reset
31:16	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	40'h0
15:14	Reserved	Reserved	RO	-
13:8	addr_region_size	<n>; used to calculate Address Region 2 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 2 size is less than or equal to 2^(address width).	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 2 size within Address Region 2 (2^n*4KB)	RW	6'h0

5.3.5.8 por_hni_sam_addrregion3_cfg

Configures Address Region 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC18
Register reset 64'b0110000000000000000000000000000000000000000000000000000000000000
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hni_secure_register_groups_override.sam

The following figure shows the higher register bit assignments.

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Figure 5-658: por_hni_por_hni_sam_addrregion3_cfg (high)



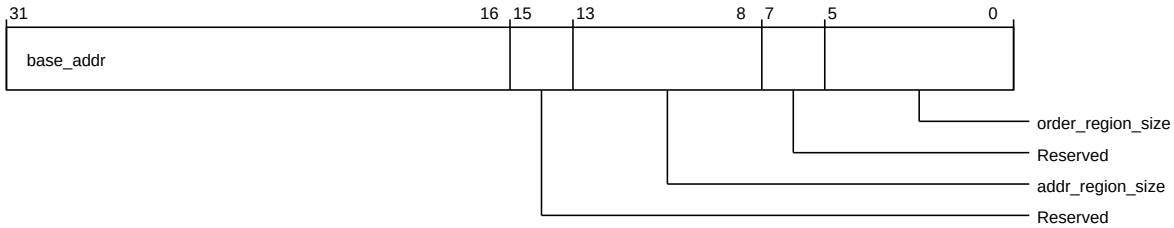
The following table shows the por_hni_sam_addrregion3_cfg higher register bit assignments.

Table 5-672: por_hni_por_hni_sam_addrregion3_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Fields of Address Region 3 are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 3; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 3; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 3	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 3	RW	1'b0
58	physical_mem_en	Address Region 3 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	40'h0

The following figure shows the lower register bit assignments.

Figure 5-659: por_hni_por_hni_sam_addrregion3_cfg (low)



The following table shows the por_hni_sam_addrregion3_cfg lower register bit assignments.

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Table 5-673: por_hni_por_hni_sam_addrregion3_cfg (low)

Bits	Field name	Description	Type	Reset
31:16	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	40'h0
15:14	Reserved	Reserved	RO	-
13:8	addr_region_size	<n>; used to calculate Address Region 3 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 3 size is less than or equal to 2^(address width).	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 3 size within Address Region 3 (2^n*4KB)	RW	6'h0

5.3.5.9 por_hni_cfg_ctl

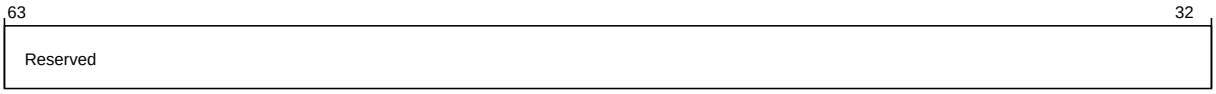
Functions as the configuration control register for HN-I.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b01
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_hni_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

Figure 5-660: por_hni_por_hni_cfg_ctl (high)



The following table shows the por_hni_cfg_ctl higher register bit assignments.

Table 5-674: por_hni_por_hni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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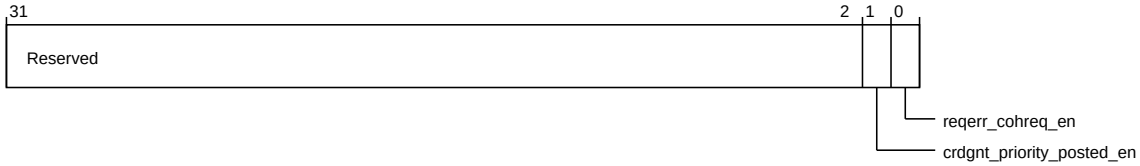
Figure 5-661: por_hni_por_hni_cfg_ctl (low)



The following table shows the por_hni_cfg_ctl lower register bit assignments.

Table 5-675: por_hni_por_hni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	crdgnt_priority_posted_en	Enables High priority Credit Grant responses to Posted requests	RW	1'b0
0	reqerr_cohreq_en	Enables sending of NDE response error to RN and logging of error information for the following requests: 1. Coherent Read 2. CleanUnique/MakeUnique 3. Coherent/CopyBack Write	RW	1'b1

5.3.5.10 por_hni_aux_ctl

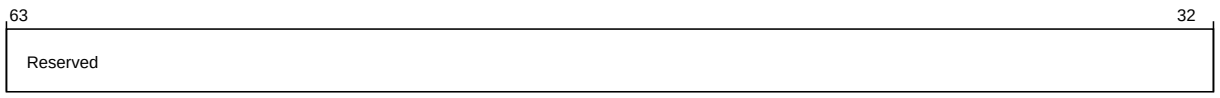
Functions as the auxiliary control register for HN-I.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-662: por_hni_por_hni_aux_ctl (high)



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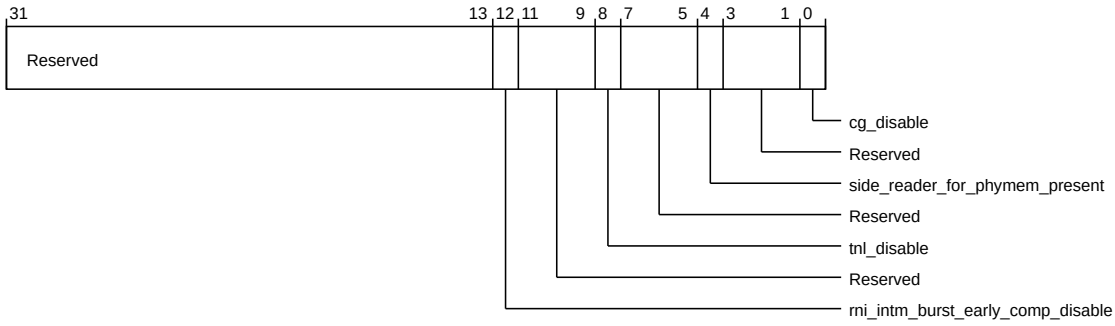
The following table shows the por_hni_aux_ctl higher register bit assignments.

Table 5-676: por_hni_por_hni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-663: por_hni_por_hni_aux_ctl (low)



The following table shows the por_hni_aux_ctl lower register bit assignments.

Table 5-677: por_hni_por_hni_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:13	Reserved	Reserved	RO	-
12	rni_intm_burst_early_comp_disable	Disables Early COMP to RNI for non-last burst writes	RW	1'b0
11:9	Reserved	Reserved	RO	-
8	tnl_disable	Disables RNI-HNI Tunneling in HNI. por_rni_aux_ctl.dis_hni_wr_stream must be set before setting this bit	RW	1'b0
7:5	Reserved	Reserved	RO	-
4	side_reader_for_phymem_present	Enables side reader in physical memory range	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	cg_disable	Disables HN-I architectural clock gates	RW	1'b0

5.3.5.11 por_hni_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64

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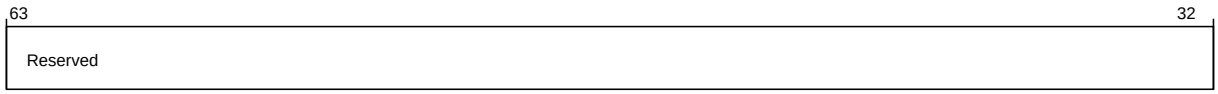
Address offset 16'h3000
Register reset 64'b0000010100101
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-664: por_hni_por_hni_errfr (high)



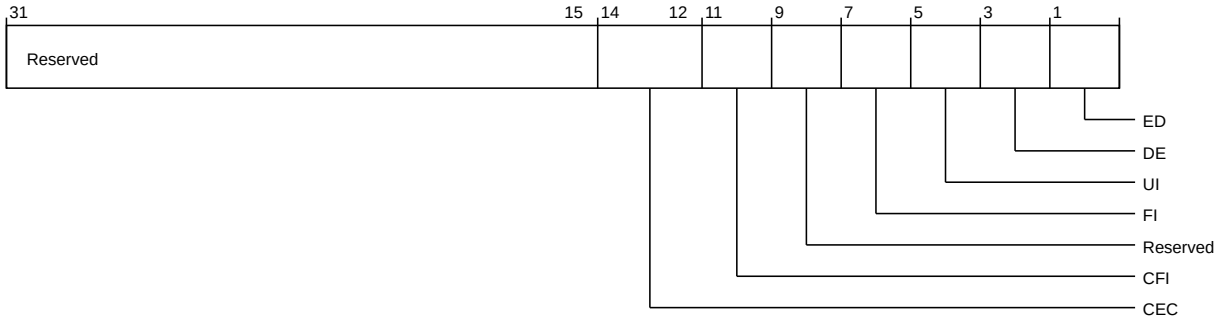
The following table shows the por_hni_errfr higher register bit assignments.

Table 5-678: por_hni_por_hni_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-665: por_hni_por_hni_errfr (low)



The following table shows the por_hni_errfr lower register bit assignments.

Table 5-679: por_hni_por_hni_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10

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Bits	Field name	Description	Type	Reset
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

5.3.5.12 por_hni_errctlr

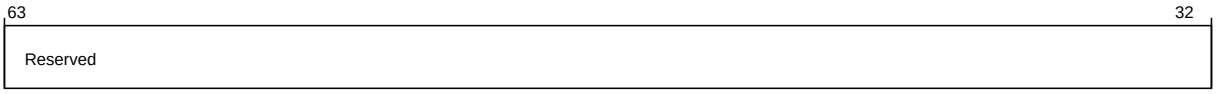
Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-666: por_hni_por_hni_errctlr (high)



The following table shows the por_hni_errctlr higher register bit assignments.

Table 5-680: por_hni_por_hni_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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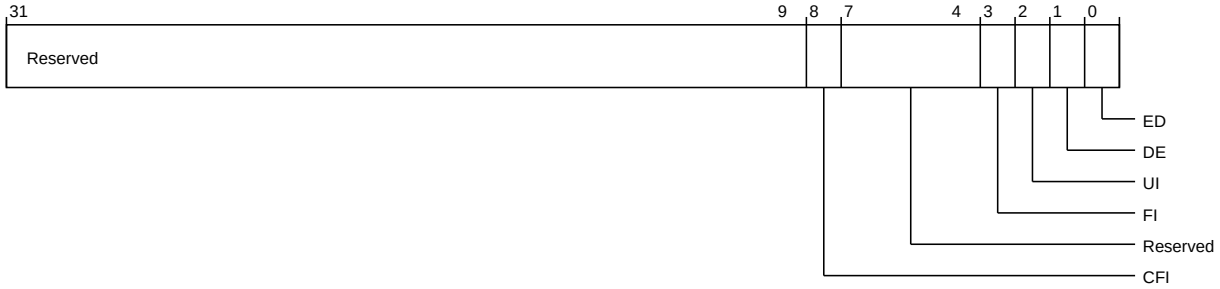
Figure 5-667: por_hni_por_hni_errctlr (low)



The following table shows the por_hni_errctlr lower register bit assignments.

Table 5-681: por_hni_por_hni_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr.ED	RW	1'b0

5.3.5.13 por_hni_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

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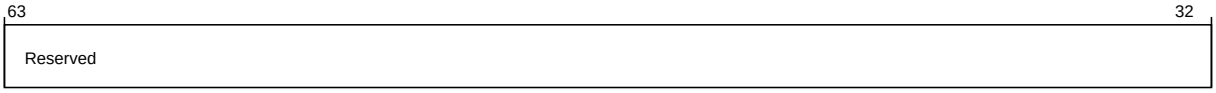
Figure 5-668: por_hni_por_hni_errstatus (high)



The following table shows the por_hni_errstatus higher register bit assignments.

Table 5-682: por_hni_por_hni_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-669: por_hni_por_hni_errstatus (low)



The following table shows the por_hni_errstatus lower register bit assignments.

Table 5-683: por_hni_por_hni_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hni_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0

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Bits	Field name	Description	Type	Reset
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hni_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.5.14 por_hni_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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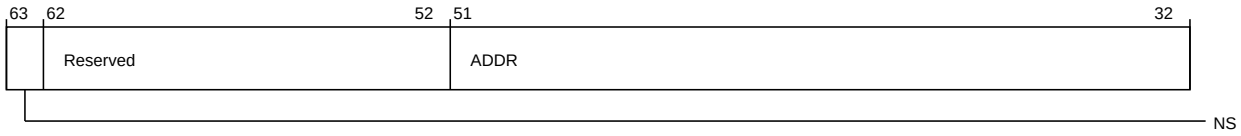
The following figure shows the higher register bit assignments.

Figure 5-670: por_hni_por_hni_erraddr (high)



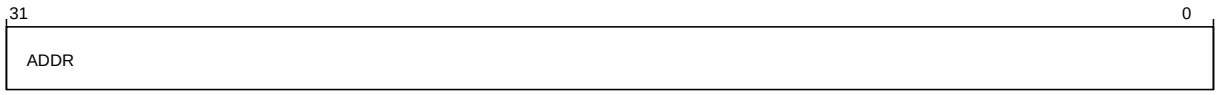
The following table shows the por_hni_erraddr higher register bit assignments.

Table 5-684: por_hni_por_hni_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-671: por_hni_por_hni_erraddr (low)



The following table shows the por_hni_erraddr lower register bit assignments.

Table 5-685: por_hni_por_hni_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

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5.3.5.15 por_hni_errmisc

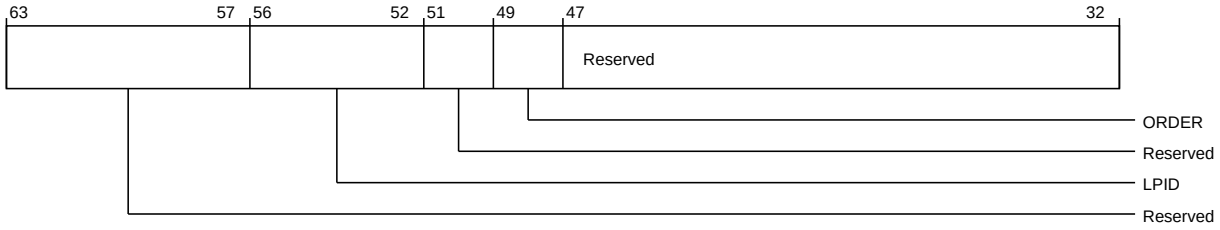
Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-672: por_hni_por_hni_errmisc (high)



The following table shows the por_hni_errmisc higher register bit assignments.

Table 5-686: por_hni_por_hni_errmisc (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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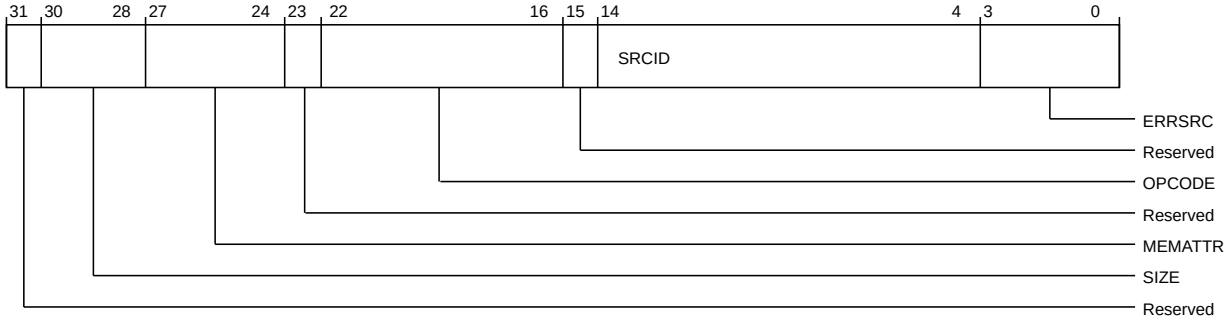
Figure 5-673: por_hni_por_hni_errmisc (low)



The following table shows the por_hni_errmisc lower register bit assignments.

Table 5-687: por_hni_por_hni_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23	Reserved	Reserved	RO	-
22:16	OPCODE	Error opcode	RW	7'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0

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Bits	Field name	Description	Type	Reset
3:0	ERRSRC	Error source 4'b0000: Coherent read 4'b0001: Coherent write 4'b0010: CleanUnique/MakeUnique 4'b0011: Atomic 4'b0100: Illegal configuration read 4'b0101: Illegal configuration write 4'b0110: Configuration write data partial byte enable error 4'b0111: Configuration write data parity error or poison error 4'b1000: BRESP error 4'b1001: Poison error 4'b1010: BRESP error and poison error NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc.SRCID is the only valid field. For other error types, all fields are valid.	RW	4'b0

5.3.5.16 por_hni_errfr_NS

Functions as the Non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b0000010100101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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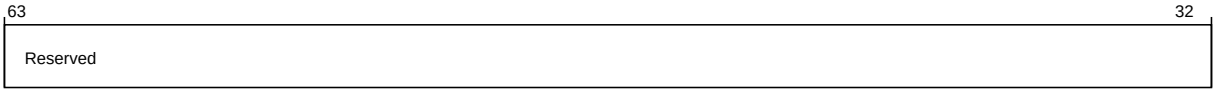
Figure 5-674: por_hni_por_hni_errfr_ns (high)



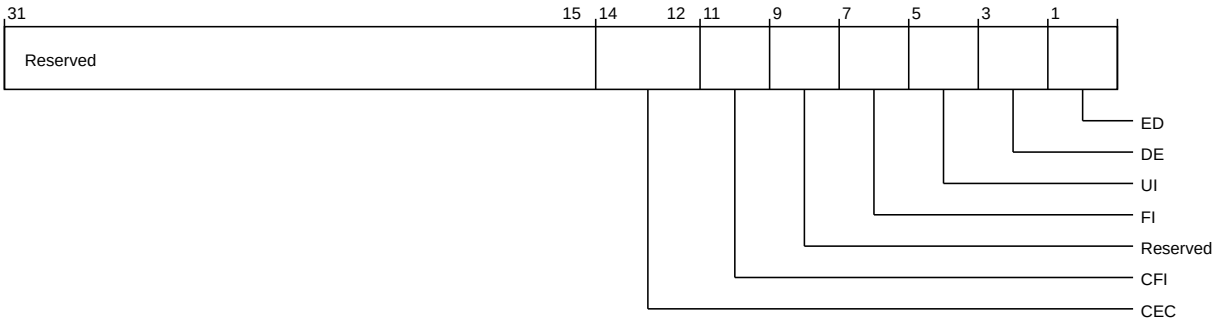
The following table shows the por_hni_errfr_NS higher register bit assignments.

Table 5-688: por_hni_por_hni_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-675: por_hni_por_hni_errfr_ns (low)



The following table shows the por_hni_errfr_NS lower register bit assignments.

Table 5-689: por_hni_por_hni_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

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5.3.5.17 por_hni_errctlr_NS

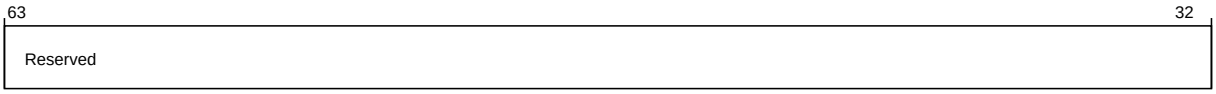
Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-676: por_hni_por_hni_errctlr_ns (high)



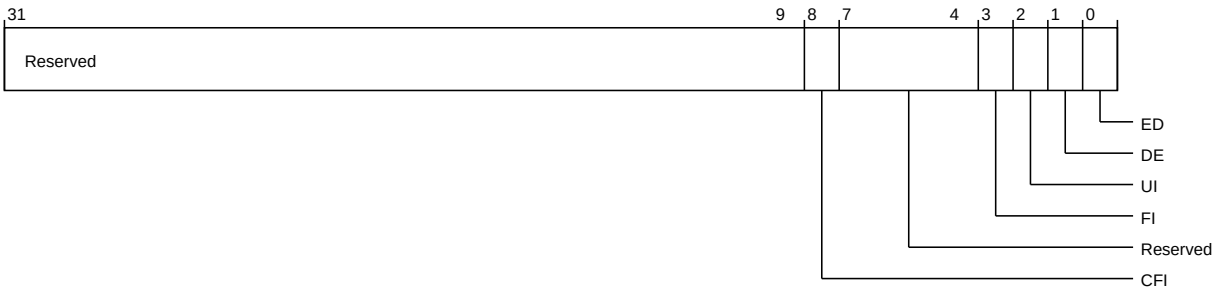
The following table shows the por_hni_errctlr_NS higher register bit assignments.

Table 5-690: por_hni_por_hni_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-677: por_hni_por_hni_errctlr_ns (low)



The following table shows the por_hni_errctlr_NS lower register bit assignments.

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Table 5-691: por_hni_por_hni_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr_NS.ED	RW	1'b0

5.3.5.18 por_hni_errstatus_NS

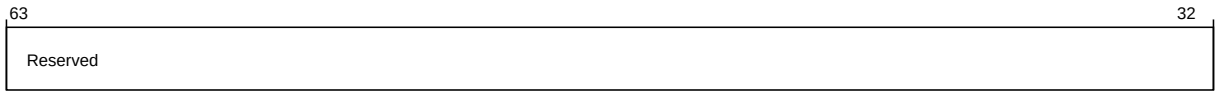
Functions as the Non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-678: por_hni_por_hni_errstatus_ns (high)



The following table shows the por_hni_errstatus_NS higher register bit assignments.

Table 5-692: por_hni_por_hni_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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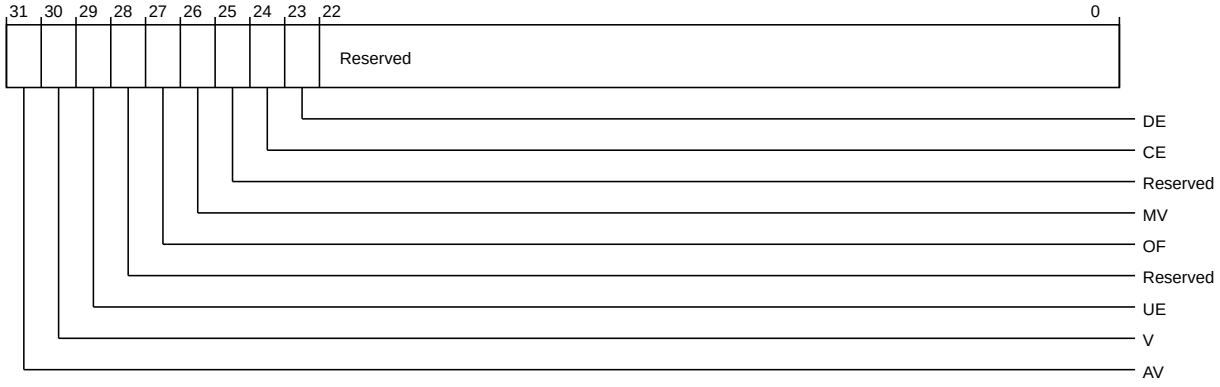
Figure 5-679: por_hni_por_hni_errstatus_ns (low)



The following table shows the por_hni_errstatus_NS lower register bit assignments.

Table 5-693: por_hni_por_hni_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hni_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hni_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0

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Bits	Field name	Description	Type	Reset
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.5.19 por_hni_erraddr_NS

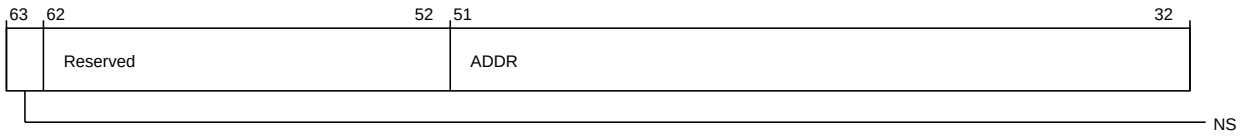
Contains the Non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-680: por_hni_por_hni_erraddr_ns (high)



The following table shows the por_hni_erraddr_NS higher register bit assignments.

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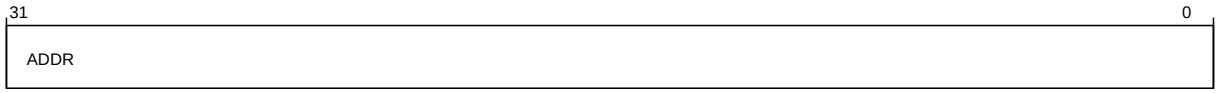
Table 5-694: por_hni_por_hni_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-681: por_hni_por_hni_erraddr_ns (low)



The following table shows the por_hni_erraddr_NS lower register bit assignments.

Table 5-695: por_hni_por_hni_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

5.3.5.20 por_hni_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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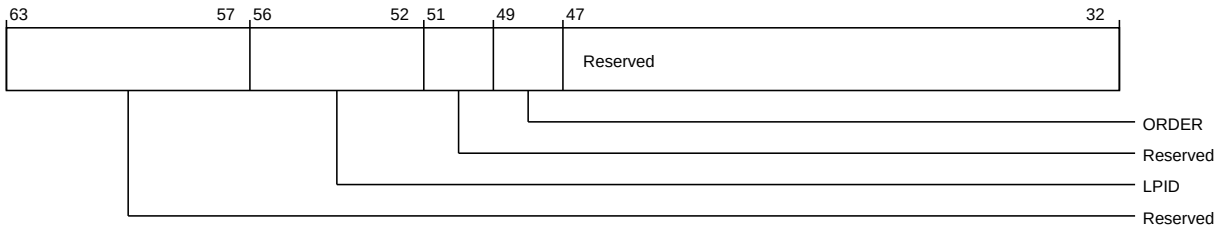
Figure 5-682: por_hni_por_hni_errmisc_ns (high)



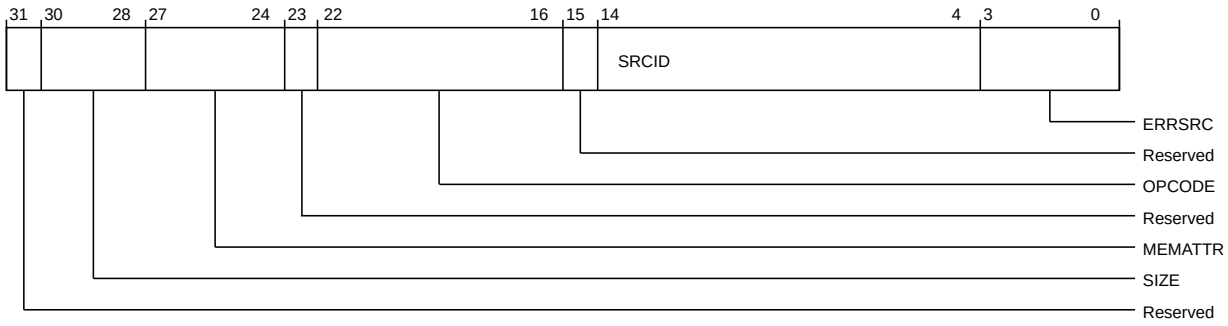
The following table shows the por_hni_errmisc_NS higher register bit assignments.

Table 5-696: por_hni_por_hni_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-683: por_hni_por_hni_errmisc_ns (low)



The following table shows the por_hni_errmisc_NS lower register bit assignments.

Table 5-697: por_hni_por_hni_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
22:16	OPCODE	Error opcode	RW	7'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0000: Coherent read 4'b0001: Coherent write 4'b0010: CleanUnique/MakeUnique 4'b0011: Atomic 4'b0100: Illegal configuration read 4'b0101: Illegal configuration write 4'b0110: Configuration write data partial byte enable error 4'b0111: Configuration write data parity error or poison error 4'b1000: BRESP error 4'b1001: Poison error 4'b1010: BRESP error and poison error NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc_NS.SRCID is the only valid field. For other error types, all fields are valid.	RW	4'b0

5.3.5.21 por_hni_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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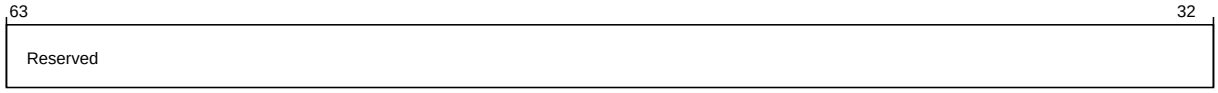
Figure 5-684: por_hni_por_hni_pmu_event_sel (high)



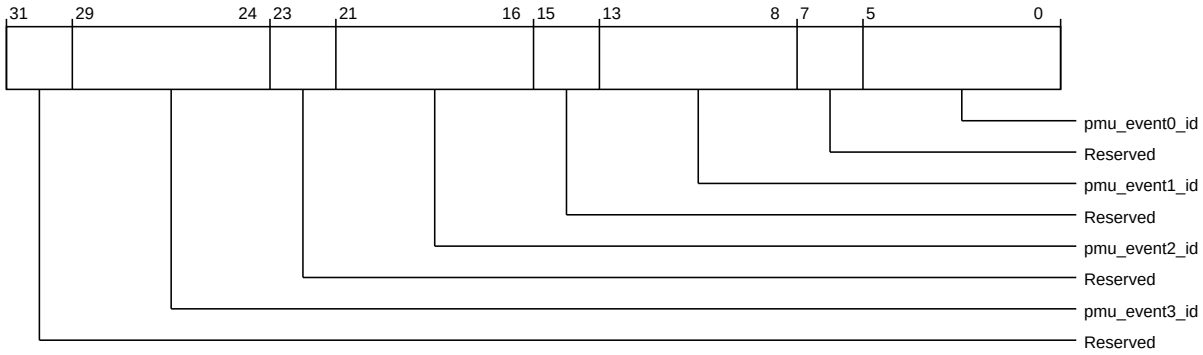
The following table shows the por_hni_pmu_event_sel higher register bit assignments.

Table 5-698: por_hni_por_hni_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-685: por_hni_por_hni_pmu_event_sel (low)



The following table shows the por_hni_pmu_event_sel lower register bit assignments.

Table 5-699: por_hni_por_hni_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	HN-I PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	HN-I PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	HN-I PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	HN-I PMU Event 0 select 6'h00: No event 6'h20: RRT read occupancy count overflow 6'h21: RRT write occupancy count overflow 6'h22: RDT read occupancy count overflow 6'h23: RDT write occupancy count overflow 6'h24: WDB occupancy count overflow 6'h25: RRT read allocation 6'h26: RRT write allocation 6'h27: RDT read allocation 6'h28: RDT write allocation 6'h29: WDB allocation 6'h2A: RETRYACK TXRSP flit sent 6'h2B: ARVALID set without ARREADY event 6'h2C: ARREADY set without ARVALID event 6'h2D: AWVALID set without AWREADY event 6'h2E: AWREADY set without AWVALID event 6'h2F: WVALID set without WREADY event 6'h30: TXDAT stall (TXDAT valid but no link credit available) 6'h31: Non-PCIe serialization event 6'h32: PCIe serialization event NOTE: All other encodings are reserved.	RW	6'b0

5.3.6 XP register descriptions

This section lists the XP registers.

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5.3.6.1 por_mxp_node_info

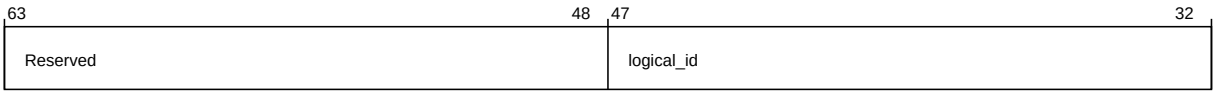
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-686: por_mxp_por_mxp_node_info (high)



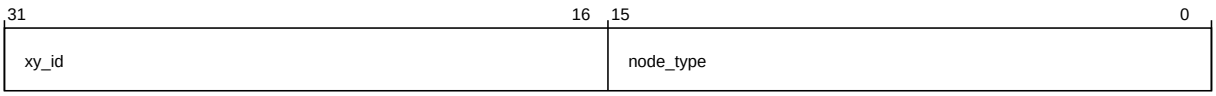
The following table shows the por_mxp_node_info higher register bit assignments.

Table 5-700: por_mxp_por_mxp_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-687: por_mxp_por_mxp_node_info (low)



The following table shows the por_mxp_node_info lower register bit assignments.

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Table 5-701: por_mxp_por_mxp_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	xy_id	Identifies (X,Y) location of XP within the mesh NOTE: The (X,Y) location is specified following the node ID format as defined in Node ID mapping section, with the bottom 3 bits, corresponding to port ID and device ID, set to 0. Bits 31:11 must always be set to 0. The range of bits representing the (X,Y) location varies for different node ID formats.	RO	16'h0000
15:0	node_type	CI-700 node type identifier	RO	16'h0006

5.3.6.2 por_mxp_device_port_connect_info_p0

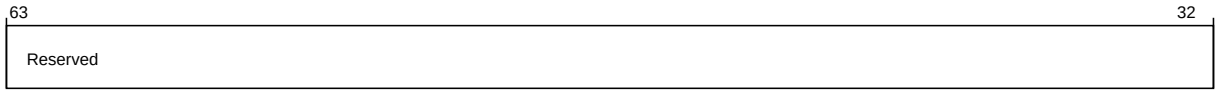
Contains device port connection information for port 0.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-688: por_mxp_por_mxp_device_port_connect_info_p0 (high)



The following table shows the por_mxp_device_port_connect_info_p0 higher register bit assignments.

Table 5-702: por_mxp_por_mxp_device_port_connect_info_p0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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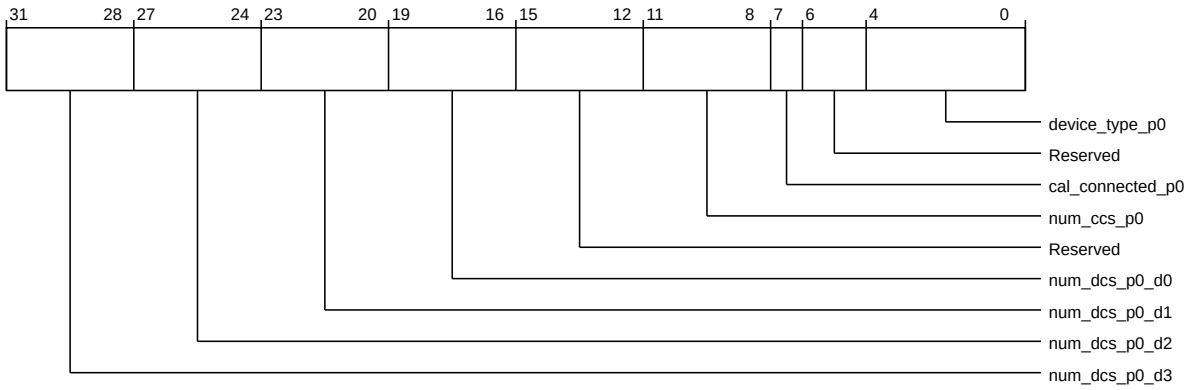
Figure 5-689: por_mxp_por_mxp_device_port_connect_info_p0 (low)



The following table shows the por_mxp_device_port_connect_info_p0 lower register bit assignments.

Table 5-703: por_mxp_por_mxp_device_port_connect_info_p0 (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p0_d3	Number of device credited slices connected to port 0 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p0_d2	Number of device credited slices connected to port 0 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p0_d1	Number of device credited slices connected to port 0 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p0_d0	Number of device credited slices connected to port 0 device 0 (Allowed values: 0-4)	RO	Configuration dependent
15:12	Reserved	Reserved	RO	-
11:8	num_ccs_p0	Number of CAL credited slices connected to port 0 (Allowed values: 0-2)	RO	Configuration dependent
7	cal_connected_p0	When set, CAL is connected on port 0 (Allowed values: 0-1)	RO	(MXP_NUM_DEV_P0_PARAM > 1) ? 1'b1 : 1'b0
6:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4:0	device_type_p0	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F_CHIB 5'b00101: RN-F_CHIB_ESAM 5'b00110: RN-F_CHIA 5'b00111: RN-F_CHIA_ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F_CHIC 5'b01101: SBSX 5'b01110: HN-F 5'b01111: SN-F_CHIE 5'b10000: SN-F_CHID 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100: RN-F_CHID 5'b10101: RN-F_CHID_ESAM 5'b10110: RN-F_CHIC 5'b10111: RN-F_CHIC_ESAM 5'b11000: RN-F_CHIE 5'b11001: RN-F_CHIE_ESAM	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
4:0	device_type_p0	5'b11010: Reserved 5'b11011: Reserved 5'b11100: MTSX 5'b11101-5'b11111: Reserved	RO	Configuration dependent

5.3.6.3 por_mxp_device_port_connect_info_p1

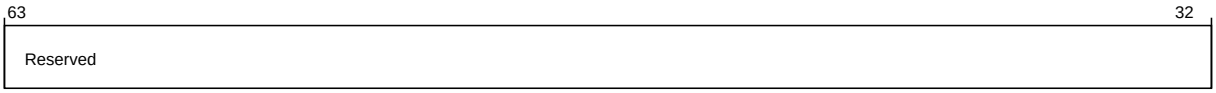
Contains device port connection information for port 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h10
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-690: por_mxp_por_mxp_device_port_connect_info_p1 (high)



The following table shows the por_mxp_device_port_connect_info_p1 higher register bit assignments.

Table 5-704: por_mxp_por_mxp_device_port_connect_info_p1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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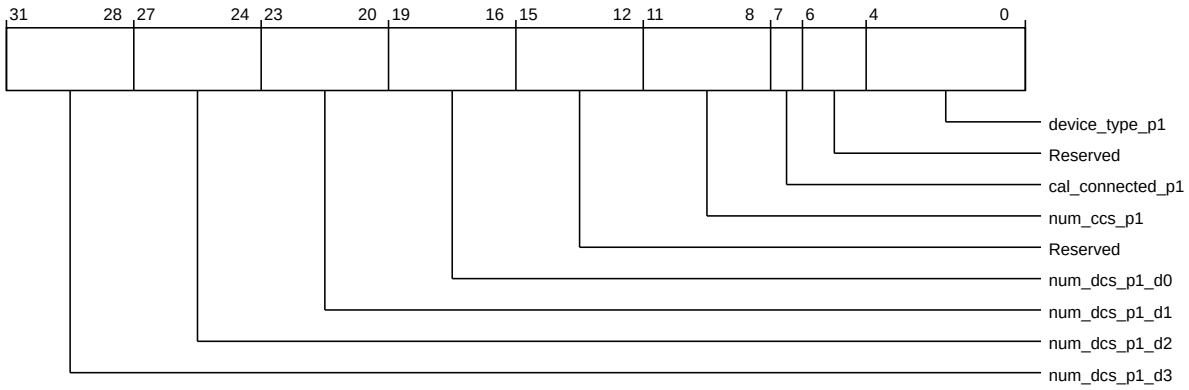
Figure 5-691: por_mxp_por_mxp_device_port_connect_info_p1 (low)



The following table shows the por_mxp_device_port_connect_info_p1 lower register bit assignments.

Table 5-705: por_mxp_por_mxp_device_port_connect_info_p1 (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p1_d3	Number of device credited slices connected to port 1 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p1_d2	Number of device credited slices connected to port 1 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p1_d1	Number of device credited slices connected to port 1 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p1_d0	Number of device credited slices connected to port 1 device 0 (Allowed values: 0-4)	RO	Configuration dependent
15:12	Reserved	Reserved	RO	-
11:8	num_ccs_p1	Number of CAL credited slices connected to port 1 (Allowed values: 0-2)	RO	Configuration dependent
7	cal_connected_p1	When set, CAL is connected on port 1 (Allowed values: 0-1)	RO	(MXP_NUM_DEV_P1_PARAM > 1) ? 1'b1 : 1'b0
6:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4:0	device_type_p1	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F_CHIB 5'b00101: RN-F_CHIB_ESAM 5'b00110: RN-F_CHIA 5'b00111: RN-F_CHIA_ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F_CHIC 5'b01101: SBSX 5'b01110: HN-F 5'b01111: SN-F_CHIE 5'b10000: SN-F_CHID 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100: RN-F_CHID 5'b10101: RN-F_CHID_ESAM 5'b10110: RN-F_CHIC 5'b10111: RN-F_CHIC_ESAM 5'b11000: RN-F_CHIE 5'b11001: RN-F_CHIE_ESAM	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
4:0	device_type_p1	5'b11010: Reserved 5'b11011: Reserved 5'b11100: MTSX 5'b11101-5'b11111: Reserved	RO	Configuration dependent

5.3.6.4 por_mxp_mesh_port_connect_info_east

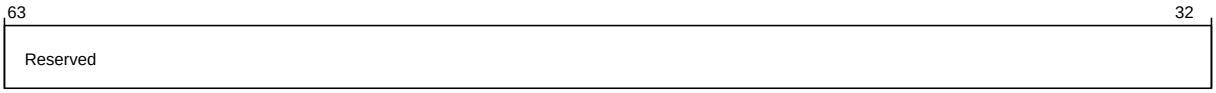
Contains port connection information for East port.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h18
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-692: por_mxp_por_mxp_mesh_port_connect_info_east (high)



The following table shows the por_mxp_mesh_port_connect_info_east higher register bit assignments.

Table 5-706: por_mxp_por_mxp_mesh_port_connect_info_east (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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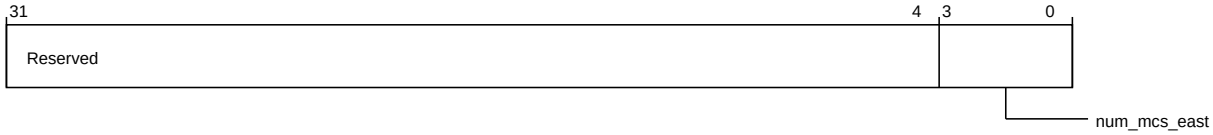
Figure 5-693: por_mxp_por_mxp_mesh_port_connect_info_east (low)



The following table shows the por_mxp_mesh_port_connect_info_east lower register bit assignments.

Table 5-707: por_mxp_por_mxp_mesh_port_connect_info_east (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_east	Number of mesh credited slices connected to East port (Allowed values: 0-4)	RO	Configuration dependent

5.3.6.5 por_mxp_mesh_port_connect_info_north

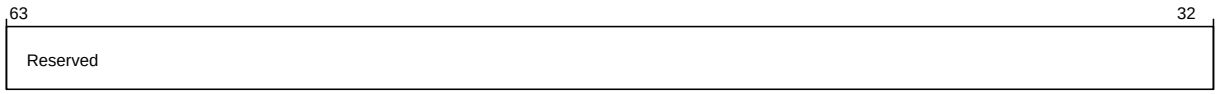
Contains port connection information for North port.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h20
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-694: por_mxp_por_mxp_mesh_port_connect_info_north (high)



The following table shows the por_mxp_mesh_port_connect_info_north higher register bit assignments.

Table 5-708: por_mxp_por_mxp_mesh_port_connect_info_north (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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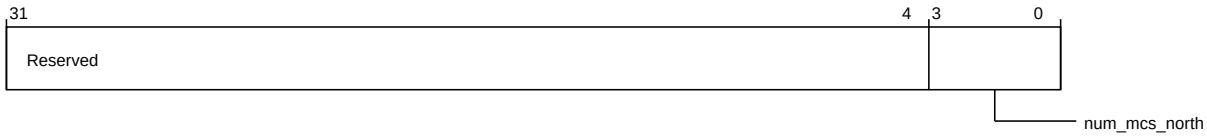
The following figure shows the lower register bit assignments.

Figure 5-695: por_mxp_por_mxp_mesh_port_connect_info_north (low)



The following table shows the por_mxp_mesh_port_connect_info_north lower register bit assignments.

Table 5-709: por_mxp_por_mxp_mesh_port_connect_info_north (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_north	Number of mesh credited slices connected to North port (Allowed values: 0-4)	RO	Configuration dependent

5.3.6.6 por_mxp_device_port_connect_info_p$index

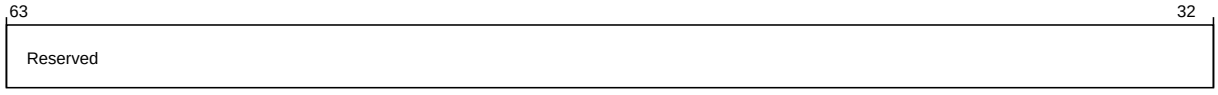
This register repeats 3 times. It is parameterized by the $index from 2 to 5. Contains device port connection information for port $index.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset NODE_TYPE_BASE + 16'h28 + (8 * ($index-2))
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-696: por_mxp_por_mxp_device_port_connect_info_p$index (high)



The following table shows the por_mxp_device_port_connect_info_p$index higher register bit assignments.

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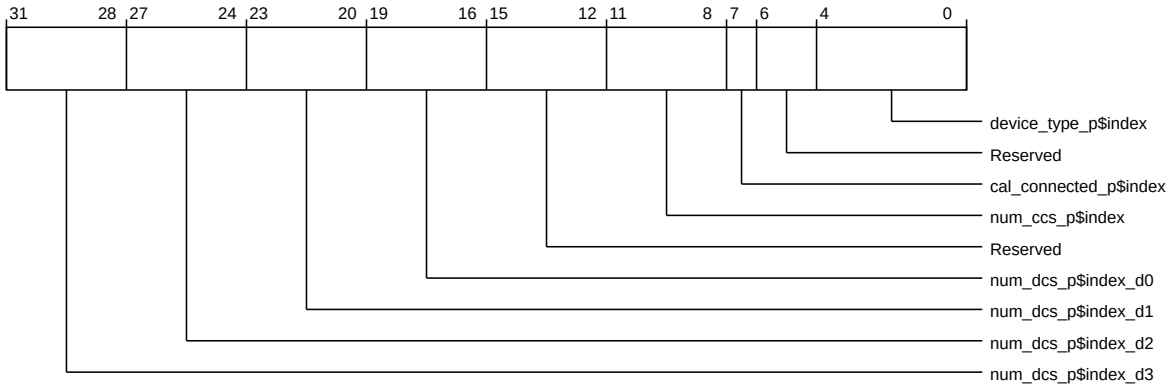
Table 5-710: por_mxp_por_mxp_device_port_connect_info_p$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-697: por_mxp_por_mxp_device_port_connect_info_p$index (low)



The following table shows the por_mxp_device_port_connect_info_p$index lower register bit assignments.

Table 5-711: por_mxp_por_mxp_device_port_connect_info_p$index (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p $index_d3	Number of device credited slices connected to port $index device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p $index_d2	Number of device credited slices connected to port $index device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p $index_d1	Number of device credited slices connected to port $index device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p $index_d0	Number of device credited slices connected to port $index device 0 (Allowed values: 0-4)	RO	Configuration dependent
15:12	Reserved	Reserved	RO	-
11:8	num_ccs_p $index	Number of CAL credited slices connected to port $index (Allowed values: 0-2)	RO	Configuration dependent
7	cal_connected_p $index	When set, CAL is connected on port $index (Allowed values: 0-1)	RO	(MXP_NUM_DEV_P$index_PARAM > 1) ? 1'b1 : 1'b0
6:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4:0	device_type_p $index	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F_CHIB 5'b00101: RN-F_CHIB_ESAM 5'b00110: RN-F_CHIA 5'b00111: RN-F_CHIA_ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F_CHIC 5'b01101: SBSX 5'b01110: HN-F 5'b01111: SN-F_CHIE 5'b10000: SN-F_CHID 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100: RN-F_CHID 5'b10101: RN-F_CHID_ESAM 5'b10110: RN-F_CHIC 5'b10111: RN-F_CHIC_ESAM 5'b11000: RN-F_CHIE 5'b11001: RN-F_CHIE_ESAM	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
4:0	device_type_p$index	5'b11010: Reserved 5'b11011: Reserved 5'b11100: MTSX 5'b11101-5'b11111: Reserved	RO	Configuration dependent

5.3.6.7 por_mxp_child_info

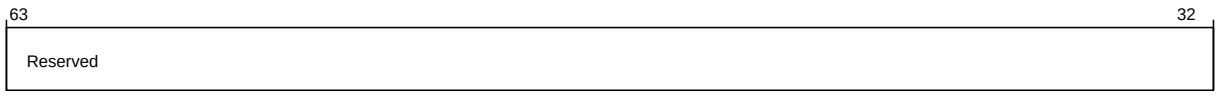
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-698: por_mxp_por_mxp_child_info (high)



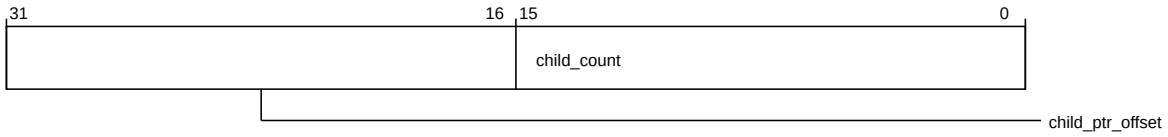
The following table shows the por_mxp_child_info higher register bit assignments.

Table 5-712: por_mxp_por_mxp_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-699: por_mxp_por_mxp_child_info (low)



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The following table shows the por_mxp_child_info lower register bit assignments.

Table 5-713: por_mxp_por_mxp_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

5.3.6.8 por_mxp_child_pointer_$index

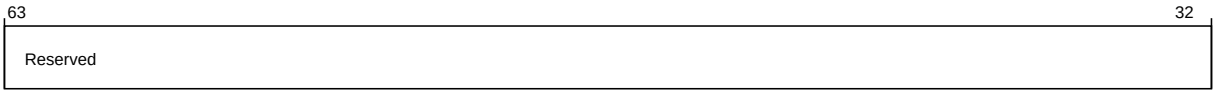
This register repeats 15 times. It is parameterized by the $index from 0 to 15. Contains base address of the configuration slave for child $index.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset CHILD_POINTER_BASE + 16'h0 + (8 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-700: por_mxp_por_mxp_child_pointer_$index (high)



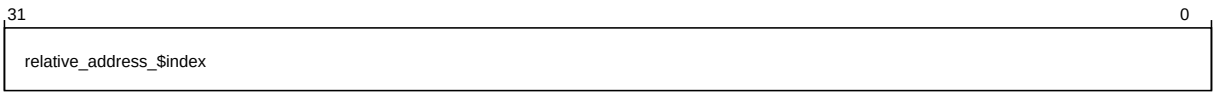
The following table shows the por_mxp_child_pointer_$index higher register bit assignments.

Table 5-714: por_mxp_por_mxp_child_pointer_$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-701: por_mxp_por_mxp_child_pointer_$index (low)



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The following table shows the por_mxp_child_pointer_$index lower register bit assignments.

Table 5-715: por_mxp_por_mxp_child_pointer_$index (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_$index	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CI-700 1'b0: Indicates this child pointer points to a configuration node that is internal to CI-700 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

5.3.6.9 por_mxp_child_pointer_$index

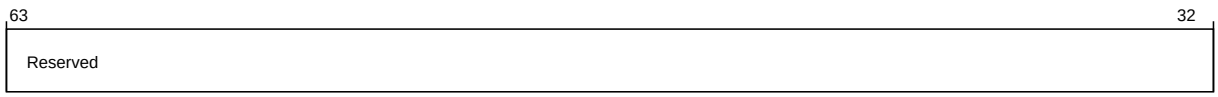
This register repeats 15 times. It is parameterized by the $index from 16 to 31. Contains base address of the configuration slave for child $index.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset CHILD_POINTER_BASE + 16'h0 + (8 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-702: por_mxp_por_mxp_child_pointer_$index (high)



The following table shows the por_mxp_child_pointer_$index higher register bit assignments.

Table 5-716: por_mxp_por_mxp_child_pointer_$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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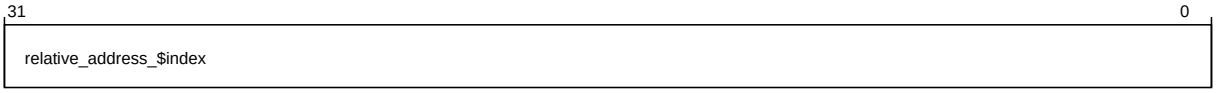
Figure 5-703: por_mxp_por_mxp_child_pointer_$index (low)



The following table shows the por_mxp_child_pointer_$index lower register bit assignments.

Table 5-717: por_mxp_por_mxp_child_pointer_$index (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_$index	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CI-700 1'b0: Indicates this child pointer points to a configuration node that is internal to CI-700 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

5.3.6.10 por_mxp_p0_info

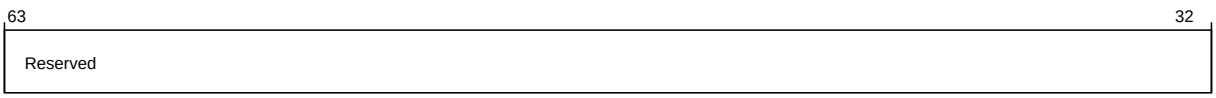
Provides component identification information for XP port 0.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-704: por_mxp_por_mxp_p0_info (high)



The following table shows the por_mxp_p0_info higher register bit assignments.

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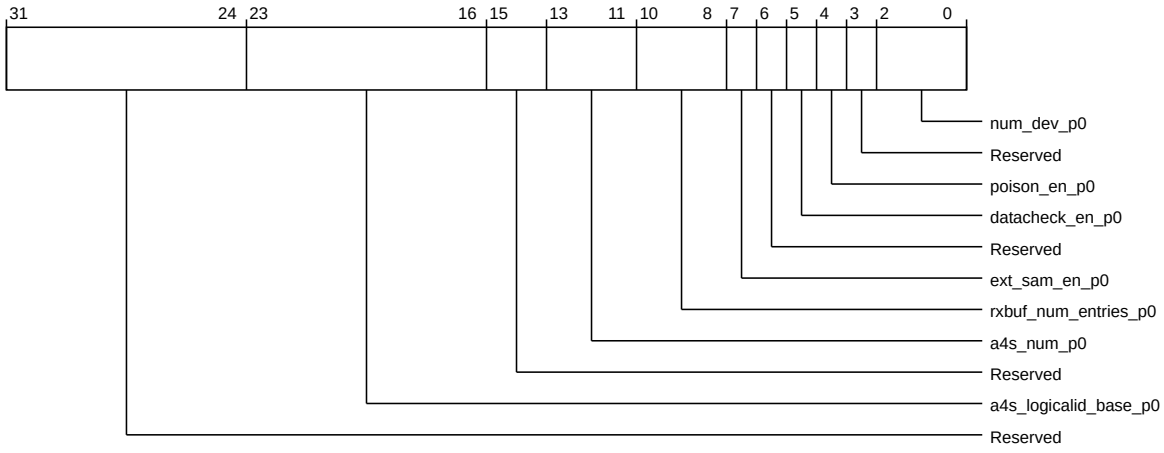
Table 5-718: por_mxp_por_mxp_p0_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-705: por_mxp_por_mxp_p0_info (low)



The following table shows the por_mxp_p0_info lower register bit assignments.

Table 5-719: por_mxp_por_mxp_p0_info (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	a4s_logicalid_base_p0	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p0	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p0	Number of input buffers for each device at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p0	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p0	Datacheck enable	RO	Configuration dependent
4	poison_en_p0	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p0	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

5.3.6.11 por_mxp_p1_info

Provides component identification information for XP port 1.

Its characteristics are:

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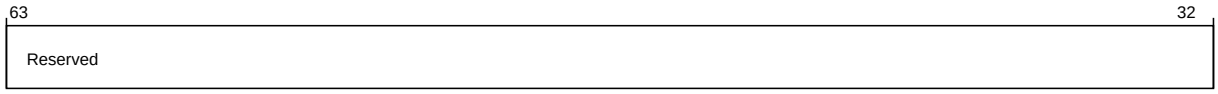
Type RO
Register width (Bits) 64
Address offset 16'h908
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-706: por_mxp_por_mxp_p1_info (high)



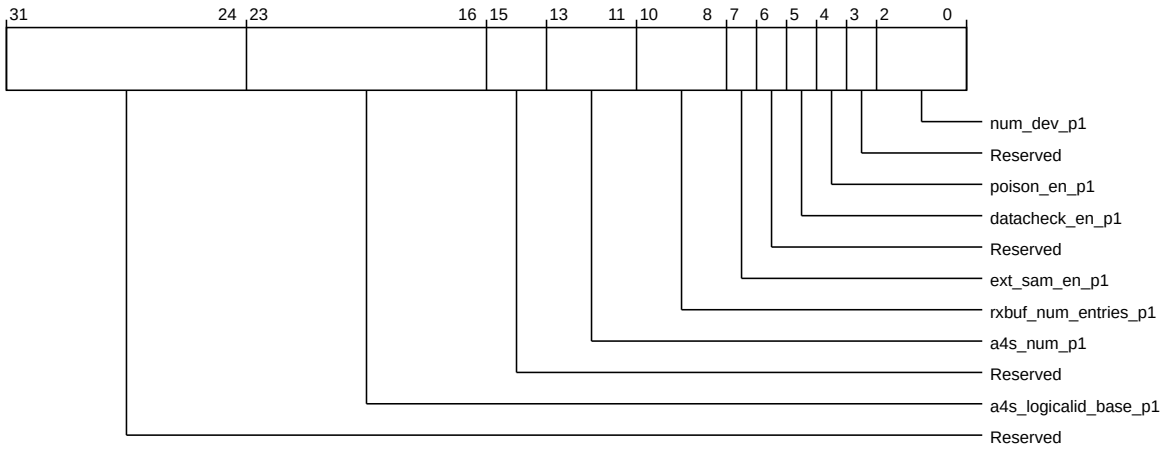
The following table shows the por_mxp_p1_info higher register bit assignments.

Table 5-720: por_mxp_por_mxp_p1_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-707: por_mxp_por_mxp_p1_info (low)



The following table shows the por_mxp_p1_info lower register bit assignments.

Table 5-721: por_mxp_por_mxp_p1_info (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
23:16	a4s_logicalid_base_p1	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p1	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p1	Number of input buffers at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p1	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p1	Datacheck enable	RO	Configuration dependent
4	poison_en_p1	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p1	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

5.3.6.12 por_dtm_unit_info

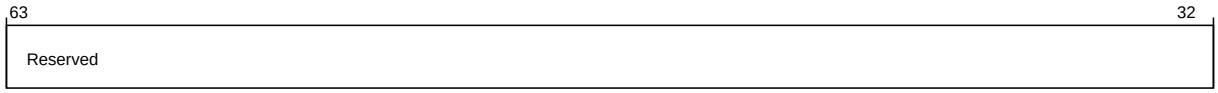
Provides component identification information for XP port 0 and 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h910
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-708: por_mxp_por_dtm_unit_info (high)



The following table shows the por_dtm_unit_info higher register bit assignments.

Table 5-722: por_mxp_por_dtm_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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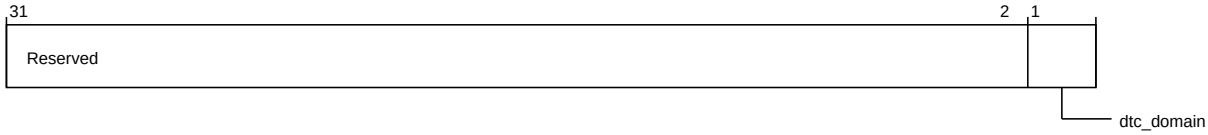
Figure 5-709: por_mxp_por_dtm_unit_info (low)



The following table shows the por_dtm_unit_info lower register bit assignments.

Table 5-723: por_mxp_por_dtm_unit_info (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	dtc_domain	DTC domain number associated with this DTM	RO	Configuration dependent

5.3.6.13 por_dtm_unit_info_dt$index

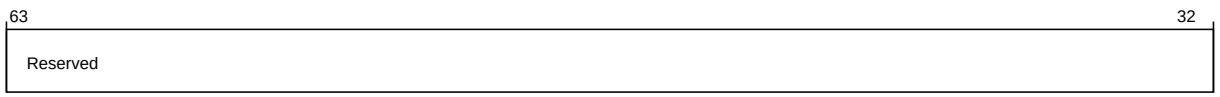
This register repeats once. It is parameterized by the $index from 1 to 2. Provides component identification information for XP ports $index and $index+1. NOTE: There will be max. of 3 DTM Unit Info registers based on MXP_MULTIPLE_DTM_EN_PARAM and MXP_NUM_DEV_PORT_PARAM value. Each successive DTM Unit Info register will be at the next 8 byte address boundary. Each successive DTM Unit Info register will be named with the suffix corresponding to the DT register number. For example por_dtm_unit_info_dt<1:2>

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_INFO_BASE + 16'h18 + (8 * ($index-1))
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-710: por_mxp_por_dtm_unit_info_dt$index (high)



The following table shows the por_dtm_unit_info_dt$index higher register bit assignments.

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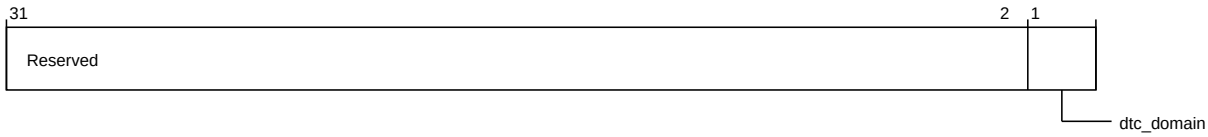
Table 5-724: por_mxp_por_dtm_unit_info_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-711: por_mxp_por_dtm_unit_info_dt$index (low)



The following table shows the por_dtm_unit_info_dt$index lower register bit assignments.

Table 5-725: por_mxp_por_dtm_unit_info_dt$index (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	dtc_domain	DTC domain number associated with this DTM	RO	Configuration dependent

5.3.6.14 por_mxp_p$index_info

This register repeats 3 times. It is parameterized by the $index from 2 to 5. Provides component identification information for XP port $index. NOTE: There will be max. of 6 MXP Port Info registers based on MXP_NUM_DEV_PORT_PARAM value. Each successive MXP Port Info register will be at the next 8 byte address boundary from P2 onwards. Each successive MXP Port Info register will be named with the suffix. For example por_mxp_p<2:5>_info

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_INFO_BASE + 16'h28 + (8 * ($index-2))
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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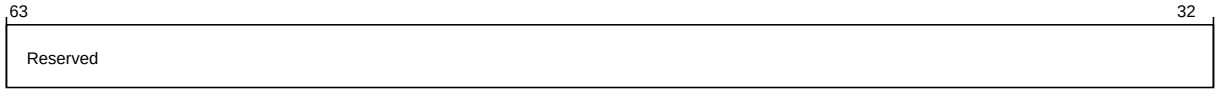
Figure 5-712: por_mxp_por_mxp_p$index_info (high)



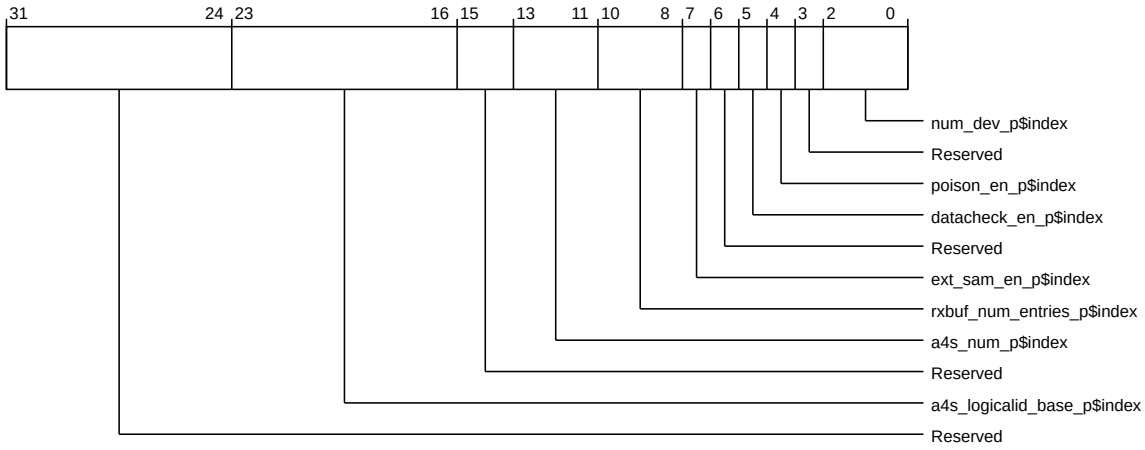
The following table shows the por_mxp_p$index_info higher register bit assignments.

Table 5-726: por_mxp_por_mxp_p$index_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-713: por_mxp_por_mxp_p$index_info (low)



The following table shows the por_mxp_p$index_info lower register bit assignments.

Table 5-727: por_mxp_por_mxp_p$index_info (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	a4s_logicalid_base_p$index	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p$index	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p$index	Number of input buffers at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p$index	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p$index	Datacheck enable	RO	Configuration dependent
4	poison_en_p$index	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	num_dev_p$index	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

5.3.6.15 por_mxp_secure_register_groups_override

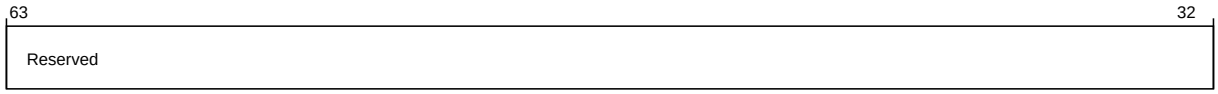
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-714: por_mxp_por_mxp_secure_register_groups_override (high)



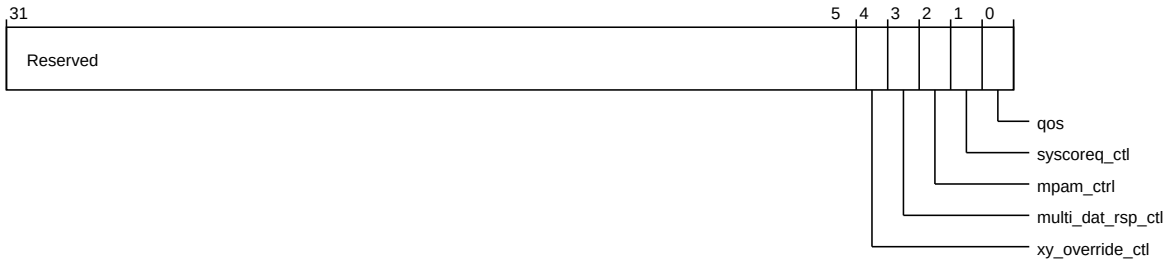
The following table shows the por_mxp_secure_register_groups_override higher register bit assignments.

Table 5-728: por_mxp_por_mxp_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-715: por_mxp_por_mxp_secure_register_groups_override (low)



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The following table shows the por_mxp_secure_register_groups_override lower register bit assignments.

Table 5-729: por_mxp_por_mxp_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	xy_override_ctl	Allows Non-secure access to Secure XY override registers	RW	1'b0
3	multi_dat_rsp_ctl	Allows Non-secure access to Secure Multi DAT and RSP control registers	RW	1'b0
2	mpam_ctrl	Allows Non-secure access to Secure CHI port MPAM override register	RW	1'b0
1	syscoreq_ctl	Allows Non-secure access to Secure syscoreq_ctl registers	RW	1'b0
0	qos	Allows Non-secure access to Secure QoS registers	RW	1'b0

5.3.6.16 por_mxp_aux_ctl

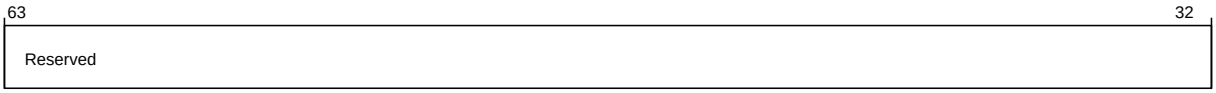
Functions as the auxiliary control register for XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-716: por_mxp_por_mxp_aux_ctl (high)



The following table shows the por_mxp_aux_ctl higher register bit assignments.

Table 5-730: por_mxp_por_mxp_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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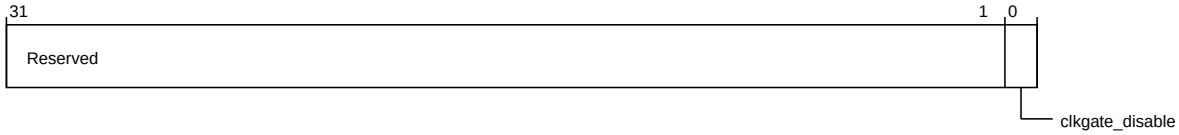
Figure 5-717: por_mxp_por_mxp_aux_ctl (low)



The following table shows the por_mxp_aux_ctl lower register bit assignments.

Table 5-731: por_mxp_por_mxp_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables clock gating when set	RW	1'b0

5.3.6.17 por_mxp_p$index_mpam_override

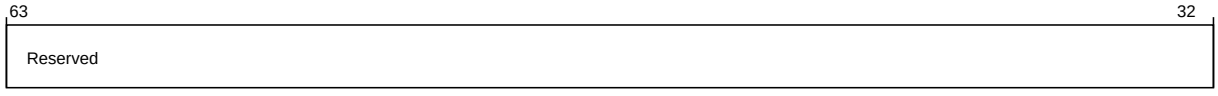
This register repeats 5 times. It is parameterized by the $index from 0 to 5. Controls MPAM fields for devices connected to port $index. Valid only if the devices doesn't support MPAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_CTRL_BASE + 16'h08 + (8 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-718: por_mxp_por_mxp_p$index_mpam_override (high)



The following table shows the por_mxp_p$index_mpam_override higher register bit assignments.

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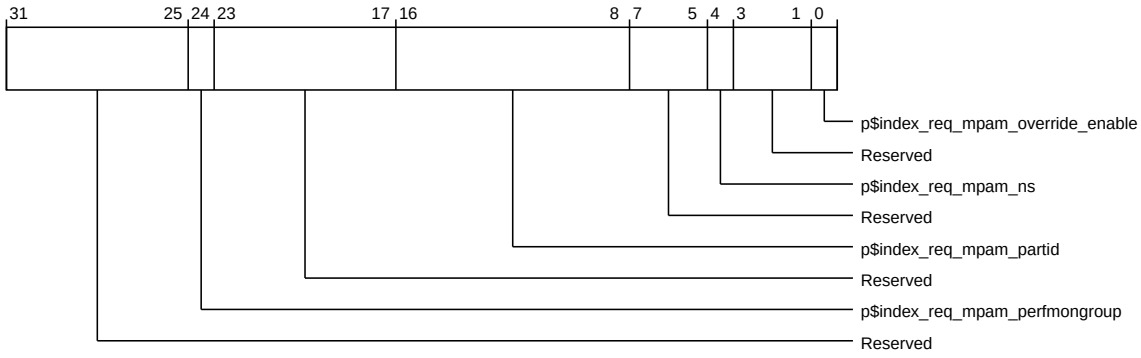
Table 5-732: por_mxp_por_mxp_p$index_mpam_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-719: por_mxp_por_mxp_p$index_mpam_override (low)



The following table shows the por_mxp_p$index_mpam_override lower register bit assignments.

Table 5-733: por_mxp_por_mxp_p$index_mpam_override (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	p$index_req_mpam_perfmongroup	MPAM.PerfMonGroup sub-field that overrides the REQ channel MPAM.PerfMonGroup when p$index_req_mpam_override_enable is set	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	p$index_req_mpam_partid	MPAM.PartID sub-field that overrides the REQ channel MPAM.PartID when p $index_req_mpam_override_enable is set	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	p$index_req_mpam_ns	MPAM.NS sub-field that overrides the REQ channel MPAM.NS when p $index_req_mpam_override_enable is set	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	p $index_req_mpam_override_enable	P$index DEV MPAM Override Enable on REQ Channel: 1 - Drive the MPAM fields on REQ channel with the values from this register, 0 - Override of MPAM fields in REQ channel is disabled	RW	1'b0

5.3.6.18 por_mxp_p$index_qos_control

This register repeats 5 times. It is parameterized by the $index from 0 to 5. Controls QoS settings for devices connected to port $index.

Its characteristics are:

Type RW

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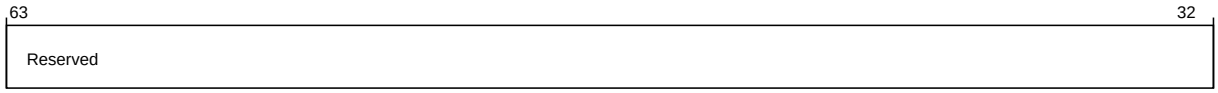
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h000 + (32 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

Figure 5-720: por_mxp_por_mxp_p$index_qos_control (high)



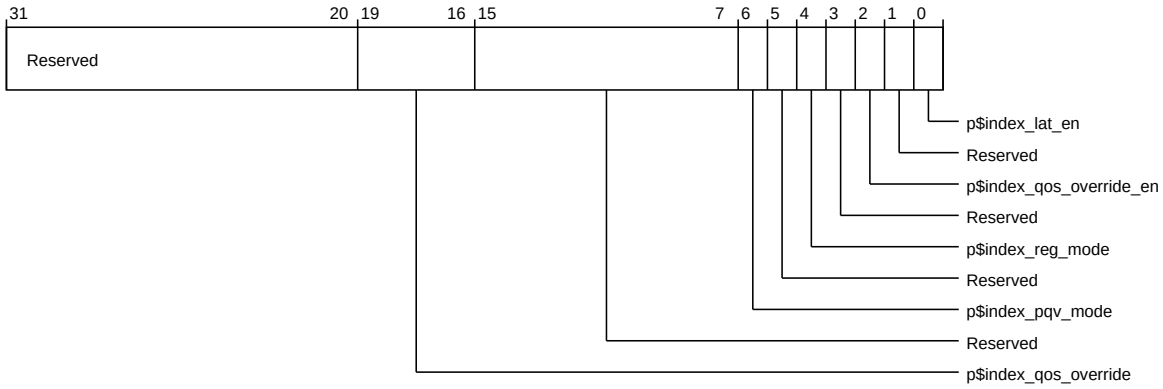
The following table shows the por_mxp_p$index_qos_control higher register bit assignments.

Table 5-734: por_mxp_por_mxp_p$index_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-721: por_mxp_por_mxp_p$index_qos_control (low)



The following table shows the por_mxp_p$index_qos_control lower register bit assignments.

Table 5-735: por_mxp_por_mxp_p$index_qos_control (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
19:16	p$index_qos_override	QoS override value for port $index	RW	4'b0000
15:7	Reserved	Reserved	RO	-
6	p$index_pqv_mode	Configures the QoS regulator mode during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	Reserved	Reserved	RO	-
4	p$index_reg_mode	Configures the QoS regulator mode 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	Reserved	Reserved	RO	-
2	p $index_qos_override_en	Enables port $index QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
1	Reserved	Reserved	RO	-
0	p$index_lat_en	Enables port $index QoS regulation when set	RW	1'b0

5.3.6.19 por_mxp_p$index_qos_lat_tgt

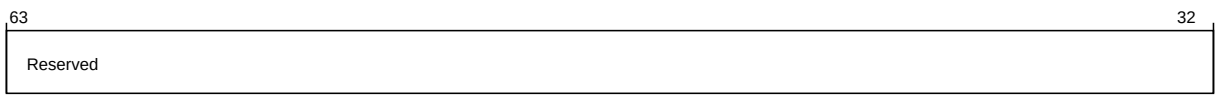
This register repeats 5 times. It is parameterized by the $index from 0 to 5. Controls QoS target latency/period (in cycles) for regulation of devices connected to port $index.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h008 + (32 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

Figure 5-722: por_mxp_por_mxp_p$index_qos_lat_tgt (high)



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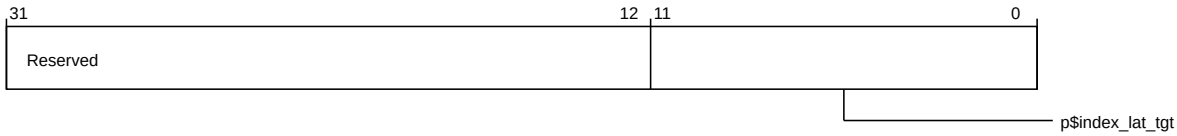
The following table shows the por_mxp_p$index_qos_lat_tgt higher register bit assignments.

Table 5-736: por_mxp_por_mxp_p$index_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-723: por_mxp_por_mxp_p$index_qos_lat_tgt (low)



The following table shows the por_mxp_p$index_qos_lat_tgt lower register bit assignments.

Table 5-737: por_mxp_por_mxp_p$index_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	p$index_lat_tgt	Port $index transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

5.3.6.20 por_mxp_p$index_qos_lat_scale

This register repeats 5 times. It is parameterized by the $index from 0 to 5. Controls the QoS target scale factor for devices connected to port $index. The scale factor is represented in powers of two from the range 2^(-3) to 2^(-10).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h010 + (32 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

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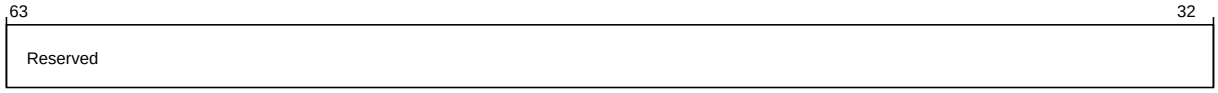
Figure 5-724: por_mxp_por_mxp_p$index_qos_lat_scale (high)



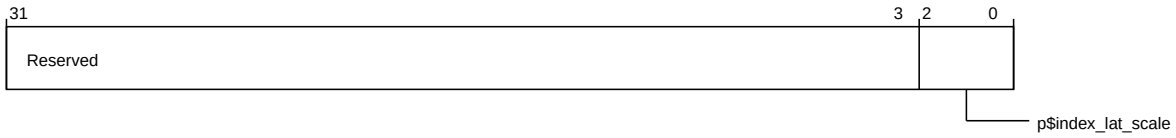
The following table shows the por_mxp_p$index_qos_lat_scale higher register bit assignments.

Table 5-738: por_mxp_por_mxp_p$index_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-725: por_mxp_por_mxp_p$index_qos_lat_scale (low)



The following table shows the por_mxp_p$index_qos_lat_scale lower register bit assignments.

Table 5-739: por_mxp_por_mxp_p$index_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	p$index_lat_scale	Port 0 QoS scale factor 3'b000: 2^(-3) 3'b001: 2^(-4) 3'b010: 2^(-5) 3'b011: 2^(-6) 3'b100: 2^(-7) 3'b101: 2^(-8) 3'b110: 2^(-9) 3'b111: 2^(-10)	RW	3'h0

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5.3.6.21 por_mxp_p$index_qos_lat_range

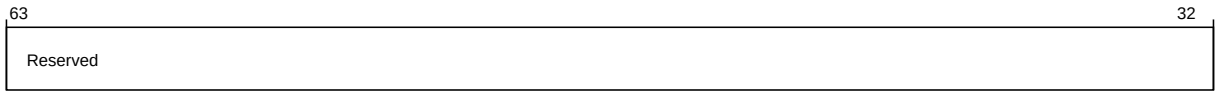
This register repeats 5 times. It is parameterized by the $index from 0 to 5. Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port $index.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_QOS_BASE + 16'h018 + (32 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.qos

The following figure shows the higher register bit assignments.

Figure 5-726: por_mxp_por_mxp_p$index_qos_lat_range (high)



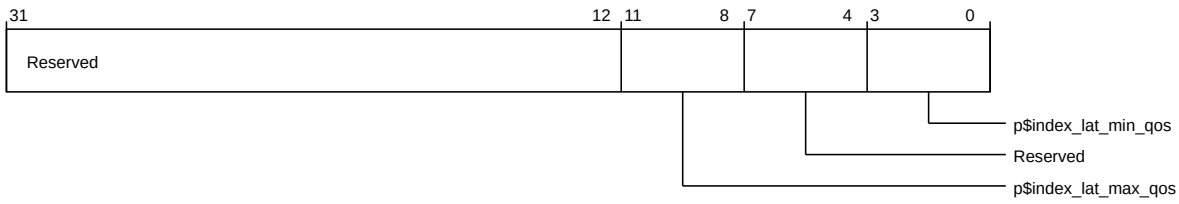
The following table shows the por_mxp_p$index_qos_lat_range higher register bit assignments.

Table 5-740: por_mxp_por_mxp_p$index_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-727: por_mxp_por_mxp_p$index_qos_lat_range (low)



The following table shows the por_mxp_p$index_qos_lat_range lower register bit assignments.

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Table 5-741: por_mxp_por_mxp_p$index_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	p$index_lat_max_qos	Port $index QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	p$index_lat_min_qos	Port $index QoS minimum value	RW	4'h0

5.3.6.22 por_mxp_pmu_event_sel

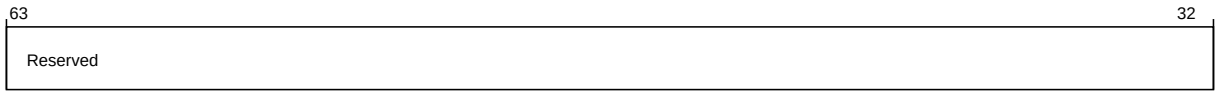
Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-728: por_mxp_por_mxp_pmu_event_sel (high)



The following table shows the por_mxp_pmu_event_sel higher register bit assignments.

Table 5-742: por_mxp_por_mxp_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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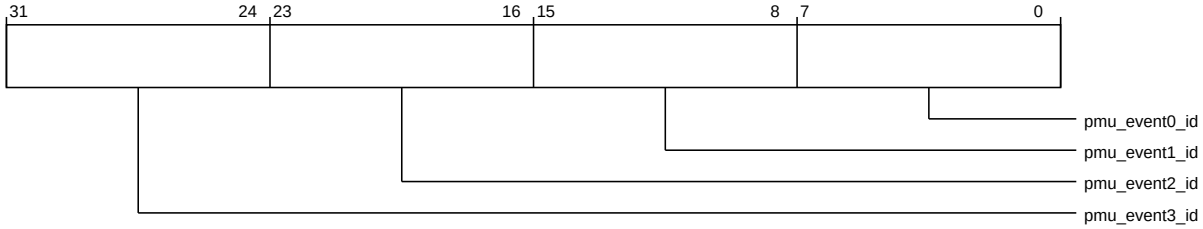
Figure 5-729: por_mxp_por_mxp_pmu_event_sel (low)



The following table shows the por_mxp_pmu_event_sel lower register bit assignments.

Table 5-743: por_mxp_por_mxp_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:24	pmu_event3_id	XP PMU Event 3 ID; see pmu_event0_id for encodings	RW	8'b0
23:16	pmu_event2_id	XP PMU Event 2 ID; see pmu_event0_id for encodings	RW	8'b0
15:8	pmu_event1_id	XP PMU Event 1 ID; see pmu_event0_id for encodings	RW	8'b0

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Bits	Field name	Description	Type	Reset
7:0	pmu_event0_id	XP PMU Event 0 ID Bits [7:5]: PC 3'b000: REQ 3'b001: RSP; RSP channel when POR_RSP_VC_NUM_PARAM = 1 ; RSP Sub-channel 1: when POR_RSP_VC_NUM_PARAM > 1 3'b010: SNP 3'b011: DAT; DAT channel when POR_DAT_VC_NUM_PARAM = 1 ; DAT Sub-channel 1: when POR_DAT_VC_NUM_PARAM > 1 3'b100: PUB 3'b101: RSP2; RSP Sub-channel 2: Applicable when POR_RSP_VC_NUM_PARAM > 1 3'b110: DAT2; DAT Sub-channel 2: Applicable when POR_DAT_VC_NUM_PARAM > 1 Bits [4:2]: Interface 3'b000: East when NUM_XP > 1 ; Device port 0 when NUM_XP == 1 (Single XP config) 3'b001: West when NUM_XP > 1 ; Device port 1 when NUM_XP == 1 (Single XP config) 3'b010: North when NUM_XP > 1 ; Device port 2 when NUM_XP == 1 (Single XP config) 3'b011: South when NUM_XP > 1 ; Device port 3 when NUM_XP == 1 (Single XP config) 3'b100: Device port 0 when NUM_XP > 1 ; Device port 4 when NUM_XP == 1 (Single XP config) 3'b101: Device port 1 when NUM_XP > 1 ; Device port 5 when NUM_XP == 1 (Single XP config) 3'b110: Device port 2 when NUM_XP > 1 ; No Selection when NUM_XP == 1 (Single XP config) 3'b111: Device port 3 when NUM_XP > 1 ; No Selection when NUM_XP == 1 (Single XP config) Bits [1:0]: Event specifier 2'b00: No event 2'b01: TX flit valid; signaled when a flit is successfully transmitted 2'b10: TX flit stall; signaled when flit transmission is stalled and waiting on credits 2'b11: Partial DAT flit; signaled when 128-bit DAT flits could not be merged into a 256-bit DAT flit; only applicable on the DAT PC on RN-F CHIA and RN-F CHIA ESAM ports	RW	8'b0

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5.3.6.23 por_mxp_errfr

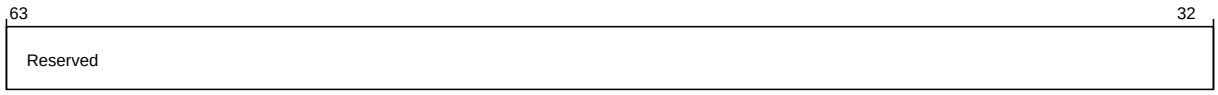
Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3000
Register reset 64'b0000010100101
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-730: por_mxp_por_mxp_errfr (high)



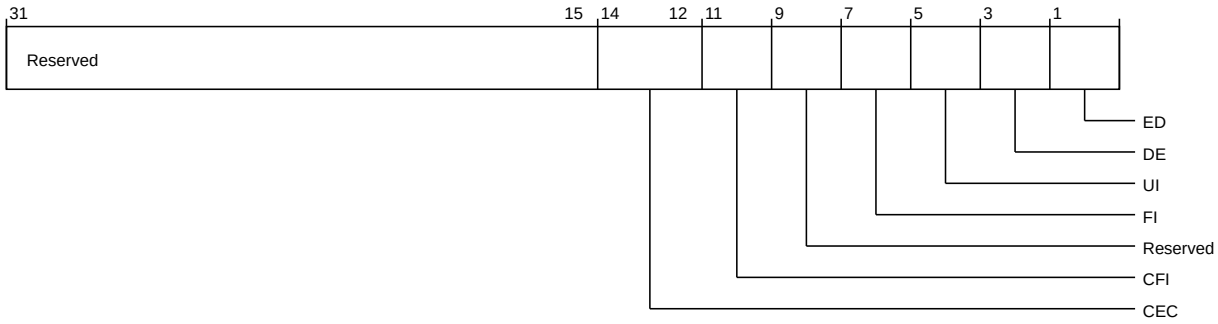
The following table shows the por_mxp_errfr higher register bit assignments.

Table 5-744: por_mxp_por_mxp_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-731: por_mxp_por_mxp_errfr (low)



The following table shows the por_mxp_errfr lower register bit assignments.

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Table 5-745: por_mxp_por_mxp_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

5.3.6.24 por_mxp_errctlr

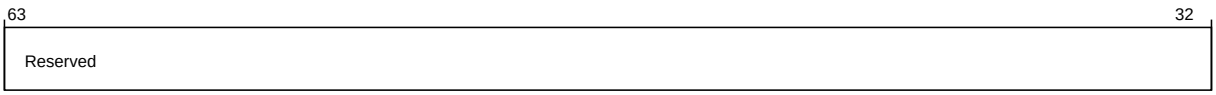
Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-732: por_mxp_por_mxp_errctlr (high)



The following table shows the por_mxp_errctlr higher register bit assignments.

Table 5-746: por_mxp_por_mxp_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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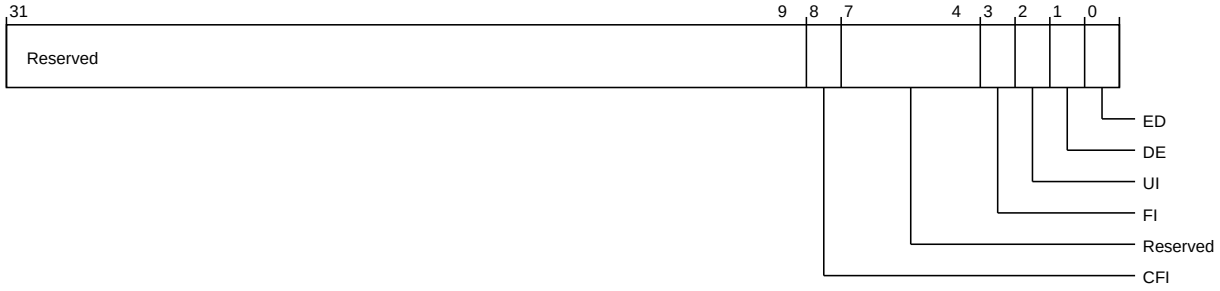
Figure 5-733: por_mxp_por_mxp_errctlr (low)



The following table shows the por_mxp_errctlr lower register bit assignments.

Table 5-747: por_mxp_por_mxp_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mxp_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mxp_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mxp_errfr.ED	RW	1'b0

5.3.6.25 por_mxp_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

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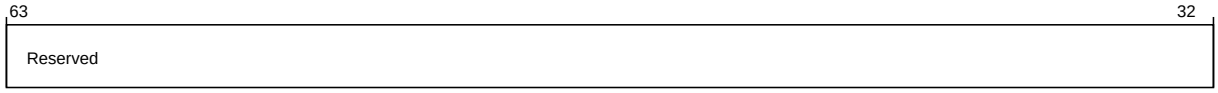
Figure 5-734: por_mxp_por_mxp_errstatus (high)



The following table shows the por_mxp_errstatus higher register bit assignments.

Table 5-748: por_mxp_por_mxp_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-735: por_mxp_por_mxp_errstatus (low)



The following table shows the por_mxp_errstatus lower register bit assignments.

Table 5-749: por_mxp_por_mxp_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0

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Bits	Field name	Description	Type	Reset
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mxp_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.6.26 por_mxp_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3028
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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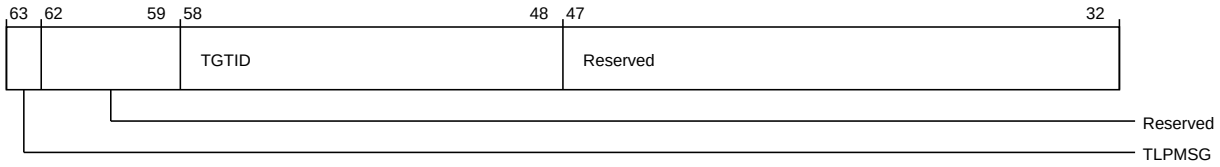
The following figure shows the higher register bit assignments.

Figure 5-736: por_mxp_por_mxp_errmisc (high)



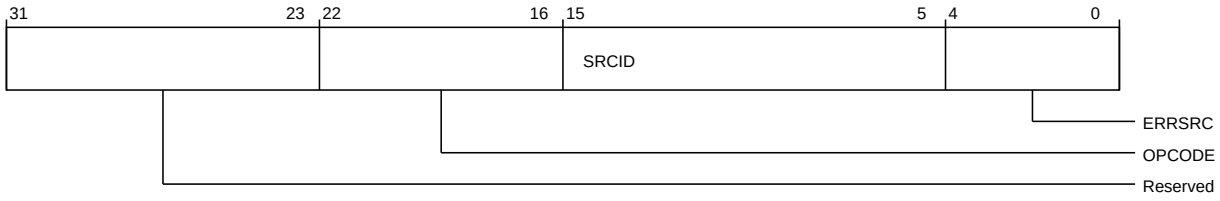
The following table shows the por_mxp_errmisc higher register bit assignments.

Table 5-750: por_mxp_por_mxp_errmisc (high)

Bits	Field name	Description	Type	Reset
63	TLPMSG	Error flit TLPMSG Status	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-737: por_mxp_por_mxp_errmisc (low)



The following table shows the por_mxp_errmisc lower register bit assignments.

Table 5-751: por_mxp_por_mxp_errmisc (low)

Bits	Field name	Description	Type	Reset
31:23	Reserved	Reserved	RO	-
22:16	OPCODE	Error flit opcode	RW	7'b0
15:5	SRCID	Error flit source ID	RW	11'b0

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Bits	Field name	Description	Type	Reset
4:0	ERRSRC	Error source Bits [4:3]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bits [2:0]: Port 3'b000: Port 0 3'b001: Port 1 3'b010: Port 2 3'b011: Port 3 3'b100: Port 4 3'b101: Port 5	RW	5'b0

5.3.6.27 por_mxp_p$index_byte_par_err_inj

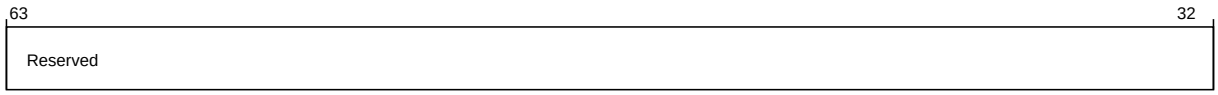
This register repeats 5 times. It is parameterized by the $index from 0 to 5. Functions as the byte parity error injection register for XP port $index.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_S_ERROR_BASE + 16'h030 + (8 * $index)
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-738: por_mxp_por_mxp_p$index_byte_par_err_inj (high)



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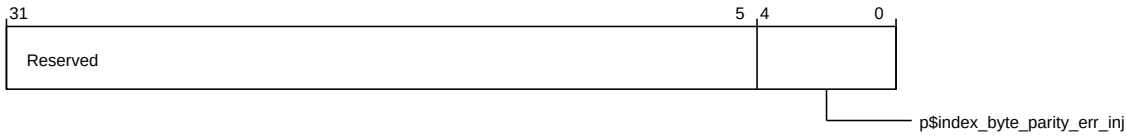
The following table shows the por_mxp_p$index_byte_par_err_inj higher register bit assignments.

Table 5-752: por_mxp_por_mxp_p$index_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-739: por_mxp_por_mxp_p$index_byte_par_err_inj (low)



The following table shows the por_mxp_p$index_byte_par_err_inj lower register bit assignments.

Table 5-753: por_mxp_por_mxp_p$index_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	p$index_byte_parity_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port $index. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

5.3.6.28 por_mxp_errfr_NS

Functions as the Non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b0000010100101
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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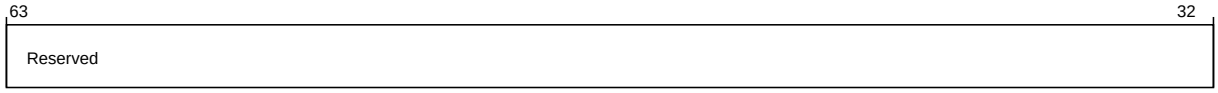
Figure 5-740: por_mxp_por_mxp_errfr_ns (high)



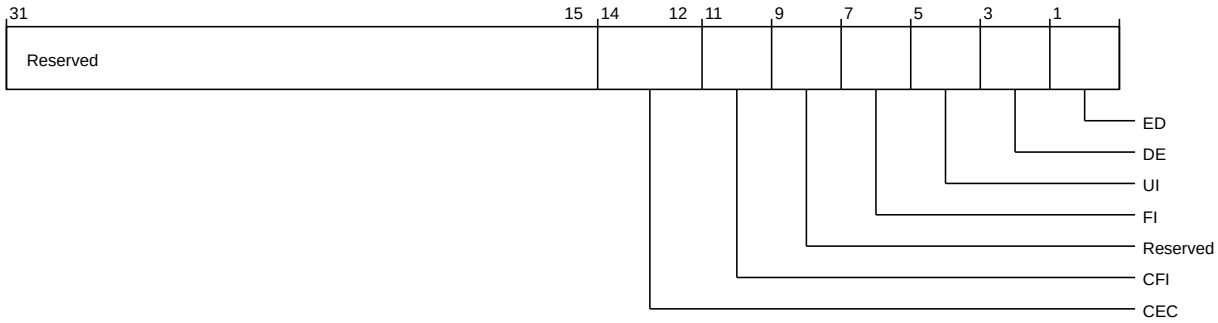
The following table shows the por_mxp_errfr_NS higher register bit assignments.

Table 5-754: por_mxp_por_mxp_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-741: por_mxp_por_mxp_errfr_ns (low)



The following table shows the por_mxp_errfr_NS lower register bit assignments.

Table 5-755: por_mxp_por_mxp_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

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5.3.6.29 por_mxp_errctlr_NS

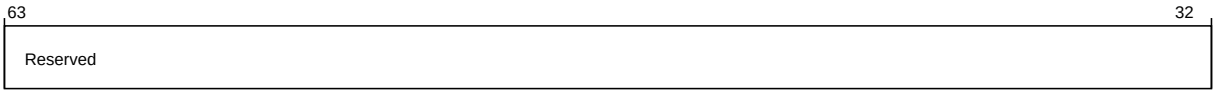
Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-742: por_mxp_por_mxp_errctlr_ns (high)



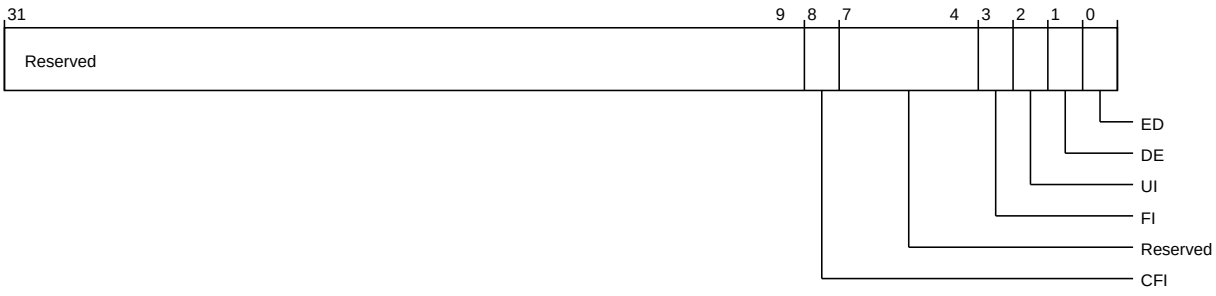
The following table shows the por_mxp_errctlr_NS higher register bit assignments.

Table 5-756: por_mxp_por_mxp_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-743: por_mxp_por_mxp_errctlr_ns (low)



The following table shows the por_mxp_errctlr_NS lower register bit assignments.

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Table 5-757: por_mxp_por_mxp_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mxp_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mxp_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mxp_errfr_NS.ED	RW	1'b0

5.3.6.30 por_mxp_errstatus_NS

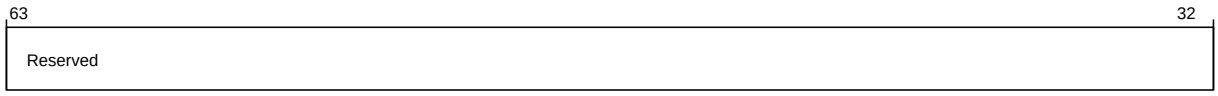
Functions as the Non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-744: por_mxp_por_mxp_errstatus_ns (high)



The following table shows the por_mxp_errstatus_NS higher register bit assignments.

Table 5-758: por_mxp_por_mxp_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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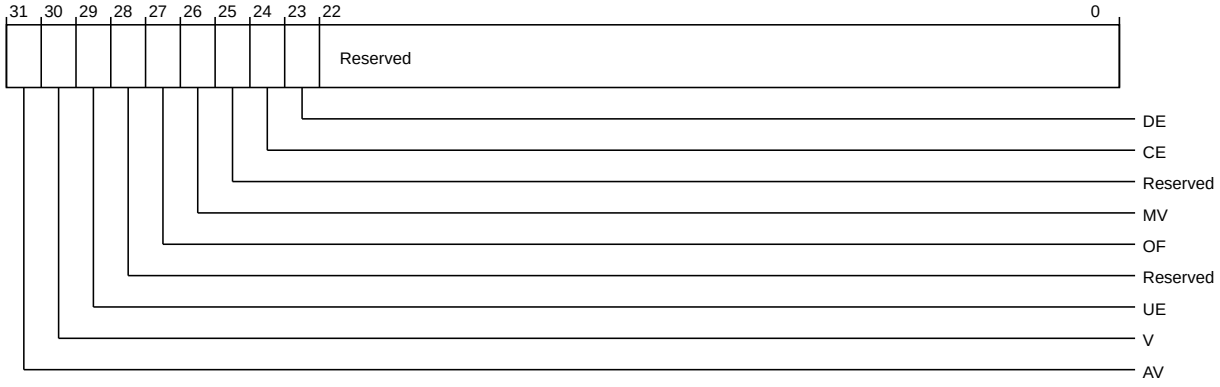
Figure 5-745: por_mxp_por_mxp_errstatus_ns (low)



The following table shows the por_mxp_errstatus_NS lower register bit assignments.

Table 5-759: por_mxp_por_mxp_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mxp_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0

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Bits	Field name	Description	Type	Reset
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.6.31 por_mxp_errmisc_NS

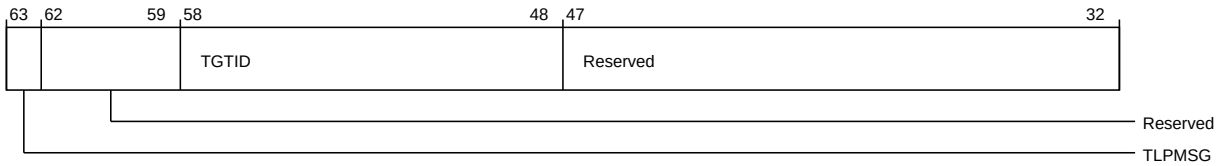
Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-746: por_mxp_por_mxp_errmisc_ns (high)



The following table shows the por_mxp_errmisc_NS higher register bit assignments.

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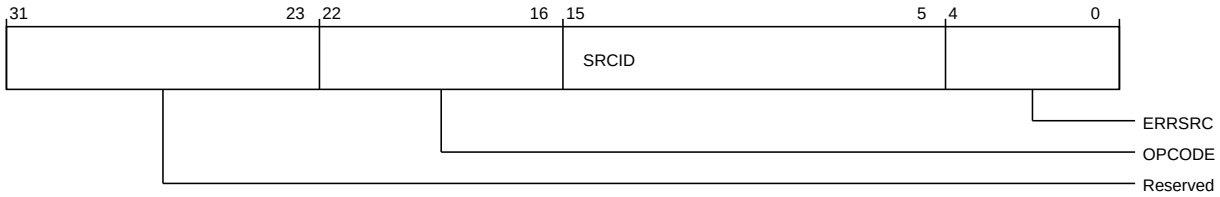
Table 5-760: por_mxp_por_mxp_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63	TLPMSG	Error flit TLPMSG Status	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-747: por_mxp_por_mxp_errmisc_ns (low)



The following table shows the por_mxp_errmisc_NS lower register bit assignments.

Table 5-761: por_mxp_por_mxp_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:23	Reserved	Reserved	RO	-
22:16	OPCODE	Error flit opcode	RW	7'b0
15:5	SRCID	Error flit source ID	RW	11'b0

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Bits	Field name	Description	Type	Reset
4:0	ERRSRC	Error source Bits [4:3]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bits [2:0]: Port 3'b000: Port 0 3'b001: Port 1 3'b010: Port 2 3'b011: Port 3 3'b100: Port 4 3'b101: Port 5	RW	5'b0

5.3.6.32 por_mxp_p$index_syscoreq_ctl

This register repeats twice. It is parameterized by the $index from 0 to 1. Functions as the port $index snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p$index_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h0 + (8 * ($index))
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.syscoreq_ctl

The following figure shows the higher register bit assignments.

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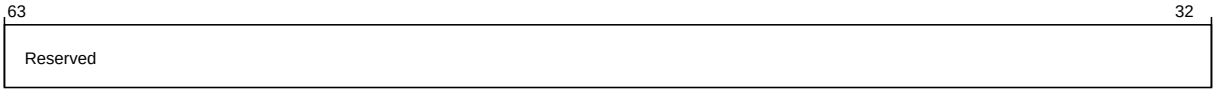
Figure 5-748: por_mxp_por_mxp_p$index_syscoreq_ctl (high)



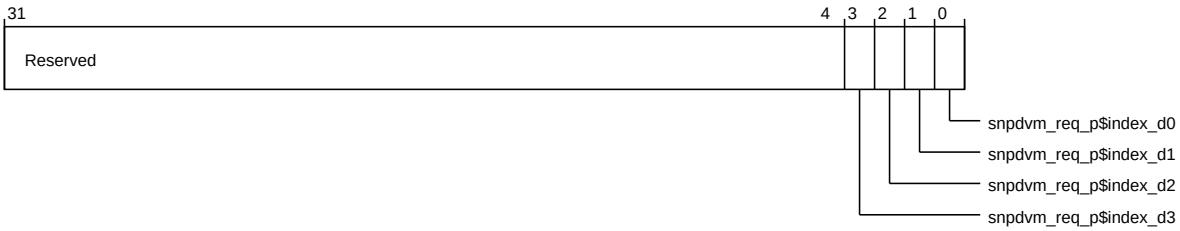
The following table shows the por_mxp_p$index_syscoreq_ctl higher register bit assignments.

Table 5-762: por_mxp_por_mxp_p$index_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-749: por_mxp_por_mxp_p$index_syscoreq_ctl (low)



The following table shows the por_mxp_p$index_syscoreq_ctl lower register bit assignments.

Table 5-763: por_mxp_por_mxp_p$index_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p $index_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port $index	RW	1'b0
2	snpdvm_req_p $index_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port $index	RW	1'b0
1	snpdvm_req_p $index_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port $index	RW	1'b0
0	snpdvm_req_p $index_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port $index	RW	1'b0

5.3.6.33 por_mxp_p$index_syscoack_status

This register repeats twice. It is parameterized by the $index from 0 to 1. Functions as the port $index snoop and DVM domain status register. Provides a software alternative to hardware

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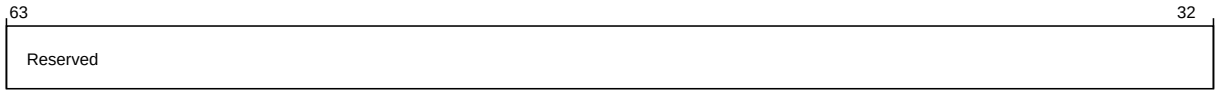
SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p$index_syscoreq_ctl. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h10 + (8 * ($index))
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.syscoreq_ctl

The following figure shows the higher register bit assignments.

Figure 5-750: por_mxp_por_mxp_p$index_syscoack_status (high)



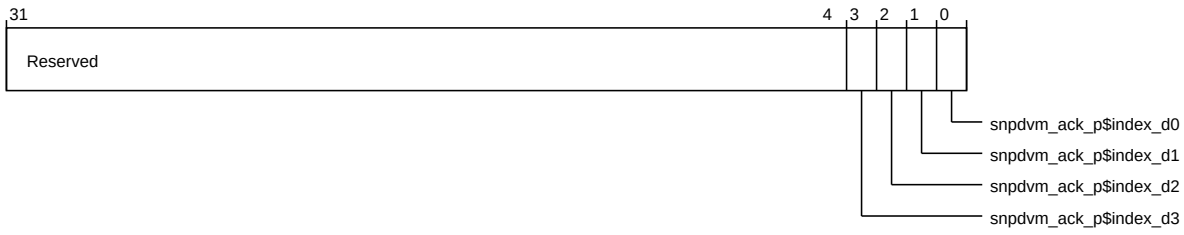
The following table shows the por_mxp_p$index_syscoack_status higher register bit assignments.

Table 5-764: por_mxp_por_mxp_p$index_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-751: por_mxp_por_mxp_p$index_syscoack_status (low)



The following table shows the por_mxp_p$index_syscoack_status lower register bit assignments.

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Table 5-765: por_mxp_por_mxp_p$index_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_ack_p $index_d3	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port $index	RO	1'b0
2	snpdvm_ack_p $index_d2	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port $index	RO	1'b0
1	snpdvm_ack_p $index_d1	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port $index	RO	1'b0
0	snpdvm_ack_p $index_d0	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port $index	RO	1'b0

5.3.6.34 por_mxp_p$index_syscoreq_ctl

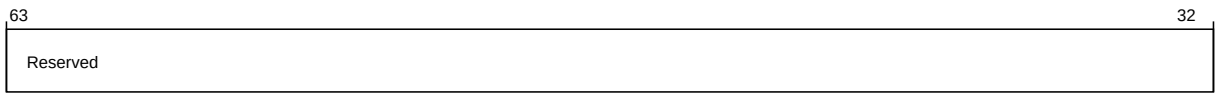
This register repeats 3 times. It is parameterized by the $index from 2 to 5. Functions as the port $index snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p$index_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h20 + (8 * ($index-2))
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.syscoreq_ctl

The following figure shows the higher register bit assignments.

Figure 5-752: por_mxp_por_mxp_p$index_syscoreq_ctl (high)



The following table shows the por_mxp_p$index_syscoreq_ctl higher register bit assignments.

Table 5-766: por_mxp_por_mxp_p$index_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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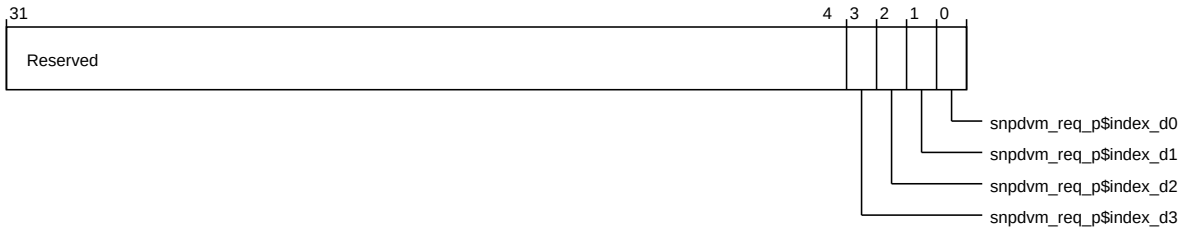
The following figure shows the lower register bit assignments.

Figure 5-753: por_mxp_por_mxp_p$index_syscoreq_ctl (low)



The following table shows the por_mxp_p$index_syscoreq_ctl lower register bit assignments.

Table 5-767: por_mxp_por_mxp_p$index_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p $index_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port $index	RW	1'b0
2	snpdvm_req_p $index_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port $index	RW	1'b0
1	snpdvm_req_p $index_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port $index	RW	1'b0
0	snpdvm_req_p $index_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port $index	RW	1'b0

5.3.6.35 por_mxp_p$index_syscoack_status

This register repeats 3 times. It is parameterized by the $index from 2 to 5. Functions as the port $index snoop and DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p$index_syscoreq_ctl. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_POWER_BASE + 16'h40 + (8 * ($index-2))
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mxp_secure_register_groups_override.syscoreq_ctl

The following figure shows the higher register bit assignments.

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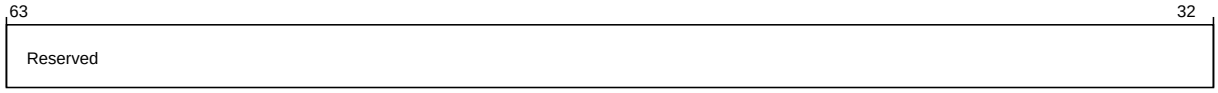
Figure 5-754: por_mxp_por_mxp_p$index_syscoack_status (high)



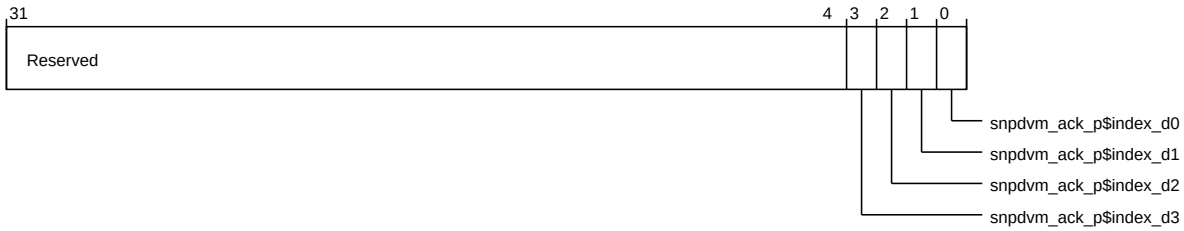
The following table shows the por_mxp_p$index_syscoack_status higher register bit assignments.

Table 5-768: por_mxp_por_mxp_p$index_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-755: por_mxp_por_mxp_p$index_syscoack_status (low)



The following table shows the por_mxp_p$index_syscoack_status lower register bit assignments.

Table 5-769: por_mxp_por_mxp_p$index_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_ack_p $index_d3	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port $index	RO	1'b0
2	snpdvm_ack_p $index_d2	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port $index	RO	1'b0
1	snpdvm_ack_p $index_d1	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port $index	RO	1'b0
0	snpdvm_ack_p $index_d0	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port $index	RO	1'b0

5.3.6.36 por_dtm_control

Functions as the DTM control register.

Its characteristics are:

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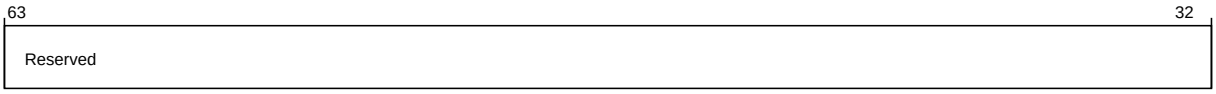
Type RW
Register width (Bits) 64
Address offset 16'h2100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-756: por_mxp_por_dtm_control (high)



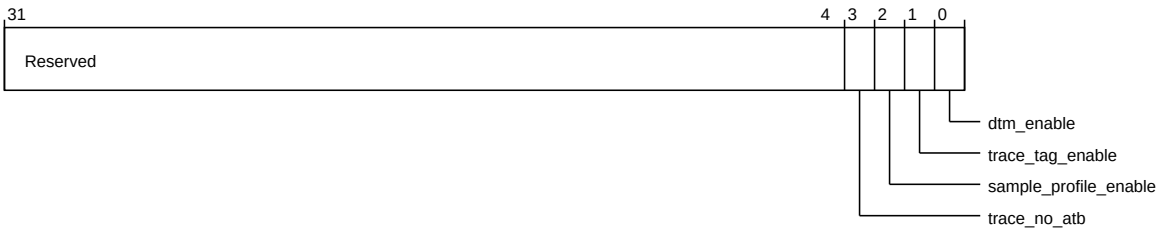
The following table shows the por_dtm_control higher register bit assignments.

Table 5-770: por_mxp_por_dtm_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-757: por_mxp_por_dtm_control (low)



The following table shows the por_dtm_control lower register bit assignments.

Table 5-771: por_mxp_por_dtm_control (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet	RW	1'b0
2	sample_profile_enable	Enables sample profile function	RW	1'b0

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Bits	Field name	Description	Type	Reset
1	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
0	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

5.3.6.37 por_dtm_fifo_entry_ready

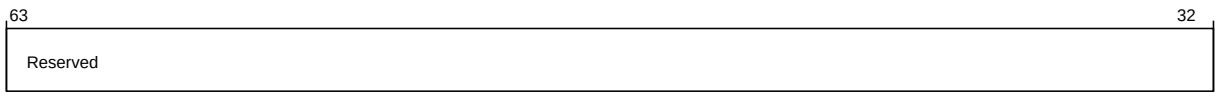
Controls status of DTM FIFO entries.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h2118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-758: por_mxp_por_dtm_fifo_entry_ready (high)



The following table shows the por_dtm_fifo_entry_ready higher register bit assignments.

Table 5-772: por_mxp_por_dtm_fifo_entry_ready (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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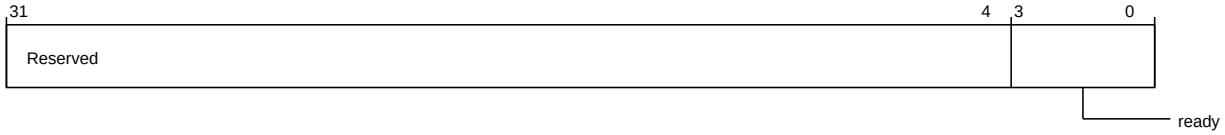
Figure 5-759: por_mxp_por_dtm_fifo_entry_ready (low)



The following table shows the por_dtm_fifo_entry_ready lower register bit assignments.

Table 5-773: por_mxp_por_dtm_fifo_entry_ready (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

5.3.6.38 por_dtm_fifo_entry0_0

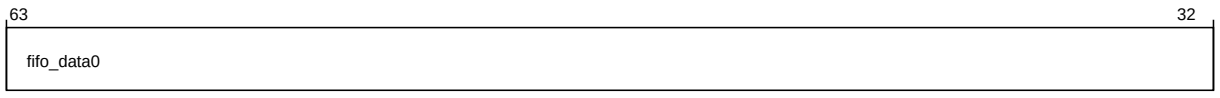
Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-760: por_mxp_por_dtm_fifo_entry0_0 (high)



The following table shows the por_dtm_fifo_entry0_0 higher register bit assignments.

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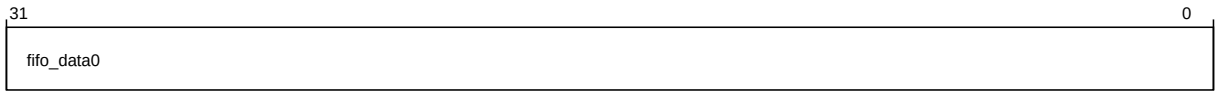
Table 5-774: por_mxp_por_dtm_fifo_entry0_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-761: por_mxp_por_dtm_fifo_entry0_0 (low)



The following table shows the por_dtm_fifo_entry0_0 lower register bit assignments.

Table 5-775: por_mxp_por_dtm_fifo_entry0_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.39 por_dtm_fifo_entry0_1

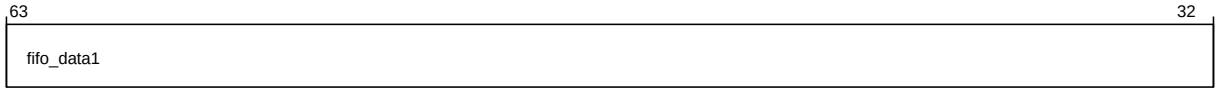
Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-762: por_mxp_por_dtm_fifo_entry0_1 (high)



The following table shows the por_dtm_fifo_entry0_1 higher register bit assignments.

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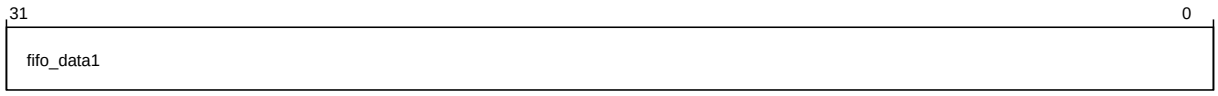
Table 5-776: por_mxp_por_dtm_fifo_entry0_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-763: por_mxp_por_dtm_fifo_entry0_1 (low)



The following table shows the por_dtm_fifo_entry0_1 lower register bit assignments.

Table 5-777: por_mxp_por_dtm_fifo_entry0_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.40 por_dtm_fifo_entry0_2

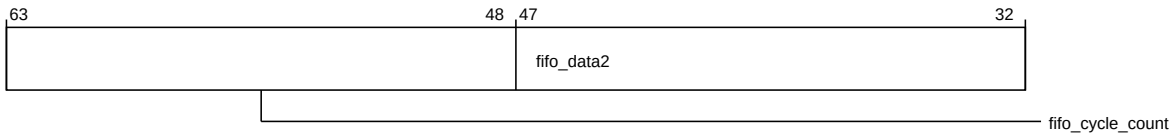
Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2130
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-764: por_mxp_por_dtm_fifo_entry0_2 (high)



The following table shows the por_dtm_fifo_entry0_2 higher register bit assignments.

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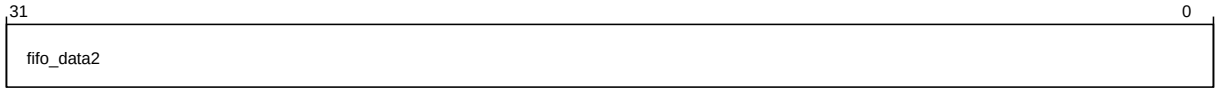
Table 5-778: por_mxp_por_dtm_fifo_entry0_2 (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-765: por_mxp_por_dtm_fifo_entry0_2 (low)



The following table shows the por_dtm_fifo_entry0_2 lower register bit assignments.

Table 5-779: por_mxp_por_dtm_fifo_entry0_2 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.41 por_dtm_fifo_entry1_0

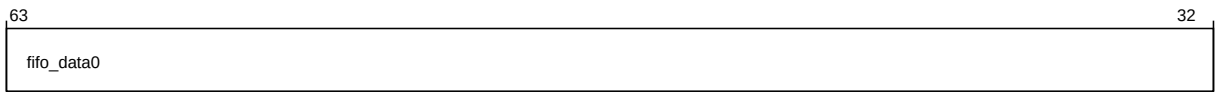
Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2138
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-766: por_mxp_por_dtm_fifo_entry1_0 (high)



The following table shows the por_dtm_fifo_entry1_0 higher register bit assignments.

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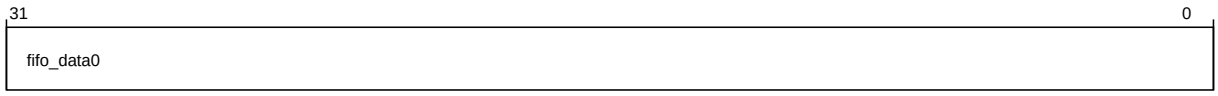
Table 5-780: por_mxp_por_dtm_fifo_entry1_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-767: por_mxp_por_dtm_fifo_entry1_0 (low)



The following table shows the por_dtm_fifo_entry1_0 lower register bit assignments.

Table 5-781: por_mxp_por_dtm_fifo_entry1_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.42 por_dtm_fifo_entry1_1

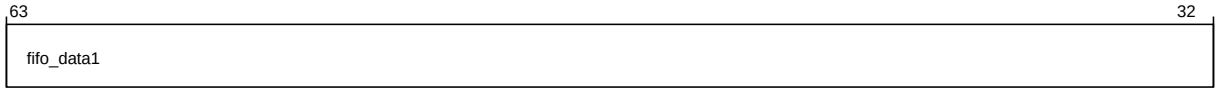
Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2140
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-768: por_mxp_por_dtm_fifo_entry1_1 (high)



The following table shows the por_dtm_fifo_entry1_1 higher register bit assignments.

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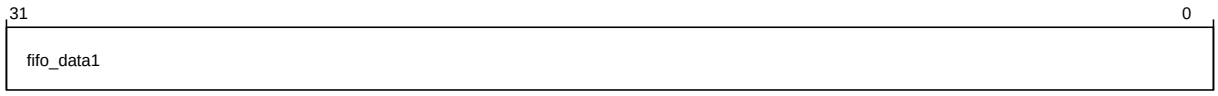
Table 5-782: por_mxp_por_dtm_fifo_entry1_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-769: por_mxp_por_dtm_fifo_entry1_1 (low)



The following table shows the por_dtm_fifo_entry1_1 lower register bit assignments.

Table 5-783: por_mxp_por_dtm_fifo_entry1_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.43 por_dtm_fifo_entry1_2

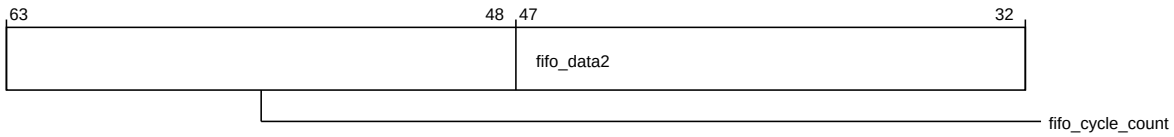
Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2148
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-770: por_mxp_por_dtm_fifo_entry1_2 (high)



The following table shows the por_dtm_fifo_entry1_2 higher register bit assignments.

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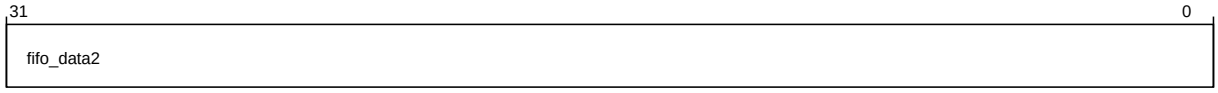
Table 5-784: por_mxp_por_dtm_fifo_entry1_2 (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-771: por_mxp_por_dtm_fifo_entry1_2 (low)



The following table shows the por_dtm_fifo_entry1_2 lower register bit assignments.

Table 5-785: por_mxp_por_dtm_fifo_entry1_2 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.44 por_dtm_fifo_entry2_0

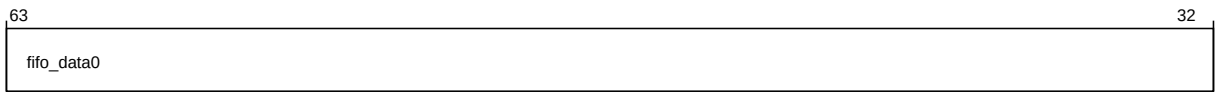
Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2150
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-772: por_mxp_por_dtm_fifo_entry2_0 (high)



The following table shows the por_dtm_fifo_entry2_0 higher register bit assignments.

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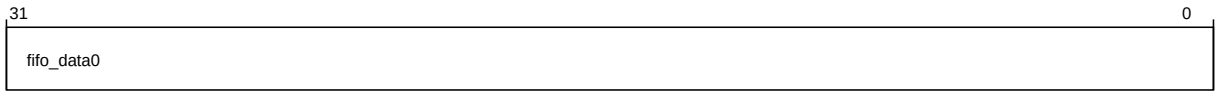
Table 5-786: por_mxp_por_dtm_fifo_entry2_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-773: por_mxp_por_dtm_fifo_entry2_0 (low)



The following table shows the por_dtm_fifo_entry2_0 lower register bit assignments.

Table 5-787: por_mxp_por_dtm_fifo_entry2_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.45 por_dtm_fifo_entry2_1

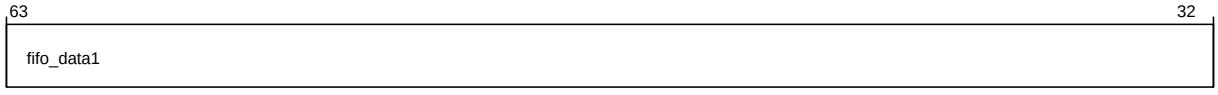
Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2158
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-774: por_mxp_por_dtm_fifo_entry2_1 (high)



The following table shows the por_dtm_fifo_entry2_1 higher register bit assignments.

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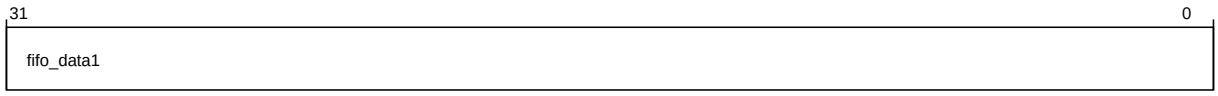
Table 5-788: por_mxp_por_dtm_fifo_entry2_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-775: por_mxp_por_dtm_fifo_entry2_1 (low)



The following table shows the por_dtm_fifo_entry2_1 lower register bit assignments.

Table 5-789: por_mxp_por_dtm_fifo_entry2_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.46 por_dtm_fifo_entry2_2

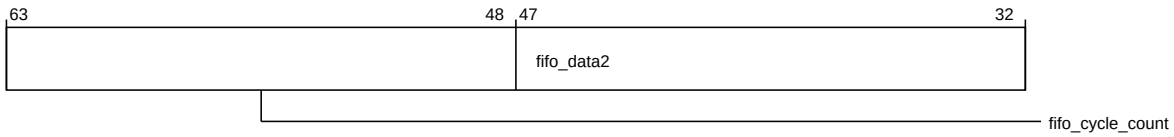
Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2160
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-776: por_mxp_por_dtm_fifo_entry2_2 (high)



The following table shows the por_dtm_fifo_entry2_2 higher register bit assignments.

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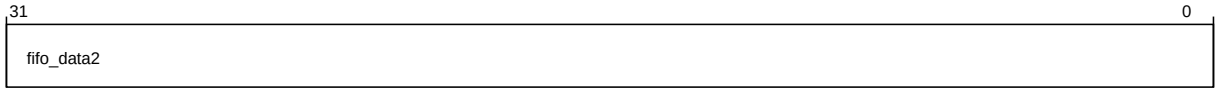
Table 5-790: por_mxp_por_dtm_fifo_entry2_2 (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-777: por_mxp_por_dtm_fifo_entry2_2 (low)



The following table shows the por_dtm_fifo_entry2_2 lower register bit assignments.

Table 5-791: por_mxp_por_dtm_fifo_entry2_2 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.47 por_dtm_fifo_entry3_0

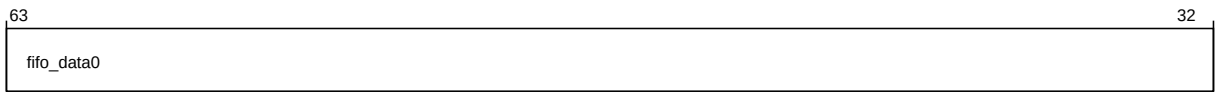
Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2168
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-778: por_mxp_por_dtm_fifo_entry3_0 (high)



The following table shows the por_dtm_fifo_entry3_0 higher register bit assignments.

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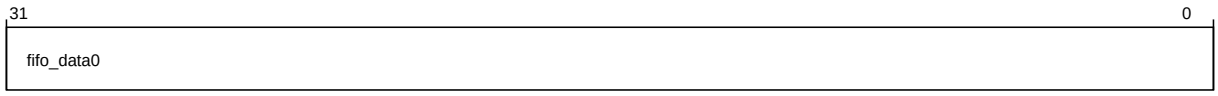
Table 5-792: por_mxp_por_dtm_fifo_entry3_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-779: por_mxp_por_dtm_fifo_entry3_0 (low)



The following table shows the por_dtm_fifo_entry3_0 lower register bit assignments.

Table 5-793: por_mxp_por_dtm_fifo_entry3_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.48 por_dtm_fifo_entry3_1

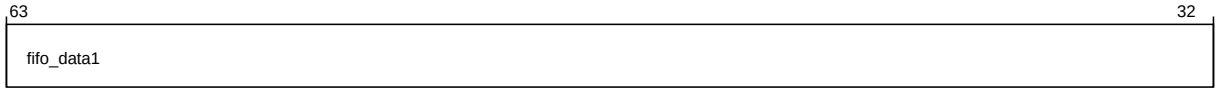
Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2170
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-780: por_mxp_por_dtm_fifo_entry3_1 (high)



The following table shows the por_dtm_fifo_entry3_1 higher register bit assignments.

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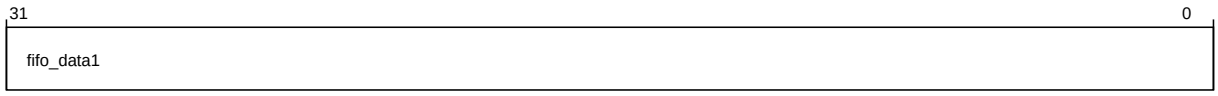
Table 5-794: por_mxp_por_dtm_fifo_entry3_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-781: por_mxp_por_dtm_fifo_entry3_1 (low)



The following table shows the por_dtm_fifo_entry3_1 lower register bit assignments.

Table 5-795: por_mxp_por_dtm_fifo_entry3_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.49 por_dtm_fifo_entry3_2

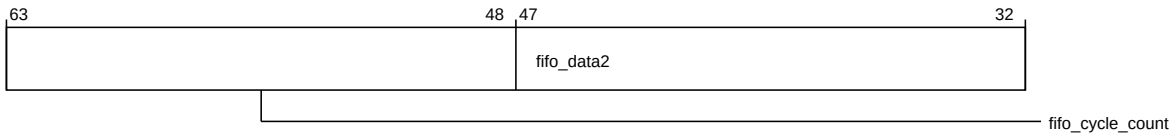
Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h2178
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-782: por_mxp_por_dtm_fifo_entry3_2 (high)



The following table shows the por_dtm_fifo_entry3_2 higher register bit assignments.

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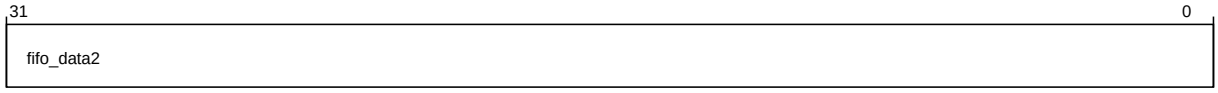
Table 5-796: por_mxp_por_dtm_fifo_entry3_2 (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-783: por_mxp_por_dtm_fifo_entry3_2 (low)



The following table shows the por_dtm_fifo_entry3_2 lower register bit assignments.

Table 5-797: por_mxp_por_dtm_fifo_entry3_2 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.50 por_dtm_wp0_config

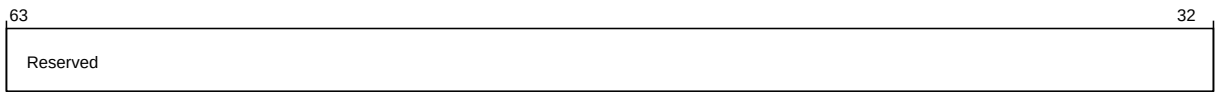
Configures watchpoint 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21A0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-784: por_mxp_por_dtm_wp0_config (high)



The following table shows the por_dtm_wp0_config higher register bit assignments.

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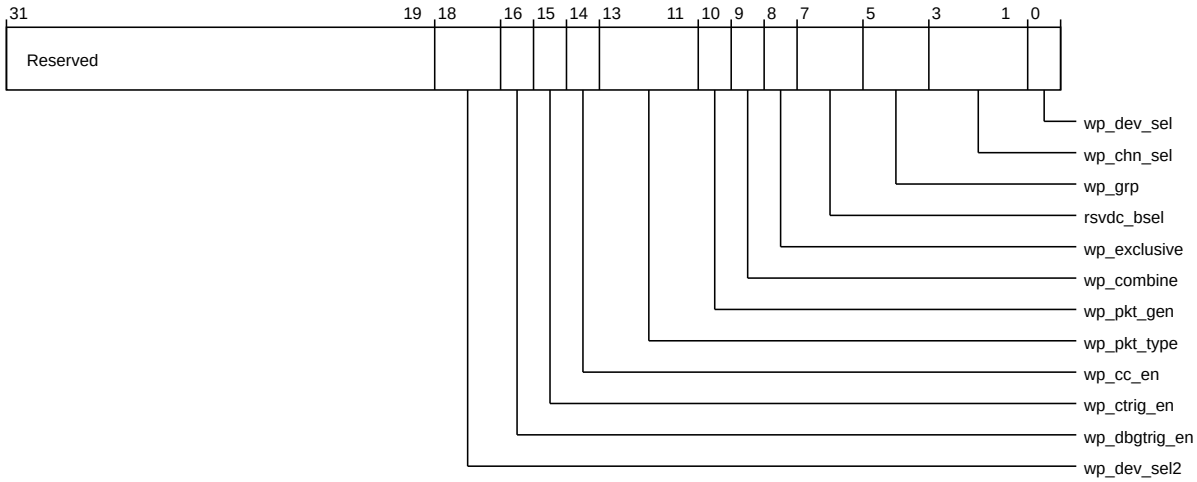
Table 5-798: por_mxp_por_dtm_wp0_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-785: por_mxp_por_dtm_wp0_config (low)



The following table shows the por_dtm_wp0_config lower register bit assignments.

Table 5-799: por_mxp_por_dtm_wp0_config (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0

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Bits	Field name	Description	Type	Reset
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	wp_combine	Enables combination of watchpoints 0 and 1	RW	1'b0
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0

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Bits	Field name	Description	Type	Reset
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.51 por_dtm_wp0_val

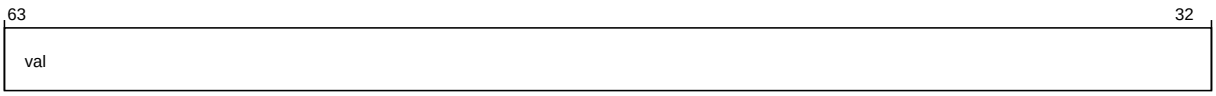
Configures watchpoint 0 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21A8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-786: por_mxp_por_dtm_wp0_val (high)



The following table shows the por_dtm_wp0_val higher register bit assignments.

Table 5-800: por_mxp_por_dtm_wp0_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

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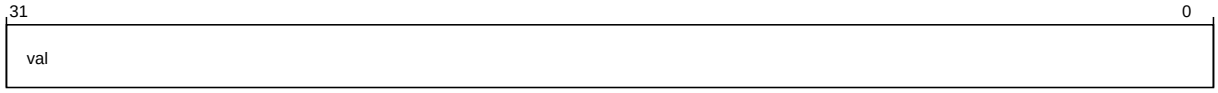
Figure 5-787: por_mxp_por_dtm_wp0_val (low)



The following table shows the por_dtm_wp0_val lower register bit assignments.

Table 5-801: por_mxp_por_dtm_wp0_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.52 por_dtm_wp0_mask

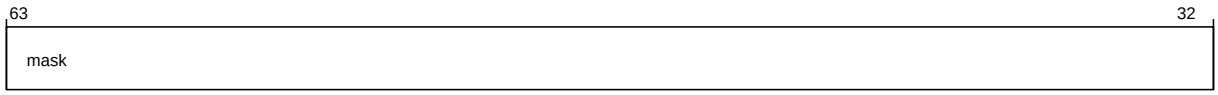
Configures watchpoint0 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21B0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-788: por_mxp_por_dtm_wp0_mask (high)



The following table shows the por_dtm_wp0_mask higher register bit assignments.

Table 5-802: por_mxp_por_dtm_wp0_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

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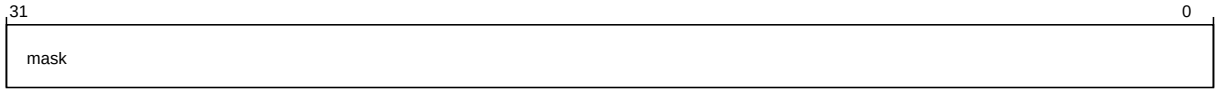
Figure 5-789: por_mxp_por_dtm_wp0_mask (low)



The following table shows the por_dtm_wp0_mask lower register bit assignments.

Table 5-803: por_mxp_por_dtm_wp0_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.53 por_dtm_wp1_config

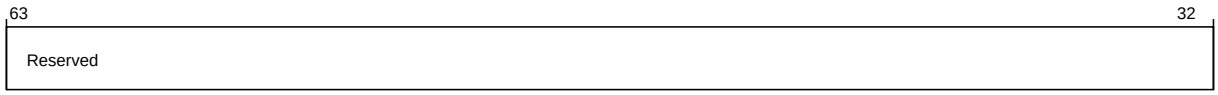
Configures watchpoint 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21B8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-790: por_mxp_por_dtm_wp1_config (high)



The following table shows the por_dtm_wp1_config higher register bit assignments.

Table 5-804: por_mxp_por_dtm_wp1_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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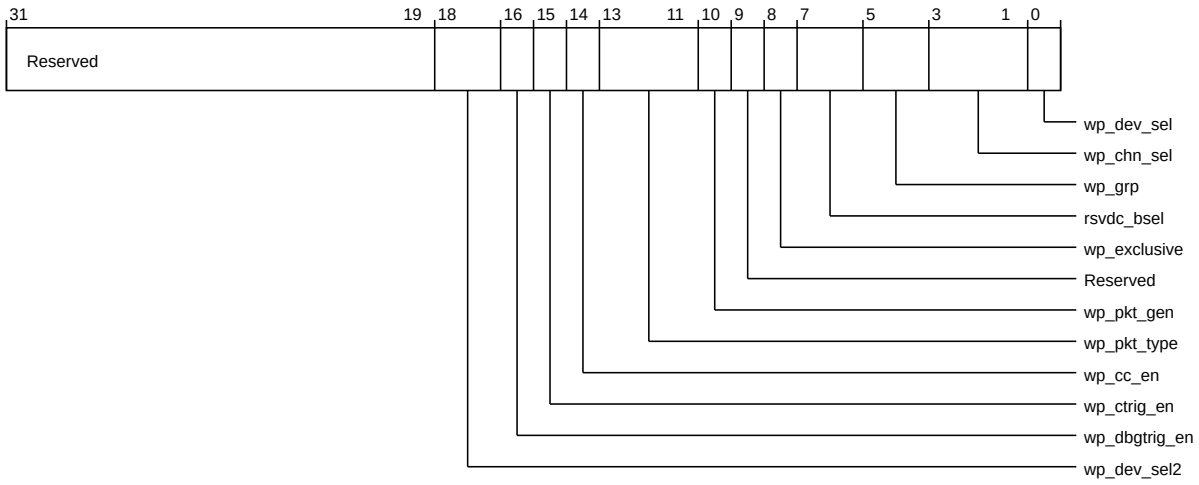
Figure 5-791: por_mxp_por_dtm_wp1_config (low)



The following table shows the por_dtm_wp1_config lower register bit assignments.

Table 5-805: por_mxp_por_dtm_wp1_config (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.54 por_dtm_wp1_val

Configures watchpoint 1 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21C0

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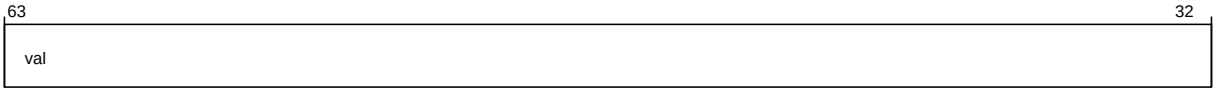
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-792: por_mxp_por_dtm_wp1_val (high)



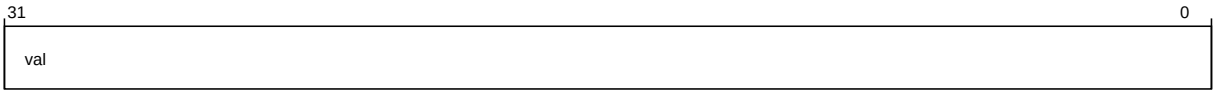
The following table shows the por_dtm_wp1_val higher register bit assignments.

Table 5-806: por_mxp_por_dtm_wp1_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-793: por_mxp_por_dtm_wp1_val (low)



The following table shows the por_dtm_wp1_val lower register bit assignments.

Table 5-807: por_mxp_por_dtm_wp1_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.55 por_dtm_wp1_mask

Configures watchpoint 1 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21C8
Register reset 64'b0

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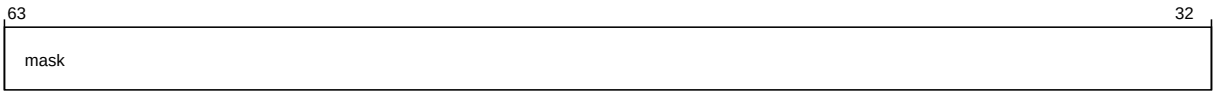
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-794: por_mxp_por_dtm_wp1_mask (high)



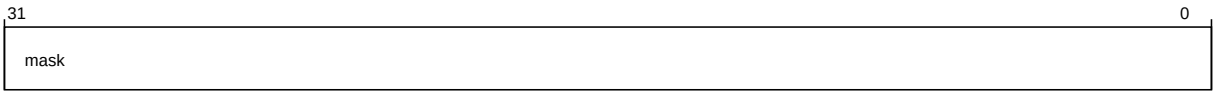
The following table shows the por_dtm_wp1_mask higher register bit assignments.

Table 5-808: por_mxp_por_dtm_wp1_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-795: por_mxp_por_dtm_wp1_mask (low)



The following table shows the por_dtm_wp1_mask lower register bit assignments.

Table 5-809: por_mxp_por_dtm_wp1_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.56 por_dtm_wp2_config

Configures watchpoint 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21D0
Register reset 64'b0
Usage constraints There are no usage constraints.

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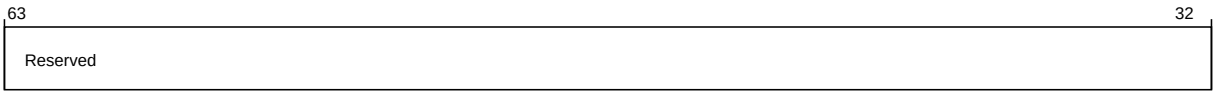
The following figure shows the higher register bit assignments.

Figure 5-796: por_mxp_por_dtm_wp2_config (high)



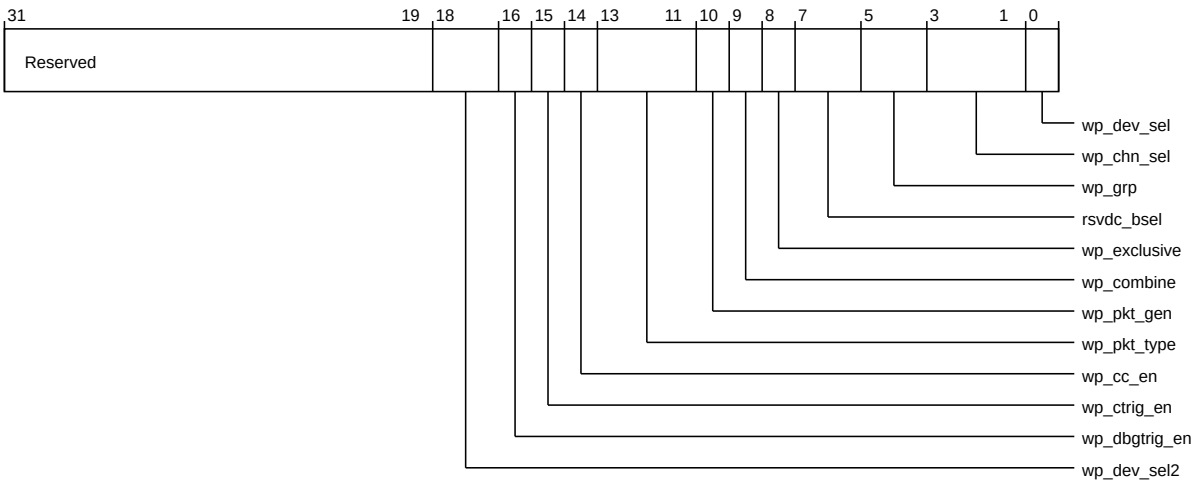
The following table shows the por_dtm_wp2_config higher register bit assignments.

Table 5-810: por_mxp_por_dtm_wp2_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-797: por_mxp_por_dtm_wp2_config (low)



The following table shows the por_dtm_wp2_config lower register bit assignments.

Table 5-811: por_mxp_por_dtm_wp2_config (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0

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Bits	Field name	Description	Type	Reset
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	wp_combine	Enables combination of watchpoints 2 and 3	RW	1'b0
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0

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Bits	Field name	Description	Type	Reset
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.57 por_dtm_wp2_val

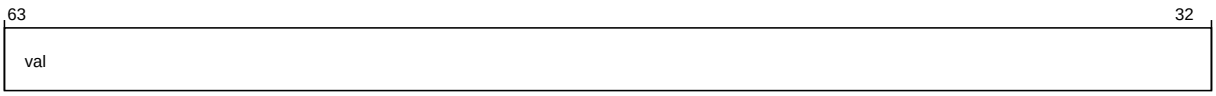
Configures watchpoint 2 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21D8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-798: por_mxp_por_dtm_wp2_val (high)



The following table shows the por_dtm_wp2_val higher register bit assignments.

Table 5-812: por_mxp_por_dtm_wp2_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

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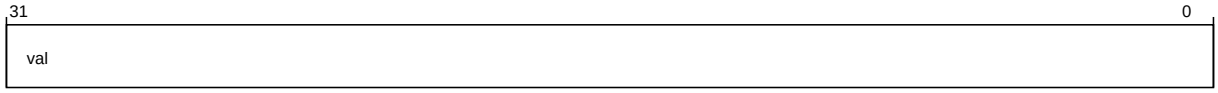
Figure 5-799: por_mxp_por_dtm_wp2_val (low)



The following table shows the por_dtm_wp2_val lower register bit assignments.

Table 5-813: por_mxp_por_dtm_wp2_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.58 por_dtm_wp2_mask

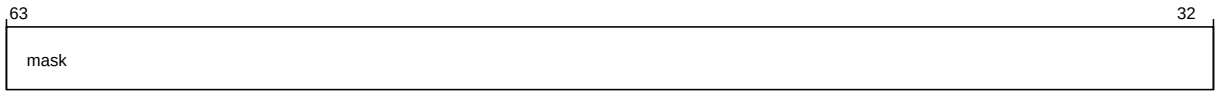
Configures watchpoint 2 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21E0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-800: por_mxp_por_dtm_wp2_mask (high)



The following table shows the por_dtm_wp2_mask higher register bit assignments.

Table 5-814: por_mxp_por_dtm_wp2_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

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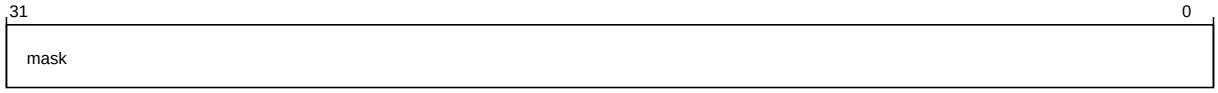
Figure 5-801: por_mxp_por_dtm_wp2_mask (low)



The following table shows the por_dtm_wp2_mask lower register bit assignments.

Table 5-815: por_mxp_por_dtm_wp2_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.59 por_dtm_wp3_config

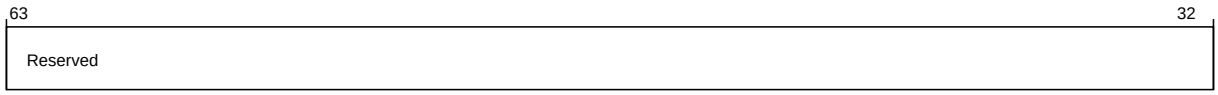
Configures watchpoint 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21E8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-802: por_mxp_por_dtm_wp3_config (high)



The following table shows the por_dtm_wp3_config higher register bit assignments.

Table 5-816: por_mxp_por_dtm_wp3_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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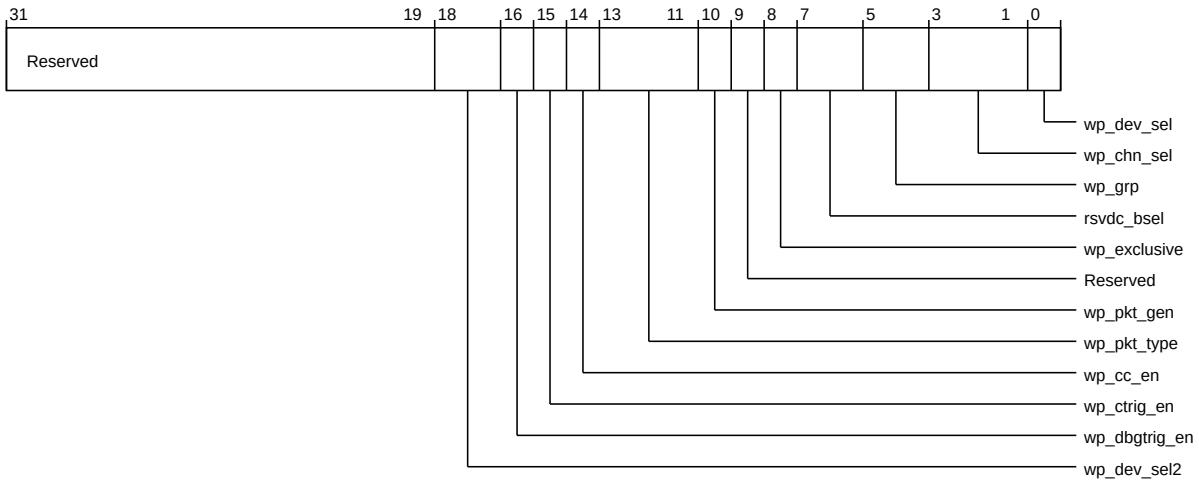
Figure 5-803: por_mxp_por_dtm_wp3_config (low)



The following table shows the por_dtm_wp3_config lower register bit assignments.

Table 5-817: por_mxp_por_dtm_wp3_config (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.60 por_dtm_wp3_val

Configures watchpoint 3 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21F0

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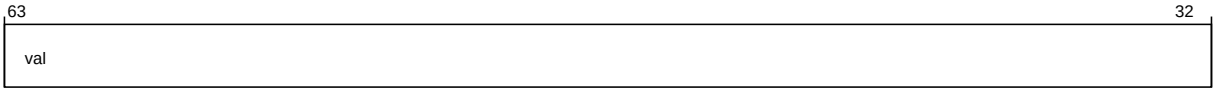
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-804: por_mxp_por_dtm_wp3_val (high)



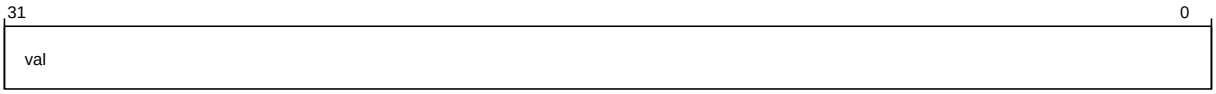
The following table shows the por_dtm_wp3_val higher register bit assignments.

Table 5-818: por_mxp_por_dtm_wp3_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-805: por_mxp_por_dtm_wp3_val (low)



The following table shows the por_dtm_wp3_val lower register bit assignments.

Table 5-819: por_mxp_por_dtm_wp3_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.61 por_dtm_wp3_mask

Configures watchpoint 3 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h21F8
Register reset 64'b0

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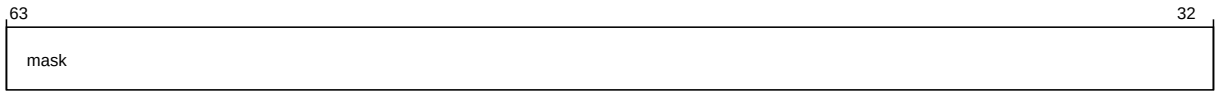
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-806: por_mxp_por_dtm_wp3_mask (high)



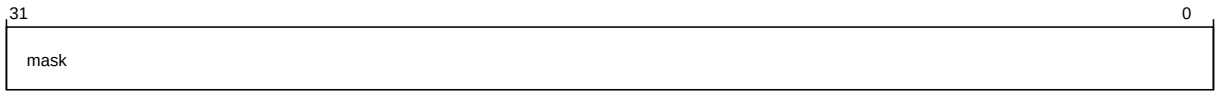
The following table shows the por_dtm_wp3_mask higher register bit assignments.

Table 5-820: por_mxp_por_dtm_wp3_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-807: por_mxp_por_dtm_wp3_mask (low)



The following table shows the por_dtm_wp3_mask lower register bit assignments.

Table 5-821: por_mxp_por_dtm_wp3_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.62 por_dtm_pmsicr

Functions as the sampling interval counter register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2200
Register reset 64'b0
Usage constraints There are no usage constraints.

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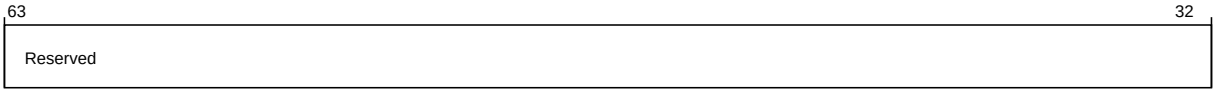
The following figure shows the higher register bit assignments.

Figure 5-808: por_mxp_por_dtm_pmsicr (high)



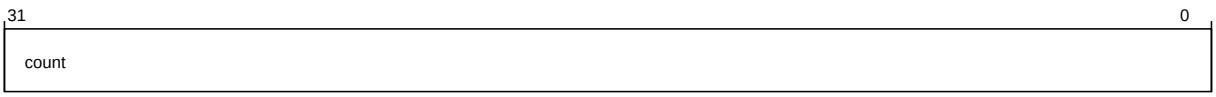
The following table shows the por_dtm_pmsicr higher register bit assignments.

Table 5-822: por_mxp_por_dtm_pmsicr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-809: por_mxp_por_dtm_pmsicr (low)



The following table shows the por_dtm_pmsicr lower register bit assignments.

Table 5-823: por_mxp_por_dtm_pmsicr (low)

Bits	Field name	Description	Type	Reset
31:0	count	Current value of sample counter	RW	32'b0

5.3.6.63 por_dtm_pmsirr

Functions as the sampling interval reload register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2208
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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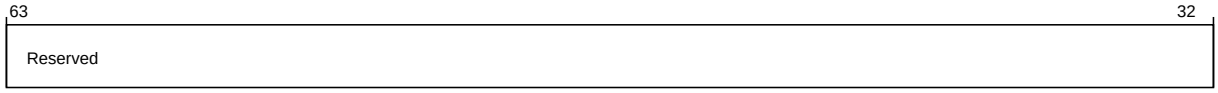
Figure 5-810: por_mxp_por_dtm_pmsirr (high)



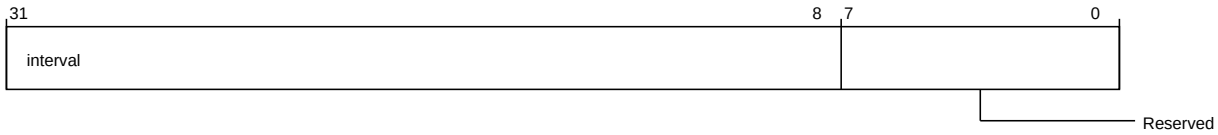
The following table shows the por_dtm_pmsirr higher register bit assignments.

Table 5-824: por_mxp_por_dtm_pmsirr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-811: por_mxp_por_dtm_pmsirr (low)



The following table shows the por_dtm_pmsirr lower register bit assignments.

Table 5-825: por_mxp_por_dtm_pmsirr (low)

Bits	Field name	Description	Type	Reset
31:8	interval	Sampling interval to be reloaded	RW	24'b0
7:0	Reserved	Reserved	RO	-

5.3.6.64 por_dtm_pmu_config

Configures the DTM PMU.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2210
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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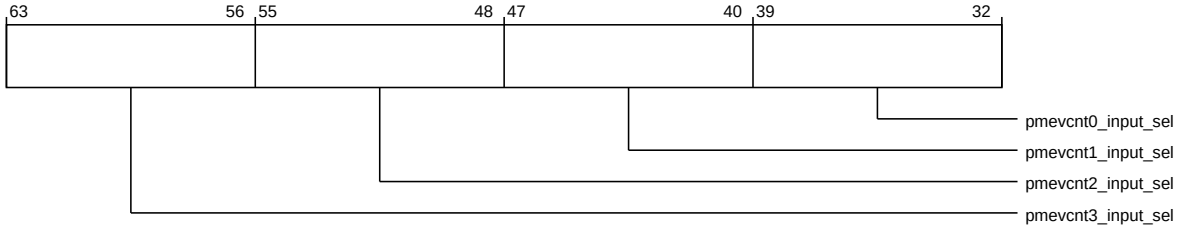
Figure 5-812: por_mxp_por_dtm_pmu_config (high)



The following table shows the por_dtm_pmu_config higher register bit assignments.

Table 5-826: por_mxp_por_dtm_pmu_config (high)

Bits	Field name	Description	Type	Reset
63:56	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	8'b0
55:48	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	8'b0
47:40	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	8'b0

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Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	Source to be counted in PMU counter 0: Port2, Port3, Port4 and Port5 encodings are applicable when (MXP_NUM_DEV_PORT_PARAM > 2 and MXP_MULTIPLE_DTM_EN_PARAM = 0) 8'h00: Watchpoint 0 8'h01: Watchpoint 1 8'h02: Watchpoint 2 8'h03: Watchpoint 3 8'h04: XP PMU Event 0 8'h05: XP PMU Event 1 8'h06: XP PMU Event 2 8'h07: XP PMU Event 3 8'h10: Port 0 Device 0 PMU Event 0 8'h11: Port 0 Device 0 PMU Event 1 8'h12: Port 0 Device 0 PMU Event 2 8'h13: Port 0 Device 0 PMU Event 3 8'h14: Port 0 Device 1 PMU Event 0 8'h15: Port 0 Device 1 PMU Event 1 8'h16: Port 0 Device 1 PMU Event 2 8'h17: Port 0 Device 1 PMU Event 3 8'h18: Port 0 Device 2 PMU Event 0 8'h19: Port 0 Device 2 PMU Event 1 8'h1A: Port 0 Device 2 PMU Event 2 8'h1B: Port 0 Device 2 PMU Event 3 8'h1C: Port 0 Device 3 PMU Event 0 8'h1D: Port 0 Device 3 PMU Event 1 8'h1E: Port 0 Device 3 PMU Event 2 8'h1F: Port 0 Device 3 PMU Event 3 8'h20: Port 1 Device 0 PMU Event 0	RW	8'b0

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Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	8'h21: Port 1 Device 0 PMU Event 1 8'h22: Port 1 Device 0 PMU Event 2 8'h23: Port 1 Device 0 PMU Event 3 8'h24: Port 1 Device 1 PMU Event 0 8'h25: Port 1 Device 1 PMU Event 1 8'h26: Port 1 Device 1 PMU Event 2 8'h27: Port 1 Device 1 PMU Event 3 8'h28: Port 1 Device 2 PMU Event 0 8'h29: Port 1 Device 2 PMU Event 1 8'h2A: Port 1 Device 2 PMU Event 2 8'h2B: Port 1 Device 2 PMU Event 3 8'h2C: Port 1 Device 3 PMU Event 0 8'h2D: Port 1 Device 3 PMU Event 1 8'h2E: Port 1 Device 3 PMU Event 2 8'h2F: Port 1 Device 3 PMU Event 3 8'h30: Port 2 Device 0 PMU Event 0 8'h31: Port 2 Device 0 PMU Event 1 8'h32: Port 2 Device 0 PMU Event 2 8'h33: Port 2 Device 0 PMU Event 3 8'h34: Port 2 Device 1 PMU Event 0 8'h35: Port 2 Device 1 PMU Event 1 8'h36: Port 2 Device 1 PMU Event 2 8'h37: Port 2 Device 1 PMU Event 3 8'h38: Port 2 Device 2 PMU Event 0 8'h39: Port 2 Device 2 PMU Event 1 8'h3A: Port 2 Device 2 PMU Event 2	RW	8'b0

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Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	8'h3B: Port 2 Device 2 PMU Event 3 8'h3C: Port 2 Device 3 PMU Event 0 8'h3D: Port 2 Device 3 PMU Event 1 8'h3E: Port 2 Device 3 PMU Event 2 8'h3F: Port 2 Device 3 PMU Event 3 8'h40: Port 3 Device 0 PMU Event 0 8'h41: Port 3 Device 0 PMU Event 1 8'h42: Port 3 Device 0 PMU Event 2 8'h43: Port 3 Device 0 PMU Event 3 8'h44: Port 3 Device 1 PMU Event 0 8'h45: Port 3 Device 1 PMU Event 1 8'h46: Port 3 Device 1 PMU Event 2 8'h47: Port 3 Device 1 PMU Event 3 8'h48: Port 3 Device 2 PMU Event 0 8'h49: Port 3 Device 2 PMU Event 1 8'h4A: Port 3 Device 2 PMU Event 2 8'h4B: Port 3 Device 2 PMU Event 3 8'h4C: Port 3 Device 3 PMU Event 0 8'h4D: Port 3 Device 3 PMU Event 1 8'h4E: Port 3 Device 3 PMU Event 2 8'h4F: Port 3 Device 3 PMU Event 3 8'h50: Port 4 Device 0 PMU Event 0 8'h51: Port 4 Device 0 PMU Event 1 8'h52: Port 4 Device 0 PMU Event 2 8'h53: Port 4 Device 0 PMU Event 3 8'h54: Port 4 Device 1 PMU Event 0	RW	8'b0

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Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	8'h55: Port 4 Device 1 PMU Event 1 8'h56: Port 4 Device 1 PMU Event 2 8'h57: Port 4 Device 1 PMU Event 3 8'h58: Port 4 Device 2 PMU Event 0 8'h59: Port 4 Device 2 PMU Event 1 8'h5A: Port 4 Device 2 PMU Event 2 8'h5B: Port 4 Device 2 PMU Event 3 8'h5C: Port 4 Device 3 PMU Event 0 8'h5D: Port 4 Device 3 PMU Event 1 8'h5E: Port 4 Device 3 PMU Event 2 8'h5F: Port 4 Device 3 PMU Event 3 8'h60: Port 5 Device 0 PMU Event 0 8'h61: Port 5 Device 0 PMU Event 1 8'h62: Port 5 Device 0 PMU Event 2 8'h63: Port 5 Device 0 PMU Event 3 8'h64: Port 5 Device 1 PMU Event 0 8'h65: Port 5 Device 1 PMU Event 1 8'h66: Port 5 Device 1 PMU Event 2 8'h67: Port 5 Device 1 PMU Event 3 8'h68: Port 5 Device 2 PMU Event 0 8'h69: Port 5 Device 2 PMU Event 1 8'h6A: Port 5 Device 2 PMU Event 2 8'h6B: Port 5 Device 2 PMU Event 3 8'h6C: Port 5 Device 3 PMU Event 0 8'h6D: Port 5 Device 3 PMU Event 1 8'h6E: Port 5 Device 3 PMU Event 2 8'h6F: Port 5 Device 3 PMU Event 3	RW	8'b0

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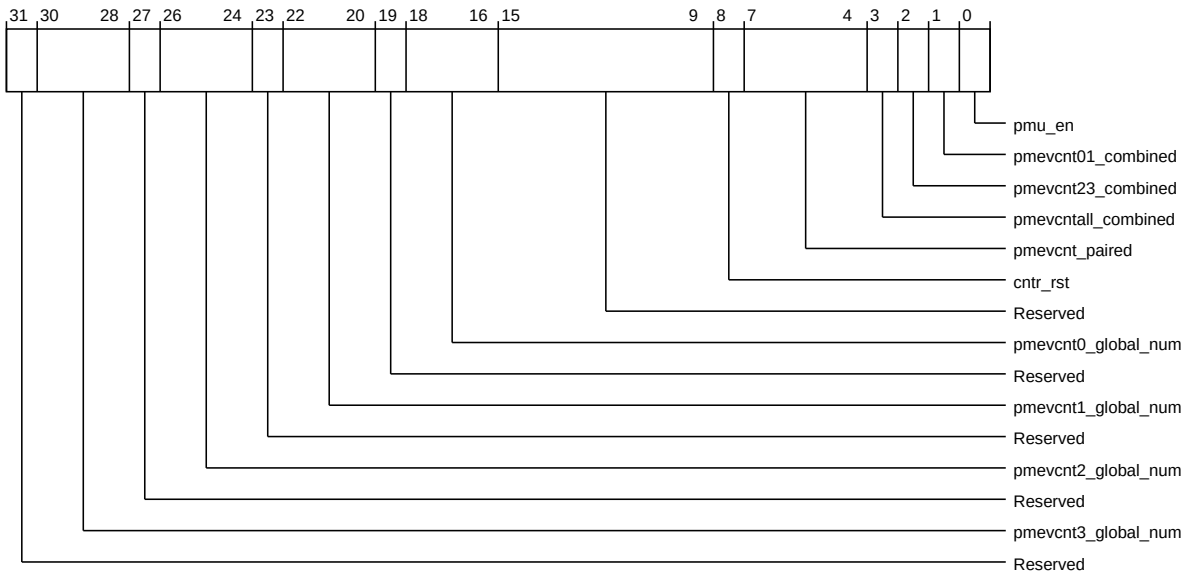
The following figure shows the lower register bit assignments.

Figure 5-813: por_mxp_por_dtm_pmu_config (low)



The following table shows the por_dtm_pmu_config lower register bit assignments.

Table 5-827: por_mxp_por_dtm_pmu_config (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0
19	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

5.3.6.65 por_dtm_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2220
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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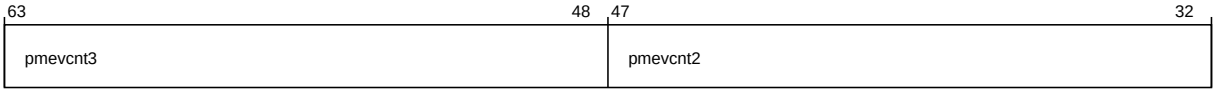
Figure 5-814: por_mxp_por_dtm_pmevcnt (high)



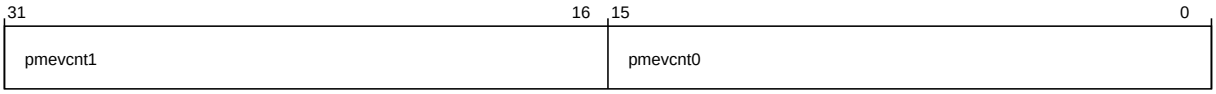
The following table shows the por_dtm_pmevcnt higher register bit assignments.

Table 5-828: por_mxp_por_dtm_pmevcnt (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcnt3	PMU event counter 3	RW	16'h0000
47:32	pmevcnt2	PMU event counter 2	RW	16'h0000

The following figure shows the lower register bit assignments.

Figure 5-815: por_mxp_por_dtm_pmevcnt (low)



The following table shows the por_dtm_pmevcnt lower register bit assignments.

Table 5-829: por_mxp_por_dtm_pmevcnt (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcnt1	PMU event counter 1	RW	16'h0000
15:0	pmevcnt0	PMU event counter 0	RW	16'h0000

5.3.6.66 por_dtm_pmevcntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2240
Register reset 64'b0
Usage constraints There are no usage constraints.

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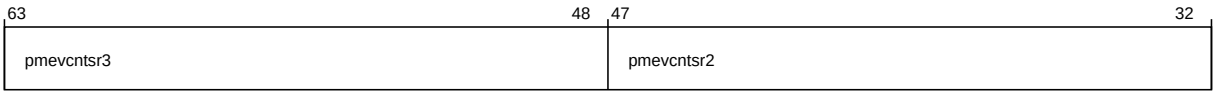
The following figure shows the higher register bit assignments.

Figure 5-816: por_mxp_por_dtm_pmevcntsr (high)



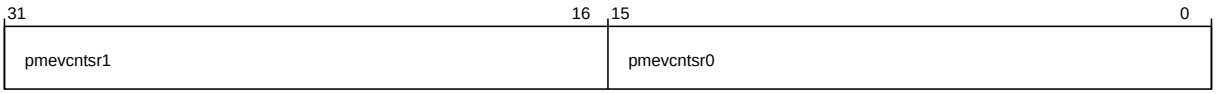
The following table shows the por_dtm_pmevcntsr higher register bit assignments.

Table 5-830: por_mxp_por_dtm_pmevcntsr (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000

The following figure shows the lower register bit assignments.

Figure 5-817: por_mxp_por_dtm_pmevcntsr (low)



The following table shows the por_dtm_pmevcntsr lower register bit assignments.

Table 5-831: por_mxp_por_dtm_pmevcntsr (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

5.3.6.67 por_dtm_control_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Functions as the DTM control register. NOTE: There will be max. of 3 DTM registers based on MXP_MULTIPLE_DTM_EN_PARAM and MXP_NUM_DEV_PORT_PARAM value. Each successive DTM register will be at the next 'h200 + 8 byte address boundary. Each successive DTM register will be named with the suffix corresponding to the DT register number. For example por_dtm_control_dt<0:2>

Its characteristics are:

Type RW

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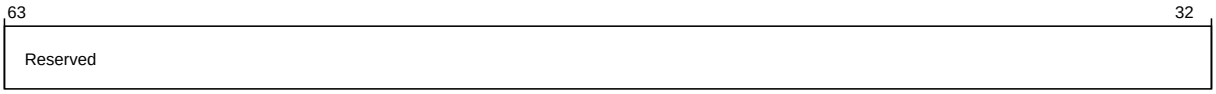
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h000 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-818: por_mxp_por_dtm_control_dt$index (high)



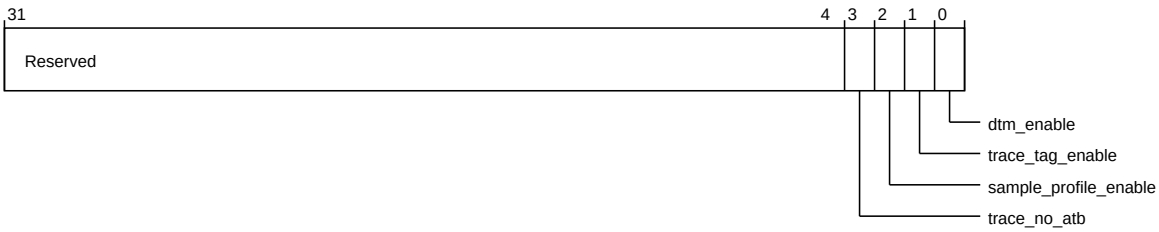
The following table shows the por_dtm_control_dt$index higher register bit assignments.

Table 5-832: por_mxp_por_dtm_control_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-819: por_mxp_por_dtm_control_dt$index (low)



The following table shows the por_dtm_control_dt$index lower register bit assignments.

Table 5-833: por_mxp_por_dtm_control_dt$index (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet	RW	1'b0
2	sample_profile_enable	Enables sample profile function	RW	1'b0

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Bits	Field name	Description	Type	Reset
1	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
0	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

5.3.6.68 por_dtm_fifo_entry_ready_dt$index

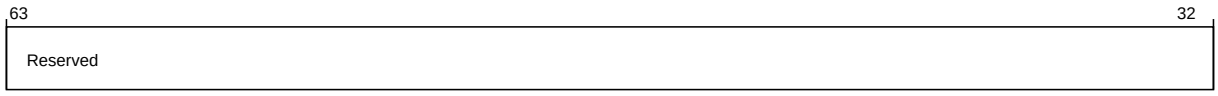
This register repeats once. It is parameterized by the $index from 1 to 2. Controls status of DTM FIFO entries.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h018 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-820: por_mxp_por_dtm_fifo_entry_ready_dt$index (high)



The following table shows the por_dtm_fifo_entry_ready_dt$index higher register bit assignments.

Table 5-834: por_mxp_por_dtm_fifo_entry_ready_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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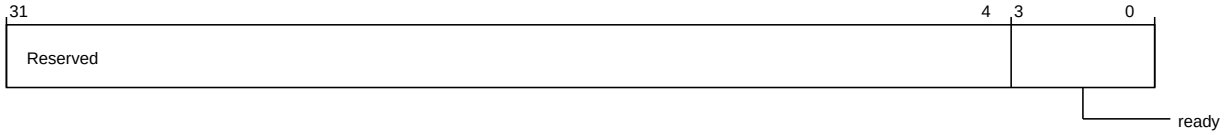
Figure 5-821: por_mxp_por_dtm_fifo_entry_ready_dt$index (low)



The following table shows the por_dtm_fifo_entry_ready_dt$index lower register bit assignments.

Table 5-835: por_mxp_por_dtm_fifo_entry_ready_dt$index (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

5.3.6.69 por_dtm_fifo_entry0_0_dt$index

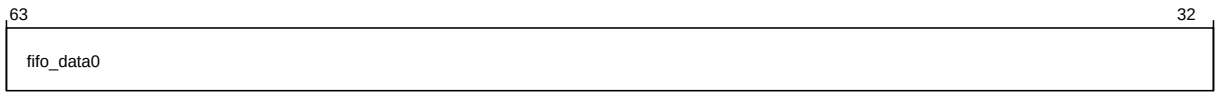
This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h020 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-822: por_mxp_por_dtm_fifo_entry0_0_dt$index (high)



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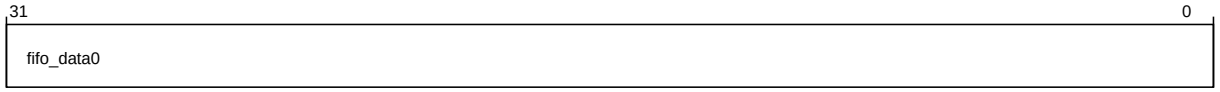
The following table shows the por_dtm_fifo_entry0_0_dt$index higher register bit assignments.

Table 5-836: por_mxp_por_dtm_fifo_entry0_0_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-823: por_mxp_por_dtm_fifo_entry0_0_dt$index (low)



The following table shows the por_dtm_fifo_entry0_0_dt$index lower register bit assignments.

Table 5-837: por_mxp_por_dtm_fifo_entry0_0_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.70 por_dtm_fifo_entry0_1_dt$index

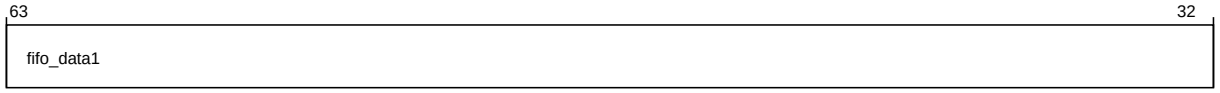
This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h028 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-824: por_mxp_por_dtm_fifo_entry0_1_dt$index (high)



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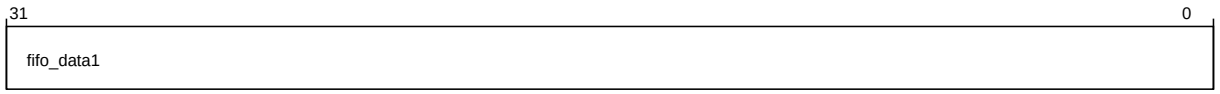
The following table shows the por_dtm_fifo_entry0_1_dt$index higher register bit assignments.

Table 5-838: por_mxp_por_dtm_fifo_entry0_1_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-825: por_mxp_por_dtm_fifo_entry0_1_dt$index (low)



The following table shows the por_dtm_fifo_entry0_1_dt$index lower register bit assignments.

Table 5-839: por_mxp_por_dtm_fifo_entry0_1_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.71 por_dtm_fifo_entry0_2_dt$index

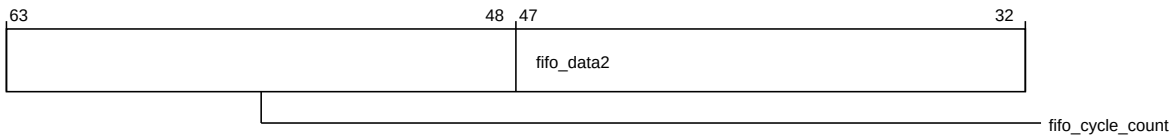
This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h030 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-826: por_mxp_por_dtm_fifo_entry0_2_dt$index (high)



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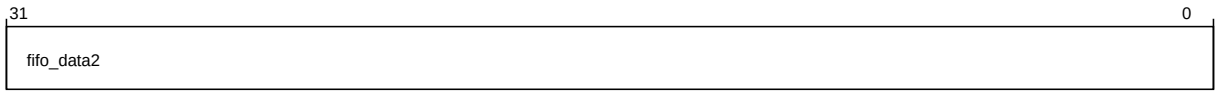
The following table shows the por_dtm_fifo_entry0_2_dt$index higher register bit assignments.

Table 5-840: por_mxp_por_dtm_fifo_entry0_2_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-827: por_mxp_por_dtm_fifo_entry0_2_dt$index (low)



The following table shows the por_dtm_fifo_entry0_2_dt$index lower register bit assignments.

Table 5-841: por_mxp_por_dtm_fifo_entry0_2_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.72 por_dtm_fifo_entry1_0_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h038 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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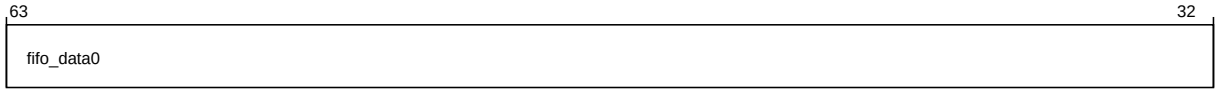
Figure 5-828: por_mxp_por_dtm_fifo_entry1_0_dt$index (high)



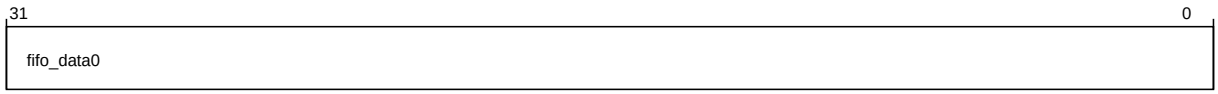
The following table shows the por_dtm_fifo_entry1_0_dt$index higher register bit assignments.

Table 5-842: por_mxp_por_dtm_fifo_entry1_0_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-829: por_mxp_por_dtm_fifo_entry1_0_dt$index (low)



The following table shows the por_dtm_fifo_entry1_0_dt$index lower register bit assignments.

Table 5-843: por_mxp_por_dtm_fifo_entry1_0_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.73 por_dtm_fifo_entry1_1_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h040 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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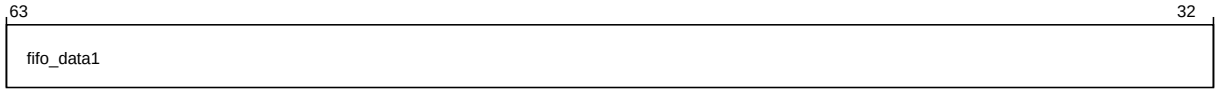
Figure 5-830: por_mxp_por_dtm_fifo_entry1_1_dt$index (high)



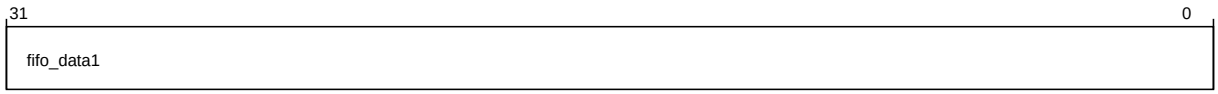
The following table shows the por_dtm_fifo_entry1_1_dt$index higher register bit assignments.

Table 5-844: por_mxp_por_dtm_fifo_entry1_1_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-831: por_mxp_por_dtm_fifo_entry1_1_dt$index (low)



The following table shows the por_dtm_fifo_entry1_1_dt$index lower register bit assignments.

Table 5-845: por_mxp_por_dtm_fifo_entry1_1_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.74 por_dtm_fifo_entry1_2_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h048 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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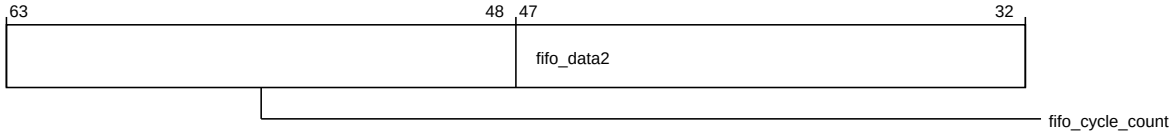
Figure 5-832: por_mxp_por_dtm_fifo_entry1_2_dt$index (high)



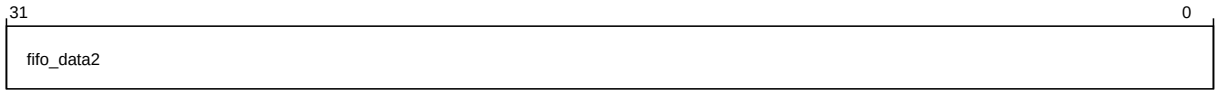
The following table shows the por_dtm_fifo_entry1_2_dt$index higher register bit assignments.

Table 5-846: por_mxp_por_dtm_fifo_entry1_2_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-833: por_mxp_por_dtm_fifo_entry1_2_dt$index (low)



The following table shows the por_dtm_fifo_entry1_2_dt$index lower register bit assignments.

Table 5-847: por_mxp_por_dtm_fifo_entry1_2_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.75 por_dtm_fifo_entry2_0_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h050 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

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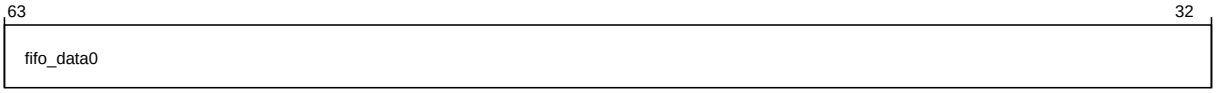
The following figure shows the higher register bit assignments.

Figure 5-834: por_mxp_por_dtm_fifo_entry2_0_dt$index (high)



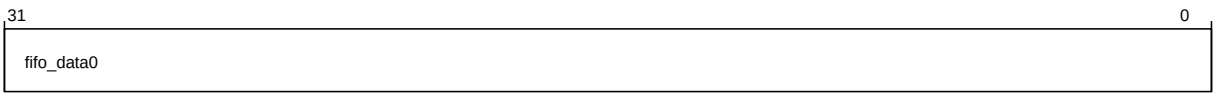
The following table shows the por_dtm_fifo_entry2_0_dt$index higher register bit assignments.

Table 5-848: por_mxp_por_dtm_fifo_entry2_0_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-835: por_mxp_por_dtm_fifo_entry2_0_dt$index (low)



The following table shows the por_dtm_fifo_entry2_0_dt$index lower register bit assignments.

Table 5-849: por_mxp_por_dtm_fifo_entry2_0_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.76 por_dtm_fifo_entry2_1_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h058 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

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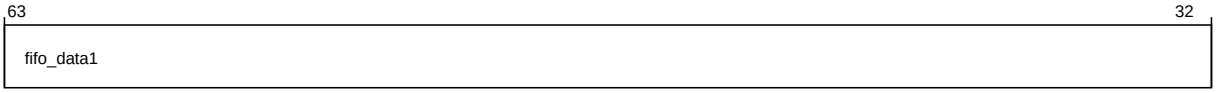
The following figure shows the higher register bit assignments.

Figure 5-836: por_mxp_por_dtm_fifo_entry2_1_dt$index (high)



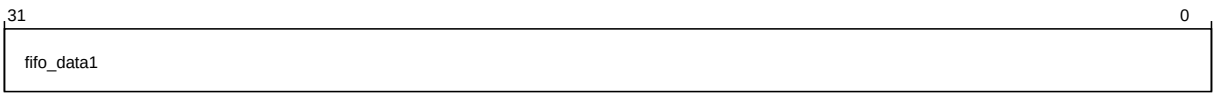
The following table shows the por_dtm_fifo_entry2_1_dt$index higher register bit assignments.

Table 5-850: por_mxp_por_dtm_fifo_entry2_1_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-837: por_mxp_por_dtm_fifo_entry2_1_dt$index (low)



The following table shows the por_dtm_fifo_entry2_1_dt$index lower register bit assignments.

Table 5-851: por_mxp_por_dtm_fifo_entry2_1_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.77 por_dtm_fifo_entry2_2_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h060 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

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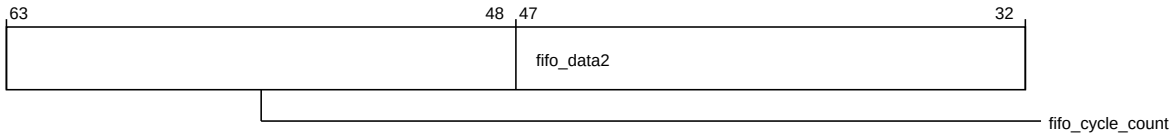
The following figure shows the higher register bit assignments.

Figure 5-838: por_mxp_por_dtm_fifo_entry2_2_dt$index (high)



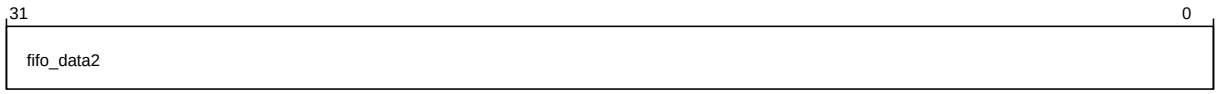
The following table shows the por_dtm_fifo_entry2_2_dt$index higher register bit assignments.

Table 5-852: por_mxp_por_dtm_fifo_entry2_2_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-839: por_mxp_por_dtm_fifo_entry2_2_dt$index (low)



The following table shows the por_dtm_fifo_entry2_2_dt$index lower register bit assignments.

Table 5-853: por_mxp_por_dtm_fifo_entry2_2_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.78 por_dtm_fifo_entry3_0_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h068 + (512 * $index)
Register reset 64'b0

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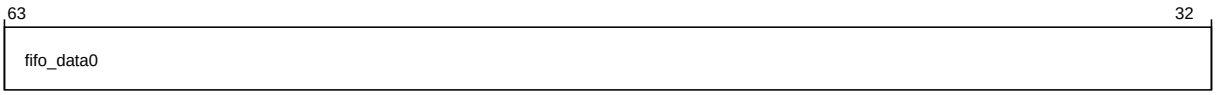
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-840: por_mxp_por_dtm_fifo_entry3_0_dt$index (high)



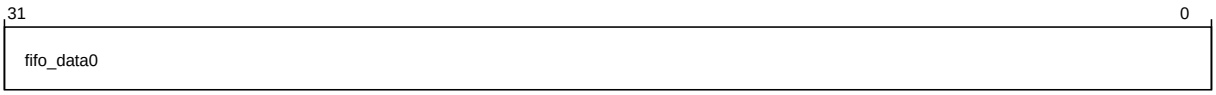
The following table shows the por_dtm_fifo_entry3_0_dt$index higher register bit assignments.

Table 5-854: por_mxp_por_dtm_fifo_entry3_0_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-841: por_mxp_por_dtm_fifo_entry3_0_dt$index (low)



The following table shows the por_dtm_fifo_entry3_0_dt$index lower register bit assignments.

Table 5-855: por_mxp_por_dtm_fifo_entry3_0_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

5.3.6.79 por_dtm_fifo_entry3_1_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h070 + (512 * $index)
Register reset 64'b0

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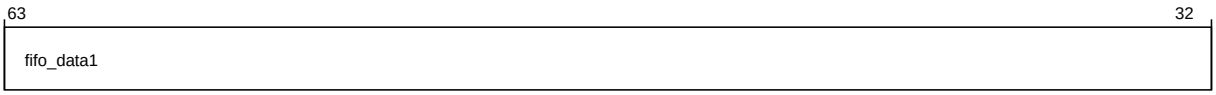
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-842: por_mxp_por_dtm_fifo_entry3_1_dt$index (high)



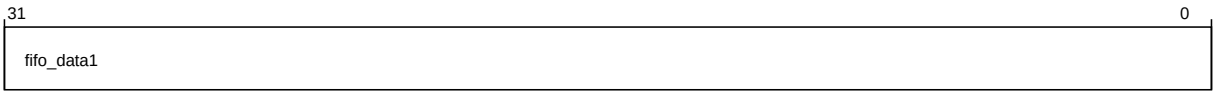
The following table shows the por_dtm_fifo_entry3_1_dt$index higher register bit assignments.

Table 5-856: por_mxp_por_dtm_fifo_entry3_1_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following figure shows the lower register bit assignments.

Figure 5-843: por_mxp_por_dtm_fifo_entry3_1_dt$index (low)



The following table shows the por_dtm_fifo_entry3_1_dt$index lower register bit assignments.

Table 5-857: por_mxp_por_dtm_fifo_entry3_1_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

5.3.6.80 por_dtm_fifo_entry3_2_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h078 + (512 * $index)
Register reset 64'b0

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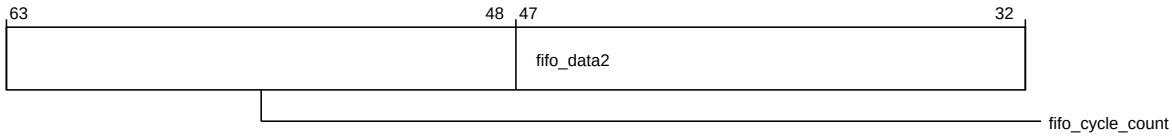
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-844: por_mxp_por_dtm_fifo_entry3_2_dt$index (high)



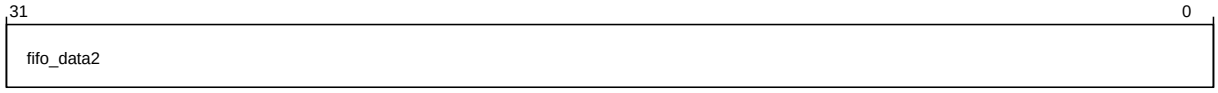
The following table shows the por_dtm_fifo_entry3_2_dt$index higher register bit assignments.

Table 5-858: por_mxp_por_dtm_fifo_entry3_2_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
47:32	fifo_data2	Entry data bit vector 143:128	RO	48'b0

The following figure shows the lower register bit assignments.

Figure 5-845: por_mxp_por_dtm_fifo_entry3_2_dt$index (low)



The following table shows the por_dtm_fifo_entry3_2_dt$index lower register bit assignments.

Table 5-859: por_mxp_por_dtm_fifo_entry3_2_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data2	Entry data bit vector 143:128	RO	48'b0

5.3.6.81 por_dtm_wp0_config_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0a0 + (512 * $index)

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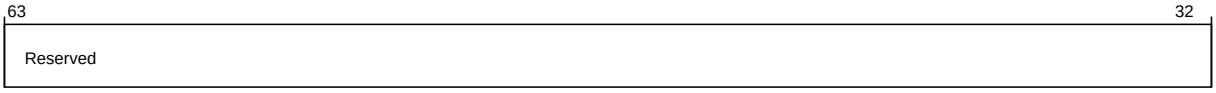
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-846: por_mxp_por_dtm_wp0_config_dt$index (high)



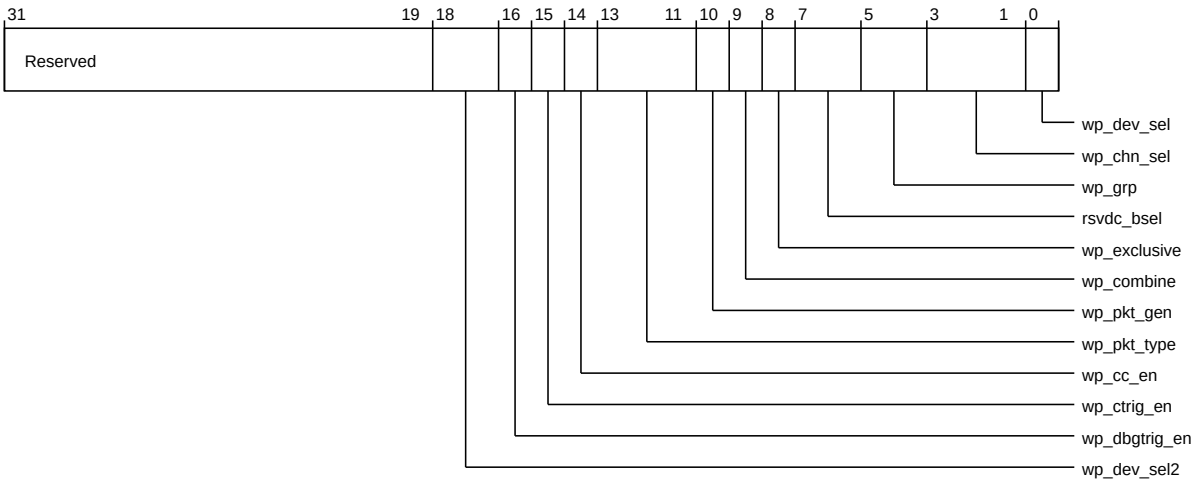
The following table shows the por_dtm_wp0_config_dt$index higher register bit assignments.

Table 5-860: por_mxp_por_dtm_wp0_config_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-847: por_mxp_por_dtm_wp0_config_dt$index (low)



The following table shows the por_dtm_wp0_config_dt$index lower register bit assignments.

Table 5-861: por_mxp_por_dtm_wp0_config_dt$index (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0

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Bits	Field name	Description	Type	Reset
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	wp_combine	Enables combination of watchpoints 0 and 1	RW	1'b0
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0

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Bits	Field name	Description	Type	Reset
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.82 por_dtm_wp0_val_dt$index

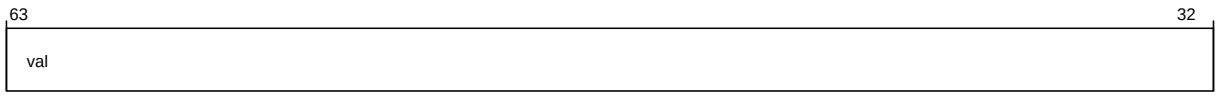
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 0 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0a8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-848: por_mxp_por_dtm_wp0_val_dt$index (high)



The following table shows the por_dtm_wp0_val_dt$index higher register bit assignments.

Table 5-862: por_mxp_por_dtm_wp0_val_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

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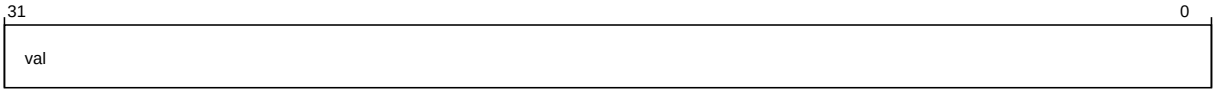
The following figure shows the lower register bit assignments.

Figure 5-849: por_mxp_por_dtm_wp0_val_dt$index (low)



The following table shows the por_dtm_wp0_val_dt$index lower register bit assignments.

Table 5-863: por_mxp_por_dtm_wp0_val_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.83 por_dtm_wp0_mask_dt$index

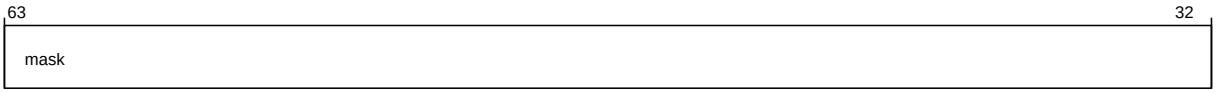
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint0 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0b0 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-850: por_mxp_por_dtm_wp0_mask_dt$index (high)



The following table shows the por_dtm_wp0_mask_dt$index higher register bit assignments.

Table 5-864: por_mxp_por_dtm_wp0_mask_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

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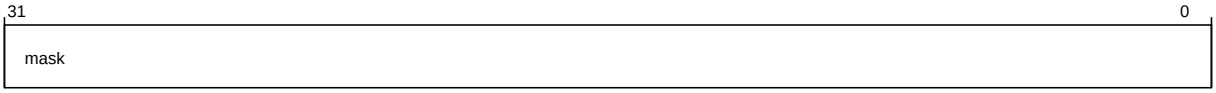
The following figure shows the lower register bit assignments.

Figure 5-851: por_mxp_por_dtm_wp0_mask_dt$index (low)



The following table shows the por_dtm_wp0_mask_dt$index lower register bit assignments.

Table 5-865: por_mxp_por_dtm_wp0_mask_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.84 por_dtm_wp1_config_dt$index

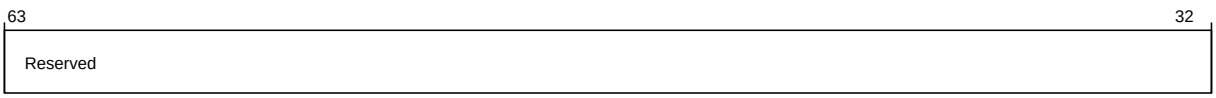
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0b8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-852: por_mxp_por_dtm_wp1_config_dt$index (high)



The following table shows the por_dtm_wp1_config_dt$index higher register bit assignments.

Table 5-866: por_mxp_por_dtm_wp1_config_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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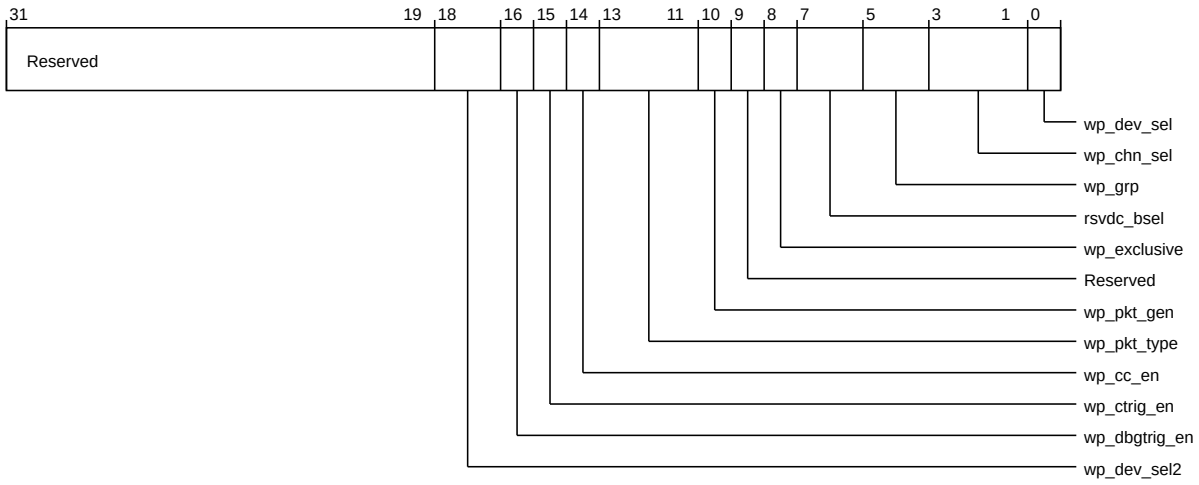
Figure 5-853: por_mxp_por_dtm_wp1_config_dt$index (low)



The following table shows the por_dtm_wp1_config_dt$index lower register bit assignments.

Table 5-867: por_mxp_por_dtm_wp1_config_dt$index (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.85 por_dtm_wp1_val_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 1 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64

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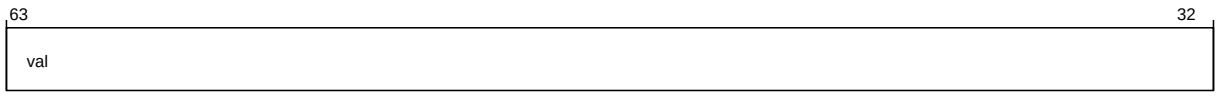
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0c0 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-854: por_mxp_por_dtm_wp1_val_dt$index (high)



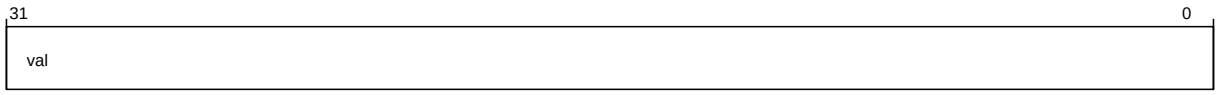
The following table shows the por_dtm_wp1_val_dt$index higher register bit assignments.

Table 5-868: por_mxp_por_dtm_wp1_val_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-855: por_mxp_por_dtm_wp1_val_dt$index (low)



The following table shows the por_dtm_wp1_val_dt$index lower register bit assignments.

Table 5-869: por_mxp_por_dtm_wp1_val_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.86 por_dtm_wp1_mask_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 1 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64

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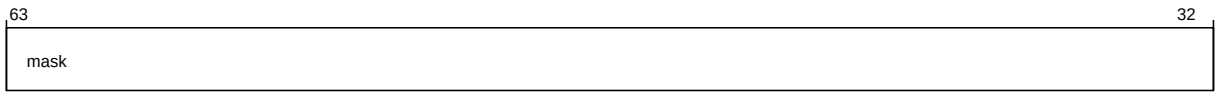
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0c8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-856: por_mxp_por_dtm_wp1_mask_dt$index (high)



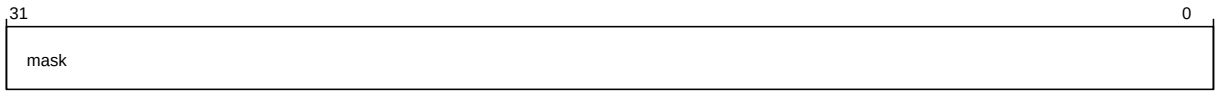
The following table shows the por_dtm_wp1_mask_dt$index higher register bit assignments.

Table 5-870: por_mxp_por_dtm_wp1_mask_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-857: por_mxp_por_dtm_wp1_mask_dt$index (low)



The following table shows the por_dtm_wp1_mask_dt$index lower register bit assignments.

Table 5-871: por_mxp_por_dtm_wp1_mask_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.87 por_dtm_wp2_config_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 2.

Its characteristics are:

Type RW
Register width (Bits) 64

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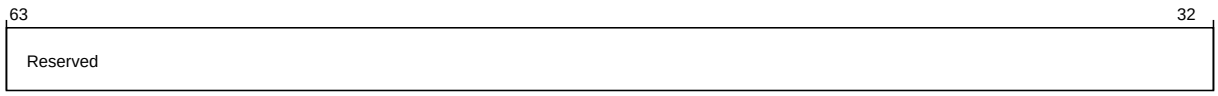
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0d0 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-858: por_mxp_por_dtm_wp2_config_dt$index (high)



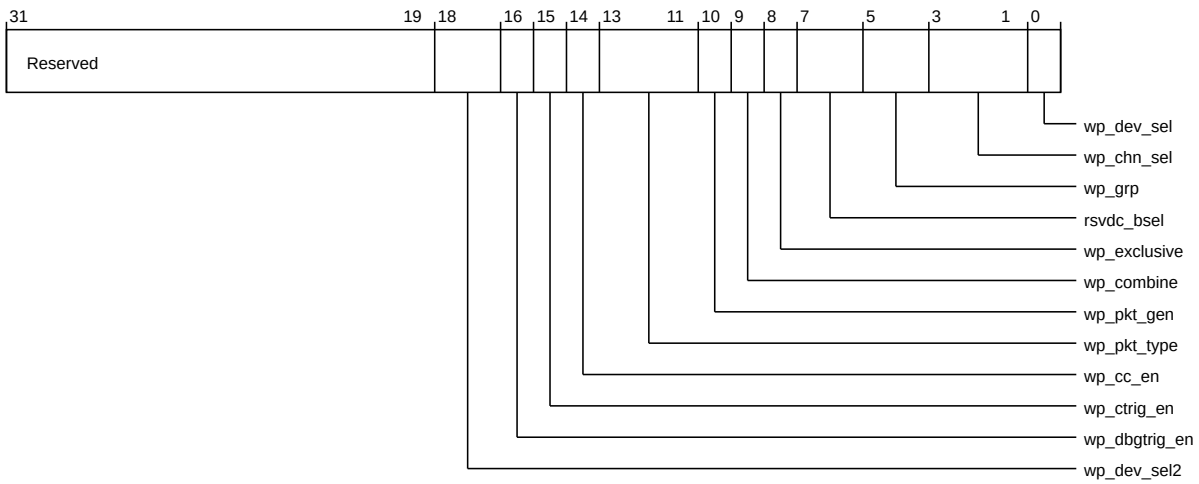
The following table shows the por_dtm_wp2_config_dt$index higher register bit assignments.

Table 5-872: por_mxp_por_dtm_wp2_config_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-859: por_mxp_por_dtm_wp2_config_dt$index (low)



The following table shows the por_dtm_wp2_config_dt$index lower register bit assignments.

Table 5-873: por_mxp_por_dtm_wp2_config_dt$index (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	wp_combine	Enables combination of watchpoints 2 and 3	RW	1'b0
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0

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Bits	Field name	Description	Type	Reset
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.88 por_dtm_wp2_val_dt$index

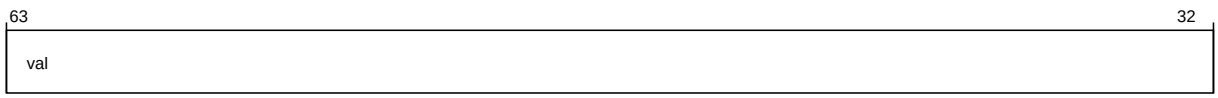
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 2 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0d8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-860: por_mxp_por_dtm_wp2_val_dt$index (high)



The following table shows the por_dtm_wp2_val_dt$index higher register bit assignments.

Table 5-874: por_mxp_por_dtm_wp2_val_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

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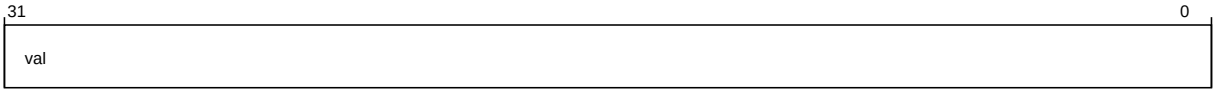
The following figure shows the lower register bit assignments.

Figure 5-861: por_mxp_por_dtm_wp2_val_dt$index (low)



The following table shows the por_dtm_wp2_val_dt$index lower register bit assignments.

Table 5-875: por_mxp_por_dtm_wp2_val_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.89 por_dtm_wp2_mask_dt$index

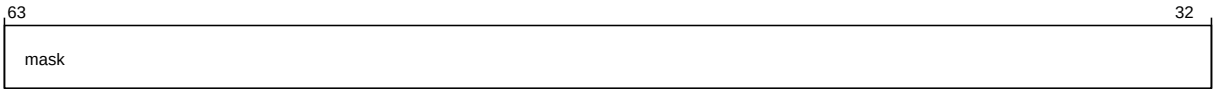
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 2 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0e0 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-862: por_mxp_por_dtm_wp2_mask_dt$index (high)



The following table shows the por_dtm_wp2_mask_dt$index higher register bit assignments.

Table 5-876: por_mxp_por_dtm_wp2_mask_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

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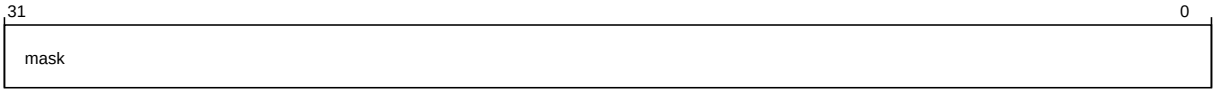
The following figure shows the lower register bit assignments.

Figure 5-863: por_mxp_por_dtm_wp2_mask_dt$index (low)



The following table shows the por_dtm_wp2_mask_dt$index lower register bit assignments.

Table 5-877: por_mxp_por_dtm_wp2_mask_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.90 por_dtm_wp3_config_dt$index

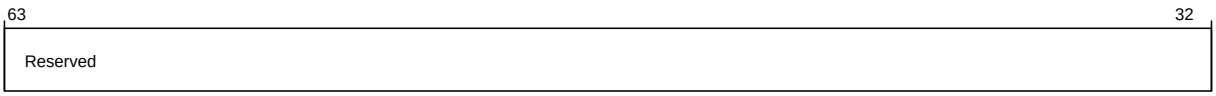
This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0e8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-864: por_mxp_por_dtm_wp3_config_dt$index (high)



The following table shows the por_dtm_wp3_config_dt$index higher register bit assignments.

Table 5-878: por_mxp_por_dtm_wp3_config_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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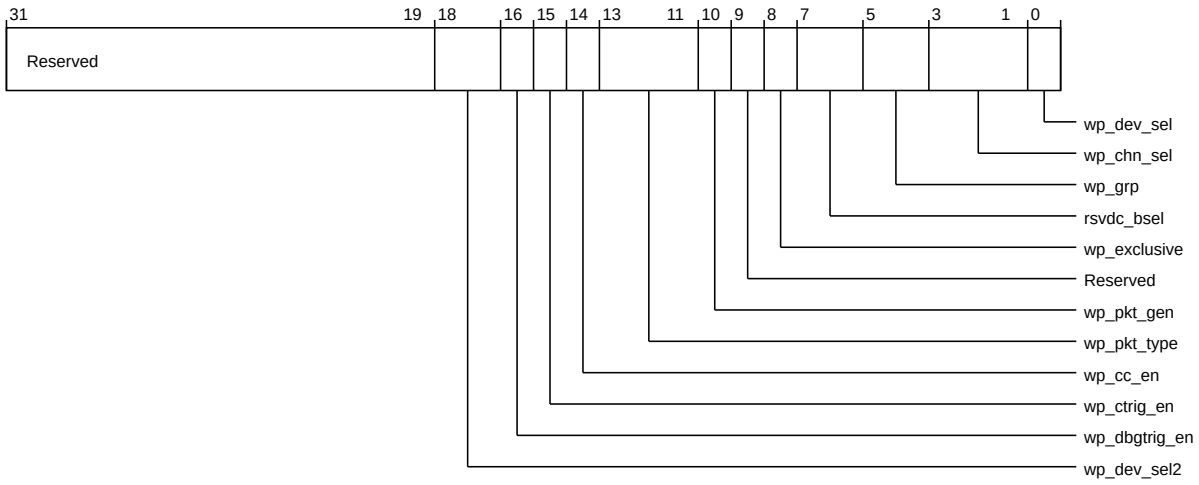
Figure 5-865: por_mxp_por_dtm_wp3_config_dt$index (low)



The following table shows the por_dtm_wp3_config_dt$index lower register bit assignments.

Table 5-879: por_mxp_por_dtm_wp3_config_dt$index (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:17	wp_dev_sel2	Upper bits for device port selection in specified SMXP	RW	2'b0
16	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
15	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
14	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
13:11	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: DAT flit DATA [127:0] 3'b110: DAT flit DATA [255:128] 3'b111: Reserved	RW	3'b000
10	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
9	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
8	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
7:6	rsvdc_bsel	Byte select of RSVDC in trace packet 2'h0: Select RSVDC[7:0] 2'h1: Select RSVDC[15:8] 2'h2: Select RSVDC[23:16] 2'h3: Select RSVDC[31:24]	RW	1'b0
5:4	wp_grp	Watchpoint register format group 2'h0: Select primary group 2'h1: Select secondary group 2'h2: Select tertiary group 2'h3: Reserved	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

5.3.6.91 por_dtm_wp3_val_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 3 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64

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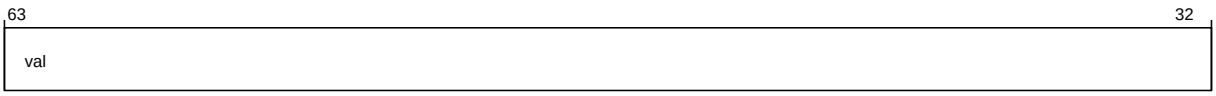
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0f0 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-866: por_mxp_por_dtm_wp3_val_dt$index (high)



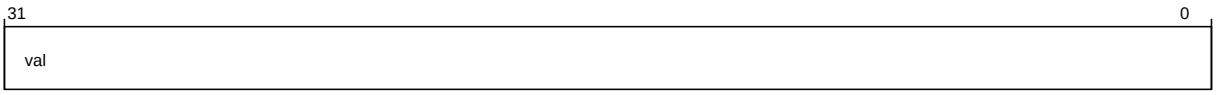
The following table shows the por_dtm_wp3_val_dt$index higher register bit assignments.

Table 5-880: por_mxp_por_dtm_wp3_val_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-867: por_mxp_por_dtm_wp3_val_dt$index (low)



The following table shows the por_dtm_wp3_val_dt$index lower register bit assignments.

Table 5-881: por_mxp_por_dtm_wp3_val_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.92 por_dtm_wp3_mask_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures watchpoint 3 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64

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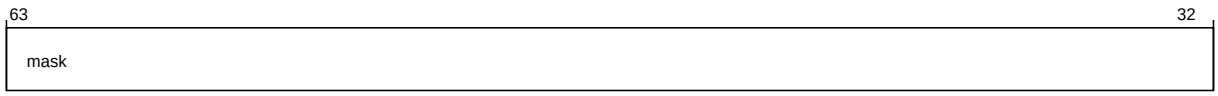
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h0f8 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-868: por_mxp_por_dtm_wp3_mask_dt$index (high)



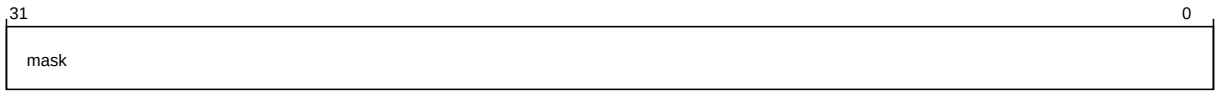
The following table shows the por_dtm_wp3_mask_dt$index higher register bit assignments.

Table 5-882: por_mxp_por_dtm_wp3_mask_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following figure shows the lower register bit assignments.

Figure 5-869: por_mxp_por_dtm_wp3_mask_dt$index (low)



The following table shows the por_dtm_wp3_mask_dt$index lower register bit assignments.

Table 5-883: por_mxp_por_dtm_wp3_mask_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

5.3.6.93 por_dtm_pmsicr_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Functions as the sampling interval counter register.

Its characteristics are:

Type RW
Register width (Bits) 64

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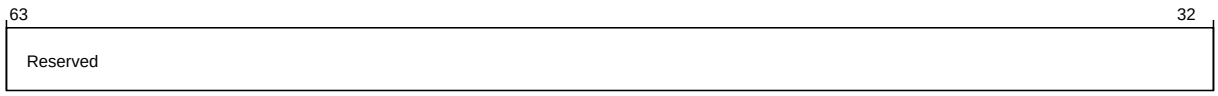
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h100 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-870: por_mxp_por_dtm_pmsicr_dt$index (high)



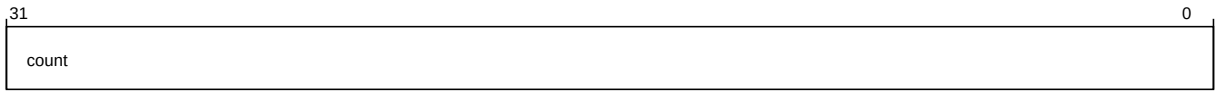
The following table shows the por_dtm_pmsicr_dt$index higher register bit assignments.

Table 5-884: por_mxp_por_dtm_pmsicr_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-871: por_mxp_por_dtm_pmsicr_dt$index (low)



The following table shows the por_dtm_pmsicr_dt$index lower register bit assignments.

Table 5-885: por_mxp_por_dtm_pmsicr_dt$index (low)

Bits	Field name	Description	Type	Reset
31:0	count	Current value of sample counter	RW	32'b0

5.3.6.94 por_dtm_pmsirr_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Functions as the sampling interval reload register.

Its characteristics are:

Type RW
Register width (Bits) 64

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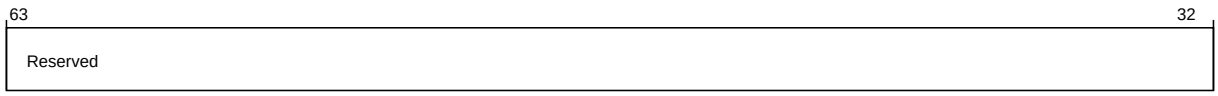
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h108 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-872: por_mxp_por_dtm_pmsirr_dt$index (high)



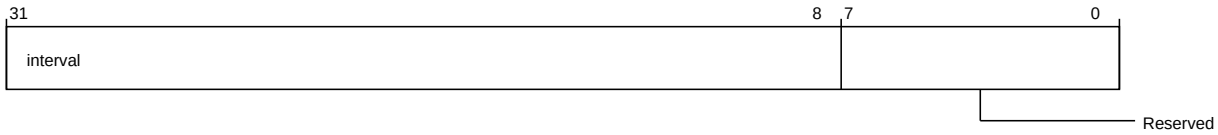
The following table shows the por_dtm_pmsirr_dt$index higher register bit assignments.

Table 5-886: por_mxp_por_dtm_pmsirr_dt$index (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-873: por_mxp_por_dtm_pmsirr_dt$index (low)



The following table shows the por_dtm_pmsirr_dt$index lower register bit assignments.

Table 5-887: por_mxp_por_dtm_pmsirr_dt$index (low)

Bits	Field name	Description	Type	Reset
31:8	interval	Sampling interval to be reloaded	RW	24'b0
7:0	Reserved	Reserved	RO	-

5.3.6.95 por_dtm_pmu_config_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Configures the DTM PMU.

Its characteristics are:

Type RW

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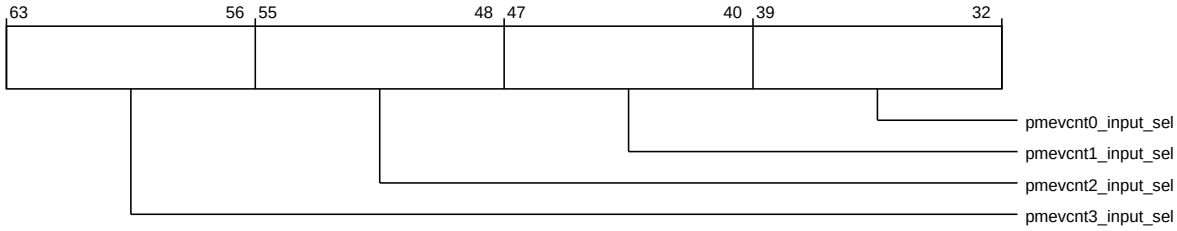
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h110 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-874: por_mxp_por_dtm_pmu_config_dt$index (high)



The following table shows the por_dtm_pmu_config_dt$index higher register bit assignments.

Table 5-888: por_mxp_por_dtm_pmu_config_dt$index (high)

Bits	Field name	Description	Type	Reset
63:56	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	8'b0
55:48	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	8'b0
47:40	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	8'b0

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Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	Source to be counted in PMU counter 0: Supports 2 Ports (DT1: P2 and P3, DT2: P4 and P5) when (MXP_NUM_DEV_PORT_PARAM > 2 and MXP_MULTIPLE_DTM_EN_PARAM = 1) 8'h00: Watchpoint 0 8'h01: Watchpoint 1 8'h02: Watchpoint 2 8'h03: Watchpoint 3 8'h04: XP PMU Event 0 8'h05: XP PMU Event 1 8'h06: XP PMU Event 2 8'h07: XP PMU Event 3 8'h10: Port 0 Device 0 PMU Event 0 8'h11: Port 0 Device 0 PMU Event 1 8'h12: Port 0 Device 0 PMU Event 2 8'h13: Port 0 Device 0 PMU Event 3 8'h14: Port 0 Device 1 PMU Event 0 8'h15: Port 0 Device 1 PMU Event 1 8'h16: Port 0 Device 1 PMU Event 2 8'h17: Port 0 Device 1 PMU Event 3 8'h18: Port 0 Device 2 PMU Event 0 8'h19: Port 0 Device 2 PMU Event 1 8'h1A: Port 0 Device 2 PMU Event 2 8'h1B: Port 0 Device 2 PMU Event 3 8'h1C: Port 0 Device 3 PMU Event 0 8'h1D: Port 0 Device 3 PMU Event 1 8'h1E: Port 0 Device 3 PMU Event 2 8'h1F: Port 0 Device 3 PMU Event 3 8'h20: Port 1 Device 0 PMU Event 0	RW	8'b0

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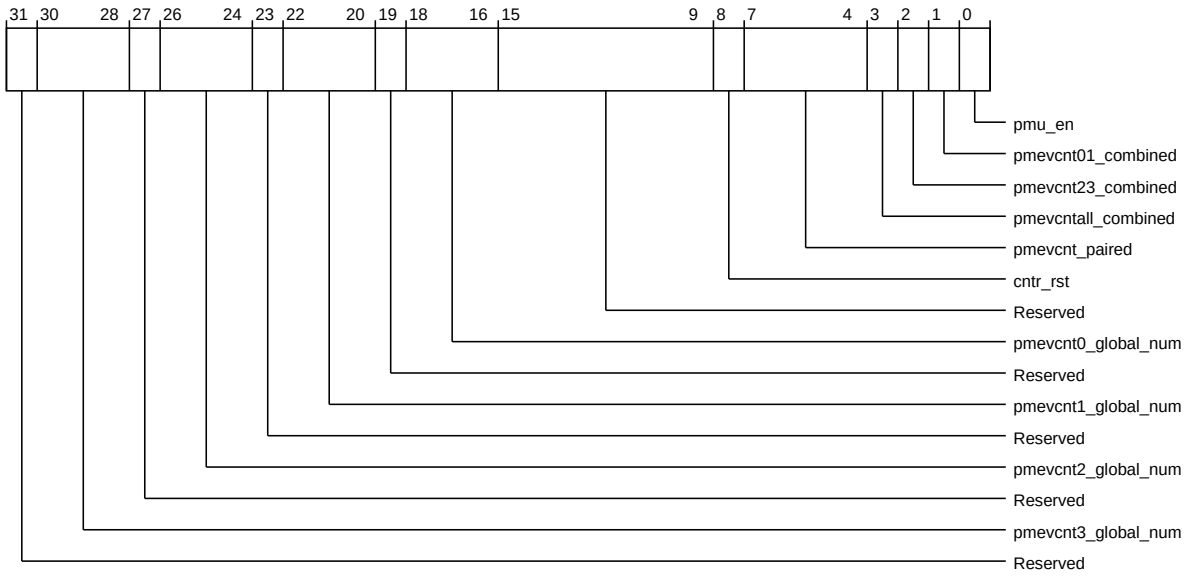
Bits	Field name	Description	Type	Reset
39:32	pmevcnt0_input_sel	8'h21: Port 1 Device 0 PMU Event 1 8'h22: Port 1 Device 0 PMU Event 2 8'h23: Port 1 Device 0 PMU Event 3 8'h24: Port 1 Device 1 PMU Event 0 8'h25: Port 1 Device 1 PMU Event 1 8'h26: Port 1 Device 1 PMU Event 2 8'h27: Port 1 Device 1 PMU Event 3 8'h28: Port 1 Device 2 PMU Event 0 8'h29: Port 1 Device 2 PMU Event 1 8'h2A: Port 1 Device 2 PMU Event 2 8'h2B: Port 1 Device 2 PMU Event 3 8'h2C: Port 1 Device 3 PMU Event 0 8'h2D: Port 1 Device 3 PMU Event 1 8'h2E: Port 1 Device 3 PMU Event 2 8'h2F: Port 1 Device 3 PMU Event 3	RW	8'b0

The following figure shows the lower register bit assignments.

Figure 5-875: por_mxp_por_dtm_pmu_config_dt$index (low)



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The following table shows the por_dtm_pmu_config_dt$index lower register bit assignments.

Table 5-889: por_mxp_por_dtm_pmu_config_dt$index (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0
19	Reserved	Reserved	RO	-
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

5.3.6.96 por_dtm_pmevcnt_dt$index

This register repeats once. It is parameterized by the $index from 1 to 2. Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

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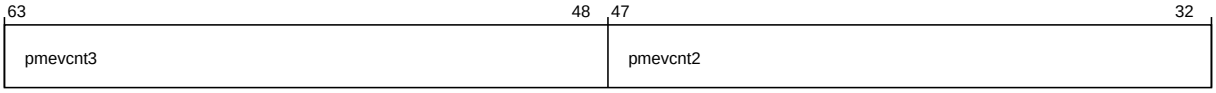
Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h120 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-876: por_mxp_por_dtm_pmevcnt_dt$index (high)



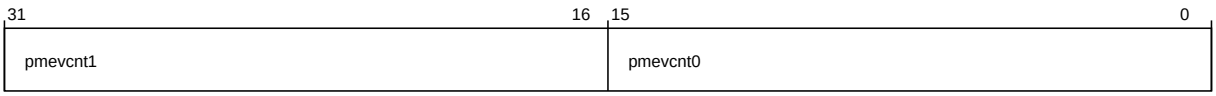
The following table shows the por_dtm_pmevcnt_dt$index higher register bit assignments.

Table 5-890: por_mxp_por_dtm_pmevcnt_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcnt3	PMU event counter 3	RW	16'h0000
47:32	pmevcnt2	PMU event counter 2	RW	16'h0000

The following figure shows the lower register bit assignments.

Figure 5-877: por_mxp_por_dtm_pmevcnt_dt$index (low)



The following table shows the por_dtm_pmevcnt_dt$index lower register bit assignments.

Table 5-891: por_mxp_por_dtm_pmevcnt_dt$index (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcnt1	PMU event counter 1	RW	16'h0000
15:0	pmevcnt0	PMU event counter 0	RW	16'h0000

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5.3.6.97 por_dtm_pmevcntsr_dt$index

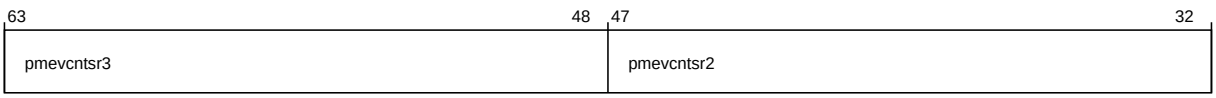
This register repeats once. It is parameterized by the $index from 1 to 2. Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset UNIT_REGISTER_BASE + UNIT_PMU_BASE + 16'h100 + 16'h140 + (512 * $index)
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-878: por_mxp_por_dtm_pmevcntsr_dt$index (high)



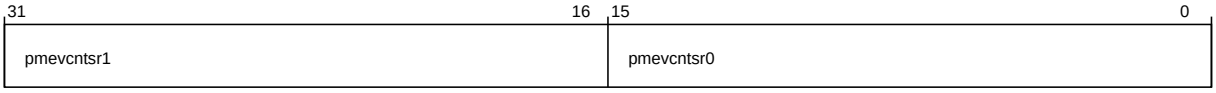
The following table shows the por_dtm_pmevcntsr_dt$index higher register bit assignments.

Table 5-892: por_mxp_por_dtm_pmevcntsr_dt$index (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000

The following figure shows the lower register bit assignments.

Figure 5-879: por_mxp_por_dtm_pmevcntsr_dt$index (low)



The following table shows the por_dtm_pmevcntsr_dt$index lower register bit assignments.

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Table 5-893: por_mxp_por_dtm_pmevcntsr_dt$index (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

5.3.6.98 por_mxp_xy_override_sel_0

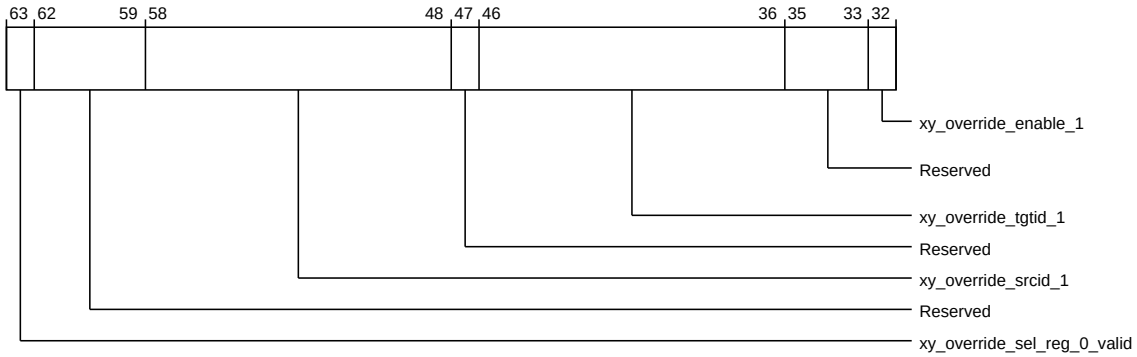
Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-880: por_mxp_por_mxp_xy_override_sel_0 (high)



The following table shows the por_mxp_xy_override_sel_0 higher register bit assignments.

Table 5-894: por_mxp_por_mxp_xy_override_sel_0 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_0_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-

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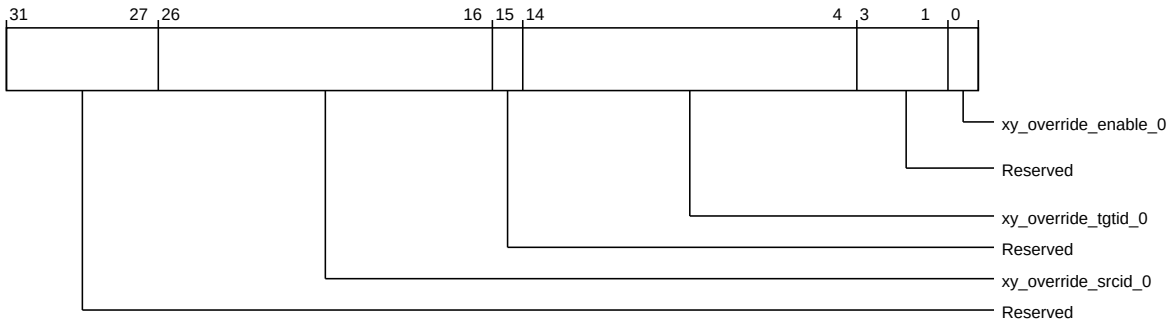
Bits	Field name	Description	Type	Reset
58:48	xy_override_srcid_1	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_1	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_1	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-881: por_mxp_por_mxp_xy_override_sel_0 (low)



The following table shows the por_mxp_xy_override_sel_0 lower register bit assignments.

Table 5-895: por_mxp_por_mxp_xy_override_sel_0 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_0	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_0	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_0	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.6.99 por_mxp_xy_override_sel_1

Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

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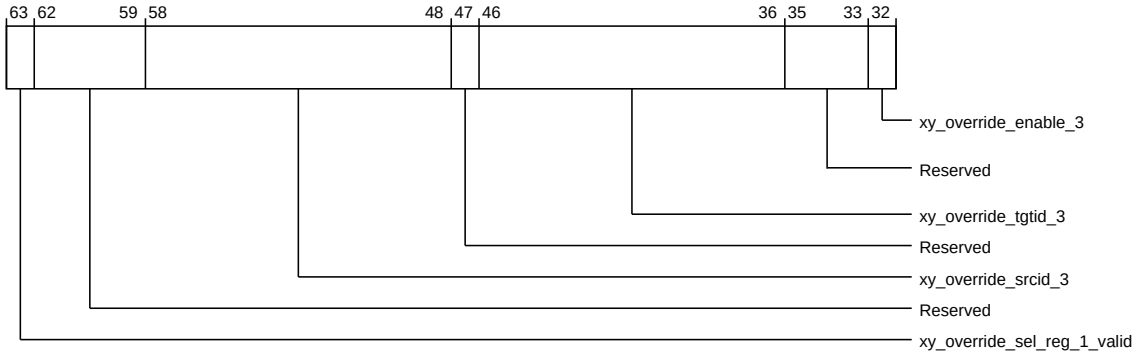
Type RW
Register width (Bits) 64
Address offset 16'hC98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-882: por_mxp_por_mxp_xy_override_sel_1 (high)



The following table shows the por_mxp_xy_override_sel_1 higher register bit assignments.

Table 5-896: por_mxp_por_mxp_xy_override_sel_1 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_1_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_3	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_3	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_3	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

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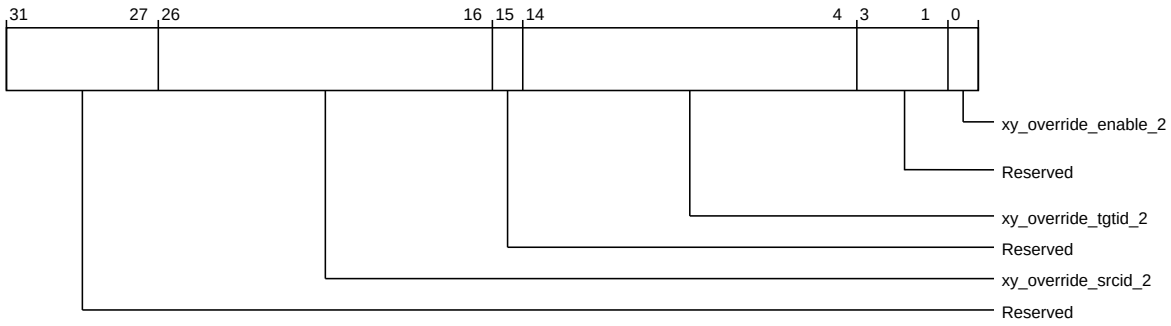
Figure 5-883: por_mxp_por_mxp_xy_override_sel_1 (low)



The following table shows the por_mxp_xy_override_sel_1 lower register bit assignments.

Table 5-897: por_mxp_por_mxp_xy_override_sel_1 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_2	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_2	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_2	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.6.100 por_mxp_xy_override_sel_2

Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

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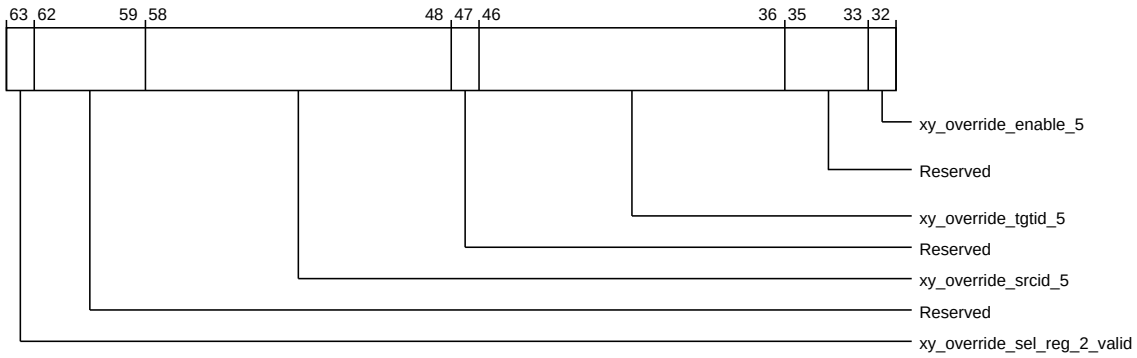
Figure 5-884: por_mxp_por_mxp_xy_override_sel_2 (high)



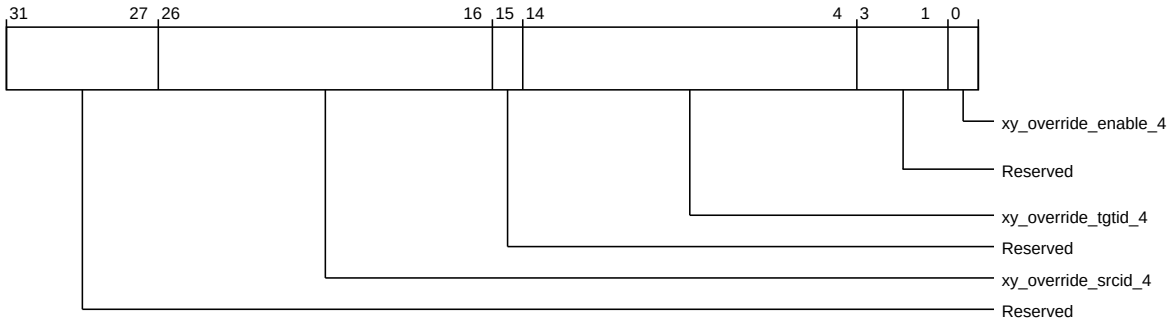
The following table shows the por_mxp_xy_override_sel_2 higher register bit assignments.

Table 5-898: por_mxp_por_mxp_xy_override_sel_2 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_2_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_5	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_5	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_5	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-885: por_mxp_por_mxp_xy_override_sel_2 (low)



The following table shows the por_mxp_xy_override_sel_2 lower register bit assignments.

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Table 5-899: por_mxp_por_mxp_xy_override_sel_2 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_4	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_4	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_4	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.6.101 por_mxp_xy_override_sel_3

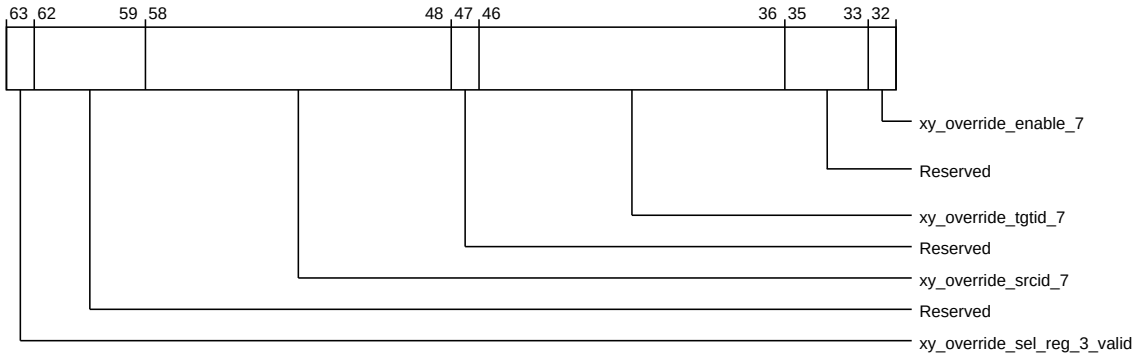
Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-886: por_mxp_por_mxp_xy_override_sel_3 (high)



The following table shows the por_mxp_xy_override_sel_3 higher register bit assignments.

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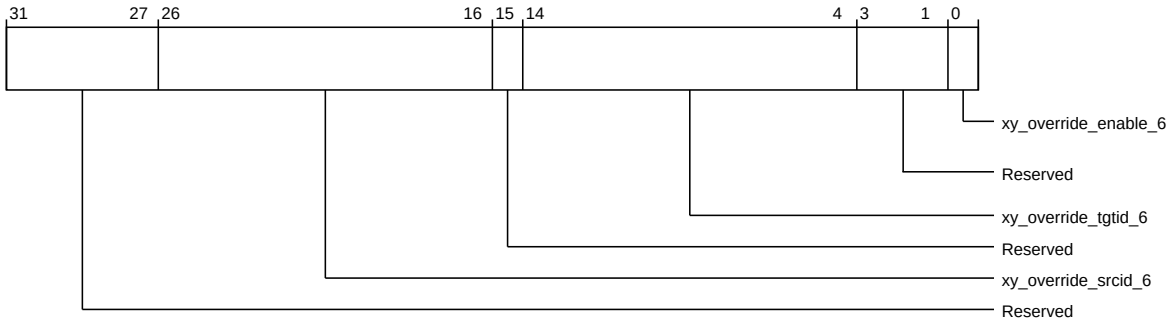
Table 5-900: por_mxp_por_mxp_xy_override_sel_3 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_3_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_7	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_7	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_7	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-887: por_mxp_por_mxp_xy_override_sel_3 (low)



The following table shows the por_mxp_xy_override_sel_3 lower register bit assignments.

Table 5-901: por_mxp_por_mxp_xy_override_sel_3 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_6	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_6	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_6	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

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5.3.6.102 por_mxp_xy_override_sel_4

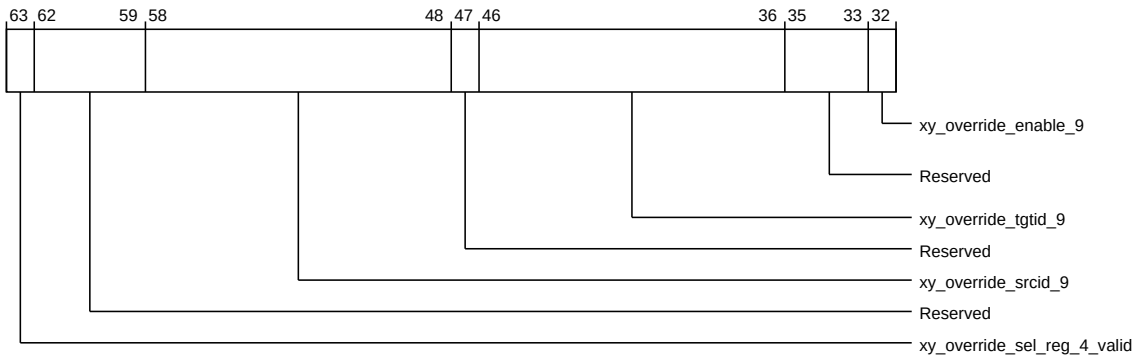
Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-888: por_mxp_por_mxp_xy_override_sel_4 (high)



The following table shows the por_mxp_xy_override_sel_4 higher register bit assignments.

Table 5-902: por_mxp_por_mxp_xy_override_sel_4 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_4_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_9	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_9	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_9	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

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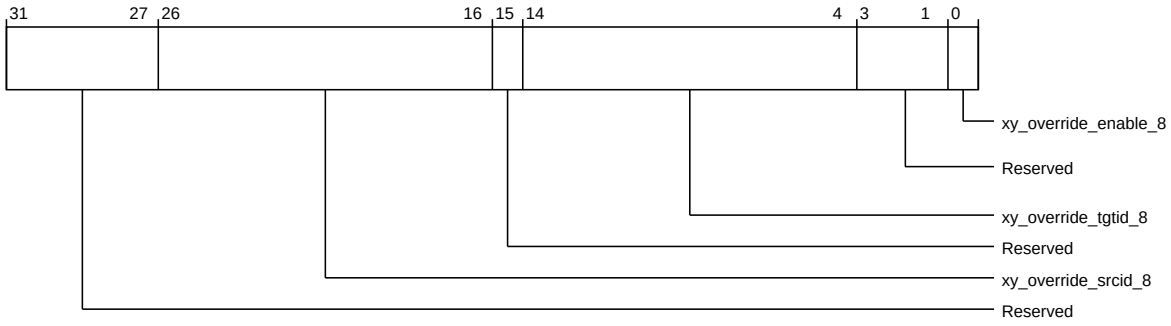
The following figure shows the lower register bit assignments.

Figure 5-889: por_mxp_por_mxp_xy_override_sel_4 (low)



The following table shows the por_mxp_xy_override_sel_4 lower register bit assignments.

Table 5-903: por_mxp_por_mxp_xy_override_sel_4 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_8	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_8	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_8	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.6.103 por_mxp_xy_override_sel_5

Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

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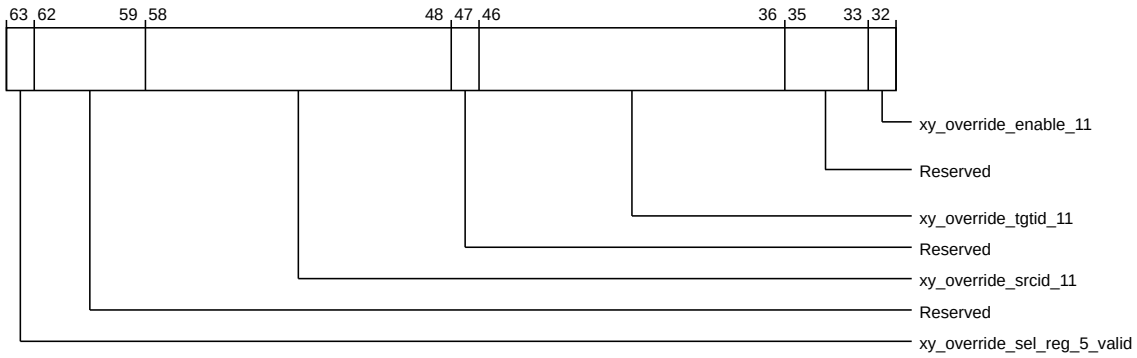
Figure 5-890: por_mxp_por_mxp_xy_override_sel_5 (high)



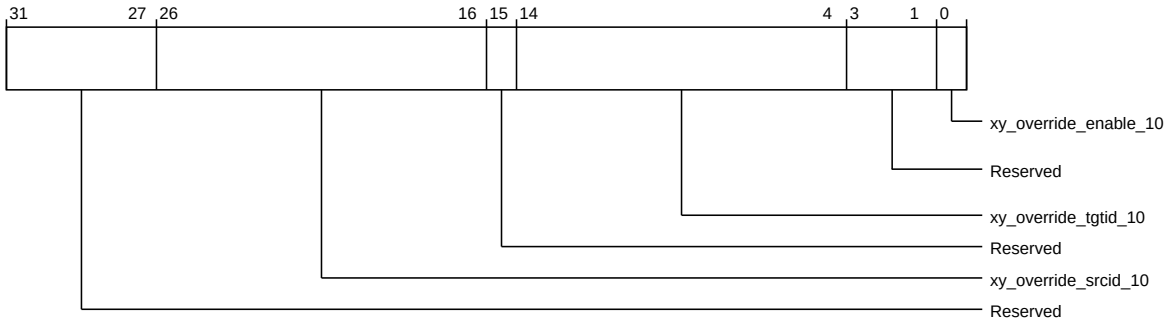
The following table shows the por_mxp_xy_override_sel_5 higher register bit assignments.

Table 5-904: por_mxp_por_mxp_xy_override_sel_5 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_5_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_11	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_11	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_11	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-891: por_mxp_por_mxp_xy_override_sel_5 (low)



The following table shows the por_mxp_xy_override_sel_5 lower register bit assignments.

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Table 5-905: por_mxp_por_mxp_xy_override_sel_5 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_10	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_10	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_10	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.6.104 por_mxp_xy_override_sel_6

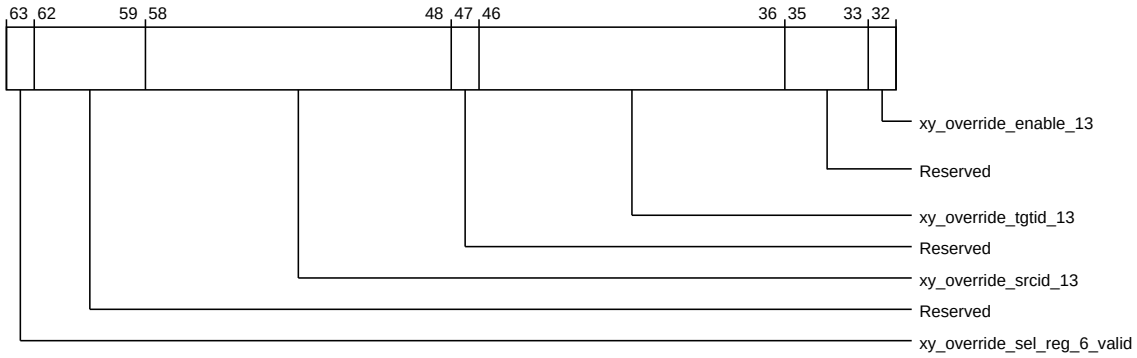
Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-892: por_mxp_por_mxp_xy_override_sel_6 (high)



The following table shows the por_mxp_xy_override_sel_6 higher register bit assignments.

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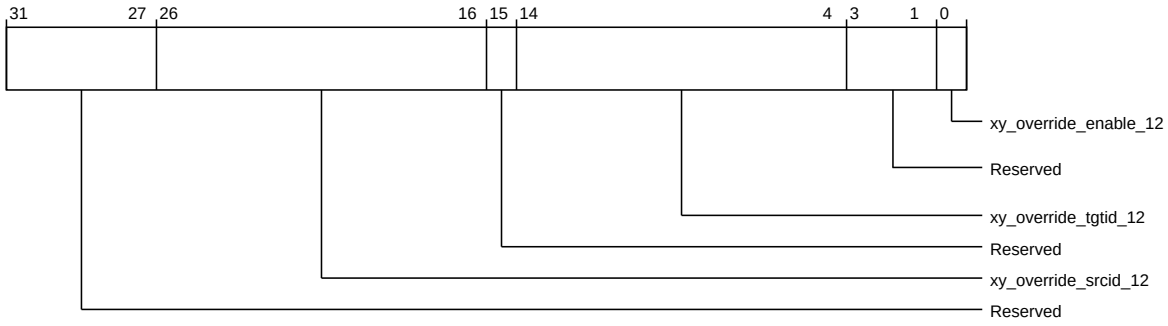
Table 5-906: por_mxp_por_mxp_xy_override_sel_6 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_6_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_13	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_13	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_13	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-893: por_mxp_por_mxp_xy_override_sel_6 (low)



The following table shows the por_mxp_xy_override_sel_6 lower register bit assignments.

Table 5-907: por_mxp_por_mxp_xy_override_sel_6 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_12	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_12	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_12	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

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5.3.6.105 por_mxp_xy_override_sel_7

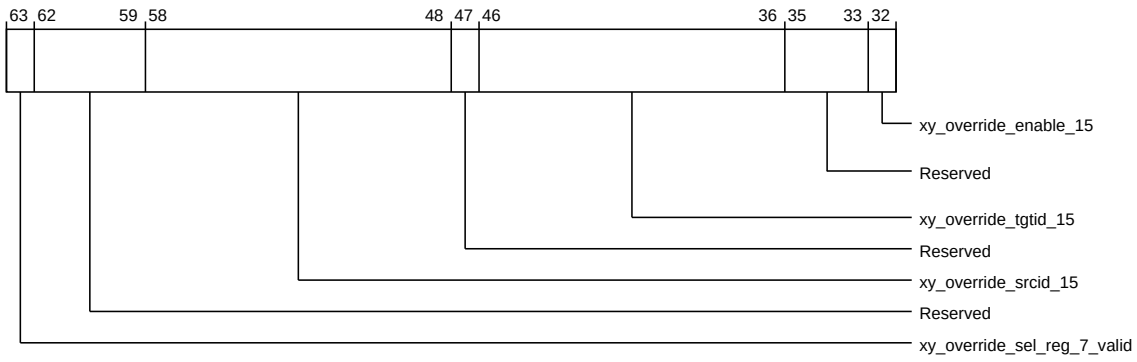
Functions as SRC-TGT pair whose X-Y route path can be overriden (for Non-XY Route feature per Souce-Target pair) per XP.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hCC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mxp_secure_register_groups_override.xy_override_ctl

The following figure shows the higher register bit assignments.

Figure 5-894: por_mxp_por_mxp_xy_override_sel_7 (high)



The following table shows the por_mxp_xy_override_sel_7 higher register bit assignments.

Table 5-908: por_mxp_por_mxp_xy_override_sel_7 (high)

Bits	Field name	Description	Type	Reset
63	xy_override_sel_reg_7_valid	Indicates that Source-Target pairs whose X-Y route path can be overriden are configured in this register.	RW	1'b0
62:59	Reserved	Reserved	RO	-
58:48	xy_override_srcid_15	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	xy_override_tgtid_15	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
35:33	Reserved	Reserved	RO	-
32	xy_override_enable_15	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

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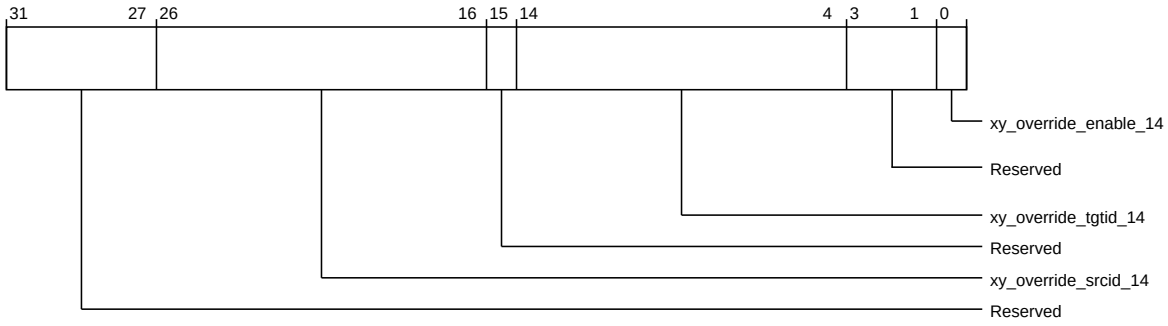
The following figure shows the lower register bit assignments.

Figure 5-895: por_mxp_por_mxp_xy_override_sel_7 (low)



The following table shows the por_mxp_xy_override_sel_7 lower register bit assignments.

Table 5-909: por_mxp_por_mxp_xy_override_sel_7 (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	xy_override_srcid_14	11-bit Source ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
15	Reserved	Reserved	RO	-
14:4	xy_override_tgtid_14	11-bit Target ID associated with the XY Override. This field is used in the LUP to determine if XY route for the associated source-target pair needs to be overriden.	RW	11'b0
3:1	Reserved	Reserved	RO	-
0	xy_override_enable_14	X-Y Route Override Enable: 1 - X-Y Route override enabled for associated Source-Target Pair, 0 - X-Y Route override disabled	RW	1'b0

5.3.7 RN-D register descriptions

This section lists the RN-D registers.

5.3.7.1 por_rnd_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

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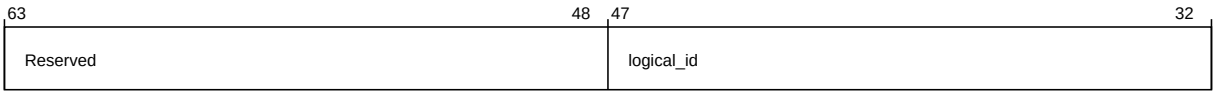
The following figure shows the higher register bit assignments.

Figure 5-896: por_rnd_por_rnd_node_info (high)



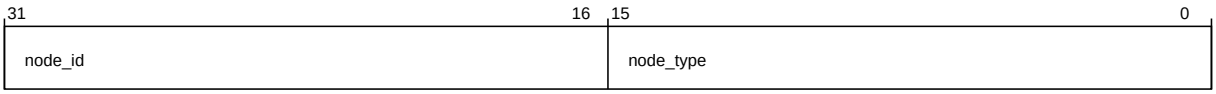
The following table shows the por_rnd_node_info higher register bit assignments.

Table 5-910: por_rnd_por_rnd_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-897: por_rnd_por_rnd_node_info (low)



The following table shows the por_rnd_node_info lower register bit assignments.

Table 5-911: por_rnd_por_rnd_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h000D

5.3.7.2 por_rnd_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0

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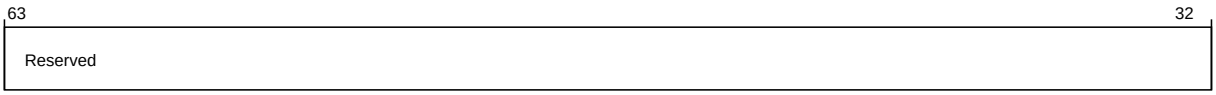
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-898: por_rnd_por_rnd_child_info (high)



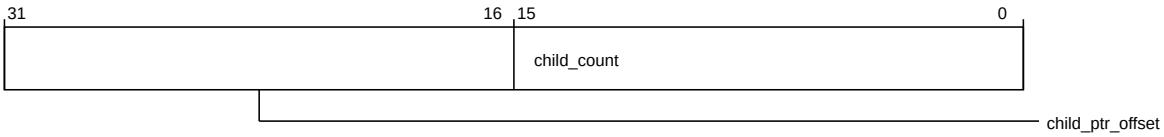
The following table shows the por_rnd_child_info higher register bit assignments.

Table 5-912: por_rnd_por_rnd_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-899: por_rnd_por_rnd_child_info (low)



The following table shows the por_rnd_child_info lower register bit assignments.

Table 5-913: por_rnd_por_rnd_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

5.3.7.3 por_rnd_secure_register_groups_override

Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0

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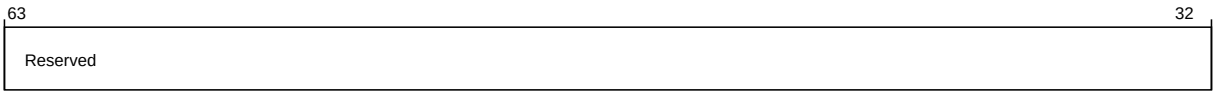
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-900: por_rnd_por_rnd_secure_register_groups_override (high)



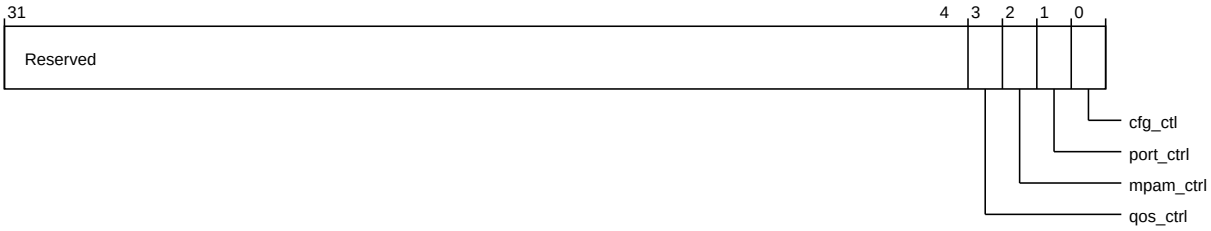
The following table shows the por_rnd_secure_register_groups_override higher register bit assignments.

Table 5-914: por_rnd_por_rnd_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-901: por_rnd_por_rnd_secure_register_groups_override (low)



The following table shows the por_rnd_secure_register_groups_override lower register bit assignments.

Table 5-915: por_rnd_por_rnd_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	qos_ctrl	Allows Non-secure access to Secure QoS control registers	RW	1'b0
2	mpam_ctrl	Allows Non-secure access to Secure AXI port MPAM override register	RW	1'b0
1	port_ctrl	Allows Non-secure access to Secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

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5.3.7.4 por_rnd_unit_info

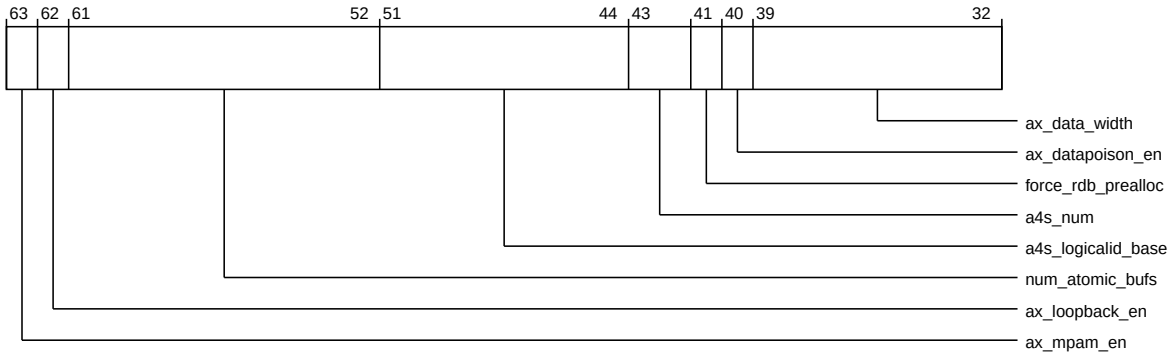
Provides component identification information for RN-D.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-902: por_rnd_por_rnd_unit_info (high)



The following table shows the por_rnd_unit_info higher register bit assignments.

Table 5-916: por_rnd_por_rnd_unit_info (high)

Bits	Field name	Description	Type	Reset
63	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
62	ax_loopback_en	LoopBack enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
61:52	num_atomic_bufs	Number of atomic data buffers	RO	Configuration dependent
51:44	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
43:42	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent

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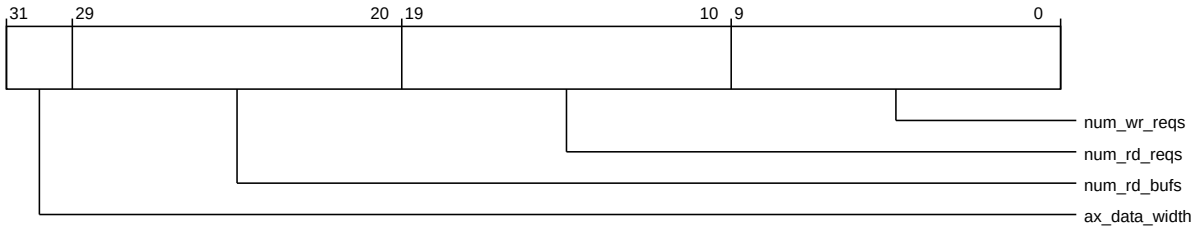
Bits	Field name	Description	Type	Reset
41	force_rdb_prealloc	Force read data buffer preallocation 1'b1: yes 1'b0: no	RO	Configuration dependent
40	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
39:32	ax_data_width	AXI interface data width in bits	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-903: por_rnd_por_rnd_unit_info (low)



The following table shows the por_rnd_unit_info lower register bit assignments.

Table 5-917: por_rnd_por_rnd_unit_info (low)

Bits	Field name	Description	Type	Reset
31:30	ax_data_width	AXI interface data width in bits	RO	Configuration dependent
29:20	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
19:10	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
9:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

5.3.7.5 por_rnd_unit_info2

Provides additonal component identification information for RN-D.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h908
Register reset Configuration dependent
Usage constraints There are no usage constraints.

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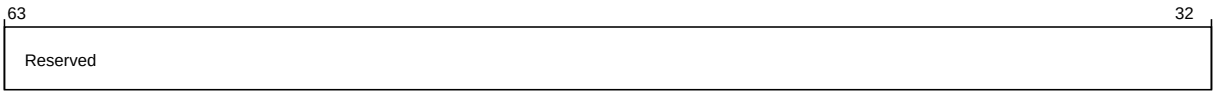
The following figure shows the higher register bit assignments.

Figure 5-904: por_rnd_por_rnd_unit_info2 (high)



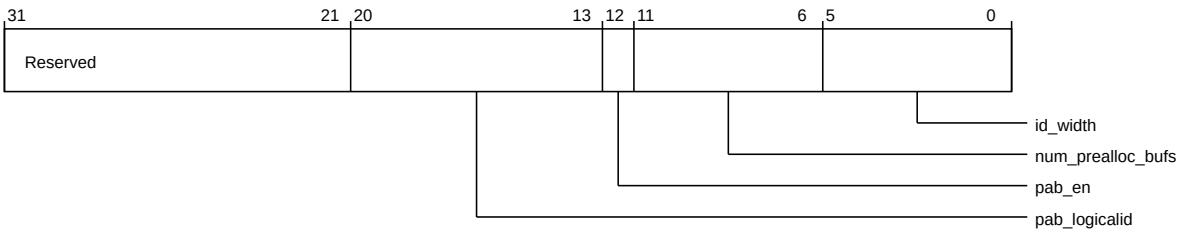
The following table shows the por_rnd_unit_info2 higher register bit assignments.

Table 5-918: por_rnd_por_rnd_unit_info2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-905: por_rnd_por_rnd_unit_info2 (low)



The following table shows the por_rnd_unit_info2 lower register bit assignments.

Table 5-919: por_rnd_por_rnd_unit_info2 (low)

Bits	Field name	Description	Type	Reset
31:21	Reserved	Reserved	RO	-
20:13	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
12	pab_en	PUB AUB bridge enable 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
11:6	num_prealloc_bufs	Number of Pre-allocated Read Data Buffers	RO	Configuration dependent
5:0	id_width	AXI ID width for ACE-Lite slave ports	RO	Configuration dependent

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5.3.7.6 por_rnd_cfg_ctl

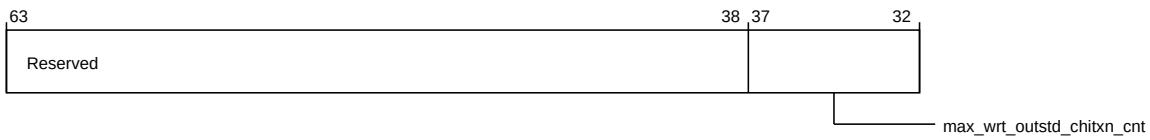
Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

Figure 5-906: por_rnd_por_rnd_cfg_ctl (high)



The following table shows the por_rnd_cfg_ctl higher register bit assignments.

Table 5-920: por_rnd_por_rnd_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent

The following figure shows the lower register bit assignments.

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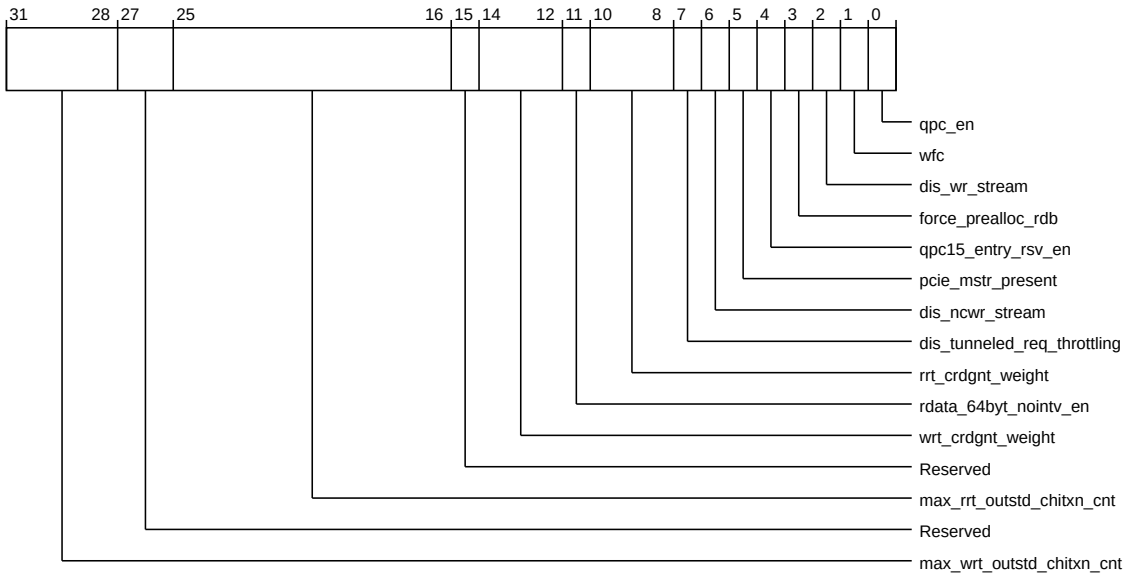
Figure 5-907: por_rnd_por_rnd_cfg_ctl (low)



The following table shows the por_rnd_cfg_ctl lower register bit assignments.

Table 5-921: por_rnd_por_rnd_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:28	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
27:26	Reserved	Reserved	RO	-
25:16	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	rdata_64byt_nointv_en	Enables no interleaving property on normal memory read data within 64B granule when set	RW	1'b1
10:8	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	dis_tunneled_req_throttling	Disables retry based throttling of tunneled write requests	RW	1'b0
6	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	pcie_mstr_present	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0
4	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rnd_qpc_en is set	RW	1'b0

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Bits	Field name	Description	Type	Reset
3	force_prealloc_rdb	When set, all reads from the RN-D are sent with a preallocated read data buffer	RW	Configuration dependent
2	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
1	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

5.3.7.7 por_rnd_aux_ctl

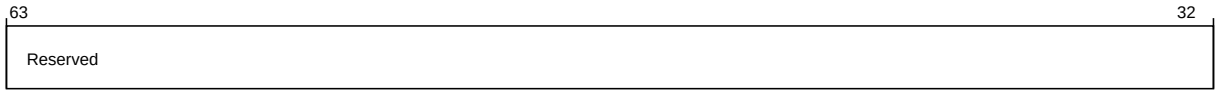
Functions as the auxiliary control register for RN-D.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-908: por_rnd_por_rnd_aux_ctl (high)



The following table shows the por_rnd_aux_ctl higher register bit assignments.

Table 5-922: por_rnd_por_rnd_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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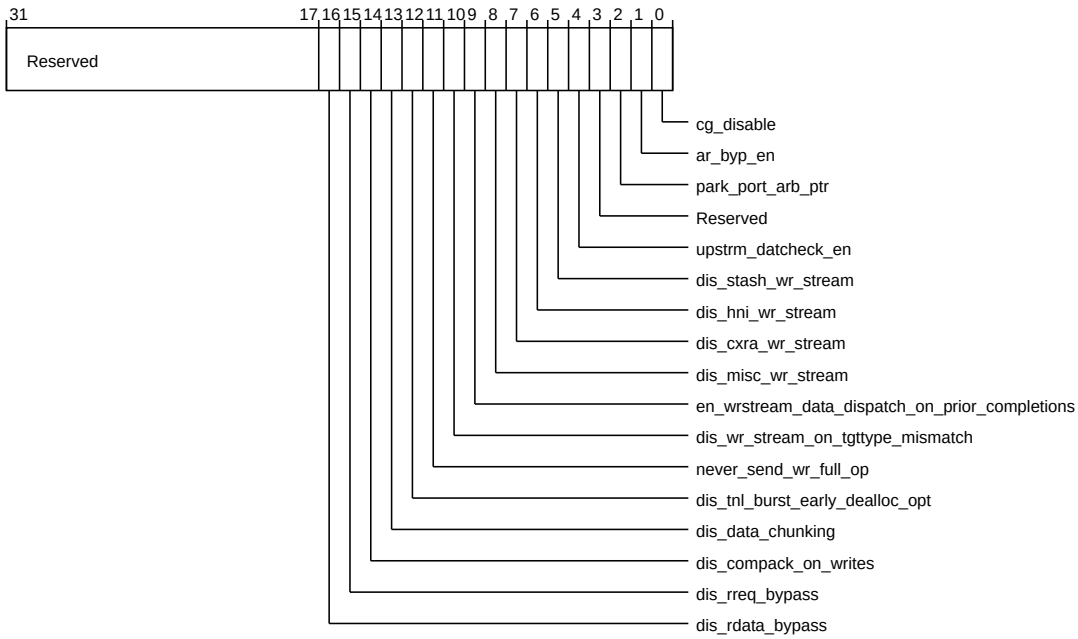
Figure 5-909: por_rnd_por_rnd_aux_ctl (low)



The following table shows the por_rnd_aux_ctl lower register bit assignments.

Table 5-923: por_rnd_por_rnd_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	dis_rdata_bypass	If set, disables read data bypass path	RW	1'b0
15	dis_rreq_bypass	If set, disables read request bypass path	RW	1'b0
14	dis_compack_on_writes	If set, disables comp_ack on streaming writes. WrData is used for ordering writes	RW	1'b1
13	dis_data_chunking	If set, disables the data chunking feature	RW	1'b0
12	dis_tnl_burst_early_dealloc_opt	If set, disables the optimization related to early deallocation of tunnelled writes for intermediate txns of burst	RW	1'b1
11	never_send_wr_full_op	If set, RNI will never send WR FULL op. All write ops will be of PTL type	RW	1'b0
10	dis_wr_stream_on_tgttype_mismatch	If set, serializes first write when moving from one tgttype to another	RW	1'b0
9	en_wrstream_data_dispatch_on_prior_completions	If set, data dispatch for streaming writes waits for completion of all older writes	RW	1'b0
8	dis_misc_wr_stream	Disables streaming of ordered writes with following attributes when set : Device memory or EWA=0 or Excl=1	RW	1'b0
7	dis_cxra_wr_stream	Disables streaming of ordered writes to CXRA when set	RW	1'b0
6	dis_hni_wr_stream	Disables streaming of ordered writes to HNI when set	RW	1'b0

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Bits	Field name	Description	Type	Reset
5	dis_stash_wr_stream	Disables streaming of ordered WrUniqStash when set	RW	1'b0
4	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
3	Reserved	Reserved	RO	-
2	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	cg_disable	Disables clock gating when set	RW	1'b0

5.3.7.8 por_rnd_s0_port_control

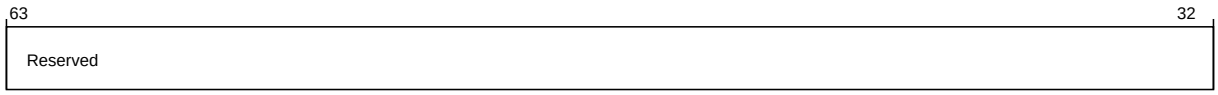
Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

Figure 5-910: por_rnd_por_rnd_s0_port_control (high)



The following table shows the por_rnd_s0_port_control higher register bit assignments.

Table 5-924: por_rnd_por_rnd_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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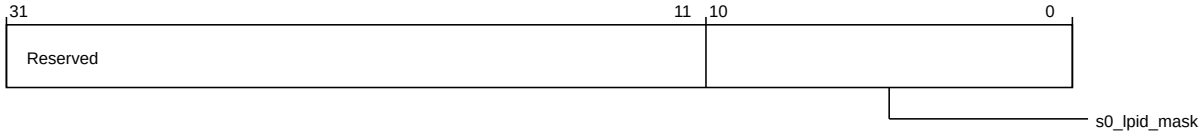
Figure 5-911: por_rnd_por_rnd_s0_port_control (low)



The following table shows the por_rnd_s0_port_control lower register bit assignments.

Table 5-925: por_rnd_por_rnd_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

5.3.7.9 por_rnd_s1_port_control

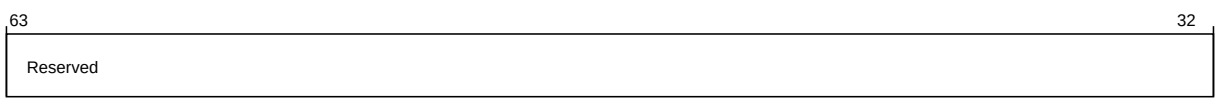
Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

Figure 5-912: por_rnd_por_rnd_s1_port_control (high)



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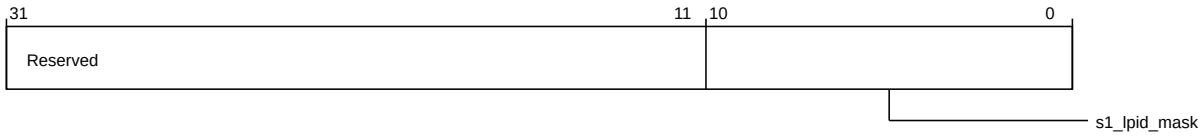
The following table shows the por_rnd_s1_port_control higher register bit assignments.

Table 5-926: por_rnd_por_rnd_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-913: por_rnd_por_rnd_s1_port_control (low)



The following table shows the por_rnd_s1_port_control lower register bit assignments.

Table 5-927: por_rnd_por_rnd_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

5.3.7.10 por_rnd_s2_port_control

Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

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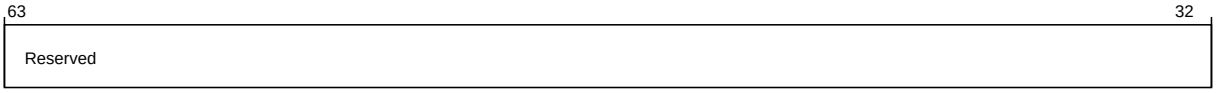
Figure 5-914: por_rnd_por_rnd_s2_port_control (high)



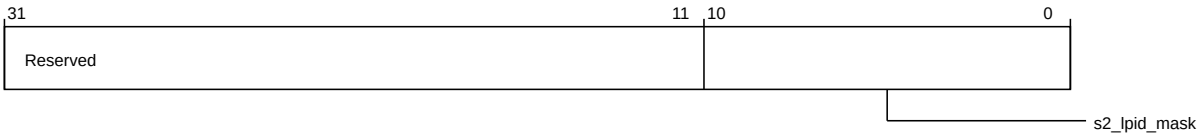
The following table shows the por_rnd_s2_port_control higher register bit assignments.

Table 5-928: por_rnd_por_rnd_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-915: por_rnd_por_rnd_s2_port_control (low)



The following table shows the por_rnd_s2_port_control lower register bit assignments.

Table 5-929: por_rnd_por_rnd_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

5.3.7.11 por_rnd_s0_mpam_control

Controls port S0 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA28

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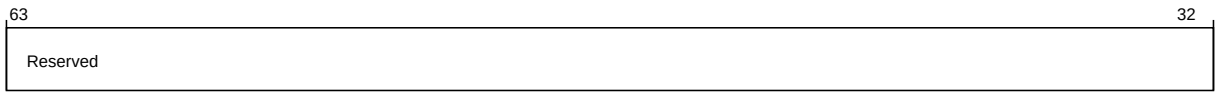
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-916: por_rnd_por_rnd_s0_mpam_control (high)



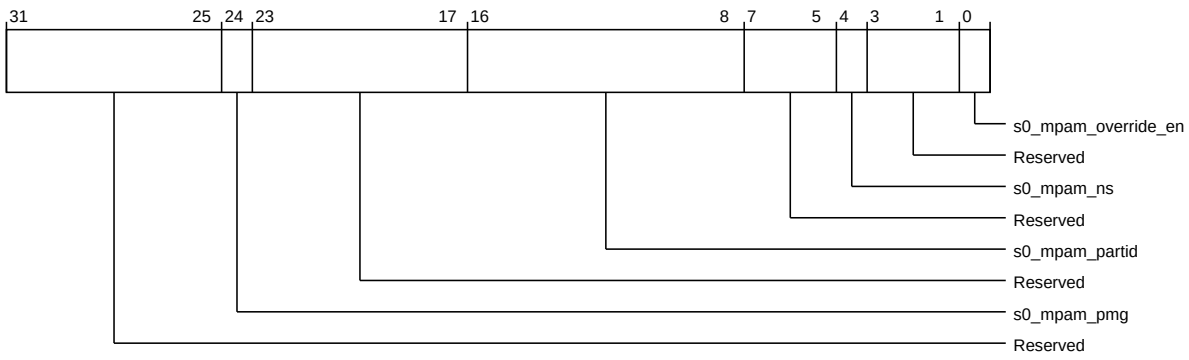
The following table shows the por_rnd_s0_mpam_control higher register bit assignments.

Table 5-930: por_rnd_por_rnd_s0_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-917: por_rnd_por_rnd_s0_mpam_control (low)



The following table shows the por_rnd_s0_mpam_control lower register bit assignments.

Table 5-931: por_rnd_por_rnd_s0_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s0_mpam_pmg	Port S0 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s0_mpam_partid	Port S0 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4	s0_mpam_ns	Port S0 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	s0_mpam_override_en	Port S0 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.7.12 por_rnd_s1_mpam_control

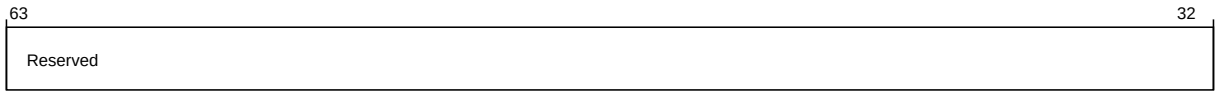
Controls port S1 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-918: por_rnd_por_rnd_s1_mpam_control (high)



The following table shows the por_rnd_s1_mpam_control higher register bit assignments.

Table 5-932: por_rnd_por_rnd_s1_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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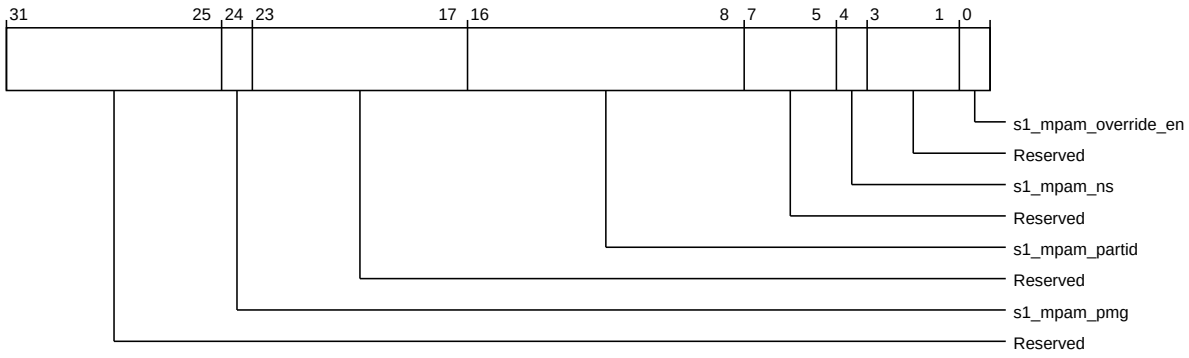
Figure 5-919: por_rnd_por_rnd_s1_mpam_control (low)



The following table shows the por_rnd_s1_mpam_control lower register bit assignments.

Table 5-933: por_rnd_por_rnd_s1_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s1_mpam_pmg	Port S1 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s1_mpam_partid	Port S1 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	s1_mpam_ns	Port S1 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	s1_mpam_override_en	Port S1 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.7.13 por_rnd_s2_mpam_control

Controls port S2 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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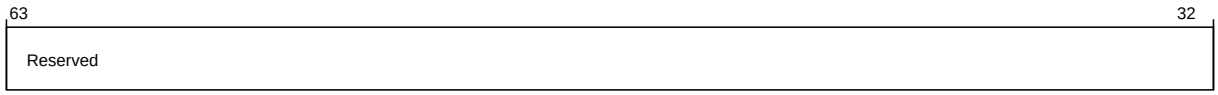
Secure group override por_rnd_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-920: por_rnd_por_rnd_s2_mpam_control (high)



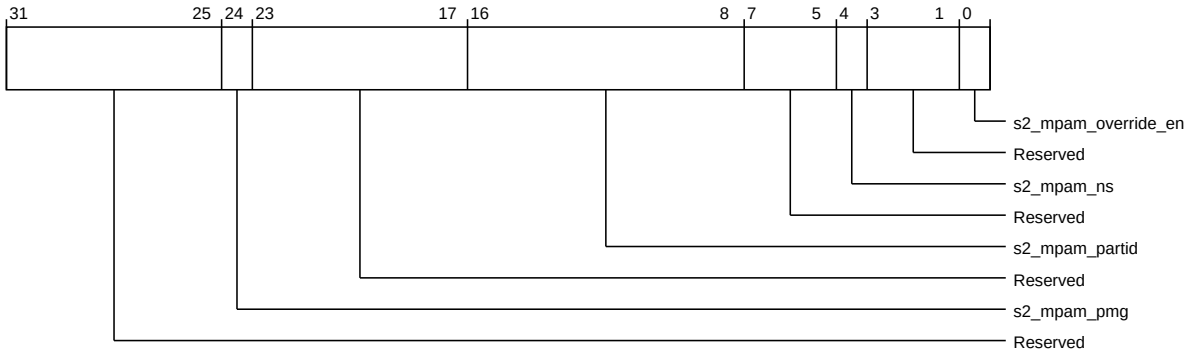
The following table shows the por_rnd_s2_mpam_control higher register bit assignments.

Table 5-934: por_rnd_por_rnd_s2_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-921: por_rnd_por_rnd_s2_mpam_control (low)



The following table shows the por_rnd_s2_mpam_control lower register bit assignments.

Table 5-935: por_rnd_por_rnd_s2_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s2_mpam_pmg	Port S2 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s2_mpam_partid	Port S2 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	s2_mpam_ns	Port S2 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	s2_mpam_override_en	Port S2 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.7.14 por_rnd_s0_qos_control

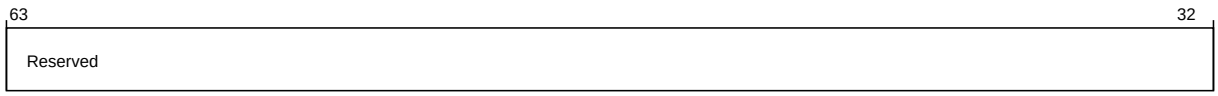
Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-922: por_rnd_por_rnd_s0_qos_control (high)



The following table shows the por_rnd_s0_qos_control higher register bit assignments.

Table 5-936: por_rnd_por_rnd_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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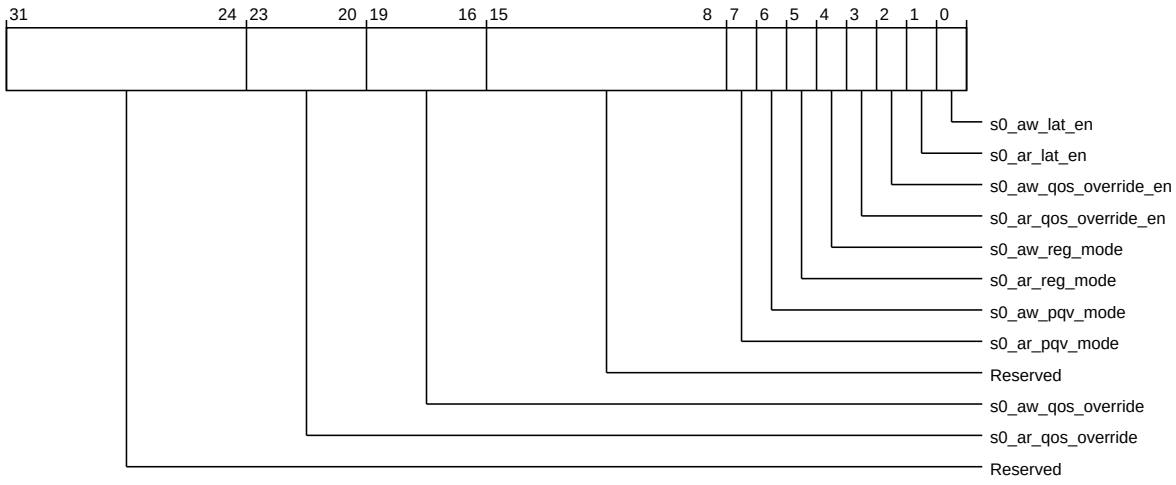
Figure 5-923: por_rnd_por_rnd_s0_qos_control (low)



The following table shows the por_rnd_s0_qos_control lower register bit assignments.

Table 5-937: por_rnd_por_rnd_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s0_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s0_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s0_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0

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Bits	Field name	Description	Type	Reset
3	s0_ar_qos_override_en	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s0_aw_qos_override_en	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s0_ar_lat_en	Enables port S0 AR QoS regulation when set	RW	1'b0
0	s0_aw_lat_en	Enables port S0 AW QoS regulation when set	RW	1'b0

5.3.7.15 por_rnd_s0_qos_lat_tgt

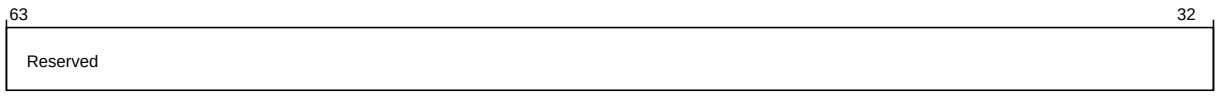
Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-924: por_rnd_por_rnd_s0_qos_lat_tgt (high)



The following table shows the por_rnd_s0_qos_lat_tgt higher register bit assignments.

Table 5-938: por_rnd_por_rnd_s0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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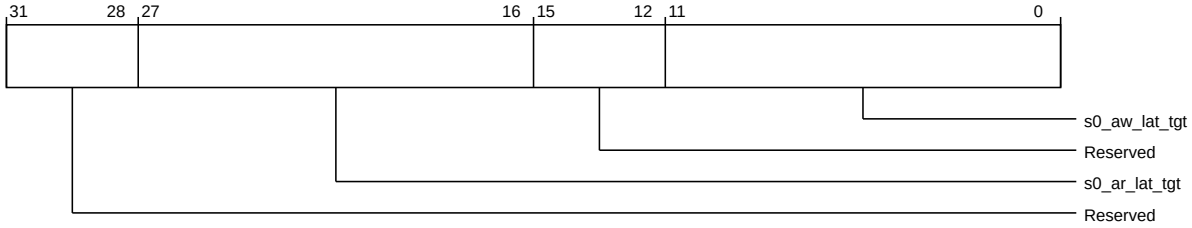
Figure 5-925: por_rnd_por_rnd_s0_qos_lat_tgt (low)



The following table shows the por_rnd_s0_qos_lat_tgt lower register bit assignments.

Table 5-939: por_rnd_por_rnd_s0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s0_ar_lat_tgt	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s0_aw_lat_tgt	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.7.16 por_rnd_s0_qos_lat_scale

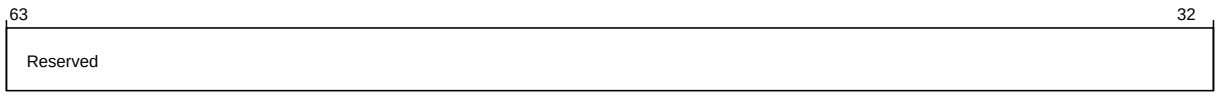
Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-926: por_rnd_por_rnd_s0_qos_lat_scale (high)



The following table shows the por_rnd_s0_qos_lat_scale higher register bit assignments.

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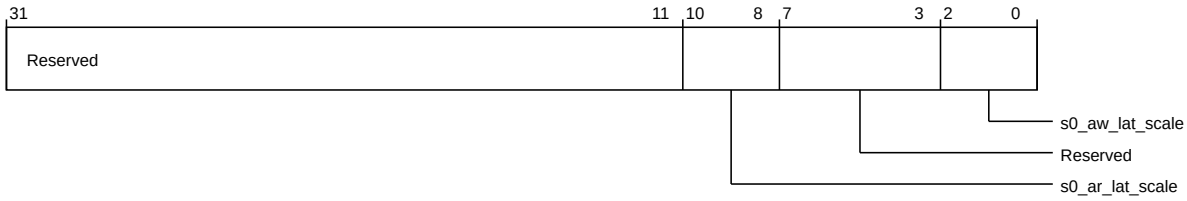
Table 5-940: por_rnd_por_rnd_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-927: por_rnd_por_rnd_s0_qos_lat_scale (low)



The following table shows the por_rnd_s0_qos_lat_scale lower register bit assignments.

Table 5-941: por_rnd_por_rnd_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.7.17 por_rnd_s0_qos_lat_range

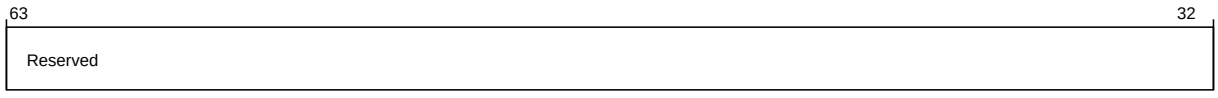
Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-928: por_rnd_por_rnd_s0_qos_lat_range (high)



The following table shows the por_rnd_s0_qos_lat_range higher register bit assignments.

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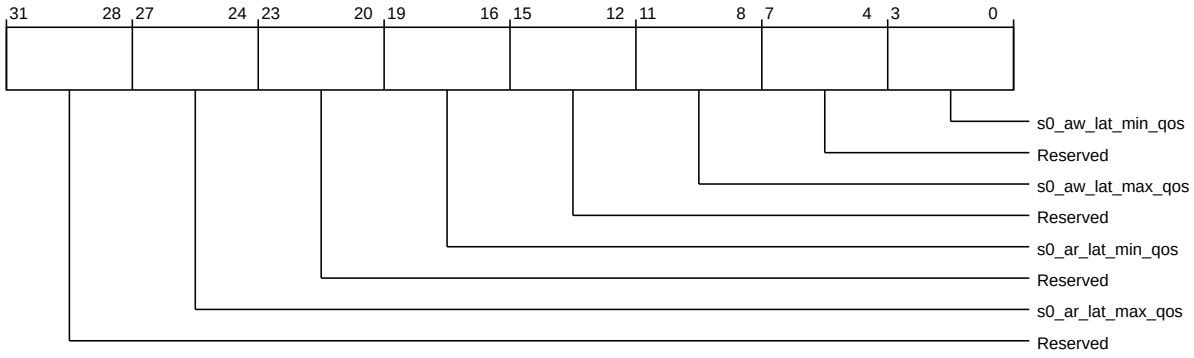
Table 5-942: por_rnd_por_rnd_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-929: por_rnd_por_rnd_s0_qos_lat_range (low)



The following table shows the por_rnd_s0_qos_lat_range lower register bit assignments.

Table 5-943: por_rnd_por_rnd_s0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s0_ar_lat_max_qos	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s0_ar_lat_min_qos	Port S0 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s0_aw_lat_max_qos	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s0_aw_lat_min_qos	Port S0 AW QoS minimum value	RW	4'h0

5.3.7.18 por_rnd_s1_qos_control

Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAA0
Register reset 64'b0

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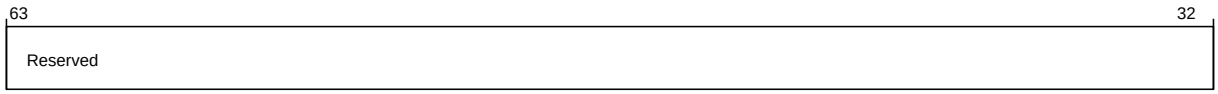
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-930: por_rnd_por_rnd_s1_qos_control (high)



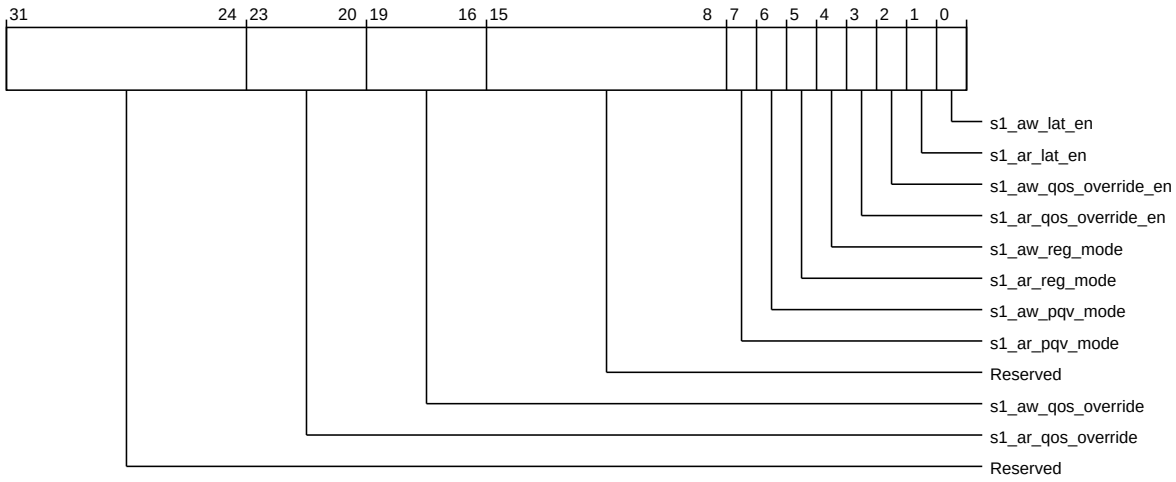
The following table shows the por_rnd_s1_qos_control higher register bit assignments.

Table 5-944: por_rnd_por_rnd_s1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-931: por_rnd_por_rnd_s1_qos_control (low)



The following table shows the por_rnd_s1_qos_control lower register bit assignments.

Table 5-945: por_rnd_por_rnd_s1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s1_ar_qos_override	AR QoS override value for port S1	RW	4'b0000
19:16	s1_aw_qos_override	AW QoS override value for port S1	RW	4'b0000

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Bits	Field name	Description	Type	Reset
15:8	Reserved	Reserved	RO	-
7	s1_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s1_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s1_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s1_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s1_ar_qos_override_en	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s1_aw_qos_override_en	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s1_ar_lat_en	Enables port S1 AR QoS regulation when set	RW	1'b0
0	s1_aw_lat_en	Enables port S1 AW QoS regulation when set	RW	1'b0

5.3.7.19 por_rnd_s1_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

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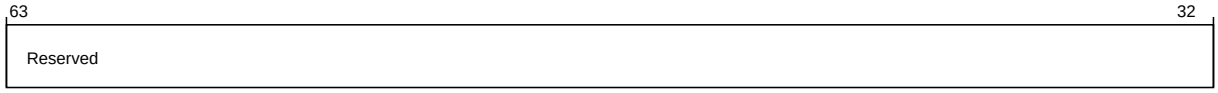
Figure 5-932: por_rnd_por_rnd_s1_qos_lat_tgt (high)



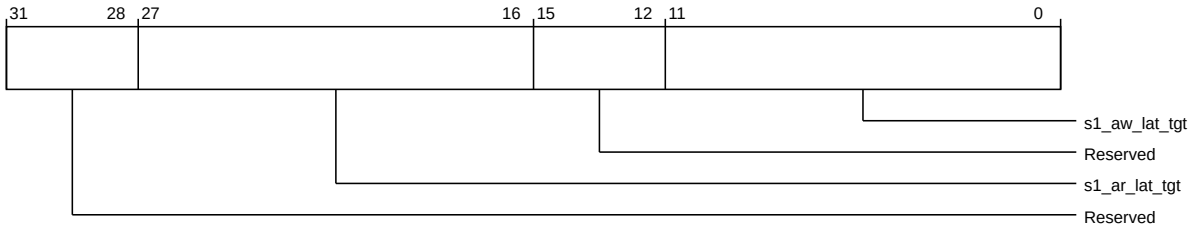
The following table shows the por_rnd_s1_qos_lat_tgt higher register bit assignments.

Table 5-946: por_rnd_por_rnd_s1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-933: por_rnd_por_rnd_s1_qos_lat_tgt (low)



The following table shows the por_rnd_s1_qos_lat_tgt lower register bit assignments.

Table 5-947: por_rnd_por_rnd_s1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s1_ar_lat_tgt	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s1_aw_lat_tgt	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.7.20 por_rnd_s1_qos_lat_scale

Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAB0

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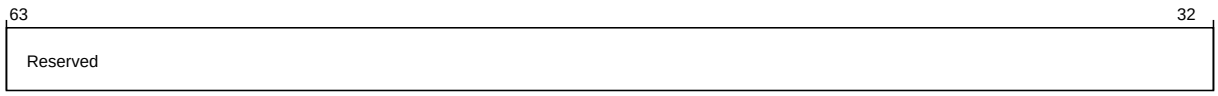
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-934: por_rnd_por_rnd_s1_qos_lat_scale (high)



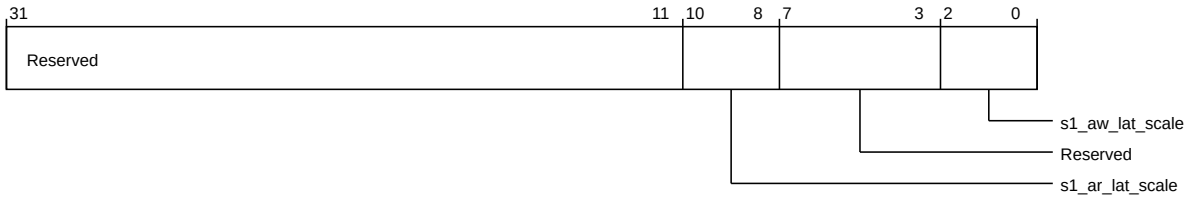
The following table shows the por_rnd_s1_qos_lat_scale higher register bit assignments.

Table 5-948: por_rnd_por_rnd_s1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-935: por_rnd_por_rnd_s1_qos_lat_scale (low)



The following table shows the por_rnd_s1_qos_lat_scale lower register bit assignments.

Table 5-949: por_rnd_por_rnd_s1_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:8	s1_ar_lat_scale	Port S1 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s1_aw_lat_scale	Port S1 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.7.21 por_rnd_s1_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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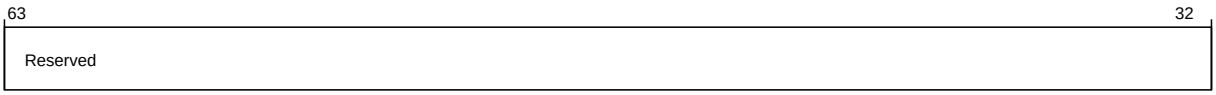
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-936: por_rnd_por_rnd_s1_qos_lat_range (high)



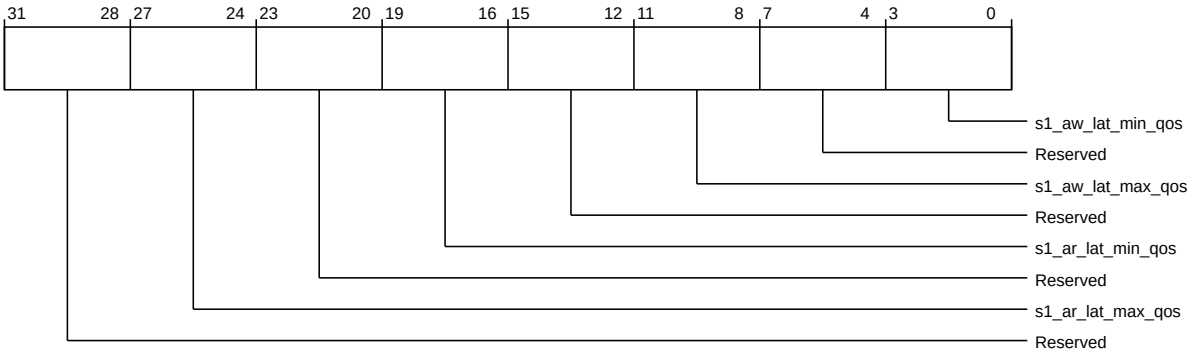
The following table shows the por_rnd_s1_qos_lat_range higher register bit assignments.

Table 5-950: por_rnd_por_rnd_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-937: por_rnd_por_rnd_s1_qos_lat_range (low)



The following table shows the por_rnd_s1_qos_lat_range lower register bit assignments.

Table 5-951: por_rnd_por_rnd_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

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5.3.7.22 por_rnd_s2_qos_control

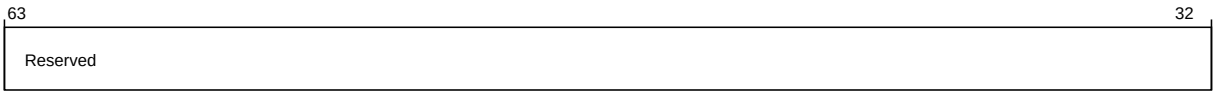
Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-938: por_rnd_por_rnd_s2_qos_control (high)



The following table shows the por_rnd_s2_qos_control higher register bit assignments.

Table 5-952: por_rnd_por_rnd_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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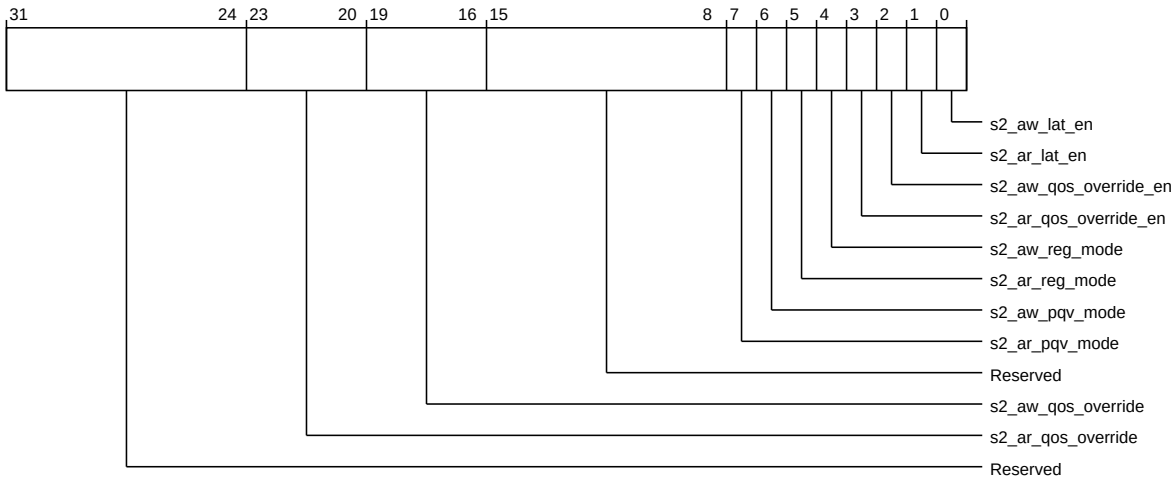
Figure 5-939: por_rnd_por_rnd_s2_qos_control (low)



The following table shows the por_rnd_s2_qos_control lower register bit assignments.

Table 5-953: por_rnd_por_rnd_s2_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s2_ar_qos_override	AR QoS override value for port S2	RW	4'b0000
19:16	s2_aw_qos_override	AW QoS override value for port S2	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s2_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s2_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s2_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s2_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0

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Bits	Field name	Description	Type	Reset
3	s2_ar_qos_override_en	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s2_aw_qos_override_en	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s2_ar_lat_en	Enables port S2 AR QoS regulation when set	RW	1'b0
0	s2_aw_lat_en	Enables port S2 AW QoS regulation when set	RW	1'b0

5.3.7.23 por_rnd_s2_qos_lat_tgt

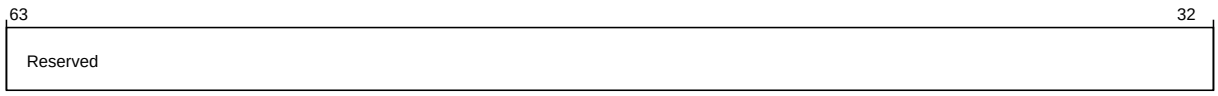
Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-940: por_rnd_por_rnd_s2_qos_lat_tgt (high)



The following table shows the por_rnd_s2_qos_lat_tgt higher register bit assignments.

Table 5-954: por_rnd_por_rnd_s2_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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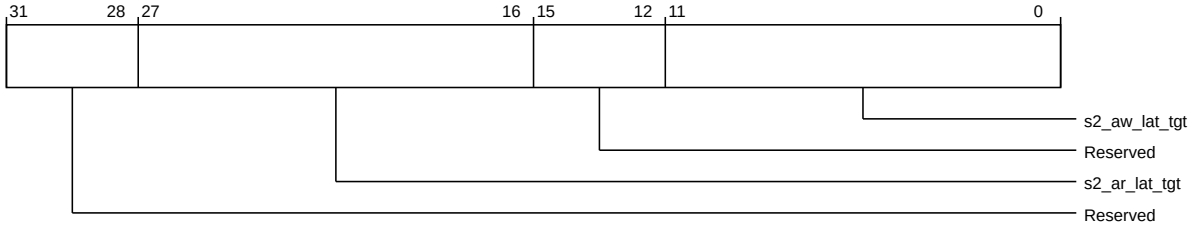
Figure 5-941: por_rnd_por_rnd_s2_qos_lat_tgt (low)



The following table shows the por_rnd_s2_qos_lat_tgt lower register bit assignments.

Table 5-955: por_rnd_por_rnd_s2_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s2_ar_lat_tgt	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s2_aw_lat_tgt	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.7.24 por_rnd_s2_qos_lat_scale

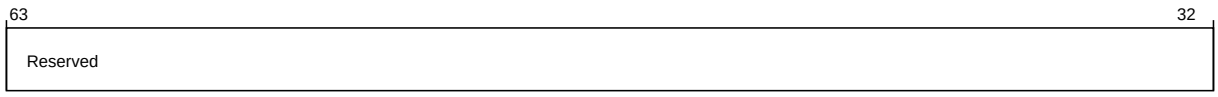
Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAD0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-942: por_rnd_por_rnd_s2_qos_lat_scale (high)



The following table shows the por_rnd_s2_qos_lat_scale higher register bit assignments.

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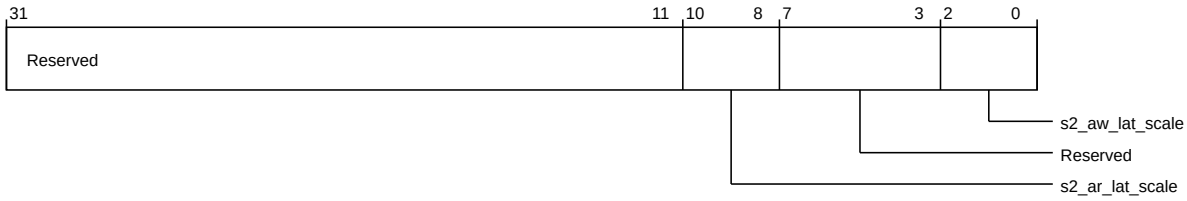
Table 5-956: por_rnd_por_rnd_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-943: por_rnd_por_rnd_s2_qos_lat_scale (low)



The following table shows the por_rnd_s2_qos_lat_scale lower register bit assignments.

Table 5-957: por_rnd_por_rnd_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	s2_aw_lat_scale	Port S2 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.7.25 por_rnd_s2_qos_lat_range

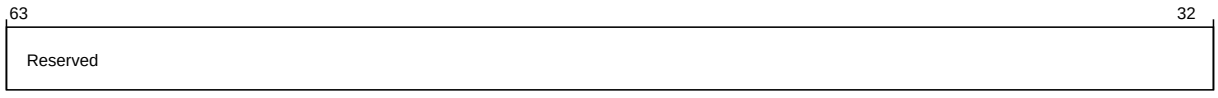
Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAD8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-944: por_rnd_por_rnd_s2_qos_lat_range (high)



The following table shows the por_rnd_s2_qos_lat_range higher register bit assignments.

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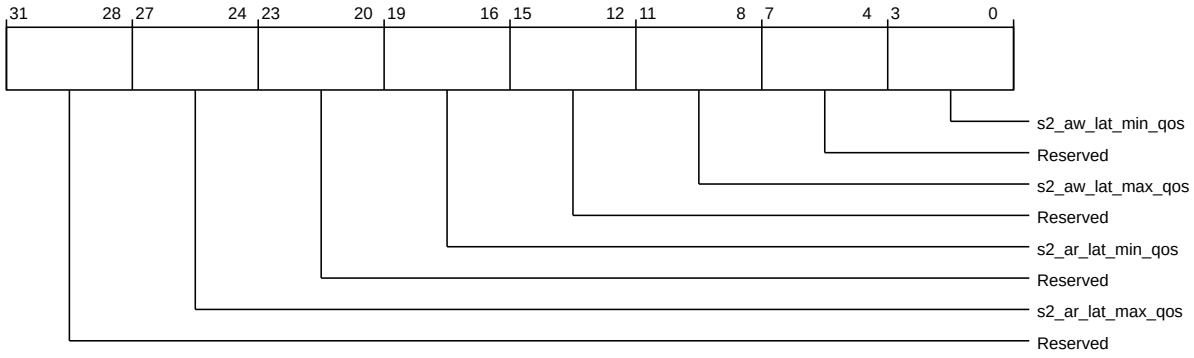
Table 5-958: por_rnd_por_rnd_s2_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-945: por_rnd_por_rnd_s2_qos_lat_range (low)



The following table shows the por_rnd_s2_qos_lat_range lower register bit assignments.

Table 5-959: por_rnd_por_rnd_s2_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s2_ar_lat_max_qos	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s2_ar_lat_min_qos	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s2_aw_lat_max_qos	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s2_aw_lat_min_qos	Port S2 AW QoS minimum value	RW	4'h0

5.3.7.26 por_rnd_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0

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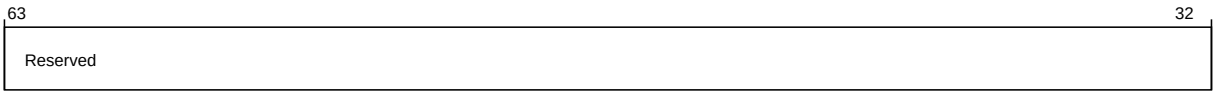
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-946: por_rnd_por_rnd_pmu_event_sel (high)



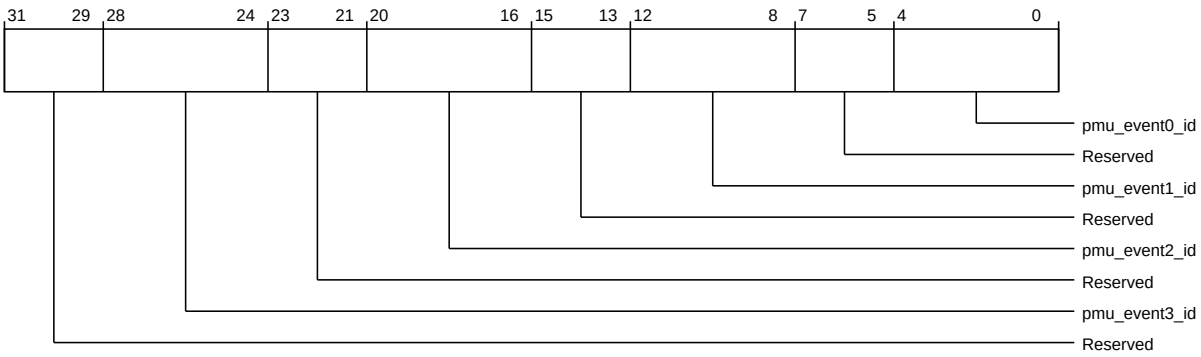
The following table shows the por_rnd_pmu_event_sel higher register bit assignments.

Table 5-960: por_rnd_por_rnd_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-947: por_rnd_por_rnd_pmu_event_sel (low)



The following table shows the por_rnd_pmu_event_sel lower register bit assignments.

Table 5-961: por_rnd_por_rnd_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	RN-D PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	RN-D PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	RN-D PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0
7:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4:0	pmu_event0_id	RN-D PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow_slice0 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: PADB occupancy count overflow 5'h12: RPDB occupancy count overflow 5'h13: RRT occupancy count overflow_slice1 5'h14: RRT occupancy count overflow_slice2 5'h15: RRT occupancy count overflow_slice3 5'h16: WRT request throttled	RW	5'b0

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5.3.7.27 por_rnd_syscoreq_ctl

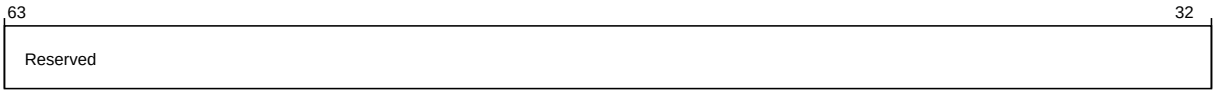
Functions as the RN-D DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoack_status.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1C00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-948: por_rnd_por_rnd_syscoreq_ctl (high)



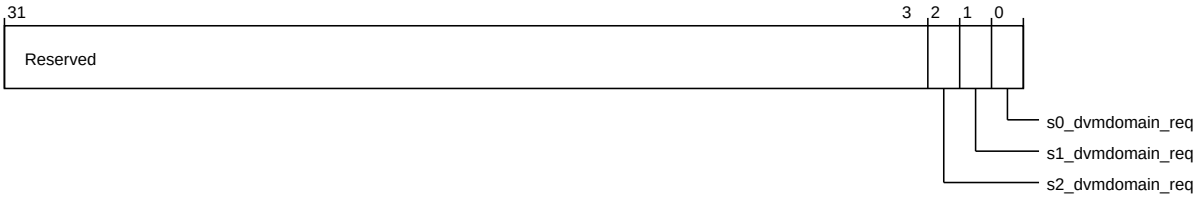
The following table shows the por_rnd_syscoreq_ctl higher register bit assignments.

Table 5-962: por_rnd_por_rnd_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-949: por_rnd_por_rnd_syscoreq_ctl (low)



The following table shows the por_rnd_syscoreq_ctl lower register bit assignments.

Table 5-963: por_rnd_por_rnd_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2	s2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S2	RW	1'b0
1	s1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S1	RW	1'b0
0	s0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S0	RW	1'b0

5.3.7.28 por_rnd_syscoack_status

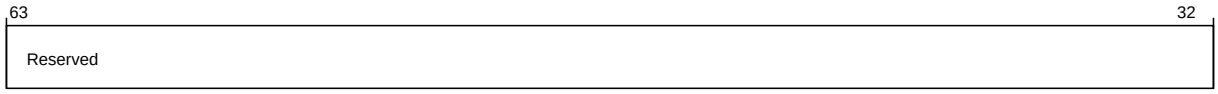
Functions as the RN-D DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoreq_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1C08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-950: por_rnd_por_rnd_syscoack_status (high)



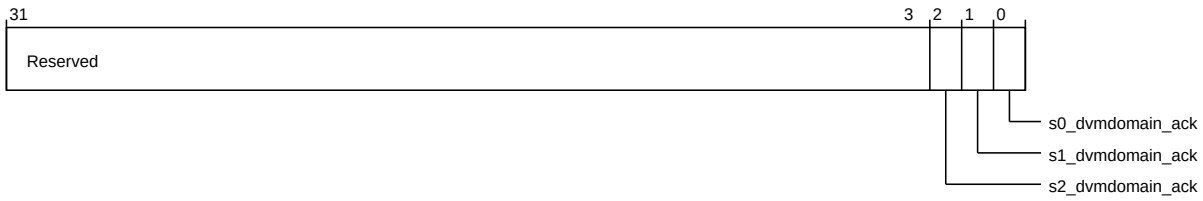
The following table shows the por_rnd_syscoack_status higher register bit assignments.

Table 5-964: por_rnd_por_rnd_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-951: por_rnd_por_rnd_syscoack_status (low)



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The following table shows the por_rnd_syscoack_status lower register bit assignments.

Table 5-965: por_rnd_por_rnd_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	s2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S2	RO	1'b0
1	s1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S1	RO	1'b0
0	s0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S0	RO	1'b0

5.3.8 RN-I register descriptions

This section lists the RN-I registers.

5.3.8.1 por_rni_node_info

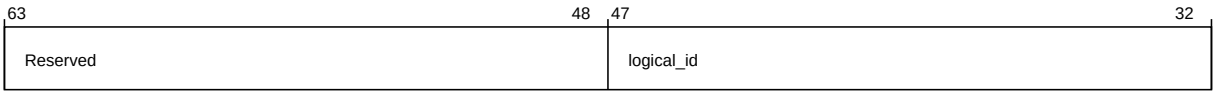
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-952: por_rni_por_rni_node_info (high)



The following table shows the por_rni_node_info higher register bit assignments.

Table 5-966: por_rni_por_rni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

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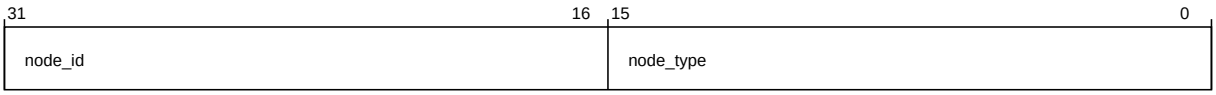
The following figure shows the lower register bit assignments.

Figure 5-953: por_rni_por_rni_node_info (low)



The following table shows the por_rni_node_info lower register bit assignments.

Table 5-967: por_rni_por_rni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h000A

5.3.8.2 por_rni_child_info

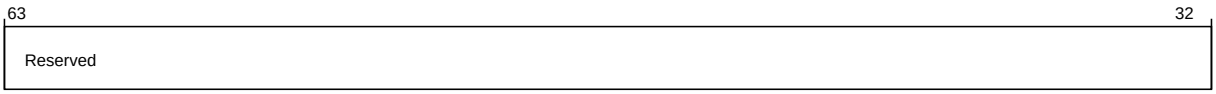
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-954: por_rni_por_rni_child_info (high)



The following table shows the por_rni_child_info higher register bit assignments.

Table 5-968: por_rni_por_rni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

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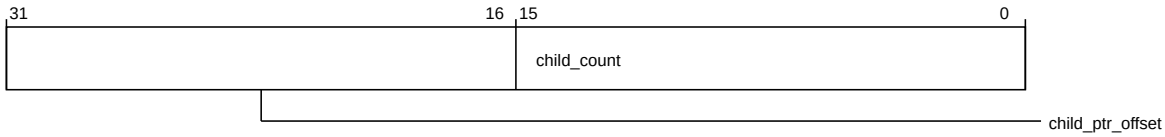
The following figure shows the lower register bit assignments.

Figure 5-955: por_rni_por_rni_child_info (low)



The following table shows the por_rni_child_info lower register bit assignments.

Table 5-969: por_rni_por_rni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

5.3.8.3 por_rni_secure_register_groups_override

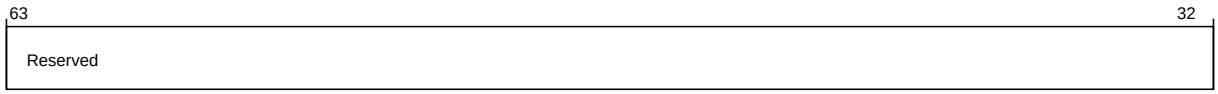
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-956: por_rni_por_rni_secure_register_groups_override (high)



The following table shows the por_rni_secure_register_groups_override higher register bit assignments.

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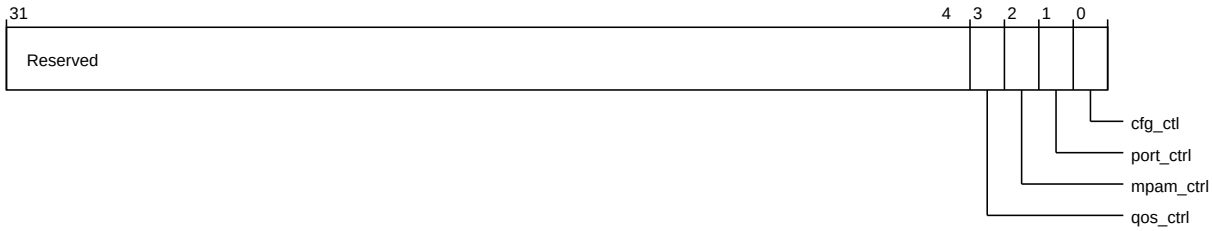
Table 5-970: por_rni_por_rni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-957: por_rni_por_rni_secure_register_groups_override (low)



The following table shows the por_rni_secure_register_groups_override lower register bit assignments.

Table 5-971: por_rni_por_rni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	qos_ctrl	Allows Non-secure access to Secure QoS control registers	RW	1'b0
2	mpam_ctrl	Allows Non-secure access to Secure AXI port MPAM override register	RW	1'b0
1	port_ctrl	Allows Non-secure access to Secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows Non-secure access to Secure configuration control register	RW	1'b0

5.3.8.4 por_rni_unit_info

Provides component identification information for RN-I.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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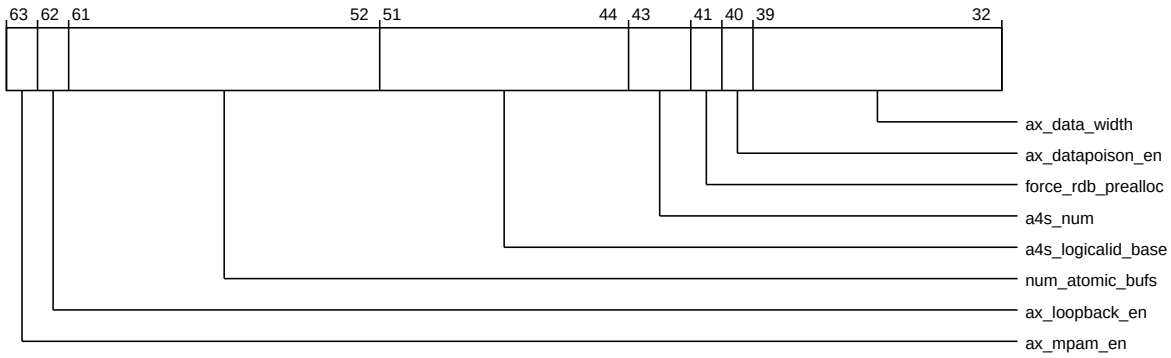
Figure 5-958: por_rni_por_rni_unit_info (high)



The following table shows the por_rni_unit_info higher register bit assignments.

Table 5-972: por_rni_por_rni_unit_info (high)

Bits	Field name	Description	Type	Reset
63	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
62	ax_loopback_en	LoopBack enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
61:52	num_atomic_bufs	Number of atomic data buffers	RO	Configuration dependent
51:44	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
43:42	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
41	force_rdb_prealloc	Force read data buffer preallocation 1'b1: yes 1'b0: no	RO	Configuration dependent
40	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
39:32	ax_data_width	AXI interface data width in bits	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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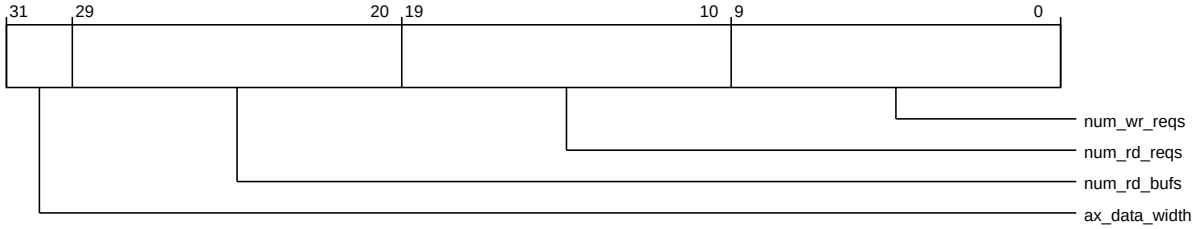
Figure 5-959: por_rni_por_rni_unit_info (low)



The following table shows the por_rni_unit_info lower register bit assignments.

Table 5-973: por_rni_por_rni_unit_info (low)

Bits	Field name	Description	Type	Reset
31:30	ax_data_width	AXI interface data width in bits	RO	Configuration dependent
29:20	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
19:10	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
9:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

5.3.8.5 por_rni_unit_info2

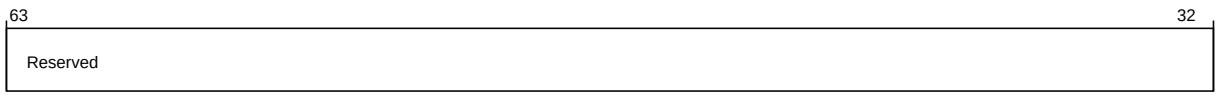
Provides additonal component identification information for RN-I.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h908
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-960: por_rni_por_rni_unit_info2 (high)



The following table shows the por_rni_unit_info2 higher register bit assignments.

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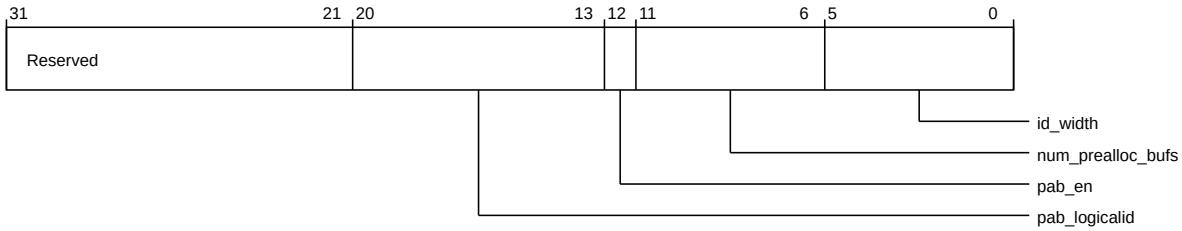
Table 5-974: por_rni_por_rni_unit_info2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-961: por_rni_por_rni_unit_info2 (low)



The following table shows the por_rni_unit_info2 lower register bit assignments.

Table 5-975: por_rni_por_rni_unit_info2 (low)

Bits	Field name	Description	Type	Reset
31:21	Reserved	Reserved	RO	-
20:13	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent
12	pab_en	PUB AUB bridge enable 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
11:6	num_prealloc_bufs	Number of Pre-allocated Read Data Buffers	RO	Configuration dependent
5:0	id_width	AXI ID width for ACE-Lite slave ports	RO	Configuration dependent

5.3.8.6 por_rni_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.cfg_ctl

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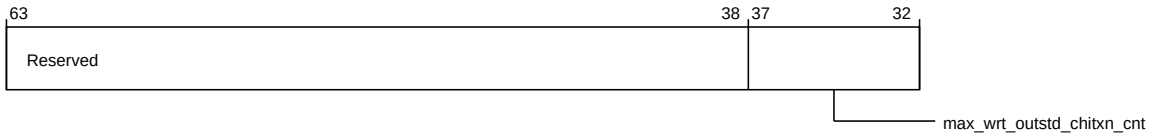
The following figure shows the higher register bit assignments.

Figure 5-962: por_rni_por_rni_cfg_ctl (high)



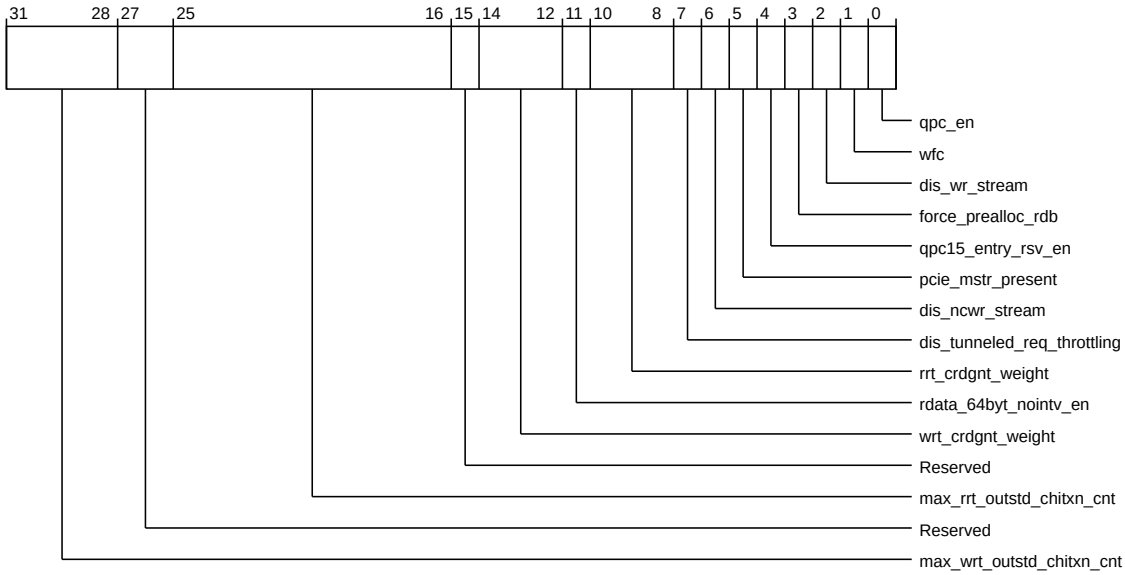
The following table shows the por_rni_cfg_ctl higher register bit assignments.

Table 5-976: por_rni_por_rni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-963: por_rni_por_rni_cfg_ctl (low)



The following table shows the por_rni_cfg_ctl lower register bit assignments.

Table 5-977: por_rni_por_rni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:28	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
27:26	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
25:16	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	rdata_64byt_nointv_en	Enables no interleaving property on normal memory read data within 64B granule when set	RW	1'b1
10:8	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	dis_tunneled_req_throttling	Disables retry based throttling of tunneled write requests	RW	1'b0
6	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	pcie_mstr_present	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0
4	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rnd_qpc_en is set	RW	1'b0
3	force_prealloc_rdb	When set, all reads from the RN-I are sent with a preallocated read data buffer	RW	Configuration dependent
2	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
1	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

5.3.8.7 por_rni_aux_ctl

Functions as the auxiliary control register for RN-I.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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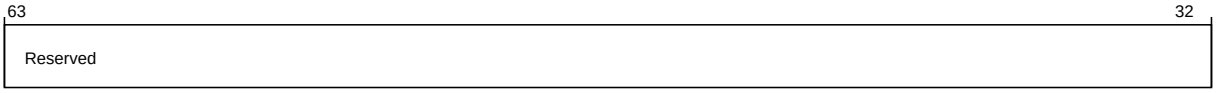
Figure 5-964: por_rni_por_rni_aux_ctl (high)



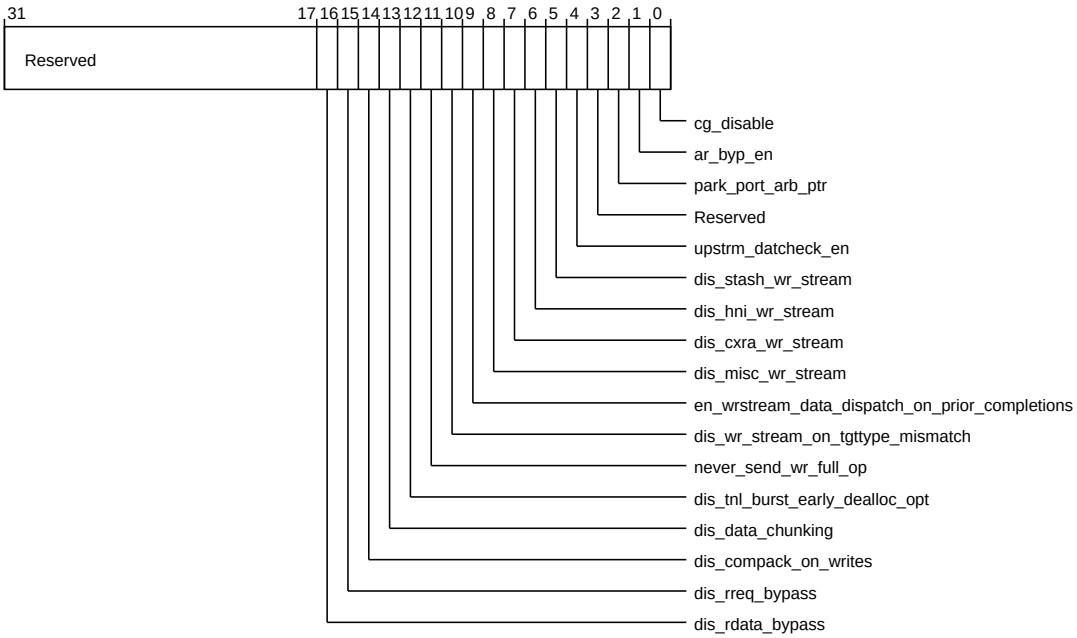
The following table shows the por_rni_aux_ctl higher register bit assignments.

Table 5-978: por_rni_por_rni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-965: por_rni_por_rni_aux_ctl (low)



The following table shows the por_rni_aux_ctl lower register bit assignments.

Table 5-979: por_rni_por_rni_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	dis_rdata_bypass	If set, disables read data bypass path	RW	1'b0
15	dis_rreq_bypass	If set, disables read request bypass path	RW	1'b0
14	dis_compack_on_writes	If set, disables comp_ack on streaming writes. WrData is used for ordering writes	RW	1'b1

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Bits	Field name	Description	Type	Reset
13	dis_data_chunking	If set, disables the data chunking feature	RW	1'b0
12	dis_tnl_burst_early_dealloc_opt	If set, disables the optimization related to early deallocation of tunnelled writes for intermediate txns of burst	RW	1'b1
11	never_send_wr_full_op	If set, RNI will never send WR FULL op. All write ops will be of PTL type	RW	1'b0
10	dis_wr_stream_on_tgttype_mismatch	If set, serializes first write when moving from one tgttype to another	RW	1'b0
9	en_wrstream_data_dispatch_on_prior_completions	If set, data dispatch for streaming writes waits for completion of all older writes	RW	1'b0
8	dis_misc_wr_stream	Disables streaming of ordered writes with following attributes when set : Device memory or EWA=0 or Excl=1	RW	1'b0
7	dis_cxra_wr_stream	Disables streaming of ordered writes to CXRA when set	RW	1'b0
6	dis_hni_wr_stream	Disables streaming of ordered writes to HNI when set	RW	1'b0
5	dis_stash_wr_stream	Disables streaming of ordered WrUniqStash when set	RW	1'b0
4	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
3	Reserved	Reserved	RO	-
2	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	cg_disable	Disables clock gating when set	RW	1'b0

5.3.8.8 por_rni_s0_port_control

Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

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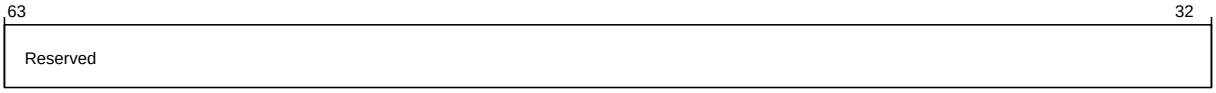
Figure 5-966: por_rni_por_rni_s0_port_control (high)



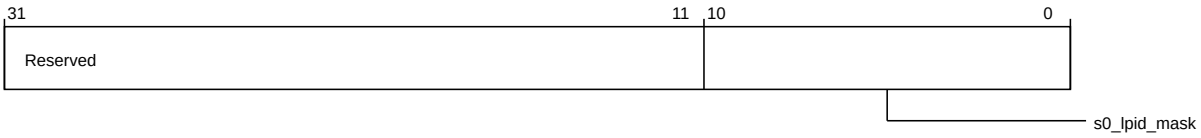
The following table shows the por_rni_s0_port_control higher register bit assignments.

Table 5-980: por_rni_por_rni_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-967: por_rni_por_rni_s0_port_control (low)



The following table shows the por_rni_s0_port_control lower register bit assignments.

Table 5-981: por_rni_por_rni_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

5.3.8.9 por_rni_s1_port_control

Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA18

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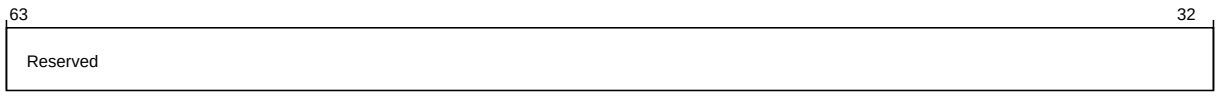
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

Figure 5-968: por_rni_por_rni_s1_port_control (high)



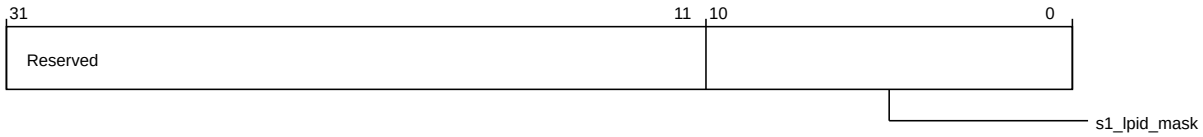
The following table shows the por_rni_s1_port_control higher register bit assignments.

Table 5-982: por_rni_por_rni_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-969: por_rni_por_rni_s1_port_control (low)



The following table shows the por_rni_s1_port_control lower register bit assignments.

Table 5-983: por_rni_por_rni_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

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5.3.8.10 por_rni_s2_port_control

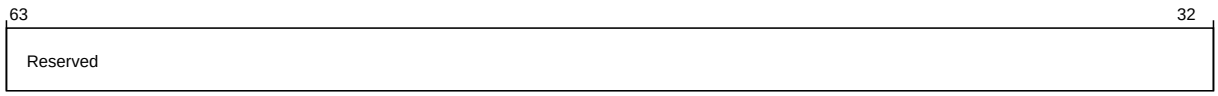
Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.port_ctrl

The following figure shows the higher register bit assignments.

Figure 5-970: por_rni_por_rni_s2_port_control (high)



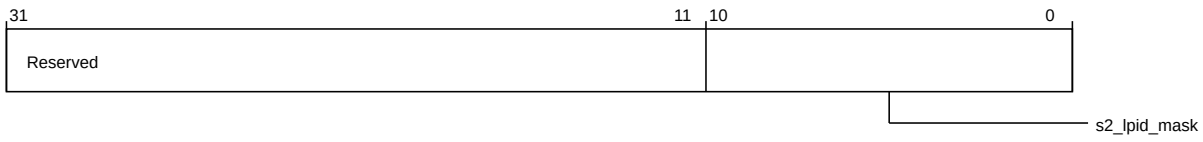
The following table shows the por_rni_s2_port_control higher register bit assignments.

Table 5-984: por_rni_por_rni_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-971: por_rni_por_rni_s2_port_control (low)



The following table shows the por_rni_s2_port_control lower register bit assignments.

Table 5-985: por_rni_por_rni_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

5.3.8.11 por_rni_s0_mpam_control

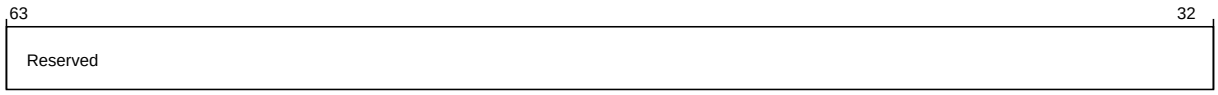
Controls port S0 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-972: por_rni_por_rni_s0_mpam_control (high)



The following table shows the por_rni_s0_mpam_control higher register bit assignments.

Table 5-986: por_rni_por_rni_s0_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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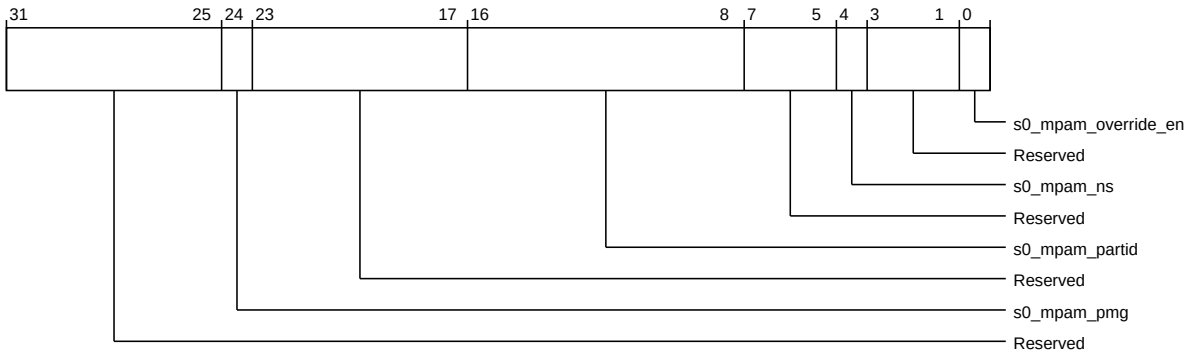
Figure 5-973: por_rni_por_rni_s0_mpam_control (low)



The following table shows the por_rni_s0_mpam_control lower register bit assignments.

Table 5-987: por_rni_por_rni_s0_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s0_mpam_pmg	Port S0 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s0_mpam_partid	Port S0 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	s0_mpam_ns	Port S0 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	s0_mpam_override_en	Port S0 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.8.12 por_rni_s1_mpam_control

Controls port S1 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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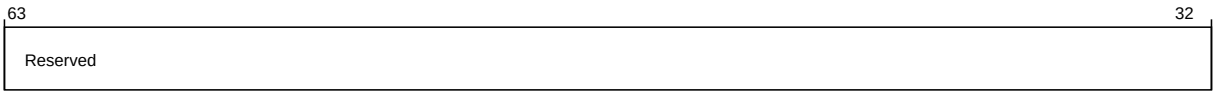
Secure group override por_rni_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-974: por_rni_por_rni_s1_mpam_control (high)



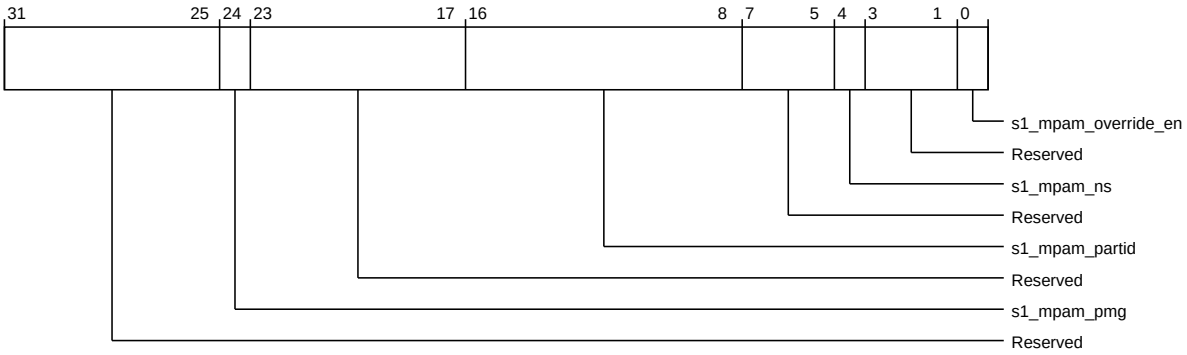
The following table shows the por_rni_s1_mpam_control higher register bit assignments.

Table 5-988: por_rni_por_rni_s1_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-975: por_rni_por_rni_s1_mpam_control (low)



The following table shows the por_rni_s1_mpam_control lower register bit assignments.

Table 5-989: por_rni_por_rni_s1_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s1_mpam_pmg	Port S1 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s1_mpam_partid	Port S1 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	s1_mpam_ns	Port S1 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	s1_mpam_override_en	Port S1 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.8.13 por_rni_s2_mpam_control

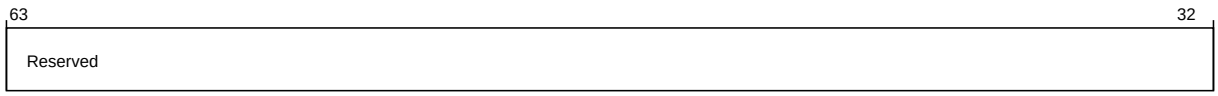
Controls port S2 AXI/ACE slave interface MPAM override values

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.mpam_ctrl

The following figure shows the higher register bit assignments.

Figure 5-976: por_rni_por_rni_s2_mpam_control (high)



The following table shows the por_rni_s2_mpam_control higher register bit assignments.

Table 5-990: por_rni_por_rni_s2_mpam_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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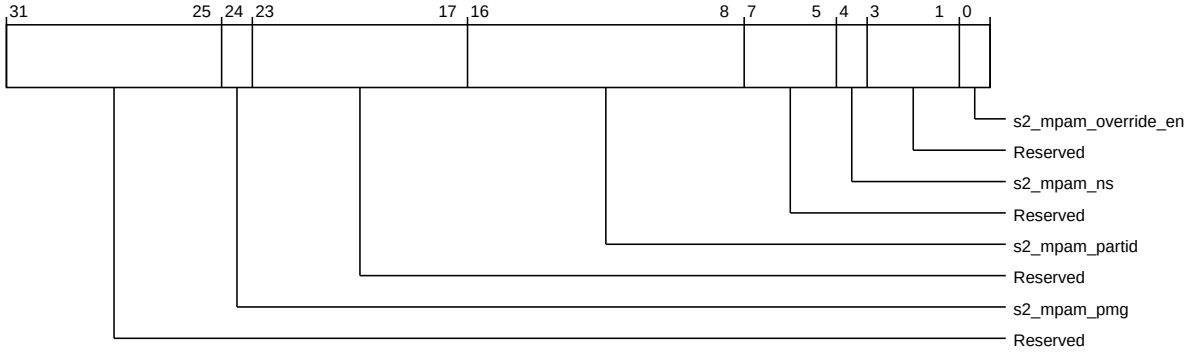
Figure 5-977: por_rni_por_rni_s2_mpam_control (low)



The following table shows the por_rni_s2_mpam_control lower register bit assignments.

Table 5-991: por_rni_por_rni_s2_mpam_control (low)

Bits	Field name	Description	Type	Reset
31:25	Reserved	Reserved	RO	-
24	s2_mpam_pmg	Port S2 MPAM_PMG value	RW	1'b0
23:17	Reserved	Reserved	RO	-
16:8	s2_mpam_partid	Port S2 MPAM_PARTID value	RW	9'b0
7:5	Reserved	Reserved	RO	-
4	s2_mpam_ns	Port S2 MPAM_NS value	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	s2_mpam_override_en	Port S2 MPAM override en When set, MPAM value on CHI side is driven from MPAM override value in this register. Note that when RNID_AXMPAM_EN_PARAM is set to 0, MPAM override value is always used irrespective of this bit value	RW	1'b0

5.3.8.14 por_rni_s0_qos_control

Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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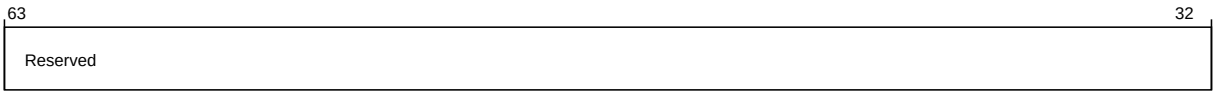
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-978: por_rni_por_rni_s0_qos_control (high)



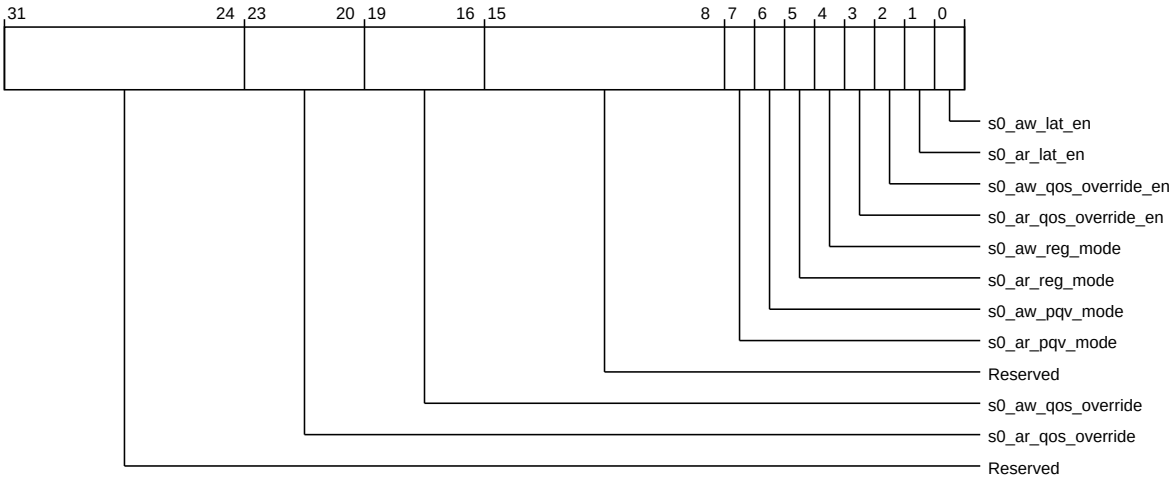
The following table shows the por_rni_s0_qos_control higher register bit assignments.

Table 5-992: por_rni_por_rni_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-979: por_rni_por_rni_s0_qos_control (low)



The following table shows the por_rni_s0_qos_control lower register bit assignments.

Table 5-993: por_rni_por_rni_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s0_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s0_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s0_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s0_ar_qos_override_en	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s0_aw_qos_override_en	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s0_ar_lat_en	Enables port S0 AR QoS regulation when set	RW	1'b0
0	s0_aw_lat_en	Enables port S0 AW QoS regulation when set	RW	1'b0

5.3.8.15 por_rni_s0_qos_lat_tgt

Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

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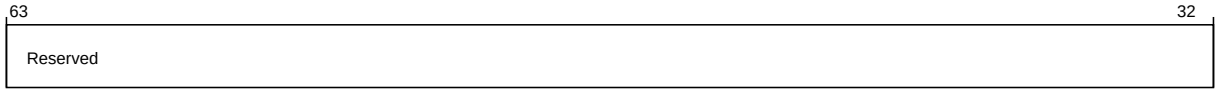
Figure 5-980: por_rni_por_rni_s0_qos_lat_tgt (high)



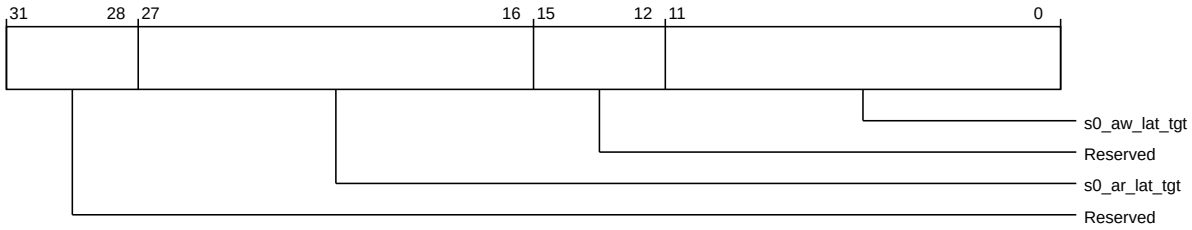
The following table shows the por_rni_s0_qos_lat_tgt higher register bit assignments.

Table 5-994: por_rni_por_rni_s0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-981: por_rni_por_rni_s0_qos_lat_tgt (low)



The following table shows the por_rni_s0_qos_lat_tgt lower register bit assignments.

Table 5-995: por_rni_por_rni_s0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s0_ar_lat_tgt	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s0_aw_lat_tgt	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.8.16 por_rni_s0_qos_lat_scale

Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA90

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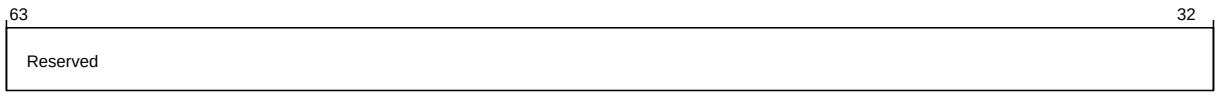
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-982: por_rni_por_rni_s0_qos_lat_scale (high)



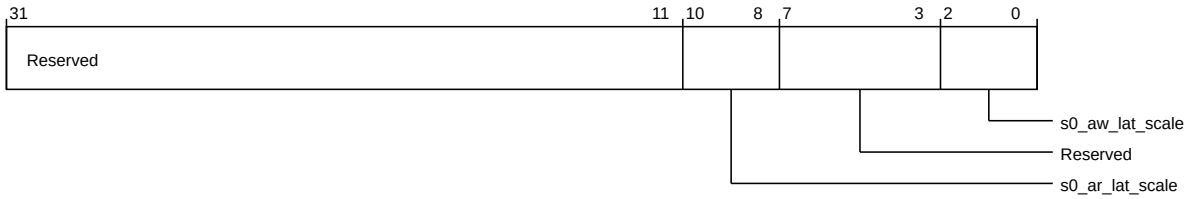
The following table shows the por_rni_s0_qos_lat_scale higher register bit assignments.

Table 5-996: por_rni_por_rni_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-983: por_rni_por_rni_s0_qos_lat_scale (low)



The following table shows the por_rni_s0_qos_lat_scale lower register bit assignments.

Table 5-997: por_rni_por_rni_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.8.17 por_rni_s0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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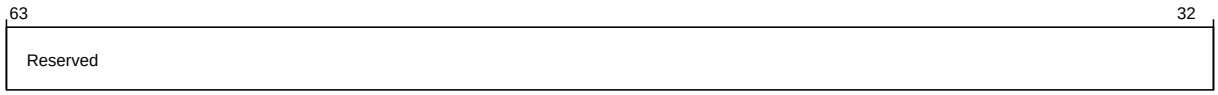
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-984: por_rni_por_rni_s0_qos_lat_range (high)



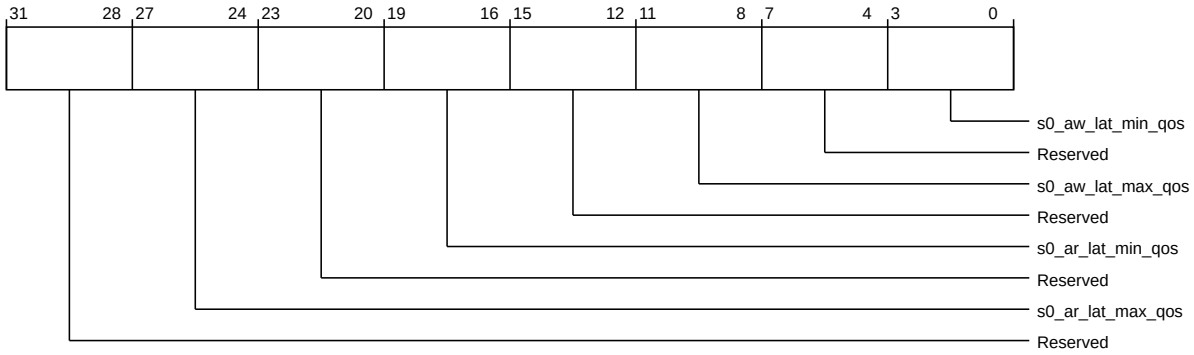
The following table shows the por_rni_s0_qos_lat_range higher register bit assignments.

Table 5-998: por_rni_por_rni_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-985: por_rni_por_rni_s0_qos_lat_range (low)



The following table shows the por_rni_s0_qos_lat_range lower register bit assignments.

Table 5-999: por_rni_por_rni_s0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s0_ar_lat_max_qos	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s0_ar_lat_min_qos	Port S0 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s0_aw_lat_max_qos	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s0_aw_lat_min_qos	Port S0 AW QoS minimum value	RW	4'h0

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5.3.8.18 por_rni_s1_qos_control

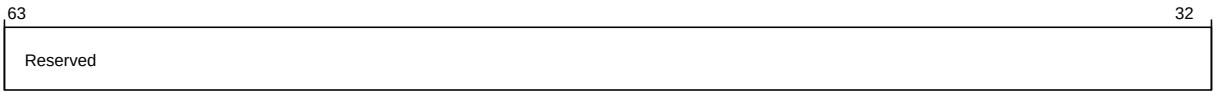
Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-986: por_rni_por_rni_s1_qos_control (high)



The following table shows the por_rni_s1_qos_control higher register bit assignments.

Table 5-1000: por_rni_por_rni_s1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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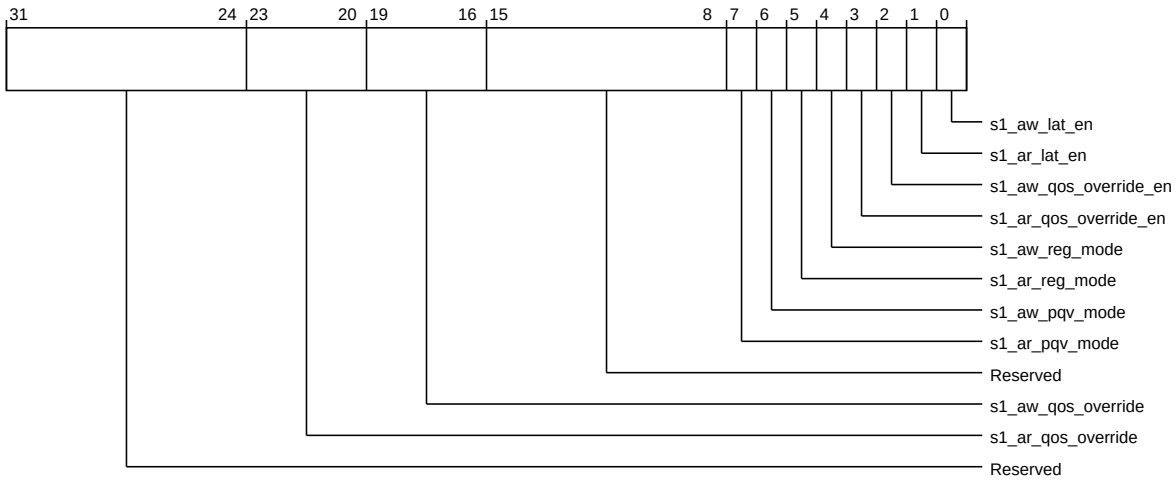
Figure 5-987: por_rni_por_rni_s1_qos_control (low)



The following table shows the por_rni_s1_qos_control lower register bit assignments.

Table 5-1001: por_rni_por_rni_s1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s1_ar_qos_override	AR QoS override value for port S1	RW	4'b0000
19:16	s1_aw_qos_override	AW QoS override value for port S1	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s1_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s1_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s1_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s1_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0

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Bits	Field name	Description	Type	Reset
3	s1_ar_qos_override_en	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s1_aw_qos_override_en	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s1_ar_lat_en	Enables port S1 AR QoS regulation when set	RW	1'b0
0	s1_aw_lat_en	Enables port S1 AW QoS regulation when set	RW	1'b0

5.3.8.19 por_rni_s1_qos_lat_tgt

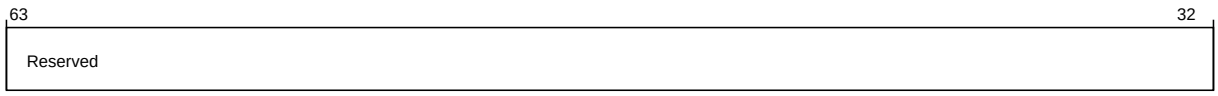
Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAA8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-988: por_rni_por_rni_s1_qos_lat_tgt (high)



The following table shows the por_rni_s1_qos_lat_tgt higher register bit assignments.

Table 5-1002: por_rni_por_rni_s1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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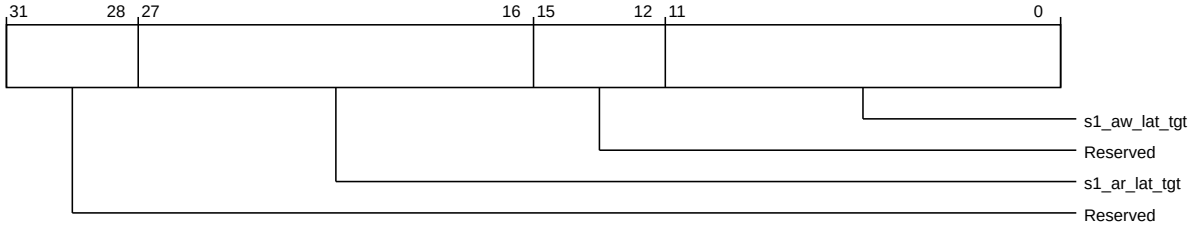
Figure 5-989: por_rni_por_rni_s1_qos_lat_tgt (low)



The following table shows the por_rni_s1_qos_lat_tgt lower register bit assignments.

Table 5-1003: por_rni_por_rni_s1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s1_ar_lat_tgt	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s1_aw_lat_tgt	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.8.20 por_rni_s1_qos_lat_scale

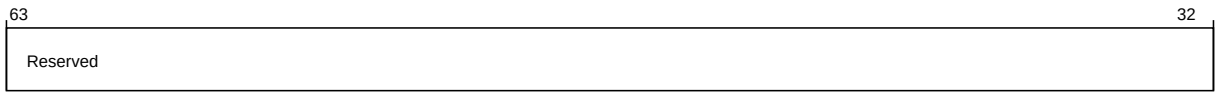
Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-990: por_rni_por_rni_s1_qos_lat_scale (high)



The following table shows the por_rni_s1_qos_lat_scale higher register bit assignments.

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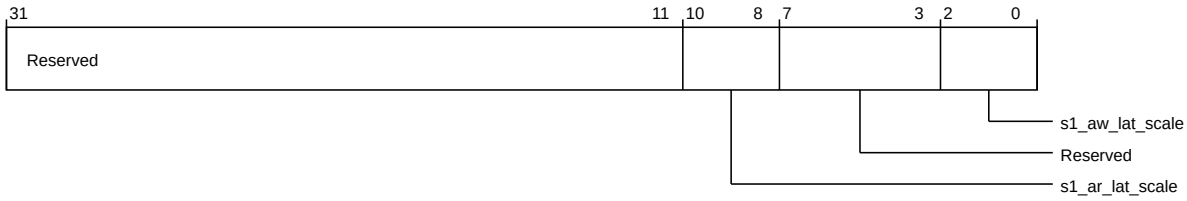
Table 5-1004: por_rni_por_rni_s1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-991: por_rni_por_rni_s1_qos_lat_scale (low)



The following table shows the por_rni_s1_qos_lat_scale lower register bit assignments.

Table 5-1005: por_rni_por_rni_s1_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s1_ar_lat_scale	Port S1 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	s1_aw_lat_scale	Port S1 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.8.21 por_rni_s1_qos_lat_range

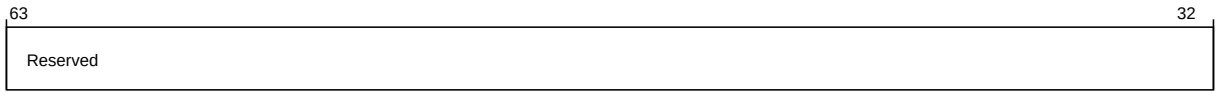
Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAB8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-992: por_rni_por_rni_s1_qos_lat_range (high)



The following table shows the por_rni_s1_qos_lat_range higher register bit assignments.

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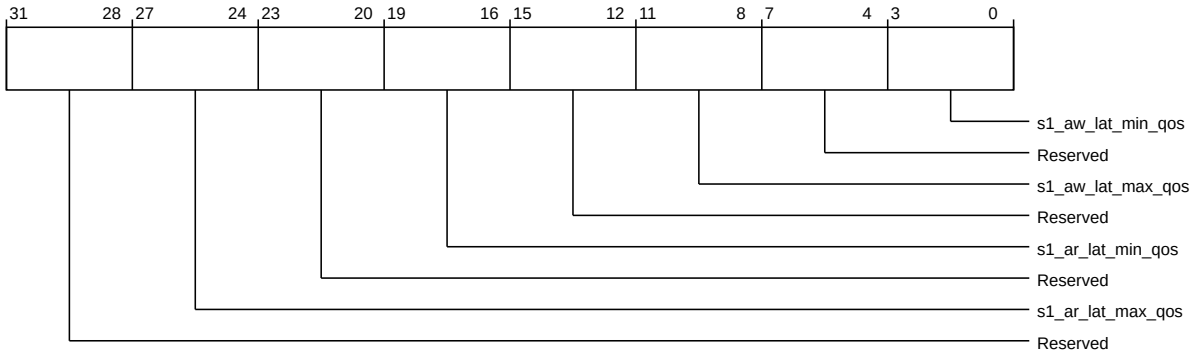
Table 5-1006: por_rni_por_rni_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-993: por_rni_por_rni_s1_qos_lat_range (low)



The following table shows the por_rni_s1_qos_lat_range lower register bit assignments.

Table 5-1007: por_rni_por_rni_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

5.3.8.22 por_rni_s2_qos_control

Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAC0
Register reset 64'b0

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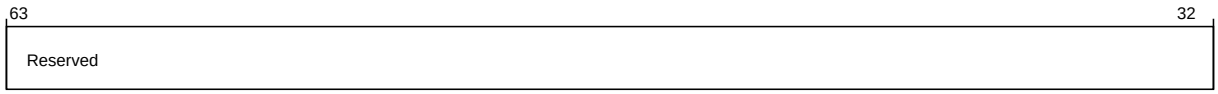
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-994: por_rni_por_rni_s2_qos_control (high)



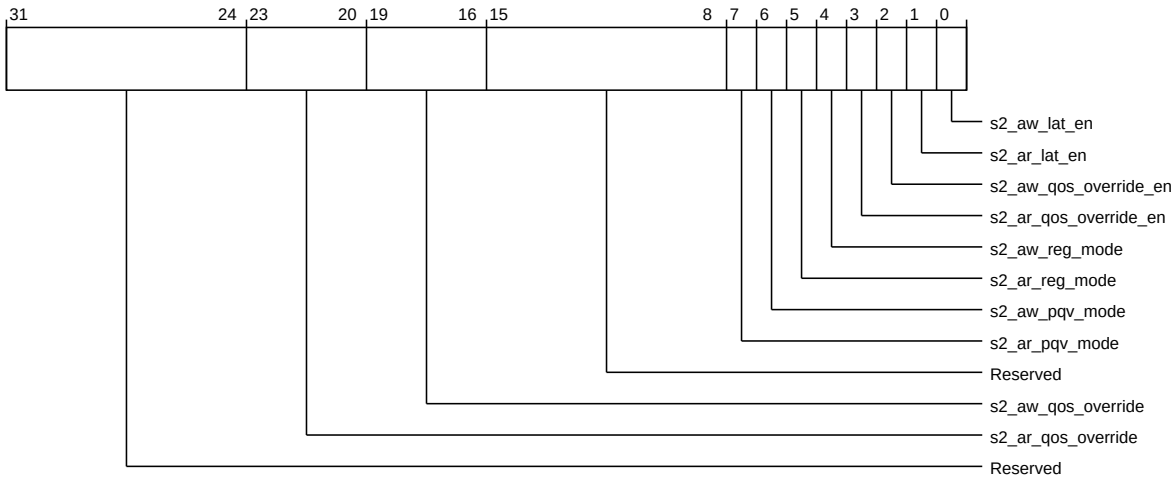
The following table shows the por_rni_s2_qos_control higher register bit assignments.

Table 5-1008: por_rni_por_rni_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-995: por_rni_por_rni_s2_qos_control (low)



The following table shows the por_rni_s2_qos_control lower register bit assignments.

Table 5-1009: por_rni_por_rni_s2_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s2_ar_qos_override	AR QoS override value for port S2	RW	4'b0000
19:16	s2_aw_qos_override	AW QoS override value for port S2	RW	4'b0000

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Bits	Field name	Description	Type	Reset
15:8	Reserved	Reserved	RO	-
7	s2_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s2_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s2_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s2_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s2_ar_qos_override_en	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s2_aw_qos_override_en	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s2_ar_lat_en	Enables port S2 AR QoS regulation when set	RW	1'b0
0	s2_aw_lat_en	Enables port S2 AW QoS regulation when set	RW	1'b0

5.3.8.23 por_rni_s2_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAC8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

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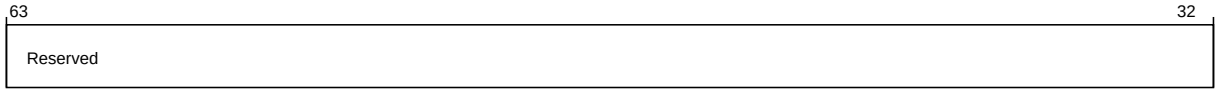
Figure 5-996: por_rni_por_rni_s2_qos_lat_tgt (high)



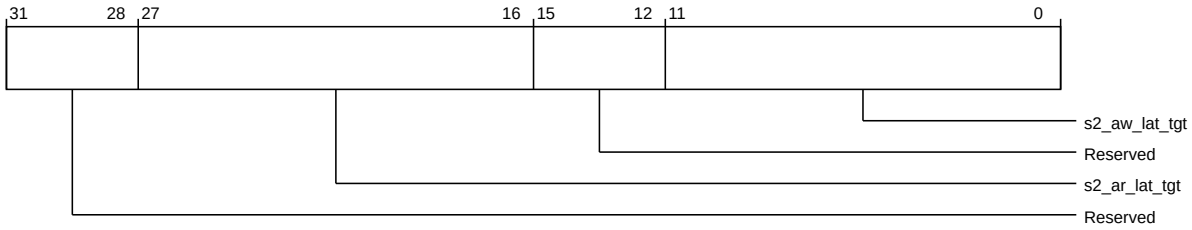
The following table shows the por_rni_s2_qos_lat_tgt higher register bit assignments.

Table 5-1010: por_rni_por_rni_s2_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-997: por_rni_por_rni_s2_qos_lat_tgt (low)



The following table shows the por_rni_s2_qos_lat_tgt lower register bit assignments.

Table 5-1011: por_rni_por_rni_s2_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s2_ar_lat_tgt	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s2_aw_lat_tgt	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

5.3.8.24 por_rni_s2_qos_lat_scale

Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAD0

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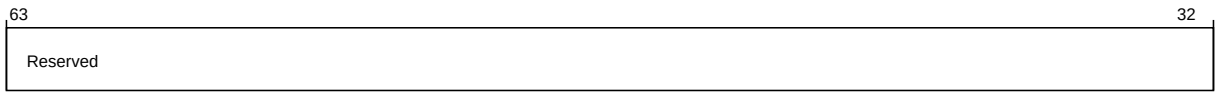
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-998: por_rni_por_rni_s2_qos_lat_scale (high)



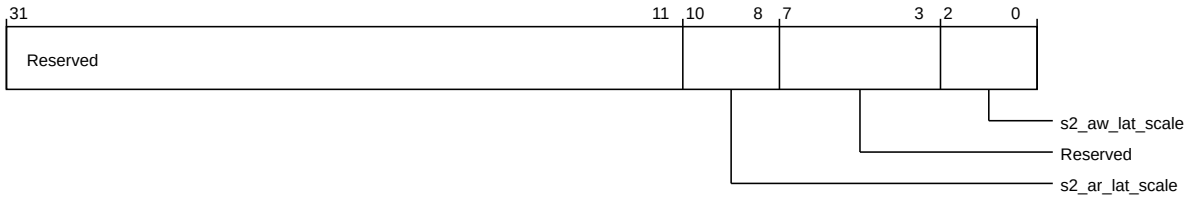
The following table shows the por_rni_s2_qos_lat_scale higher register bit assignments.

Table 5-1012: por_rni_por_rni_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-999: por_rni_por_rni_s2_qos_lat_scale (low)



The following table shows the por_rni_s2_qos_lat_scale lower register bit assignments.

Table 5-1013: por_rni_por_rni_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s2_aw_lat_scale	Port S2 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

5.3.8.25 por_rni_s2_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hAD8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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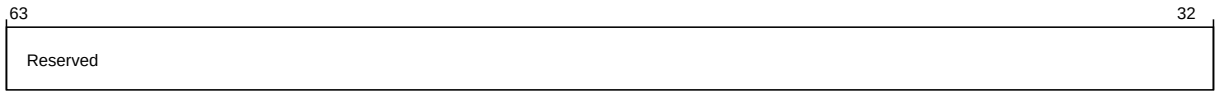
Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following figure shows the higher register bit assignments.

Figure 5-1000: por_rni_por_rni_s2_qos_lat_range (high)



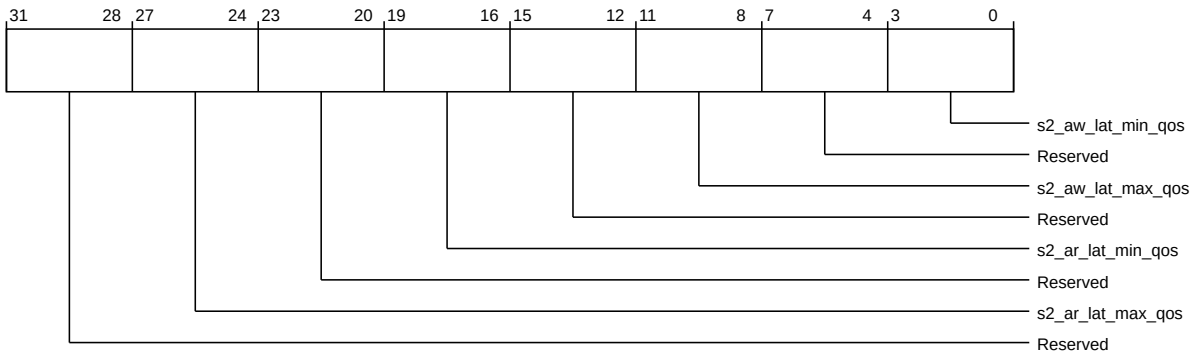
The following table shows the por_rni_s2_qos_lat_range higher register bit assignments.

Table 5-1014: por_rni_por_rni_s2_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1001: por_rni_por_rni_s2_qos_lat_range (low)



The following table shows the por_rni_s2_qos_lat_range lower register bit assignments.

Table 5-1015: por_rni_por_rni_s2_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s2_ar_lat_max_qos	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s2_ar_lat_min_qos	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s2_aw_lat_max_qos	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s2_aw_lat_min_qos	Port S2 AW QoS minimum value	RW	4'h0

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5.3.8.26 por_rni_pmu_event_sel

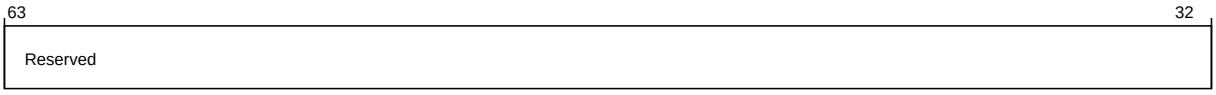
Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1002: por_rni_por_rni_pmu_event_sel (high)



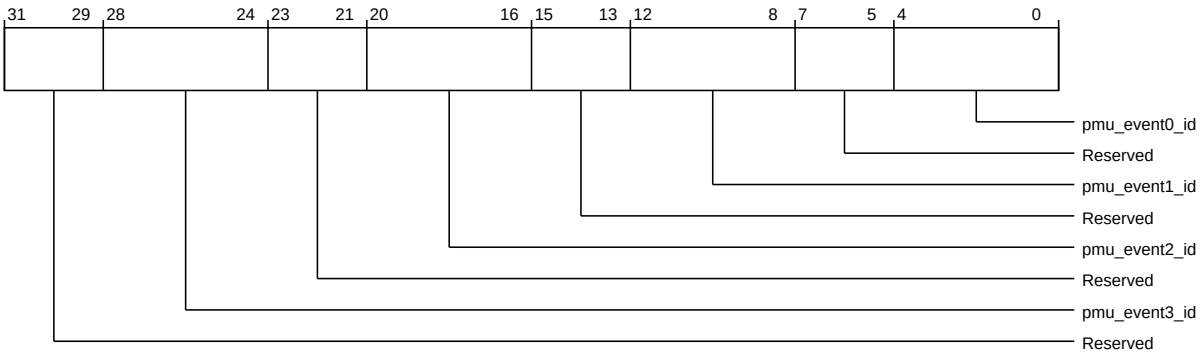
The following table shows the por_rni_pmu_event_sel higher register bit assignments.

Table 5-1016: por_rni_por_rni_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1003: por_rni_por_rni_pmu_event_sel (low)



The following table shows the por_rni_pmu_event_sel lower register bit assignments.

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Table 5-1017: por_rni_por_rni_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	RN-I PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	RN-I PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	RN-I PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0
7:5	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
4:0	pmu_event0_id	RN-I PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: PADB occupancy count overflow 5'h12: RPDB occupancy count overflow 5'h13: RRT occupancy count overflow_slice1 5'h14: RRT occupancy count overflow_slice2 5'h15: RRT occupancy count overflow_slice3 5'h16: WRT request throttled	RW	5'b0

5.3.9 RN SAM register descriptions

This section lists the RN SAM registers.

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5.3.9.1 por_rnsam_node_info

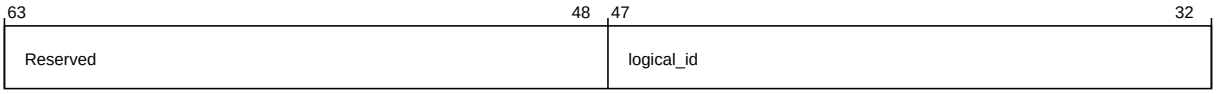
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1004: por_rnsam_por_rnsam_node_info (high)



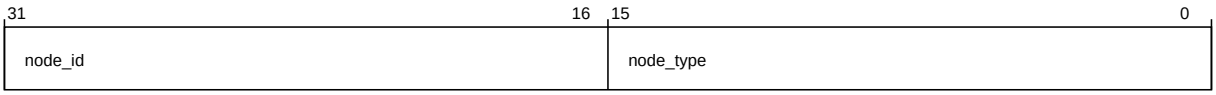
The following table shows the por_rnsam_node_info higher register bit assignments.

Table 5-1018: por_rnsam_por_rnsam_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID NOTE: RN SAM logical ID is always set to 16'b0.	RO	16'h0

The following figure shows the lower register bit assignments.

Figure 5-1005: por_rnsam_por_rnsam_node_info (low)



The following table shows the por_rnsam_node_info lower register bit assignments.

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Table 5-1019: por_rnsam_por_rnsam_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h000F

5.3.9.2 por_rnsam_child_info

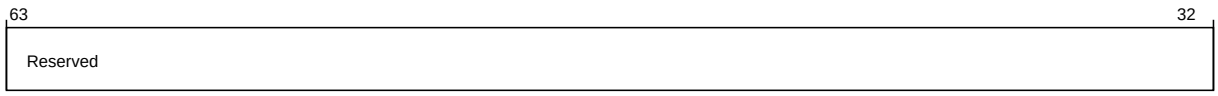
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1006: por_rnsam_por_rnsam_child_info (high)



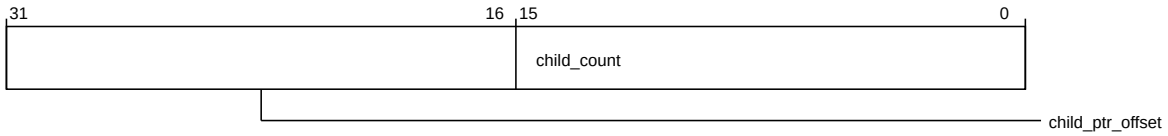
The following table shows the por_rnsam_child_info higher register bit assignments.

Table 5-1020: por_rnsam_por_rnsam_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1007: por_rnsam_por_rnsam_child_info (low)



The following table shows the por_rnsam_child_info lower register bit assignments.

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Table 5-1021: por_rnsam_por_rnsam_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.9.3 por_rnsam_secure_register_groups_override

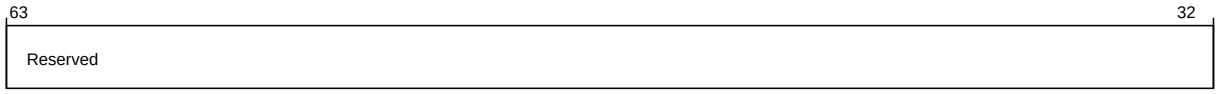
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1008: por_rnsam_por_rnsam_secure_register_groups_override (high)



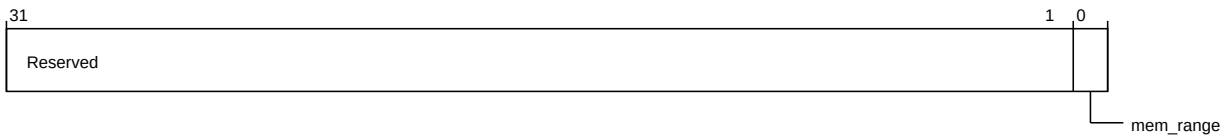
The following table shows the por_rnsam_secure_register_groups_override higher register bit assignments.

Table 5-1022: por_rnsam_por_rnsam_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1009: por_rnsam_por_rnsam_secure_register_groups_override (low)



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The following table shows the por_rnsam_secure_register_groups_override lower register bit assignments.

Table 5-1023: por_rnsam_por_rnsam_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	mem_range	Allows Non-secure access to Secure mem_ranges registers	RW	1'b0

5.3.9.4 por_rnsam_unit_info

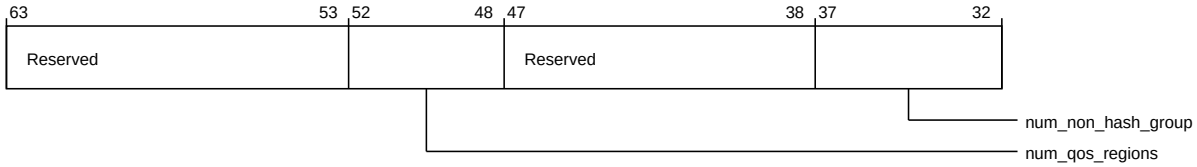
Provides component identification information for RN SAM.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1010: por_rnsam_por_rnsam_unit_info (high)



The following table shows the por_rnsam_unit_info higher register bit assignments.

Table 5-1024: por_rnsam_por_rnsam_unit_info (high)

Bits	Field name	Description	Type	Reset
63:53	Reserved	Reserved	RO	-
52:48	num_qos_regions	Number of QoS override regions supported	RO	Configuration dependent
47:38	Reserved	Reserved	RO	-
37:32	num_non_hash_group	Number of non-hashed groups supported	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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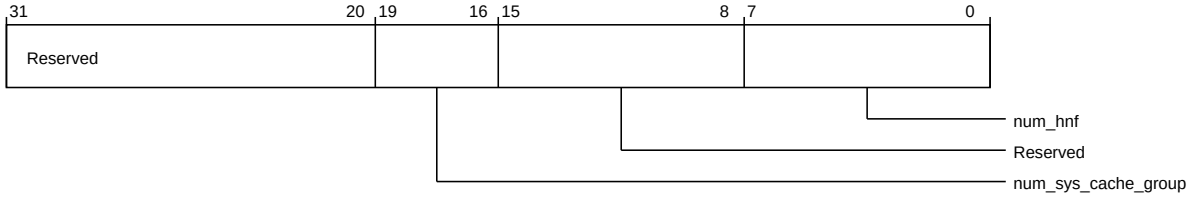
Figure 5-1011: por_rnsam_por_rnsam_unit_info (low)



The following table shows the por_rnsam_unit_info lower register bit assignments.

Table 5-1025: por_rnsam_por_rnsam_unit_info (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	num_sys_cache_group	Number of system cache groups supported	RO	Configuration dependent
15:8	Reserved	Reserved	RO	-
7:0	num_hnf	Number of hashed targets supported	RO	Configuration dependent

5.3.9.5 non_hash_mem_region_reg0

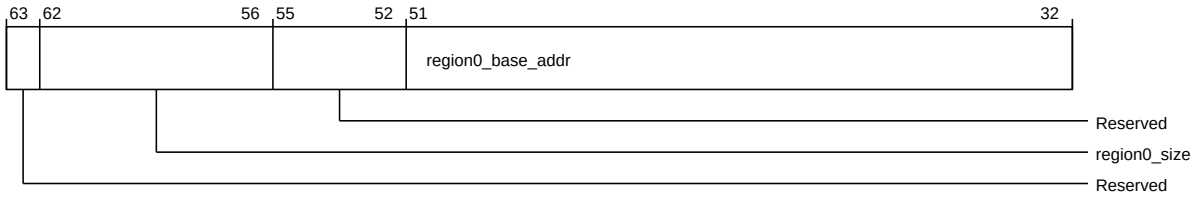
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1012: por_rnsam_non_hash_mem_region_reg0 (high)



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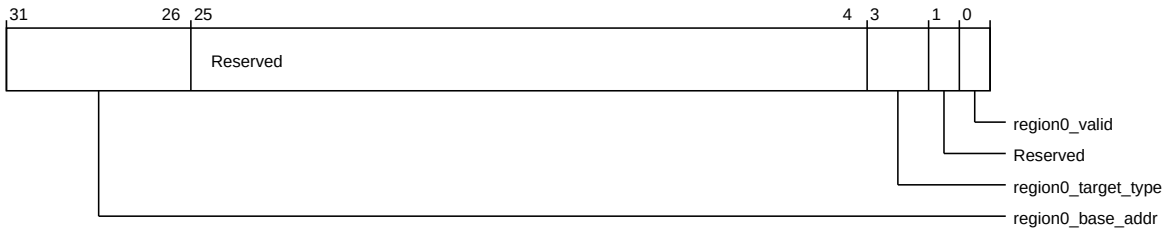
The following table shows the non_hash_mem_region_reg0 higher register bit assignments.

Table 5-1026: por_rnsam_non_hash_mem_region_reg0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region0_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1013: por_rnsam_non_hash_mem_region_reg0 (low)



The following table shows the non_hash_mem_region_reg0 lower register bit assignments.

Table 5-1027: por_rnsam_non_hash_mem_region_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	region0_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.6 non_hash_mem_region_reg1

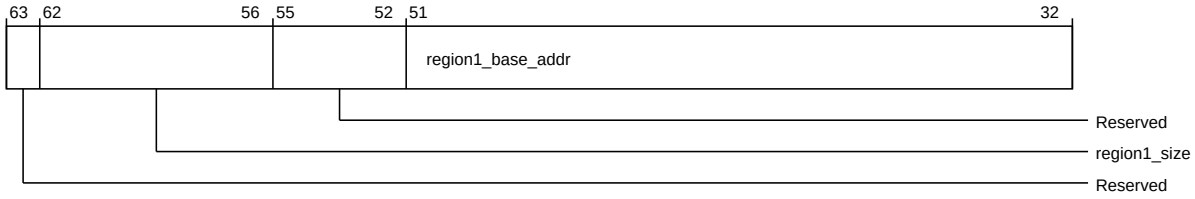
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1014: por_rnsam_non_hash_mem_region_reg1 (high)



The following table shows the non_hash_mem_region_reg1 higher register bit assignments.

Table 5-1028: por_rnsam_non_hash_mem_region_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region1_size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-

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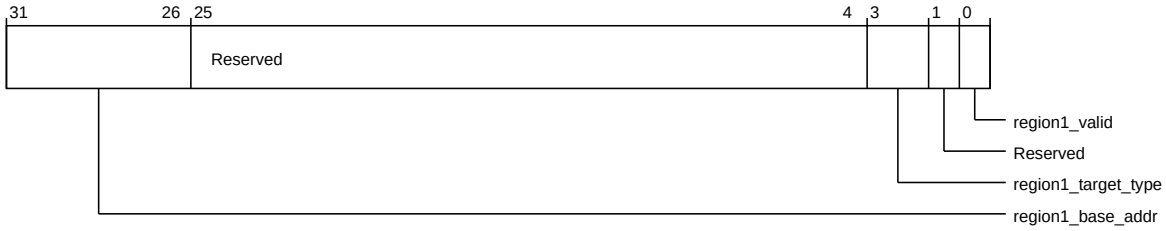
Bits	Field name	Description	Type	Reset
51:32	region1_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1015: por_rnsam_non_hash_mem_region_reg1 (low)



The following table shows the non_hash_mem_region_reg1 lower register bit assignments.

Table 5-1029: por_rnsam_non_hash_mem_region_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	region1_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region1_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region1_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.7 non_hash_mem_region_reg2

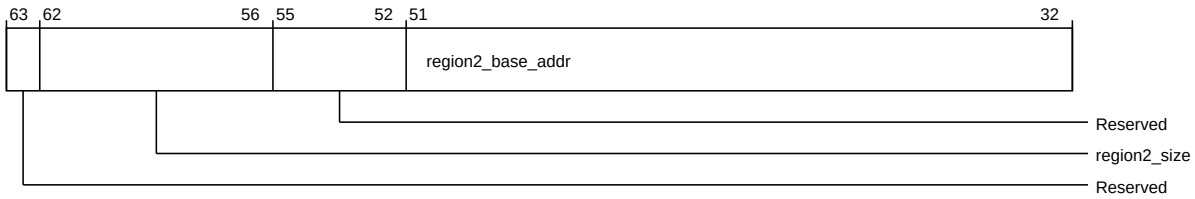
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1016: por_rnsam_non_hash_mem_region_reg2 (high)



The following table shows the non_hash_mem_region_reg2 higher register bit assignments.

Table 5-1030: por_rnsam_non_hash_mem_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region2_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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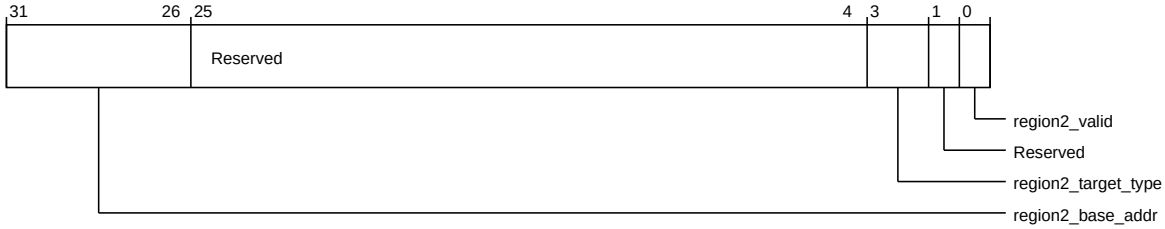
Figure 5-1017: por_rnsam_non_hash_mem_region_reg2 (low)



The following table shows the non_hash_mem_region_reg2 lower register bit assignments.

Table 5-1031: por_rnsam_non_hash_mem_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	region2_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.8 non_hash_mem_region_reg3

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC18
Register reset 64'b0

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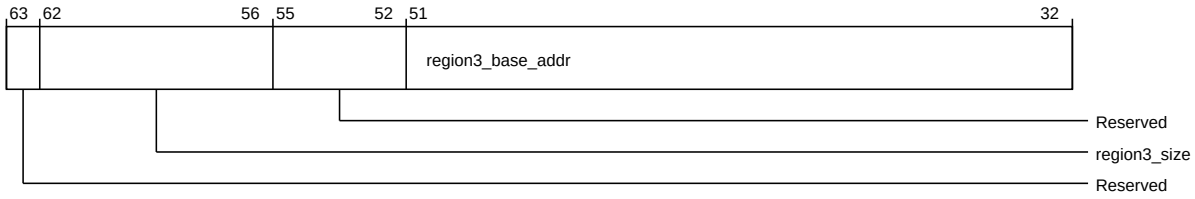
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1018: por_rnsam_non_hash_mem_region_reg3 (high)



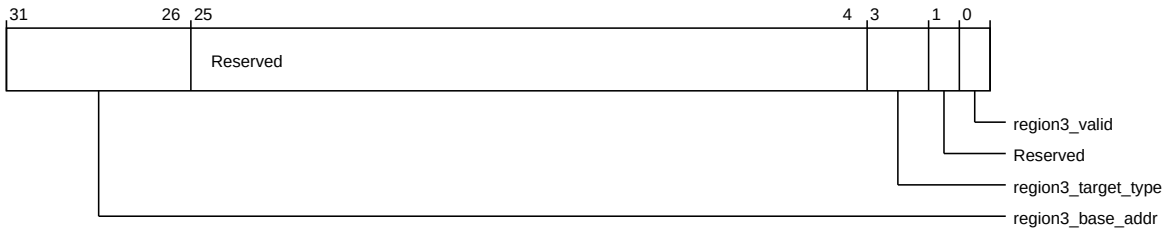
The following table shows the non_hash_mem_region_reg3 higher register bit assignments.

Table 5-1032: por_rnsam_non_hash_mem_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region3_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1019: por_rnsam_non_hash_mem_region_reg3 (low)



The following table shows the non_hash_mem_region_reg3 lower register bit assignments.

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Table 5-1033: por_rnsam_non_hash_mem_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	region3_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.9 non_hash_mem_region_reg4

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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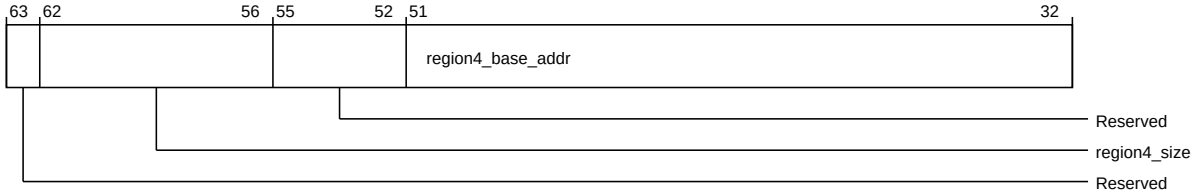
Figure 5-1020: por_rnsam_non_hash_mem_region_reg4 (high)



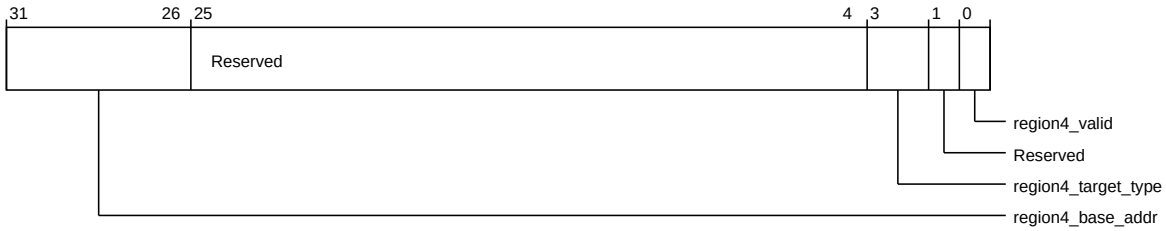
The following table shows the non_hash_mem_region_reg4 higher register bit assignments.

Table 5-1034: por_rnsam_non_hash_mem_region_reg4 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region4_size	Memory region 4 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region4_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 4 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1021: por_rnsam_non_hash_mem_region_reg4 (low)



The following table shows the non_hash_mem_region_reg4 lower register bit assignments.

Table 5-1035: por_rnsam_non_hash_mem_region_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	region4_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 4 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region4_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region4_valid	Memory region 4 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.10 non_hash_mem_region_reg5

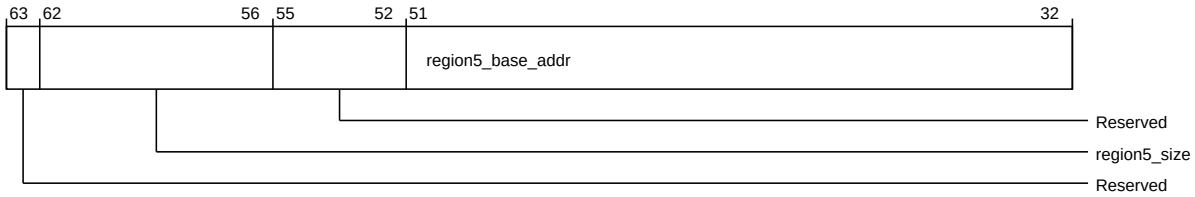
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1022: por_rnsam_non_hash_mem_region_reg5 (high)



The following table shows the non_hash_mem_region_reg5 higher register bit assignments.

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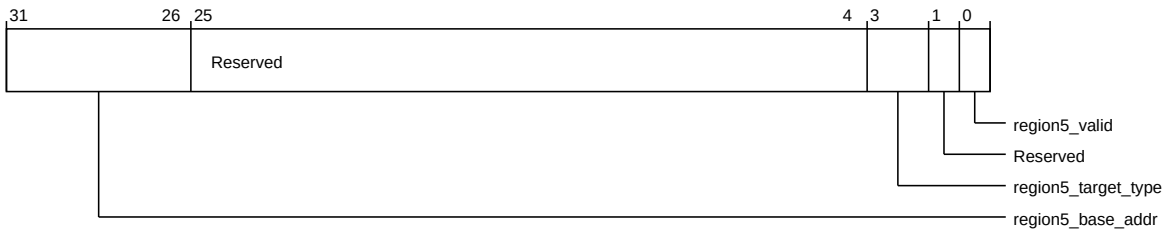
Table 5-1036: por_rnsam_non_hash_mem_region_reg5 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region5_size	Memory region 5 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region5_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 5 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1023: por_rnsam_non_hash_mem_region_reg5 (low)



The following table shows the non_hash_mem_region_reg5 lower register bit assignments.

Table 5-1037: por_rnsam_non_hash_mem_region_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	region5_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 5 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region5_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	region5_valid	Memory region 5 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.11 non_hash_mem_region_reg6

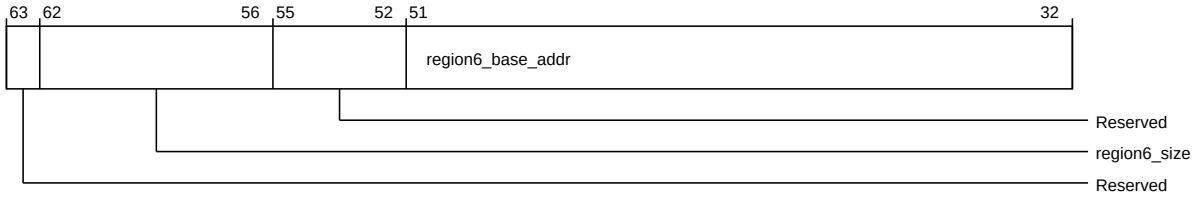
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1024: por_rnsam_non_hash_mem_region_reg6 (high)



The following table shows the non_hash_mem_region_reg6 higher register bit assignments.

Table 5-1038: por_rnsam_non_hash_mem_region_reg6 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region6_size	Memory region 6 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-

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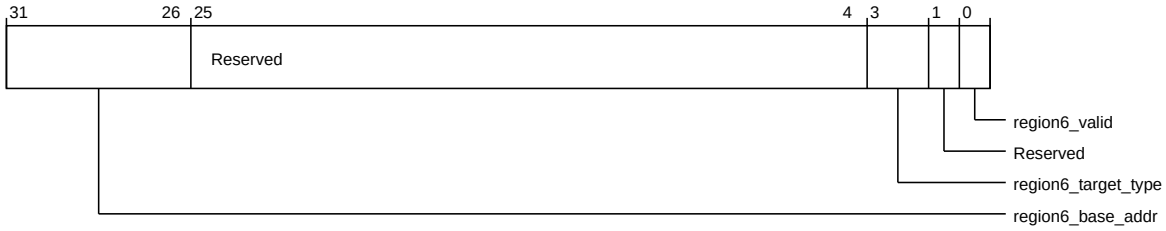
Bits	Field name	Description	Type	Reset
51:32	region6_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 6 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1025: por_rnsam_non_hash_mem_region_reg6 (low)



The following table shows the non_hash_mem_region_reg6 lower register bit assignments.

Table 5-1039: por_rnsam_non_hash_mem_region_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	region6_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 6 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region6_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region6_valid	Memory region 6 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.12 non_hash_mem_region_reg7

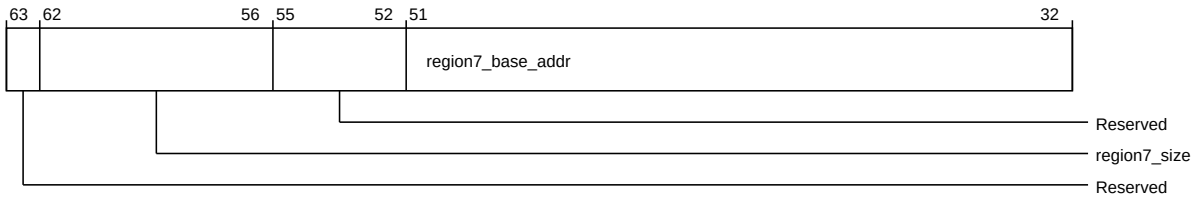
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1026: por_rnsam_non_hash_mem_region_reg7 (high)



The following table shows the non_hash_mem_region_reg7 higher register bit assignments.

Table 5-1040: por_rnsam_non_hash_mem_region_reg7 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region7_size	Memory region 7 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region7_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 7 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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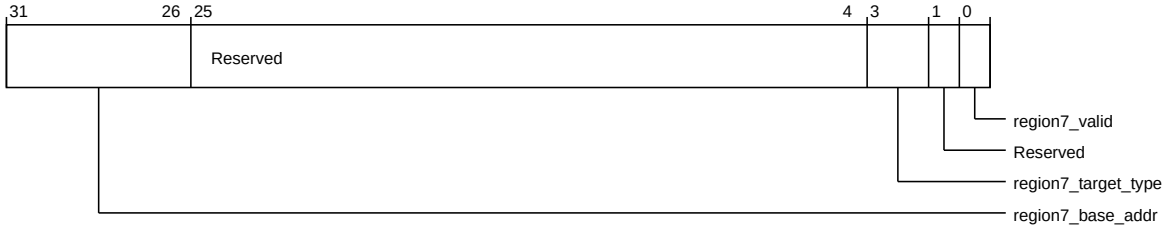
Figure 5-1027: por_rnsam_non_hash_mem_region_reg7 (low)



The following table shows the non_hash_mem_region_reg7 lower register bit assignments.

Table 5-1041: por_rnsam_non_hash_mem_region_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	region7_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 7 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region7_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region7_valid	Memory region 7 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.13 non_hash_mem_region_reg8

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC40
Register reset 64'b0

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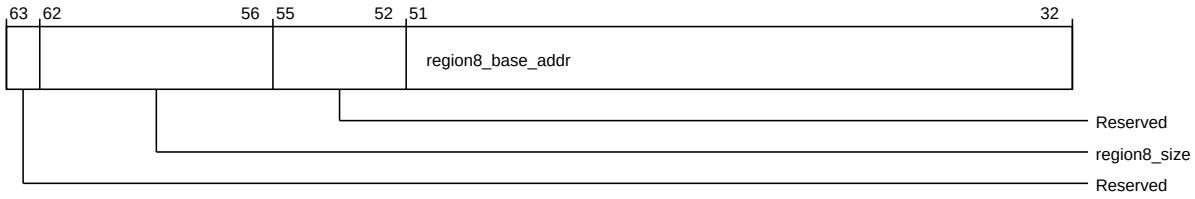
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1028: por_rnsam_non_hash_mem_region_reg8 (high)



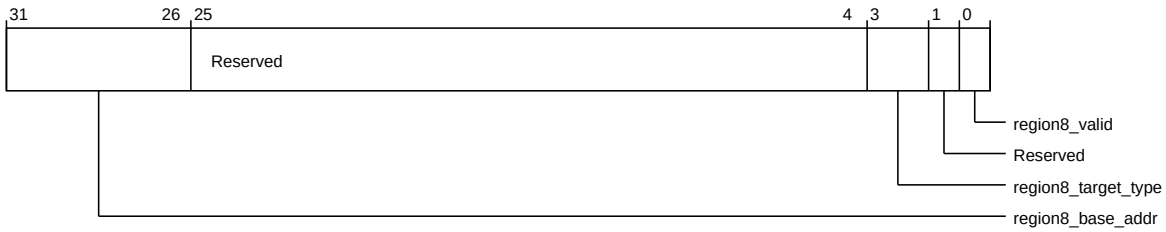
The following table shows the non_hash_mem_region_reg8 higher register bit assignments.

Table 5-1042: por_rnsam_non_hash_mem_region_reg8 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region8_size	Memory region 8 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region8_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 8 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1029: por_rnsam_non_hash_mem_region_reg8 (low)



The following table shows the non_hash_mem_region_reg8 lower register bit assignments.

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Table 5-1043: por_rnsam_non_hash_mem_region_reg8 (low)

Bits	Field name	Description	Type	Reset
31:26	region8_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 8 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region8_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region8_valid	Memory region 8 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.14 non_hash_mem_region_reg9

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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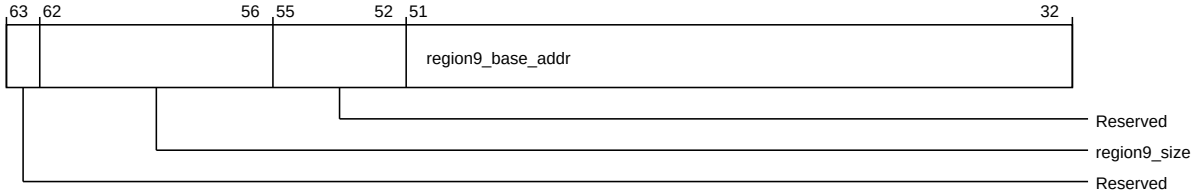
Figure 5-1030: por_rnsam_non_hash_mem_region_reg9 (high)



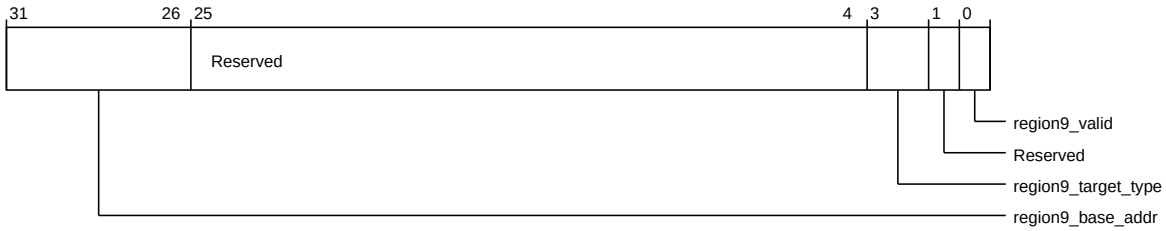
The following table shows the non_hash_mem_region_reg9 higher register bit assignments.

Table 5-1044: por_rnsam_non_hash_mem_region_reg9 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region9_size	Memory region 9 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region9_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 9 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1031: por_rnsam_non_hash_mem_region_reg9 (low)



The following table shows the non_hash_mem_region_reg9 lower register bit assignments.

Table 5-1045: por_rnsam_non_hash_mem_region_reg9 (low)

Bits	Field name	Description	Type	Reset
31:26	region9_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 9 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region9_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region9_valid	Memory region 9 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.15 non_hash_mem_region_reg10

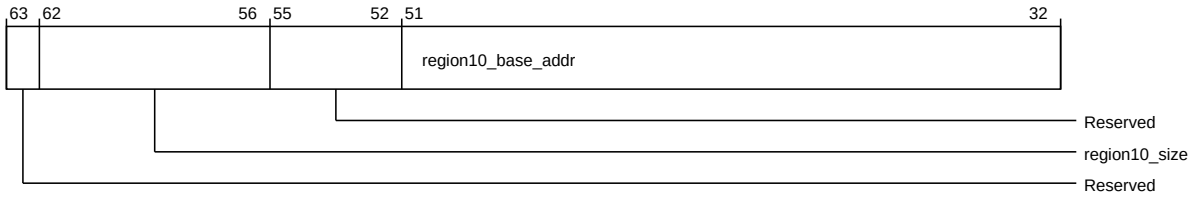
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1032: por_rnsam_non_hash_mem_region_reg10 (high)



The following table shows the non_hash_mem_region_reg10 higher register bit assignments.

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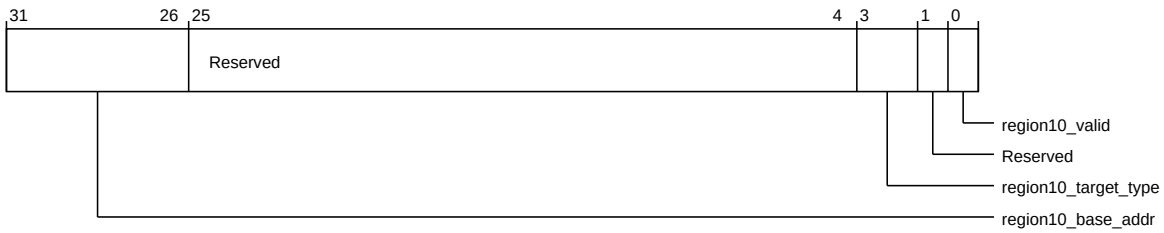
Table 5-1046: por_rnsam_non_hash_mem_region_reg10 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region10_size	Memory region 10 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region10_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 10 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1033: por_rnsam_non_hash_mem_region_reg10 (low)



The following table shows the non_hash_mem_region_reg10 lower register bit assignments.

Table 5-1047: por_rnsam_non_hash_mem_region_reg10 (low)

Bits	Field name	Description	Type	Reset
31:26	region10_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 10 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region10_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	region10_valid	Memory region 10 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.16 non_hash_mem_region_reg11

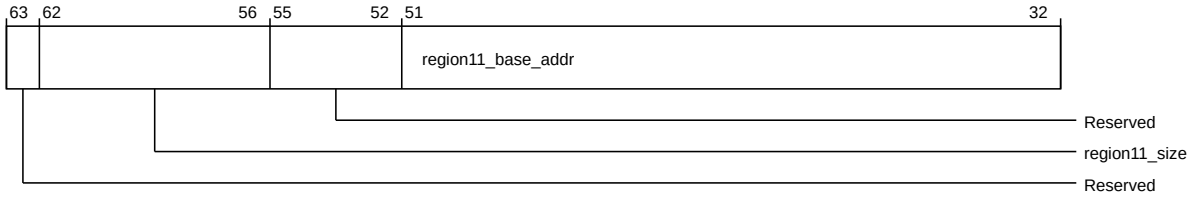
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1034: por_rnsam_non_hash_mem_region_reg11 (high)



The following table shows the non_hash_mem_region_reg11 higher register bit assignments.

Table 5-1048: por_rnsam_non_hash_mem_region_reg11 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region11_size	Memory region 11 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-

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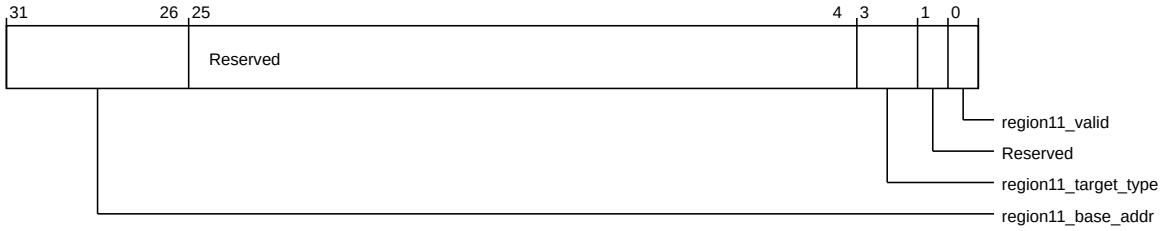
Bits	Field name	Description	Type	Reset
51:32	region11_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 11 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1035: por_rnsam_non_hash_mem_region_reg11 (low)



The following table shows the non_hash_mem_region_reg11 lower register bit assignments.

Table 5-1049: por_rnsam_non_hash_mem_region_reg11 (low)

Bits	Field name	Description	Type	Reset
31:26	region11_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 11 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region11_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region11_valid	Memory region 11 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.17 non_hash_mem_region_reg12

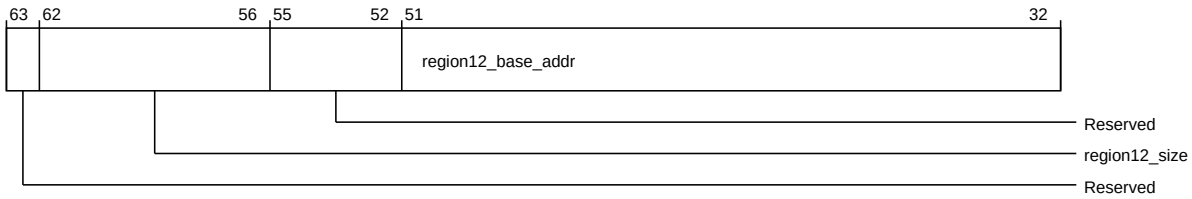
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1036: por_rnsam_non_hash_mem_region_reg12 (high)



The following table shows the non_hash_mem_region_reg12 higher register bit assignments.

Table 5-1050: por_rnsam_non_hash_mem_region_reg12 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region12_size	Memory region 12 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region12_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 12 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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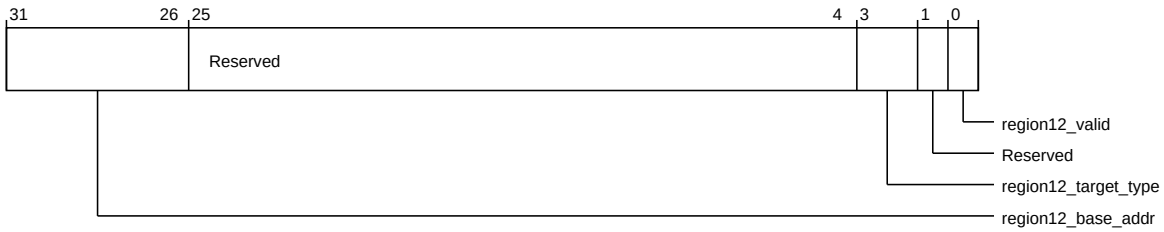
Figure 5-1037: por_rnsam_non_hash_mem_region_reg12 (low)



The following table shows the non_hash_mem_region_reg12 lower register bit assignments.

Table 5-1051: por_rnsam_non_hash_mem_region_reg12 (low)

Bits	Field name	Description	Type	Reset
31:26	region12_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 12 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region12_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region12_valid	Memory region 12 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.18 non_hash_mem_region_reg13

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC68

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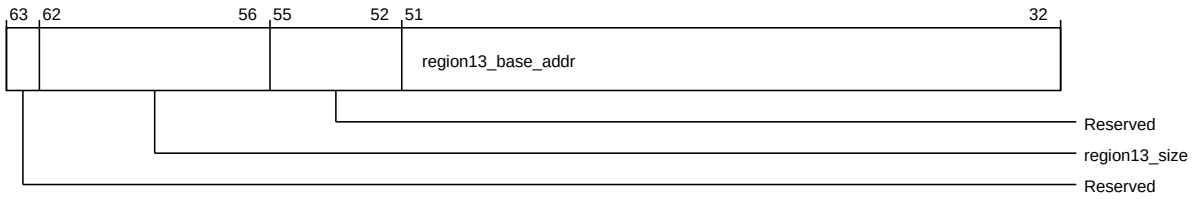
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1038: por_rnsam_non_hash_mem_region_reg13 (high)



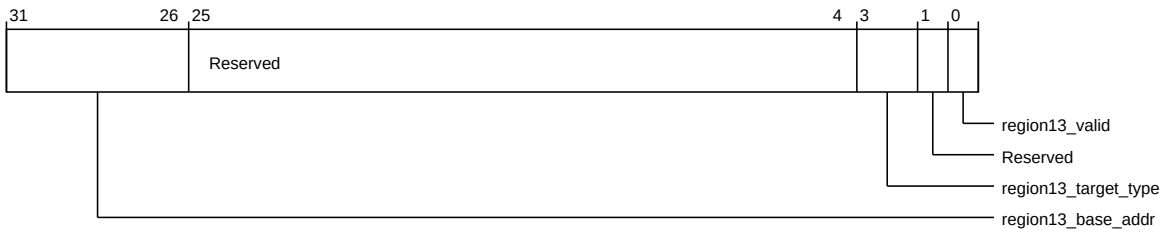
The following table shows the non_hash_mem_region_reg13 higher register bit assignments.

Table 5-1052: por_rnsam_non_hash_mem_region_reg13 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region13_size	Memory region 13 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region13_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 13 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1039: por_rnsam_non_hash_mem_region_reg13 (low)



The following table shows the non_hash_mem_region_reg13 lower register bit assignments.

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Table 5-1053: por_rnsam_non_hash_mem_region_reg13 (low)

Bits	Field name	Description	Type	Reset
31:26	region13_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 13 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region13_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region13_valid	Memory region 13 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.19 non_hash_mem_region_reg14

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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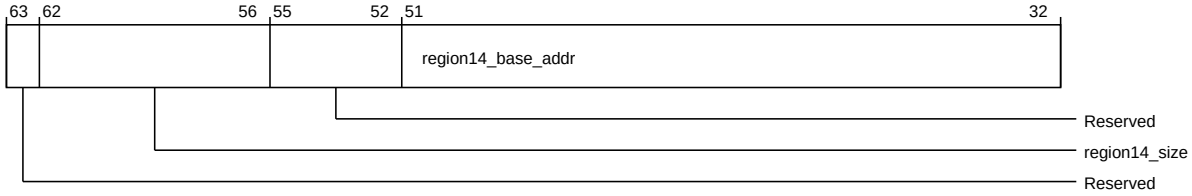
Figure 5-1040: por_rnsam_non_hash_mem_region_reg14 (high)



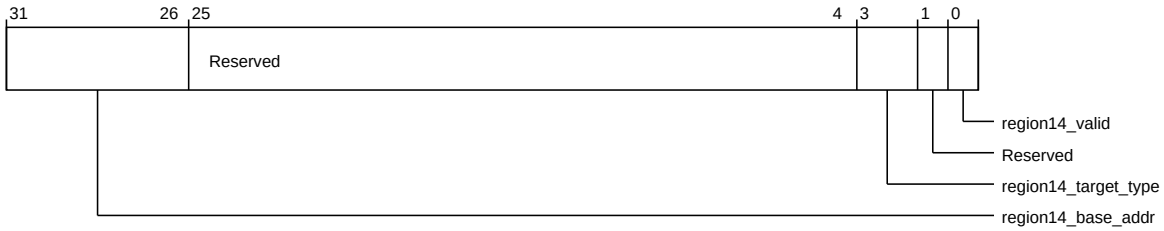
The following table shows the non_hash_mem_region_reg14 higher register bit assignments.

Table 5-1054: por_rnsam_non_hash_mem_region_reg14 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region14_size	Memory region 14 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region14_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 14 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1041: por_rnsam_non_hash_mem_region_reg14 (low)



The following table shows the non_hash_mem_region_reg14 lower register bit assignments.

Table 5-1055: por_rnsam_non_hash_mem_region_reg14 (low)

Bits	Field name	Description	Type	Reset
31:26	region14_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 14 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region14_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region14_valid	Memory region 14 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.20 non_hash_mem_region_reg15

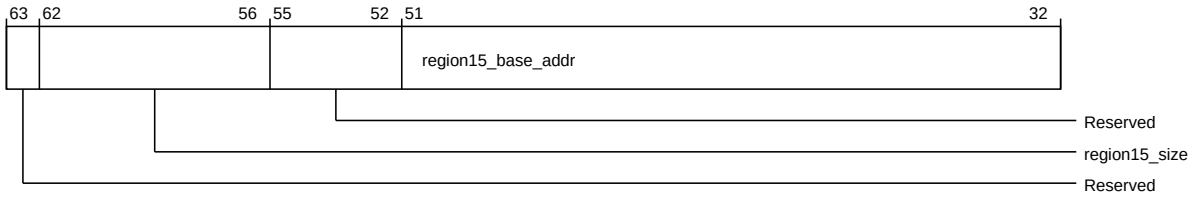
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1042: por_rnsam_non_hash_mem_region_reg15 (high)



The following table shows the non_hash_mem_region_reg15 higher register bit assignments.

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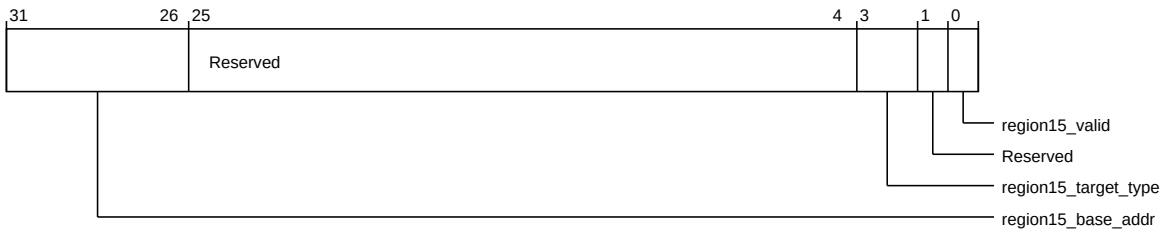
Table 5-1056: por_rnsam_non_hash_mem_region_reg15 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region15_size	Memory region 15 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region15_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 15 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1043: por_rnsam_non_hash_mem_region_reg15 (low)



The following table shows the non_hash_mem_region_reg15 lower register bit assignments.

Table 5-1057: por_rnsam_non_hash_mem_region_reg15 (low)

Bits	Field name	Description	Type	Reset
31:26	region15_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 15 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region15_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
0	region15_valid	Memory region 15 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.21 non_hash_mem_region_reg16

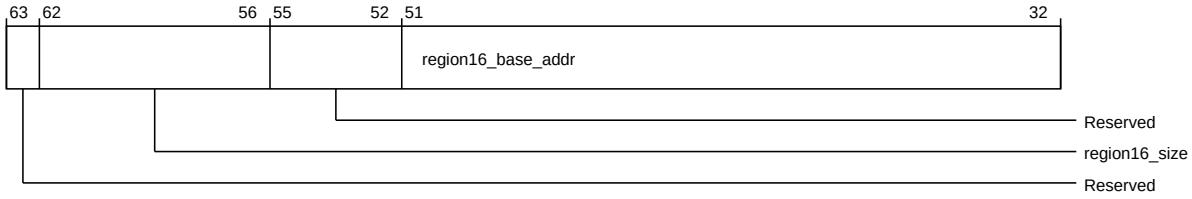
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1044: por_rnsam_non_hash_mem_region_reg16 (high)



The following table shows the non_hash_mem_region_reg16 higher register bit assignments.

Table 5-1058: por_rnsam_non_hash_mem_region_reg16 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region16_size	Memory region 16 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-

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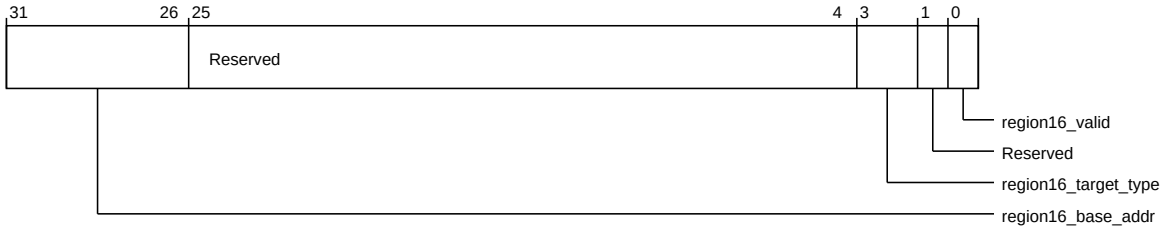
Bits	Field name	Description	Type	Reset
51:32	region16_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 16 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1045: por_rnsam_non_hash_mem_region_reg16 (low)



The following table shows the non_hash_mem_region_reg16 lower register bit assignments.

Table 5-1059: por_rnsam_non_hash_mem_region_reg16 (low)

Bits	Field name	Description	Type	Reset
31:26	region16_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 16 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region16_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region16_valid	Memory region 16 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.22 non_hash_mem_region_reg17

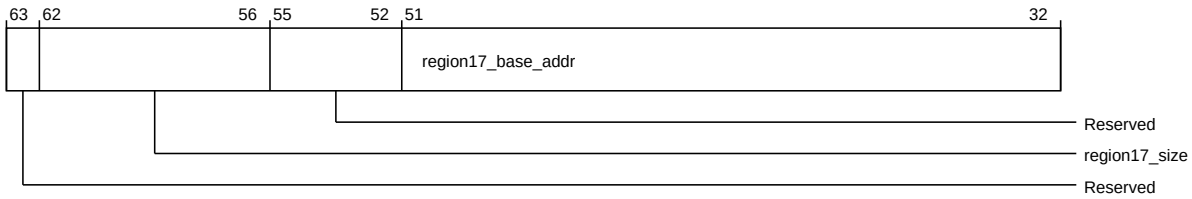
Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1046: por_rnsam_non_hash_mem_region_reg17 (high)



The following table shows the non_hash_mem_region_reg17 higher register bit assignments.

Table 5-1060: por_rnsam_non_hash_mem_region_reg17 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region17_size	Memory region 17 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region17_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 17 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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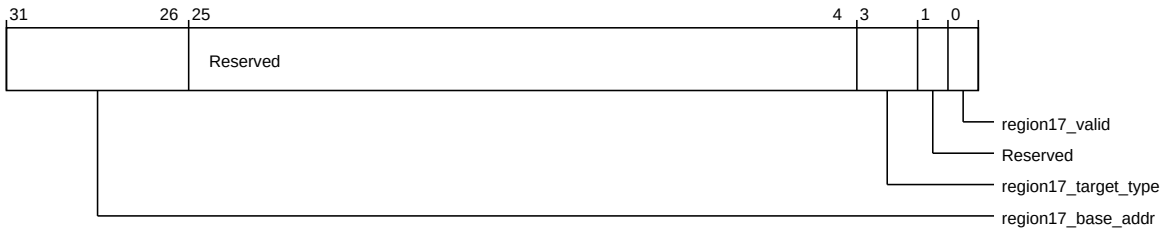
Figure 5-1047: por_rnsam_non_hash_mem_region_reg17 (low)



The following table shows the non_hash_mem_region_reg17 lower register bit assignments.

Table 5-1061: por_rnsam_non_hash_mem_region_reg17 (low)

Bits	Field name	Description	Type	Reset
31:26	region17_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 17 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region17_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region17_valid	Memory region 17 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.23 non_hash_mem_region_reg18

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC90

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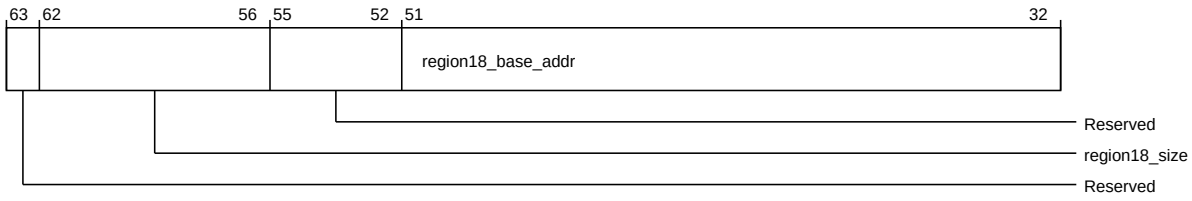
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1048: por_rnsam_non_hash_mem_region_reg18 (high)



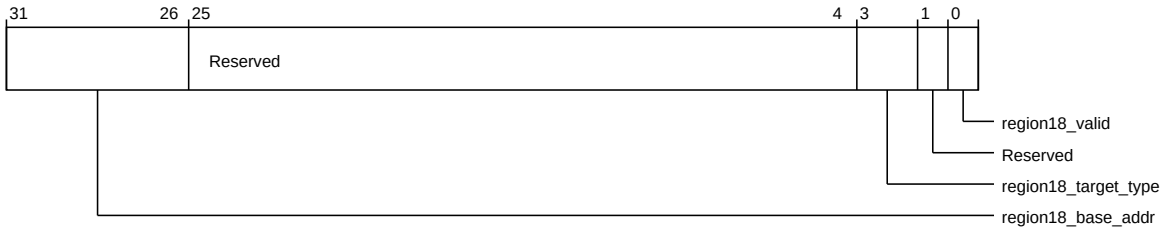
The following table shows the non_hash_mem_region_reg18 higher register bit assignments.

Table 5-1062: por_rnsam_non_hash_mem_region_reg18 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region18_size	Memory region 18 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region18_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 18 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1049: por_rnsam_non_hash_mem_region_reg18 (low)



The following table shows the non_hash_mem_region_reg18 lower register bit assignments.

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Table 5-1063: por_rnsam_non_hash_mem_region_reg18 (low)

Bits	Field name	Description	Type	Reset
31:26	region18_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 18 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region18_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region18_valid	Memory region 18 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.24 non_hash_mem_region_reg19

Configures non-hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hC98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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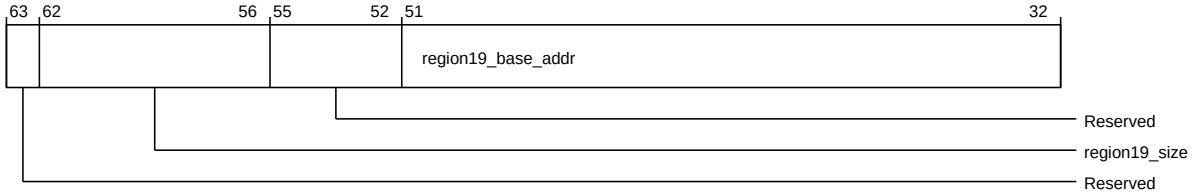
Figure 5-1050: por_rnsam_non_hash_mem_region_reg19 (high)



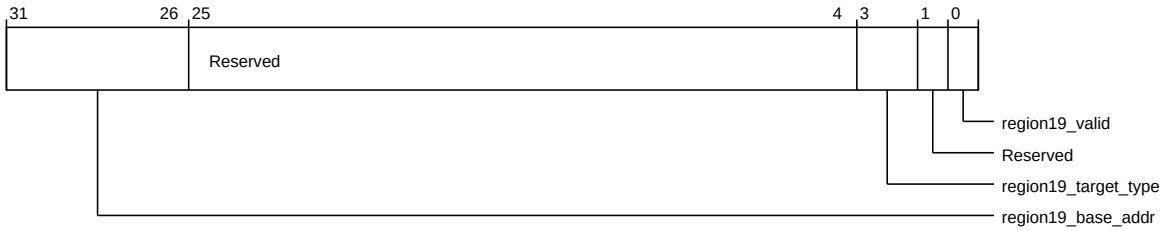
The following table shows the non_hash_mem_region_reg19 higher register bit assignments.

Table 5-1064: por_rnsam_non_hash_mem_region_reg19 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region19_size	Memory region 19 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region19_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 19 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1051: por_rnsam_non_hash_mem_region_reg19 (low)



The following table shows the non_hash_mem_region_reg19 lower register bit assignments.

Table 5-1065: por_rnsam_non_hash_mem_region_reg19 (low)

Bits	Field name	Description	Type	Reset
31:26	region19_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 19 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region19_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region19_valid	Memory region 19 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.25 non_hash_tgt_nodeid0

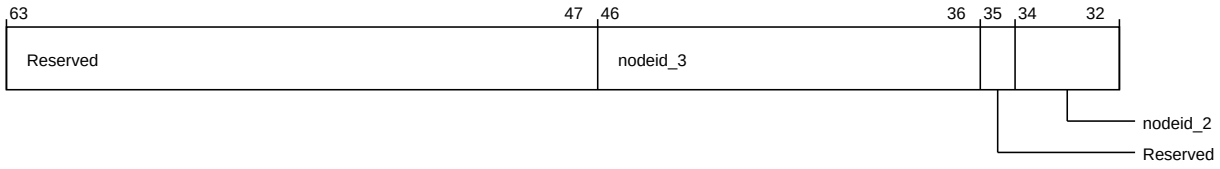
Configures non-hashed target node IDs 0 to 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD80
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1052: por_rnsam_non_hash_tgt_nodeid0 (high)



The following table shows the non_hash_tgt_nodeid0 higher register bit assignments.

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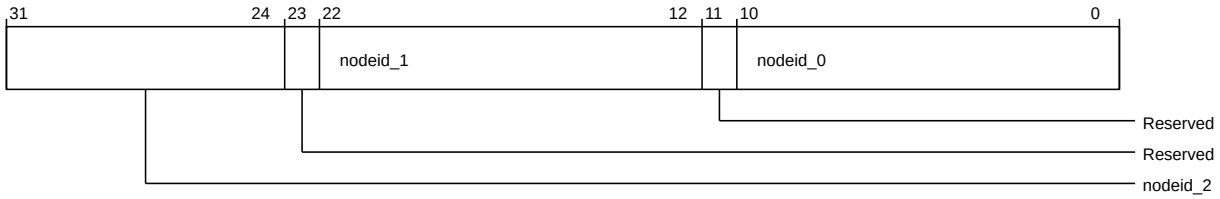
Table 5-1066: por_rnsam_non_hash_tgt_nodeid0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_3	Non-hashed target node ID 3	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_2	Non-hashed target node ID 2	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1053: por_rnsam_non_hash_tgt_nodeid0 (low)



The following table shows the non_hash_tgt_nodeid0 lower register bit assignments.

Table 5-1067: por_rnsam_non_hash_tgt_nodeid0 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_2	Non-hashed target node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_1	Non-hashed target node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_0	Non-hashed target node ID 0	RW	11'b00000000000

5.3.9.26 non_hash_tgt_nodeid1

Configures non-hashed target node IDs 4 to 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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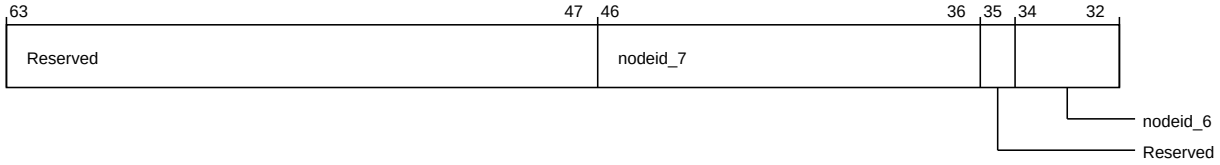
Figure 5-1054: por_rnsam_non_hash_tgt_nodeid1 (high)



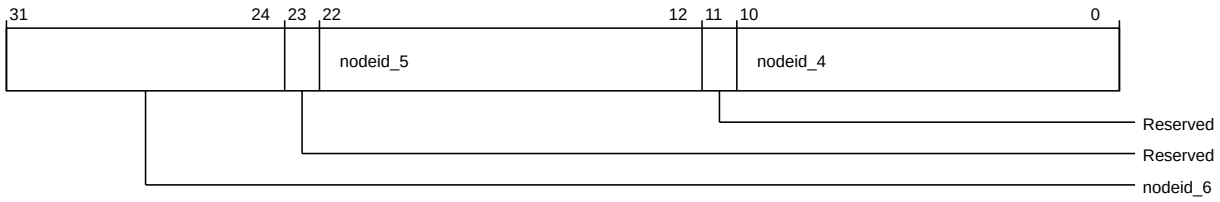
The following table shows the non_hash_tgt_nodeid1 higher register bit assignments.

Table 5-1068: por_rnsam_non_hash_tgt_nodeid1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_7	Non-hashed target node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_6	Non-hashed target node ID 6	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1055: por_rnsam_non_hash_tgt_nodeid1 (low)



The following table shows the non_hash_tgt_nodeid1 lower register bit assignments.

Table 5-1069: por_rnsam_non_hash_tgt_nodeid1 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_6	Non-hashed target node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_5	Non-hashed target node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_4	Non-hashed target node ID 4	RW	11'b00000000000

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5.3.9.27 non_hash_tgt_nodeid2

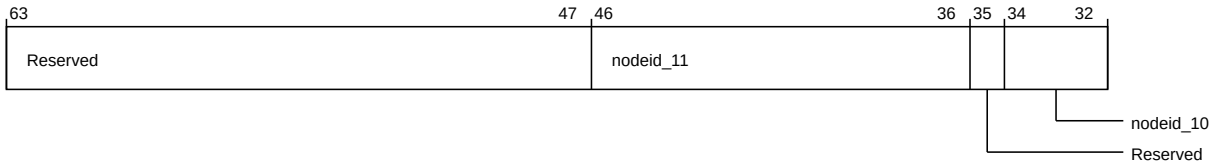
Configures non-hashed target node IDs 8 to 11.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD90
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1056: por_rnsam_non_hash_tgt_nodeid2 (high)



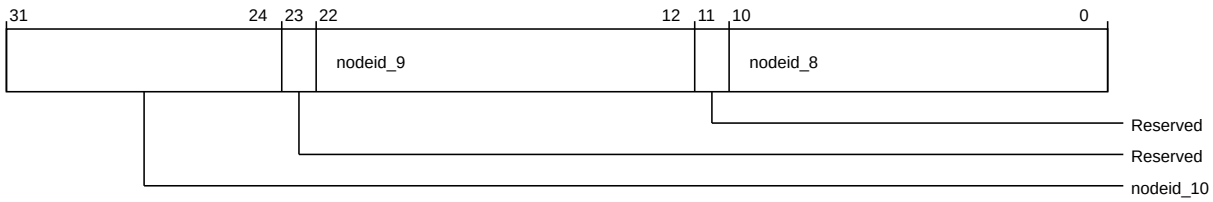
The following table shows the non_hash_tgt_nodeid2 higher register bit assignments.

Table 5-1070: por_rnsam_non_hash_tgt_nodeid2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_11	Non-hashed target node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_10	Non-hashed target node ID 10	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1057: por_rnsam_non_hash_tgt_nodeid2 (low)



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The following table shows the non_hash_tgt_nodeid2 lower register bit assignments.

Table 5-1071: por_rnsam_non_hash_tgt_nodeid2 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_10	Non-hashed target node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_9	Non-hashed target node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Non-hashed target node ID 8	RW	11'b00000000000

5.3.9.28 non_hash_tgt_nodeid3

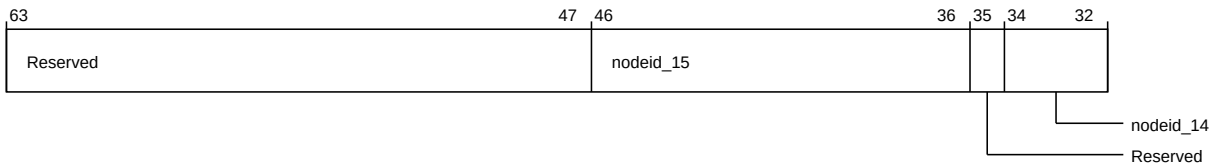
Configures non-hashed target node IDs 12 to 15.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hD98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1058: por_rnsam_non_hash_tgt_nodeid3 (high)



The following table shows the non_hash_tgt_nodeid3 higher register bit assignments.

Table 5-1072: por_rnsam_non_hash_tgt_nodeid3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_15	Non-hashed target node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_14	Non-hashed target node ID 14	RW	11'b00000000000

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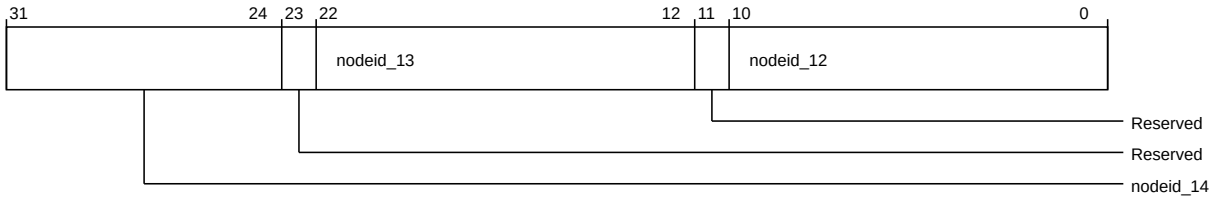
The following figure shows the lower register bit assignments.

Figure 5-1059: por_rnsam_non_hash_tgt_nodeid3 (low)



The following table shows the non_hash_tgt_nodeid3 lower register bit assignments.

Table 5-1073: por_rnsam_non_hash_tgt_nodeid3 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_14	Non-hashed target node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_13	Non-hashed target node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_12	Non-hashed target node ID 12	RW	11'b00000000000

5.3.9.29 non_hash_tgt_nodeid4

Configures non-hashed target node IDs 16 to 19.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hDA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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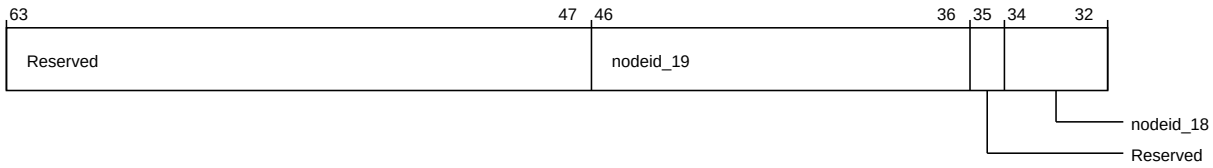
Figure 5-1060: por_rnsam_non_hash_tgt_nodeid4 (high)



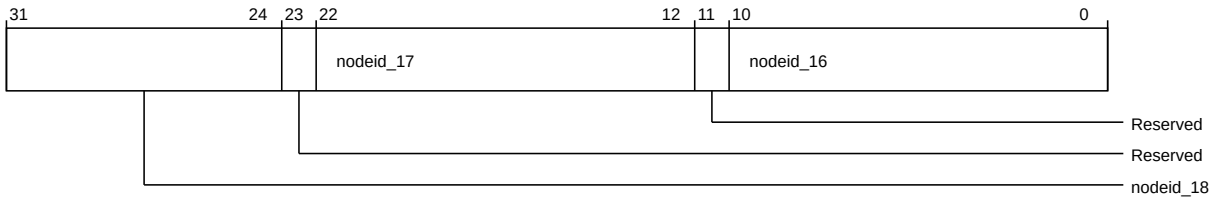
The following table shows the non_hash_tgt_nodeid4 higher register bit assignments.

Table 5-1074: por_rnsam_non_hash_tgt_nodeid4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_19	Non-hashed target node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_18	Non-hashed target node ID 18	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1061: por_rnsam_non_hash_tgt_nodeid4 (low)



The following table shows the non_hash_tgt_nodeid4 lower register bit assignments.

Table 5-1075: por_rnsam_non_hash_tgt_nodeid4 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_18	Non-hashed target node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_17	Non-hashed target node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_16	Non-hashed target node ID 16	RW	11'b00000000000

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5.3.9.30 sys_cache_grp_region0

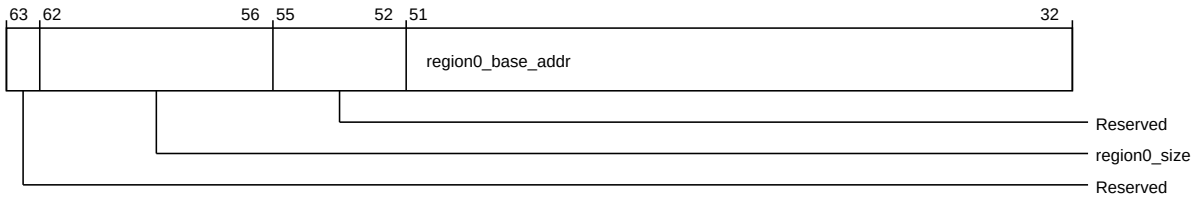
Configures hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1062: por_rnsam_sys_cache_grp_region0 (high)



The following table shows the sys_cache_grp_region0 higher register bit assignments.

Table 5-1076: por_rnsam_sys_cache_grp_region0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region0_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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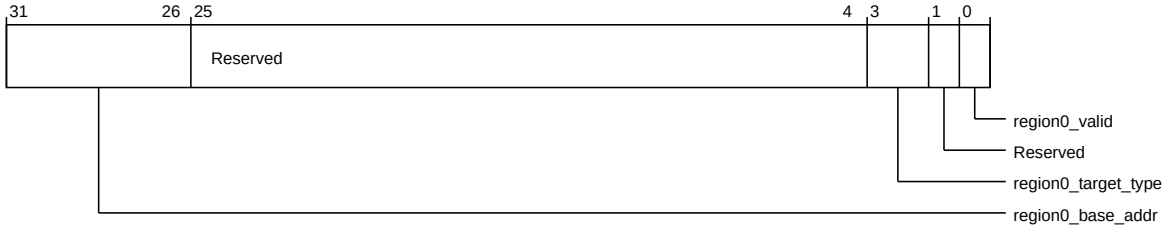
Figure 5-1063: por_rnsam_sys_cache_grp_region0 (low)



The following table shows the sys_cache_grp_region0 lower register bit assignments.

Table 5-1077: por_rnsam_sys_cache_grp_region0 (low)

Bits	Field name	Description	Type	Reset
31:26	region0_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.31 sys_cache_grp_region1

Configures hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE08
Register reset 64'b0

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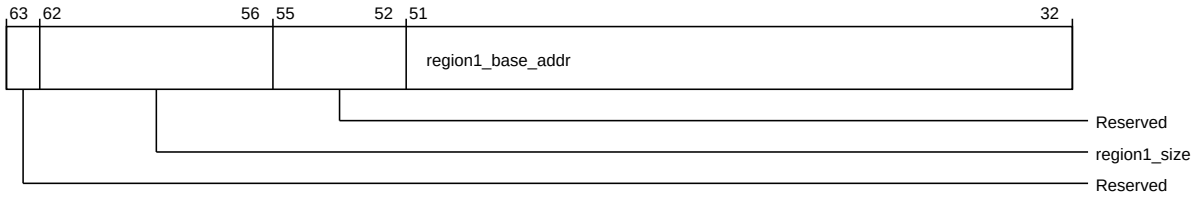
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1064: por_rnsam_sys_cache_grp_region1 (high)



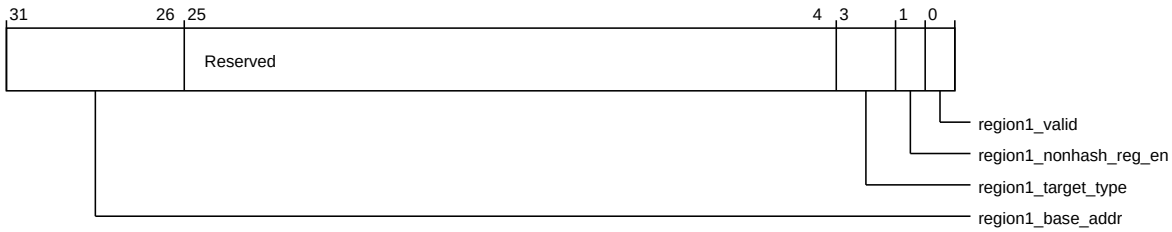
The following table shows the sys_cache_grp_region1 higher register bit assignments.

Table 5-1078: por_rnsam_sys_cache_grp_region1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region1_size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	7'b0000000
55:52	Reserved	Reserved	RO	-
51:32	region1_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1065: por_rnsam_sys_cache_grp_region1 (low)



The following table shows the sys_cache_grp_region1 lower register bit assignments.

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Table 5-1079: por_rnsam_sys_cache_grp_region1 (low)

Bits	Field name	Description	Type	Reset
31:26	region1_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region1_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	region1_nonhash_reg_en	Enables hashed region 1 to select non-hashed node	RW	1'b0
0	region1_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.32 sys_cache_grp_region2

Configures hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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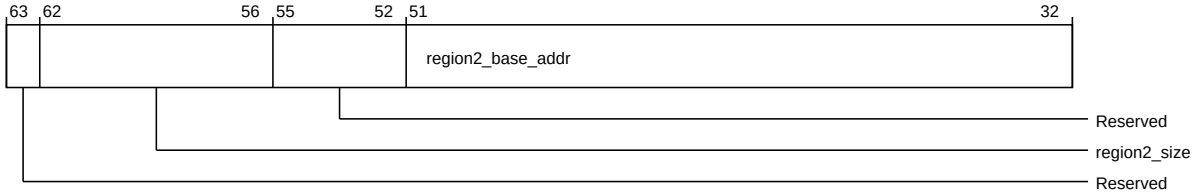
Figure 5-1066: por_rnsam_sys_cache_grp_region2 (high)



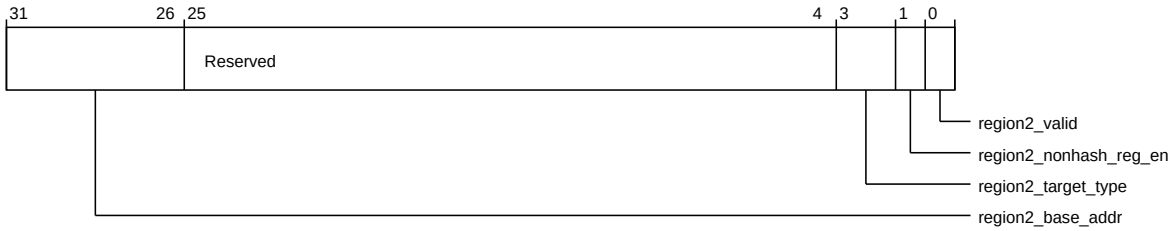
The following table shows the sys_cache_grp_region2 higher register bit assignments.

Table 5-1080: por_rnsam_sys_cache_grp_region2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	region2_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1067: por_rnsam_sys_cache_grp_region2 (low)



The following table shows the sys_cache_grp_region2 lower register bit assignments.

Table 5-1081: por_rnsam_sys_cache_grp_region2 (low)

Bits	Field name	Description	Type	Reset
31:26	region2_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	region2_nonhash_reg_en	Enables hashed region 2 to select non-hashed node	RW	1'b0
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.33 sys_cache_grp_region3

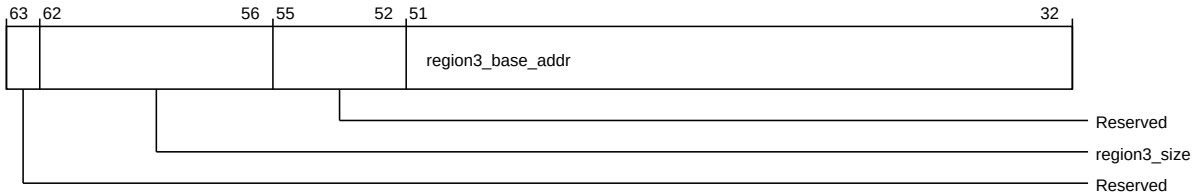
Configures hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1068: por_rnsam_sys_cache_grp_region3 (high)



The following table shows the sys_cache_grp_region3 higher register bit assignments.

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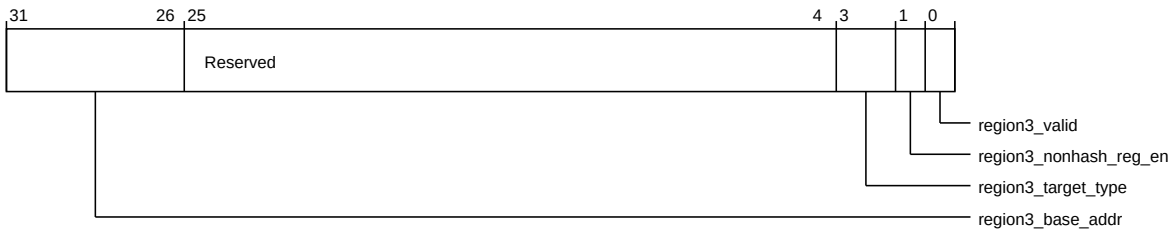
Table 5-1082: por_rnsam_sys_cache_grp_region3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	region3_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1069: por_rnsam_sys_cache_grp_region3 (low)



The following table shows the sys_cache_grp_region3 lower register bit assignments.

Table 5-1083: por_rnsam_sys_cache_grp_region3 (low)

Bits	Field name	Description	Type	Reset
31:26	region3_base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	region3_nonhash_reg_en	Enables hashed region 3 to select non-hashed node	RW	1'b0

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Bits	Field name	Description	Type	Reset
0	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.34 sys_cache_grp_secondary_reg0

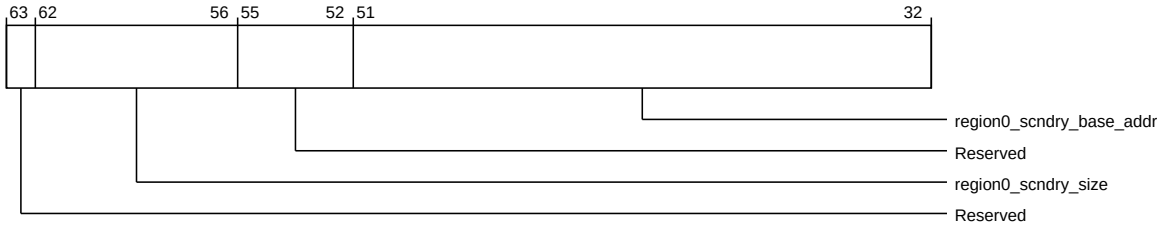
Configures secondary hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1070: por_rnsam_sys_cache_grp_secondary_reg0 (high)



The following table shows the sys_cache_grp_secondary_reg0 higher register bit assignments.

Table 5-1084: por_rnsam_sys_cache_grp_secondary_reg0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region0_scndry_size	Secondary memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-

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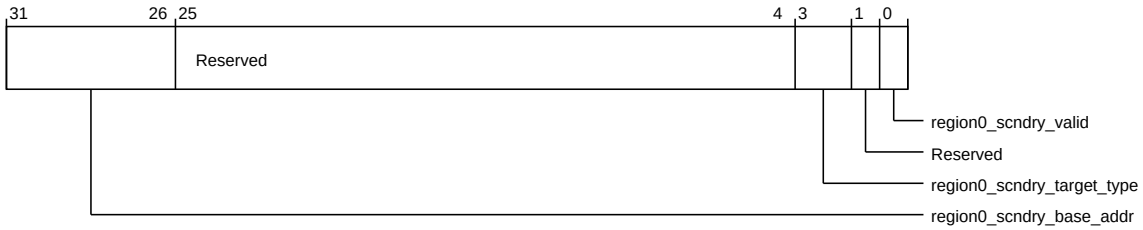
Bits	Field name	Description	Type	Reset
51:32	region0_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1071: por_rnsam_sys_cache_grp_secondary_reg0 (low)



The following table shows the sys_cache_grp_secondary_reg0 lower register bit assignments.

Table 5-1085: por_rnsam_sys_cache_grp_secondary_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	region0_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region0_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_scndry_valid	Secondary memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.35 sys_cache_grp_secondary_reg1

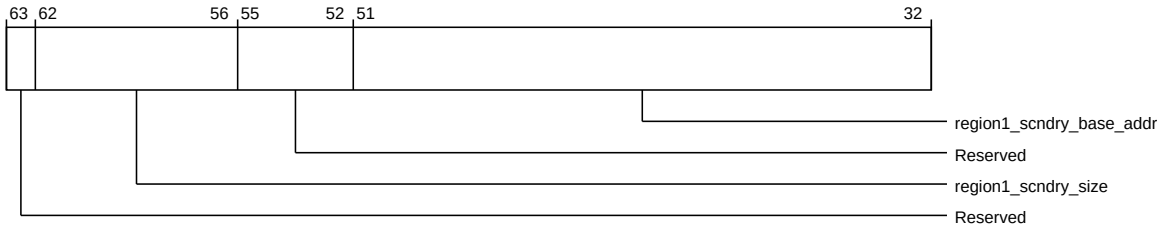
Configures secondary hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1072: por_rnsam_sys_cache_grp_secondary_reg1 (high)



The following table shows the sys_cache_grp_secondary_reg1 higher register bit assignments.

Table 5-1086: por_rnsam_sys_cache_grp_secondary_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region1_scndry_size	Secondary memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	region1_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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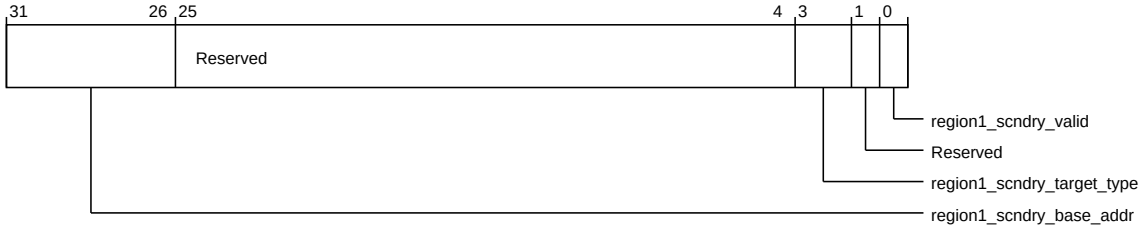
Figure 5-1073: por_rnsam_sys_cache_grp_secondary_reg1 (low)



The following table shows the sys_cache_grp_secondary_reg1 lower register bit assignments.

Table 5-1087: por_rnsam_sys_cache_grp_secondary_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	region1_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region1_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region1_scndry_valid	Secondary memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.36 sys_cache_grp_secondary_reg2

Configures secondary hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE50

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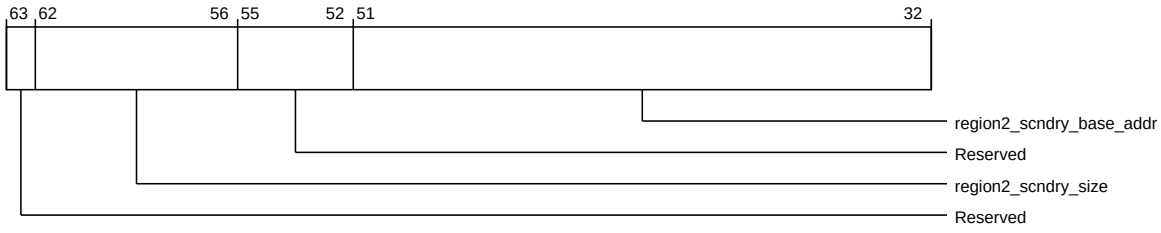
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1074: por_rnsam_sys_cache_grp_secondary_reg2 (high)



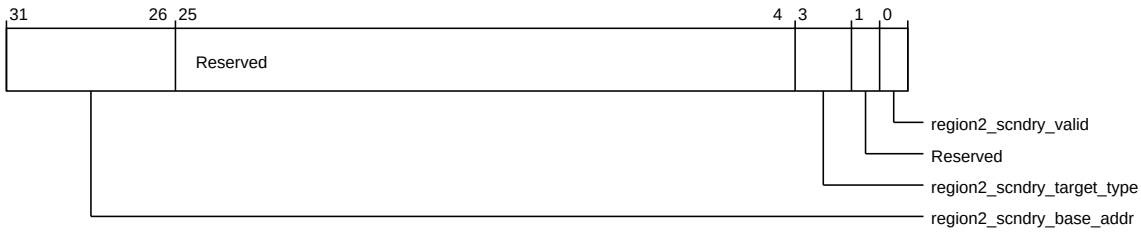
The following table shows the sys_cache_grp_secondary_reg2 higher register bit assignments.

Table 5-1088: por_rnsam_sys_cache_grp_secondary_reg2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region2_scndry_size	Secondary memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	region2_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1075: por_rnsam_sys_cache_grp_secondary_reg2 (low)



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The following table shows the sys_cache_grp_secondary_reg2 lower register bit assignments.

Table 5-1089: por_rnsam_sys_cache_grp_secondary_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	region2_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-
3:2	region2_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region2_scndry_valid	Secondary memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.37 sys_cache_grp_secondary_reg3

Configures secondary hashed memory regions

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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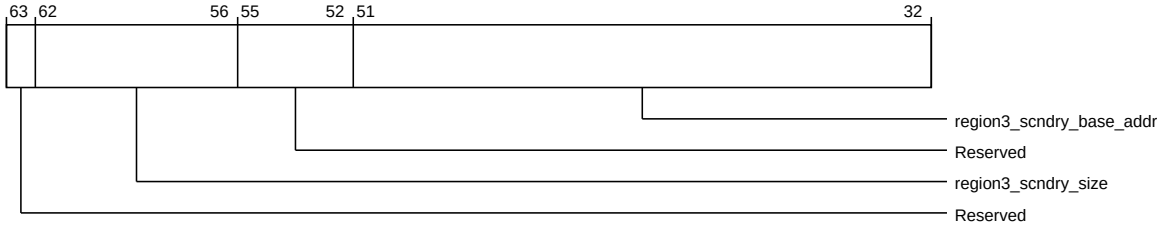
Figure 5-1076: por_rnsam_sys_cache_grp_secondary_reg3 (high)



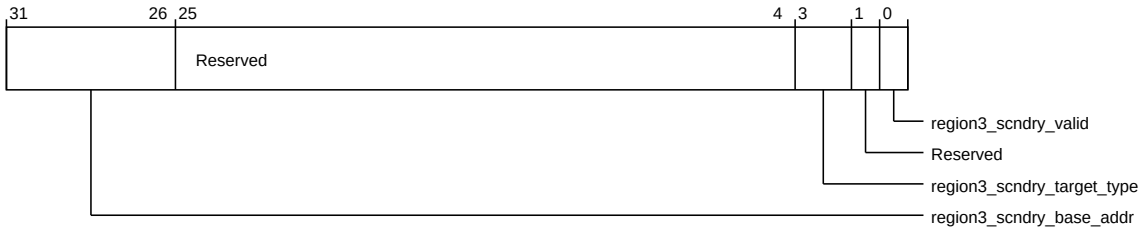
The following table shows the sys_cache_grp_secondary_reg3 higher register bit assignments.

Table 5-1090: por_rnsam_sys_cache_grp_secondary_reg3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	region3_scndry_size	Secondary memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	region3_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1077: por_rnsam_sys_cache_grp_secondary_reg3 (low)



The following table shows the sys_cache_grp_secondary_reg3 lower register bit assignments.

Table 5-1091: por_rnsam_sys_cache_grp_secondary_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	region3_scndry_base_addr	Bits [51:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	26'b00000000000000000000000000
25:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:2	region3_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region3_scndry_valid	Secondary memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.38 rnsam_hash_addr_mask_reg

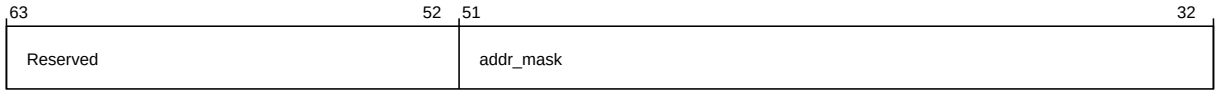
Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE80
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1078: por_rnsam_rnsam_hash_addr_mask_reg (high)



The following table shows the rnsam_hash_addr_mask_reg higher register bit assignments.

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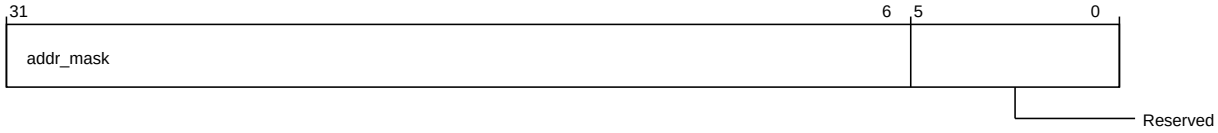
Table 5-1092: por_rnsam_rnsam_hash_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1079: por_rnsam_rnsam_hash_addr_mask_reg (low)



The following table shows the rnsam_hash_addr_mask_reg lower register bit assignments.

Table 5-1093: por_rnsam_rnsam_hash_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.39 rnsam_region_cmp_addr_mask_reg

Configures the address mask that is applied before region compare.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hE90
Register reset 64'b1111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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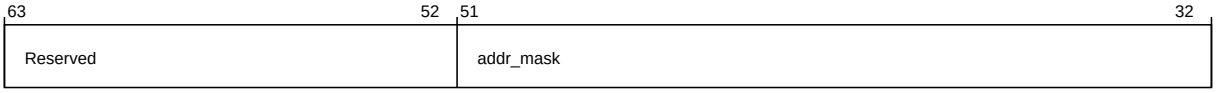
Figure 5-1080: por_rnsam_rnsam_region_cmp_addr_mask_reg (high)



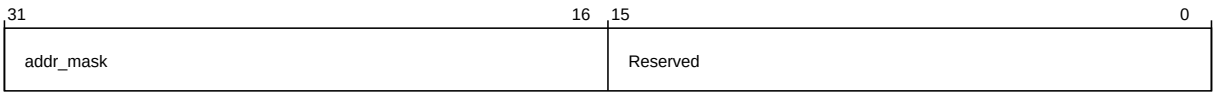
The following table shows the rnsam_region_cmp_addr_mask_reg higher register bit assignments.

Table 5-1094: por_rnsam_rnsam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask applied before memory region compare	RW	36'hFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1081: por_rnsam_rnsam_region_cmp_addr_mask_reg (low)



The following table shows the rnsam_region_cmp_addr_mask_reg lower register bit assignments.

Table 5-1095: por_rnsam_rnsam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:16	addr_mask	Address mask applied before memory region compare	RW	36'hFFFFFFFFF
15:0	Reserved	Reserved	RO	-

5.3.9.40 sys_cache_group_hn_count

Indicates number of HN-Fs in system cache groups 0 to 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEA0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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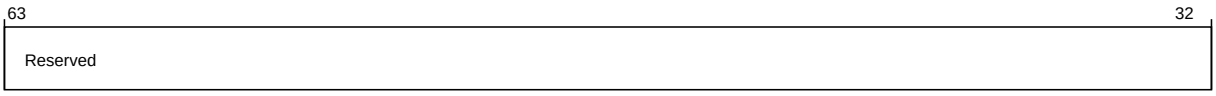
The following figure shows the higher register bit assignments.

Figure 5-1082: por_rnsam_sys_cache_group_hn_count (high)



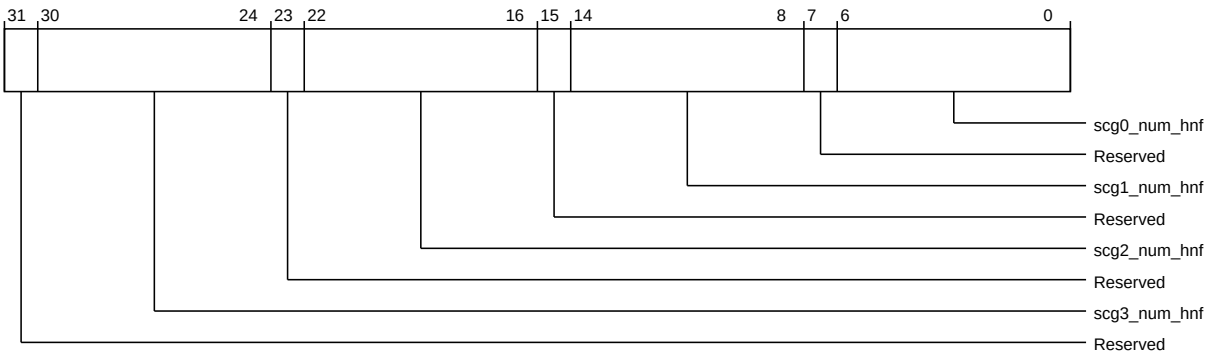
The following table shows the sys_cache_group_hn_count higher register bit assignments.

Table 5-1096: por_rnsam_sys_cache_group_hn_count (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1083: por_rnsam_sys_cache_group_hn_count (low)



The following table shows the sys_cache_group_hn_count lower register bit assignments.

Table 5-1097: por_rnsam_sys_cache_group_hn_count (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:24	scg3_num_hnf	HN-F count for system cache group 3	RW	7'b00000
23	Reserved	Reserved	RO	-
22:16	scg2_num_hnf	HN-F count for system cache group 2	RW	7'b00000
15	Reserved	Reserved	RO	-
14:8	scg1_num_hnf	HN-F count for system cache group 1	RW	7'b00000
7	Reserved	Reserved	RO	-
6:0	scg0_num_hnf	HN-F count for system cache group 0	RW	7'b00000

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5.3.9.41 sys_cache_grp_sn_attr

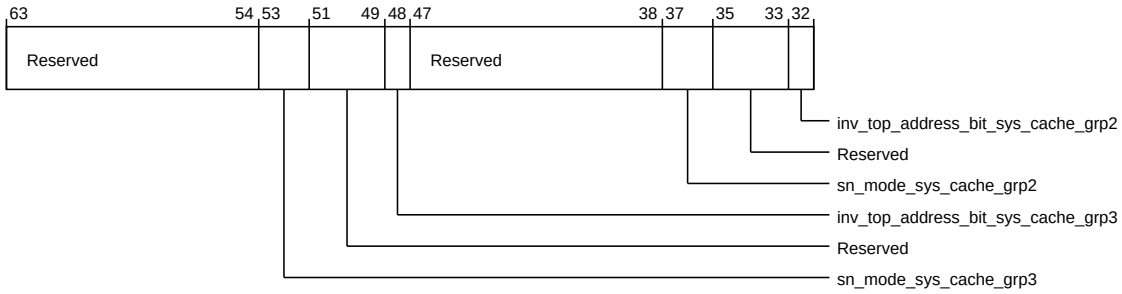
Configures attributes for SN node IDs for system cache groups.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEB0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1084: por_rnsam_sys_cache_grp_sn_attr (high)



The following table shows the sys_cache_grp_sn_attr higher register bit assignments.

Table 5-1098: por_rnsam_sys_cache_grp_sn_attr (high)

Bits	Field name	Description	Type	Reset
63:54	Reserved	Reserved	RO	-
53:52	sn_mode_sys_cache_grp3	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
51:49	Reserved	Reserved	RO	-
48	inv_top_address_bit_sys_cache_grp3	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
47:38	Reserved	Reserved	RO	-

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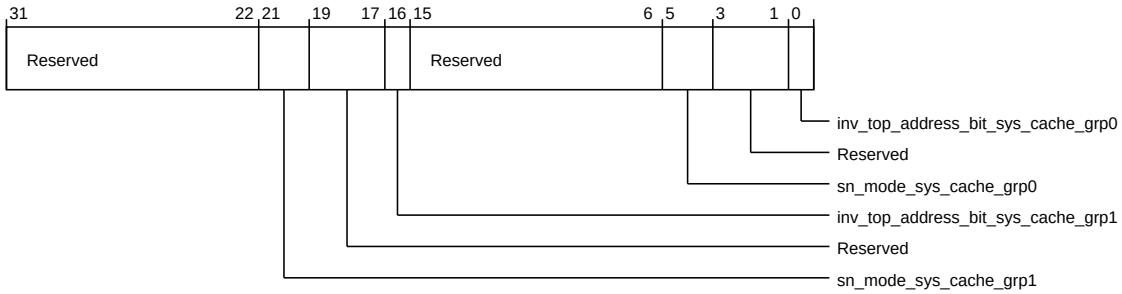
Bits	Field name	Description	Type	Reset
37:36	sn_mode_sys_cache_grp2	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b00
35:33	Reserved	Reserved	RO	-
32	inv_top_address_bit_sys_cache_grp2	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

The following figure shows the lower register bit assignments.

Figure 5-1085: por_rnsam_sys_cache_grp_sn_attr (low)



The following table shows the sys_cache_grp_sn_attr lower register bit assignments.

Table 5-1099: por_rnsam_sys_cache_grp_sn_attr (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:20	sn_mode_sys_cache_grp1	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
19:17	Reserved	Reserved	RO	-
16	inv_top_address_bit_sys_cache_grp1	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

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Bits	Field name	Description	Type	Reset
15:6	Reserved	Reserved	RO	-
5:4	sn_mode_sys_cache_grp0	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
3:1	Reserved	Reserved	RO	-
0	inv_top_address_bit_sys_cache_grp0	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

5.3.9.42 sys_cache_grp_nonhash_nodeid

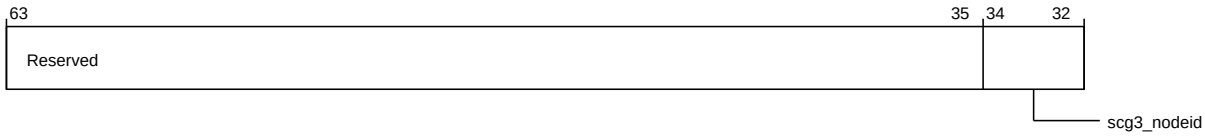
Configures non-hashed node IDs for system cache groups 1 to 3. NOTE: Only applicable in the non-hashed mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hEC0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1086: por_rnsam_sys_cache_grp_nonhash_nodeid (high)



The following table shows the sys_cache_grp_nonhash_nodeid higher register bit assignments.

Table 5-1100: por_rnsam_sys_cache_grp_nonhash_nodeid (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b00000000000

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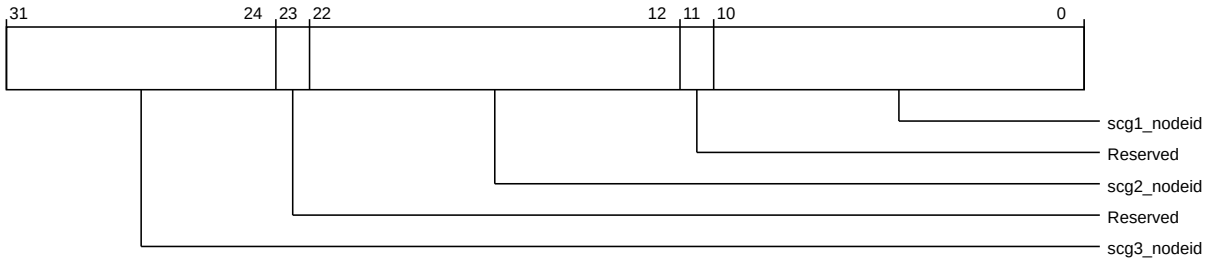
The following figure shows the lower register bit assignments.

Figure 5-1087: por_rnsam_sys_cache_grp_nonhash_nodeid (low)



The following table shows the sys_cache_grp_nonhash_nodeid lower register bit assignments.

Table 5-1101: por_rnsam_sys_cache_grp_nonhash_nodeid (low)

Bits	Field name	Description	Type	Reset
31:24	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	scg2_nodeid	Non-hashed node ID for system cache group 2	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	scg1_nodeid	Non-hashed node ID for system cache group 1	RW	11'b00000000000

5.3.9.43 sys_cache_grp_hn_nodeid_reg0

Configures hashed node IDs for system cache groups. Controls target HN node IDs 0 to 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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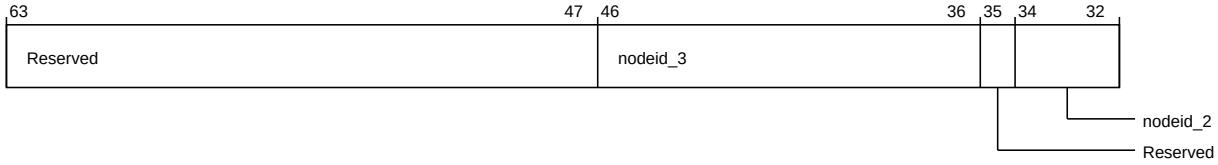
Figure 5-1088: por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)



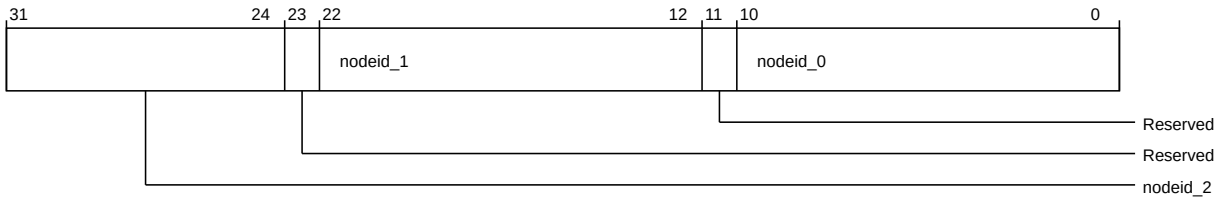
The following table shows the sys_cache_grp_hn_nodeid_reg0 higher register bit assignments.

Table 5-1102: por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_3	Hashed target node ID 3	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_2	Hashed target node ID 2	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1089: por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg0 lower register bit assignments.

Table 5-1103: por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_2	Hashed target node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_1	Hashed target node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_0	Hashed target node ID 0	RW	11'b00000000000

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5.3.9.44 sys_cache_grp_hn_nodeid_reg1

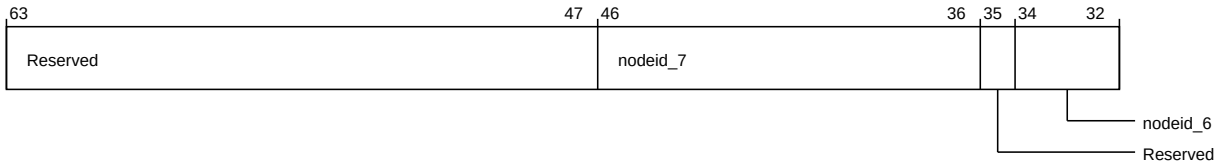
Configures hashed node IDs for system cache groups. Controls target HN node IDs 4 to 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF08
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1090: por_rnsam_sys_cache_grp_hn_nodeid_reg1 (high)



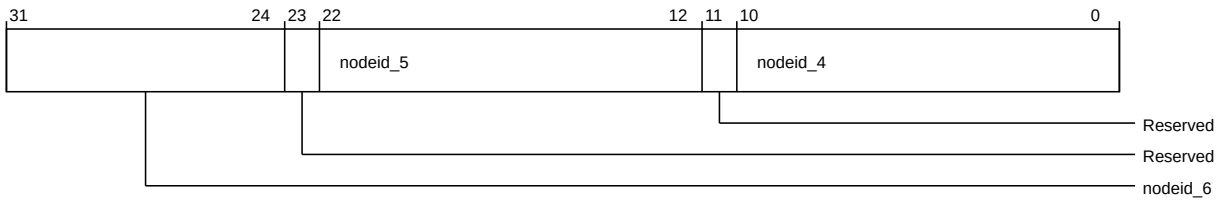
The following table shows the sys_cache_grp_hn_nodeid_reg1 higher register bit assignments.

Table 5-1104: por_rnsam_sys_cache_grp_hn_nodeid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_7	Hashed target node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_6	Hashed target node ID 6	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1091: por_rnsam_sys_cache_grp_hn_nodeid_reg1 (low)



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The following table shows the sys_cache_grp_hn_nodeid_reg1 lower register bit assignments.

Table 5-1105: por_rnsam_sys_cache_grp_hn_nodeid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_6	Hashed target node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_5	Hashed target node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_4	Hashed target node ID 4	RW	11'b00000000000

5.3.9.45 sys_cache_grp_hn_nodeid_reg2

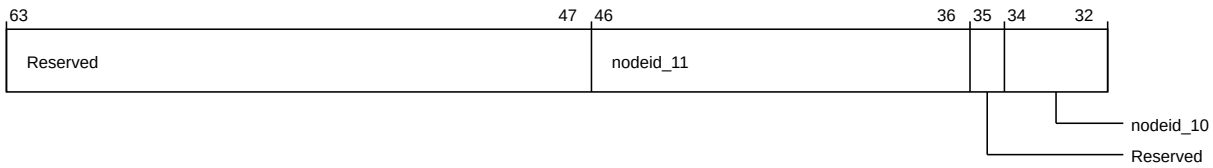
Configures hashed node IDs for system cache groups. Controls target HN node IDs 8 to 11.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF10
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1092: por_rnsam_sys_cache_grp_hn_nodeid_reg2 (high)



The following table shows the sys_cache_grp_hn_nodeid_reg2 higher register bit assignments.

Table 5-1106: por_rnsam_sys_cache_grp_hn_nodeid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_11	Hashed target node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_10	Hashed target node ID 10	RW	11'b00000000000

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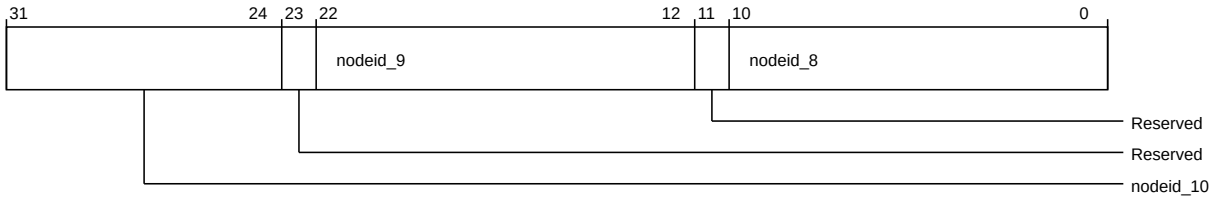
The following figure shows the lower register bit assignments.

Figure 5-1093: por_rnsam_sys_cache_grp_hn_nodeid_reg2 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg2 lower register bit assignments.

Table 5-1107: por_rnsam_sys_cache_grp_hn_nodeid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_10	Hashed target node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_9	Hashed target node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Hashed target node ID 8	RW	11'b00000000000

5.3.9.46 sys_cache_grp_hn_nodeid_reg3

Configures hashed node IDs for system cache groups. Controls target HN node IDs 12 to 15.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF18
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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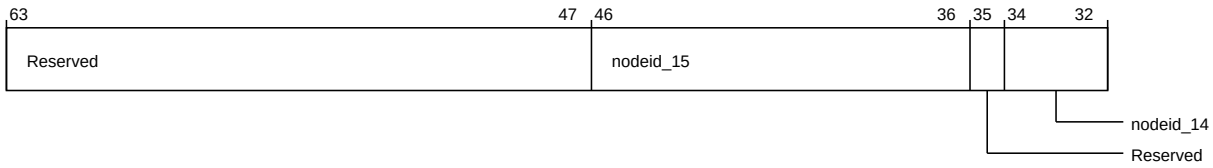
Figure 5-1094: por_rnsam_sys_cache_grp_hn_nodeid_reg3 (high)



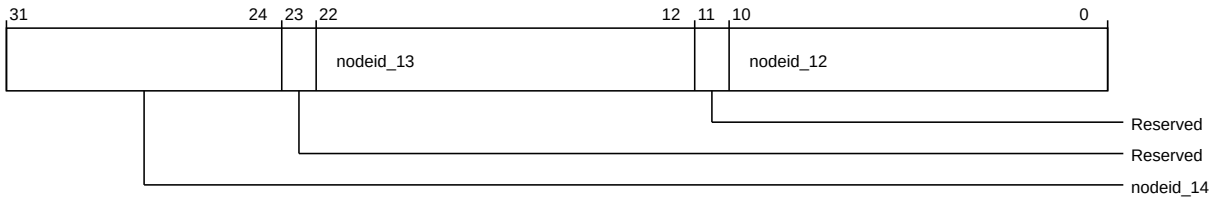
The following table shows the sys_cache_grp_hn_nodeid_reg3 higher register bit assignments.

Table 5-1108: por_rnsam_sys_cache_grp_hn_nodeid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_15	Hashed target node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_14	Hashed target node ID 14	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1095: por_rnsam_sys_cache_grp_hn_nodeid_reg3 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg3 lower register bit assignments.

Table 5-1109: por_rnsam_sys_cache_grp_hn_nodeid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_14	Hashed target node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_13	Hashed target node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_12	Hashed target node ID 12	RW	11'b00000000000

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5.3.9.47 sys_cache_grp_hn_nodeid_reg4

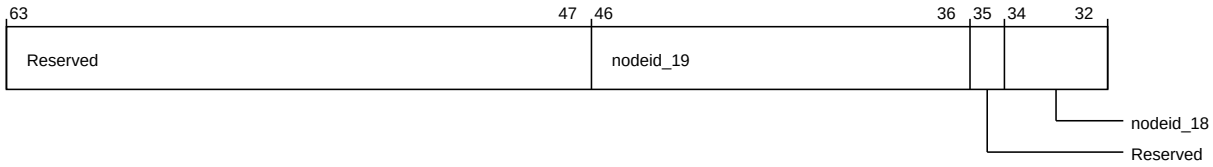
Configures hashed node IDs for system cache groups. Controls target HN node IDs 16 to 19.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF20
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1096: por_rnsam_sys_cache_grp_hn_nodeid_reg4 (high)



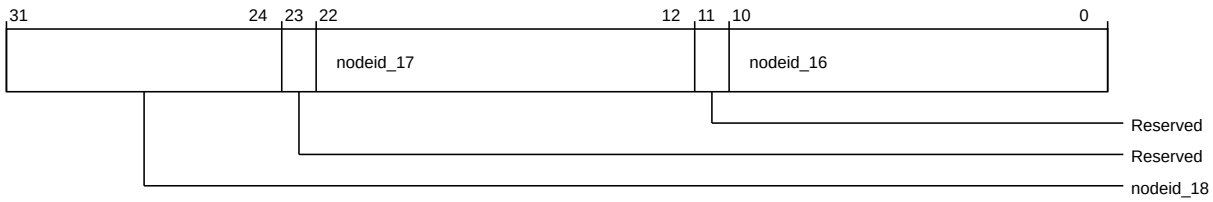
The following table shows the sys_cache_grp_hn_nodeid_reg4 higher register bit assignments.

Table 5-1110: por_rnsam_sys_cache_grp_hn_nodeid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_19	Hashed target node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_18	Hashed target node ID 18	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1097: por_rnsam_sys_cache_grp_hn_nodeid_reg4 (low)



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The following table shows the sys_cache_grp_hn_nodeid_reg4 lower register bit assignments.

Table 5-1111: por_rnsam_sys_cache_grp_hn_nodeid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_18	Hashed target node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_17	Hashed target node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_16	Hashed target node ID 16	RW	11'b00000000000

5.3.9.48 sys_cache_grp_hn_nodeid_reg5

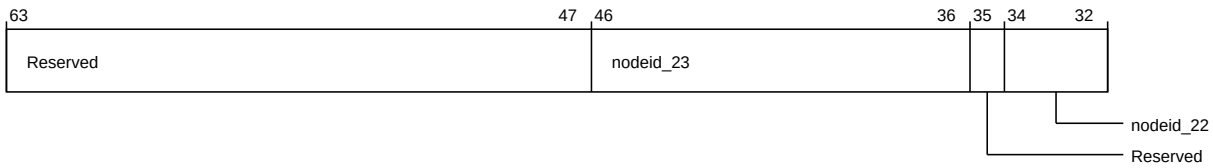
Configures hashed node IDs for system cache groups. Controls target HN node IDs 20 to 23.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF28
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1098: por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)



The following table shows the sys_cache_grp_hn_nodeid_reg5 higher register bit assignments.

Table 5-1112: por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_23	Hashed target node ID 23	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_22	Hashed target node ID 22	RW	11'b00000000000

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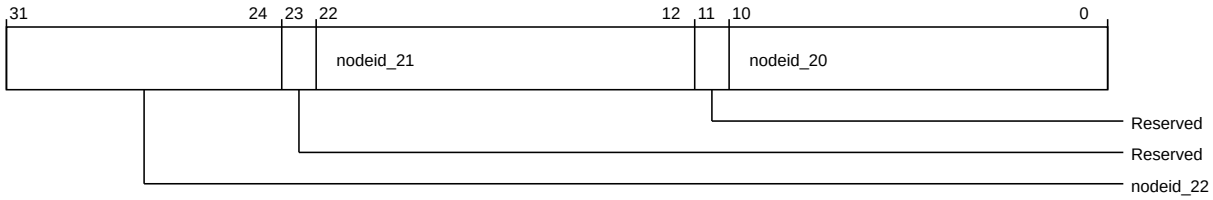
The following figure shows the lower register bit assignments.

Figure 5-1099: por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg5 lower register bit assignments.

Table 5-1113: por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_22	Hashed target node ID 22	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_21	Hashed target node ID 21	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_20	Hashed target node ID 20	RW	11'b00000000000

5.3.9.49 sys_cache_grp_hn_nodeid_reg6

Configures hashed node IDs for system cache groups. Controls target HN node IDs 24 to 27.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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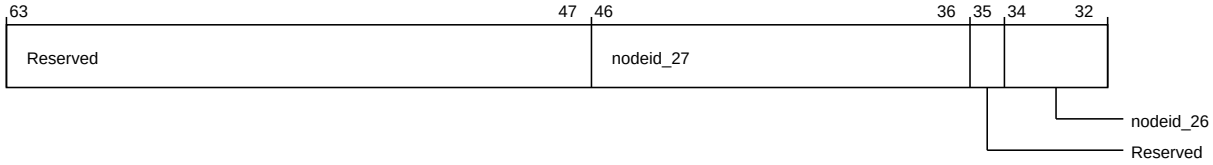
Figure 5-1100: por_rnsam_sys_cache_grp_hn_nodeid_reg6 (high)



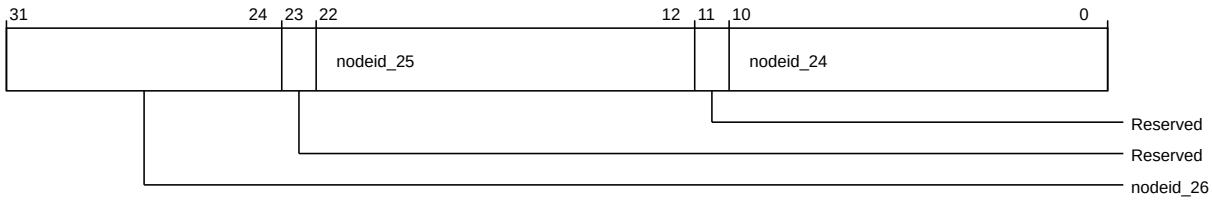
The following table shows the sys_cache_grp_hn_nodeid_reg6 higher register bit assignments.

Table 5-1114: por_rnsam_sys_cache_grp_hn_nodeid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_27	Hashed target node ID 27	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_26	Hashed target node ID 26	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1101: por_rnsam_sys_cache_grp_hn_nodeid_reg6 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg6 lower register bit assignments.

Table 5-1115: por_rnsam_sys_cache_grp_hn_nodeid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_26	Hashed target node ID 26	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_25	Hashed target node ID 25	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_24	Hashed target node ID 24	RW	11'b00000000000

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5.3.9.50 sys_cache_grp_hn_nodeid_reg7

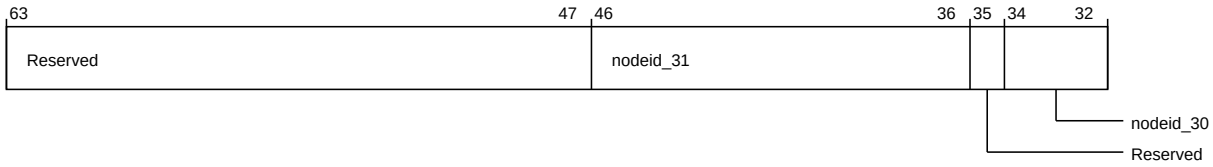
Configures hashed node IDs for system cache groups. Controls target HN node IDs 28 to 31.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF38
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1102: por_rnsam_sys_cache_grp_hn_nodeid_reg7 (high)



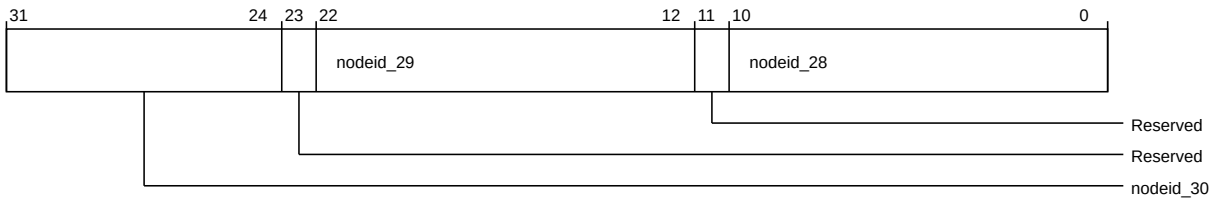
The following table shows the sys_cache_grp_hn_nodeid_reg7 higher register bit assignments.

Table 5-1116: por_rnsam_sys_cache_grp_hn_nodeid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_31	Hashed target node ID 31	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_30	Hashed target node ID 30	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1103: por_rnsam_sys_cache_grp_hn_nodeid_reg7 (low)



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The following table shows the sys_cache_grp_hn_nodeid_reg7 lower register bit assignments.

Table 5-1117: por_rnsam_sys_cache_grp_hn_nodeid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_30	Hashed target node ID 30	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_29	Hashed target node ID 29	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_28	Hashed target node ID 28	RW	11'b00000000000

5.3.9.51 sys_cache_grp_hn_nodeid_reg8

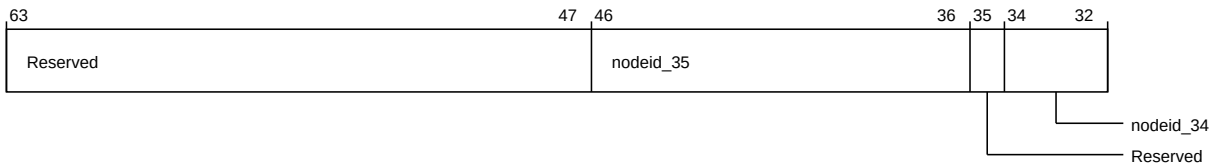
Configures hashed node IDs for system cache groups. Controls target HN node IDs 32 to 35.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1104: por_rnsam_sys_cache_grp_hn_nodeid_reg8 (high)



The following table shows the sys_cache_grp_hn_nodeid_reg8 higher register bit assignments.

Table 5-1118: por_rnsam_sys_cache_grp_hn_nodeid_reg8 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_35	Hashed target node ID 35	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_34	Hashed target node ID 34	RW	11'b00000000000

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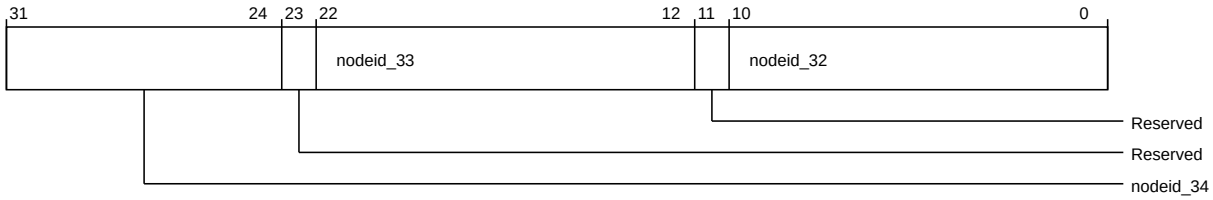
The following figure shows the lower register bit assignments.

Figure 5-1105: por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg8 lower register bit assignments.

Table 5-1119: por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_34	Hashed target node ID 34	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_33	Hashed target node ID 33	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_32	Hashed target node ID 32	RW	11'b00000000000

5.3.9.52 sys_cache_grp_hn_nodeid_reg9

Configures hashed node IDs for system cache groups. Controls target HN node IDs 36 to 39.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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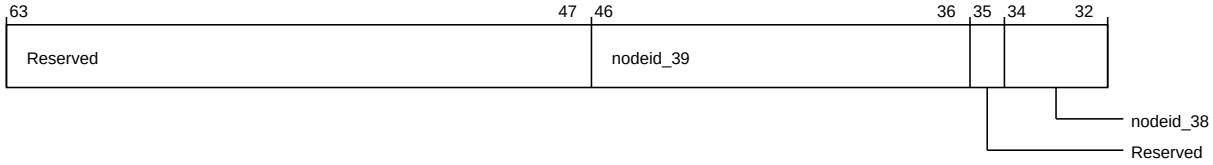
Figure 5-1106: por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)



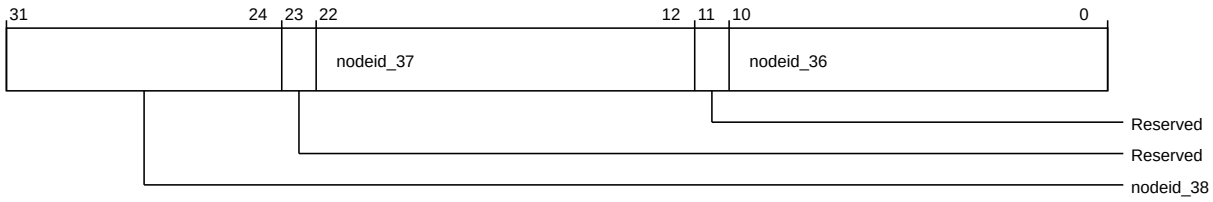
The following table shows the sys_cache_grp_hn_nodeid_reg9 higher register bit assignments.

Table 5-1120: por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_39	Hashed target node ID 39	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_38	Hashed target node ID 38	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1107: por_rnsam_sys_cache_grp_hn_nodeid_reg9 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg9 lower register bit assignments.

Table 5-1121: por_rnsam_sys_cache_grp_hn_nodeid_reg9 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_38	Hashed target node ID 38	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_37	Hashed target node ID 37	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_36	Hashed target node ID 36	RW	11'b00000000000

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5.3.9.53 sys_cache_grp_hn_nodeid_reg10

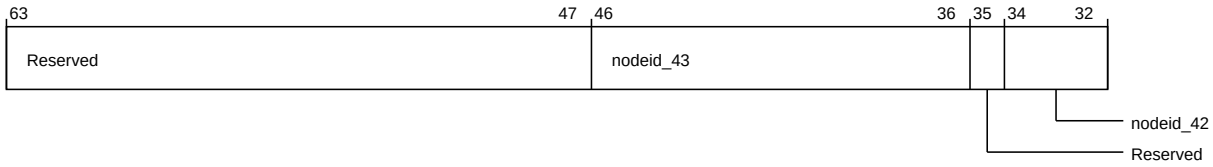
Configures hashed node IDs for system cache groups. Controls target HN node IDs 40 to 43.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1108: por_rnsam_sys_cache_grp_hn_nodeid_reg10 (high)



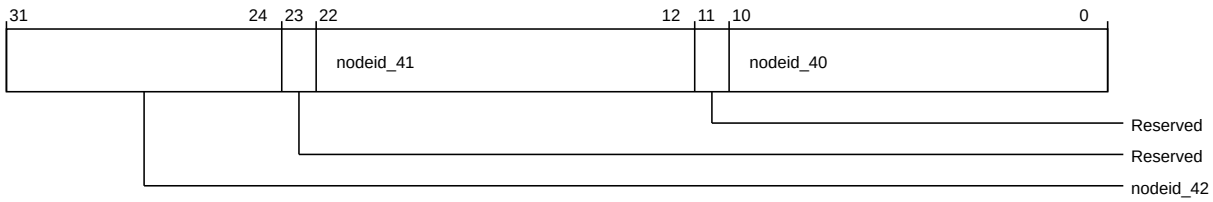
The following table shows the sys_cache_grp_hn_nodeid_reg10 higher register bit assignments.

Table 5-1122: por_rnsam_sys_cache_grp_hn_nodeid_reg10 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_43	Hashed target node ID 43	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_42	Hashed target node ID 42	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1109: por_rnsam_sys_cache_grp_hn_nodeid_reg10 (low)



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The following table shows the sys_cache_grp_hn_nodeid_reg10 lower register bit assignments.

Table 5-1123: por_rnsam_sys_cache_grp_hn_nodeid_reg10 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_42	Hashed target node ID 42	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_41	Hashed target node ID 41	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_40	Hashed target node ID 40	RW	11'b00000000000

5.3.9.54 sys_cache_grp_hn_nodeid_reg11

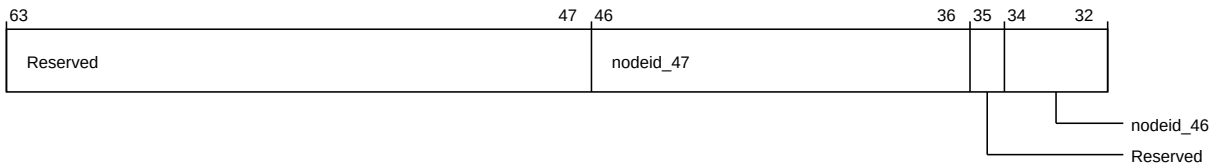
Configures hashed node IDs for system cache groups. Controls target HN node IDs 44 to 47.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1110: por_rnsam_sys_cache_grp_hn_nodeid_reg11 (high)



The following table shows the sys_cache_grp_hn_nodeid_reg11 higher register bit assignments.

Table 5-1124: por_rnsam_sys_cache_grp_hn_nodeid_reg11 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_47	Hashed target node ID 47	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_46	Hashed target node ID 46	RW	11'b00000000000

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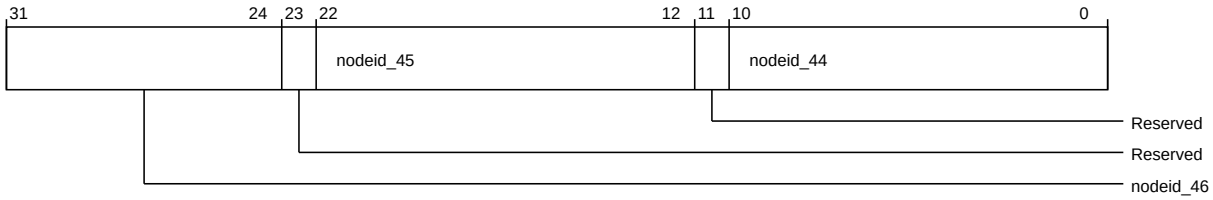
The following figure shows the lower register bit assignments.

Figure 5-1111: por_rnsam_sys_cache_grp_hn_nodeid_reg11 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg11 lower register bit assignments.

Table 5-1125: por_rnsam_sys_cache_grp_hn_nodeid_reg11 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_46	Hashed target node ID 46	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_45	Hashed target node ID 45	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_44	Hashed target node ID 44	RW	11'b00000000000

5.3.9.55 sys_cache_grp_hn_nodeid_reg12

Configures hashed node IDs for system cache groups. Controls target HN node IDs 48 to 51.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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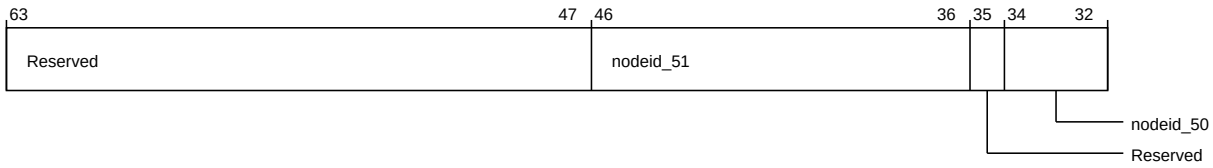
Figure 5-1112: por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)



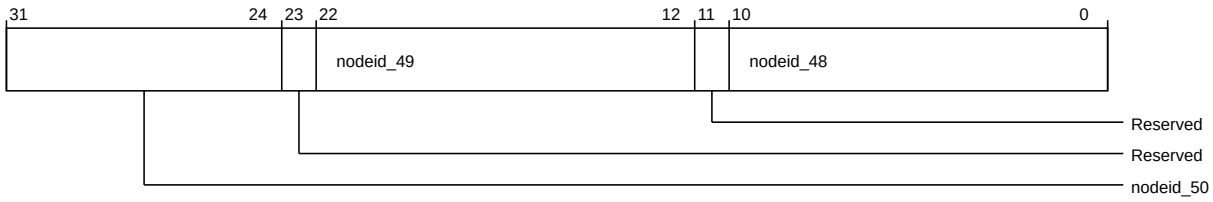
The following table shows the sys_cache_grp_hn_nodeid_reg12 higher register bit assignments.

Table 5-1126: por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_51	Hashed target node ID 51	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_50	Hashed target node ID 50	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1113: por_rnsam_sys_cache_grp_hn_nodeid_reg12 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg12 lower register bit assignments.

Table 5-1127: por_rnsam_sys_cache_grp_hn_nodeid_reg12 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_50	Hashed target node ID 50	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_49	Hashed target node ID 49	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_48	Hashed target node ID 48	RW	11'b00000000000

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5.3.9.56 sys_cache_grp_hn_nodeid_reg13

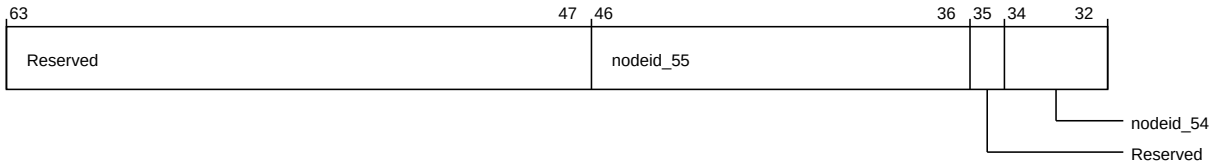
Configures hashed node IDs for system cache groups. Controls target HN node IDs 52 to 55.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF68
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1114: por_rnsam_sys_cache_grp_hn_nodeid_reg13 (high)



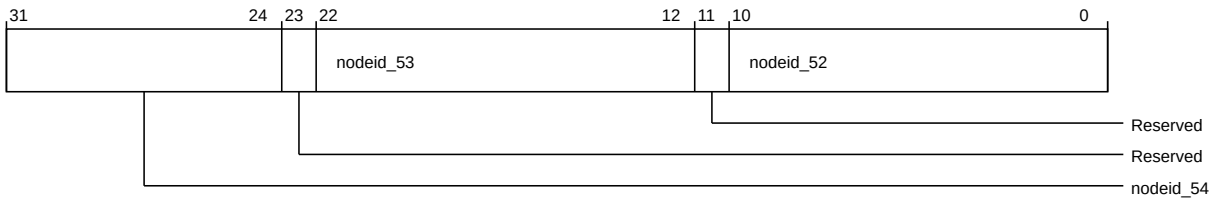
The following table shows the sys_cache_grp_hn_nodeid_reg13 higher register bit assignments.

Table 5-1128: por_rnsam_sys_cache_grp_hn_nodeid_reg13 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_55	Hashed target node ID 55	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_54	Hashed target node ID 54	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1115: por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)



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The following table shows the sys_cache_grp_hn_nodeid_reg13 lower register bit assignments.

Table 5-1129: por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_54	Hashed target node ID 54	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_53	Hashed target node ID 53	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_52	Hashed target node ID 52	RW	11'b00000000000

5.3.9.57 sys_cache_grp_hn_nodeid_reg14

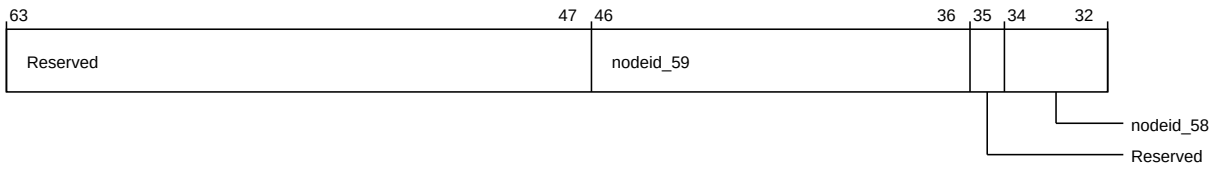
Configures hashed node IDs for system cache groups. Controls target HN node IDs 56 to 59.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF70
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1116: por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)



The following table shows the sys_cache_grp_hn_nodeid_reg14 higher register bit assignments.

Table 5-1130: por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_59	Hashed target node ID 59	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_58	Hashed target node ID 58	RW	11'b00000000000

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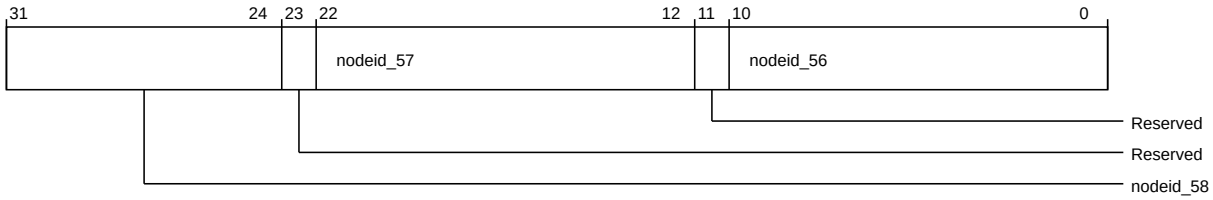
The following figure shows the lower register bit assignments.

Figure 5-1117: por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg14 lower register bit assignments.

Table 5-1131: por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_58	Hashed target node ID 58	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_57	Hashed target node ID 57	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_56	Hashed target node ID 56	RW	11'b00000000000

5.3.9.58 sys_cache_grp_hn_nodeid_reg15

Configures hashed node IDs for system cache groups. Controls target HN node IDs 60 to 63.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hF78
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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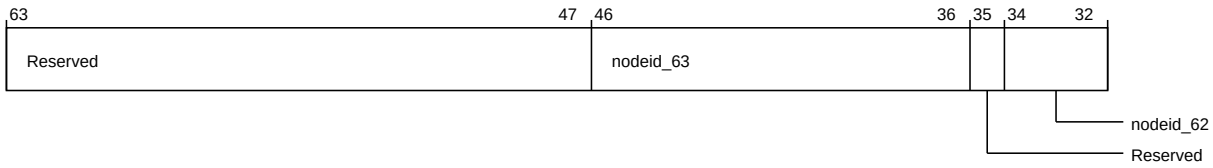
Figure 5-1118: por_rnsam_sys_cache_grp_hn_nodeid_reg15 (high)



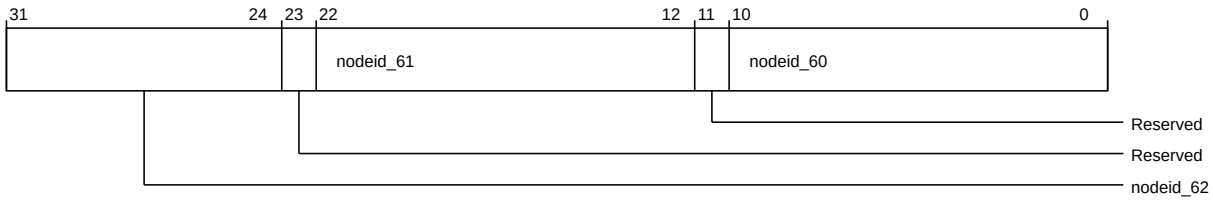
The following table shows the sys_cache_grp_hn_nodeid_reg15 higher register bit assignments.

Table 5-1132: por_rnsam_sys_cache_grp_hn_nodeid_reg15 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_63	Hashed target node ID 63	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_62	Hashed target node ID 62	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1119: por_rnsam_sys_cache_grp_hn_nodeid_reg15 (low)



The following table shows the sys_cache_grp_hn_nodeid_reg15 lower register bit assignments.

Table 5-1133: por_rnsam_sys_cache_grp_hn_nodeid_reg15 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_62	Hashed target node ID 62	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_61	Hashed target node ID 61	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_60	Hashed target node ID 60	RW	11'b00000000000

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5.3.9.59 sys_cache_grp_sn_nodeid_reg0

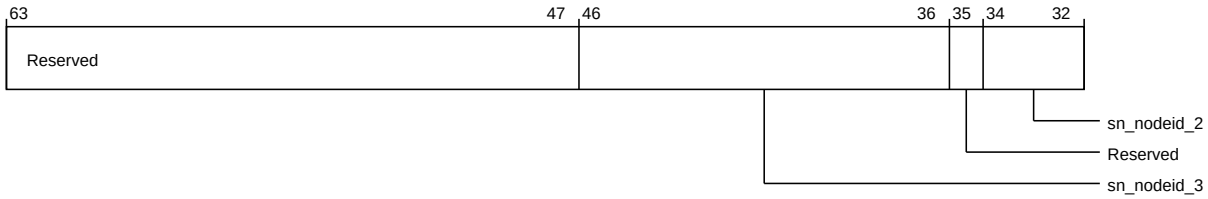
Configures hashed node IDs for system cache groups. Controls target SN node IDs 0 to 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1000
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1120: por_rnsam_sys_cache_grp_sn_nodeid_reg0 (high)



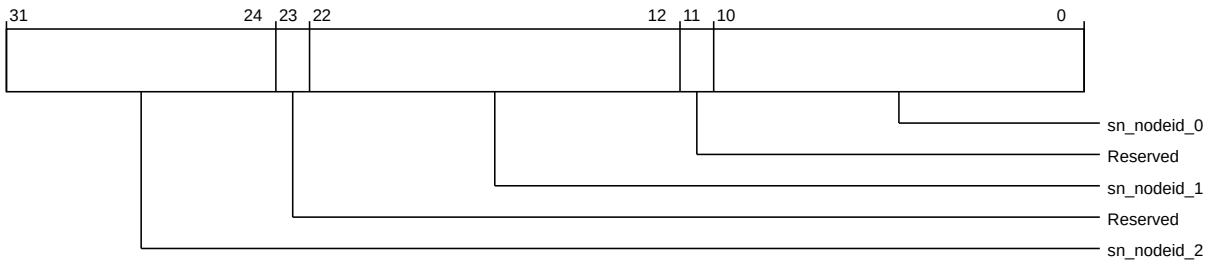
The following table shows the sys_cache_grp_sn_nodeid_reg0 higher register bit assignments.

Table 5-1134: por_rnsam_sys_cache_grp_sn_nodeid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_3	Hashed target SN node ID 3	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_2	Hashed target SN node ID 2	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1121: por_rnsam_sys_cache_grp_sn_nodeid_reg0 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg0 lower register bit assignments.

Table 5-1135: por_rnsam_sys_cache_grp_sn_nodeid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_2	Hashed target SN node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_1	Hashed target SN node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_0	Hashed target SN node ID 0	RW	11'b00000000000

5.3.9.60 sys_cache_grp_sn_nodeid_reg1

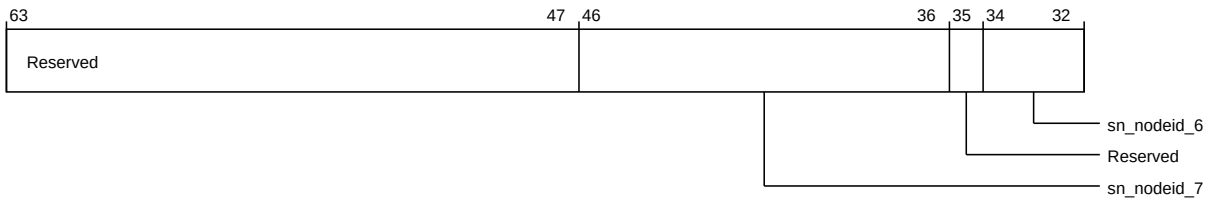
Configures hashed node IDs for system cache groups. Controls target SN node IDs 4 to 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1122: por_rnsam_sys_cache_grp_sn_nodeid_reg1 (high)



The following table shows the sys_cache_grp_sn_nodeid_reg1 higher register bit assignments.

Table 5-1136: por_rnsam_sys_cache_grp_sn_nodeid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_7	Hashed target SN node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_6	Hashed target SN node ID 6	RW	11'b00000000000

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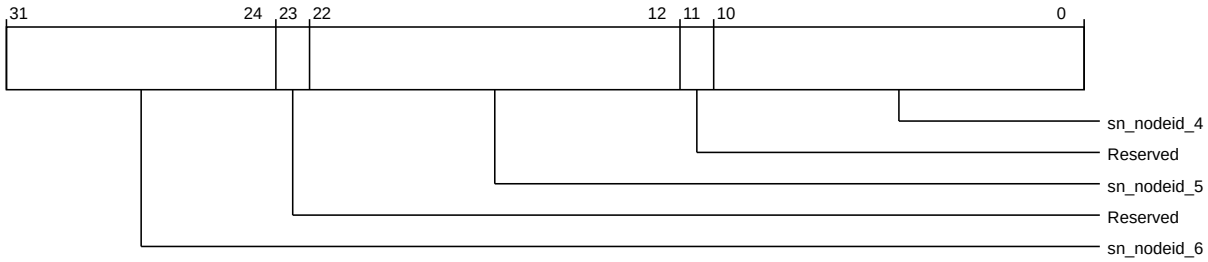
The following figure shows the lower register bit assignments.

Figure 5-1123: por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg1 lower register bit assignments.

Table 5-1137: por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_6	Hashed target SN node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_5	Hashed target SN node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_4	Hashed target SN node ID 4	RW	11'b00000000000

5.3.9.61 sys_cache_grp_sn_nodeid_reg2

Configures hashed node IDs for system cache groups. Controls target SN node IDs 8 to 11.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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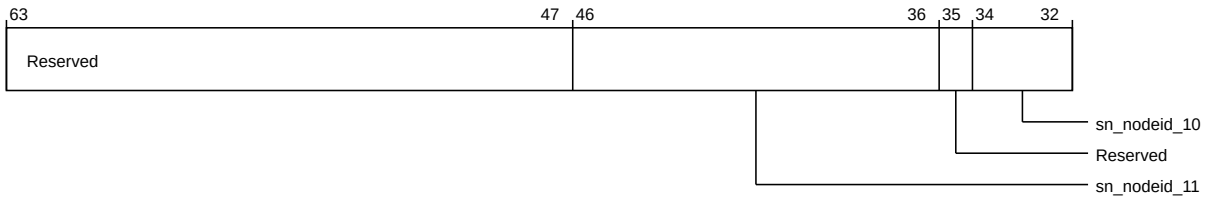
Figure 5-1124: por_rnsam_sys_cache_grp_sn_nodeid_reg2 (high)



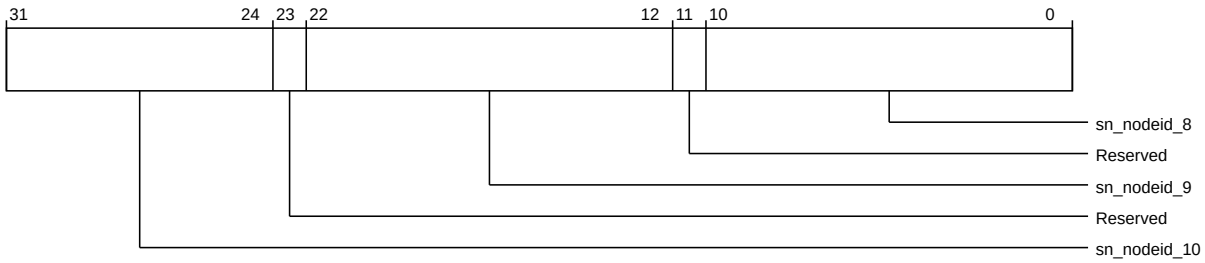
The following table shows the sys_cache_grp_sn_nodeid_reg2 higher register bit assignments.

Table 5-1138: por_rnsam_sys_cache_grp_sn_nodeid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_11	Hashed target SN node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_10	Hashed target SN node ID 10	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1125: por_rnsam_sys_cache_grp_sn_nodeid_reg2 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg2 lower register bit assignments.

Table 5-1139: por_rnsam_sys_cache_grp_sn_nodeid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_10	Hashed target SN node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_9	Hashed target SN node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_8	Hashed target SN node ID 8	RW	11'b00000000000

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5.3.9.62 sys_cache_grp_sn_nodeid_reg3

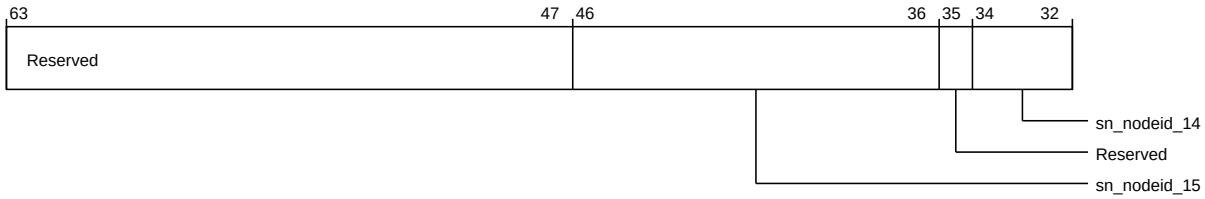
Configures hashed node IDs for system cache groups. Controls target SN node IDs 12 to 15.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1126: por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)



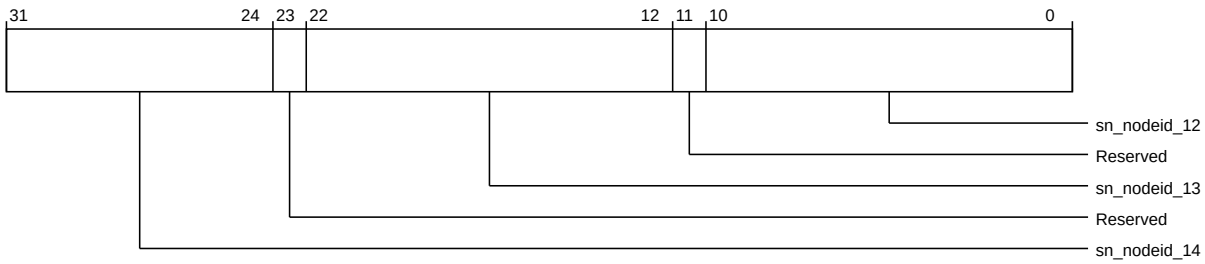
The following table shows the sys_cache_grp_sn_nodeid_reg3 higher register bit assignments.

Table 5-1140: por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_15	Hashed target SN node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1127: por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg3 lower register bit assignments.

Table 5-1141: por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_13	Hashed target SN node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_12	Hashed target SN node ID 12	RW	11'b00000000000

5.3.9.63 sys_cache_grp_sn_nodeid_reg4

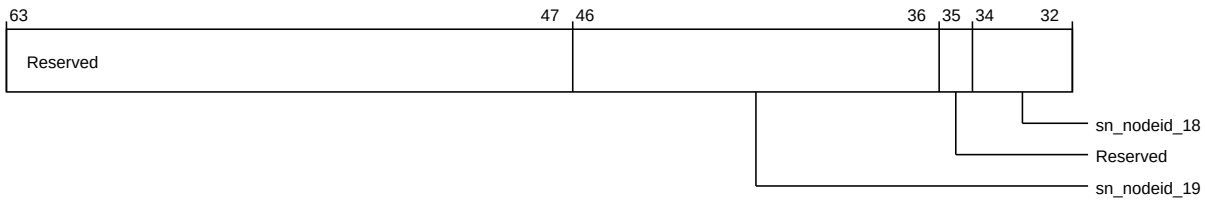
Configures hashed node IDs for system cache groups. Controls target SN node IDs 16 to 19.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1128: por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)



The following table shows the sys_cache_grp_sn_nodeid_reg4 higher register bit assignments.

Table 5-1142: por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_19	Hashed target SN node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_18	Hashed target SN node ID 18	RW	11'b00000000000

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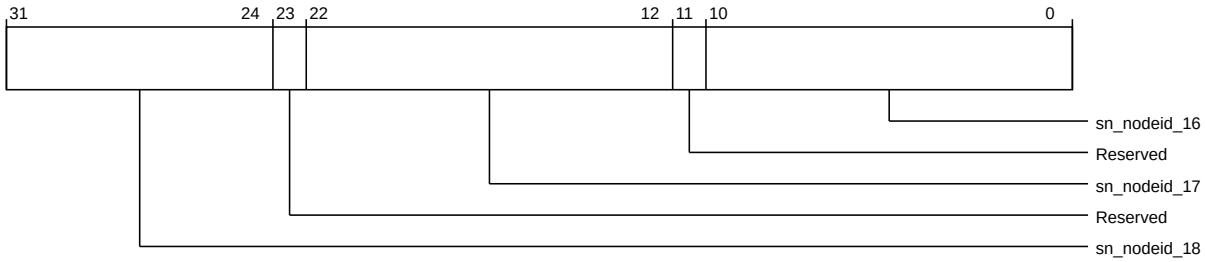
The following figure shows the lower register bit assignments.

Figure 5-1129: por_rnsam_sys_cache_grp_sn_nodeid_reg4 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg4 lower register bit assignments.

Table 5-1143: por_rnsam_sys_cache_grp_sn_nodeid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_18	Hashed target SN node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_17	Hashed target SN node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_16	Hashed target SN node ID 16	RW	11'b00000000000

5.3.9.64 sys_cache_grp_sn_nodeid_reg5

Configures hashed node IDs for system cache groups. Controls target SN node IDs 20 to 23.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1028
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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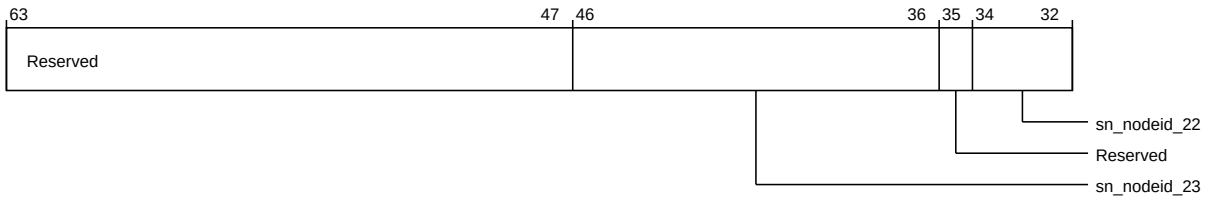
Figure 5-1130: por_rnsam_sys_cache_grp_sn_nodeid_reg5 (high)



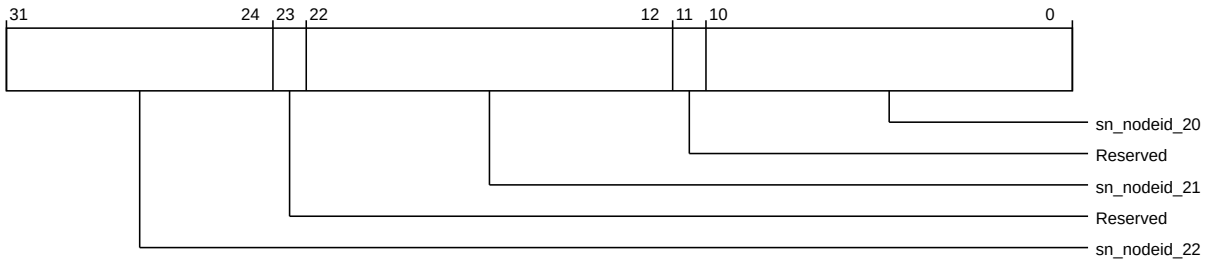
The following table shows the sys_cache_grp_sn_nodeid_reg5 higher register bit assignments.

Table 5-1144: por_rnsam_sys_cache_grp_sn_nodeid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_23	Hashed target SN node ID 23	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_22	Hashed target SN node ID 22	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1131: por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg5 lower register bit assignments.

Table 5-1145: por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_22	Hashed target SN node ID 22	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_21	Hashed target SN node ID 21	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_20	Hashed target SN node ID 20	RW	11'b00000000000

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5.3.9.65 sys_cache_grp_sn_nodeid_reg6

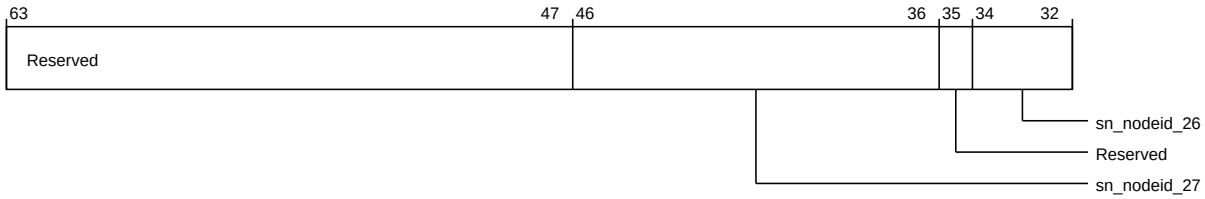
Configures hashed node IDs for system cache groups. Controls target SN node IDs 24 to 27.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1030
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1132: por_rnsam_sys_cache_grp_sn_nodeid_reg6 (high)



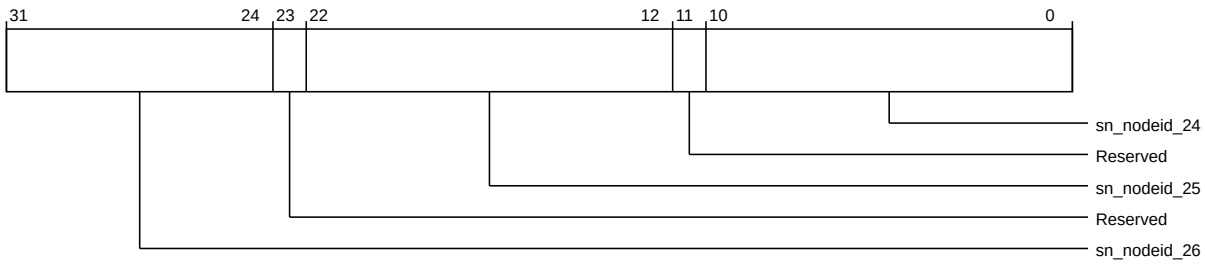
The following table shows the sys_cache_grp_sn_nodeid_reg6 higher register bit assignments.

Table 5-1146: por_rnsam_sys_cache_grp_sn_nodeid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_27	Hashed target SN node ID 27	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_26	Hashed target SN node ID 26	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1133: por_rnsam_sys_cache_grp_sn_nodeid_reg6 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg6 lower register bit assignments.

Table 5-1147: por_rnsam_sys_cache_grp_sn_nodeid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_26	Hashed target SN node ID 26	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_25	Hashed target SN node ID 25	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_24	Hashed target SN node ID 24	RW	11'b00000000000

5.3.9.66 sys_cache_grp_sn_nodeid_reg7

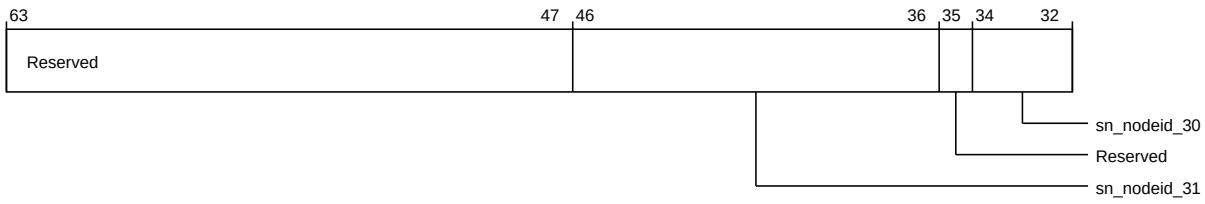
Configures hashed node IDs for system cache groups. Controls target SN node IDs 28 to 31.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1038
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1134: por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)



The following table shows the sys_cache_grp_sn_nodeid_reg7 higher register bit assignments.

Table 5-1148: por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_31	Hashed target SN node ID 31	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b00000000000

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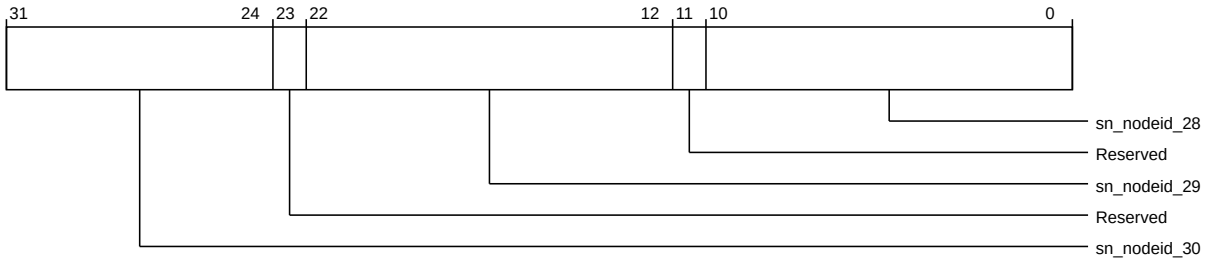
The following figure shows the lower register bit assignments.

Figure 5-1135: por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg7 lower register bit assignments.

Table 5-1149: por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_29	Hashed target SN node ID 29	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_28	Hashed target SN node ID 28	RW	11'b00000000000

5.3.9.67 sys_cache_grp_sn_nodeid_reg8

Configures hashed node IDs for system cache groups. Controls target SN node IDs 32 to 35.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1040
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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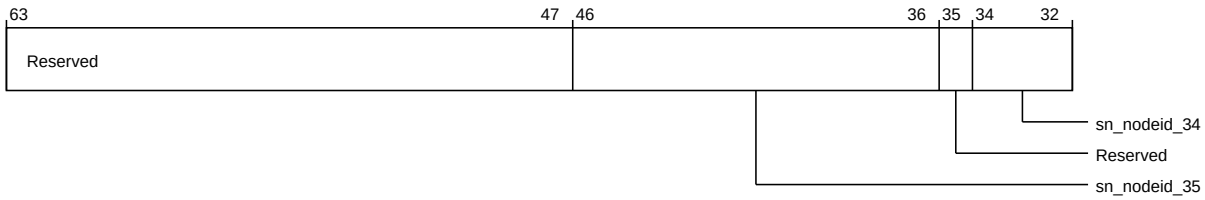
Figure 5-1136: por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)



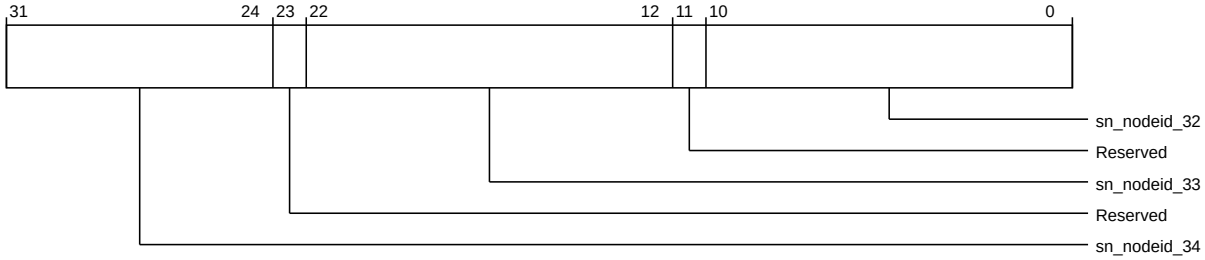
The following table shows the sys_cache_grp_sn_nodeid_reg8 higher register bit assignments.

Table 5-1150: por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_35	Hashed target SN node ID 35	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1137: por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg8 lower register bit assignments.

Table 5-1151: por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_33	Hashed target SN node ID 33	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_32	Hashed target SN node ID 32	RW	11'b00000000000

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5.3.9.68 sys_cache_grp_sn_nodeid_reg9

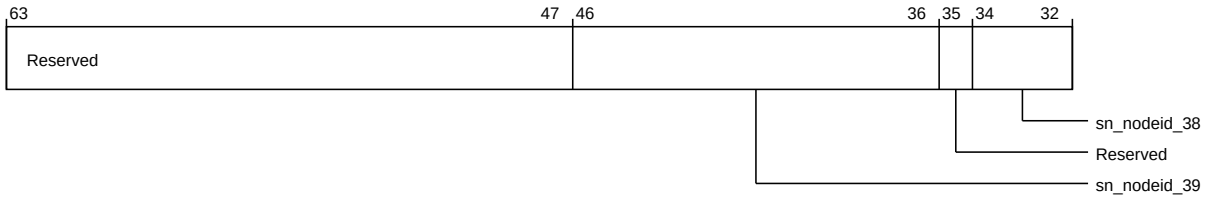
Configures hashed node IDs for system cache groups. Controls target SN node IDs 36 to 39.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1048
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1138: por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)



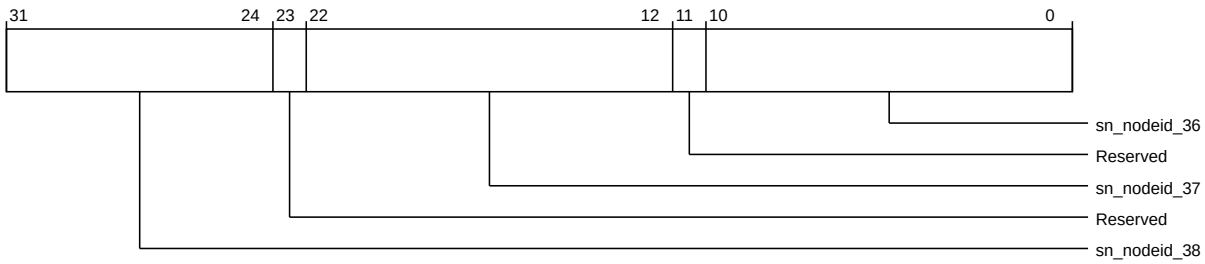
The following table shows the sys_cache_grp_sn_nodeid_reg9 higher register bit assignments.

Table 5-1152: por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_39	Hashed target SN node ID 39	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1139: por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg9 lower register bit assignments.

Table 5-1153: por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_37	Hashed target SN node ID 37	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_36	Hashed target SN node ID 36	RW	11'b00000000000

5.3.9.69 sys_cache_grp_sn_nodeid_reg10

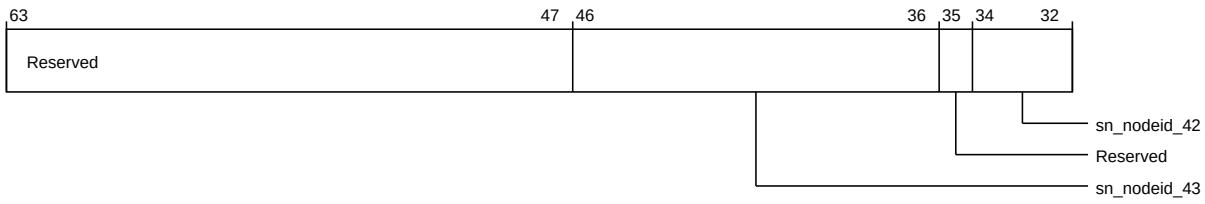
Configures hashed node IDs for system cache groups. Controls target SN node IDs 40 to 43.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1050
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1140: por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)



The following table shows the sys_cache_grp_sn_nodeid_reg10 higher register bit assignments.

Table 5-1154: por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_43	Hashed target SN node ID 43	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b00000000000

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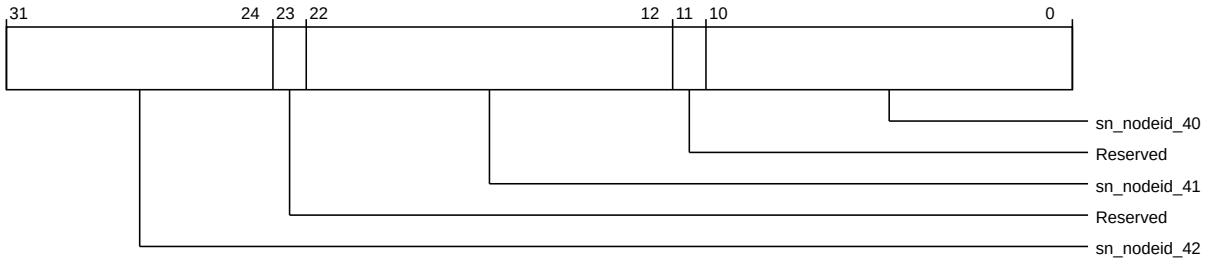
The following figure shows the lower register bit assignments.

Figure 5-1141: por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg10 lower register bit assignments.

Table 5-1155: por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_41	Hashed target SN node ID 41	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_40	Hashed target SN node ID 40	RW	11'b00000000000

5.3.9.70 sys_cache_grp_sn_nodeid_reg11

Configures hashed node IDs for system cache groups. Controls target SN node IDs 44 to 47.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1058
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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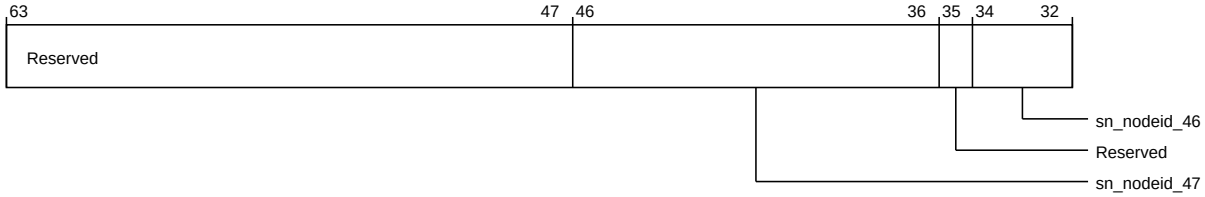
Figure 5-1142: por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)



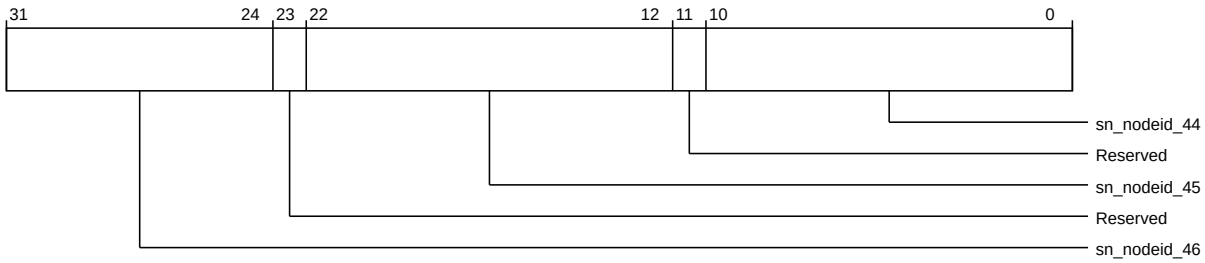
The following table shows the sys_cache_grp_sn_nodeid_reg11 higher register bit assignments.

Table 5-1156: por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_47	Hashed target SN node ID 47	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1143: por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg11 lower register bit assignments.

Table 5-1157: por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_45	Hashed target SN node ID 45	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_44	Hashed target SN node ID 44	RW	11'b00000000000

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5.3.9.71 sys_cache_grp_sn_nodeid_reg12

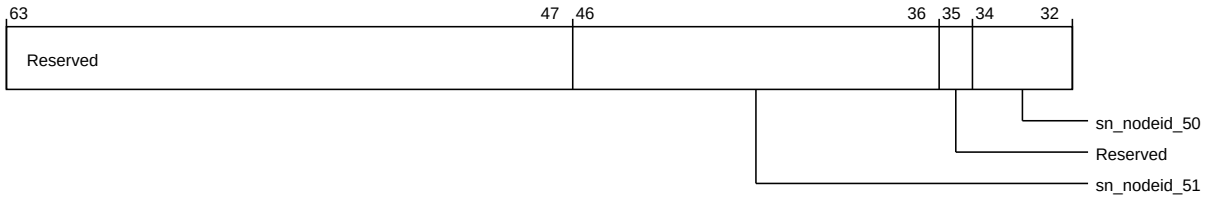
Configures hashed node IDs for system cache groups. Controls target SN node IDs 48 to 51.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1060
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1144: por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)



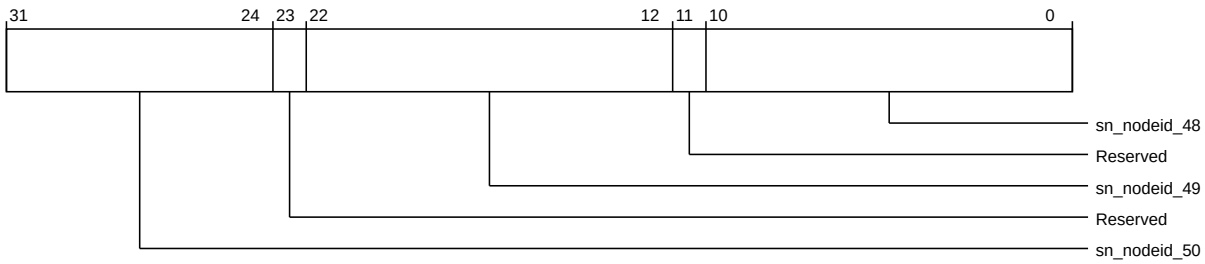
The following table shows the sys_cache_grp_sn_nodeid_reg12 higher register bit assignments.

Table 5-1158: por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_51	Hashed target SN node ID 51	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_50	Hashed target SN node ID 50	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1145: por_rnsam_sys_cache_grp_sn_nodeid_reg12 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg12 lower register bit assignments.

Table 5-1159: por_rnsam_sys_cache_grp_sn_nodeid_reg12 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_50	Hashed target SN node ID 50	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_49	Hashed target SN node ID 49	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_48	Hashed target SN node ID 48	RW	11'b00000000000

5.3.9.72 sys_cache_grp_sn_nodeid_reg13

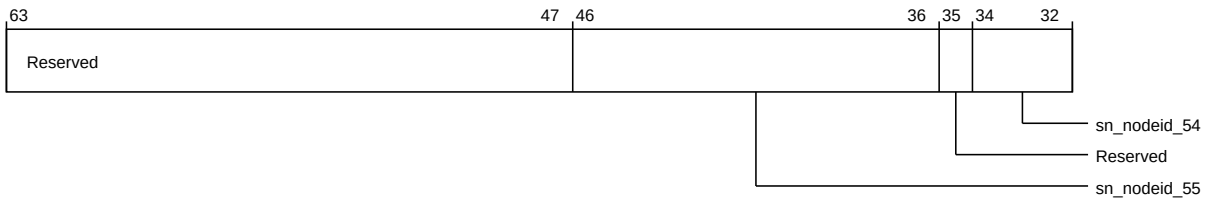
Configures hashed node IDs for system cache groups. Controls target SN node IDs 52 to 55.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1068
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1146: por_rnsam_sys_cache_grp_sn_nodeid_reg13 (high)



The following table shows the sys_cache_grp_sn_nodeid_reg13 higher register bit assignments.

Table 5-1160: por_rnsam_sys_cache_grp_sn_nodeid_reg13 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_55	Hashed target SN node ID 55	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_54	Hashed target SN node ID 54	RW	11'b00000000000

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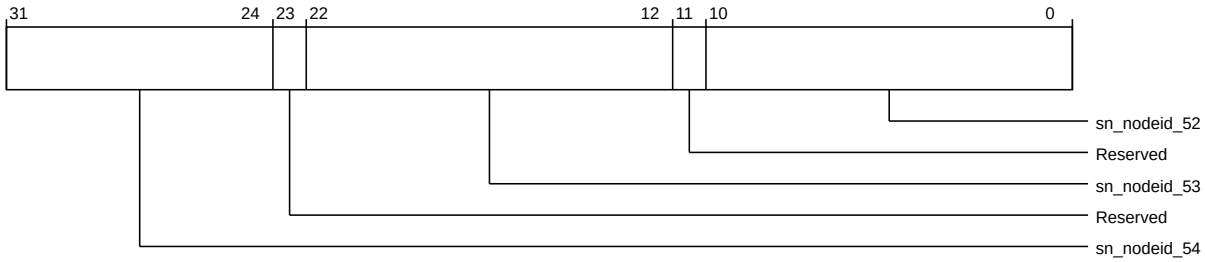
The following figure shows the lower register bit assignments.

Figure 5-1147: por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg13 lower register bit assignments.

Table 5-1161: por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_54	Hashed target SN node ID 54	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_53	Hashed target SN node ID 53	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_52	Hashed target SN node ID 52	RW	11'b00000000000

5.3.9.73 sys_cache_grp_sn_nodeid_reg14

Configures hashed node IDs for system cache groups. Controls target SN node IDs 56 to 59.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1070
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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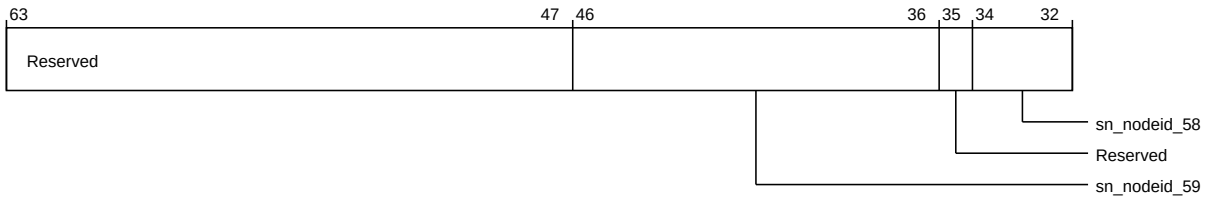
Figure 5-1148: por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)



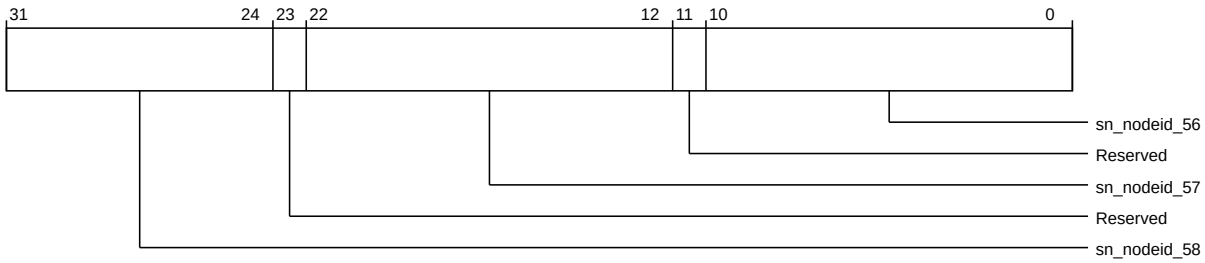
The following table shows the sys_cache_grp_sn_nodeid_reg14 higher register bit assignments.

Table 5-1162: por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_59	Hashed target SN node ID 59	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1149: por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)



The following table shows the sys_cache_grp_sn_nodeid_reg14 lower register bit assignments.

Table 5-1163: por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_57	Hashed target SN node ID 57	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_56	Hashed target SN node ID 56	RW	11'b00000000000

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5.3.9.74 sys_cache_grp_sn_nodeid_reg15

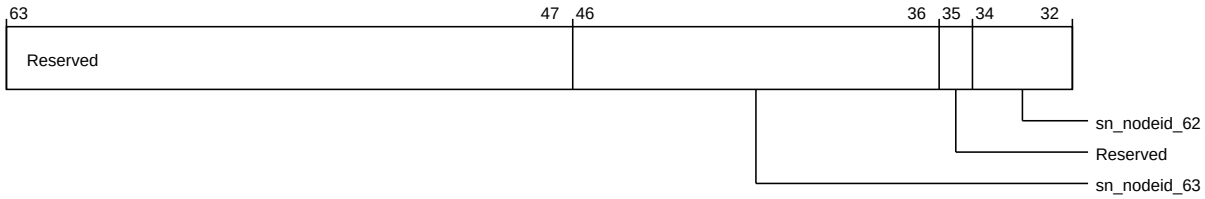
Configures hashed node IDs for system cache groups. Controls target SN node IDs 60 to 63.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1078
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1150: por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)



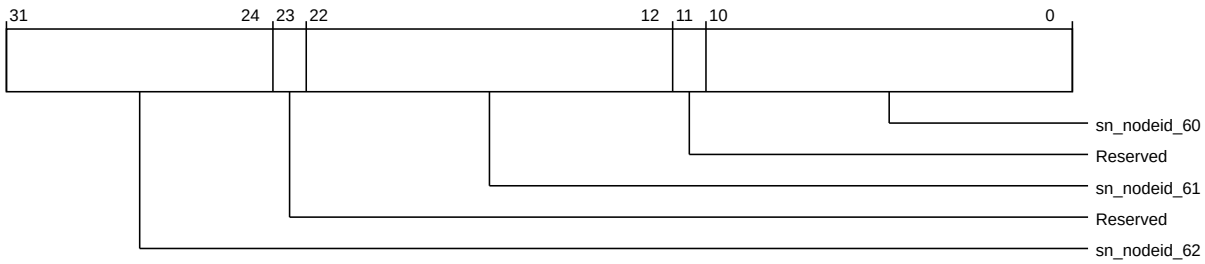
The following table shows the sys_cache_grp_sn_nodeid_reg15 higher register bit assignments.

Table 5-1164: por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_63	Hashed target SN node ID 63	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b00000000000

The following figure shows the lower register bit assignments.

Figure 5-1151: por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)



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The following table shows the sys_cache_grp_sn_nodeid_reg15 lower register bit assignments.

Table 5-1165: por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_61	Hashed target SN node ID 61	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_60	Hashed target SN node ID 60	RW	11'b00000000000

5.3.9.75 rnsam_status

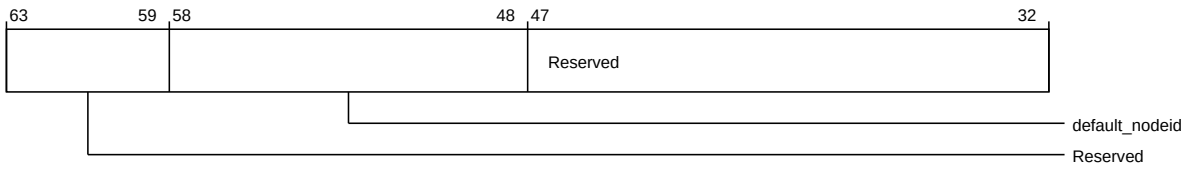
Functions as the default and programming mode status register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1100
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1152: por_rnsam_rnsam_status (high)



The following table shows the rnsam_status higher register bit assignments.

Table 5-1166: por_rnsam_rnsam_status (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	default_nodeid	Default Node ID	RW	Configuration dependent
47:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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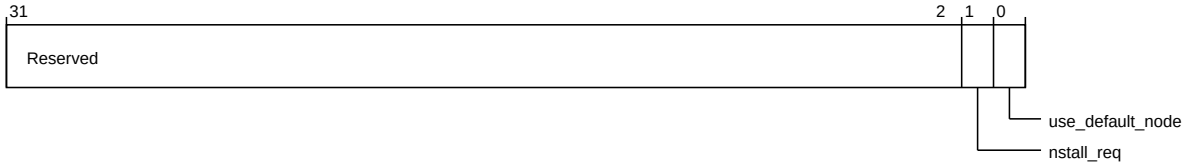
Figure 5-1153: por_rnsam_rnsam_status (low)



The following table shows the rnsam_status lower register bit assignments.

Table 5-1167: por_rnsam_rnsam_status (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	nstall_req	Indicates RN SAM is programmed and ready 1'b0: STALL requests 1'b1: UNSTALL requests	RW	1'b0
0	use_default_node	Indicates target ID selection mode 1'b0: Enables RN SAM to hash address bits and generate target ID 1'b1: Uses default target ID	RW	1'b1

5.3.9.76 gic_mem_region_reg

Configures GIC memory region.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1108
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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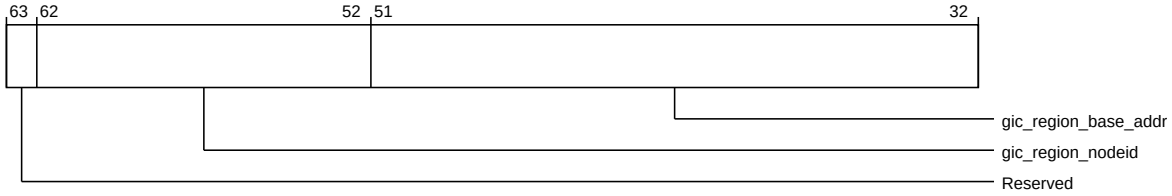
Figure 5-1154: por_rnsam_gic_mem_region_reg (high)



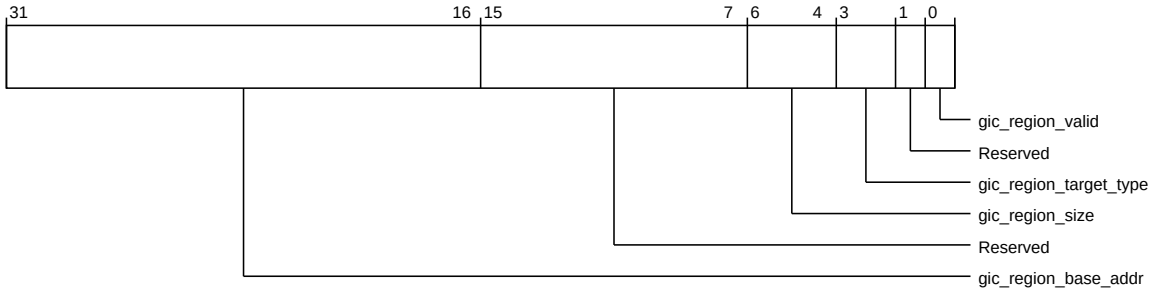
The following table shows the gic_mem_region_reg higher register bit assignments.

Table 5-1168: por_rnsam_gic_mem_region_reg (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:52	gic_region_nodeid	GIC node ID	RW	11'b00000000000
51:32	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	36'h000000000

The following figure shows the lower register bit assignments.

Figure 5-1155: por_rnsam_gic_mem_region_reg (low)



The following table shows the gic_mem_region_reg lower register bit assignments.

Table 5-1169: por_rnsam_gic_mem_region_reg (low)

Bits	Field name	Description	Type	Reset
31:16	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	36'h000000000
15:7	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
6:4	gic_region_size	GIC memory region size 3'b000: 64KB 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB CONSTRAINT: Memory region must be a power of 2.	RW	3'b000
3:2	gic_region_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	gic_region_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.77 sys_cache_grp_cal_mode_reg

Configures the HN-F CAL mode support for all system cache groups.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1120
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

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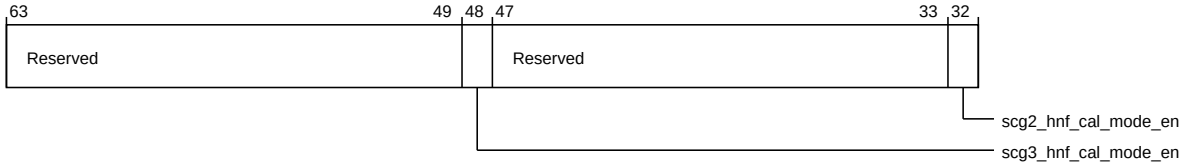
Figure 5-1156: por_rnsam_sys_cache_grp_cal_mode_reg (high)



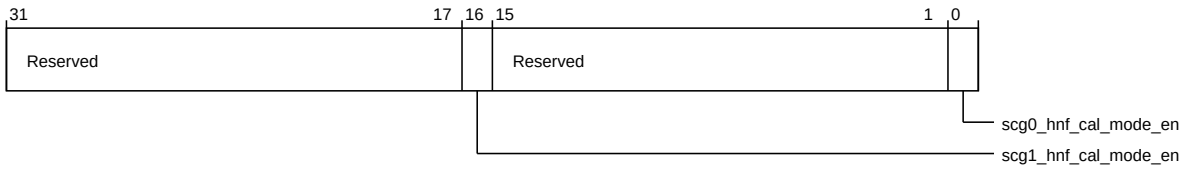
The following table shows the sys_cache_grp_cal_mode_reg higher register bit assignments.

Table 5-1170: por_rnsam_sys_cache_grp_cal_mode_reg (high)

Bits	Field name	Description	Type	Reset
63:49	Reserved	Reserved	RO	-
48	scg3_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 3	RW	1'b0
47:33	Reserved	Reserved	RO	-
32	scg2_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 2	RW	1'b0

The following figure shows the lower register bit assignments.

Figure 5-1157: por_rnsam_sys_cache_grp_cal_mode_reg (low)



The following table shows the sys_cache_grp_cal_mode_reg lower register bit assignments.

Table 5-1171: por_rnsam_sys_cache_grp_cal_mode_reg (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	scg1_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 1	RW	1'b0
15:1	Reserved	Reserved	RO	-
0	scg0_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 0	RW	1'b0

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5.3.9.78 sys_cache_grp_sn_sam_cfg0

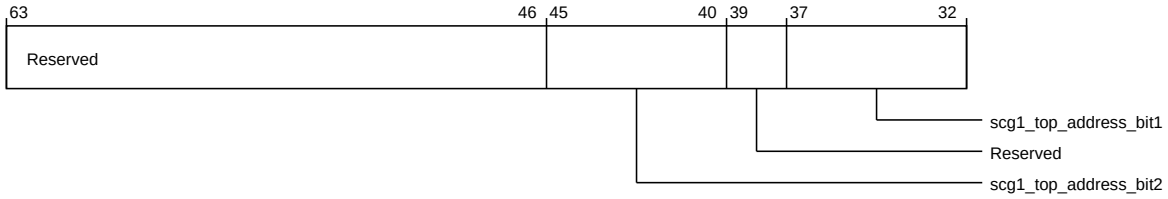
Configures top address bits for SN SAM system cache groups 0 and 1. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 > top_address_bit1 > top_address_bit0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1140
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1158: por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)



The following table shows the sys_cache_grp_sn_sam_cfg0 higher register bit assignments.

Table 5-1172: por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	scg1_top_address_bit2	Top address bit 2 for system cache group 1	RW	6'h00
39:38	Reserved	Reserved	RO	-
37:32	scg1_top_address_bit1	Top address bit 1 for system cache group 1	RW	6'h00

The following figure shows the lower register bit assignments.

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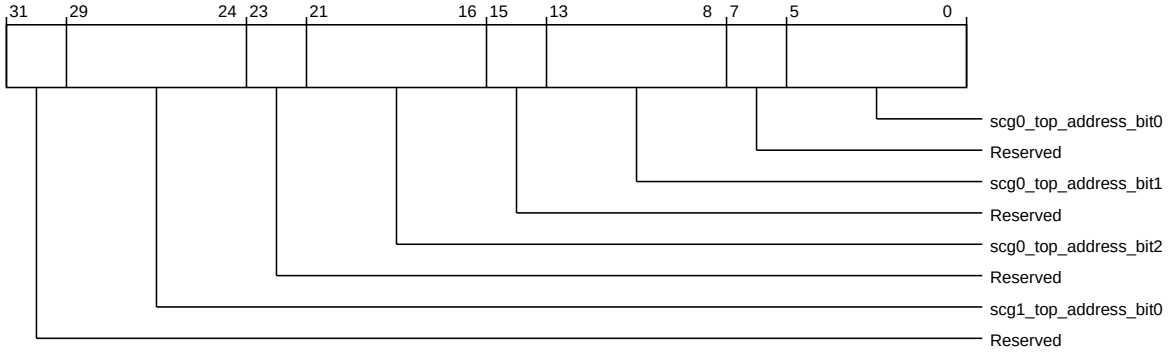
Figure 5-1159: por_rnsam_sys_cache_grp_sn_sam_cfg0 (low)



The following table shows the sys_cache_grp_sn_sam_cfg0 lower register bit assignments.

Table 5-1173: por_rnsam_sys_cache_grp_sn_sam_cfg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	scg1_top_address_bit0	Top address bit 0 for system cache group 1	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	scg0_top_address_bit2	Top address bit 2 for system cache group 0	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	scg0_top_address_bit1	Top address bit 1 for system cache group 0	RW	6'h00
7:6	Reserved	Reserved	RO	-
5:0	scg0_top_address_bit0	Top address bit 0 for system cache group 0	RW	6'h00

5.3.9.79 sys_cache_grp_sn_sam_cfg1

Configures top address bits for SN SAM system cache groups 2 and 3. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 andgt; top_address_bit1 andgt; top_address_bit0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1148
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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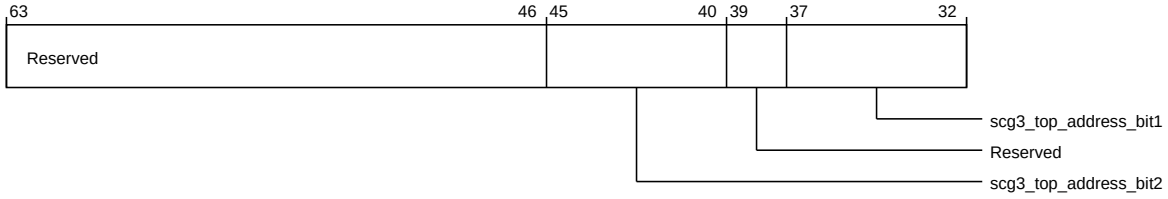
Figure 5-1160: por_rnsam_sys_cache_grp_sn_sam_cfg1 (high)



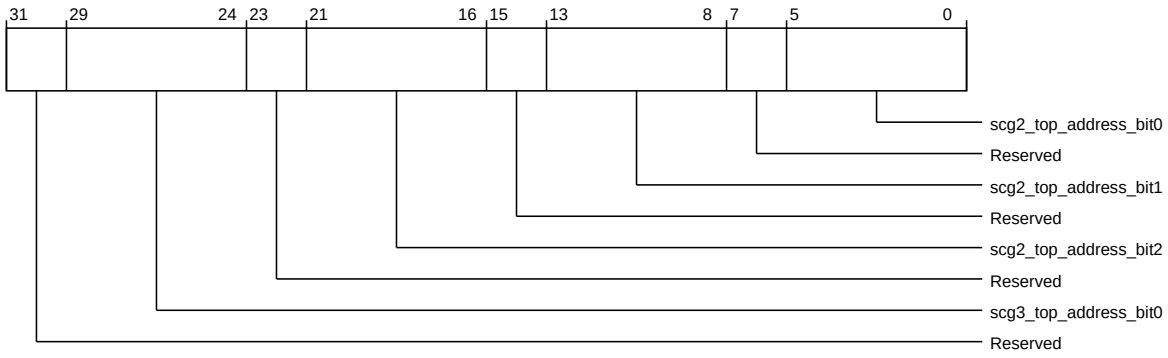
The following table shows the sys_cache_grp_sn_sam_cfg1 higher register bit assignments.

Table 5-1174: por_rnsam_sys_cache_grp_sn_sam_cfg1 (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	scg3_top_address_bit2	Top address bit 2 for system cache group 3	RW	6'h00
39:38	Reserved	Reserved	RO	-
37:32	scg3_top_address_bit1	Top address bit 1 for system cache group 3	RW	6'h00

The following figure shows the lower register bit assignments.

Figure 5-1161: por_rnsam_sys_cache_grp_sn_sam_cfg1 (low)



The following table shows the sys_cache_grp_sn_sam_cfg1 lower register bit assignments.

Table 5-1175: por_rnsam_sys_cache_grp_sn_sam_cfg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	scg3_top_address_bit0	Top address bit 0 for system cache group 3	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	scg2_top_address_bit2	Top address bit 2 for system cache group 2	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	scg2_top_address_bit1	Top address bit 1 for system cache group 2	RW	6'h00
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	scg2_top_address_bit0	Top address bit 0 for system cache group 2	RW	6'h00

5.3.9.80 sys_cache_grp_hn_cpa_en_reg

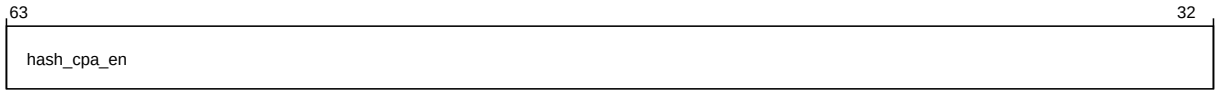
Configures CCIX port aggregation mode for hashed HN node IDs

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1180
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1162: por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)



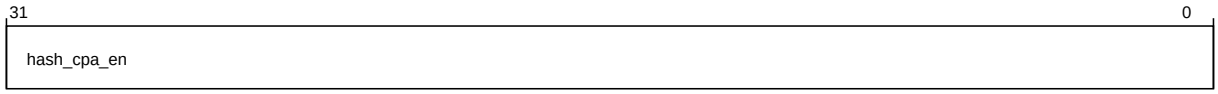
The following table shows the sys_cache_grp_hn_cpa_en_reg higher register bit assignments.

Table 5-1176: por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)

Bits	Field name	Description	Type	Reset
63:32	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1163: por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)



The following table shows the sys_cache_grp_hn_cpa_en_reg lower register bit assignments.

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Table 5-1177: por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)

Bits	Field name	Description	Type	Reset
31:0	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

5.3.9.81 sys_cache_grp_hn_cpa_grp_reg

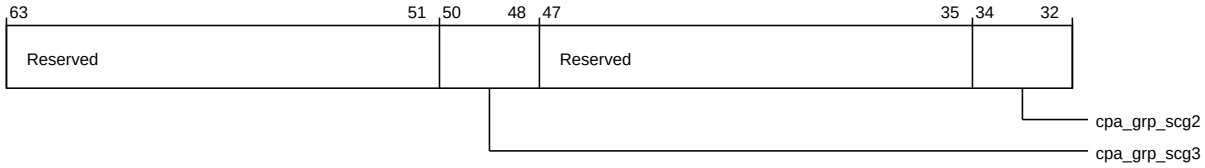
Configures CCIX port aggregation group ID for each System Cache Group

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1190
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1164: por_rnsam_sys_cache_grp_hn_cpa_grp_reg (high)



The following table shows the sys_cache_grp_hn_cpa_grp_reg higher register bit assignments.

Table 5-1178: por_rnsam_sys_cache_grp_hn_cpa_grp_reg (high)

Bits	Field name	Description	Type	Reset
63:51	Reserved	Reserved	RO	-
50:48	cpa_grp_scg3	Specifies CCIX port aggregation group ID for System Cache Group 3 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'b000
47:35	Reserved	Reserved	RO	-

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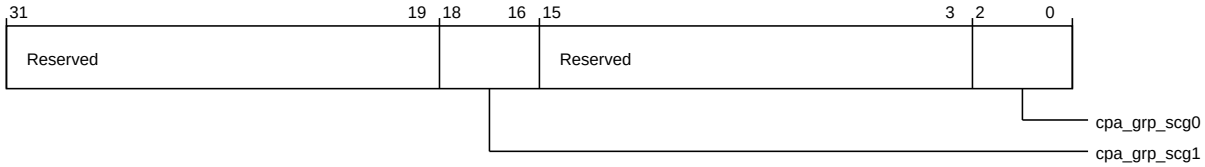
Bits	Field name	Description	Type	Reset
34:32	cpa_grp_scg2	Specifies CCIX port aggregation group ID for System Cache Group 2 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'b000

The following figure shows the lower register bit assignments.

Figure 5-1165: por_rnsam_sys_cache_grp_hn_cpa_grp_reg (low)



The following table shows the sys_cache_grp_hn_cpa_grp_reg lower register bit assignments.

Table 5-1179: por_rnsam_sys_cache_grp_hn_cpa_grp_reg (low)

Bits	Field name	Description	Type	Reset
31:19	Reserved	Reserved	RO	-
18:16	cpa_grp_scg1	Specifies CCIX port aggregation group ID for System Cache Group 1 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'b000
15:3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	cpa_grp_scg0	Specifies CCIX port aggregation group ID for System Cache Group 0 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'b000

5.3.9.82 cml_port_aggr_mode_ctrl_reg

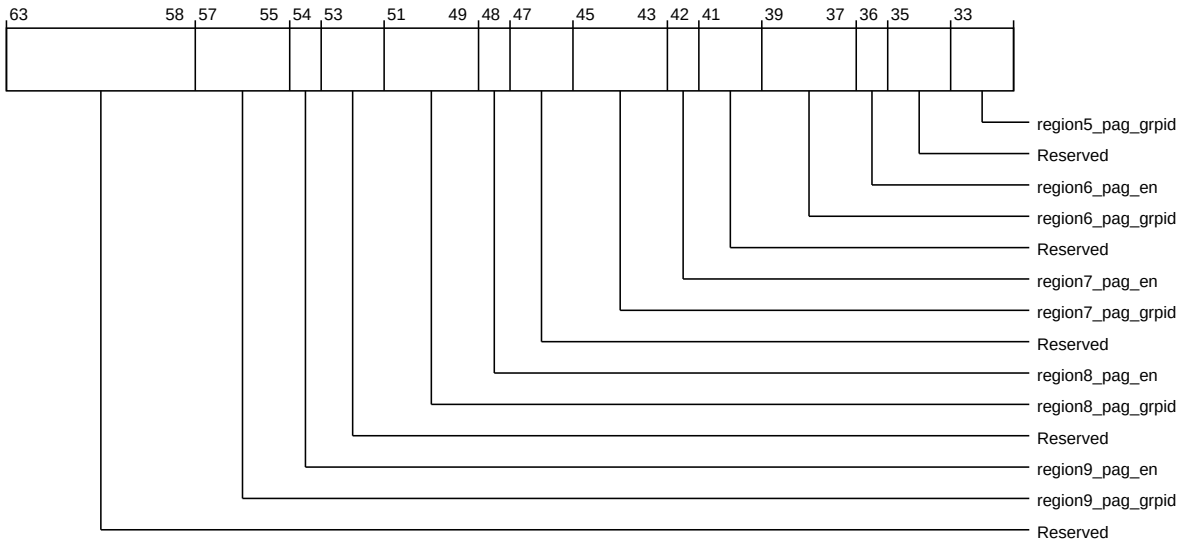
Configures the CCIX port aggregation modes for all non-hashed memory regions.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11A0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1166: por_rnsam_cml_port_aggr_mode_ctrl_reg (high)



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The following table shows the cml_port_aggr_mode_ctrl_reg higher register bit assignments.

Table 5-1180: por_rnsam_cml_port_aggr_mode_ctrl_reg (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:55	region9_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
54	region9_pag_en	Enables the CPA mode for non-hashed memory region 9	RW	1'b0
53:52	Reserved	Reserved	RO	-
51:49	region8_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	region8_pag_en	Enables the CPA mode for non-hashed memory region 8	RW	1'b0
47:46	Reserved	Reserved	RO	-
45:43	region7_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
42	region7_pag_en	Enables the CPA mode for non-hashed memory region 7	RW	1'b0
41:40	Reserved	Reserved	RO	-

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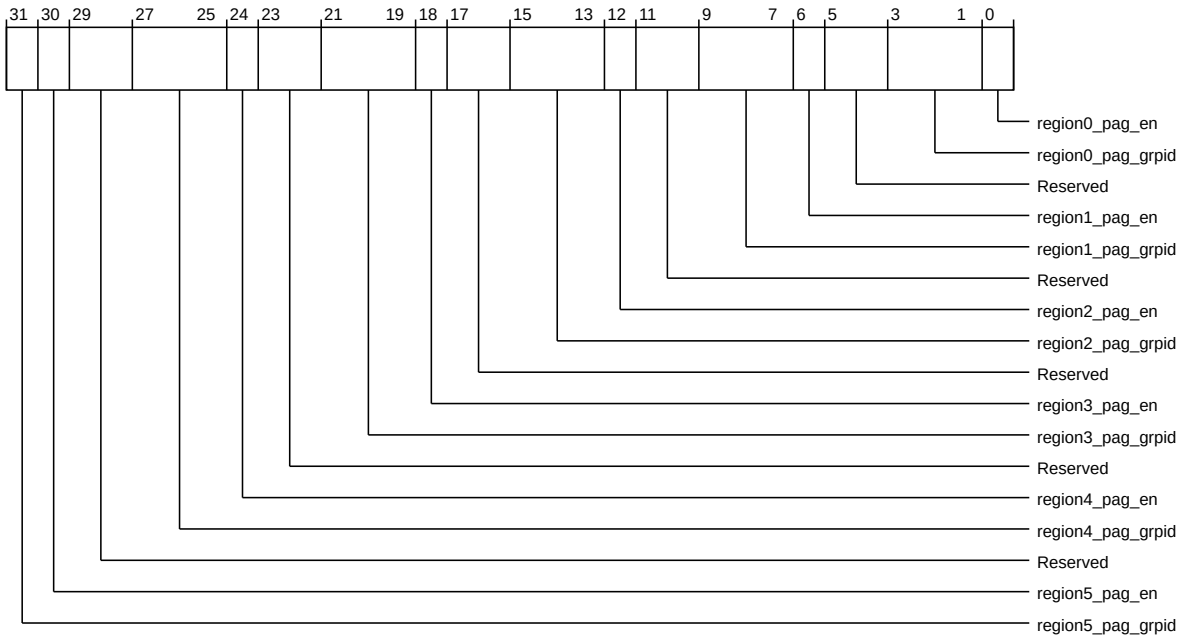
Bits	Field name	Description	Type	Reset
39:37	region6_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
36	region6_pag_en	Enables the CPA mode for non-hashed memory region 6	RW	1'b0
35:34	Reserved	Reserved	RO	-
33:32	region5_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0

The following figure shows the lower register bit assignments.

Figure 5-1167: por_rnsam_cml_port_aggr_mode_ctrl_reg (low)



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The following table shows the cml_port_aggr_mode_ctrl_reg lower register bit assignments.

Table 5-1181: por_rnsam_cml_port_aggr_mode_ctrl_reg (low)

Bits	Field name	Description	Type	Reset
31	region5_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
30	region5_pag_en	Enables the CPA mode for non-hashed memory region 5	RW	1'b0
29:28	Reserved	Reserved	RO	-
27:25	region4_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
24	region4_pag_en	Enables the CPA mode for non-hashed memory region 4	RW	1'b0
23:22	Reserved	Reserved	RO	-
21:19	region3_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
18	region3_pag_en	Enables the CPA mode for non-hashed memory region 3	RW	1'b0
17:16	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
15:13	region2_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
12	region2_pag_en	Enables the CPA mode for non-hashed memory region 2	RW	1'b0
11:10	Reserved	Reserved	RO	-
9:7	region1_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
6	region1_pag_en	Enables the CPA mode for non-hashed memory region 1	RW	1'b0
5:4	Reserved	Reserved	RO	-
3:1	region0_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
0	region0_pag_en	Enables the CPA mode for non-hashed memory region 0	RW	1'b0

5.3.9.83 cml_port_aggr_mode_ctrl_reg1

Configures the CCIX port aggregation modes for non-hashed memory regions 8 through 19.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11A8

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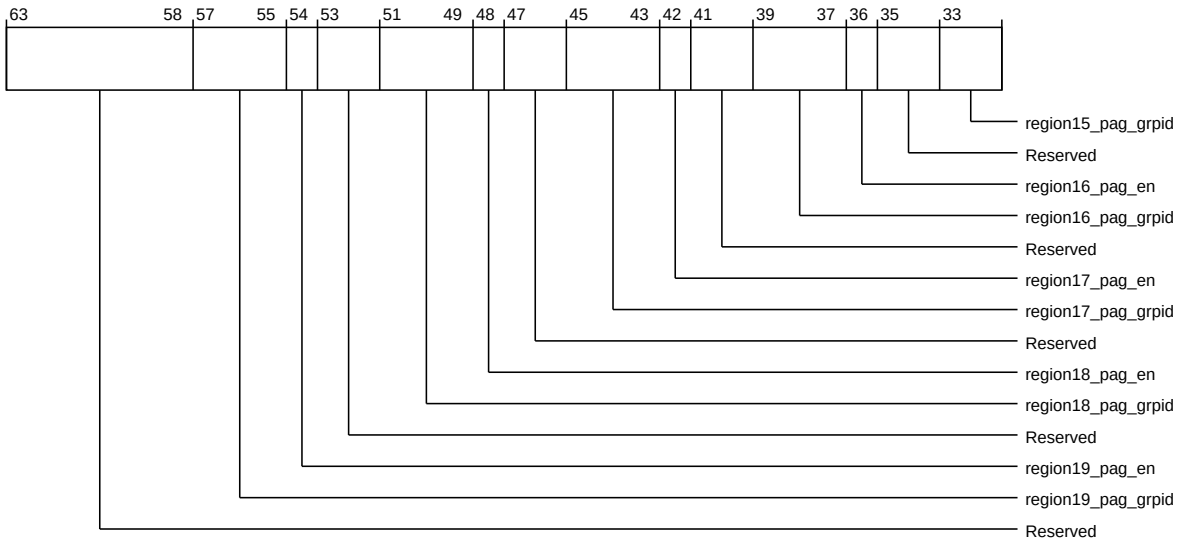
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1168: por_rnsam_cml_port_aggr_mode_ctrl_reg1 (high)



The following table shows the cml_port_aggr_mode_ctrl_reg1 higher register bit assignments.

Table 5-1182: por_rnsam_cml_port_aggr_mode_ctrl_reg1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:55	region19_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
54	region19_pag_en	Enables the CPA mode for non-hashed memory region 19	RW	1'b0
53:52	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
51:49	region18_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
48	region18_pag_en	Enables the CPA mode for non-hashed memory region 18	RW	1'b0
47:46	Reserved	Reserved	RO	-
45:43	region17_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
42	region17_pag_en	Enables the CPA mode for non-hashed memory region 17	RW	1'b0
41:40	Reserved	Reserved	RO	-
39:37	region16_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
36	region16_pag_en	Enables the CPA mode for non-hashed memory region 16	RW	1'b0
35:34	Reserved	Reserved	RO	-
33:32	region15_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0

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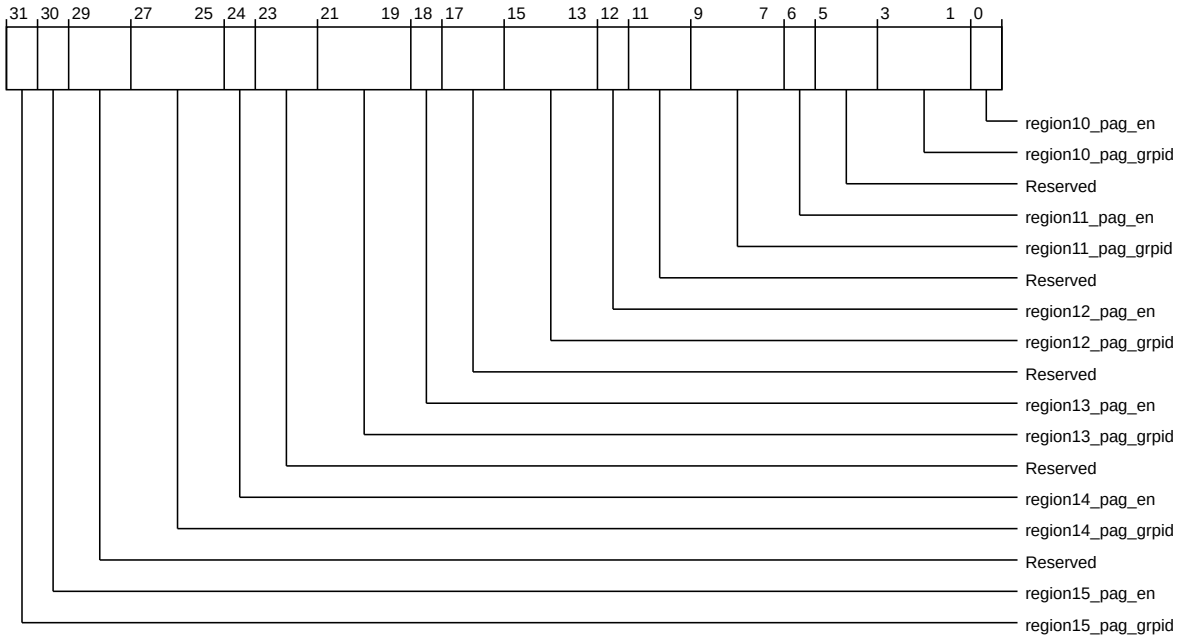
The following figure shows the lower register bit assignments.

Figure 5-1169: por_rnsam_cml_port_aggr_mode_ctrl_reg1 (low)



The following table shows the cml_port_aggr_mode_ctrl_reg1 lower register bit assignments.

Table 5-1183: por_rnsam_cml_port_aggr_mode_ctrl_reg1 (low)

Bits	Field name	Description	Type	Reset
31	region15_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
30	region15_pag_en	Enables the CPA mode for non-hashed memory region 15	RW	1'b0
29:28	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
27:25	region14_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
24	region14_pag_en	Enables the CPA mode for non-hashed memory region 14	RW	1'b0
23:22	Reserved	Reserved	RO	-
21:19	region13_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
18	region13_pag_en	Enables the CPA mode for non-hashed memory region 13	RW	1'b0
17:16	Reserved	Reserved	RO	-
15:13	region12_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
12	region12_pag_en	Enables the CPA mode for non-hashed memory region 12	RW	1'b0
11:10	Reserved	Reserved	RO	-
9:7	region11_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0

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Bits	Field name	Description	Type	Reset
6	region11_pag_en	Enables the CPA mode for non-hashed memory region 11	RW	1'b0
5:4	Reserved	Reserved	RO	-
3:1	region10_pag_grpid	Specifies CCIX port aggregation group ID 3'b000: CPA Group ID 0 3'b001: CPA Group ID 1 3'b010: CPA Group ID 2 3'b011: CPA Group ID 3 3'b100: CPA Group ID 4	RW	3'h0
0	region10_pag_en	Enables the CPA mode for non-hashed memory region 10	RW	1'b0

5.3.9.84 cml_port_aggr_grp0_add_mask

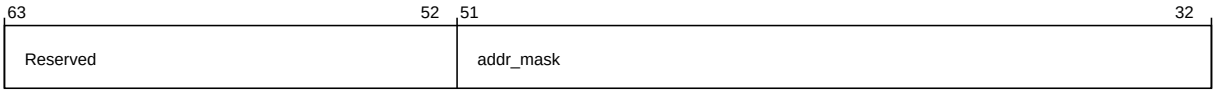
Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11C0
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1170: por_rnsam_cml_port_aggr_grp0_add_mask (high)



The following table shows the cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 5-1184: por_rnsam_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

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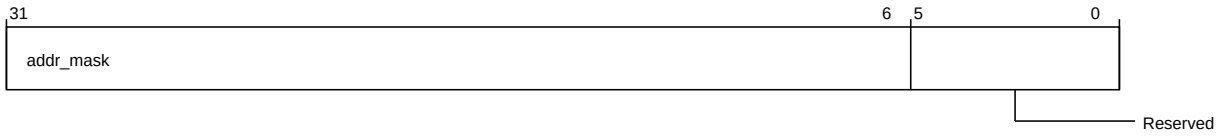
The following figure shows the lower register bit assignments.

Figure 5-1171: por_rnsam_cml_port_aggr_grp0_add_mask (low)



The following table shows the cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 5-1185: por_rnsam_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.85 cml_port_aggr_grp1_add_mask

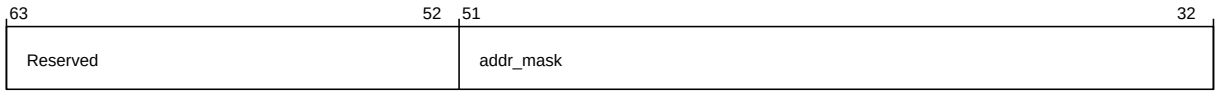
Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11C8
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1172: por_rnsam_cml_port_aggr_grp1_add_mask (high)



The following table shows the cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 5-1186: por_rnsam_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-

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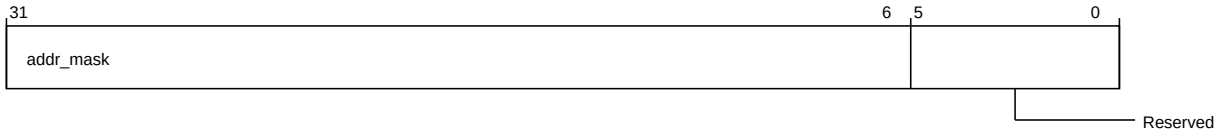
Bits	Field name	Description	Type	Reset
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1173: por_rnsam_cml_port_aggr_grp1_add_mask (low)



The following table shows the cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 5-1187: por_rnsam_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.86 cml_port_aggr_grp2_add_mask

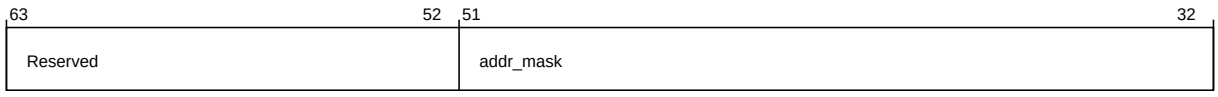
Configures the CCIX port aggregation address mask for group 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11D0
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1174: por_rnsam_cml_port_aggr_grp2_add_mask (high)



The following table shows the cml_port_aggr_grp2_add_mask higher register bit assignments.

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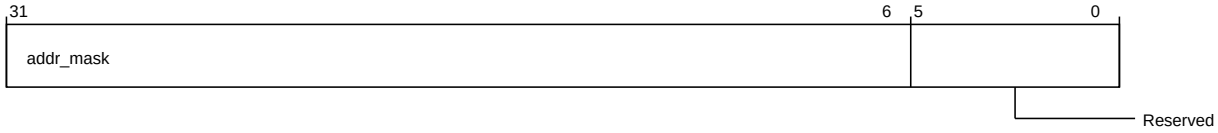
Table 5-1188: por_rnsam_cml_port_aggr_grp2_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1175: por_rnsam_cml_port_aggr_grp2_add_mask (low)



The following table shows the cml_port_aggr_grp2_add_mask lower register bit assignments.

Table 5-1189: por_rnsam_cml_port_aggr_grp2_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.87 cml_port_aggr_grp3_add_mask

Configures the CCIX port aggregation address mask for group 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11D8
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1176: por_rnsam_cml_port_aggr_grp3_add_mask (high)



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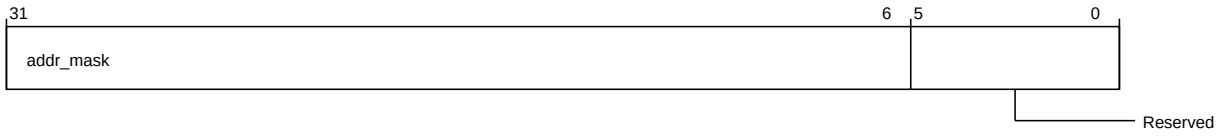
The following table shows the cml_port_aggr_grp3_add_mask higher register bit assignments.

Table 5-1190: por_rnsam_cml_port_aggr_grp3_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1177: por_rnsam_cml_port_aggr_grp3_add_mask (low)



The following table shows the cml_port_aggr_grp3_add_mask lower register bit assignments.

Table 5-1191: por_rnsam_cml_port_aggr_grp3_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.88 cml_port_aggr_grp4_add_mask

Configures the CCIX port aggregation address mask for group 4.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11E0
Register reset 64'b1111111111111111111111111111111111111111111111111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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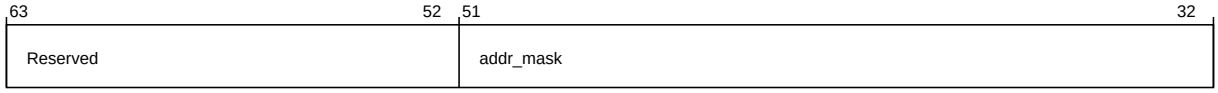
Figure 5-1178: por_rnsam_cml_port_aggr_grp4_add_mask (high)



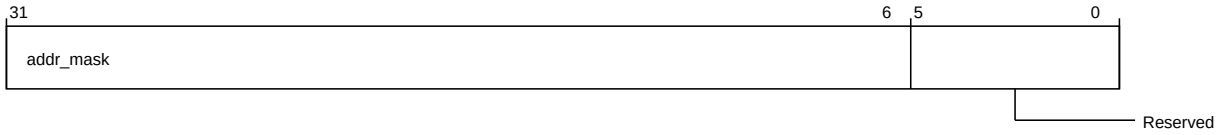
The following table shows the cml_port_aggr_grp4_add_mask higher register bit assignments.

Table 5-1192: por_rnsam_cml_port_aggr_grp4_add_mask (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF

The following figure shows the lower register bit assignments.

Figure 5-1179: por_rnsam_cml_port_aggr_grp4_add_mask (low)



The following table shows the cml_port_aggr_grp4_add_mask lower register bit assignments.

Table 5-1193: por_rnsam_cml_port_aggr_grp4_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	46'h3FFFFFFFFFF
5:0	Reserved	Reserved	RO	-

5.3.9.89 cml_port_aggr_grp_reg0

Configures the CCIX port aggregation port Node IDs

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11F0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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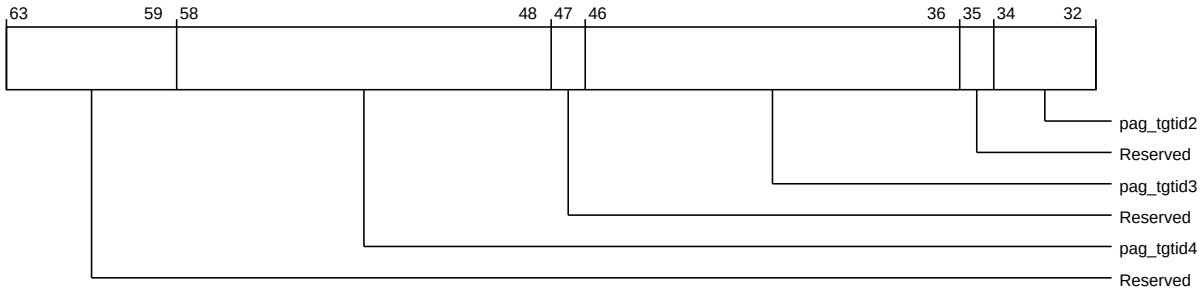
The following figure shows the higher register bit assignments.

Figure 5-1180: por_rnsam_cml_port_aggr_grp_reg0 (high)



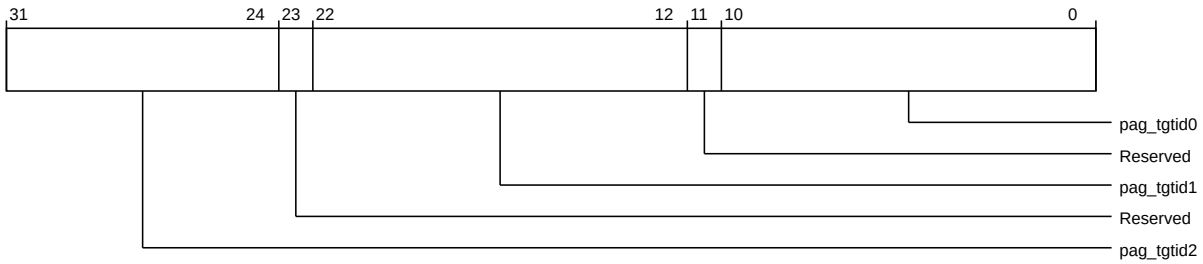
The following table shows the cml_port_aggr_grp_reg0 higher register bit assignments.

Table 5-1194: por_rnsam_cml_port_aggr_grp_reg0 (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	pag_tgtid4	Specifies target ID 4 for CPAG	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	pag_tgtid3	Specifies target ID 3 for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag_tgtid2	Specifies target ID 2 for CPAG	RW	11'b0

The following figure shows the lower register bit assignments.

Figure 5-1181: por_rnsam_cml_port_aggr_grp_reg0 (low)



The following table shows the cml_port_aggr_grp_reg0 lower register bit assignments.

Table 5-1195: por_rnsam_cml_port_aggr_grp_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	pag_tgtid2	Specifies target ID 2 for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag_tgtid1	Specifies target ID 1 for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:0	pag_tgtid0	Specifies target ID 0 for CPAG	RW	11'b0

5.3.9.90 cml_port_aggr_grp_reg1

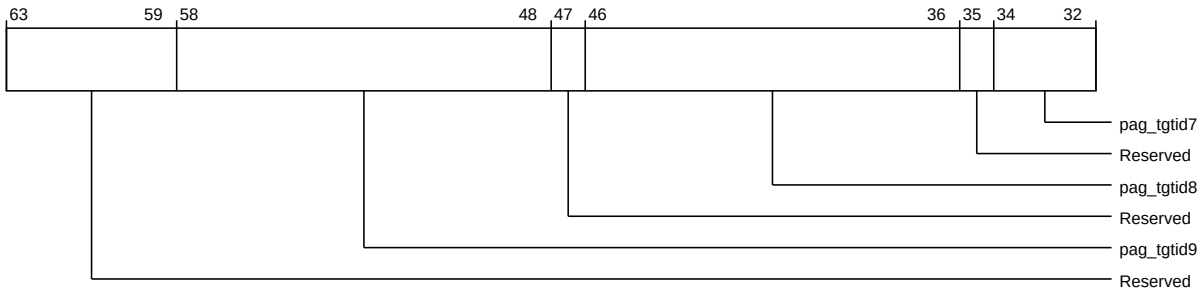
Configures the CCIX port aggregation port Node IDs

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h11F8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1182: por_rnsam_cml_port_aggr_grp_reg1 (high)



The following table shows the cml_port_aggr_grp_reg1 higher register bit assignments.

Table 5-1196: por_rnsam_cml_port_aggr_grp_reg1 (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	pag_tgtid9	Specifies target ID 9 for CPAG	RW	11'b0
47	Reserved	Reserved	RO	-
46:36	pag_tgtid8	Specifies target ID 8 for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag_tgtid7	Specifies target ID 7 for CPAG	RW	11'b0

The following figure shows the lower register bit assignments.

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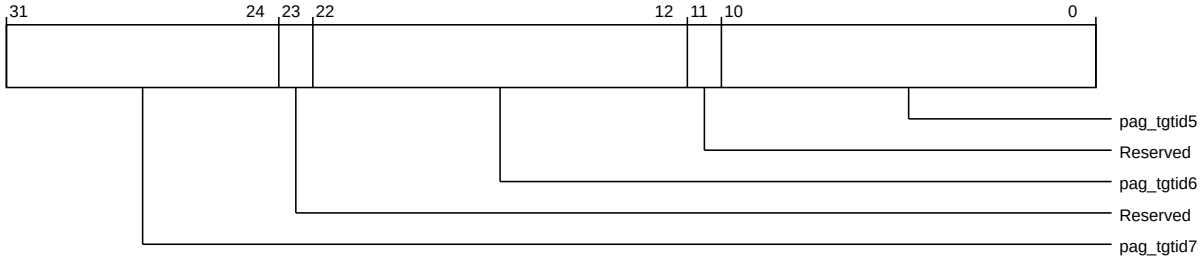
Figure 5-1183: por_rnsam_cml_port_aggr_grp_reg1 (low)



The following table shows the cml_port_aggr_grp_reg1 lower register bit assignments.

Table 5-1197: por_rnsam_cml_port_aggr_grp_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	pag_tgtid7	Specifies target ID 7 for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag_tgtid6	Specifies target ID 6 for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag_tgtid5	Specifies target ID 5 for CPAG	RW	11'b0

5.3.9.91 cml_port_aggr_ctrl_reg

Configures the CCIX port aggregation port IDs for group 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1208
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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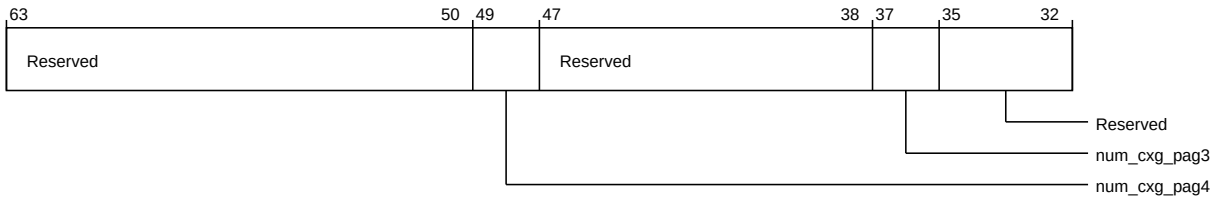
Figure 5-1184: por_rnsam_cml_port_aggr_ctrl_reg (high)



The following table shows the cml_port_aggr_ctrl_reg higher register bit assignments.

Table 5-1198: por_rnsam_cml_port_aggr_ctrl_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag4	Specifies the number of CXRAs in CPAG 4 Constraint: May use pag_tgtid8 through pag_tgtid9 of cml_port_aggr_grp_reg1 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
47:38	Reserved	Reserved	RO	-
37:36	num_cxg_pag3	Specifies the number of CXRAs in CPAG 3 Constraint: May use pag_tgtid6 through pag_tgtid7 of cml_port_aggr_grp_reg1 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
35:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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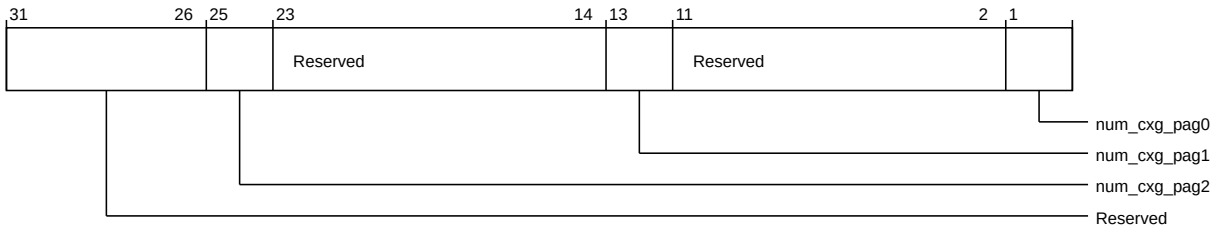
Figure 5-1185: por_rnsam_cml_port_aggr_ctrl_reg (low)



The following table shows the cml_port_aggr_ctrl_reg lower register bit assignments.

Table 5-1199: por_rnsam_cml_port_aggr_ctrl_reg (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	num_cxg_pag2	Specifies the number of CXRAs in CPAG 2 Constraint: May use pag_tgtid4 through pag_tgtid7 of cml_port_aggr_grp_reg[0,1] 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
23:14	Reserved	Reserved	RO	-
13:12	num_cxg_pag1	Specifies the number of CXRAs in CPAG 1 Constraint: May use pag_tgtid2 through pag_tgtid3 of cml_port_aggr_grp_reg0 2'b00: 1 port used 2'b01: 2 ports used 2'b10: Reserved 2'b11: Reserved	RW	2'b0
11:2	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
1:0	num_cxg_pag0	Specifies the number of CXRAs in CPAG 0 Constraint: May use pag_tgtid0 through pag_tgtid7 of cml_port_aggr_grp_reg[0,1] 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: 8 ports used	RW	2'b0

5.3.9.92 sam_qos_mem_region_reg0

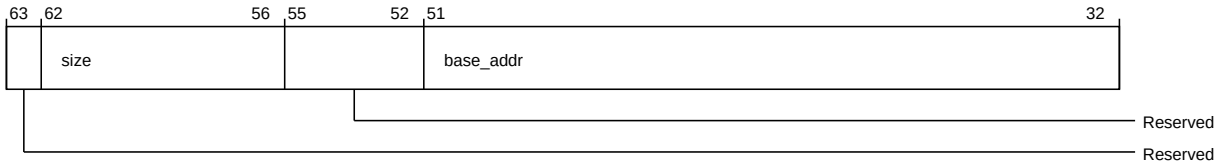
Configures the QoS value for memory region 0

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1280
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1186: por_rnsam_sam_qos_mem_region_reg0 (high)



The following table shows the sam_qos_mem_region_reg0 higher register bit assignments.

Table 5-1200: por_rnsam_sam_qos_mem_region_reg0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-

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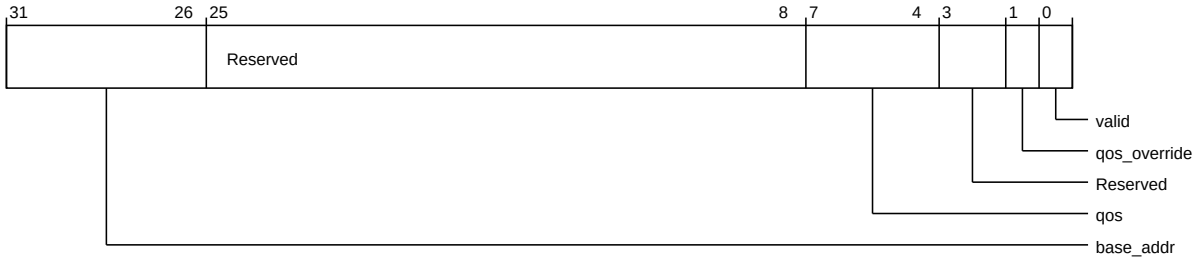
Bits	Field name	Description	Type	Reset
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1187: por_rnsam_sam_qos_mem_region_reg0 (low)



The following table shows the sam_qos_mem_region_reg0 lower register bit assignments.

Table 5-1201: por_rnsam_sam_qos_mem_region_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

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5.3.9.93 sam_qos_mem_region_reg1

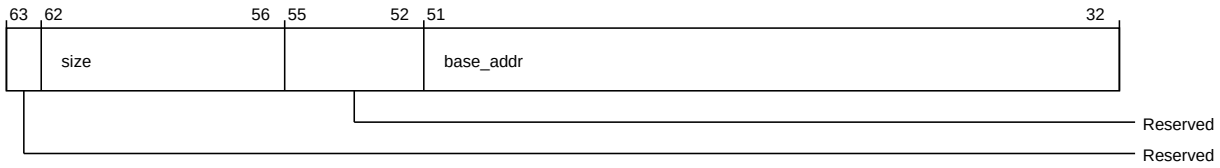
Configures the QoS value for memory region 1

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1288
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1188: por_rnsam_sam_qos_mem_region_reg1 (high)



The following table shows the sam_qos_mem_region_reg1 higher register bit assignments.

Table 5-1202: por_rnsam_sam_qos_mem_region_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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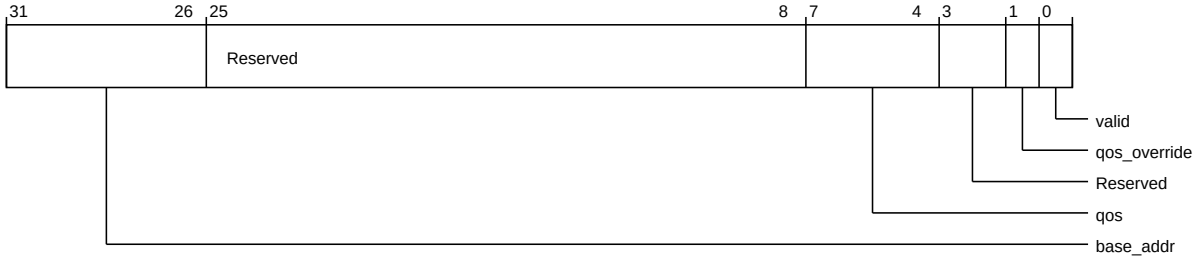
Figure 5-1189: por_rnsam_sam_qos_mem_region_reg1 (low)



The following table shows the sam_qos_mem_region_reg1 lower register bit assignments.

Table 5-1203: por_rnsam_sam_qos_mem_region_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.94 sam_qos_mem_region_reg2

Configures the QoS value for memory region 2

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1290
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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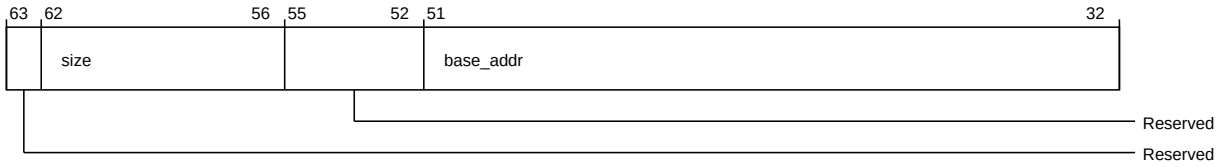
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1190: por_rnsam_sam_qos_mem_region_reg2 (high)



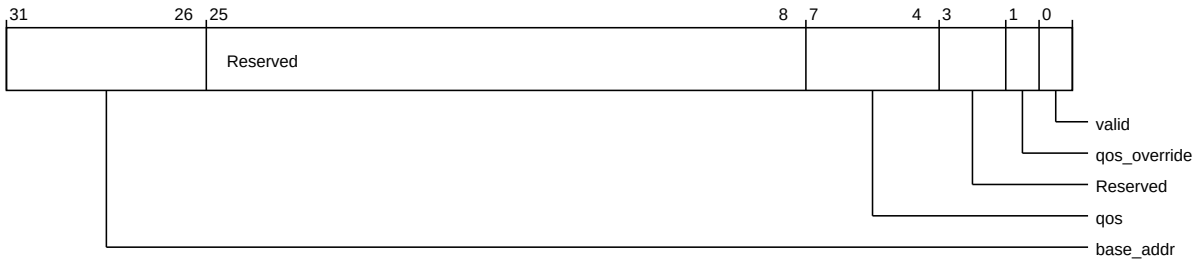
The following table shows the sam_qos_mem_region_reg2 higher register bit assignments.

Table 5-1204: por_rnsam_sam_qos_mem_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1191: por_rnsam_sam_qos_mem_region_reg2 (low)



The following table shows the sam_qos_mem_region_reg2 lower register bit assignments.

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Table 5-1205: por_rnsam_sam_qos_mem_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.95 sam_qos_mem_region_reg3

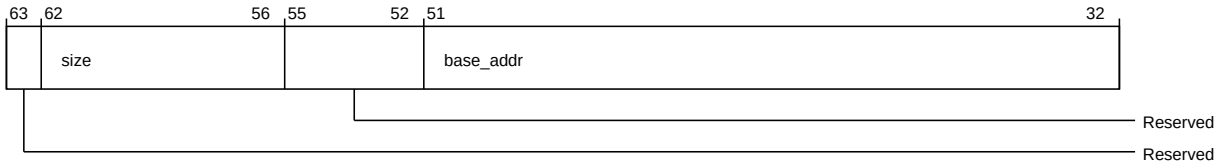
Configures the QoS value for memory region 3

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1298
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1192: por_rnsam_sam_qos_mem_region_reg3 (high)



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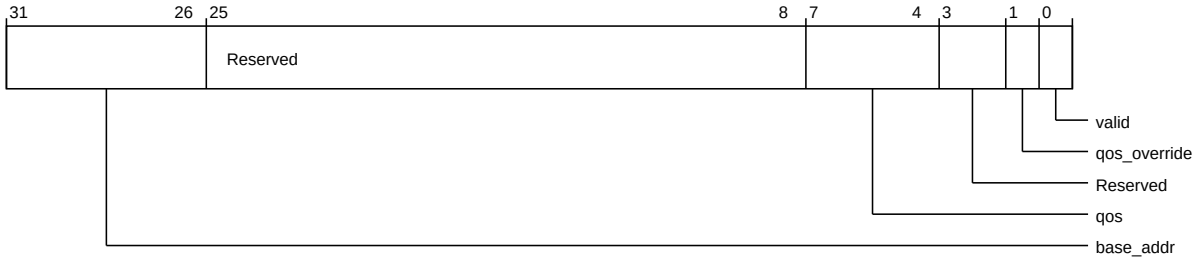
The following table shows the sam_qos_mem_region_reg3 higher register bit assignments.

Table 5-1206: por_rnsam_sam_qos_mem_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1193: por_rnsam_sam_qos_mem_region_reg3 (low)



The following table shows the sam_qos_mem_region_reg3 lower register bit assignments.

Table 5-1207: por_rnsam_sam_qos_mem_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0

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Bits	Field name	Description	Type	Reset
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.96 sam_qos_mem_region_reg4

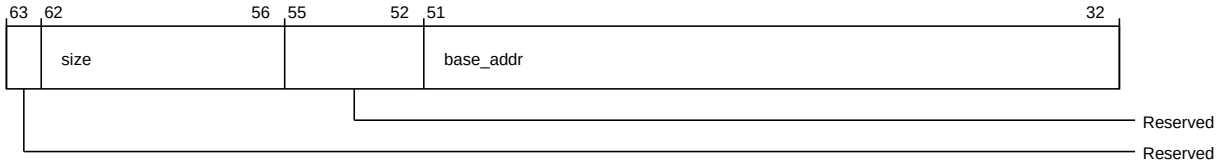
Configures the QoS value for memory region 4

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h12A0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1194: por_rnsam_sam_qos_mem_region_reg4 (high)



The following table shows the sam_qos_mem_region_reg4 higher register bit assignments.

Table 5-1208: por_rnsam_sam_qos_mem_region_reg4 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-

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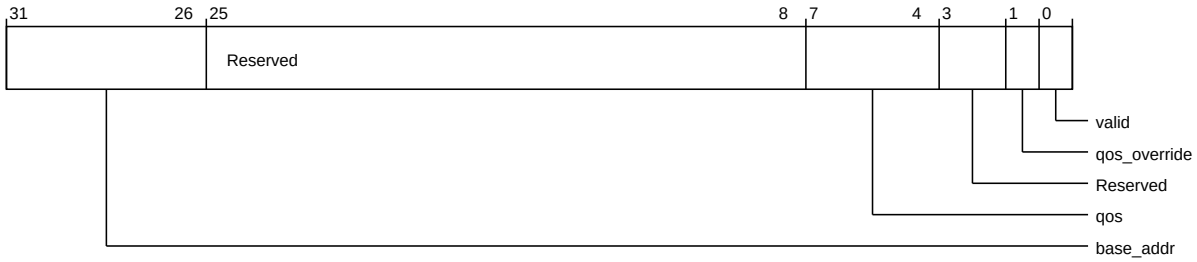
Bits	Field name	Description	Type	Reset
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1195: por_rnsam_sam_qos_mem_region_reg4 (low)



The following table shows the sam_qos_mem_region_reg4 lower register bit assignments.

Table 5-1209: por_rnsam_sam_qos_mem_region_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.97 sam_qos_mem_region_reg5

Configures the QoS value for memory region 5

Its characteristics are:

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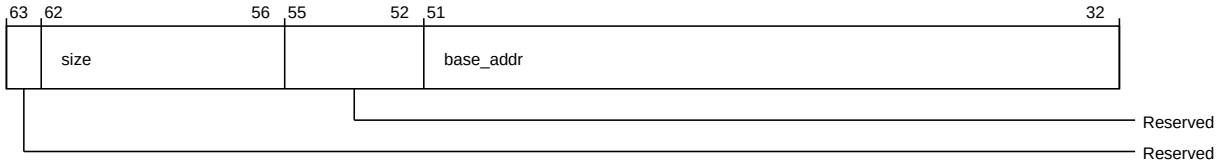
Type RW
Register width (Bits) 64
Address offset 16'h12A8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1196: por_rnsam_sam_qos_mem_region_reg5 (high)



The following table shows the sam_qos_mem_region_reg5 higher register bit assignments.

Table 5-1210: por_rnsam_sam_qos_mem_region_reg5 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

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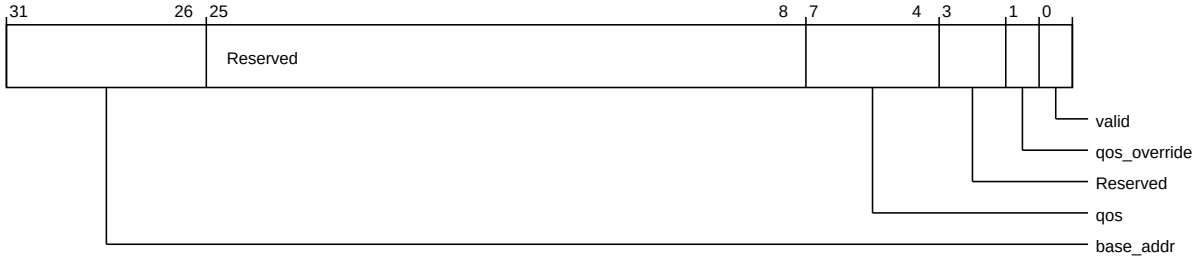
Figure 5-1197: por_rnsam_sam_qos_mem_region_reg5 (low)



The following table shows the sam_qos_mem_region_reg5 lower register bit assignments.

Table 5-1211: por_rnsam_sam_qos_mem_region_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.98 sam_qos_mem_region_reg6

Configures the QoS value for memory region 6

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h12B0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

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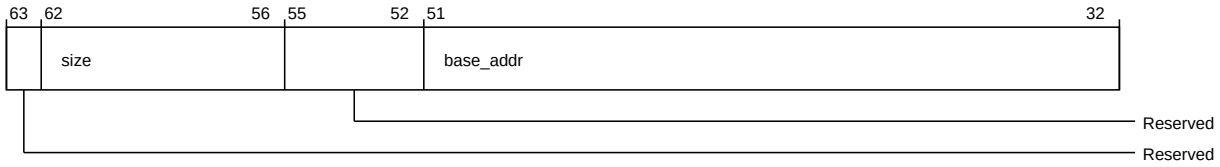
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1198: por_rnsam_sam_qos_mem_region_reg6 (high)



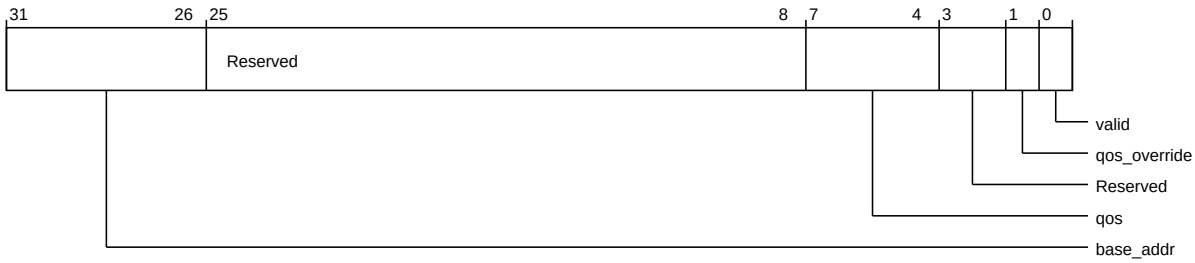
The following table shows the sam_qos_mem_region_reg6 higher register bit assignments.

Table 5-1212: por_rnsam_sam_qos_mem_region_reg6 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1199: por_rnsam_sam_qos_mem_region_reg6 (low)



The following table shows the sam_qos_mem_region_reg6 lower register bit assignments.

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Table 5-1213: por_rnsam_sam_qos_mem_region_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.99 sam_qos_mem_region_reg7

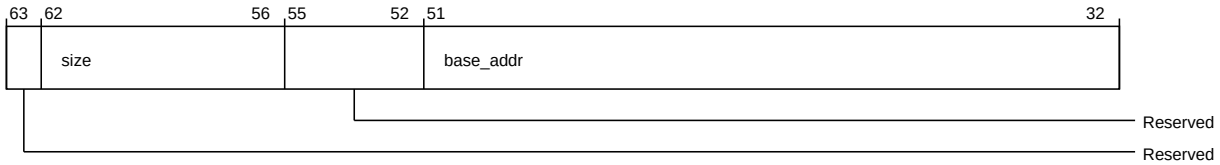
Configures the QoS value for memory region 7

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h12B8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1200: por_rnsam_sam_qos_mem_region_reg7 (high)



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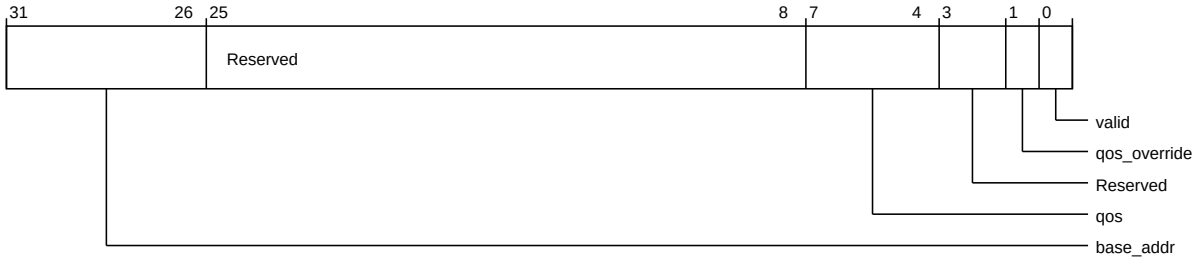
The following table shows the sam_qos_mem_region_reg7 higher register bit assignments.

Table 5-1214: por_rnsam_sam_qos_mem_region_reg7 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:56	size	Memory region size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
55:52	Reserved	Reserved	RO	-
51:32	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000

The following figure shows the lower register bit assignments.

Figure 5-1201: por_rnsam_sam_qos_mem_region_reg7 (low)



The following table shows the sam_qos_mem_region_reg7 lower register bit assignments.

Table 5-1215: por_rnsam_sam_qos_mem_region_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Bits [51:26] of base address of the range CONSTRAINT: Must be an integer multiple of region size	RW	26'b00000000000000000000000000
25:8	Reserved	Reserved	RO	-
7:4	qos	Indicates the QoS value to be used for this region	RW	4'b0000
3:2	Reserved	Reserved	RO	-
1	qos_override	QoS Memory region allow override 1'b0: Do not override the QoS value from the QoS regulator 1'b1: Override the QoS value with the programmed value in regionX_qos	RW	1'b0

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Bits	Field name	Description	Type	Reset
0	valid	QoS Memory region valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

5.3.9.100 sam_generic_regs0

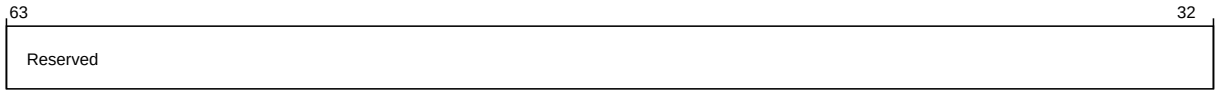
Configuration register for the custom logic

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1600
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_rnsam_secure_register_groups_override.mem_range

The following figure shows the higher register bit assignments.

Figure 5-1202: por_rnsam_sam_generic_regs0 (high)



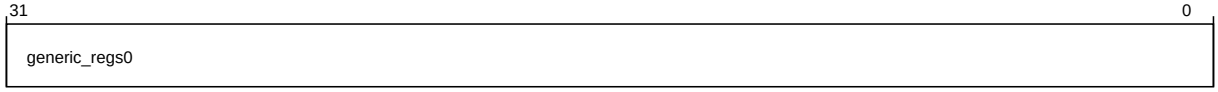
The following table shows the sam_generic_regs0 higher register bit assignments.

Table 5-1216: por_rnsam_sam_generic_regs0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1203: por_rnsam_sam_generic_regs0 (low)



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The following table shows the sam_generic_regs0 lower register bit assignments.

Table 5-1217: por_rnsam_sam_generic_regs0 (low)

Bits	Field name	Description	Type	Reset
31:0	generic_regs0	Configuration register for the custom logic	RW	32'h0

5.3.10 SBSX register descriptions

This section lists the SBSX registers.

5.3.10.1 por_sbsx_node_info

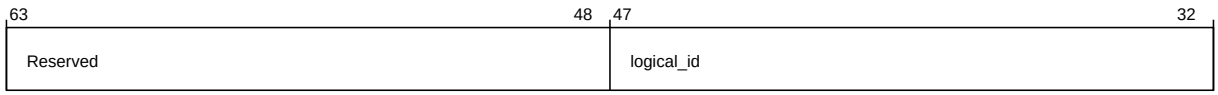
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1204: por_sbsx_por_sbsx_node_info (high)



The following table shows the por_sbsx_node_info higher register bit assignments.

Table 5-1218: por_sbsx_por_sbsx_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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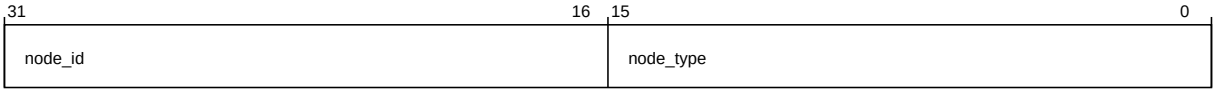
Figure 5-1205: por_sbsx_por_sbsx_node_info (low)



The following table shows the por_sbsx_node_info lower register bit assignments.

Table 5-1219: por_sbsx_por_sbsx_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0007

5.3.10.2 por_sbsx_child_info

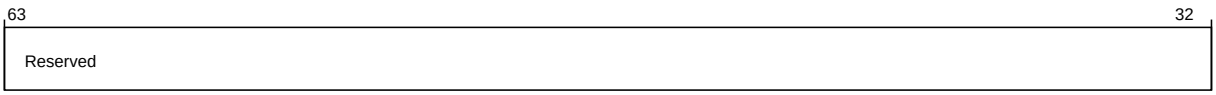
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1206: por_sbsx_por_sbsx_child_info (high)



The following table shows the por_sbsx_child_info higher register bit assignments.

Table 5-1220: por_sbsx_por_sbsx_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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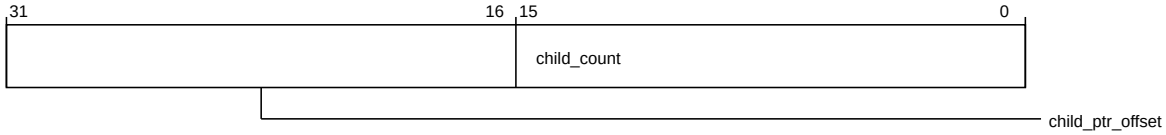
Figure 5-1207: por_sbsx_por_sbsx_child_info (low)



The following table shows the por_sbsx_child_info lower register bit assignments.

Table 5-1221: por_sbsx_por_sbsx_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.10.3 por_sbsx_secure_register_groups_override

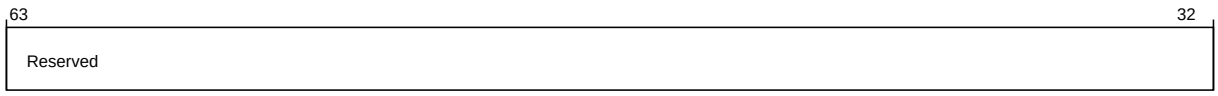
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1208: por_sbsx_por_sbsx_secure_register_groups_override (high)



The following table shows the por_sbsx_secure_register_groups_override higher register bit assignments.

Table 5-1222: por_sbsx_por_sbsx_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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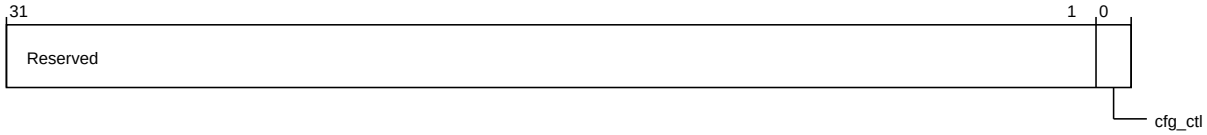
Figure 5-1209: por_sbsx_por_sbsx_secure_register_groups_override (low)



The following table shows the por_sbsx_secure_register_groups_override lower register bit assignments.

Table 5-1223: por_sbsx_por_sbsx_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_sbsx_cfg_ctl)	RW	1'b0

5.3.10.4 por_sbsx_unit_info

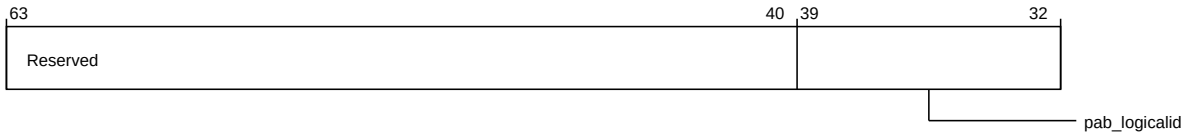
Provides component identification information for SBSX.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1210: por_sbsx_por_sbsx_unit_info (high)



The following table shows the por_sbsx_unit_info higher register bit assignments.

Table 5-1224: por_sbsx_por_sbsx_unit_info (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-

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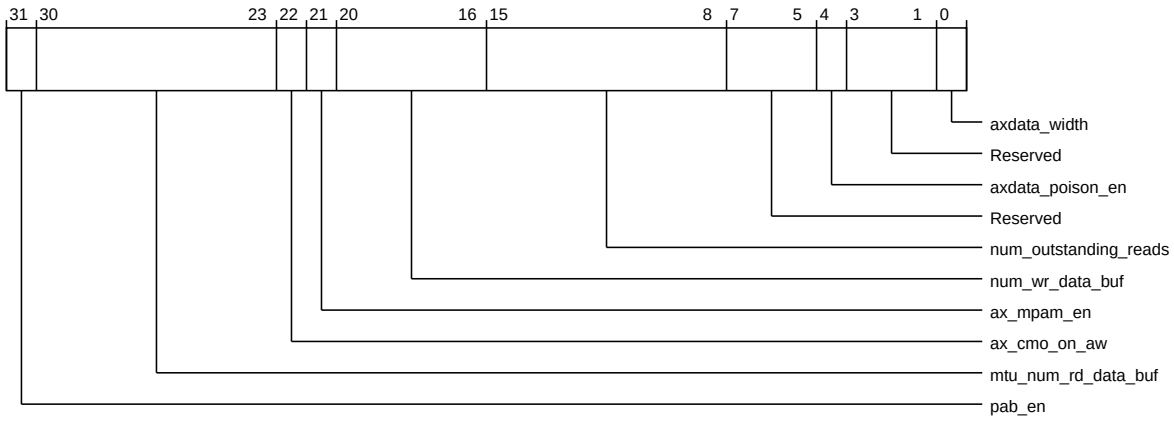
Bits	Field name	Description	Type	Reset
39:32	pab_logicalid	PUB AUB bridge Logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-1211: por_sbsx_por_sbsx_unit_info (low)



The following table shows the por_sbsx_unit_info lower register bit assignments.

Table 5-1225: por_sbsx_por_sbsx_unit_info (low)

Bits	Field name	Description	Type	Reset
31	pab_en	PUB AUB bridge enable 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
30:23	mtu_num_rd_data_buf	Number of mtu read data buffers in SBSX	RO	Configuration dependent
22	ax_cmo_on_aw	Write Channel CMOs enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
21	ax_mpam_en	MPAM enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
20:16	num_wr_data_buf	Number of write data buffers in SBSX	RO	Configuration dependent
15:8	num_outstanding_reads	Maximum number of outstanding AXI read requests from SBSX	RO	Configuration dependent
7:5	Reserved	Reserved	RO	-
4	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
3:1	Reserved	Reserved	RO	-
0	axdata_width	Data width on ACE-Lite/AXI4 interface 1'b0: 128 bits 1'b1: 256 bits	RO	Configuration dependent

5.3.10.5 por_sbsx_cfg_ctl

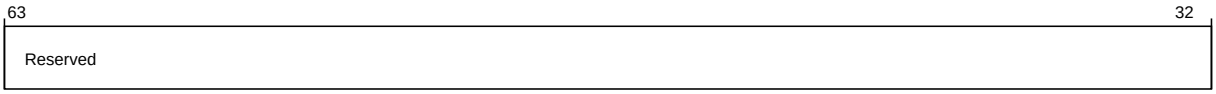
Functions as the configuration control register for SBSX bridge.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b1111111
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_sbsx_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

Figure 5-1212: por_sbsx_por_sbsx_cfg_ctl (high)



The following table shows the por_sbsx_cfg_ctl higher register bit assignments.

Table 5-1226: por_sbsx_por_sbsx_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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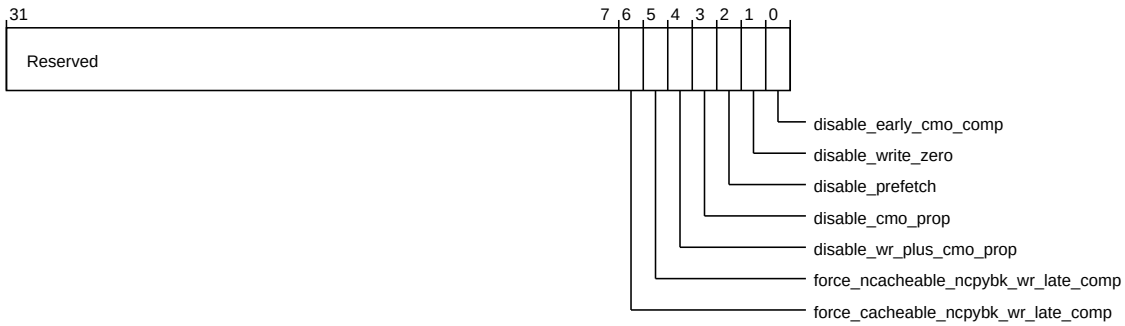
Figure 5-1213: por_sbsx_por_sbsx_cfg_ctl (low)



The following table shows the por_sbsx_cfg_ctl lower register bit assignments.

Table 5-1227: por_sbsx_por_sbsx_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6	force_cacheable_ncpybk_wr_late_comp	Late Comp for Cacheable Non-CopyBack Writes. Overrides EWA **Note:** The value of this bit must not be changed.	RW	1'b1
5	force_ncacheable_ncpybk_wr_late_comp	Late Comp for Non-cacheable Non-CopyBack Writes. Overrides EWA **Note:** The value of this bit must not be changed.	RW	1'b1
4	disable_wr_plus_cmo_prop	Disables Write_plus_CMO propagation on ACE.	RW	1'b1
3	disable_cmo_prop	Disables CMO propagation on ACE. **Note:** The value of this bit must not be changed.	RW	1'b1
2	disable_prefetch	Disables Prefetches on AXI.	RW	1'b1
1	disable_write_zero	Disables WriteZero Op on AXI.	RW	1'b1
0	disable_early_cmo_comp	Disables Early Comp for CMOs in SBSX to HNF.	RW	1'b1

5.3.10.6 por_sbsx_aux_ctl

Functions as the auxiliary control register for the SBSX bridge.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset 64'b0

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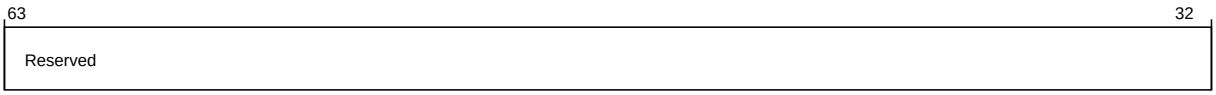
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1214: por_sbsx_por_sbsx_aux_ctl (high)



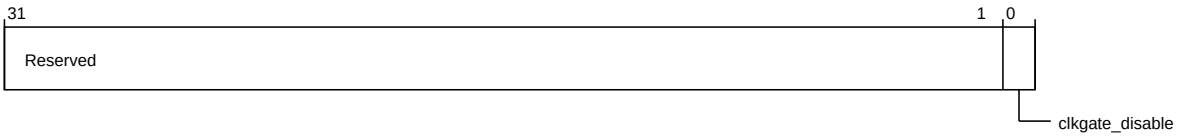
The following table shows the por_sbsx_aux_ctl higher register bit assignments.

Table 5-1228: por_sbsx_por_sbsx_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1215: por_sbsx_por_sbsx_aux_ctl (low)



The following table shows the por_sbsx_aux_ctl lower register bit assignments.

Table 5-1229: por_sbsx_por_sbsx_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables internal clock gating in SBSX bridge	RW	1'b0

5.3.10.7 por_sbsx_cbusy_limit_ctl

Cbusy threshold limits for Request Tracker entries.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA18
Register reset Configuration dependent

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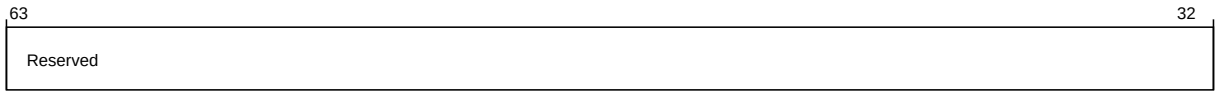
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1216: por_sbsx_por_sbsx_cbusy_limit_ctl (high)



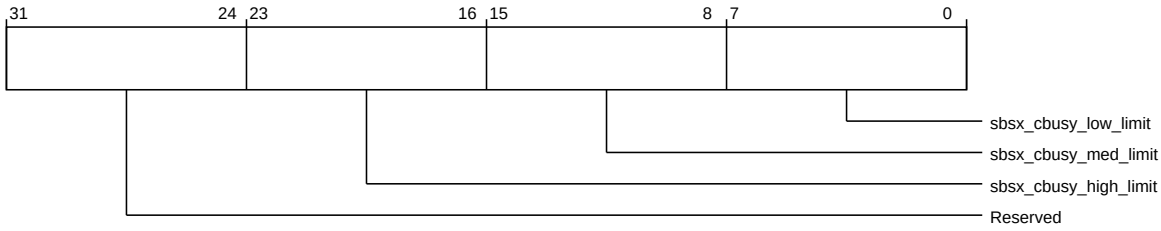
The following table shows the por_sbsx_cbusy_limit_ctl higher register bit assignments.

Table 5-1230: por_sbsx_por_sbsx_cbusy_limit_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1217: por_sbsx_por_sbsx_cbusy_limit_ctl (low)



The following table shows the por_sbsx_cbusy_limit_ctl lower register bit assignments.

Table 5-1231: por_sbsx_por_sbsx_cbusy_limit_ctl (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	sbsx_cbusy_high_limit	ReqTracker limit for CBusy High	RW	Configuration dependent
15:8	sbsx_cbusy_med_limit	ReqTracker limit for CBusy Med	RW	Configuration dependent
7:0	sbsx_cbusy_low_limit	ReqTracker limit for CBusy Low	RW	Configuration dependent

5.3.10.8 por_sbsx_errfr

Functions as the error feature register.

Its characteristics are:

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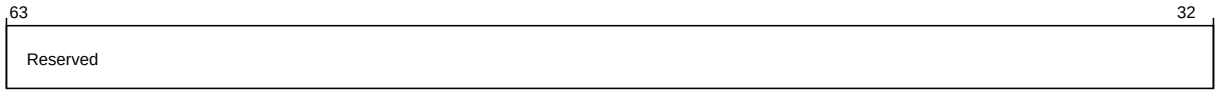
Type RO
Register width (Bits) 64
Address offset 16'h3000
Register reset 64'b0000010100001
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1218: por_sbsx_por_sbsx_errfr (high)



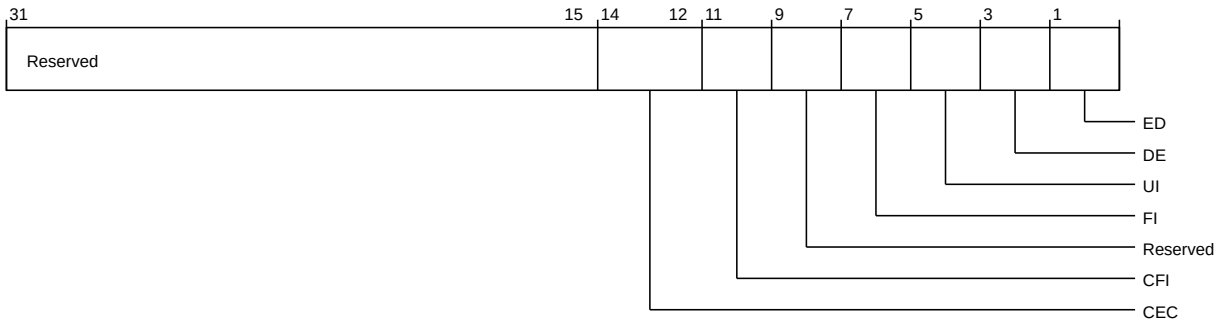
The following table shows the por_sbsx_errfr higher register bit assignments.

Table 5-1232: por_sbsx_por_sbsx_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1219: por_sbsx_por_sbsx_errfr (low)



The following table shows the por_sbsx_errfr lower register bit assignments.

Table 5-1233: por_sbsx_por_sbsx_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000

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Bits	Field name	Description	Type	Reset
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

5.3.10.9 por_sbsx_errctlr

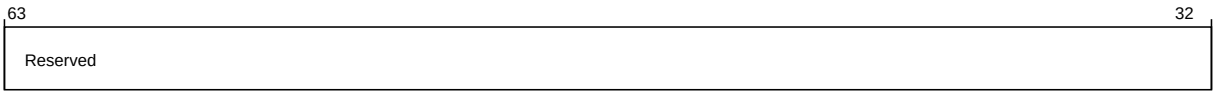
Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1220: por_sbsx_por_sbsx_errctlr (high)



The following table shows the por_sbsx_errctlr higher register bit assignments.

Table 5-1234: por_sbsx_por_sbsx_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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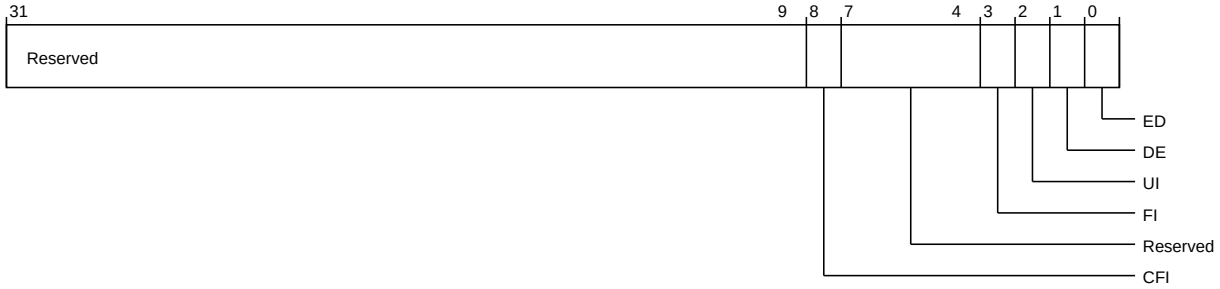
Figure 5-1221: por_sbsx_por_sbsx_errctlr (low)



The following table shows the por_sbsx_errctlr lower register bit assignments.

Table 5-1235: por_sbsx_por_sbsx_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_sbsx_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_sbsx_errfr.ED	RW	1'b0

5.3.10.10 por_sbsx_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

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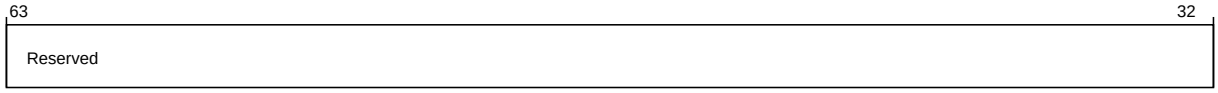
Figure 5-1222: por_sbsx_por_sbsx_errstatus (high)



The following table shows the por_sbsx_errstatus higher register bit assignments.

Table 5-1236: por_sbsx_por_sbsx_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1223: por_sbsx_por_sbsx_errstatus (low)



The following table shows the por_sbsx_errstatus lower register bit assignments.

Table 5-1237: por_sbsx_por_sbsx_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_sbsx_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0

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Bits	Field name	Description	Type	Reset
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_sbsx_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.10.11 por_sbsx_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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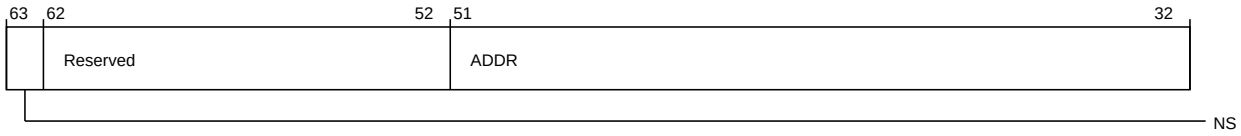
The following figure shows the higher register bit assignments.

Figure 5-1224: por_sbsx_por_sbsx_erraddr (high)



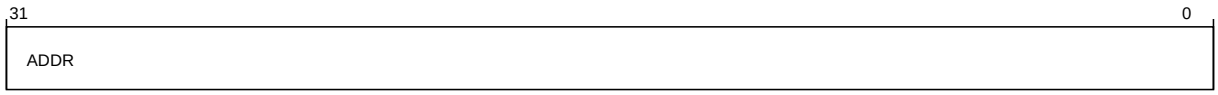
The following table shows the por_sbsx_erraddr higher register bit assignments.

Table 5-1238: por_sbsx_por_sbsx_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_sbsx_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-1225: por_sbsx_por_sbsx_erraddr (low)



The following table shows the por_sbsx_erraddr lower register bit assignments.

Table 5-1239: por_sbsx_por_sbsx_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

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5.3.10.12 por_sbsx_errmisc

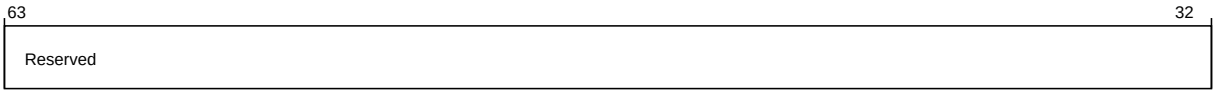
Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1226: por_sbsx_por_sbsx_errmisc (high)



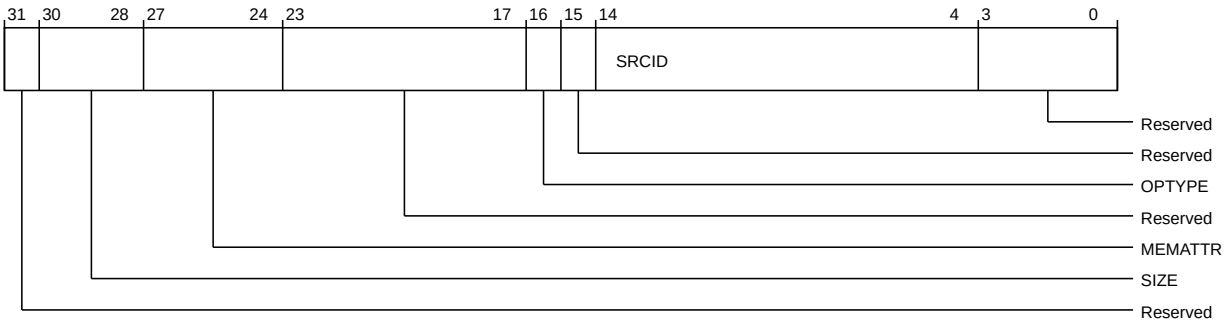
The following table shows the por_sbsx_errmisc higher register bit assignments.

Table 5-1240: por_sbsx_por_sbsx_errmisc (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1227: por_sbsx_por_sbsx_errmisc (low)



The following table shows the por_sbsx_errmisc lower register bit assignments.

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Table 5-1241: por_sbsx_por_sbsx_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

5.3.10.13 por_sbsx_errfr_NS

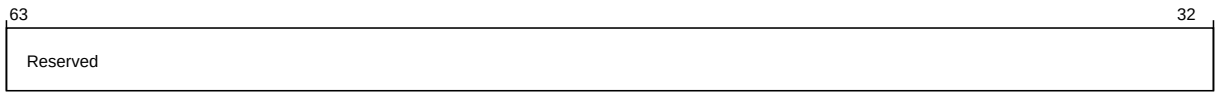
Functions as the Non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b0000010100001
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1228: por_sbsx_por_sbsx_errfr_ns (high)



The following table shows the por_sbsx_errfr_NS higher register bit assignments.

Table 5-1242: por_sbsx_por_sbsx_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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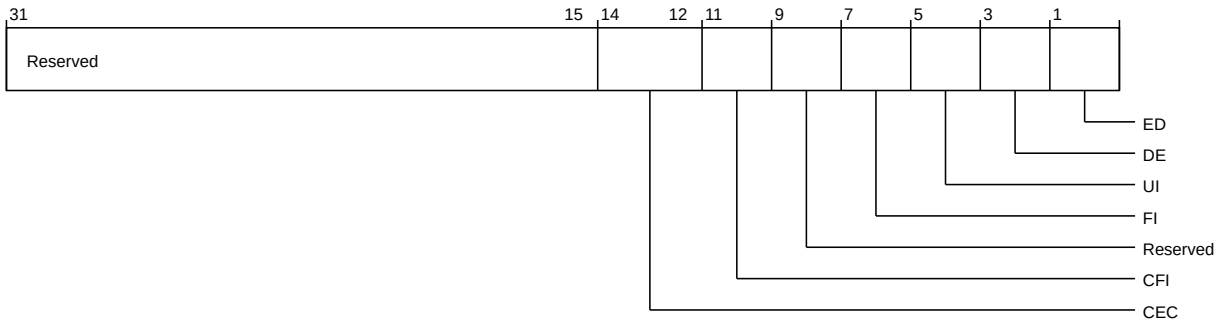
Figure 5-1229: por_sbsx_por_sbsx_errfr_ns (low)



The following table shows the por_sbsx_errfr_NS lower register bit assignments.

Table 5-1243: por_sbsx_por_sbsx_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

5.3.10.14 por_sbsx_errctlr_NS

Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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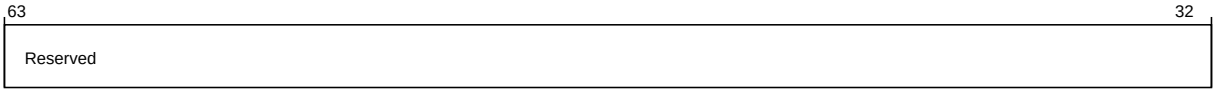
Figure 5-1230: por_sbsx_por_sbsx_errctlr_ns (high)



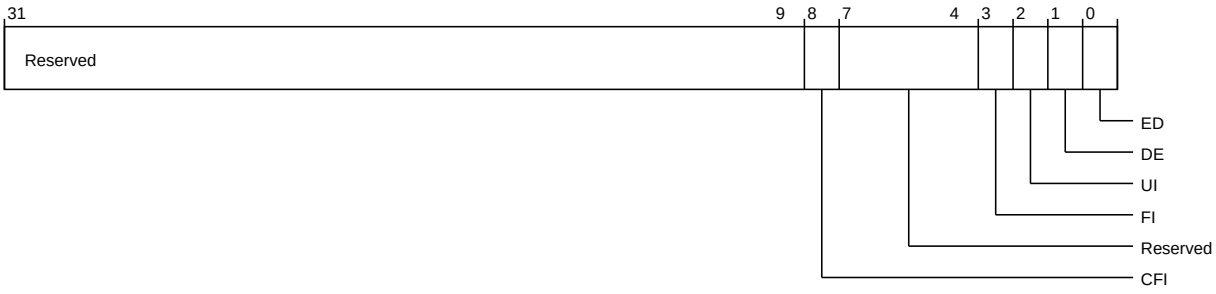
The following table shows the por_sbsx_errctlr_NS higher register bit assignments.

Table 5-1244: por_sbsx_por_sbsx_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1231: por_sbsx_por_sbsx_errctlr_ns (low)



The following table shows the por_sbsx_errctlr_NS lower register bit assignments.

Table 5-1245: por_sbsx_por_sbsx_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_sbsx_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_sbsx_errfr_NS.ED	RW	1'b0

5.3.10.15 por_sbsx_errstatus_NS

Functions as the Non-secure error status register.

Its characteristics are:

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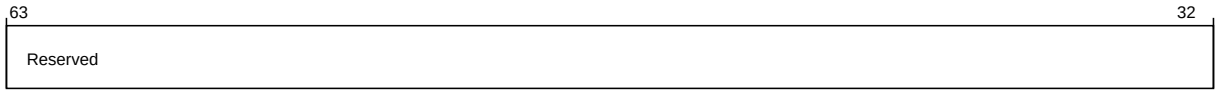
Type W1C
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1232: por_sbsx_por_sbsx_errstatus_ns (high)



The following table shows the por_sbsx_errstatus_NS higher register bit assignments.

Table 5-1246: por_sbsx_por_sbsx_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1233: por_sbsx_por_sbsx_errstatus_ns (low)



The following table shows the por_sbsx_errstatus_NS lower register bit assignments.

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Table 5-1247: por_sbsx_por_sbsx_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_sbsx_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_sbsx_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

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5.3.10.16 por_sbsx_erraddr_NS

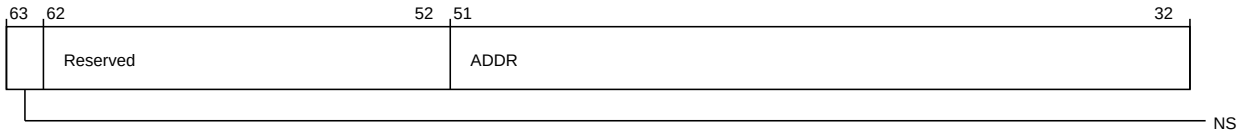
Contains the Non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1234: por_sbsx_por_sbsx_erraddr_ns (high)



The following table shows the por_sbsx_erraddr_NS higher register bit assignments.

Table 5-1248: por_sbsx_por_sbsx_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_sbsx_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address	RW	52'b0

The following figure shows the lower register bit assignments.

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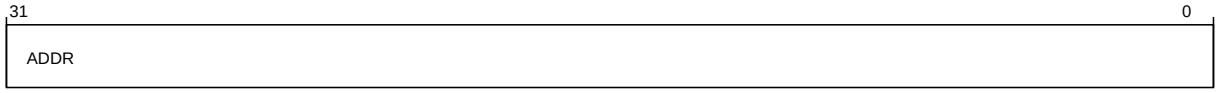
Figure 5-1235: por_sbsx_por_sbsx_erraddr_ns (low)



The following table shows the por_sbsx_erraddr_NS lower register bit assignments.

Table 5-1249: por_sbsx_por_sbsx_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	52'b0

5.3.10.17 por_sbsx_errmisc_NS

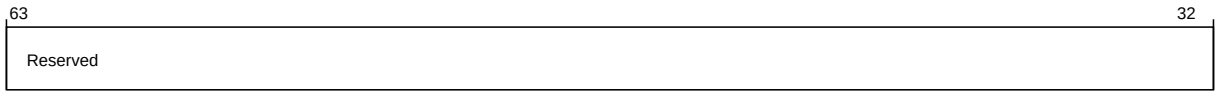
Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1236: por_sbsx_por_sbsx_errmisc_ns (high)



The following table shows the por_sbsx_errmisc_NS higher register bit assignments.

Table 5-1250: por_sbsx_por_sbsx_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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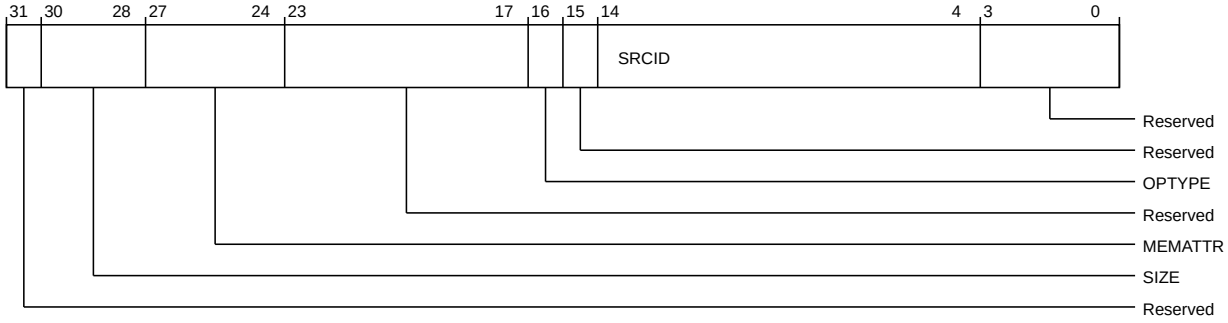
Figure 5-1237: por_sbsx_por_sbsx_errmisc_ns (low)



The following table shows the por_sbsx_errmisc_NS lower register bit assignments.

Table 5-1251: por_sbsx_por_sbsx_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

5.3.10.18 por_sbsx_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

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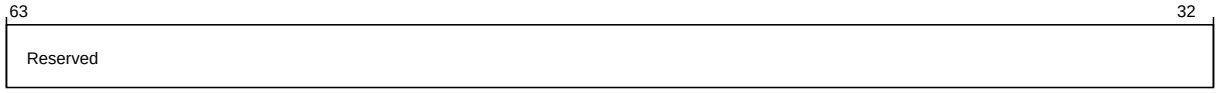
Figure 5-1238: por_sbsx_por_sbsx_pmu_event_sel (high)



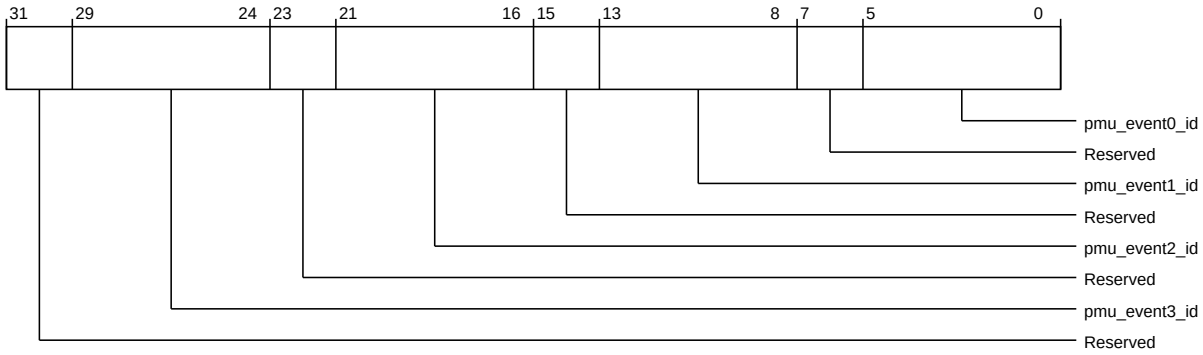
The following table shows the por_sbsx_pmu_event_sel higher register bit assignments.

Table 5-1252: por_sbsx_por_sbsx_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1239: por_sbsx_por_sbsx_pmu_event_sel (low)



The following table shows the por_sbsx_pmu_event_sel lower register bit assignments.

Table 5-1253: por_sbsx_por_sbsx_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	SBSX PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	SBSX PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	SBSX PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	SBSX PMU Event 0 select 6'h00: No event 6'h01: Read request 6'h02: Write request 6'h03: CMO request 6'h04: RETRYACK TXRSP flit sent 6'h05: TXDAT flit seen 6'h06: TXRSP flit seen 6'h11: Read request tracker occupancy count overflow 6'h12: Write request tracker occupancy count overflow 6'h13: CMO request tracker occupancy count overflow 6'h14: WDB occupancy count overflow 6'h15: Read AXI pending tracker occupancy count overflow 6'h16: CMO AXI pending tracker occupancy count overflow 6'h17: RDB occupancy count overflow. (Only when MTU is enabled) 6'h21: ARVALID set without ARREADY 6'h22: AWVALID set without AWREADY 6'h23: WVALID set without WREADY 6'h24: TXDAT stall (TXDAT valid but no link credit available) 6'h25: TXRSP stall (TXRSP valid but no link credit available) NOTE: All other encodings are reserved.	RW	6'b0

5.3.11 HN-F MPAM_NS register descriptions

This section lists the HN-F MPAM_NS registers.

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5.3.11.1 por_hnf_mpam_ns_node_info

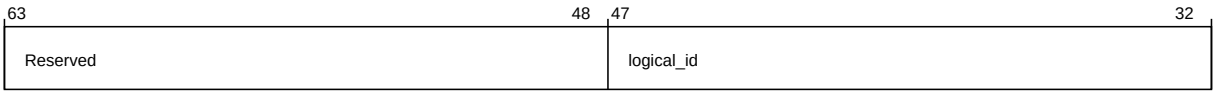
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1240: por_hnf_mpam_ns_por_hnf_mpam_ns_node_info (high)



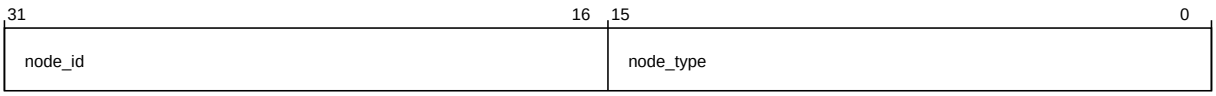
The following table shows the por_hnf_mpam_ns_node_info higher register bit assignments.

Table 5-1254: por_hnf_mpam_ns_por_hnf_mpam_ns_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-1241: por_hnf_mpam_ns_por_hnf_mpam_ns_node_info (low)



The following table shows the por_hnf_mpam_ns_node_info lower register bit assignments.

Table 5-1255: por_hnf_mpam_ns_por_hnf_mpam_ns_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent

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Bits	Field name	Description	Type	Reset
15:0	node_type	CI-700 node type identifier	RO	16'h0009

5.3.11.2 por_hnf_mpam_ns_child_info

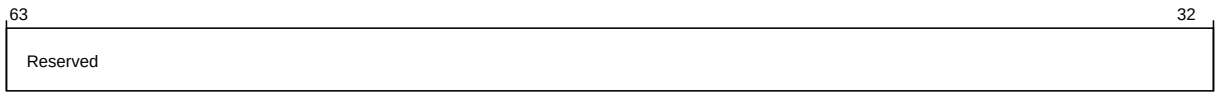
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1242: por_hnf_mpam_ns_por_hnf_mpam_ns_child_info (high)



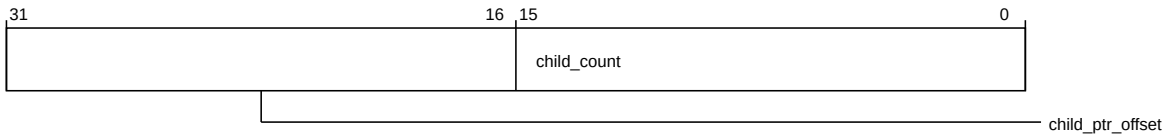
The following table shows the por_hnf_mpam_ns_child_info higher register bit assignments.

Table 5-1256: por_hnf_mpam_ns_por_hnf_mpam_ns_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1243: por_hnf_mpam_ns_por_hnf_mpam_ns_child_info (low)



The following table shows the por_hnf_mpam_ns_child_info lower register bit assignments.

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Table 5-1257: por_hnf_mpam_ns_por_hnf_mpam_ns_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.11.3 por_hnf_mpam_idr

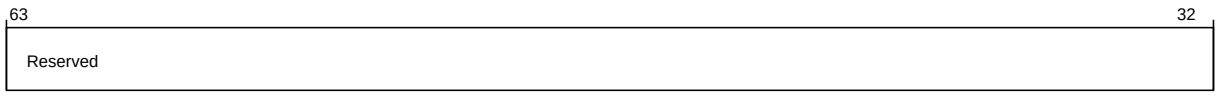
MPAM features ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1000
Register reset Configuration dependent
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1244: por_hnf_mpam_ns_por_hnf_mpam_idr (high)



The following table shows the por_hnf_mpam_idr higher register bit assignments.

Table 5-1258: por_hnf_mpam_ns_por_hnf_mpam_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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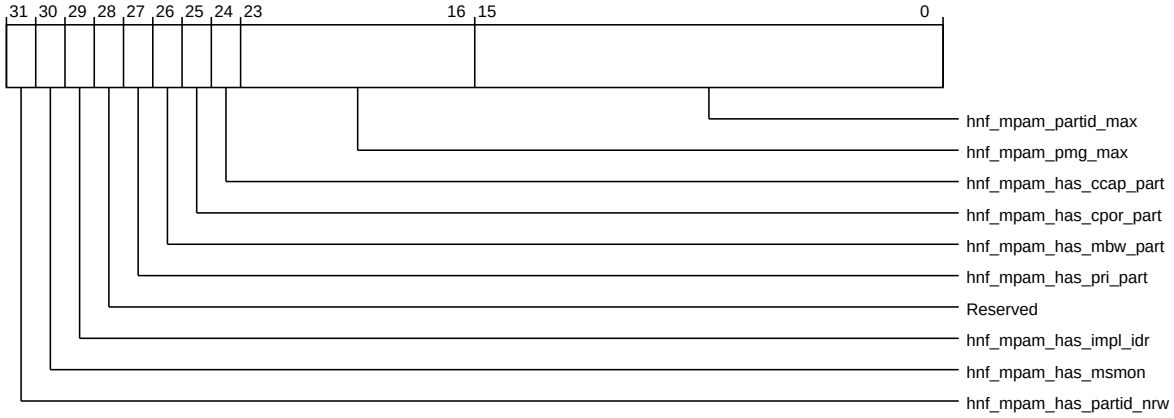
Figure 5-1245: por_hnf_mpam_ns_por_hnf_mpam_idr (low)



The following table shows the por_hnf_mpam_idr lower register bit assignments.

Table 5-1259: por_hnf_mpam_ns_por_hnf_mpam_idr (low)

Bits	Field name	Description	Type	Reset
31	hnf_mpam_has_partid_nrw	0: HN-F does not support MPAM PARTID Narrowing 1: HN-F supports MPAM PARTID Narrowing	RO	1'b0
30	hnf_mpam_has_msmon	0: MPAM performance monitoring is not supported 1: MPAM performance monitoring is supported	RO	1'b1
29	hnf_mpam_has_impl_idr	0: MPAM implementation specific partitioning features not supported 1: MPAM implementation specific partitioning features supported	RO	1'b0
28	Reserved	Reserved	RO	-
27	hnf_mpam_has_pri_part	0: MPAM priority partitioning is not supported 1: MPAM priority partitioning is supported	RO	1'b0
26	hnf_mpam_has_mbw_part	0: MPAM memory bandwidth partitioning is not supported 1: MPAM memory bandwidth partitioning is supported	RO	1'b0
25	hnf_mpam_has_cpor_part	0: MPAM cache portion partitioning is not supported 1: MPAM cache portion partitioning is supported	RO	1'b1
24	hnf_mpam_has_ccap_part	0: MPAM cache maximum capacity partitioning is not supported 1: MPAM cache maximum capacity partitioning is supported	RO	1'b1
23:16	hnf_mpam_pmg_max	Maximum value of Non-secure PMG supported by this HN-F	RO	Configuration dependent
15:0	hnf_mpam_partid_max	Maximum value of Non-secure PARTID supported by this HN-F	RO	Configuration dependent

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5.3.11.4 por_hnf_mpam_iidr

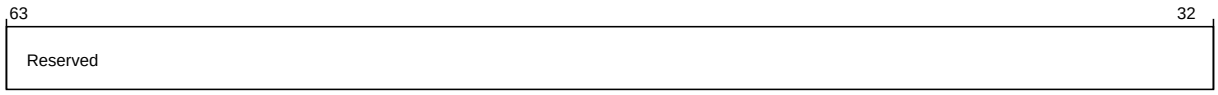
MPAM Implementation ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1018
Register reset 64'b0000000000000000000000000100111011
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1246: por_hnf_mpam_ns_por_hnf_mpam_iidr (high)



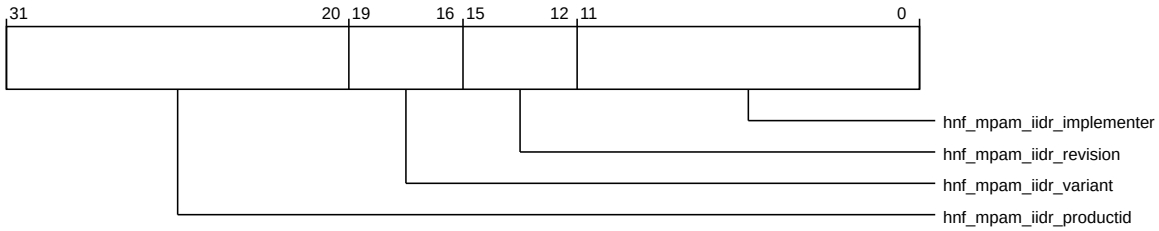
The following table shows the por_hnf_mpam_iidr higher register bit assignments.

Table 5-1260: por_hnf_mpam_ns_por_hnf_mpam_iidr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1247: por_hnf_mpam_ns_por_hnf_mpam_iidr (low)



The following table shows the por_hnf_mpam_iidr lower register bit assignments.

Table 5-1261: por_hnf_mpam_ns_por_hnf_mpam_iidr (low)

Bits	Field name	Description	Type	Reset
31:20	hnf_mpam_iidr_productid	Implementation defined value identifying MPAM memory system component	RO	12'h000
19:16	hnf_mpam_iidr_variant	Implementation defined value identifying major revision of the product	RO	4'b0000

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Bits	Field name	Description	Type	Reset
15:12	hnf_mpam_iidr_revision	Implementation defined value identifying minor revision of the product	RO	4'b0000
11:0	hnf_mpam_iidr_implementer	Implementation defined value identifying company that implemented MPAM memory system component	RO	12'h43B

5.3.11.5 por_hnf_mpam_aidr

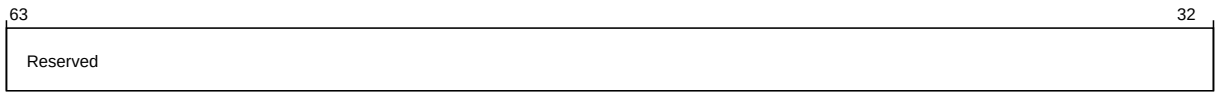
MPAM architecture ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1020
Register reset 64'b00010000
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1248: por_hnf_mpam_ns_por_hnf_mpam_aidr (high)



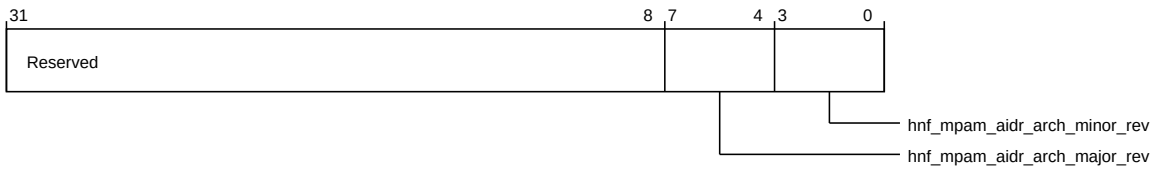
The following table shows the por_hnf_mpam_aidr higher register bit assignments.

Table 5-1262: por_hnf_mpam_ns_por_hnf_mpam_aidr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1249: por_hnf_mpam_ns_por_hnf_mpam_aidr (low)



The following table shows the por_hnf_mpam_aidr lower register bit assignments.

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Table 5-1263: por_hnf_mpam_ns_por_hnf_mpam_aidr (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:4	hnf_mpam_aidr_arch_major_rev	Major revision of the MPAM architecture that this memory system component implements	RO	4'b0001
3:0	hnf_mpam_aidr_arch_minor_rev	Minor revision of the MPAM architecture that this memory system component implements	RO	4'b0000

5.3.11.6 por_hnf_mpam_impl_idr

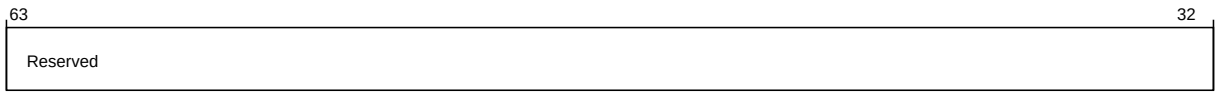
MPAM Implementation defined partitioning feature ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1028
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1250: por_hnf_mpam_ns_por_hnf_mpam_impl_idr (high)



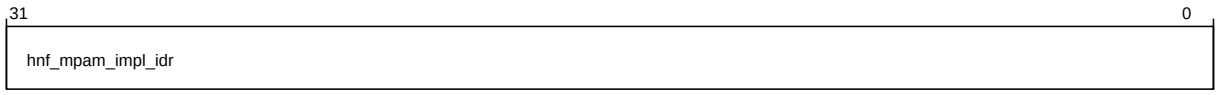
The following table shows the por_hnf_mpam_impl_idr higher register bit assignments.

Table 5-1264: por_hnf_mpam_ns_por_hnf_mpam_impl_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1251: por_hnf_mpam_ns_por_hnf_mpam_impl_idr (low)



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The following table shows the por_hnf_mpam_impl_idr lower register bit assignments.

Table 5-1265: por_hnf_mpam_ns_por_hnf_mpam_impl_idr (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_mpam_impl_idr	Implementation defined partitioning features.	RO	32'h00000000

5.3.11.7 por_hnf_mpam_cpor_idr

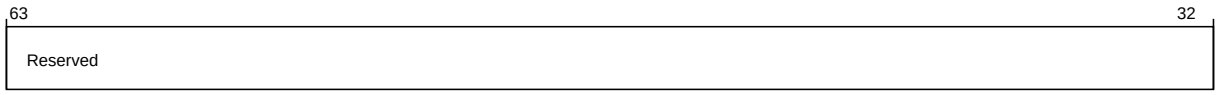
MPAM cache portion partitioning ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1030
Register reset Configuration dependent
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1252: por_hnf_mpam_ns_por_hnf_mpam_cpor_idr (high)



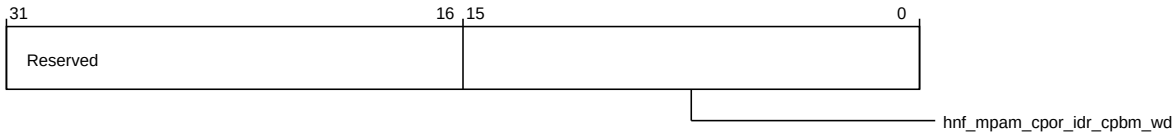
The following table shows the por_hnf_mpam_cpor_idr higher register bit assignments.

Table 5-1266: por_hnf_mpam_ns_por_hnf_mpam_cpor_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1253: por_hnf_mpam_ns_por_hnf_mpam_cpor_idr (low)



The following table shows the por_hnf_mpam_cpor_idr lower register bit assignments.

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Table 5-1267: por_hnf_mpam_ns_por_hnf_mpam_cpor_idr (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_mpam_cpor_idr_cpbm_wd	Number of bits in the cache portion partitioning bit map of this device.	RO	Configuration dependent

5.3.11.8 por_hnf_mpam_ccap_idr

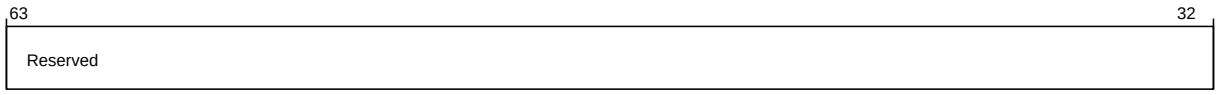
MPAM cache capacity partitioning ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1038
Register reset Configuration dependent
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1254: por_hnf_mpam_ns_por_hnf_mpam_ccap_idr (high)



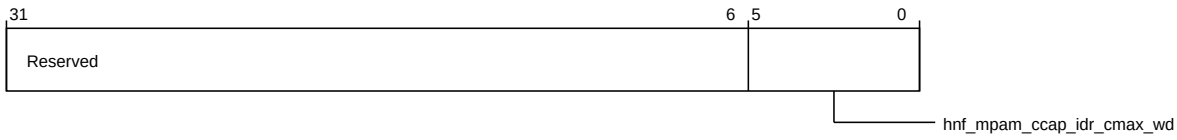
The following table shows the por_hnf_mpam_ccap_idr higher register bit assignments.

Table 5-1268: por_hnf_mpam_ns_por_hnf_mpam_ccap_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1255: por_hnf_mpam_ns_por_hnf_mpam_ccap_idr (low)



The following table shows the por_hnf_mpam_ccap_idr lower register bit assignments.

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Table 5-1269: por_hnf_mpam_ns_por_hnf_mpam_ccap_idr (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	hnf_mpam_ccap_idr_cmax_wd	Number of fractional bits implemented in the cache capacity partitioning.	RO	Configuration dependent

5.3.11.9 por_hnf_mpam_mbw_idr

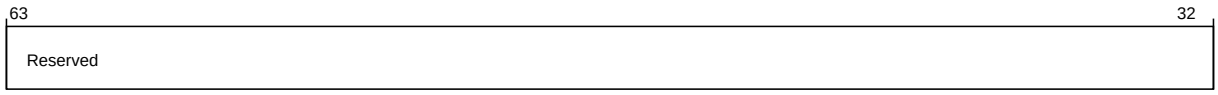
MPAM Memory Bandwidth partitioning ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1040
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1256: por_hnf_mpam_ns_por_hnf_mpam_mbw_idr (high)



The following table shows the por_hnf_mpam_mbw_idr higher register bit assignments.

Table 5-1270: por_hnf_mpam_ns_por_hnf_mpam_mbw_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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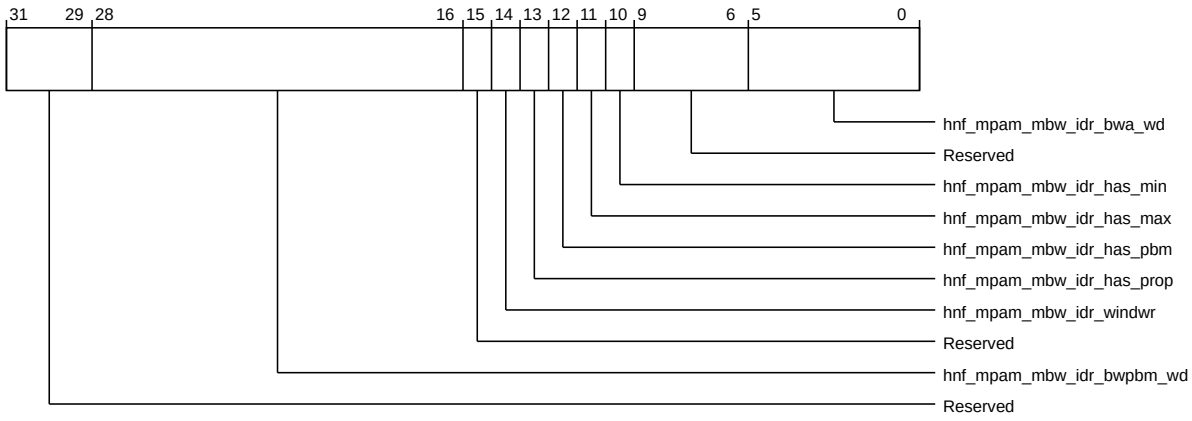
Figure 5-1257: por_hnf_mpam_ns_por_hnf_mpam_mbw_idr (low)



The following table shows the por_hnf_mpam_mbw_idr lower register bit assignments.

Table 5-1271: por_hnf_mpam_ns_por_hnf_mpam_mbw_idr (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:16	hnf_mpam_mbw_idr_bwpbm_wd	Number of bits indication portions in MPAMCFG_MBW_PBM register.	RO	13'h0
15	Reserved	Reserved	RO	-
14	hnf_mpam_mbw_idr_windwr	0: The bandwidth accounting period should be read from MPAMCFG_MBW_WINDWR register, which might be fixed. 1: The bandwidth accounting width is readable and writable per partition in MPAMCFG_MBW_WINDWR register.	RO	1'h0
13	hnf_mpam_mbw_idr_has_prop	0: There is no memory bandwidth proportional stride control and no MPAMCFG_MBW_PROP register 1: MPAMCFG_MBW_PROP register exists and memory bandwidth proportional stride memory bandwidth allocation scheme is supported.	RO	1'h0
12	hnf_mpam_mbw_idr_has_pbm	0: There is no memory bandwidth portion control and no MPAMCFG_MBW_PBM register 1: MPAMCFG_MBW_PBM register exists and memory bandwidth portion allocation scheme is supported.	RO	1'h0
11	hnf_mpam_mbw_idr_has_max	0: There is no maximum memory bandwidth control and no MPAMCFG_MBW_MAX register 1: MPAMCFG_MBW_MAX register exists and maximum memory bandwidth allocation scheme is supported.	RO	1'h0
10	hnf_mpam_mbw_idr_has_min	0: There is no minimum memory bandwidth control and no MPAMCFG_MBW_MIN register 1: MPAMCFG_MBW_MIN register exists and minimum memory bandwidth allocation scheme is supported.	RO	1'h0
9:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	hnf_mpam_mbw_idr_bwa_wd	Number of implemented bits in bandwidth allocation fields: MIN, MAX, and STRIDE. Value must be between 1 to 16	RO	4'b0000

5.3.11.10 por_hnf_mpam_pri_idr

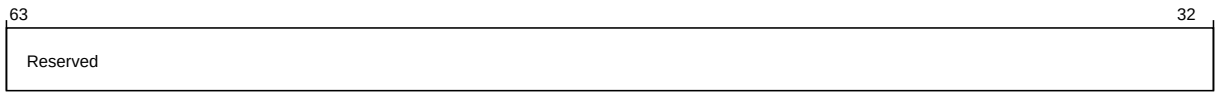
MPAM Priority partitioning ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1048
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1258: por_hnf_mpam_ns_por_hnf_mpam_pri_idr (high)



The following table shows the por_hnf_mpam_pri_idr higher register bit assignments.

Table 5-1272: por_hnf_mpam_ns_por_hnf_mpam_pri_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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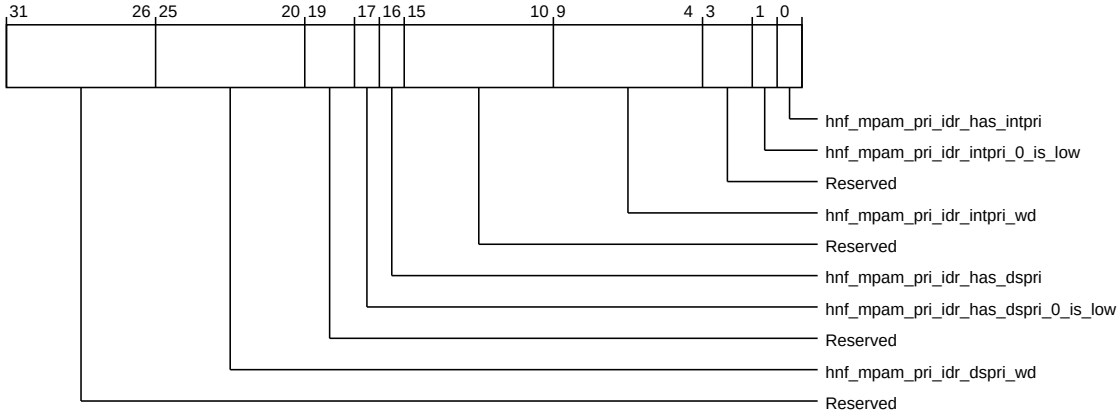
Figure 5-1259: por_hnf_mpam_ns_por_hnf_mpam_pri_idr (low)



The following table shows the por_hnf_mpam_pri_idr lower register bit assignments.

Table 5-1273: por_hnf_mpam_ns_por_hnf_mpam_pri_idr (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:20	hnf_mpam_pri_idr_dspri_wd	Number of bits in downstream priority field (DSPRI) in MPAMCFG_PRI.	RO	6'h0
19:18	Reserved	Reserved	RO	-
17	hnf_mpam_pri_idr_has_dspri_0_is_low	0: In the DSPRI field, a value of 0 means highest priority. 1: In the DSPRI field, a value of 0 means lowest priority.	RO	1'h0
16	hnf_mpam_pri_idr_has_dspri	0: This memory system component supports priority, but doesn't have a downstream priority (DSPRI) field in MPAMCFG_PRI. 1: This memory system component supports downstream priority and has an DSPRI field.	RO	1'h0
15:10	Reserved	Reserved	RO	-
9:4	hnf_mpam_pri_idr_intpri_wd	Number of bits in the internal priority field (INTPRI) in MPAMCFG_PRI.	RO	6'h0
3:2	Reserved	Reserved	RO	-
1	hnf_mpam_pri_idr_intpri_0_is_low	0: In the INTPRI field, a value of 0 means highest priority. 1: In the INTPRI field, a value of 0 means lowest priority.	RO	1'h0
0	hnf_mpam_pri_idr_has_intpri	0: This memory system component supports priority, but doesn't have an internal priority field in MPAMCFG_PRI. 1: This memory system component supports internal priority and has an INTPRI field.	RO	1'h0

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5.3.11.11 por_hnf_mpam_partid_nrw_idr

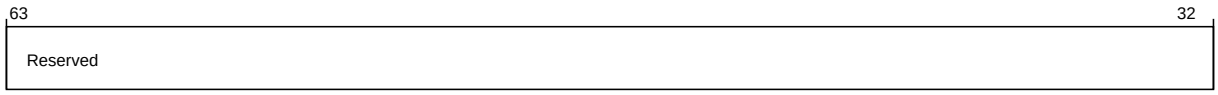
MPAM PARTID narrowing ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1050
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1260: por_hnf_mpam_ns_por_hnf_mpam_partid_nrw_idr (high)



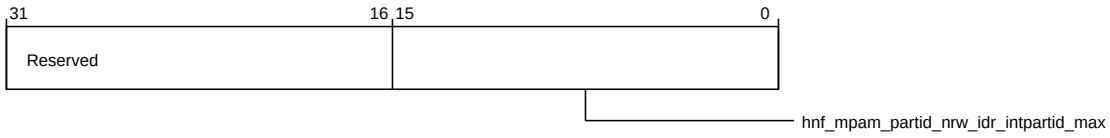
The following table shows the por_hnf_mpam_partid_nrw_idr higher register bit assignments.

Table 5-1274: por_hnf_mpam_ns_por_hnf_mpam_partid_nrw_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1261: por_hnf_mpam_ns_por_hnf_mpam_partid_nrw_idr (low)



The following table shows the por_hnf_mpam_partid_nrw_idr lower register bit assignments.

Table 5-1275: por_hnf_mpam_ns_por_hnf_mpam_partid_nrw_idr (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_mpam_partid_nrw_idr_intpartid_max	This field indicates the largest intPARTID supported in this component.	RO	16'h00

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5.3.11.12 por_hnf_mpam_msmon_idr

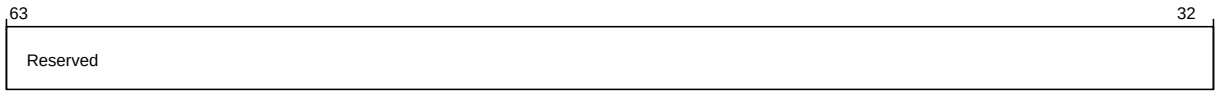
MPAM performance monitoring ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1080
Register reset Configuration dependent
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1262: por_hnf_mpam_ns_por_hnf_mpam_msmon_idr (high)



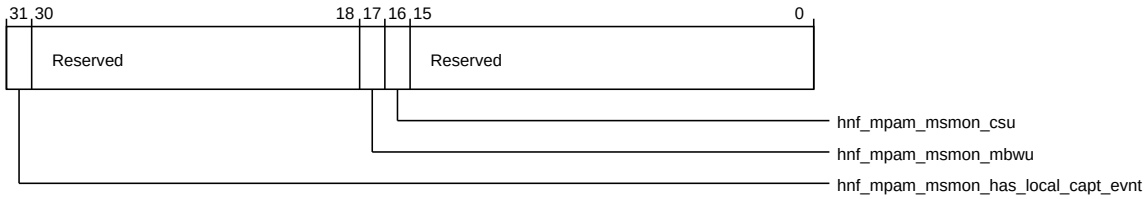
The following table shows the por_hnf_mpam_msmon_idr higher register bit assignments.

Table 5-1276: por_hnf_mpam_ns_por_hnf_mpam_msmon_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1263: por_hnf_mpam_ns_por_hnf_mpam_msmon_idr (low)



The following table shows the por_hnf_mpam_msmon_idr lower register bit assignments.

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Table 5-1277: por_hnf_mpam_ns_por_hnf_mpam_msmon_idr (low)

Bits	Field name	Description	Type	Reset
31	hnf_mpam_msmon_has_local_capt_evnt	Has the local capture event generator and the MSMON_CAPT_EVNT register.	RO	1'h1
30:18	Reserved	Reserved	RO	-
17	hnf_mpam_msmon_mbwu	This component has a performance monitor for Memory Bandwidth Usage by PARTID and PMG.	RO	Configuration dependent
16	hnf_mpam_msmon_csu	This component has a performance monitor for Cache Storage Usage by PARTID and PMG.	RO	Configuration dependent
15:0	Reserved	Reserved	RO	-

5.3.11.13 por_hnf_mpam_csumon_idr

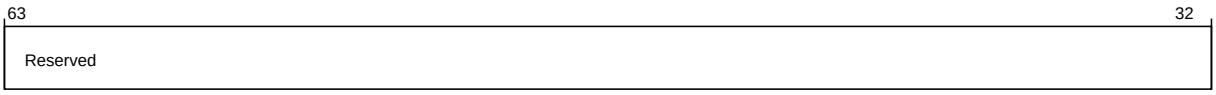
MPAM cache storage usage monitor ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1088
Register reset Configuration dependent
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1264: por_hnf_mpam_ns_por_hnf_mpam_csumon_idr (high)



The following table shows the por_hnf_mpam_csumon_idr higher register bit assignments.

Table 5-1278: por_hnf_mpam_ns_por_hnf_mpam_csumon_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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Figure 5-1265: por_hnf_mpam_ns_por_hnf_mpam_csumon_idr (low)



The following table shows the por_hnf_mpam_csumon_idr lower register bit assignments.

Table 5-1279: por_hnf_mpam_ns_por_hnf_mpam_csumon_idr (low)

Bits	Field name	Description	Type	Reset
31	hnf_mpam_csumon_has_capture	0: MSMON_CSU_CAPTURE is not implemented and there is no support for capture events in this component's CSU monitor feature. 1: This component's CSU monitor feature has an MSMON_CSU_CAPTURE register for every MSMON_CSU and supports the capture event behaviour.	RO	1'h1
30:16	Reserved	Reserved	RO	-
15:0	hnf_mpam_csumon_num_mon	The number of CSU monitoring counters implemented in this component.	RO	Configuration dependent

5.3.11.14 por_hnf_mpam_mbwumon_idr

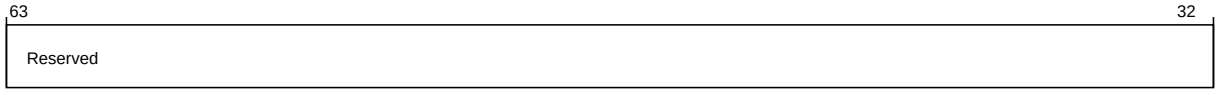
MPAM memory bandwidth usage monitor ID register. This is a shared register for S and NS

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1090
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1266: por_hnf_mpam_ns_por_hnf_mpam_mbwumon_idr (high)



The following table shows the por_hnf_mpam_mbwumon_idr higher register bit assignments.

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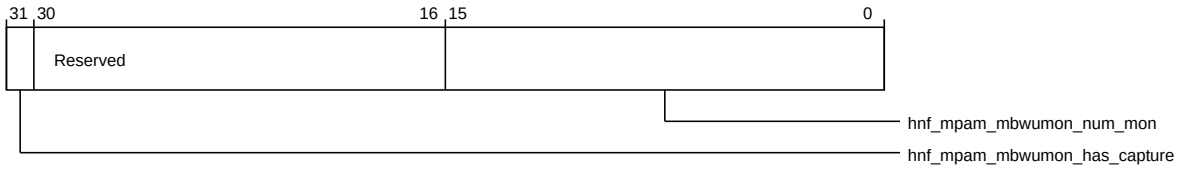
Table 5-1280: por_hnf_mpam_ns_por_hnf_mpam_mbwumon_idr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1267: por_hnf_mpam_ns_por_hnf_mpam_mbwumon_idr (low)



The following table shows the por_hnf_mpam_mbwumon_idr lower register bit assignments.

Table 5-1281: por_hnf_mpam_ns_por_hnf_mpam_mbwumon_idr (low)

Bits	Field name	Description	Type	Reset
31	hnf_mpam_mbwumon_has_capture	0: MSMON_MBWU_CAPTURE is not implemented and there is no support for capture events in this component's MBWU monitor feature. 1: This component's MBWU monitor feature has an MSMON_MBWU_CAPTURE register for every MSMON_MBWU and supports the capture event behaviour.	RO	1'h0
30:16	Reserved	Reserved	RO	-
15:0	hnf_mpam_mbwumon_num_mon	The number of MBWU monitoring counters implemented in this component.	RO	16'h0

5.3.11.15 por_hnf_ns_mpam_ecr

MPAM Error Control Register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h10F0
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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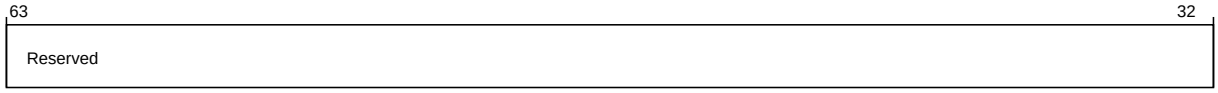
Figure 5-1268: por_hnf_mpam_ns_por_hnf_ns_mpam_ecr (high)



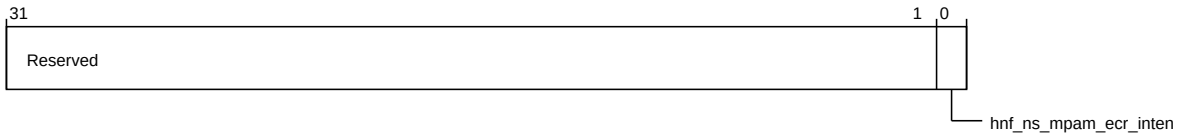
The following table shows the por_hnf_ns_mpam_ecr higher register bit assignments.

Table 5-1282: por_hnf_mpam_ns_por_hnf_ns_mpam_ecr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1269: por_hnf_mpam_ns_por_hnf_ns_mpam_ecr (low)



The following table shows the por_hnf_ns_mpam_ecr lower register bit assignments.

Table 5-1283: por_hnf_mpam_ns_por_hnf_ns_mpam_ecr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	hnf_ns_mpam_ecr_inten	Interrupt Enable. When INTEN = 0, MPAM error interrupts are not generated. When INTEN = 1, MPAM error interrupts are generated.	RW	1'h0

5.3.11.16 por_hnf_ns_mpam_esr

MPAM Error Status Register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h10F8
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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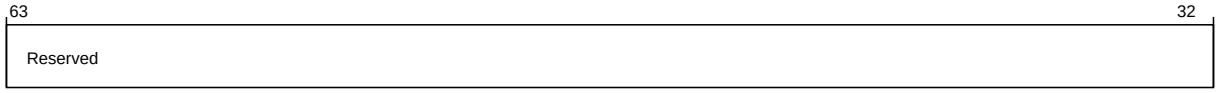
Figure 5-1270: por_hnf_mpam_ns_por_hnf_ns_mpam_esr (high)



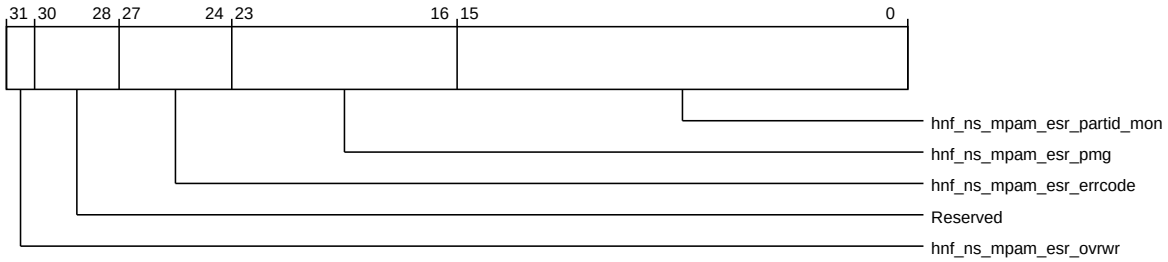
The following table shows the por_hnf_ns_mpam_esr higher register bit assignments.

Table 5-1284: por_hnf_mpam_ns_por_hnf_ns_mpam_esr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1271: por_hnf_mpam_ns_por_hnf_ns_mpam_esr (low)



The following table shows the por_hnf_ns_mpam_esr lower register bit assignments.

Table 5-1285: por_hnf_mpam_ns_por_hnf_ns_mpam_esr (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_mpam_esr_ovrwr	Overwritten. If 0 and ERRCODE is zero, no errors have occurred. If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register. If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error. The state where this bit is 1 and ERRCODE is zero is not produced by hardware and is only reached when software writes this combination into this register.	RW	1'h0
30:28	Reserved	Reserved	RO	-
27:24	hnf_ns_mpam_esr_errcode	Error code	RW	4'h0
23:16	hnf_ns_mpam_esr_pmg	PMG captured if the error code captures PMG, otherwise 0x0000.	RW	8'h0
15:0	hnf_ns_mpam_esr_partid_mon	PARTID captured if the error code captures PARTID. MON selector captured if the error code captures MON. Otherwise 0x0000.	RW	16'h0

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5.3.11.17 por_hnf_ns_mpamcfg_part_sel

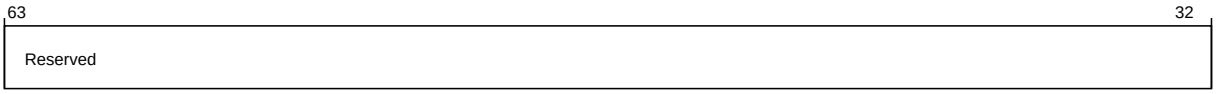
MPAM partition configuration selection register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1100
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1272: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_part_sel (high)



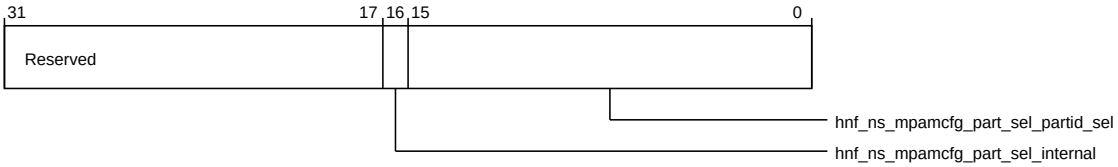
The following table shows the por_hnf_ns_mpamcfg_part_sel higher register bit assignments.

Table 5-1286: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_part_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1273: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_part_sel (low)



The following table shows the por_hnf_ns_mpamcfg_part_sel lower register bit assignments.

Table 5-1287: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_part_sel (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
16	hnf_ns_mpamcfg_part_sel_internal	If MPAMF_IDR.HAS_PARTID_NRW = 0, this field is RAZ/WI. If MPAMF_IDR.HAS_PARTID_NRW = 1, this bit decides how to interprete PARTID_SEL.	RW	1'h0
15:0	hnf_ns_mpamcfg_part_sel_partid_sel	Selects the partition ID to configure.	RW	16'h0

5.3.11.18 por_hnf_ns_mpamcfg_cmax

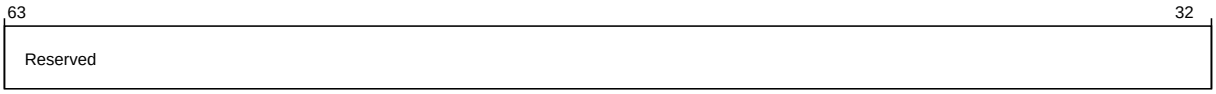
MPAM cache maximum capacity partition configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1108
Register reset 64'b111111
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1274: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cmax (high)



The following table shows the por_hnf_ns_mpamcfg_cmax higher register bit assignments.

Table 5-1288: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cmax (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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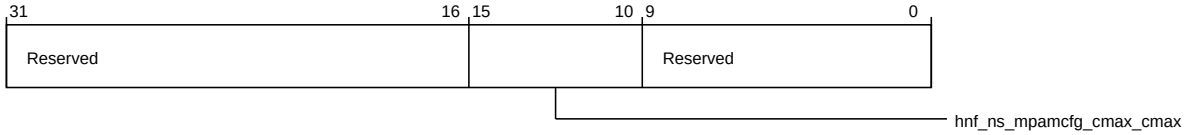
Figure 5-1275: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cmax (low)



The following table shows the por_hnf_ns_mpamcfg_cmax lower register bit assignments.

Table 5-1289: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cmax (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:10	hnf_ns_mpamcfg_cmax_cmax	Maximum cache capacity usage in fixed-point fraction of the cache capacity by the partition selected by MPAMCFG_PART_SEL.	RW	6'h3f
9:0	Reserved	Reserved	RO	-

5.3.11.19 por_hnf_ns_mpamcfg_mbw_min

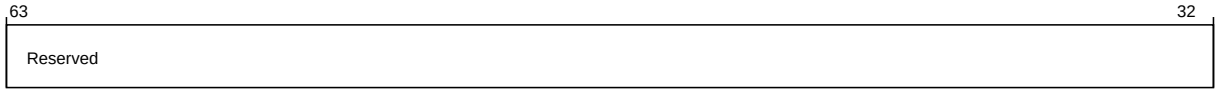
MPAM memory minimum bandwidth partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1200
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1276: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_min (high)



The following table shows the por_hnf_ns_mpamcfg_mbw_min higher register bit assignments.

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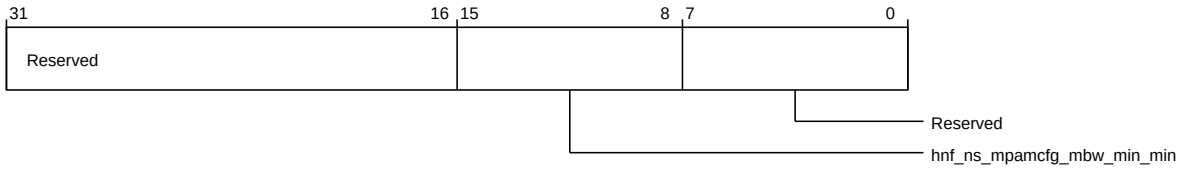
Table 5-1290: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_min (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1277: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_min (low)



The following table shows the por_hnf_ns_mpamcfg_mbw_min lower register bit assignments.

Table 5-1291: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_min (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:8	hnf_ns_mpamcfg_mbw_min_min	Memory minimum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
7:0	Reserved	Reserved	RO	-

5.3.11.20 por_hnf_ns_mpamcfg_mbw_max

MPAM memory maximum bandwidth partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1208
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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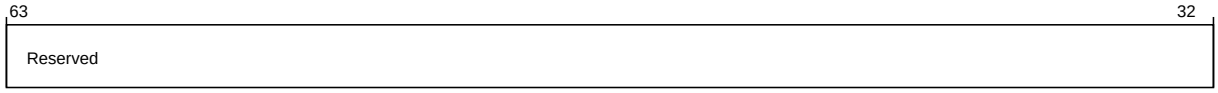
Figure 5-1278: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_max (high)



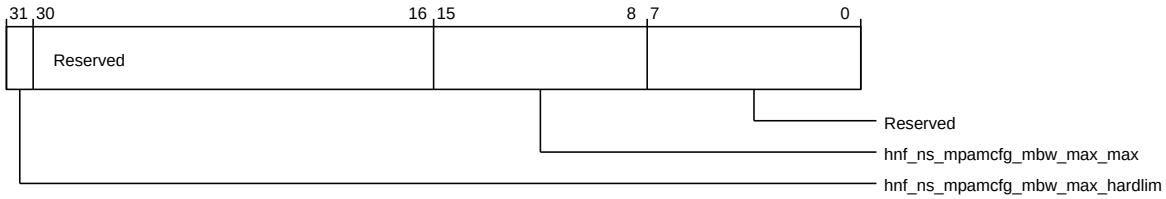
The following table shows the por_hnf_ns_mpamcfg_mbw_max higher register bit assignments.

Table 5-1292: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_max (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1279: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_max (low)



The following table shows the por_hnf_ns_mpamcfg_mbw_max lower register bit assignments.

Table 5-1293: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_max (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_mpamcfg_mbw_max_hardlim	0: When MAX bandwidth is exceeded, the partition may contend with a low preference for downstream bandwidth beyond its maximum bandwidth. 1: When MAX bandwidth is exceeded, the partition may not be use any more bandwidth until its memory bandwidth measurement falls below the maximum limit.	RW	1'h0
30:16	Reserved	Reserved	RO	-
15:8	hnf_ns_mpamcfg_mbw_max_max	Memory maximum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
7:0	Reserved	Reserved	RO	-

5.3.11.21 por_hnf_ns_mpamcfg_mbw_winwd

MPAM memory bandwidth partitioning window width register. This register is a banked seperately for S and NS

Its characteristics are:

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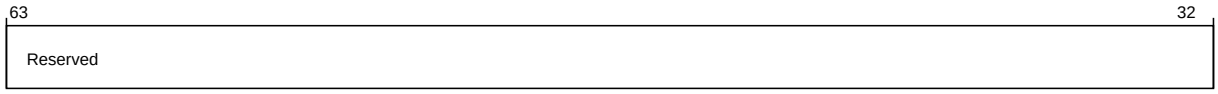
Type RW
Register width (Bits) 64
Address offset 16'h1220
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1280: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_winwd (high)



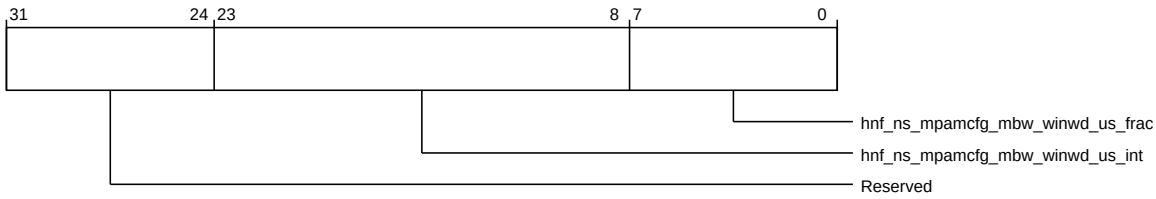
The following table shows the por_hnf_ns_mpamcfg_mbw_winwd higher register bit assignments.

Table 5-1294: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_winwd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1281: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_winwd (low)



The following table shows the por_hnf_ns_mpamcfg_mbw_winwd lower register bit assignments.

Table 5-1295: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_winwd (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:8	hnf_ns_mpamcfg_mbw_winwd_us_int	Memory bandwidth accounting period integer microseconds.	RW	16'h0
7:0	hnf_ns_mpamcfg_mbw_winwd_us_frac	Memory bandwidth accounting period fractions of a microsecond.	RW	8'h0

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5.3.11.22 por_hnf_ns_mpamcfg_pri

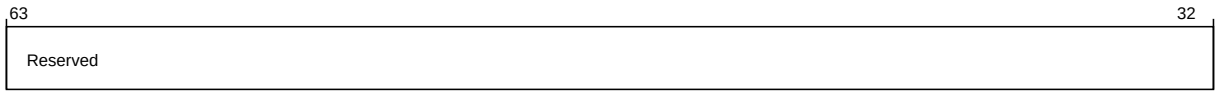
MPAM priority partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1400
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1282: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_pri (high)



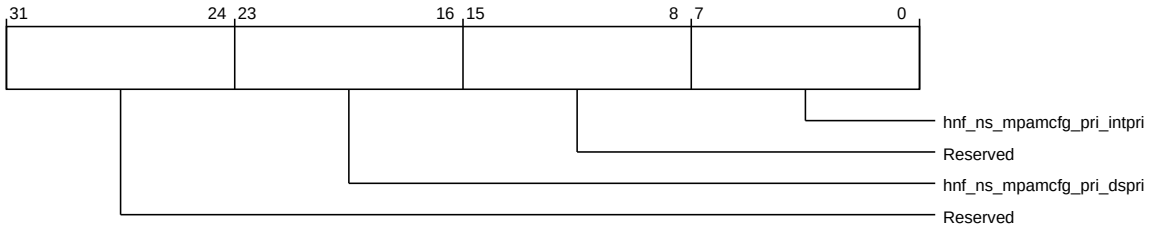
The following table shows the por_hnf_ns_mpamcfg_pri higher register bit assignments.

Table 5-1296: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_pri (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1283: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_pri (low)



The following table shows the por_hnf_ns_mpamcfg_pri lower register bit assignments.

Table 5-1297: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_pri (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
23:16	hnf_ns_mpamcfg_pri_dspri	If HAS_DSPRI is 1, this field is a priority value applied to downstream communications from this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_ns_mpamcfg_pri_intpri	If HAS_INTPRI is 1, this field is a priority value applied internally inside this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0

5.3.11.23 por_hnf_ns_mpamcfg_mbw_prop

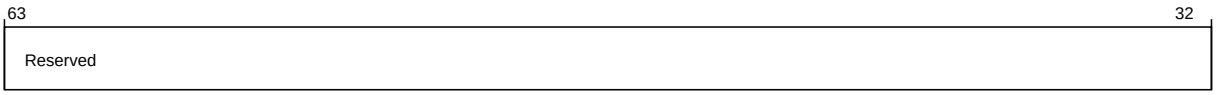
Memory bandwidth proportional stride partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1500
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1284: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_prop (high)



The following table shows the por_hnf_ns_mpamcfg_mbw_prop higher register bit assignments.

Table 5-1298: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_prop (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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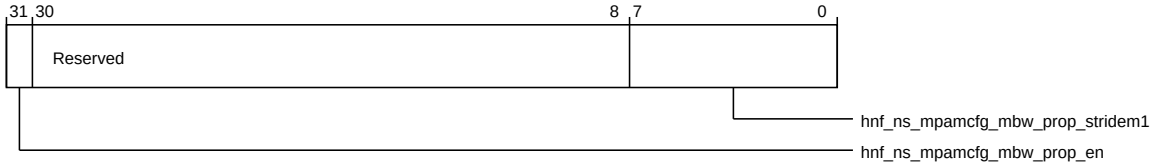
Figure 5-1285: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_prop (low)



The following table shows the por_hnf_ns_mpamcfg_mbw_prop lower register bit assignments.

Table 5-1299: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_mbw_prop (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_mpamcfg_mbw_prop_en	0: The selected partition is not regulated by proportional stride bandwidth partitioning. 1: The selected partition has bandwidth usage regulated by proportional stride bandwidth partitioning as controlled by STRIDEM1.	RW	1'h0
30:8	Reserved	Reserved	RO	-
7:0	hnf_ns_mpamcfg_mbw_prop_stridem1	Normalized cost of a bandwidth consumption by the partition. STRIDEM1 is the stride for the partition minus one.	RW	8'h0

5.3.11.24 por_hnf_ns_mpamcfg_intpartid

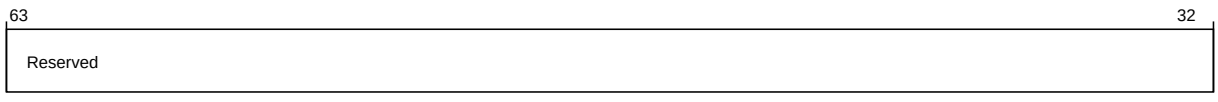
MPAM internal partition narrowing configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1600
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1286: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_intpartid (high)



The following table shows the por_hnf_ns_mpamcfg_intpartid higher register bit assignments.

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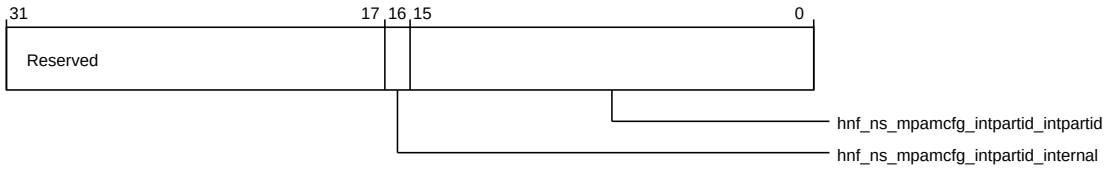
Table 5-1300: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_intpartid (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1287: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_intpartid (low)



The following table shows the por_hnf_ns_mpamcfg_intpartid lower register bit assignments.

Table 5-1301: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_intpartid (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	hnf_ns_mpamcfg_intpartid_internal	This bit must be 1 when written to the register. If written as 0, the write will not update the reqPARTID to intPARTID association.	RW	1'h0
15:0	hnf_ns_mpamcfg_intpartid_intpartid	This field contains the intPARTID mapped to the reqPARTID in MPAMCFG_PART_SEL.	RW	16'h0

5.3.11.25 por_hnf_ns_msmon_cfg_mon_sel

Memory system performance monitor selection register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1800
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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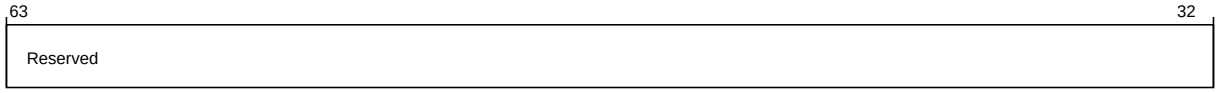
Figure 5-1288: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mon_sel (high)



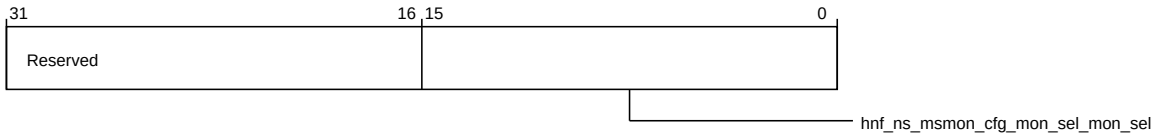
The following table shows the por_hnf_ns_msmon_cfg_mon_sel higher register bit assignments.

Table 5-1302: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mon_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1289: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mon_sel (low)



The following table shows the por_hnf_ns_msmon_cfg_mon_sel lower register bit assignments.

Table 5-1303: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mon_sel (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_ns_msmon_cfg_mon_sel_mon_sel	Selects the performance monitor to configure.	RW	16'h0

5.3.11.26 por_hnf_ns_msmon_capt_evnt

Memory system performance monitoring capture event generation register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1808
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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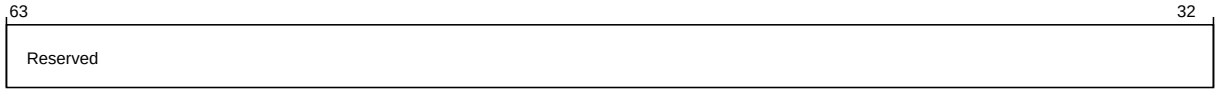
Figure 5-1290: por_hnf_mpam_ns_por_hnf_ns_msmon_capt_evnt (high)



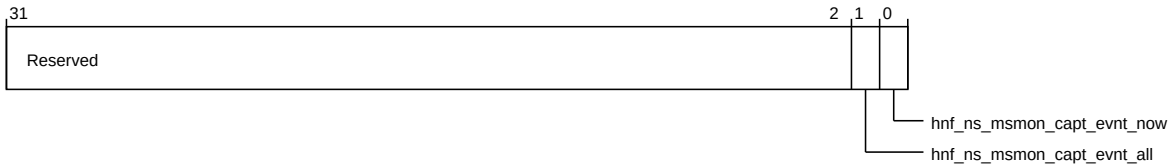
The following table shows the por_hnf_ns_msmon_capt_evnt higher register bit assignments.

Table 5-1304: por_hnf_mpam_ns_por_hnf_ns_msmon_capt_evnt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1291: por_hnf_mpam_ns_por_hnf_ns_msmon_capt_evnt (low)



The following table shows the por_hnf_ns_msmon_capt_evnt lower register bit assignments.

Table 5-1305: por_hnf_mpam_ns_por_hnf_ns_msmon_capt_evnt (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	hnf_ns_msmon_capt_evnt_all	In Secure version, if ALL written as 1 and NOW is also written as 1, signal a capture event to Secure and Non-secure monitors in this memory system component with CAPT_EVNT = 7. If written as 0 and NOW is written as 1, signal a capture event to Secure monitors in this memory system component with CAPT_EVNT = 7. In Non-secure version if NOW is written as 1, signal a capture event to Non-secure monitors in this memory system component with CAPT_EVNT = 7.	RW	1'h0
0	hnf_ns_msmon_capt_evnt_now	When written as 1, this bit causes an event to all monitors in this memory system component with CAPT_EVNT set to the value of 7. When this bit is written as 0, no event is signalled.	RW	1'h0

5.3.11.27 por_hnf_ns_msmon_cfg_csu_flt

Memory system performance monitor configure cache storage usage monitor filter register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW

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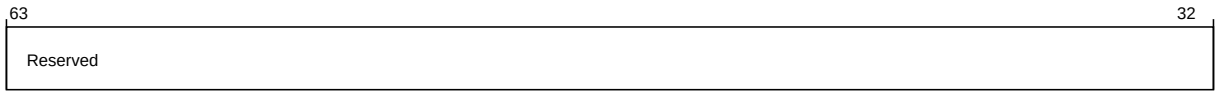
Register width (Bits) 64
Address offset 16'h1810
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1292: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_flt (high)



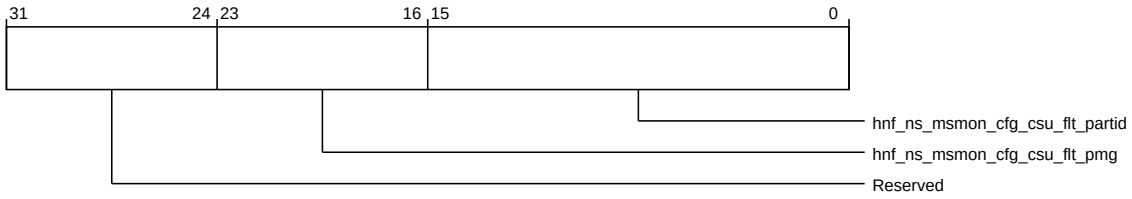
The following table shows the por_hnf_ns_msmon_cfg_csu_flt higher register bit assignments.

Table 5-1306: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_flt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1293: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_flt (low)



The following table shows the por_hnf_ns_msmon_cfg_csu_flt lower register bit assignments.

Table 5-1307: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_flt (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_ns_msmon_cfg_csu_flt_pmg	Configures the cache storage usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	8'h0
15:0	hnf_ns_msmon_cfg_csu_flt_partid	Configures the cache storage usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	16'h0

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5.3.11.28 por_hnf_ns_msmon_cfg_csu_ctl

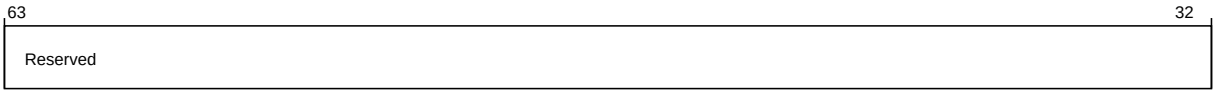
Memory system performance monitor configure cache storage usage monitor control register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1818
Register reset 64'b0000000000000000010011
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1294: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_ctl (high)



The following table shows the por_hnf_ns_msmon_cfg_csu_ctl higher register bit assignments.

Table 5-1308: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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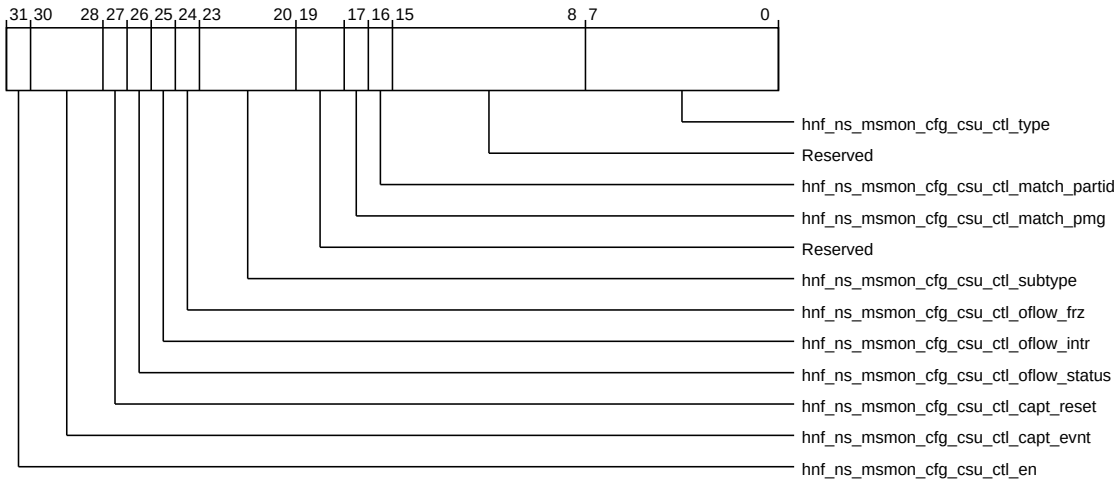
Figure 5-1295: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_ctl (low)



The following table shows the por_hnf_ns_msmon_cfg_csu_ctl lower register bit assignments.

Table 5-1309: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_csu_ctl (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_cfg_csu_ctl_en	0: The monitor is disabled and must not collect any information. 1: The monitor is enabled to collect information according to its configuration.	RW	1'h0
30:28	hnf_ns_msmon_cfg_csu_ctl_capt_evnt	Select the event that triggers capture from the following: 0: No capture event is triggered. 1: External capture event 1 (optional but recommended)	RW	3'h0
27	hnf_ns_msmon_cfg_csu_ctl_capt_reset	Capture is not implemented for the CSU monitor type.	RW	1'h0
26	hnf_ns_msmon_cfg_csu_ctl_oflow_status	0: No overflow has occurred. 1: At least one overflow has occurred since this bit was last written.	RW	1'h0
25	hnf_ns_msmon_cfg_csu_ctl_oflow_intr	0: No interrupt. 1: On overflow, an implementation-specific interrupt is signalled.	RW	1'h0
24	hnf_ns_msmon_cfg_csu_ctl_oflow_frz	0: Monitor count wraps on overflow. 1: Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1.	RW	1'h0
23:20	hnf_ns_msmon_cfg_csu_ctl_subtype	Not currently used for CSU monitors, but reserved for future use.	RW	4'h0
19:18	Reserved	Reserved	RO	-
17	hnf_ns_msmon_cfg_csu_ctl_match_pmg	0: Monitor storage used by all PMG values. 1: Only monitor storage used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0

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Bits	Field name	Description	Type	Reset
16	hnf_ns_msmon_cfg_csu_ctl_match_partid	0: Monitor storage used by all PARTIDs. 1: Only monitor storage used with the PARTID matching MSMON_CFG_CSU_FLT.PARTID.	RW	1'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_ns_msmon_cfg_csu_ctl_type	Read-only: Constant type indicating the type of the monitor. CSU monitor is TYPE = 0x43.	RW	8'h43

5.3.11.29 por_hnf_ns_msmon_cfg_mbwu_flt

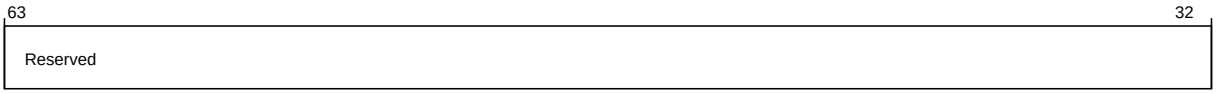
Memory system performance monitor configure memory bandwidth usage monitor filter register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1820
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1296: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_flt (high)



The following table shows the por_hnf_ns_msmon_cfg_mbwu_flt higher register bit assignments.

Table 5-1310: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_flt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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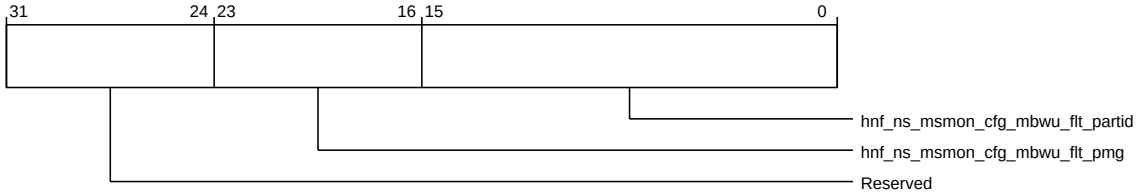
Figure 5-1297: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_flt (low)



The following table shows the por_hnf_ns_msmon_cfg_mbwu_flt lower register bit assignments.

Table 5-1311: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_flt (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_ns_msmon_cfg_mbwu_flt_pmg	Configures the memory bandwidth usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	8'h0
15:0	hnf_ns_msmon_cfg_mbwu_flt_partid	Configures the memory bandwidth usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	16'h0

5.3.11.30 por_hnf_ns_msmon_cfg_mbwu_ctl

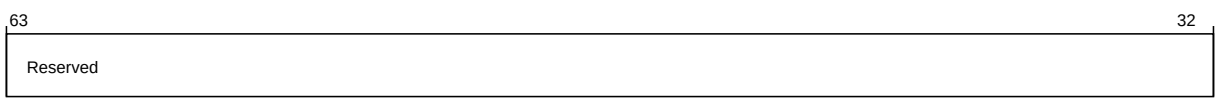
Memory system performance monitor configure memory bandwidth usage monitor control register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1828
Register reset 64'b0000000000000000010010
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1298: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_ctl (high)



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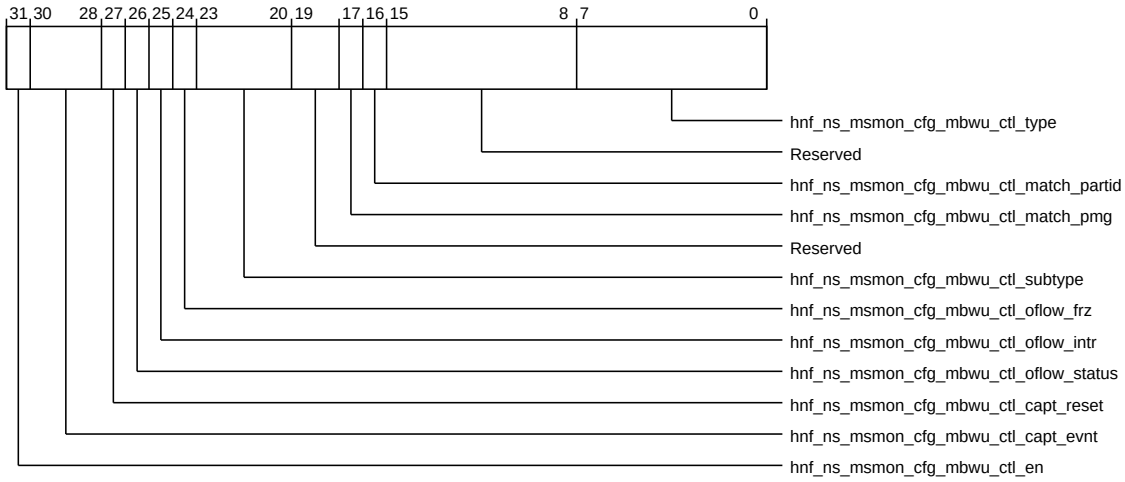
The following table shows the por_hnf_ns_msmon_cfg_mbwu_ctl higher register bit assignments.

Table 5-1312: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1299: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_ctl (low)



The following table shows the por_hnf_ns_msmon_cfg_mbwu_ctl lower register bit assignments.

Table 5-1313: por_hnf_mpam_ns_por_hnf_ns_msmon_cfg_mbwu_ctl (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_cfg_mbwu_ctl_en	0: The monitor is disabled and must not collect any information. 1: The monitor is enabled to collect information according to its configuration.	RW	1'h0
30:28	hnf_ns_msmon_cfg_mbwu_ctl_capt_evnt	Select the event that triggers capture from the following: 0: No capture event is triggered. 1: External capture event 1 (optional but recommended)	RW	3'h0
27	hnf_ns_msmon_cfg_mbwu_ctl_capt_reset	0: Monitor is not reset on capture. 1: Monitor is reset on capture.	RW	1'h0
26	hnf_ns_msmon_cfg_mbwu_ctl_oflow_status	0: No overflow has occurred. 1: At least one overflow has occurred since this bit was last written.	RW	1'h0
25	hnf_ns_msmon_cfg_mbwu_ctl_oflow_intr	0: No interrupt. 1: On overflow, an implementation-specific interrupt is signalled.	RW	1'h0

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Bits	Field name	Description	Type	Reset
24	hnf_ns_msmon_cfg_mbwu_ctl_oflow_frz	0: Monitor count wraps on overflow. 1: Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1.	RW	1'h0
23:20	hnf_ns_msmon_cfg_mbwu_ctl_subtype	A monitor can have other event matching criteria. The meaning of values in this field varies by monitor type. The MBWU monitor type supports: 0: Do not count any bandwidth. 1: Count bandwidth used by memory reads 2: Count bandwidth used by memory writes 3: Count bandwidth used by memory reads and memory writes All other values are reserved and behaviour of a monitor with SUBTYPE set to one of the reserved values is UNPREDICTABLE.	RW	4'h0
19:18	Reserved	Reserved	RO	-
17	hnf_ns_msmon_cfg_mbwu_ctl_match_pmg	0: Monitor bandwidth used by all PMG values. 1: Only monitor bandwidth used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0
16	hnf_ns_msmon_cfg_mbwu_ctl_match_partid	0: Monitor bandwidth used by all PARTIDs. 1: Only monitor bandwidth used with the PARTID matching MSMON_CFG_MBWU_FLT.PARTID.	RW	1'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_ns_msmon_cfg_mbwu_ctl_type	Read-only: Constant type indicating the type of the monitor. MBWU monitor is TYPE = 0x42.	RW	8'h42

5.3.11.31 por_hnf_ns_msmon_csu

Memory system performance monitor cache storage usage monitor register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1840
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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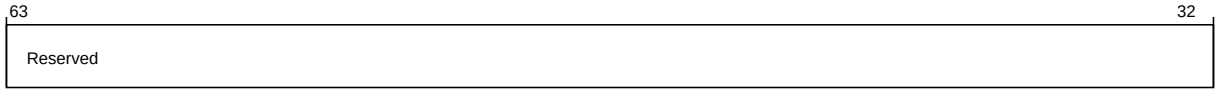
Figure 5-1300: por_hnf_mpam_ns_por_hnf_ns_msmon_csu (high)



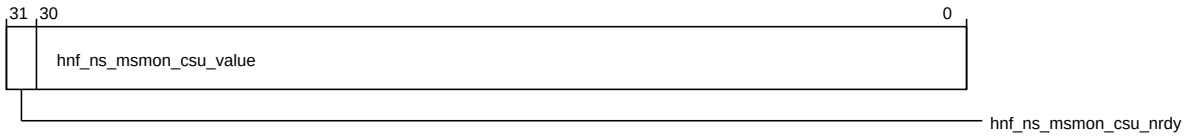
The following table shows the por_hnf_ns_msmon_csu higher register bit assignments.

Table 5-1314: por_hnf_mpam_ns_por_hnf_ns_msmon_csu (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1301: por_hnf_mpam_ns_por_hnf_ns_msmon_csu (low)



The following table shows the por_hnf_ns_msmon_csu lower register bit assignments.

Table 5-1315: por_hnf_mpam_ns_por_hnf_ns_msmon_csu (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_csu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_ns_msmon_csu_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

5.3.11.32 por_hnf_ns_msmon_csu_capture

Memory system performance monitor cache storage usage capture register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1848
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

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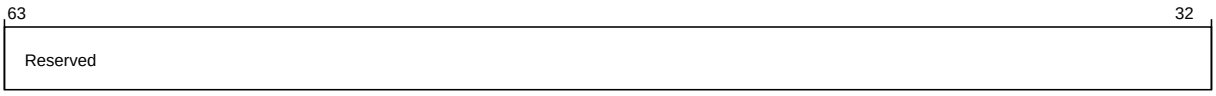
The following figure shows the higher register bit assignments.

Figure 5-1302: por_hnf_mpam_ns_por_hnf_ns_msmon_csu_capture (high)



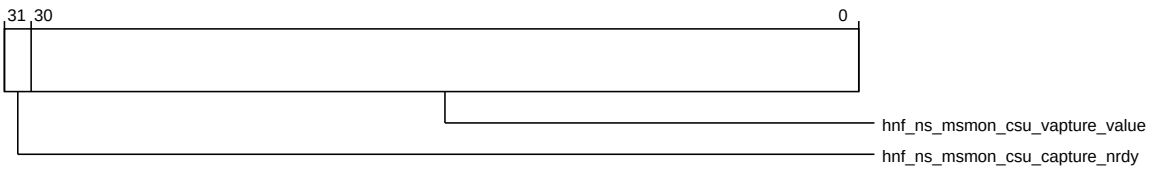
The following table shows the por_hnf_ns_msmon_csu_capture higher register bit assignments.

Table 5-1316: por_hnf_mpam_ns_por_hnf_ns_msmon_csu_capture (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1303: por_hnf_mpam_ns_por_hnf_ns_msmon_csu_capture (low)



The following table shows the por_hnf_ns_msmon_csu_capture lower register bit assignments.

Table 5-1317: por_hnf_mpam_ns_por_hnf_ns_msmon_csu_capture (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_csu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_ns_msmon_csu_vapture_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

5.3.11.33 por_hnf_ns_msmon_mbwu

Memory system performance monitor memory bandwidth usage monitor register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1860
Register reset 64'b0

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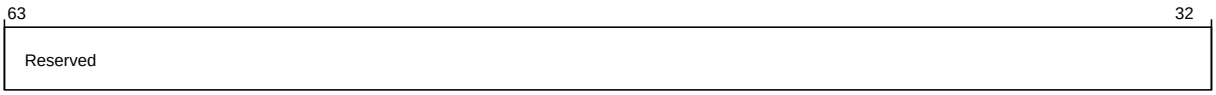
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1304: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu (high)



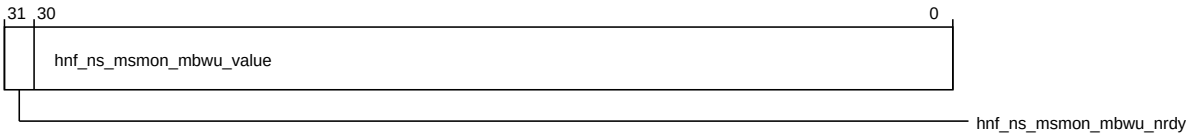
The following table shows the por_hnf_ns_msmon_mbwu higher register bit assignments.

Table 5-1318: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1305: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu (low)



The following table shows the por_hnf_ns_msmon_mbwu lower register bit assignments.

Table 5-1319: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_mbwu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_ns_msmon_mbwu_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

5.3.11.34 por_hnf_ns_msmon_mbwu_capture

Memory system performance monitor memory bandwidth usage capture register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW

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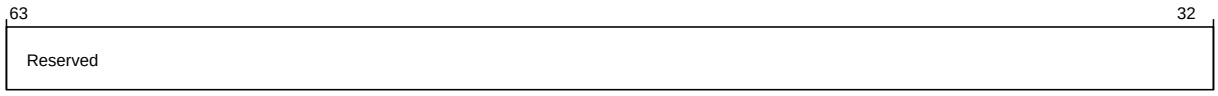
Register width (Bits) 64
Address offset 16'h1868
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1306: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu_capture (high)



The following table shows the por_hnf_ns_msmon_mbwu_capture higher register bit assignments.

Table 5-1320: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu_capture (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1307: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu_capture (low)



The following table shows the por_hnf_ns_msmon_mbwu_capture lower register bit assignments.

Table 5-1321: por_hnf_mpam_ns_por_hnf_ns_msmon_mbwu_capture (low)

Bits	Field name	Description	Type	Reset
31	hnf_ns_msmon_mbwu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_ns_msmon_mbwu_capture_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

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5.3.11.35 por_hnf_ns_mpamcfg_cpbm

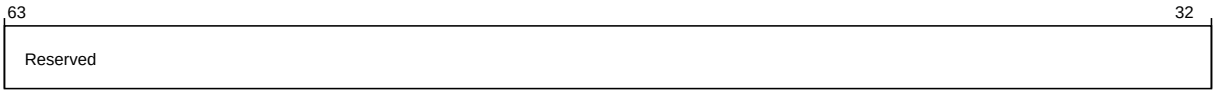
MPAM cache portion bitmap partition configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b1111111111111111
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1308: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cpbm (high)



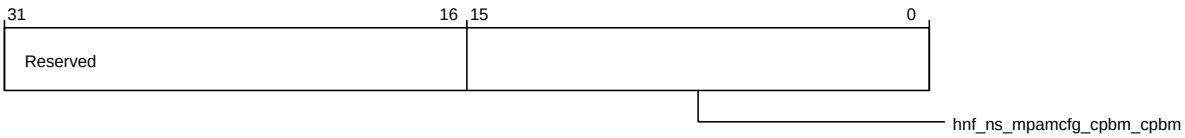
The following table shows the por_hnf_ns_mpamcfg_cpbm higher register bit assignments.

Table 5-1322: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cpbm (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1309: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cpbm (low)



The following table shows the por_hnf_ns_mpamcfg_cpbm lower register bit assignments.

Table 5-1323: por_hnf_mpam_ns_por_hnf_ns_mpamcfg_cpbm (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
15:0	hnf_ns_mpamcfg_cpbm_cpbm	Bitmap of portions of cache capacity allocable by the partition selected by MPAMCFG_PART_SEL. NOTE: CPBM can not be all zeros for any PARTID.	RW	16'hFFFF

5.3.12 HN-F MPAM_S register descriptions

This section lists the HN-F MPAM_S registers.

5.3.12.1 por_hnf_mpam_s_node_info

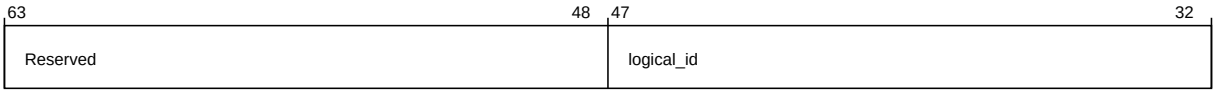
Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1310: por_hnf_mpam_s_por_hnf_mpam_s_node_info (high)



The following table shows the por_hnf_mpam_s_node_info higher register bit assignments.

Table 5-1324: por_hnf_mpam_s_por_hnf_mpam_s_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

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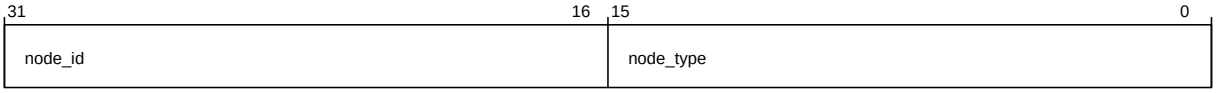
Figure 5-1311: por_hnf_mpam_s_por_hnf_mpam_s_node_info (low)



The following table shows the por_hnf_mpam_s_node_info lower register bit assignments.

Table 5-1325: por_hnf_mpam_s_por_hnf_mpam_s_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0008

5.3.12.2 por_hnf_mpam_s_child_info

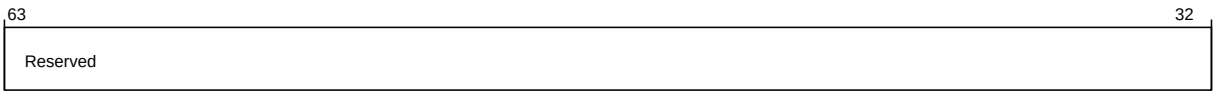
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1312: por_hnf_mpam_s_por_hnf_mpam_s_child_info (high)



The following table shows the por_hnf_mpam_s_child_info higher register bit assignments.

Table 5-1326: por_hnf_mpam_s_por_hnf_mpam_s_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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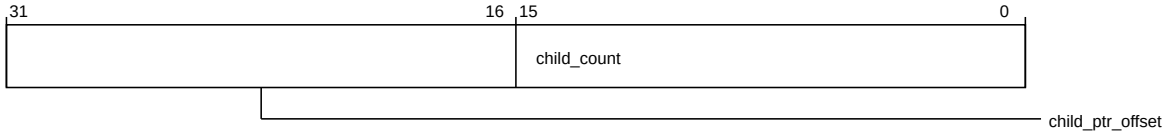
Figure 5-1313: por_hnf_mpam_s_por_hnf_mpam_s_child_info (low)



The following table shows the por_hnf_mpam_s_child_info lower register bit assignments.

Table 5-1327: por_hnf_mpam_s_por_hnf_mpam_s_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

5.3.12.3 por_hnf_mpam_s_secure_register_groups_override

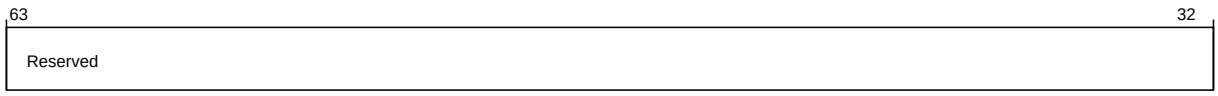
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1314: por_hnf_mpam_s_por_hnf_mpam_s_secure_register_groups_override (high)



The following table shows the por_hnf_mpam_s_secure_register_groups_override higher register bit assignments.

Table 5-1328: por_hnf_mpam_s_por_hnf_mpam_s_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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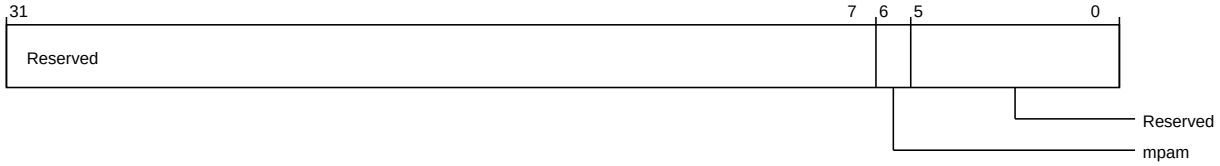
Figure 5-1315: por_hnf_mpam_s_por_hnf_mpam_s_secure_register_groups_override (low)



The following table shows the por_hnf_mpam_s_secure_register_groups_override lower register bit assignments.

Table 5-1329: por_hnf_mpam_s_por_hnf_mpam_s_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6	mpam	Allows Non-secure access to Secure MPAM registers	RW	1'b0
5:0	Reserved	Reserved	RO	-

5.3.12.4 por_hnf_mpam_sidr

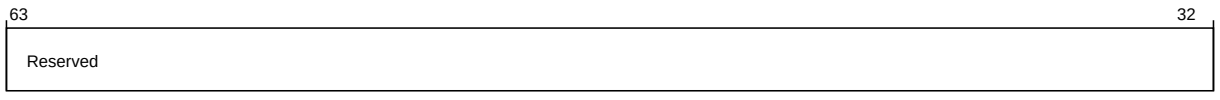
MPAM features Secure ID register. This is Secure (S) register only.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h1008
Register reset Configuration dependent
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1316: por_hnf_mpam_s_por_hnf_mpam_sidr (high)



The following table shows the por_hnf_mpam_sidr higher register bit assignments.

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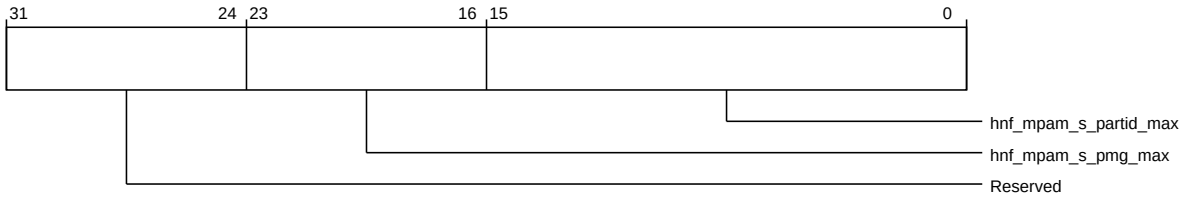
Table 5-1330: por_hnf_mpam_s_por_hnf_mpam_sidr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1317: por_hnf_mpam_s_por_hnf_mpam_sidr (low)



The following table shows the por_hnf_mpam_sidr lower register bit assignments.

Table 5-1331: por_hnf_mpam_s_por_hnf_mpam_sidr (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_mpam_s_pmg_max	Maximum value of Secure PMG supported by this HN-F	RO	Configuration dependent
15:0	hnf_mpam_s_partid_max	Maximum value of Secure PARTID supported by this HN-F	RO	Configuration dependent

5.3.12.5 por_hnf_s_mpam_ecr

MPAM Error Control Register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h10F0
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

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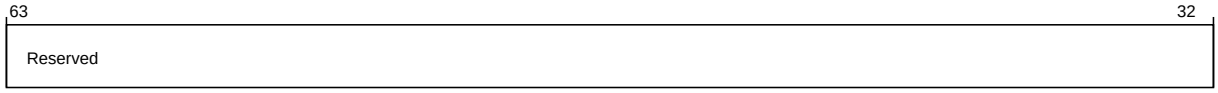
Figure 5-1318: por_hnf_mpam_s_por_hnf_s_mpam_ecr (high)



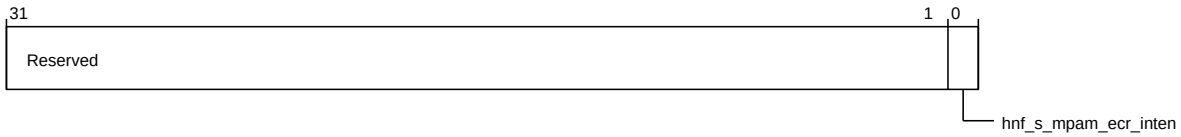
The following table shows the por_hnf_s_mpam_ecr higher register bit assignments.

Table 5-1332: por_hnf_mpam_s_por_hnf_s_mpam_ecr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1319: por_hnf_mpam_s_por_hnf_s_mpam_ecr (low)



The following table shows the por_hnf_s_mpam_ecr lower register bit assignments.

Table 5-1333: por_hnf_mpam_s_por_hnf_s_mpam_ecr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	hnf_s_mpam_ecr_inten	Interrupt Enable. When INTEN = 0, MPAM error interrupts are not generated. When INTEN = 1, MPAM error interrupts are generated.	RW	1'h0

5.3.12.6 por_hnf_s_mpam_esr

MPAM Error Status Register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h10F8
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

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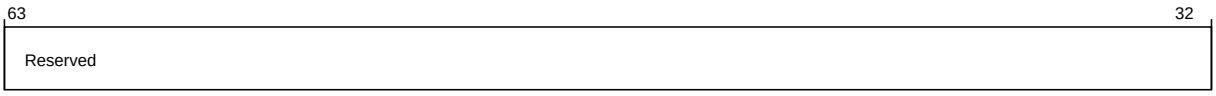
The following figure shows the higher register bit assignments.

Figure 5-1320: por_hnf_mpam_s_por_hnf_s_mpam_esr (high)



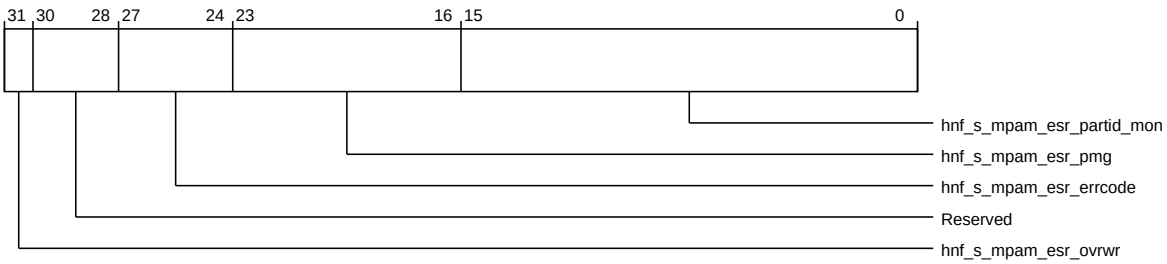
The following table shows the por_hnf_s_mpam_esr higher register bit assignments.

Table 5-1334: por_hnf_mpam_s_por_hnf_s_mpam_esr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1321: por_hnf_mpam_s_por_hnf_s_mpam_esr (low)



The following table shows the por_hnf_s_mpam_esr lower register bit assignments.

Table 5-1335: por_hnf_mpam_s_por_hnf_s_mpam_esr (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_mpam_esr_ovrwr	Overwritten. If 0 and ERRCODE is zero, no errors have occurred. If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register. If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error. The state where this bit is 1 and ERRCODE is zero is not produced by hardware and is only reached when software writes this combination into this register.	RW	1'h0
30:28	Reserved	Reserved	RO	-
27:24	hnf_s_mpam_esr_errcode	Error code	RW	4'h0
23:16	hnf_s_mpam_esr_pmg	PMG captured if the error code captures PMG, otherwise 0x0000.	RW	8'h0

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Bits	Field name	Description	Type	Reset
15:0	hnf_s_mpam_esr_partid_mon	PARTID captured if the error code captures PARTID. MON selector captured if the error code captures MON. Otherwise 0x0000.	RW	16'h0

5.3.12.7 por_hnf_s_mpamcfg_part_sel

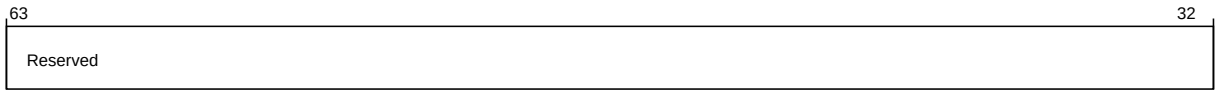
MPAM partition configuration selection register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1100
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1322: por_hnf_mpam_s_por_hnf_s_mpamcfg_part_sel (high)



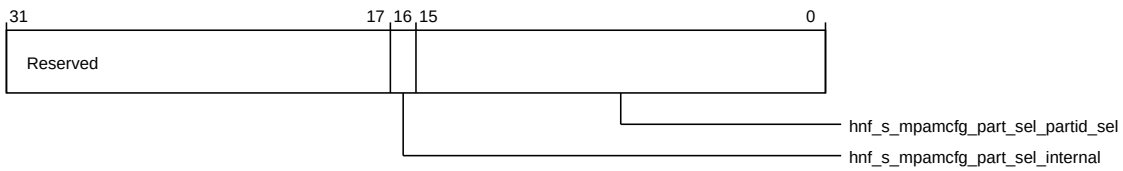
The following table shows the por_hnf_s_mpamcfg_part_sel higher register bit assignments.

Table 5-1336: por_hnf_mpam_s_por_hnf_s_mpamcfg_part_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1323: por_hnf_mpam_s_por_hnf_s_mpamcfg_part_sel (low)



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The following table shows the por_hnf_s_mpamcfg_part_sel lower register bit assignments.

Table 5-1337: por_hnf_mpam_s_por_hnf_s_mpamcfg_part_sel (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	hnf_s_mpamcfg_part_sel_internal	If MPAMF_IDR.HAS_PARTID_NRW = 0, this field is RAZ/WI. If MPAMF_IDR.HAS_PARTID_NRW = 1, this bit decides how to interprete PARTID_SEL.	RW	1'h0
15:0	hnf_s_mpamcfg_part_sel_partid_sel	Selects the partition ID to configure.	RW	16'h0

5.3.12.8 por_hnf_s_mpamcfg_cmax

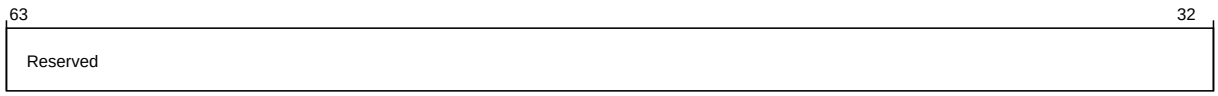
MPAM cache maximum capacity partition configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1108
Register reset 64'b111111
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1324: por_hnf_mpam_s_por_hnf_s_mpamcfg_cmax (high)



The following table shows the por_hnf_s_mpamcfg_cmax higher register bit assignments.

Table 5-1338: por_hnf_mpam_s_por_hnf_s_mpamcfg_cmax (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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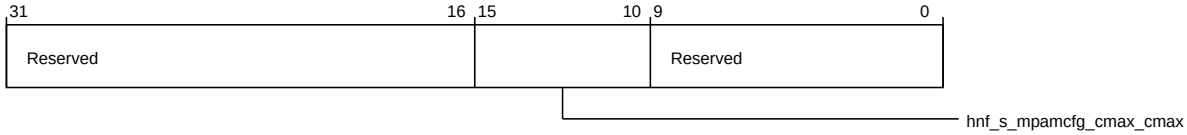
Figure 5-1325: por_hnf_mpam_s_por_hnf_s_mpamcfg_cmax (low)



The following table shows the por_hnf_s_mpamcfg_cmax lower register bit assignments.

Table 5-1339: por_hnf_mpam_s_por_hnf_s_mpamcfg_cmax (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:10	hnf_s_mpamcfg_cmax_cmax	Maximum cache capacity usage in fixed-point fraction of the cache capacity by the partition selected by MPAMCFG_PART_SEL.	RW	6'h3f
9:0	Reserved	Reserved	RO	-

5.3.12.9 por_hnf_s_mpamcfg_mbw_min

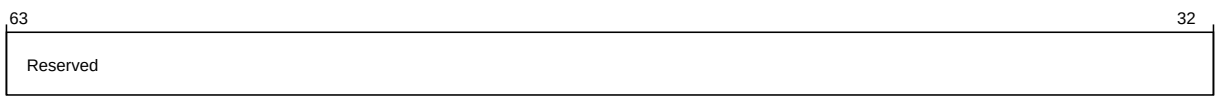
MPAM memory minimum bandwidth partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1200
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1326: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_min (high)



The following table shows the por_hnf_s_mpamcfg_mbw_min higher register bit assignments.

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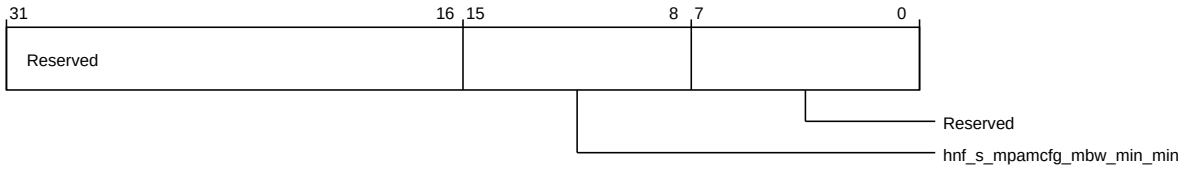
Table 5-1340: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_min (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1327: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_min (low)



The following table shows the por_hnf_s_mpamcfg_mbw_min lower register bit assignments.

Table 5-1341: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_min (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:8	hnf_s_mpamcfg_mbw_min_min	Memory minimum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
7:0	Reserved	Reserved	RO	-

5.3.12.10 por_hnf_s_mpamcfg_mbw_max

MPAM memory maximum bandwidth partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1208
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

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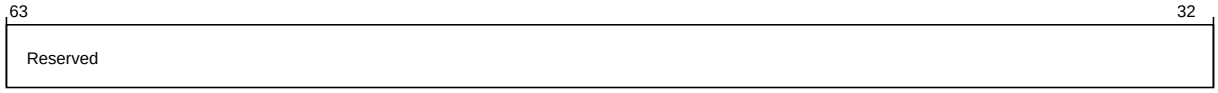
Figure 5-1328: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_max (high)



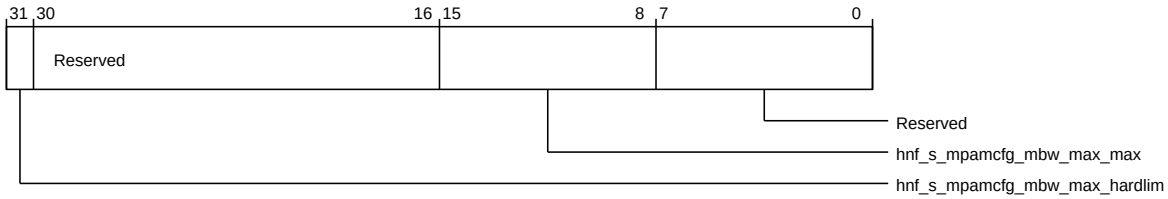
The following table shows the por_hnf_s_mpamcfg_mbw_max higher register bit assignments.

Table 5-1342: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_max (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1329: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_max (low)



The following table shows the por_hnf_s_mpamcfg_mbw_max lower register bit assignments.

Table 5-1343: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_max (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_mpamcfg_mbw_max_hardlim	0: When MAX bandwidth is exceeded, the partition may contend with a low preference for downstream bandwidth beyond its maximum bandwidth. 1: When MAX bandwidth is exceeded, the partition may not be use any more bandwidth until its memory bandwidth measurement falls below the maximum limit.	RW	1'h0
30:16	Reserved	Reserved	RO	-
15:8	hnf_s_mpamcfg_mbw_max_max	Memory maximum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
7:0	Reserved	Reserved	RO	-

5.3.12.11 por_hnf_s_mpamcfg_mbw_winwd

MPAM memory bandwidth partitioning window width register. This register is a banked seperately for S and NS

Its characteristics are:

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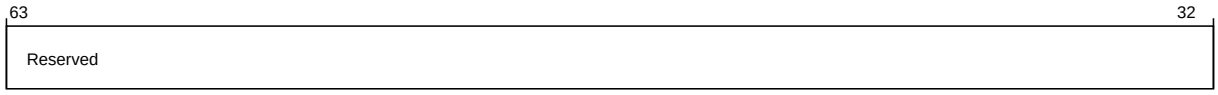
Type RW
Register width (Bits) 64
Address offset 16'h1220
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1330: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_winwd (high)



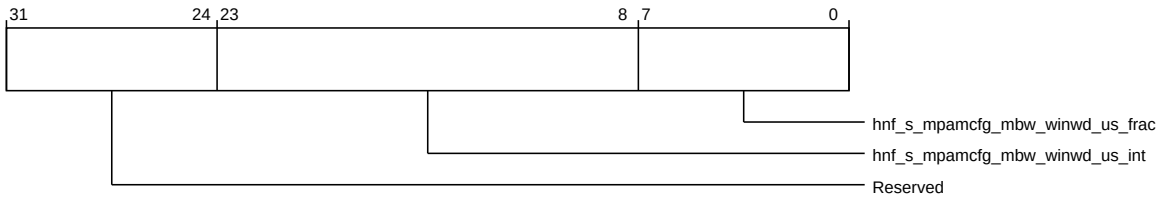
The following table shows the por_hnf_s_mpamcfg_mbw_winwd higher register bit assignments.

Table 5-1344: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_winwd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1331: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_winwd (low)



The following table shows the por_hnf_s_mpamcfg_mbw_winwd lower register bit assignments.

Table 5-1345: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_winwd (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:8	hnf_s_mpamcfg_mbw_winwd_us_int	Memory bandwidth accounting period integer microseconds.	RW	16'h0
7:0	hnf_s_mpamcfg_mbw_winwd_us_frac	Memory bandwidth accounting period fractions of a microsecond.	RW	8'h0

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5.3.12.12 por_hnf_s_mpamcfg_pri

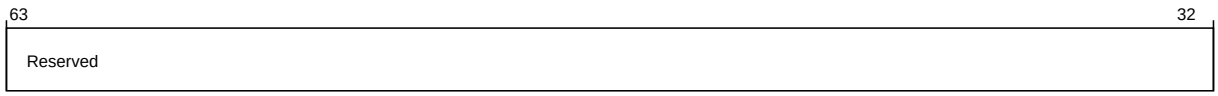
MPAM priority partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1400
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1332: por_hnf_mpam_s_por_hnf_s_mpamcfg_pri (high)



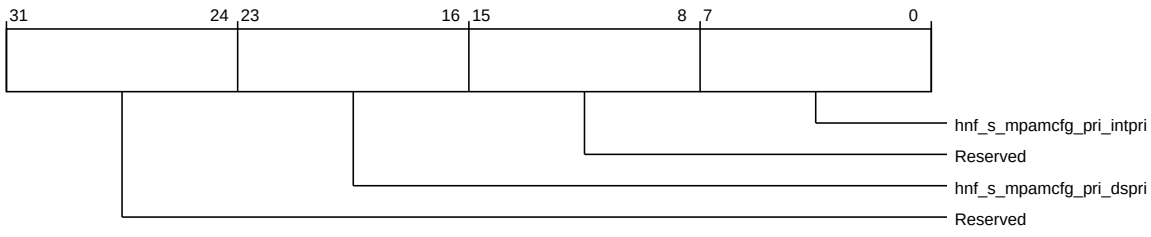
The following table shows the por_hnf_s_mpamcfg_pri higher register bit assignments.

Table 5-1346: por_hnf_mpam_s_por_hnf_s_mpamcfg_pri (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1333: por_hnf_mpam_s_por_hnf_s_mpamcfg_pri (low)



The following table shows the por_hnf_s_mpamcfg_pri lower register bit assignments.

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Table 5-1347: por_hnf_mpam_s_por_hnf_s_mpamcfg_pri (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_s_mpamcfg_pri_dspri	If HAS_DSPRI is 1, this field is a priority value applied to downstream communications from this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_s_mpamcfg_pri_intpri	If HAS_INTPRI is 1, this field is a priority value applied internally inside this memory system component for transactions of the partition selected by MPAMCFG_PART_SEL.	RW	8'h0

5.3.12.13 por_hnf_s_mpamcfg_mbw_prop

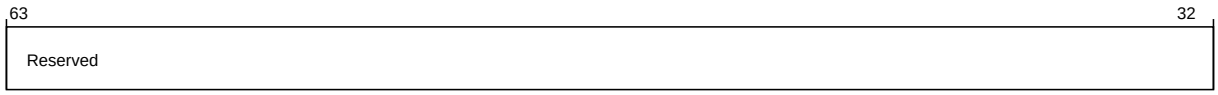
Memory bandwidth proportional stride partitioning configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1500
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1334: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_prop (high)



The following table shows the por_hnf_s_mpamcfg_mbw_prop higher register bit assignments.

Table 5-1348: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_prop (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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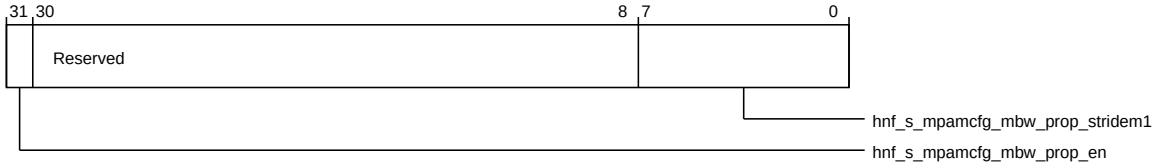
Figure 5-1335: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_prop (low)



The following table shows the por_hnf_s_mpamcfg_mbw_prop lower register bit assignments.

Table 5-1349: por_hnf_mpam_s_por_hnf_s_mpamcfg_mbw_prop (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_mpamcfg_mbw_prop_en	0: The selected partition is not regulated by proportional stride bandwidth partitioning. 1: The selected partition has bandwidth usage regulated by proportional stride bandwidth partitioning as controlled by STRIDEM1.	RW	1'h0
30:8	Reserved	Reserved	RO	-
7:0	hnf_s_mpamcfg_mbw_prop_stridem1	Normalized cost of a bandwidth consumption by the partition. STRIDEM1 is the stride for the partition minus one.	RW	8'h0

5.3.12.14 por_hnf_s_mpamcfg_intpartid

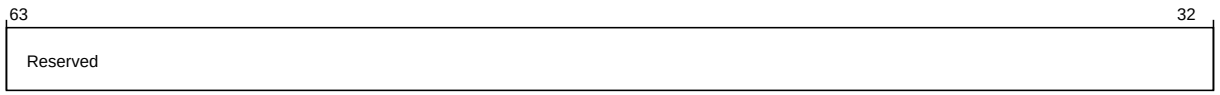
MPAM internal partition narrowing configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1600
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1336: por_hnf_mpam_s_por_hnf_s_mpamcfg_intpartid (high)



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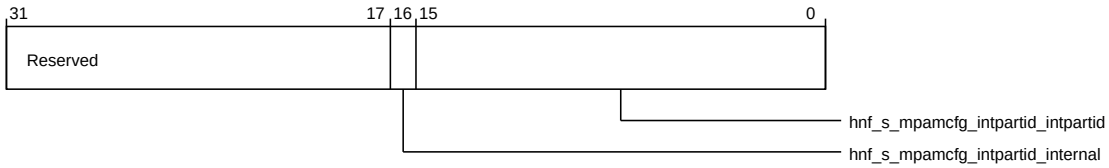
The following table shows the por_hnf_s_mpamcfg_intpartid higher register bit assignments.

Table 5-1350: por_hnf_mpam_s_por_hnf_s_mpamcfg_intpartid (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1337: por_hnf_mpam_s_por_hnf_s_mpamcfg_intpartid (low)



The following table shows the por_hnf_s_mpamcfg_intpartid lower register bit assignments.

Table 5-1351: por_hnf_mpam_s_por_hnf_s_mpamcfg_intpartid (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	hnf_s_mpamcfg_intpartid_internal	This bit must be 1 when written to the register. If written as 0, the write will not update the reqPARTID to intPARTID association.	RW	1'h0
15:0	hnf_s_mpamcfg_intpartid_intpartid	This field contains the intPARTID mapped to the reqPARTID in MPAMCFG_PART_SEL.	RW	16'h0

5.3.12.15 por_hnf_s_msmon_cfg_mon_sel

Memory system performance monitor selection register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1800
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

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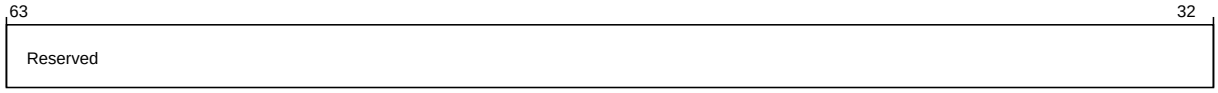
Figure 5-1338: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mon_sel (high)



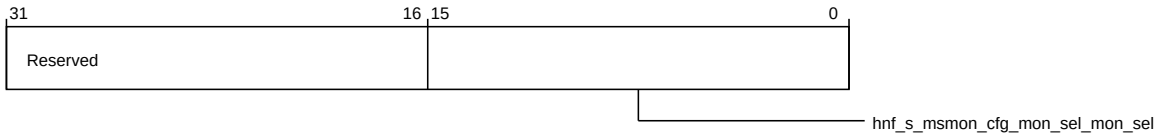
The following table shows the por_hnf_s_msmon_cfg_mon_sel higher register bit assignments.

Table 5-1352: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mon_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1339: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mon_sel (low)



The following table shows the por_hnf_s_msmon_cfg_mon_sel lower register bit assignments.

Table 5-1353: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mon_sel (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_s_msmon_cfg_mon_sel_mon_sel	Selects the performance monitor to configure.	RW	16'h0

5.3.12.16 por_hnf_s_msmon_capt_evnt

Memory system performance monitoring capture event generation register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1808
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

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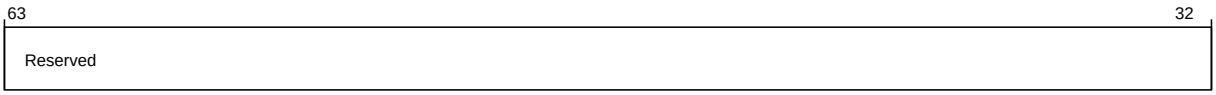
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1340: por_hnf_mpam_s_por_hnf_s_msmon_capt_evnt (high)



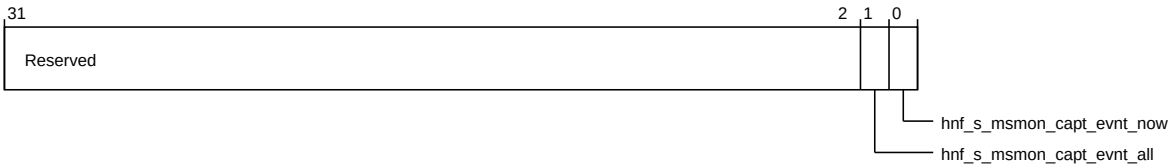
The following table shows the por_hnf_s_msmon_capt_evnt higher register bit assignments.

Table 5-1354: por_hnf_mpam_s_por_hnf_s_msmon_capt_evnt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1341: por_hnf_mpam_s_por_hnf_s_msmon_capt_evnt (low)



The following table shows the por_hnf_s_msmon_capt_evnt lower register bit assignments.

Table 5-1355: por_hnf_mpam_s_por_hnf_s_msmon_capt_evnt (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	hnf_s_msmon_capt_evnt_all	In Secure version, if ALL written as 1 and NOW is also written as 1, signal a capture event to Secure and Non-secure monitors in this memory system component with CAPT_EVNT = 7. If written as 0 and NOW is written as 1, signal a capture event to Secure monitors in this memory system component with CAPT_EVNT = 7. In Non-secure version if NOW is written as 1, signal a capture event to Non-secure monitors in this memory system component with CAPT_EVNT = 7.	RW	1'h0
0	hnf_s_msmon_capt_evnt_now	When written as 1, this bit causes an event to all monitors in this memory system component with CAPT_EVNT set to the value of 7. When this bit is written as 0, no event is signalled.	RW	1'h0

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5.3.12.17 por_hnf_s_msmon_cfg_csu_flt

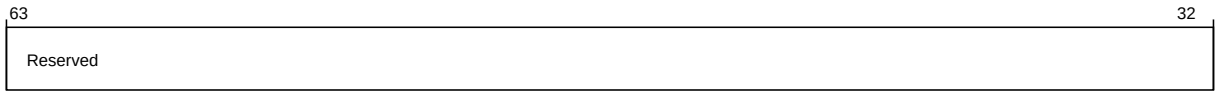
Memory system performance monitor configure cache storage usage monitor filter register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1810
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1342: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_flt (high)



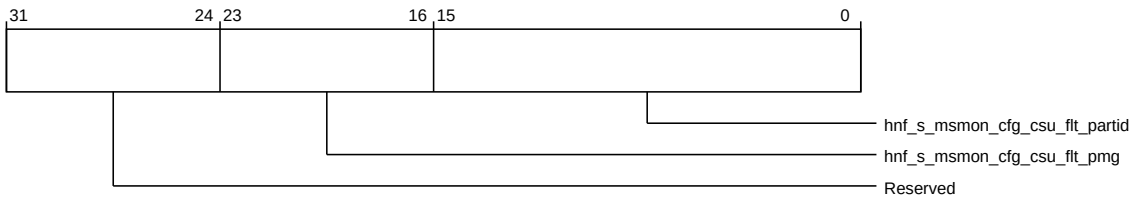
The following table shows the por_hnf_s_msmon_cfg_csu_flt higher register bit assignments.

Table 5-1356: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_flt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1343: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_flt (low)



The following table shows the por_hnf_s_msmon_cfg_csu_flt lower register bit assignments.

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Table 5-1357: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_flt (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_s_msmon_cfg_csu_flt_pmg	Configures the cache storage usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	8'h0
15:0	hnf_s_msmon_cfg_csu_flt_partid	Configures the cache storage usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the storage usage by cache lines labelled with both the configured PARTID and PMG.	RW	16'h0

5.3.12.18 por_hnf_s_msmon_cfg_csu_ctl

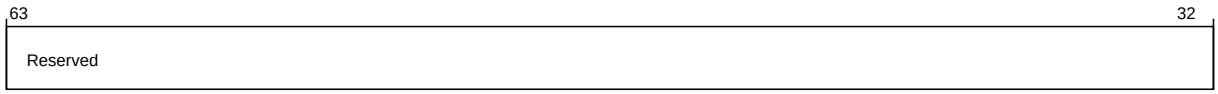
Memory system performance monitor configure cache storage usage monitor control register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1818
Register reset 64'b0000000000000000010011
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1344: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_ctl (high)



The following table shows the por_hnf_s_msmon_cfg_csu_ctl higher register bit assignments.

Table 5-1358: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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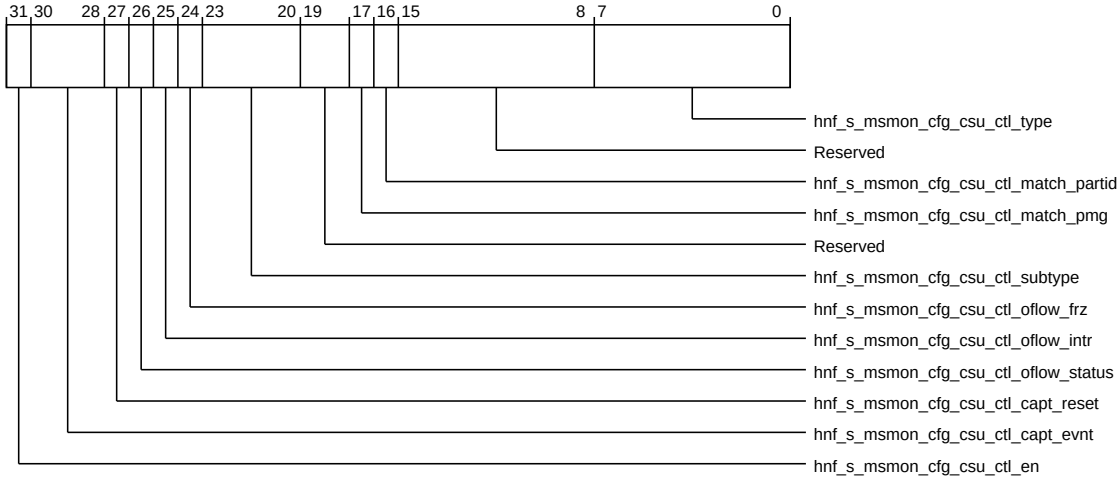
Figure 5-1345: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_ctl (low)



The following table shows the por_hnf_s_msmon_cfg_csu_ctl lower register bit assignments.

Table 5-1359: por_hnf_mpam_s_por_hnf_s_msmon_cfg_csu_ctl (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_cfg_csu_ctl_en	0: The monitor is disabled and must not collect any information. 1: The monitor is enabled to collect information according to its configuration.	RW	1'h0
30:28	hnf_s_msmon_cfg_csu_ctl_capt_evnt	Select the event that triggers capture from the following: 0: No capture event is triggered. 1: External capture event 1 (optional but recommended)	RW	3'h0
27	hnf_s_msmon_cfg_csu_ctl_capt_reset	Capture is not implemented for the CSU monitor type.	RW	1'h0
26	hnf_s_msmon_cfg_csu_ctl_oflow_status	0: No overflow has occurred. 1: At least one overflow has occurred since this bit was last written.	RW	1'h0
25	hnf_s_msmon_cfg_csu_ctl_oflow_intr	0: No interrupt. 1: On overflow, an implementation-specific interrupt is signalled.	RW	1'h0
24	hnf_s_msmon_cfg_csu_ctl_oflow_frz	0: Monitor count wraps on overflow. 1: Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1.	RW	1'h0
23:20	hnf_s_msmon_cfg_csu_ctl_subtype	Not currently used for CSU monitors, but reserved for future use.	RW	4'h0
19:18	Reserved	Reserved	RO	-
17	hnf_s_msmon_cfg_csu_ctl_match_pmg	0: Monitor storage used by all PMG values. 1: Only monitor storage used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0

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Bits	Field name	Description	Type	Reset
16	hnf_s_msmon_cfg_csu_ctl_match_partid	0: Monitor storage used by all PARTIDs. 1: Only monitor storage used with the PARTID matching MSMON_CFG_CSU_FLT.PARTID.	RW	1'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_s_msmon_cfg_csu_ctl_type	Read-only: Constant type indicating the type of the monitor. CSU monitor is TYPE = 0x43.	RW	8'h43

5.3.12.19 por_hnf_s_msmon_cfg_mbwu_flt

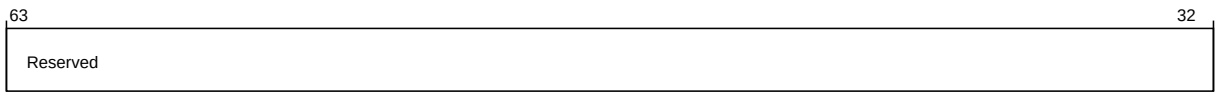
Memory system performance monitor configure memory bandwidth usage monitor filter register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1820
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1346: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_flt (high)



The following table shows the por_hnf_s_msmon_cfg_mbwu_flt higher register bit assignments.

Table 5-1360: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_flt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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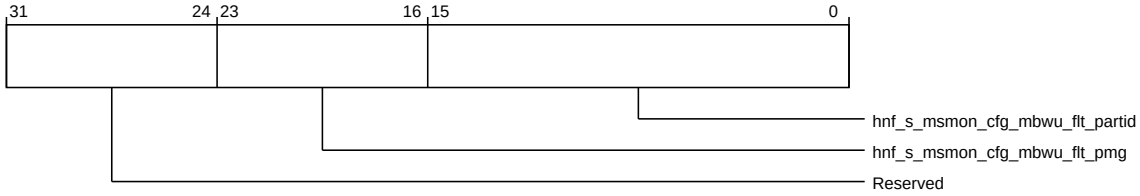
Figure 5-1347: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_flt (low)



The following table shows the por_hnf_s_msmon_cfg_mbwu_flt lower register bit assignments.

Table 5-1361: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_flt (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	hnf_s_msmon_cfg_mbwu_flt_pmg	Configures the memory bandwidth usage performance monitor to a PMG. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	8'h0
15:0	hnf_s_msmon_cfg_mbwu_flt_partid	Configures the memory bandwidth usage performance monitor to a PARTID. The monitor selected by MSMON_CFG_MON_SEL.MON_SEL counts or measures the memory bandwidth used by requests labelled with both the configured PARTID and PMG.	RW	16'h0

5.3.12.20 por_hnf_s_msmon_cfg_mbwu_ctl

Memory system performance monitor configure memory bandwidth usage monitor control register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1828
Register reset 64'b0000000000000000010010
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

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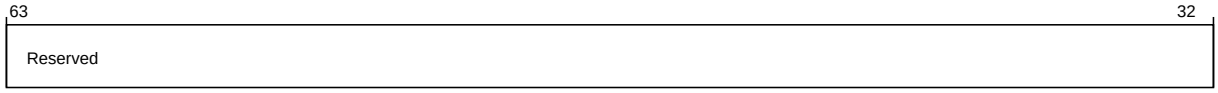
Figure 5-1348: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_ctl (high)



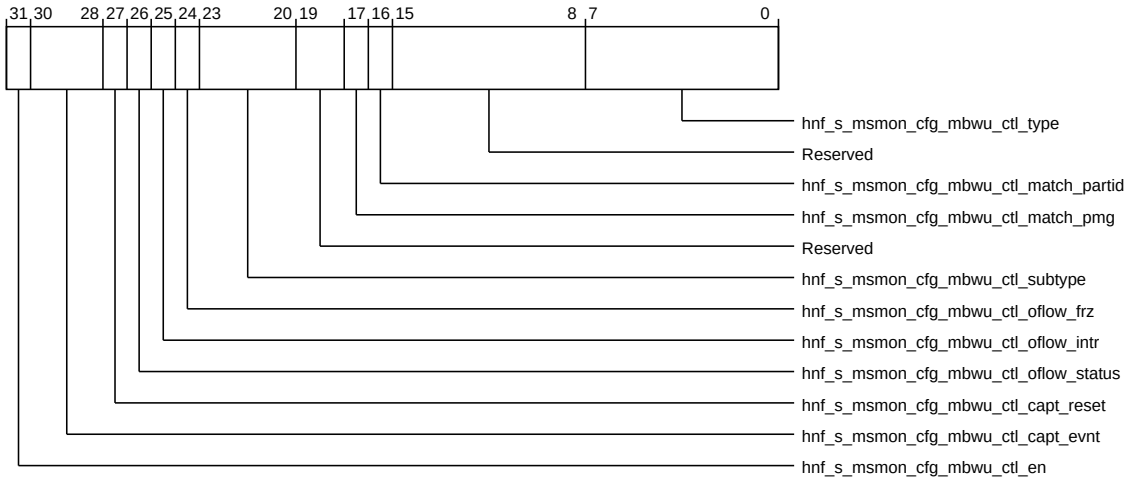
The following table shows the por_hnf_s_msmon_cfg_mbwu_ctl higher register bit assignments.

Table 5-1362: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1349: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_ctl (low)



The following table shows the por_hnf_s_msmon_cfg_mbwu_ctl lower register bit assignments.

Table 5-1363: por_hnf_mpam_s_por_hnf_s_msmon_cfg_mbwu_ctl (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_cfg_mbwu_ctl_en	0: The monitor is disabled and must not collect any information. 1: The monitor is enabled to collect information according to its configuration.	RW	1'h0
30:28	hnf_s_msmon_cfg_mbwu_ctl_capt_evnt	Select the event that triggers capture from the following: 0: No capture event is triggered. 1: External capture event 1 (optional but recommended)	RW	3'h0

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Bits	Field name	Description	Type	Reset
27	hnf_s_msmon_cfg_mbwu_ctl_capt_reset	0: Monitor is not reset on capture. 1: Monitor is reset on capture.	RW	1'h0
26	hnf_s_msmon_cfg_mbwu_ctl_oflow_status	0: No overflow has occurred. 1: At least one overflow has occurred since this bit was last written.	RW	1'h0
25	hnf_s_msmon_cfg_mbwu_ctl_oflow_intr	0: No interrupt. 1: On overflow, an implementation-specific interrupt is signalled.	RW	1'h0
24	hnf_s_msmon_cfg_mbwu_ctl_oflow_frz	0: Monitor count wraps on overflow. 1: Monitor count freezes on overflow. The frozen value may be 0 or another value if the monitor overflowed with an increment larger than 1.	RW	1'h0
23:20	hnf_s_msmon_cfg_mbwu_ctl_subtype	A monitor can have other event matching criteria. The meaning of values in this field varies by monitor type. The MBWU monitor type supports: 0: Do not count any bandwidth. 1: Count bandwidth used by memory reads 2: Count bandwidth used by memory writes 3: Count bandwidth used by memory reads and memory writes All other values are reserved and behaviour of a monitor with SUBTYPE set to one of the reserved values is UNPREDICTABLE.	RW	4'h0
19:18	Reserved	Reserved	RO	-
17	hnf_s_msmon_cfg_mbwu_ctl_match_pmg	0: Monitor bandwidth used by all PMG values. 1: Only monitor bandwidth used with the PMG value matching MSMON_CFG_CSU_FLT.PMG.	RW	1'h0
16	hnf_s_msmon_cfg_mbwu_ctl_match_partid	0: Monitor bandwidth used by all PARTIDs. 1: Only monitor bandwidth used with the PARTID matching MSMON_CFG_MBWU_FLT.PARTID.	RW	1'h0
15:8	Reserved	Reserved	RO	-
7:0	hnf_s_msmon_cfg_mbwu_ctl_type	Read-only: Constant type indicating the type of the monitor. MBWU monitor is TYPE = 0x42.	RW	8'h42

5.3.12.21 por_hnf_s_msmon_csu

Memory system performance monitor cache storage usage monitor register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW

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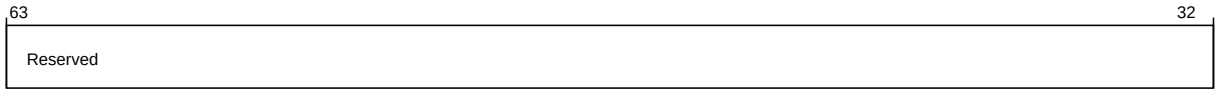
Register width (Bits) 64
Address offset 16'h1840
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1350: por_hnf_mpam_s_por_hnf_s_msmon_csu (high)



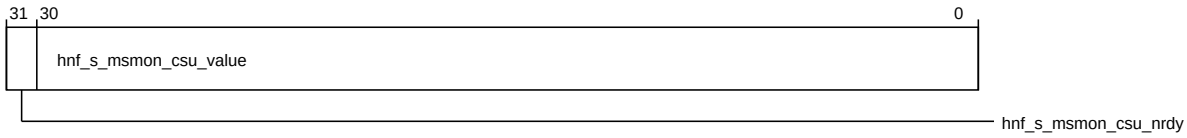
The following table shows the por_hnf_s_msmon_csu higher register bit assignments.

Table 5-1364: por_hnf_mpam_s_por_hnf_s_msmon_csu (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1351: por_hnf_mpam_s_por_hnf_s_msmon_csu (low)



The following table shows the por_hnf_s_msmon_csu lower register bit assignments.

Table 5-1365: por_hnf_mpam_s_por_hnf_s_msmon_csu (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_csu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_s_msmon_csu_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

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5.3.12.22 por_hnf_s_msmon_csu_capture

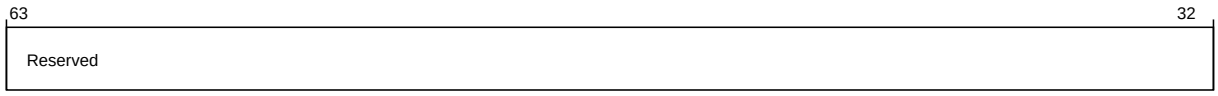
Memory system performance monitor cache storage usage capture register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1848
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1352: por_hnf_mpam_s_por_hnf_s_msmon_csu_capture (high)



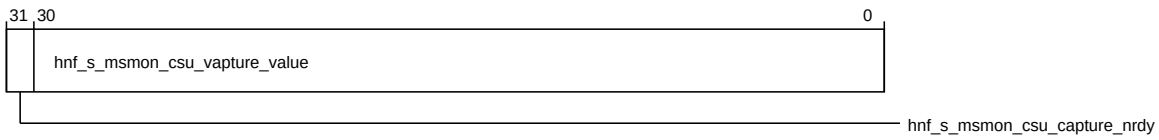
The following table shows the por_hnf_s_msmon_csu_capture higher register bit assignments.

Table 5-1366: por_hnf_mpam_s_por_hnf_s_msmon_csu_capture (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1353: por_hnf_mpam_s_por_hnf_s_msmon_csu_capture (low)



The following table shows the por_hnf_s_msmon_csu_capture lower register bit assignments.

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Table 5-1367: por_hnf_mpam_s_por_hnf_s_msmon_csu_capture (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_csu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_s_msmon_csu_vapture_value	Cache storage usage value if NRDY is 0. Invalid if NRDY is 1. VALUE is the cache storage usage in bytes.	RW	31'h0

5.3.12.23 por_hnf_s_msmon_mbwu

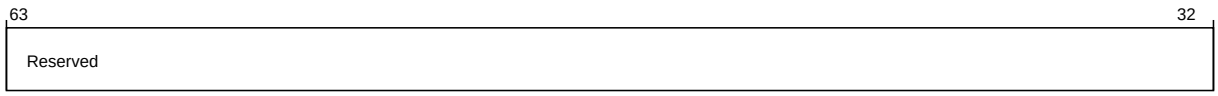
Memory system performance monitor memory bandwidth usage monitor register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1860
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1354: por_hnf_mpam_s_por_hnf_s_msmon_mbwu (high)



The following table shows the por_hnf_s_msmon_mbwu higher register bit assignments.

Table 5-1368: por_hnf_mpam_s_por_hnf_s_msmon_mbwu (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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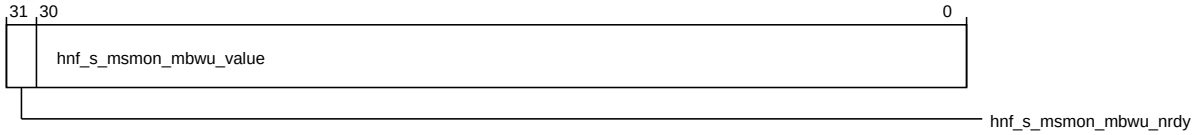
Figure 5-1355: por_hnf_mpam_s_por_hnf_s_msmon_mbwu (low)



The following table shows the por_hnf_s_msmon_mbwu lower register bit assignments.

Table 5-1369: por_hnf_mpam_s_por_hnf_s_msmon_mbwu (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_mbwu_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_s_msmon_mbwu_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

5.3.12.24 por_hnf_s_msmon_mbwu_capture

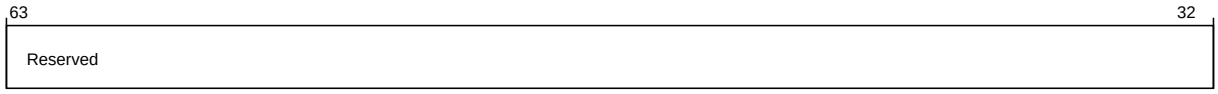
Memory system performance monitor memory bandwidth usage capture register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h1868
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

Figure 5-1356: por_hnf_mpam_s_por_hnf_s_msmon_mbwu_capture (high)



The following table shows the por_hnf_s_msmon_mbwu_capture higher register bit assignments.

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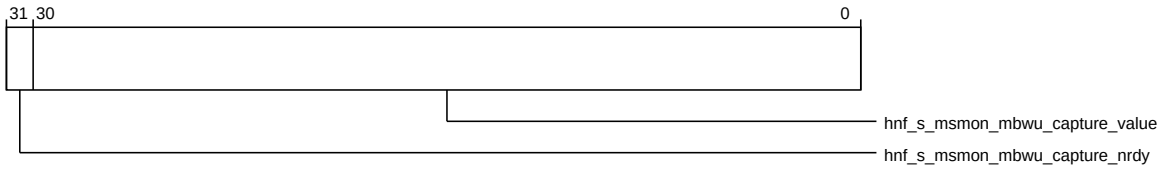
Table 5-1370: por_hnf_mpam_s_por_hnf_s_msmon_mbwu_capture (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1357: por_hnf_mpam_s_por_hnf_s_msmon_mbwu_capture (low)



The following table shows the por_hnf_s_msmon_mbwu_capture lower register bit assignments.

Table 5-1371: por_hnf_mpam_s_por_hnf_s_msmon_mbwu_capture (low)

Bits	Field name	Description	Type	Reset
31	hnf_s_msmon_mbwu_capture_nrdy	Indicates that the monitor does not have accurate data, possibly because insufficient time has elapsed since the monitor was last configured.	RW	1'h0
30:0	hnf_s_msmon_mbwu_capture_value	Memory channel bandwidth value if NRDY is 0. Invalid if NRDY is 1. VALUE is the memory channel bandwidth usage in megabytes.	RW	31'h0

5.3.12.25 por_hnf_s_mpamcfg_cpbm

MPAM cache portion bitmap partition configuration register. This register is a banked seperately for S and NS

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b1111111111111111
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_hnf_mpam_s_secure_register_groups_override.mpam

The following figure shows the higher register bit assignments.

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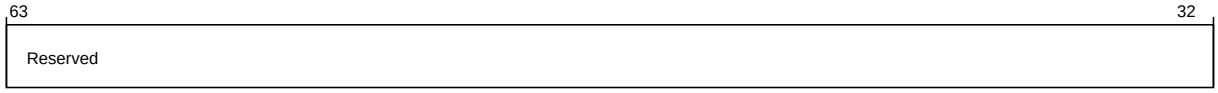
Figure 5-1358: por_hnf_mpam_s_por_hnf_s_mpamcfg_cpbm (high)



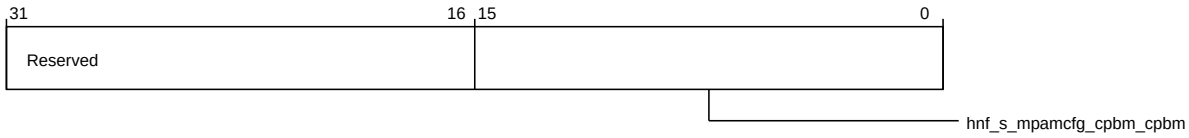
The following table shows the por_hnf_s_mpamcfg_cpbm higher register bit assignments.

Table 5-1372: por_hnf_mpam_s_por_hnf_s_mpamcfg_cpbm (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1359: por_hnf_mpam_s_por_hnf_s_mpamcfg_cpbm (low)



The following table shows the por_hnf_s_mpamcfg_cpbm lower register bit assignments.

Table 5-1373: por_hnf_mpam_s_por_hnf_s_mpamcfg_cpbm (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_s_mpamcfg_cpbm_cpbm	Bitmap of portions of cache capacity allocable by the partition selected by MPAMCFG_PART_SEL. NOTE: CPBM can not be all zeros for any PARTID.	RW	16'hFFFF

5.3.13 MTU register descriptions

This section lists the MTU registers.

5.3.13.1 por_mtu_node_info

Provides component identification information.

Its characteristics are:

Type RO

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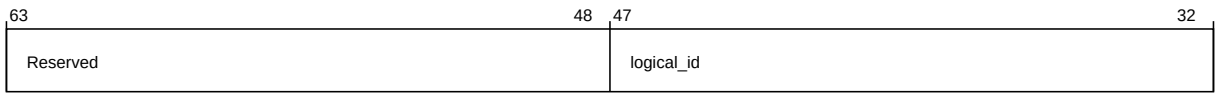
Register width (Bits) 64
Address offset 16'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1360: por_mtu_por_mtu_node_info (high)



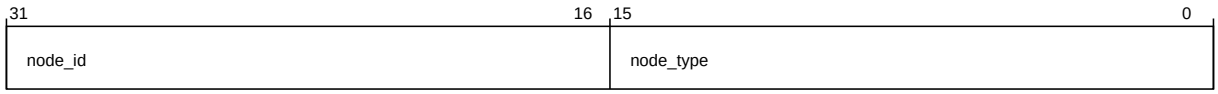
The following table shows the por_mtu_node_info higher register bit assignments.

Table 5-1374: por_mtu_por_mtu_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following figure shows the lower register bit assignments.

Figure 5-1361: por_mtu_por_mtu_node_info (low)



The following table shows the por_mtu_node_info lower register bit assignments.

Table 5-1375: por_mtu_por_mtu_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CI-700 node type identifier	RO	16'h0010

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5.3.13.2 por_mtu_child_info

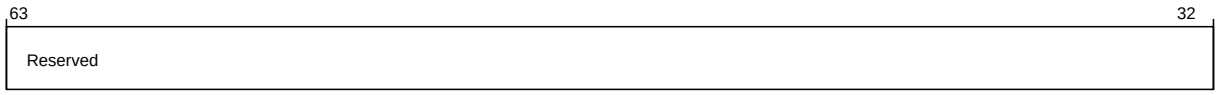
Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1362: por_mtu_por_mtu_child_info (high)



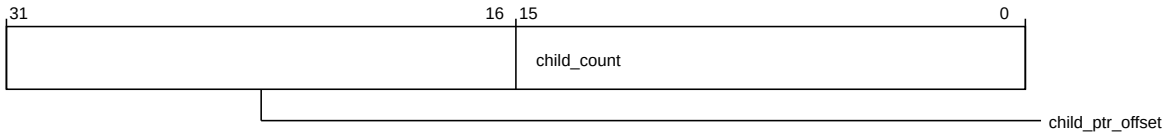
The following table shows the por_mtu_child_info higher register bit assignments.

Table 5-1376: por_mtu_por_mtu_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1363: por_mtu_por_mtu_child_info (low)



The following table shows the por_mtu_child_info lower register bit assignments.

Table 5-1377: por_mtu_por_mtu_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

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5.3.13.3 por_mtu_secure_register_groups_override

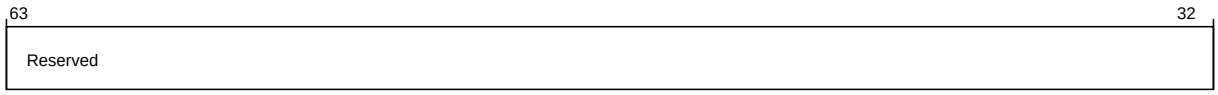
Allows Non-secure access to predefined groups of Secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h980
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1364: por_mtu_por_mtu_secure_register_groups_override (high)



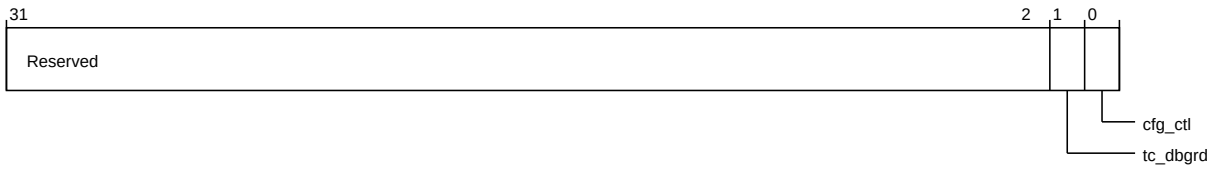
The following table shows the por_mtu_secure_register_groups_override higher register bit assignments.

Table 5-1378: por_mtu_por_mtu_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1365: por_mtu_por_mtu_secure_register_groups_override (low)



The following table shows the por_mtu_secure_register_groups_override lower register bit assignments.

Table 5-1379: por_mtu_por_mtu_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
1	tc_dbgrd	Allows Non-secure access to Secure debug register (por_mtu_cfg_tc_dgbrd)	RW	1'b0
0	cfg_ctl	Allows Non-secure access to Secure configuration control register (por_mtu_cfg_ctl)	RW	1'b0

5.3.13.4 por_mtu_unit_info

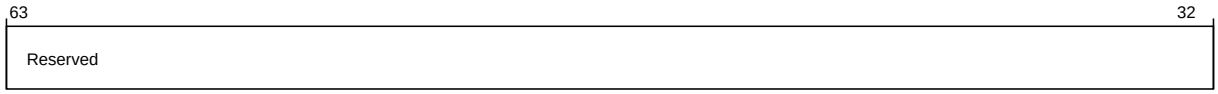
Provides component identification information for MTU.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1366: por_mtu_por_mtu_unit_info (high)



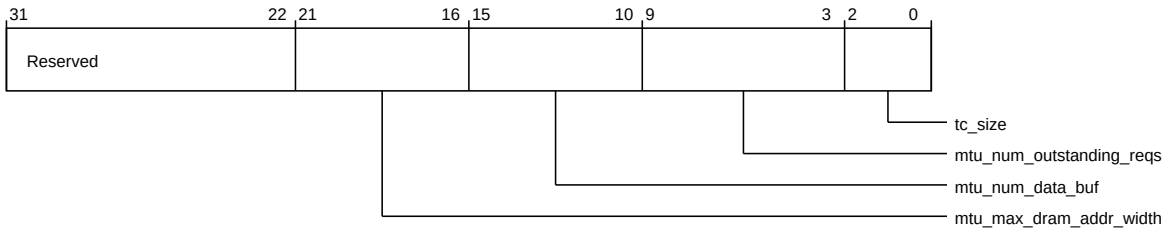
The following table shows the por_mtu_unit_info higher register bit assignments.

Table 5-1380: por_mtu_por_mtu_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1367: por_mtu_por_mtu_unit_info (low)



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The following table shows the por_mtu_unit_info lower register bit assignments.

Table 5-1381: por_mtu_por_mtu_unit_info (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	mtu_max_dram_addr_width	DRAM Addr width	RO	Configuration dependent
15:10	mtu_num_data_buf	Number of data buffers in MTU	RO	Configuration dependent
9:3	mtu_num_outstanding_reqs	Maximum number of outstanding AXI requests from MTU	RO	Configuration dependent
2:0	tc_size	TC size 3'b000: No TC 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1MB 3'b101: 2MB 3'b110: 32KB 3'b111: 64KB	RO	-

5.3.13.5 por_mtu_cfg_ctl

Functions as the configuration control register for MTU.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA00
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override por_mtu_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

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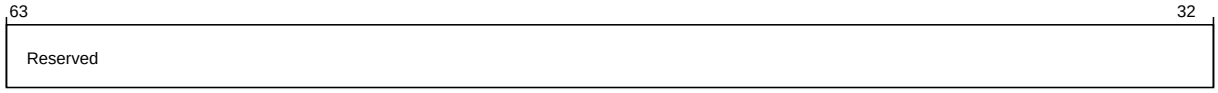
Figure 5-1368: por_mtu_por_mtu_cfg_ctl (high)



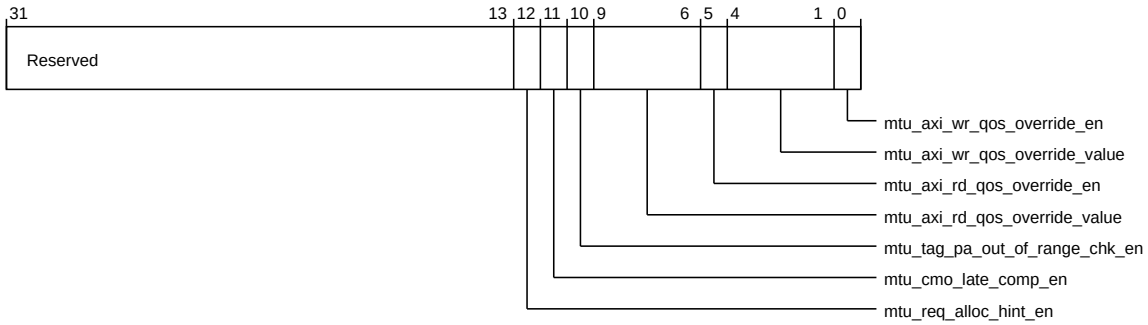
The following table shows the por_mtu_cfg_ctl higher register bit assignments.

Table 5-1382: por_mtu_por_mtu_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1369: por_mtu_por_mtu_cfg_ctl (low)



The following table shows the por_mtu_cfg_ctl lower register bit assignments.

Table 5-1383: por_mtu_por_mtu_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:13	Reserved	Reserved	RO	-
12	mtu_req_alloc_hint_en	Request Alloc Hint is used to determine TC allocation for TC Miss. Note: If this bit is clear, Tags are always allocated in TC. During no_tc_mode, and no_fill_mode; Tags are never allocated.	RW	1'b0
11	mtu_cmo_late_comp_en	Enables CMO completion only when data is flushed out of TC to Memory	RW	1'b0
10	mtu_tag_pa_out_of_range_chk_en	Enables Tag Address Out of Range checking.	RW	1'b0
9:6	mtu_axi_rd_qos_override_value	QoS Override value to be used for all AXI Read requests generated by MTU. This value is used only when axi_rd_qos_override_en is set.	RW	4'b0000
5	mtu_axi_rd_qos_override_en	Enables QoS override for all AXI Read requests.	RW	1'b0
4:1	mtu_axi_wr_qos_override_value	QoS Override value to be used for all AXI Write requests generated by MTU. This value is used only when axi_wr_qos_override_en is set.	RW	4'b0000
0	mtu_axi_wr_qos_override_en	Enables QoS override for all AXI Write requests.	RW	1'b0

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5.3.13.6 por_mtu_aux_ctl

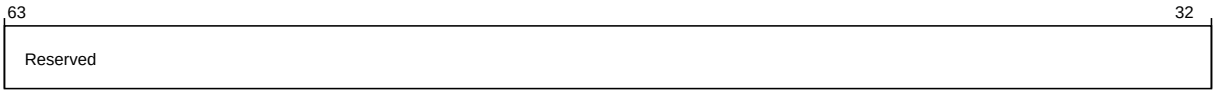
Functions as the auxiliary control register for the MTU

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA08
Register reset 64'b0001000
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

Figure 5-1370: por_mtu_por_mtu_aux_ctl (high)



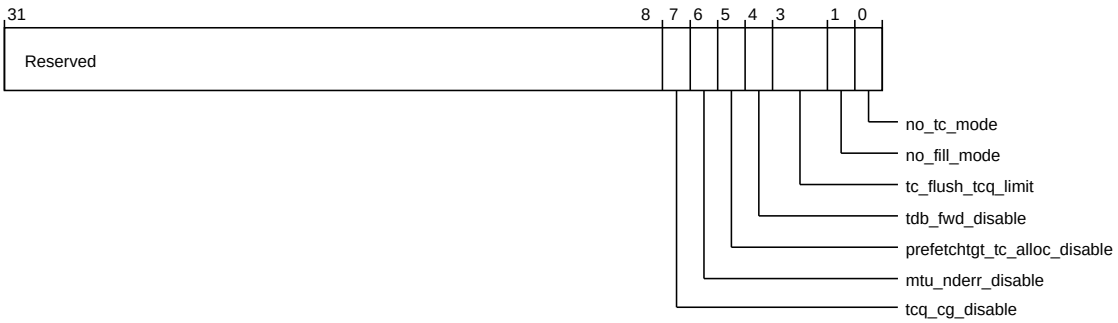
The following table shows the por_mtu_aux_ctl higher register bit assignments.

Table 5-1384: por_mtu_por_mtu_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1371: por_mtu_por_mtu_aux_ctl (low)



The following table shows the por_mtu_aux_ctl lower register bit assignments.

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Table 5-1385: por_mtu_por_mtu_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7	tcq_cg_disable	Disables TCQ architectural clock gates	RW	1'b0
6	mtu_nderr_disable	Disable NDErr from MTU to RN for any Tag errors.	RW	1'b0
5	prefetchtgt_tc_alloc_disable	Do not allocate PrefetchTgt requests in TC.	RW	1'b0
4	tdb_fwd_disable	Disable Tag Data Buffer forwarding from a request to a dependent child request.	RW	1'b0
3:2	tc_flush_tcq_limit	Controls number of TC Flush requests allowed to occupy TCQ entries. 2'b00: TC Flush Requests allowed to take one TCQ entry. 2'b01: TC Flush Requests allowed to take 25% of TCQ entries. 2'b10: TC Flush Requests allowed to take 50% of TCQ entries. 2'b11: TC Flush Requests allowed to take All TCQ entries.	RW	2'b10
1	no_fill_mode	Enables No Fill Mode for Tag Cache. When set, no new lines would be allocated in Tag Cache.	RW	1'b0
0	no_tc_mode	Enables No TC Mode; disables MTU Tag Cache when set.	RW	1'b0

5.3.13.7 por_mtu_tc_flush_pr

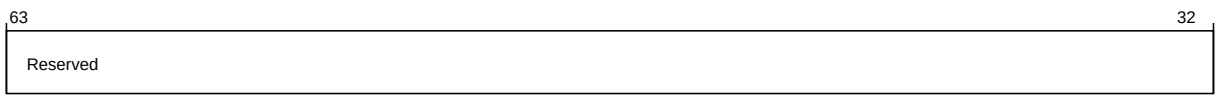
Functions as Tag Cache Flush Policy Register

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA30
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. This register can be modified only with prior written permission from Arm.
Secure group override por_mtu_secure_register_groups_override.cfg_ctl

The following figure shows the higher register bit assignments.

Figure 5-1372: por_mtu_por_mtu_tc_flush_pr (high)



The following table shows the por_mtu_tc_flush_pr higher register bit assignments.

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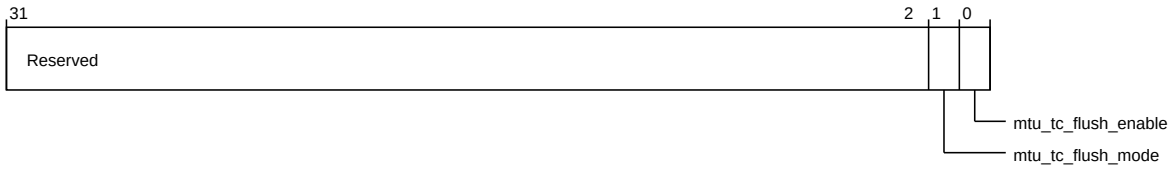
Table 5-1386: por_mtu_por_mtu_tc_flush_pr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1373: por_mtu_por_mtu_tc_flush_pr (low)



The following table shows the por_mtu_tc_flush_pr lower register bit assignments.

Table 5-1387: por_mtu_por_mtu_tc_flush_pr (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	mtu_tc_flush_mode	Tag Cache Flush Mode 1'b0: Clean Invalid. WB dirty data and invalidate local copy in TC. 1'b1: Clean Shared. WB dirty data and keep clean copy in TC.	RW	1'b0
0	mtu_tc_flush_enable	Start Tag Cache Flush	RW	1'b0

5.3.13.8 por_mtu_tc_flush_sr

Functions as Tag Cache Flush Status Register

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hA38
Register reset 64'b0
Usage constraints This register can be modified only with prior written permission from Arm.

The following figure shows the higher register bit assignments.

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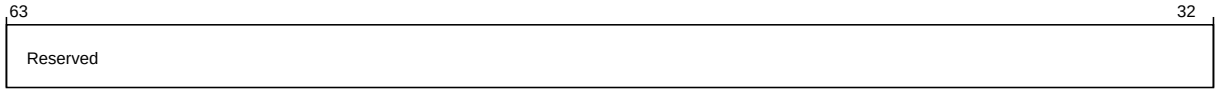
Figure 5-1374: por_mtu_por_mtu_tc_flush_sr (high)



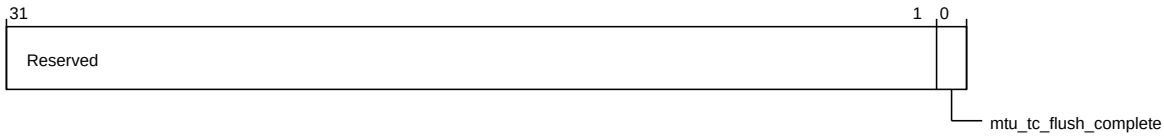
The following table shows the por_mtu_tc_flush_sr higher register bit assignments.

Table 5-1388: por_mtu_por_mtu_tc_flush_sr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1375: por_mtu_por_mtu_tc_flush_sr (low)



The following table shows the por_mtu_tc_flush_sr lower register bit assignments.

Table 5-1389: por_mtu_por_mtu_tc_flush_sr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	mtu_tc_flush_complete	Tag Cache Flush Complete	RO	1'b0

5.3.13.9 por_mtu_tag_addr_ctl

PA to DA address conversion control

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA40
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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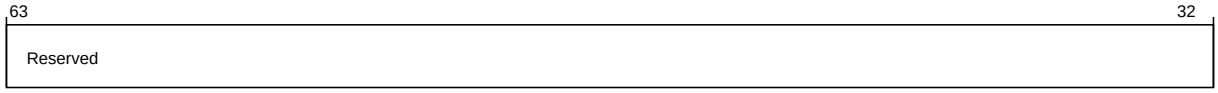
Figure 5-1376: por_mtu_por_mtu_tag_addr_ctl (high)



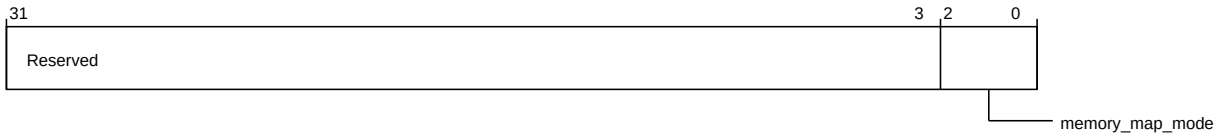
The following table shows the por_mtu_tag_addr_ctl higher register bit assignments.

Table 5-1390: por_mtu_por_mtu_tag_addr_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1377: por_mtu_por_mtu_tag_addr_ctl (low)



The following table shows the por_mtu_tag_addr_ctl lower register bit assignments.

Table 5-1391: por_mtu_por_mtu_tag_addr_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	memory_map_mode	Memory map mode used for translating data physical address to data DRAM address 3'b000: Pass-through 3'b001: PDD 3'b010: Infra 3'b011: Infra with 2 sockets 3'b100: Map Type 0 **Note:** Encoding 3'b100 (Map Type 0) can only be used with prior written permission from Arm.	RW	3'b0

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5.3.13.10 por_mtu_tag_addr_base

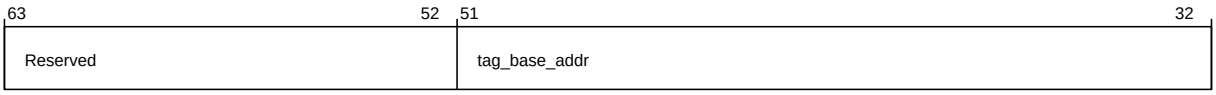
Physical address of tag base

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA48
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1378: por_mtu_por_mtu_tag_addr_base (high)



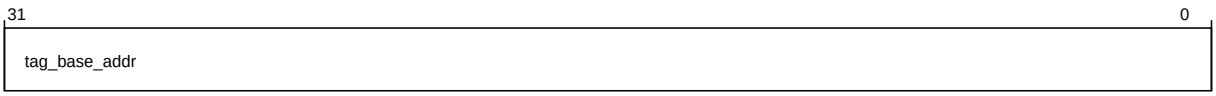
The following table shows the por_mtu_tag_addr_base higher register bit assignments.

Table 5-1392: por_mtu_por_mtu_tag_addr_base (high)

Bits	Field name	Description	Type	Reset
63:52	Reserved	Reserved	RO	-
51:32	tag_base_addr	52-bit Physical address for tag base	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-1379: por_mtu_por_mtu_tag_addr_base (low)



The following table shows the por_mtu_tag_addr_base lower register bit assignments.

Table 5-1393: por_mtu_por_mtu_tag_addr_base (low)

Bits	Field name	Description	Type	Reset
31:0	tag_base_addr	52-bit Physical address for tag base	RW	52'b0

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5.3.13.11 por_mtu_tag_addr_shutter0

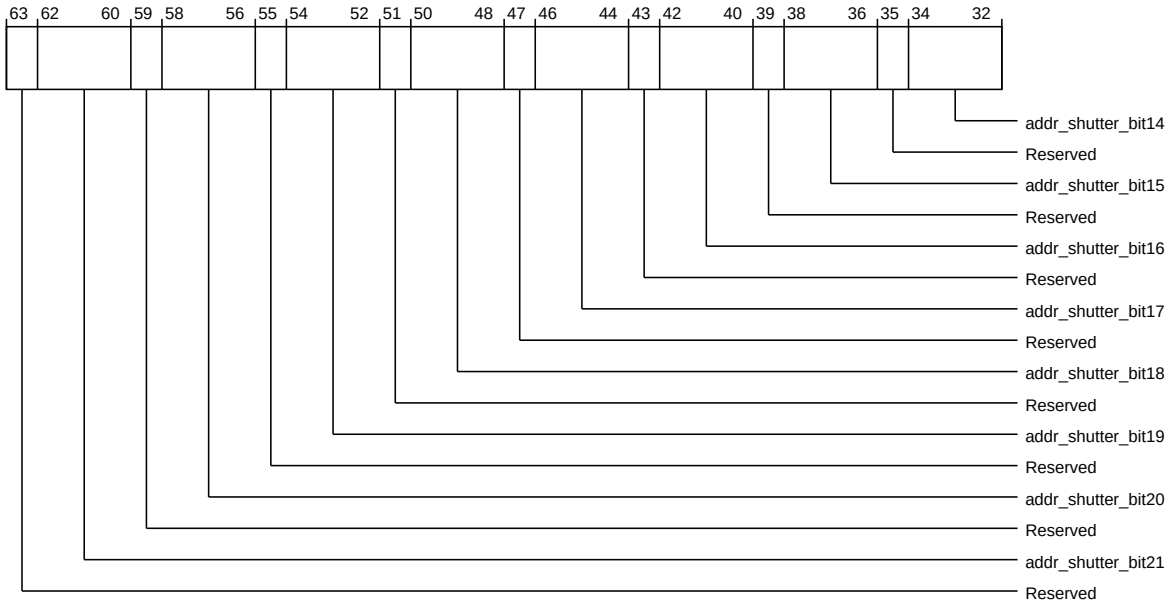
shutter value to generate DRAM address from physical address

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA50
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

Figure 5-1380: por_mtu_por_mtu_tag_addr_shutter0 (high)



The following table shows the por_mtu_tag_addr_shutter0 higher register bit assignments.

Table 5-1394: por_mtu_por_mtu_tag_addr_shutter0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
62:60	addr_shutter_bit21	Program to specify how shuttered address bit 21 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
59	Reserved	Reserved	RO	-
58:56	addr_shutter_bit20	Program to specify how shuttered address bit 20 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
55	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
54:52	addr_shutter_bit19	Program to specify how shuttered address bit 19 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
51	Reserved	Reserved	RO	-
50:48	addr_shutter_bit18	Program to specify how shuttered address bit 18 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
47	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
46:44	addr_shutter_bit17	Program to specify how shuttered address bit 17 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
43	Reserved	Reserved	RO	-
42:40	addr_shutter_bit16	Program to specify how shuttered address bit 16 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
39	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
38:36	addr_shutter_bit15	Program to specify how shuttered address bit 15 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
35	Reserved	Reserved	RO	-
34:32	addr_shutter_bit14	Program to specify how shuttered address bit 14 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

The following figure shows the lower register bit assignments.

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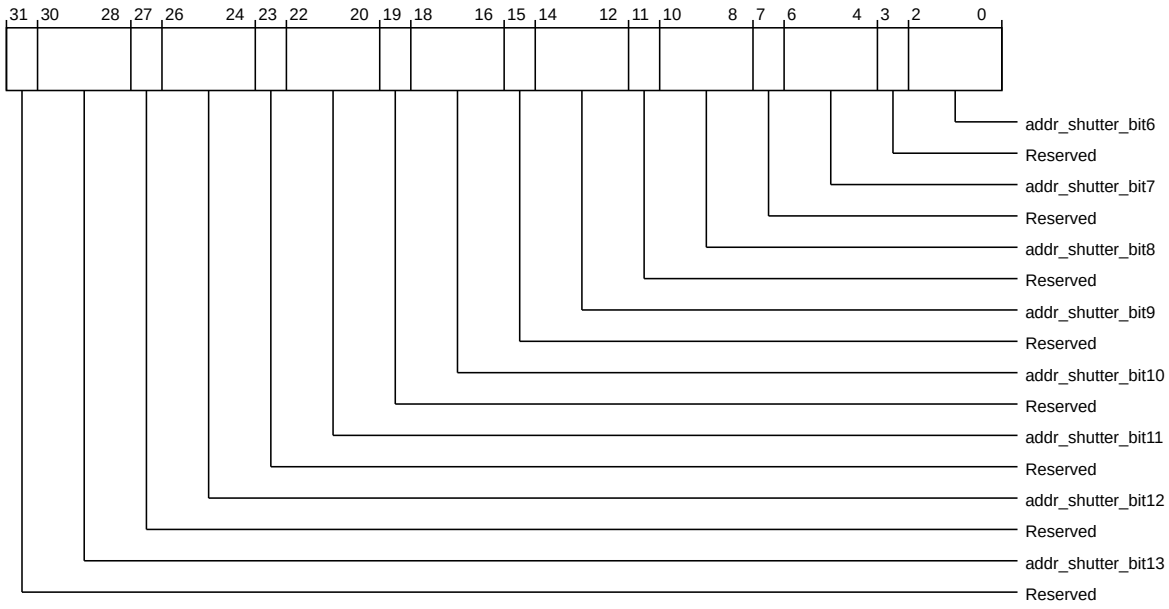
Figure 5-1381: por_mtu_por_mtu_tag_addr_shutter0 (low)



The following table shows the por_mtu_tag_addr_shutter0 lower register bit assignments.

Table 5-1395: por_mtu_por_mtu_tag_addr_shutter0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	addr_shutter_bit13	Program to specify how shuttered address bit 13 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
27	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
26:24	addr_shutter_bit12	Program to specify how shuttered address bit 12 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	addr_shutter_bit11	Program to specify how shuttered address bit 11 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
19	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
18:16	addr_shutter_bit10	Program to specify how shuttered address bit 10 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
15	Reserved	Reserved	RO	-
14:12	addr_shutter_bit9	Program to specify how shuttered address bit 9 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:8	addr_shutter_bit8	Program to specify how shuttered address bit 8 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
7	Reserved	Reserved	RO	-
6:4	addr_shutter_bit7	Program to specify how shuttered address bit 7 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	addr_shutter_bit6	Program to specify how shuttered address bit 6 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

5.3.13.12 por_mtu_tag_addr_shutter1

shutter value to generate DRAM address from physical address

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA58
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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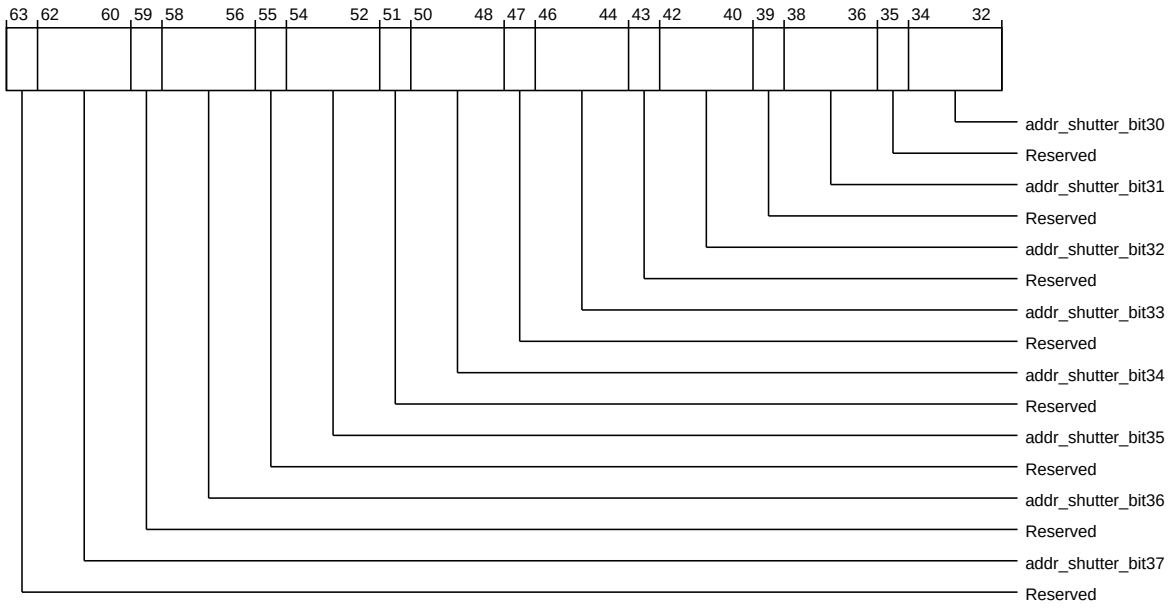
Figure 5-1382: por_mtu_por_mtu_tag_addr_shutter1 (high)



The following table shows the por_mtu_tag_addr_shutter1 higher register bit assignments.

Table 5-1396: por_mtu_por_mtu_tag_addr_shutter1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:60	addr_shutter_bit37	Program to specify how shuttered address bit 37 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
59	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
58:56	addr_shutter_bit36	Program to specify how shuttered address bit 36 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
55	Reserved	Reserved	RO	-
54:52	addr_shutter_bit35	Program to specify how shuttered address bit 35 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
51	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
50:48	addr_shutter_bit34	Program to specify how shuttered address bit 34 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
47	Reserved	Reserved	RO	-
46:44	addr_shutter_bit33	Program to specify how shuttered address bit 33 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6	RW	3'b0
43	Reserved	Reserved	RO	-
42:40	addr_shutter_bit32	Program to specify how shuttered address bit 32 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
39	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
38:36	addr_shutter_bit31	Program to specify how shuttered address bit 31 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
35	Reserved	Reserved	RO	-
34:32	addr_shutter_bit30	Program to specify how shuttered address bit 30 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

The following figure shows the lower register bit assignments.

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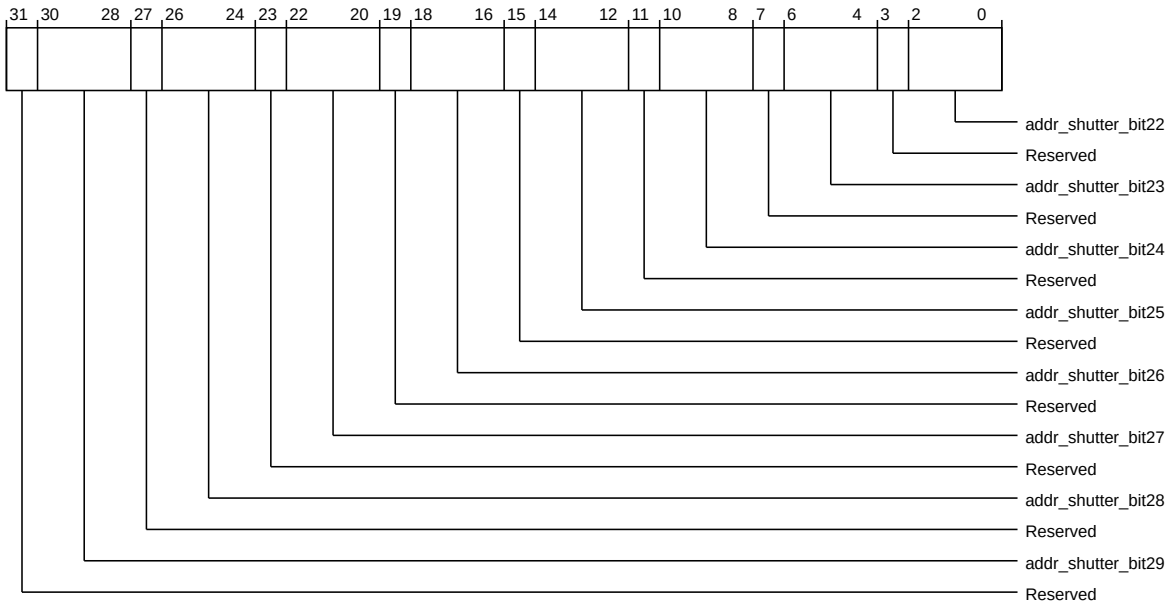
Figure 5-1383: por_mtu_por_mtu_tag_addr_shutter1 (low)



The following table shows the por_mtu_tag_addr_shutter1 lower register bit assignments.

Table 5-1397: por_mtu_por_mtu_tag_addr_shutter1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	addr_shutter_bit29	Program to specify how shuttered address bit 29 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
27	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
26:24	addr_shutter_bit28	Program to specify how shuttered address bit 28 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	addr_shutter_bit27	Program to specify how shuttered address bit 27 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
19	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
18:16	addr_shutter_bit26	Program to specify how shuttered address bit 26 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
15	Reserved	Reserved	RO	-
14:12	addr_shutter_bit25	Program to specify how shuttered address bit 25 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
11	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
10:8	addr_shutter_bit24	Program to specify how shuttered address bit 24 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
7	Reserved	Reserved	RO	-
6:4	addr_shutter_bit23	Program to specify how shuttered address bit 23 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
3	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
2:0	addr_shutter_bit22	Program to specify how shuttered address bit 22 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

5.3.13.13 por_mtu_tag_addr_shutter2

shutter value to generate DRAM address from physical address

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'hA60
Register reset 64'b0
Usage constraints Only accessible by Secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following figure shows the higher register bit assignments.

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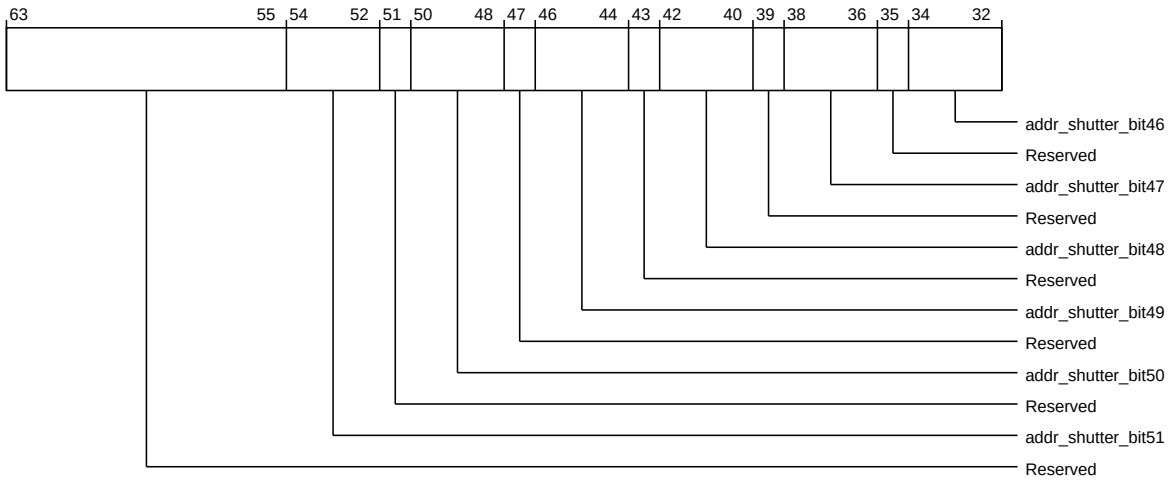
Figure 5-1384: por_mtu_por_mtu_tag_addr_shutter2 (high)



The following table shows the por_mtu_tag_addr_shutter2 higher register bit assignments.

Table 5-1398: por_mtu_por_mtu_tag_addr_shutter2 (high)

Bits	Field name	Description	Type	Reset
63:55	Reserved	Reserved	RO	-
54:52	addr_shutter_bit51	Program to specify how shuttered address bit 51 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
51	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
50:48	addr_shutter_bit50	Program to specify how shuttered address bit 50 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
47	Reserved	Reserved	RO	-
46:44	addr_shutter_bit49	Program to specify how shuttered address bit 49 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
43	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
42:40	addr_shutter_bit48	Program to specify how shuttered address bit 48 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
39	Reserved	Reserved	RO	-
38:36	addr_shutter_bit47	Program to specify how shuttered address bit 47 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
35	Reserved	Reserved	RO	-

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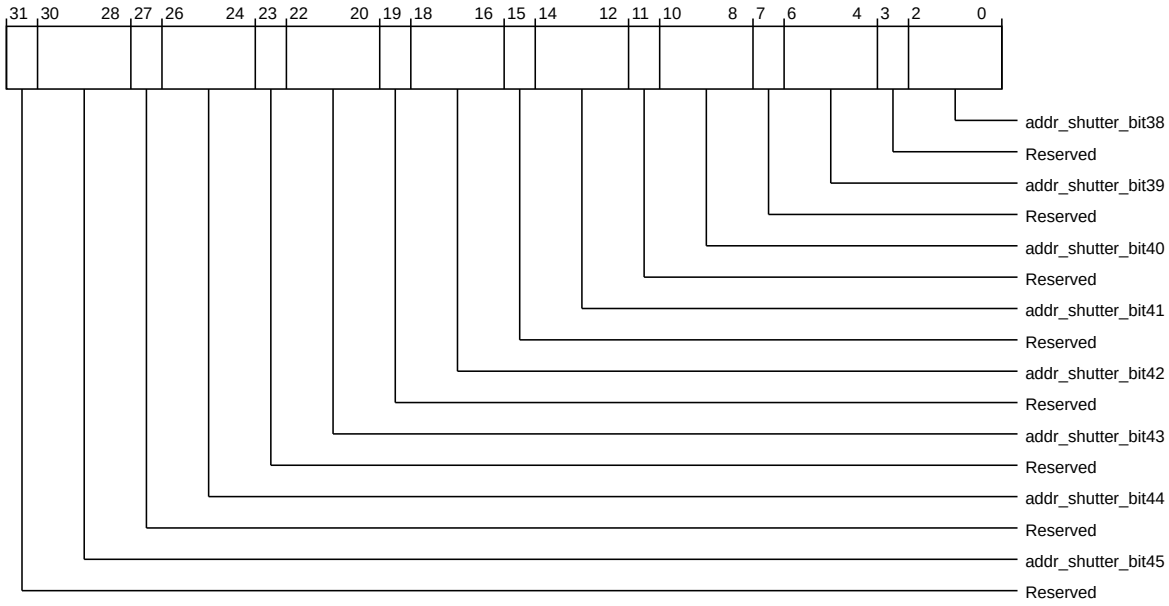
Bits	Field name	Description	Type	Reset
34:32	addr_shutter_bit46	Program to specify how shuttered address bit 46 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

The following figure shows the lower register bit assignments.

Figure 5-1385: por_mtu_por_mtu_tag_addr_shutter2 (low)



The following table shows the por_mtu_tag_addr_shutter2 lower register bit assignments.

Table 5-1399: por_mtu_por_mtu_tag_addr_shutter2 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
30:28	addr_shutter_bit45	Program to specify how shuttered address bit 45 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	addr_shutter_bit44	Program to specify how shuttered address bit 44 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
23	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
22:20	addr_shutter_bit43	Program to specify how shuttered address bit 43 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
19	Reserved	Reserved	RO	-
18:16	addr_shutter_bit42	Program to specify how shuttered address bit 42 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
15	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
14:12	addr_shutter_bit41	Program to specify how shuttered address bit 41 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
11	Reserved	Reserved	RO	-
10:8	addr_shutter_bit40	Program to specify how shuttered address bit 40 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
7	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
6:4	addr_shutter_bit39	Program to specify how shuttered address bit 39 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0
3	Reserved	Reserved	RO	-
2:0	addr_shutter_bit38	Program to specify how shuttered address bit 38 should be driven from post-translation address 3'b000 : pass-through 3'b001 : shift_1 3'b010 : shift_2 3'b011 : shift_3 3'b100 : shift_4 3'b101 : shift_5 3'b110 : shift_6 3'b111 : shift_7	RW	3'b0

5.3.13.14 por_mtu_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3000
Register reset 64'b1001010100001
Usage constraints Only accessible by Secure accesses.

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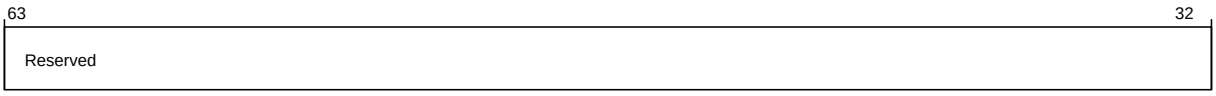
The following figure shows the higher register bit assignments.

Figure 5-1386: por_mtu_por_mtu_errfr (high)



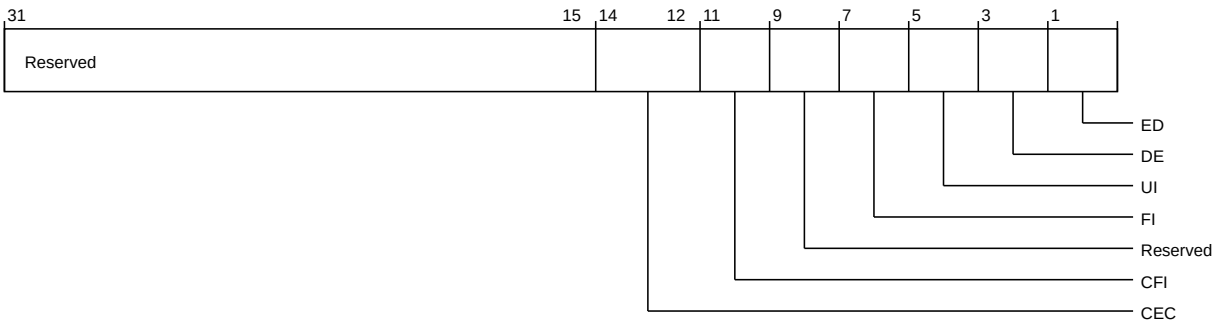
The following table shows the por_mtu_errfr higher register bit assignments.

Table 5-1400: por_mtu_por_mtu_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1387: por_mtu_por_mtu_errfr (low)



The following table shows the por_mtu_errfr lower register bit assignments.

Table 5-1401: por_mtu_por_mtu_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_mtu_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_mtu_errmisc[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10

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Bits	Field name	Description	Type	Reset
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection 2'b00: Feature not supported 2'b01: Feature always enabled 2'b10: Feature is controllable 2'b11: Reserved	RO	2'b01

5.3.13.15 por_mtu_errctlr

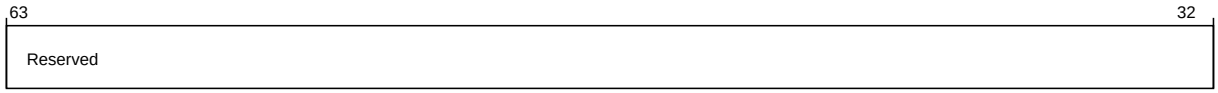
Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3008
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1388: por_mtu_por_mtu_errctlr (high)



The following table shows the por_mtu_errctlr higher register bit assignments.

Table 5-1402: por_mtu_por_mtu_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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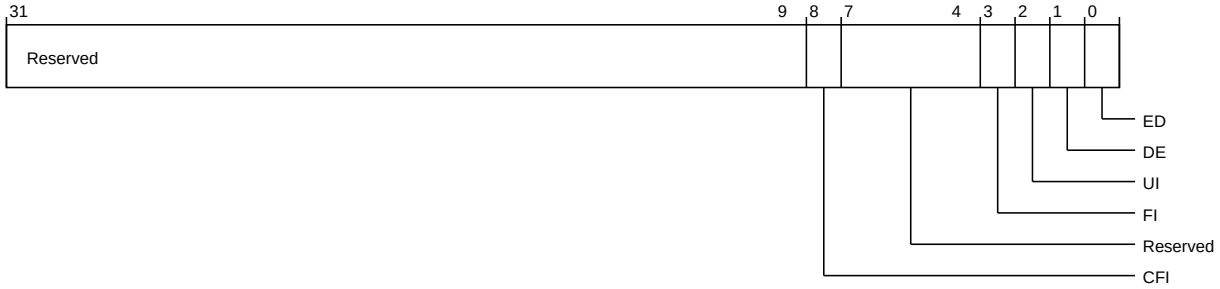
Figure 5-1389: por_mtu_por_mtu_errctlr (low)



The following table shows the por_mtu_errctlr lower register bit assignments.

Table 5-1403: por_mtu_por_mtu_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mtu_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mtu_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mtu_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mtu_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mtu_errfr.ED	RW	1'b0

5.3.13.16 por_mtu_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3010
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

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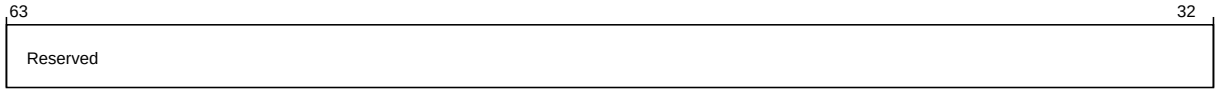
Figure 5-1390: por_mtu_por_mtu_errstatus (high)



The following table shows the por_mtu_errstatus higher register bit assignments.

Table 5-1404: por_mtu_por_mtu_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1391: por_mtu_por_mtu_errstatus (low)



The following table shows the por_mtu_errstatus lower register bit assignments.

Table 5-1405: por_mtu_por_mtu_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_mtu_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0

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Bits	Field name	Description	Type	Reset
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mtu_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.13.17 por_mtu_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3018
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

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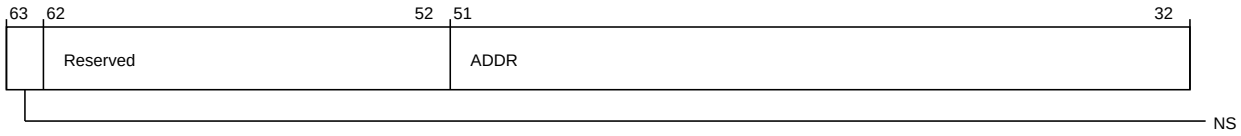
The following figure shows the higher register bit assignments.

Figure 5-1392: por_mtu_por_mtu_erraddr (high)



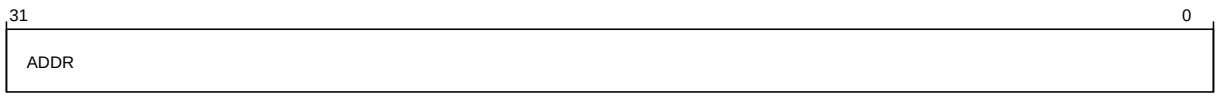
The following table shows the por_mtu_erraddr higher register bit assignments.

Table 5-1406: por_mtu_por_mtu_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_mtu_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address for Data Request (Data PA). Same PA received from HN. Note: For Errors on TC evictions, this represents address that caused eviction. Note: Address is undefined if errmisc.OPTYPE is Other. For most part, these transactions are set/way based and not PA based.	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-1393: por_mtu_por_mtu_erraddr (low)



The following table shows the por_mtu_erraddr lower register bit assignments.

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Table 5-1407: por_mtu_por_mtu_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address for Data Request (Data PA). Same PA received from HN. Note: For Errors on TC evictions, this represents address that caused eviction. Note: Address is undefined if errmisc.OPTYPE is Other. For most part, these transactions are set/way based and not PA based.	RW	52'b0

5.3.13.18 por_mtu_errmisc

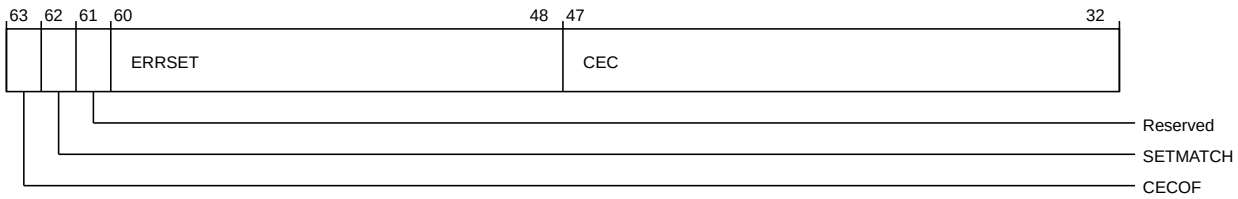
Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3020
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1394: por_mtu_por_mtu_errmisc (high)



The following table shows the por_mtu_errmisc higher register bit assignments.

Table 5-1408: por_mtu_por_mtu_errmisc (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	TC set address for ECC Single bit error	RW	13'b0

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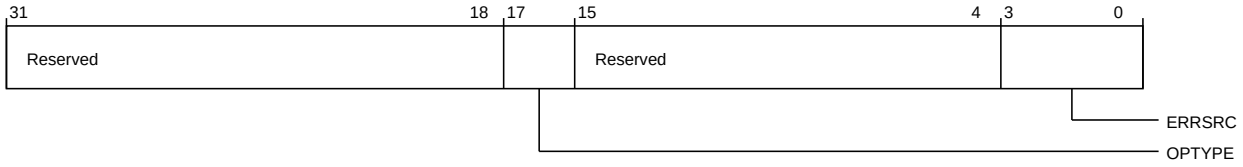
Bits	Field name	Description	Type	Reset
47:32	CEC	Corrected ECC error count	RW	16'b0

The following figure shows the lower register bit assignments.

Figure 5-1395: por_mtu_por_mtu_errmisc (low)



The following table shows the por_mtu_errmisc lower register bit assignments.

Table 5-1409: por_mtu_por_mtu_errmisc (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error opcode type 2'b00: Read Type (RD_NO_SNP, PrefetchTgt) 2'b01: Write (WR_NO_SNP) 2'b10: CMO, WR+CMO 2'b11: Other	RW	2'b00
15:4	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0101: Control single-bit ECC 4'b0110: Control double-bit ECC 4'b1000: AXI AR Slave Error 4'b1001: AXI AR Decode Error 4'b1010: AXI AR Poison Error 4'b1011: AXI AR Datachk Error 4'b1100: AXI W Slave Error 4'b1101: AXI W Decode Error 4'b1110: PA out of range Error	RW	4'b0000

5.3.13.19 por_mtu_errfr_NS

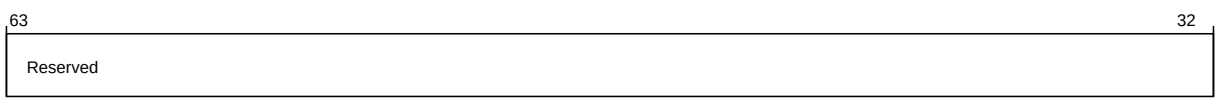
Functions as the Non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'h3100
Register reset 64'b1001010100001
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1396: por_mtu_por_mtu_errfr_ns (high)



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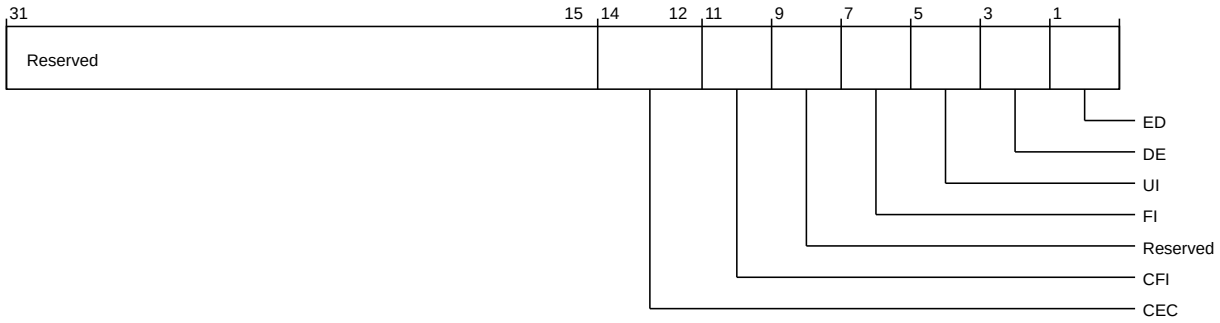
The following table shows the por_mtu_errfr_NS higher register bit assignments.

Table 5-1410: por_mtu_por_mtu_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1397: por_mtu_por_mtu_errfr_ns (low)



The following table shows the por_mtu_errfr_NS lower register bit assignments.

Table 5-1411: por_mtu_por_mtu_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_mtu_errmisc_NS[39:32] 3'b100: Implements 16-bit error counter in por_mtu_errmisc_NS[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection 2'b00: Feature not supported 2'b01: Feature always enabled 2'b10: Feature is controllable 2'b11: Reserved	RO	2'b01

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5.3.13.20 por_mtu_errctlr_NS

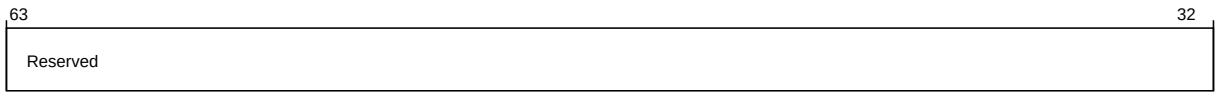
Functions as the Non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1398: por_mtu_por_mtu_errctlr_ns (high)



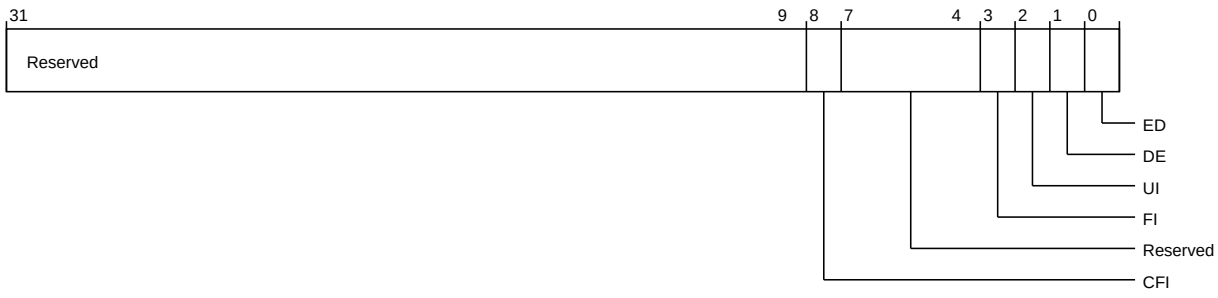
The following table shows the por_mtu_errctlr_NS higher register bit assignments.

Table 5-1412: por_mtu_por_mtu_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1399: por_mtu_por_mtu_errctlr_ns (low)



The following table shows the por_mtu_errctlr_NS lower register bit assignments.

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Table 5-1413: por_mtu_por_mtu_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mtu_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mtu_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mtu_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mtu_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mtu_errfr_NS.ED	RW	1'b0

5.3.13.21 por_mtu_errstatus_NS

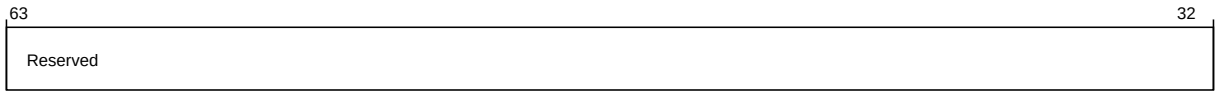
Functions as the Non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 16'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1400: por_mtu_por_mtu_errstatus_ns (high)



The following table shows the por_mtu_errstatus_NS higher register bit assignments.

Table 5-1414: por_mtu_por_mtu_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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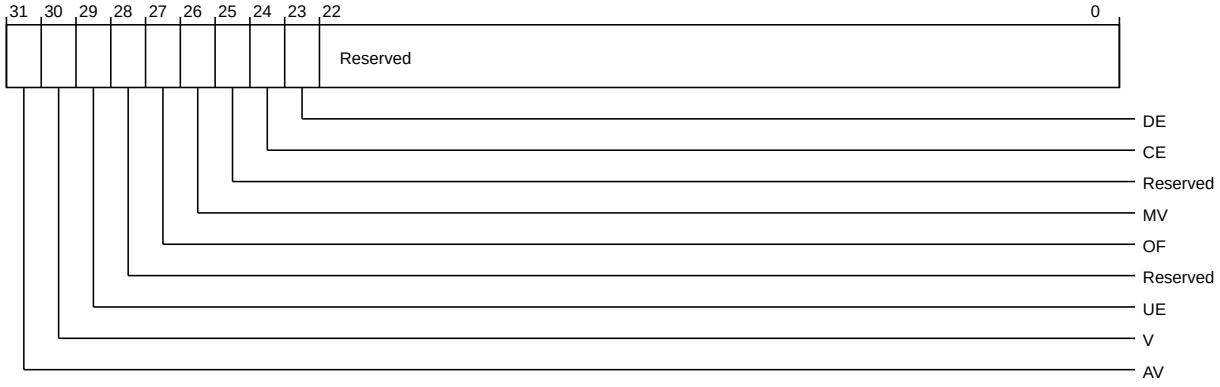
Figure 5-1401: por_mtu_por_mtu_errstatus_ns (low)



The following table shows the por_mtu_errstatus_NS lower register bit assignments.

Table 5-1415: por_mtu_por_mtu_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_mtu_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mtu_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0

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Bits	Field name	Description	Type	Reset
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

5.3.13.22 por_mtu_erraddr_NS

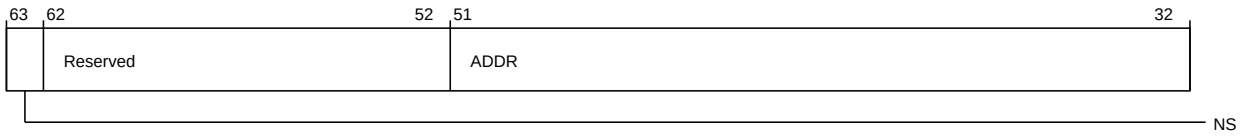
Contains the Non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1402: por_mtu_por_mtu_erraddr_ns (high)



The following table shows the por_mtu_erraddr_NS higher register bit assignments.

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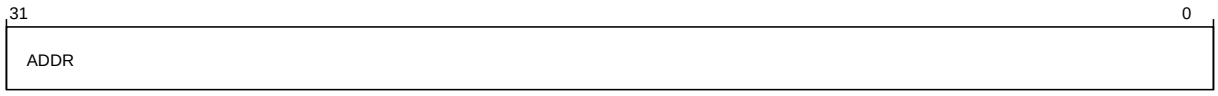
Table 5-1416: por_mtu_por_mtu_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_mtu_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:52	Reserved	Reserved	RO	-
51:32	ADDR	Transaction address for Data Request (Data PA). Same PA received from HN. Note: For Errors on TC evictions, this represents address that caused eviction. Note: Address is undefined if errmisc.OPTYPE is Other. For most part, these transactions are set/way based and not PA based.	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-1403: por_mtu_por_mtu_erraddr_ns (low)



The following table shows the por_mtu_erraddr_NS lower register bit assignments.

Table 5-1417: por_mtu_por_mtu_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address for Data Request (Data PA). Same PA received from HN. Note: For Errors on TC evictions, this represents address that caused eviction. Note: Address is undefined if errmisc.OPTYPE is Other. For most part, these transactions are set/way based and not PA based.	RW	52'b0

5.3.13.23 por_mtu_errmisc_NS

Functions as the Non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

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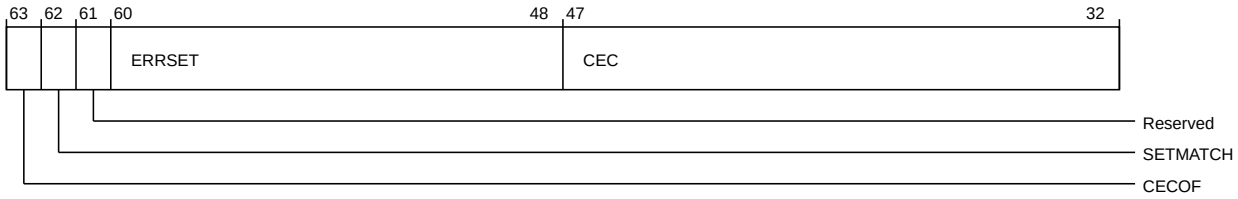
Register width (Bits) 64
Address offset 16'h3120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1404: por_mtu_por_mtu_errmisc_ns (high)



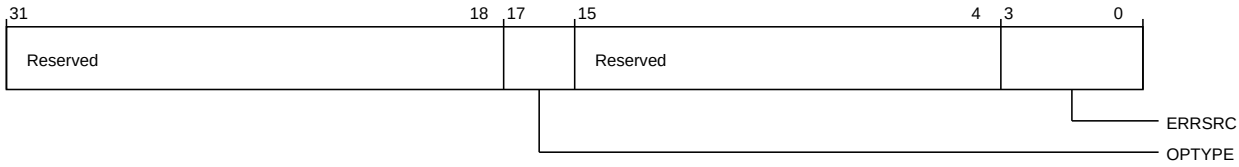
The following table shows the por_mtu_errmisc_NS higher register bit assignments.

Table 5-1418: por_mtu_por_mtu_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	TC set address for ECC Single bit error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following figure shows the lower register bit assignments.

Figure 5-1405: por_mtu_por_mtu_errmisc_ns (low)



The following table shows the por_mtu_errmisc_NS lower register bit assignments.

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Table 5-1419: por_mtu_por_mtu_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error opcode type 2'b00: Read Type (RD_NO_SNP, PrefetchTgt) 2'b01: Write (WR_NO_SNP) 2'b10: CMO, WR+CMO 2'b11: Other op types	RW	2'b00
15:4	Reserved	Reserved	RO	-
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0101: Control single-bit ECC 4'b0110: Control double-bit ECC 4'b1000: AXI AR Slave Error 4'b1001: AXI AR Decode Error 4'b1010: AXI AR Poison Error 4'b1011: AXI AR Datachk Error 4'b1100: AXI W Slave Error 4'b1101: AXI W Decode Error 4'b1110: PA out of range Error	RW	4'b0000

5.3.13.24 por_mtu_err_inj

Enables error injection and setup. When enabled for a given PA and NS bit, MTU returns an error interrupt which emulates a TC double-bit data ECC error. This feature enables software to test the error handler. The error is reported for cacheable read access with Tag Op Transfer for which TC hit. No error is reported for cacheable read access for which TC miss.

Its characteristics are:

Type RW

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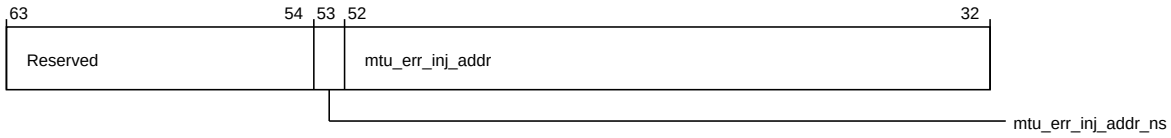
Register width (Bits) 64
Address offset 16'h3030
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.

The following figure shows the higher register bit assignments.

Figure 5-1406: por_mtu_por_mtu_err_inj (high)



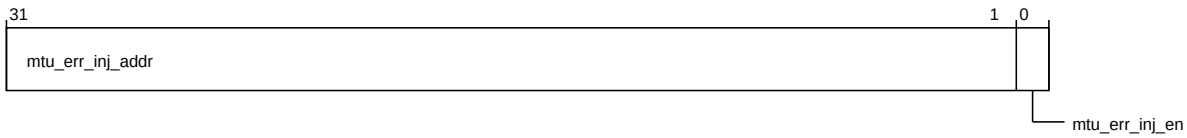
The following table shows the por_mtu_err_inj higher register bit assignments.

Table 5-1420: por_mtu_por_mtu_err_inj (high)

Bits	Field name	Description	Type	Reset
63:54	Reserved	Reserved	RO	-
53	mtu_err_inj_addr_ns	Address NS used to match for error injection	RW	1'b0
52:32	mtu_err_inj_addr	Physical Address used to match for error injection	RW	52'b0

The following figure shows the lower register bit assignments.

Figure 5-1407: por_mtu_por_mtu_err_inj (low)



The following table shows the por_mtu_err_inj lower register bit assignments.

Table 5-1421: por_mtu_por_mtu_err_inj (low)

Bits	Field name	Description	Type	Reset
31:1	mtu_err_inj_addr	Physical Address used to match for error injection	RW	52'b0
0	mtu_err_inj_en	Enables error injection and report	RW	1'b0

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5.3.13.25 por_mtu_cfg_tc_dbgrd

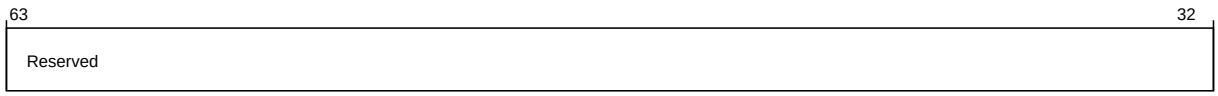
Controls access modes for TC data and TC Control debug read.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 16'hB80
Register reset 64'b1000000000000000000000
Usage constraints Only accessible by Secure accesses.
Secure group override por_mtu_secure_register_groups_override.tc_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-1408: por_mtu_por_mtu_cfg_tc_dbgrd (high)



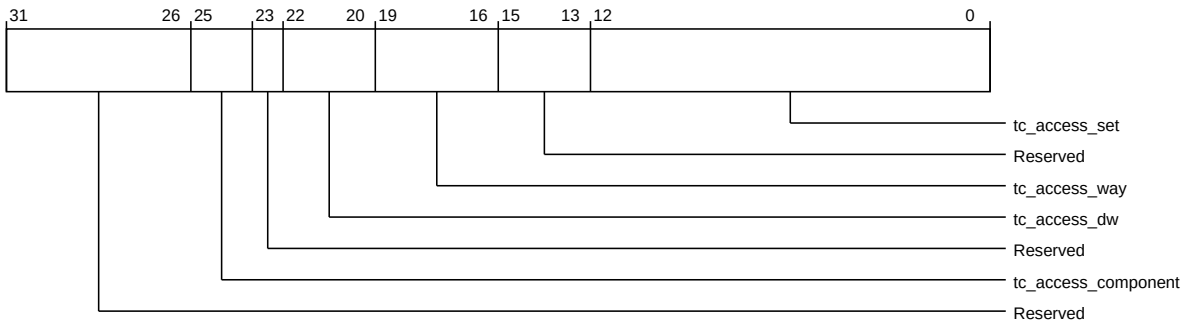
The following table shows the por_mtu_cfg_tc_dbgrd higher register bit assignments.

Table 5-1422: por_mtu_por_mtu_cfg_tc_dbgrd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

Figure 5-1409: por_mtu_por_mtu_cfg_tc_dbgrd (low)



The following table shows the por_mtu_cfg_tc_dbgrd lower register bit assignments.

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Table 5-1423: por_mtu_por_mtu_cfg_tc_dbgrd (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	tc_access_component	Specifies TC Data/Control array debug read 2'b01: TC data read 2'b10: TC control read	WO	2'b10
23	Reserved	Reserved	RO	-
22:20	tc_access_dw	64-bit chunk address for TC data debug read access	WO	3'h0
19:16	tc_access_way	Way address for TC debug read access	WO	4'h0
15:13	Reserved	Reserved	RO	-
12:0	tc_access_set	Set address for TC debug read access	WO	13'h0

5.3.13.26 por_mtu_tc_cache_access_tc_ctl

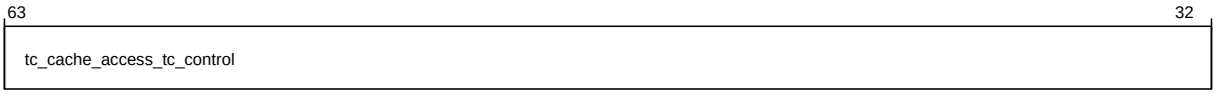
Contains TC Control debug read data bits

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hB88
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mtu_secure_register_groups_override.tc_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-1410: por_mtu_por_mtu_tc_cache_access_tc_ctl (high)



The following table shows the por_mtu_tc_cache_access_tc_ctl higher register bit assignments.

Table 5-1424: por_mtu_por_mtu_tc_cache_access_tc_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	tc_cache_access_tc_control	TC Control debug read data	RO	64'h0

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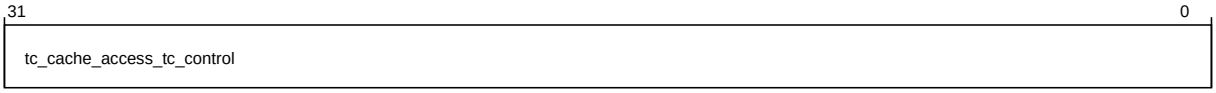
The following figure shows the lower register bit assignments.

Figure 5-1411: por_mtu_por_mtu_tc_cache_access_tc_ctl (low)



The following table shows the por_mtu_tc_cache_access_tc_ctl lower register bit assignments.

Table 5-1425: por_mtu_por_mtu_tc_cache_access_tc_ctl (low)

Bits	Field name	Description	Type	Reset
31:0	tc_cache_access_tc_control	TC Control debug read data	RO	64'h0

5.3.13.27 por_mtu_tc_cache_access_tc_data

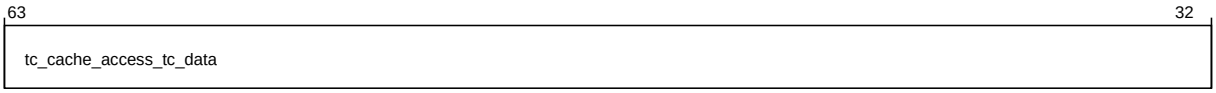
Contains TC data RAM debug read data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 16'hB98
Register reset 64'b0
Usage constraints Only accessible by Secure accesses.
Secure group override por_mtu_secure_register_groups_override.tc_dbgrd

The following figure shows the higher register bit assignments.

Figure 5-1412: por_mtu_por_mtu_tc_cache_access_tc_data (high)



The following table shows the por_mtu_tc_cache_access_tc_data higher register bit assignments.

Table 5-1426: por_mtu_por_mtu_tc_cache_access_tc_data (high)

Bits	Field name	Description	Type	Reset
63:32	tc_cache_access_tc_data	TC data RAM debug read data	RO	64'h0

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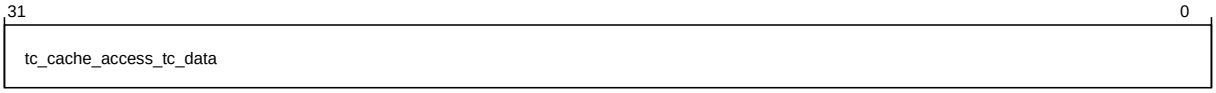
The following figure shows the lower register bit assignments.

Figure 5-1413: por_mtu_por_mtu_tc_cache_access_tc_data (low)



The following table shows the por_mtu_tc_cache_access_tc_data lower register bit assignments.

Table 5-1427: por_mtu_por_mtu_tc_cache_access_tc_data (low)

Bits	Field name	Description	Type	Reset
31:0	tc_cache_access_tc_data	TC data RAM debug read data	RO	64'h0

5.3.13.28 por_mtu_pmu_event_sel

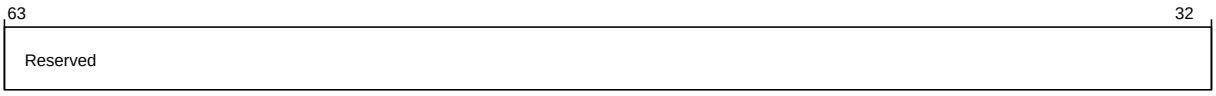
Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 16'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following figure shows the higher register bit assignments.

Figure 5-1414: por_mtu_por_mtu_pmu_event_sel (high)



The following table shows the por_mtu_pmu_event_sel higher register bit assignments.

Table 5-1428: por_mtu_por_mtu_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following figure shows the lower register bit assignments.

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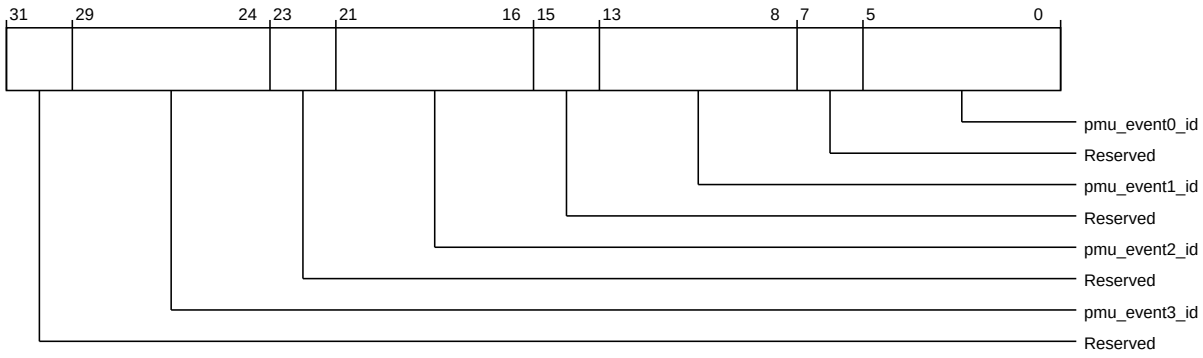
Figure 5-1415: por_mtu_por_mtu_pmu_event_sel (low)



The following table shows the por_mtu_pmu_event_sel lower register bit assignments.

Table 5-1429: por_mtu_por_mtu_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	MTU PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	MTU PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	MTU PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0
7:6	Reserved	Reserved	RO	-

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Bits	Field name	Description	Type	Reset
5:0	pmu_event0_id	MTU PMU Event 0 select 6'h00: No event 6'h01: PMU_MTU_TC_LOOKUP_EVENT; Count total cache lookup requests. 6'h02: PMU_MTU_TC_FILL_EVENT; Count total number of tag cache allocation (Dirty or Clean) requests. 6'h03; PMU_MTU_TC_MISS_EVENT; Count total cache miss responses. 6'h04; PMU_MTU_TDB_FORWARD_EVENT: Count total number of requests that got TDB forwarded data. 6'h05; PMU_MTU_TCQ_HAZARD_EVENT: Count number of incoming requests hazarding againt pending TCQ requests. 6'h06; PMU_MTU_TCQ_RD_ALLOC_EVENT; Count number of read requests allocated in TCQ. This includes Read and Write_Match. 6'h07; PMU_MTU_TCQ_WR_ALLOC_EVENT; Count number of write requests allocated in TCQ. This includes Write_Update. 6'h08; PMU_MTU_TCQ_CMO_ALLOC_EVENT; Count number of CMO requests allocated in TCQ. This includes CMOs and wr+CMO. 6'h09; PMU_MTU_AXI_RD_REQ_EVENT; Count number of read requests sent out on AXI. 6'h0A; PMU_MTU_AXI_WR_REQ_EVENT; Count number of write requests sent out on AXI. 6'h0B; PMU_MTU_TCQ_OCCUPANCY_CNT_OVERFLOW_EVENT; TCQ tracker occupancy count overflow. 6'h0C; PMU_MTU_TDB_OCCUPANCY_CNT_OVERFLOW_EVENT; TDB occupancy count overflow. NOTE: All other encodings are reserved.	RW	6'b0

5.4 CI-700 programming

This section contains CI-700 programming information.

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5.4.1 Boot-time programming sequence

You must use a specific boot-time programming sequence must be used to set up CI-700 correctly. An example sequence is provided, which uses a *System Control Processor* (SCP) to perform the initial boot configuration.

After reset, the following configuration steps must occur before broad access to CI-700 components is available:

1. CI-700 uses a default configuration to access boot flash through the HN-D ACE-Lite master interface and also the configuration registers.
2. An RN-F, or a master that is connected to an RN-I, must then access the configuration registers to configure CI-700. This boot-time configuration must happen before there is broader access to components such as HN-F or SN.

The following example provides more information on the boot process. It assumes an SCP is performing the CI-700 configuration:

1. The SCP boots, either from local memory or through CI-700 memory accesses targeting memory behind the HN-D:
   - All other masters are either held in reset or issue no requests to CI-700 until the boot programming is complete
   - The HN-D is identified through straps on the RN SAM
2. If necessary, the SCP discovers the system
3. The SCP determines the wanted address map and corresponding SAM register values
4. If necessary, the SCP remaps the configuration register space by completing the following steps:
   a. The SCP drains all requests in flight by waiting for their responses
   b. The SCP issues a single 64-bit store to a PERIPHBASE register behind the HN-D. This register would be in logic that is external to CI-700 and an update would cause the signal values on the CFGM_PERIPHBASE input to change
   c. The SCP waits for the response for that store
5. If necessary, the SCP writes to the CI-700 configuration registers to program the SAM for all HN-Fs.
6. The SCP writes to the CI-700 configuration registers to program the SAM for all RNs including the one being used by the SCP.


Note

RN-F ESAM interfaces are active and accept transactions before and during RN SAM programming. Therefore, transactions requiring RN SAM programming must be stalled or prevented until programming is complete.

After programming the SAM for all RNs, the SCP sets a bit that enables use of the programmed address map instead of the default address map. This bit indicates that the SAM setup is complete.

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When the preceding steps are complete, the SCP can make general accesses anywhere in the address space and other masters can begin issuing requests.

5.4.2 Runtime programming requirements

This section describes the requirements for programming during runtime.

The hardware for handling RN membership in the coherence domain or DVM domain has been shifted to the XP to which the RN is attached. A low-level four-phase handshake mechanism, **SYSCOREQ**/**SYSCOACK**, is added to allow quick and local entry to and exit from snoop and DVM domains. No communication with central hardware resources is required. When a block is removed from the coherence or DVM domain, the XP acts as a protocol agent to give a generic response to any snoop or DVM messages.

For legacy devices that do not support the **SYSCOREQ**/**SYSCOACK** mechanism, direct configuration writes to the XP by software can trigger the same mechanism. For more information, see 4.2.8 RN entry to and exit from snoop and DVM domains on page 71.

5.4.3 RN SAM and HN-F SAM programming

You must follow specific programming sequences to set up the RN SAM and HN-F SAM correctly. The register operating modes and encodings you use depend on your system configuration and requirements.

The following HN-F SAM restrictions apply to the MTSX:

- HN-F SAM programming must specify MTSX as a non-hashed target. This means that, MTSX must be a range-based or direct-mapped target of the HN-F.
- All target devices of each SCG must be the same type. In other words, they must be either SBSX or MTSX.
- All MTSX target devices of each SCG must be programmed consistently, including the tag base address.

5.4.3.1 Program the SAM

The SAM must be programmed using a specific sequence. An RN-F or master that is connected to an RN-I must perform this sequence during the configuration of CI-700 at boot.

Before you begin

This sequence is part of the overall CI-700 boot configuration process. There are steps that must occur at boot-time before SAM programming. For more information about the full process, see 5.4.1 Boot-time programming sequence on page 1276.

All **MBISTREQ** and **nMBISTRESET** signals must be disabled during functional operation. The P-Channel, Q-Channel, ACLKEN_M, and ACLKEN_S signals must also all be set correctly for SAM programming.

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About this task

There are several configuration decisions that must be made when setting up the SAM. For more information, see the following sections:

- 4.5 RN SAM on page 84
- 4.6 HN-F SAM on page 98

Procedure

1. Define the following memory map regions:
   - Hashed memory regions, which target HN-Fs. The hashed memory regions can be partitioned into SCGs, if applicable.
   - Non-hashed memory regions, which likely target HN-I or HN-D.
   - Non-hashed regions with HN-I or HN-D mapping. If a single HN-F is the target, HN-F can also be used in non-hashed mode.
   - GIC memory region, if present.
   - HN-F SAM memory regions, if applicable.
   - Mapping of HN-Fs to SN-Fs. This mapping can be direct, 3-SN, or 6-SN mode.
2. Ensure that the memory map meets the following requirements:
   - Non-hashed memory regions must not overlap.
   - Hashed memory regions must not overlap.
   - The memory regions must be size-aligned.
3. Program the following attributes and registers for each HN-F SAM:
   a) Program the appropriate properties for each SN-F ID, according to the features that are supported in the por_hnf_sam_sn_properties register.
   These properties provide the interface width as either 128-bit or 256-bit, CMO support, and PCMO support.
   b) Program the HN-F to SN-F mapping, which depends on the mapping schemes that are used:
      - If the HN-F is directly mapped to an SN-F, program the SN0 target ID and corresponding attributes.
      - If the HN-F is in 3-SN or 6-SN mode, program the following:
        - All SN-F target IDs and the attributes for each SN-F.
        - The mode of operation as 3-SN or 6-SN.
        - The top address bits.
      - If the HN-F uses range-based SN-F partitioning for a particular memory region, program the memory region registers, including the target ID that is associated with each region.
4. Complete the following programming for the RN-F RN SAM:
   a) Program the following attributes and registers for each SCG:
      - Memory region registers.
      - HN-F count registers.
      - HN-F target ID registers.

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- If PrefetchTgt operations are enabled:
  - SN-F target ID registers for SCG.
  - SN-F target ID selection mode for SCG.
  - If 3-SN or 6-SN mode is enabled, program the top address bits.

b) Program the non-hashed memory region registers.
c) Program the non-hashed target ID registers.
d) Program the rnsam_status register to disable the default target ID mode.

5. Complete the following programming for each RN-I RN SAM and RN-D RN SAM:
   a) Program the following registers for each SCG:
      - Memory region registers.
      - HN-F count registers.
      - HN-F target ID registers.
   b) Program the non-hashed memory region registers.
   c) Program the non-hashed target ID registers.
   d) Program the rnsam_status register to disable the default target ID mode.

5.4.3.2 Example memory map programming

This section describes an example memory map and how to program it in the RN SAM and HN-F SAM.

The following figure shows an example memory map with 1024GB addressable size. It is based on the Arm 40-bit proposed address map. It has three separate DRAM regions (in the address ranges from 2-4GB, 34-64GB and 544-1024GB) and four I/O regions, which must be mapped to specific targets. It is assumed that the I/O region 256-512GB is unused and no requests are sent to this address.

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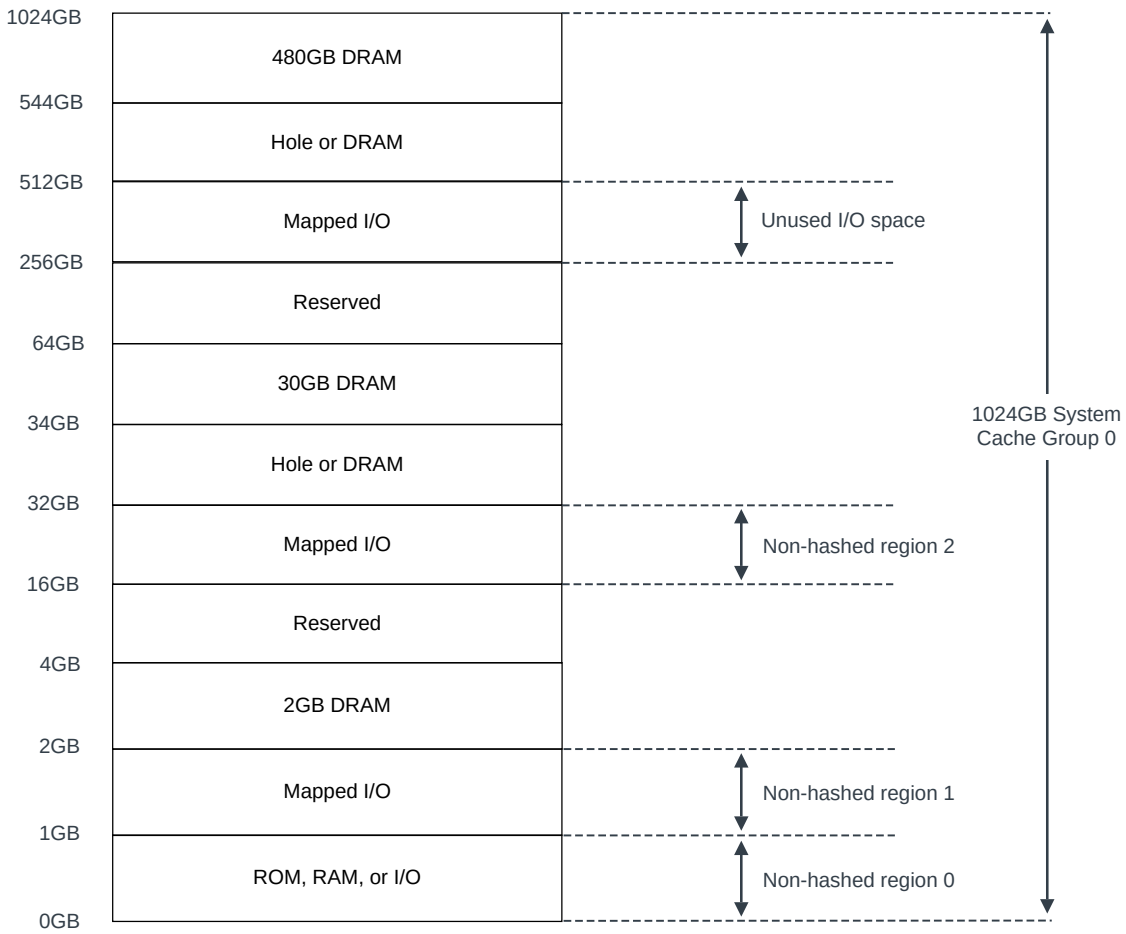
Figure 5-1416: CI-700 example memory map



It is assumed that there are eight HN-Fs in the system and all HN-Fs are being used for one SCG (group 0). To program the RN SAM, follow these steps:

1. Map the full 1024GB memory map to the system cache group. Arm recommends this mapping because DRAM regions are non-contiguous and the entire DRAM space is assigned to one SCG.
2. Carve out each of the non-hashed regions from the full 1024GB memory map as shown in the preceding figure. Assign each non-hashed region to individual non-hashed targets.
3. When the RN SAM programming is done, turn ON the region-based target ID selection by disabling the default mode of the RN SAM.

The following table shows the RN SAM registers and the corresponding programmed values.

Table 5-1430: RN SAM registers and programmed values

Register name	Field name	Value	Description
sys_cache_grp_region0	region0_base_address	0x0_0000	Base address [51:26]

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Register name	Field name	Value	Description
	region0_size	7'b0001110	1024GB size
	region0_target_type	2'b00	HN-F target type
	region0_valid	1'b1	Region 0 is valid.
sys_cache_grp_hn_nodeid_reg0	nodeid_0	<hnf0_node_id>	Physical node IDs of the HN-Fs in the system from HN-F 0 to HN-F 7. If RN-Fs are generating PrefetchTarget operations, then you must program the SN node IDs corresponding to each HN-F in sys_cache_grp_sn_nodeid_regX registers.
	nodeid_1	<hnf1_node_id>	
	nodeid_2	<hnf2_node_id>	
	nodeid_3	<hnf3_node_id>	
sys_cache_grp_hn_nodeid_reg1	nodeid_4	<hnf4_node_id>	
	nodeid_5	<hnf5_node_id>	
	nodeid_6	<hnf6_node_id>	
	nodeid_7	<hnf7_node_id>	
sys_cache_group_hn_count	scg0_num_hnf	0x08	Total of eight HN-Fs in this system cache group.
non_hash_mem_region_reg0	region0_base_address	0x0_0000	1GB from [51:26] 0x0_0000_0000
	region0_size	7'b0000100	1GB size
	region0_target_type	2'b01	HN-I target type
	region0_valid	1'b1	Region 0 is valid.
non_hash_mem_region_reg1	region1_base_address	0x0_0010	1GB region from 0x0_4000_0000
	region1_size	7'b0000100	1GB size
	region1_target_type	2'b01	HN-I target type
	region1_valid	1'b1	Region 1 is valid.
non_hash_mem_region_reg2	region2_base_address	0x0_0100	16GB region from 0x4_0000_0000
	region2_size	7'b0001000	16GB size
	region2_target_type	2'b01	HN-I target type
	region2_valid	1'b1	Region 2 is valid.
non_hash_tgt_nodeid0	nodeid_0	<hni0_node_id>	Node ID of HN-I 0 corresponding to non-hashed region 0
	nodeid_1	<hni1_node_id>	Node ID of HN-I 1 corresponding to non-hashed region 1
	nodeid_2	<hni2_node_id>	Node ID of HN-I 2 corresponding to non-hashed region 2
rnsam_status	nstall_req	1'b1	Unstall any operations that depend on SAM programming.
	default_target	1'b0	Disable default mode and use the programmed ranges for new incoming addresses.

Similarly to RN SAM, HN-F SAM must also be programmed so that it can select the correct SN-F target ID. All HN-F SAMs within SCG 0 must have the same programming, as the following table shows, including the attributes of each SN-F.

Table 5-1431: HN-F programming information

Register name	Field name	Value	Description
por_hnf_sam_control	hn_cfg_sn0_nodeid	<sn0_node_id>	Node ID of SN-F 0
	hn_cfg_sn1_nodeid	<sn1_node_id>	Node ID of SN-F 1
	hn_cfg_sn2_nodeid	<sn2_node_id>	Node ID of SN-F 2

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Register name	Field name	Value	Description
	hn_cfg_three_sn_en	1'b1	Enable 3-SN mode.
	hn_cfg_sam_top_address_bit1	39	Bit 39 of address
	hn_cfg_sam_top_address_bit0	36	Bit 36 of address
	hn_cfg_sam_inv_top_address_bit	1'b1	Invert top address bit.

5.4.4 Program non-XY routing registers

To configure the behavior of the CI-700 non-XY routing feature at boot, you must program the por_mxp_xy_override_sel_* registers for each MXP.

Before you begin

You must ensure that your mesh configuration is free of deadlocks when using the non-XY routing feature. For more information on how to avoid deadlocks when setting up this feature, see 4.11.2.2 Rules for avoiding deadlocks in non-XY routing on page 123.

About this task

When you enable this feature by setting the configuration parameter, the default XY route is applied. The default scheme is active until it is reconfigured by programming the por_mxp_xy_override_sel_* registers.

The following constraints apply to this process:

- A maximum of 16 source-target pairs are supported.
- You must configure all MXPs in your mesh with the same set of <SRCID> and <TGTID> values. These values correspond to the set of source-target pairs that is overridden, so must be identical in all MXPs.
- You must only set the XY override bit in the registers for the overridden MXP or MXPs.
- All devices that are attached to a CAL have the same routing scheme applied. Therefore all devices that are attached to a CAL are either part of the non-XY scheme or not. Selection of partial devices behind a CAL for non-XY routing is not allowed.

Procedure

1. Identify the node source-target pairs and the MXP or MXPs to be overridden.
2. Program the <SRCID> and <TGTID> bits in the relevant por_mxp_xy_override_sel_* registers with the IDs of the chosen source-target pairs.
3. Set the VALID bit in each por_mxp_xy_override_sel_* register to indicate that valid source-target pairs are configured in each register.
4. Repeat steps 1-3 for each MXP in the mesh, ensuring that you program the same values for all MXPs.
5. Set the XY_OVERRIDE_ENABLE bit or bits in any MXPs where you want to override the XY route for a given source-target pair.

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5.4.5 RN-I and HN-I PCIe programming sequence

To ensure proper PCIe functionality, software must complete the following programming before any non-configuration access to the RN-I or HN-I.

About this task

When setting up PCIe RN-Is and HN-Is, the entire PCIe configuration space of an RC must be mapped to a single HN-I address region. HN-I has a SAM that can be configured for up to three address regions. All address regions that are not configured into these three regions are considered to be the default address region. For more information about configuring the HN-I SAM, including example configurations, see 4.7 HN-I SAM on page 107.
If you map an HN-I SAM address region to a PCIe slave, you must map all address regions of that HN-I SAM to PCIe slaves.

Throughout the following procedure, address region X or address region Y can refer to any of the four address regions (0, 1, 2, or 3).

Procedure

1. If there is a PCIe-RC attached to the RN-I, then set the pcie_mstr_present field of the por_rni_cfg_ctl register. This programming indicates that one or more PCIe masters are present upstream.
2. Program the por_hni_sam_addrregion{0,1,2,3}_cfg registers so that the PCIe configuration space falls under one of the four HN-I address regions. This programmed address region is referred to as address region X.
3. Set only one of the following bits in por_hni_sam_addrregionX_cfg for address region X:

   ser_devne_wr

   Set this bit if the PCIe configuration space is marked as the Arm Device-nGnRnE memory type. If this bit is set, HN-I serializes all Device-nGnRnE writes to address region X. The HN-I does not send any other write requests with the same AWID as an outstanding Device-nGnRnE write.

   ser_all_wr

   Set this bit if the PCIe configuration space cannot be marked as Arm memory type of Device-nGnRnE. If this bit is set, HN-I serializes all writes targeting address region X.
4. Clear the pos_early_wr_comp_en bit of the por_hni_sam_addrregionY_cfg register for address region Y.
   Address region Y is the region in which PCIe EP memory space (posted traffic) is programmed. If the pos_early_wr_comp_en bit is cleared, HN-I does not provide early write completions for any write requests targeting address region Y.

5.4.6 MTSX programming

To ensure that the MTSX generates the correct tag addresses, the MTSX registers must be programmed correctly.

Any misprogramming of MTSX registers might cause **UNDEFINED** behavior.

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5.4.6.1 Programming MTU tag address generation registers

There are specific programming requirements that you must follow so the MTSX can determine the tag address according to the PA of the request.

You must program all address generation registers consistently with the associated memory controller in the system.

The following registers must be programmed for the MTSX to determine the tag address according to the PA of the request:

- mtu_tag_addr_ctl
- mtu_tag_addr_base
- mtu_tag_addr_shutter{0-2}

mtu_tag_addr_ctl

The mtu_tag_addr_ctl register indicates which memory map mode is being used. A slave that is downstream of MTSX might use a contiguous memory map. However, the regions that the slave serves might be non-contiguous in the CI-700 SAM. Therefore, the MTSX can use various translation modes to map system addresses to addresses in the memory map of the downstream slave. The memory map mode determines the mapping structure that the MTSX uses to translate these addresses. MTSX supports five memory map modes, which are defined in 5.3.13.9 por_mtu_tag_addr_ctl on page 1223.

The following table shows the five supported memory map modes.

Table 5-1432: MTSX memory map modes

Memory map mode	por_mtu_tag_addr_ctl.memory_map_mode encoding	Description
Pass-through	`0b000`	Used when the system address maps directly to the downstream slave without any translation.
PDD translation	`0b001`	Used with the PDD memory map. For more information, see Figure 5-1417: PDD memory map on page 1286 and the *Principles of Arm® Memory Maps White Paper*.
Alternate translation	`0b010`	Used with a memory map that is a mixture of a flat (non-translated) memory map and a PDD-translated memory map. It has a DRAM region between 2GB and 4GB for compatibility with legacy 32-bit peripherals, but is flat for the rest of the map. For more information, see Figure 5-1418: Alternate translation mode memory map on page 1287.
Alternate translation with multiple sockets	`0b011`	Used with a memory map that is similar to one for which alternate translation mode is used. However, if the MTSX receives an address above 4TB, then it simply drops the most significant bits over 4TB. In this mode, MTSX cannot differentiate between an access to `0x700_0000_0000` and an access to `0x300_0000_0000`. Therefore, the system must prevent such accesses. For more information, see Figure 5-1419: Alternate translation with multiple sockets mode memory map on page 1288.

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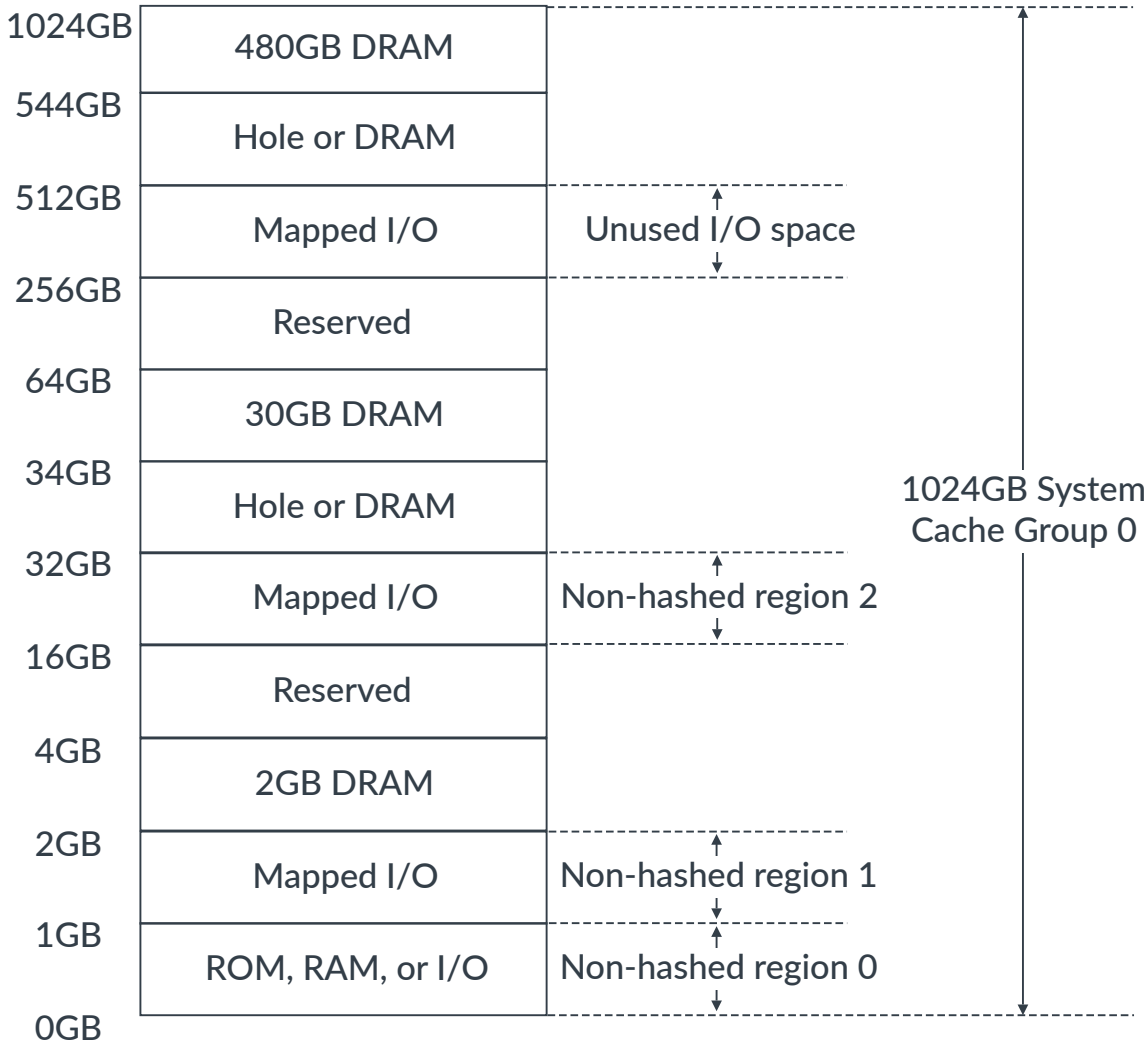
Memory map mode	por_mtu_tag_addr_ctl.memory_map_mode encoding	Description
Map type 0 mode	0b100	For more information, see Figure 5-1420: Map type 0 mode memory map on page 1289 **Note:** You can only use the map_type_0 encoding with prior written permission from Arm®.

The following figure shows the PDD memory map, which the MTSX can convert into a contiguous address map using the PDD translation mode.

Figure 5-1417: PDD memory map



The following figure shows the memory map that is used with the alternate translation memory map mode.

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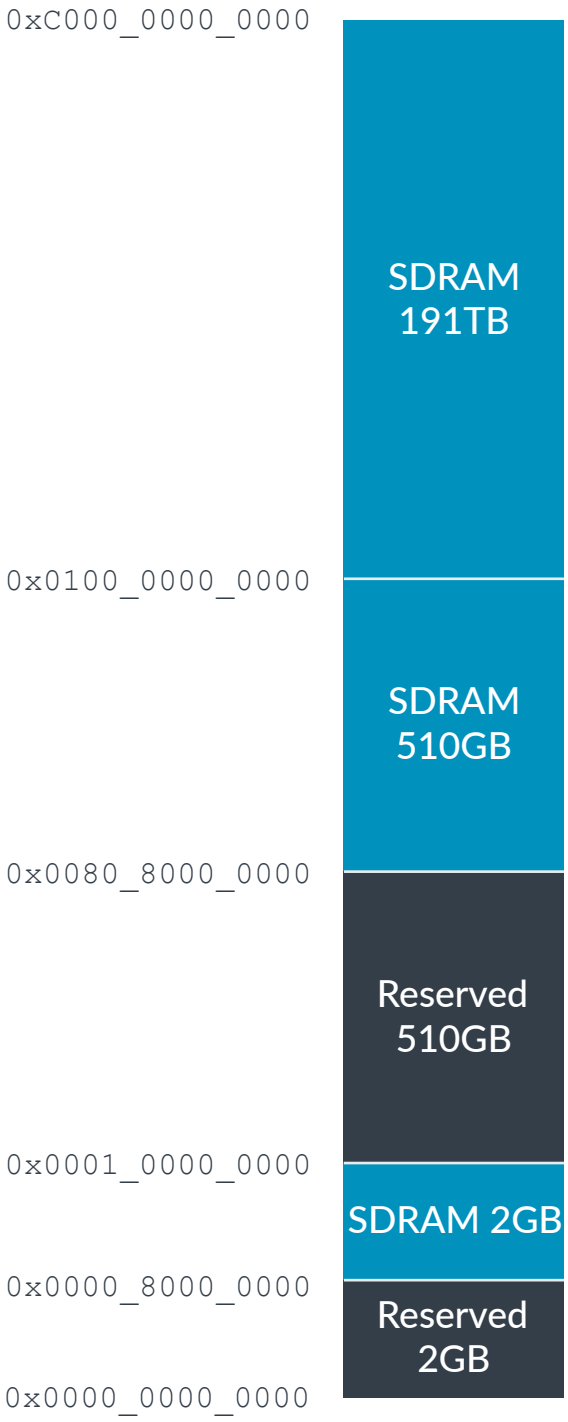
Figure 5-1418: Alternate translation mode memory map



The following figure shows the memory map that is used with the alternate translation with multiple sockets memory map mode.

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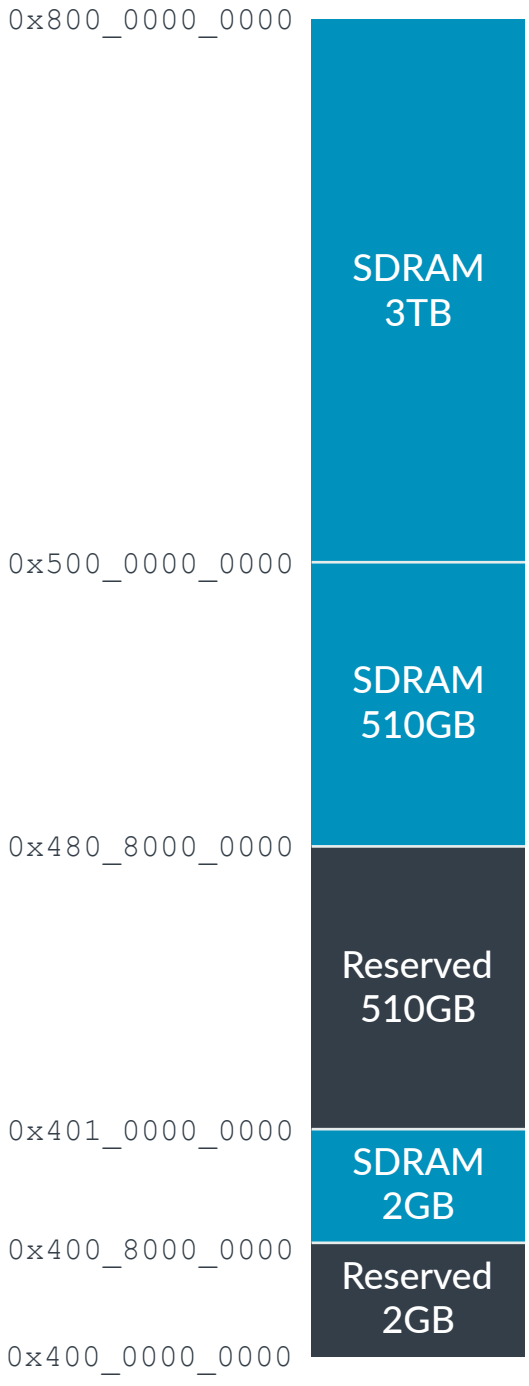
Figure 5-1419: Alternate translation with multiple sockets mode memory map



The following figure shows the memory map that is used with the map type 0 memory map mode.

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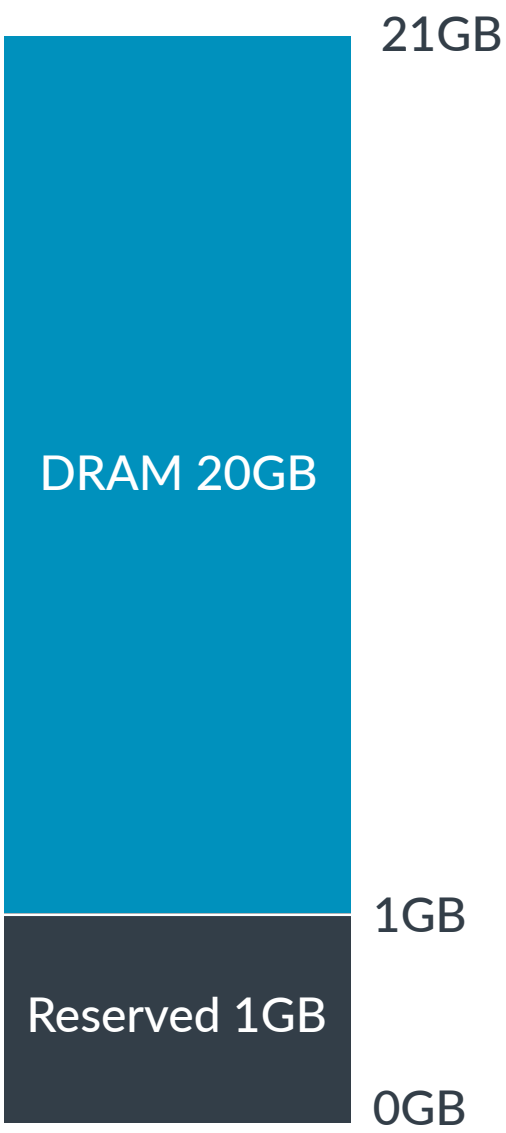
Figure 5-1420: Map type 0 mode memory map



mtu_tag_addr_base

The mtu_tag_addr_base register indicates the starting PA of the tag space in local DRAM, as shown in the following figure.

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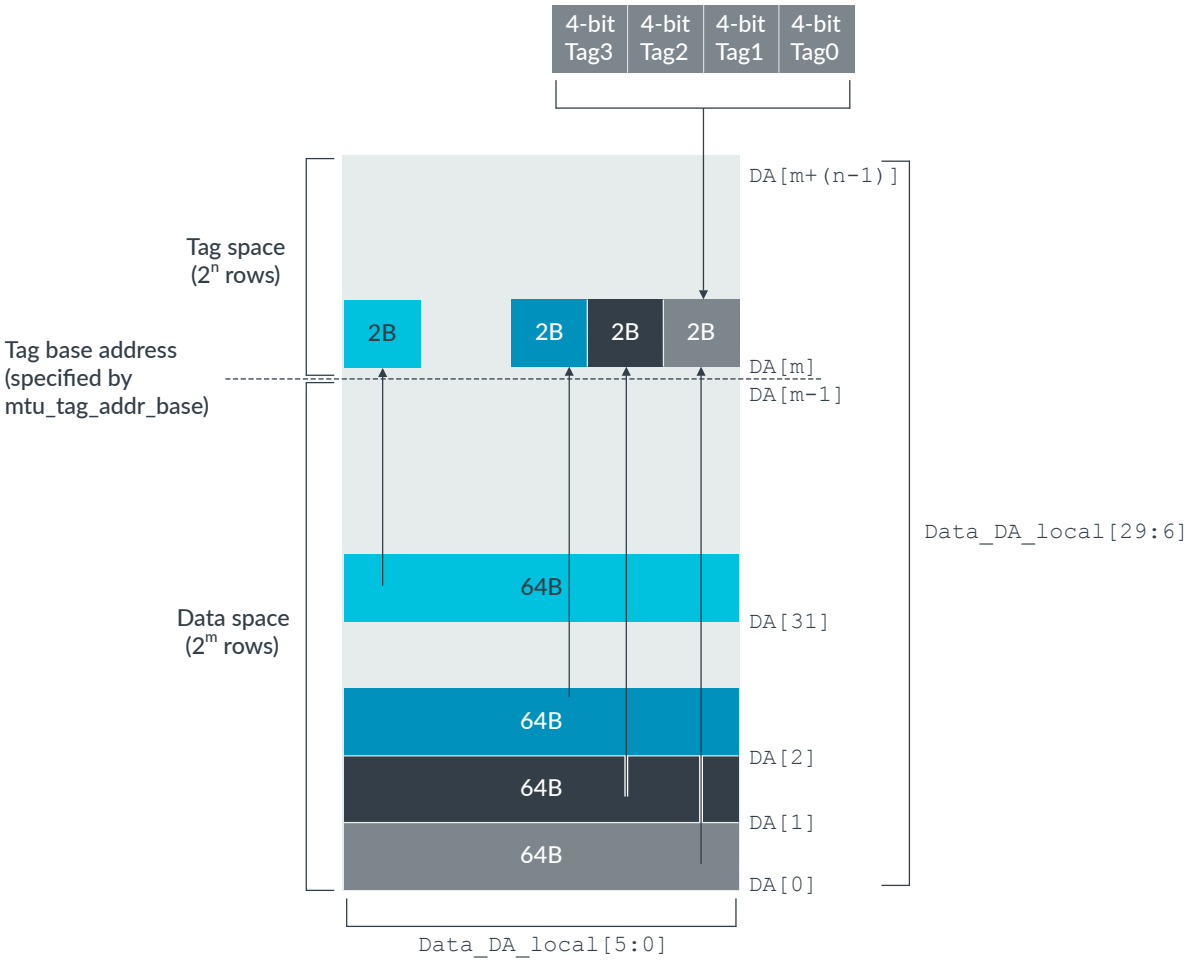
Figure 5-1421: Relationship between mtu_tag_addr_base and DRAM tag space base address



The following constraints apply to the tag regions in DRAM:

- The tag region cannot be interleaved with the data region. The tag region must also be above the data region within DRAM.
- The tag region in the physical address space cannot straddle multiple regions of a memory map.

For example, for the PDD memory map, it is not allowed to have part of the tag region between 2GB-4GB and another part between 34GB-64GB.

mtu_tag_addr_shutter{2:0}

To determine the correct DRAM address, you must program the mtu_tag_addr_shutter{2:0} registers correctly to remove address bits. The address bits that must be removed are based on the number of HN-Fs and SNs within an SCG, as shown in Table 4-27: HN-F and SN-F combinations supported within an SCG on page 106. These registers allow the removal of up to seven PA bits in the range of bit [51] to bit [6]. To program these registers, you must set the shift behavior of each individual address bit as shown in the following figure.

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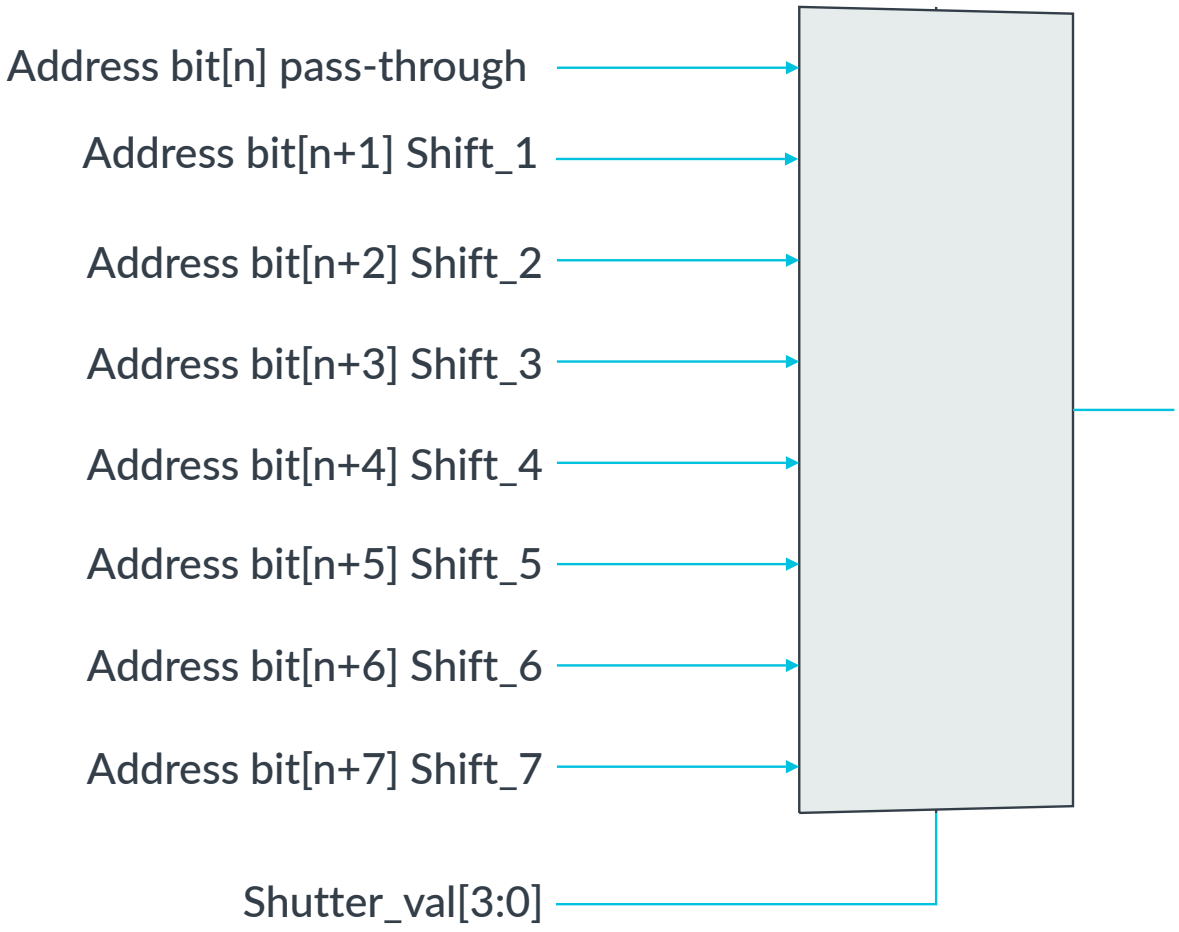
Figure 5-1422: Address shutter register shift behavior



As the preceding figure shows, you can configure the address shutter registers to either:

- Pass through PA bit[n] unchanged.
- Shift another PA bit between bit[n+1] to bit[n+7] into the position of bit[n].

The following figure shows example shutter register programming to remove bit [10] and bit [7] within the PA bit range of bit [12] to bit [6].

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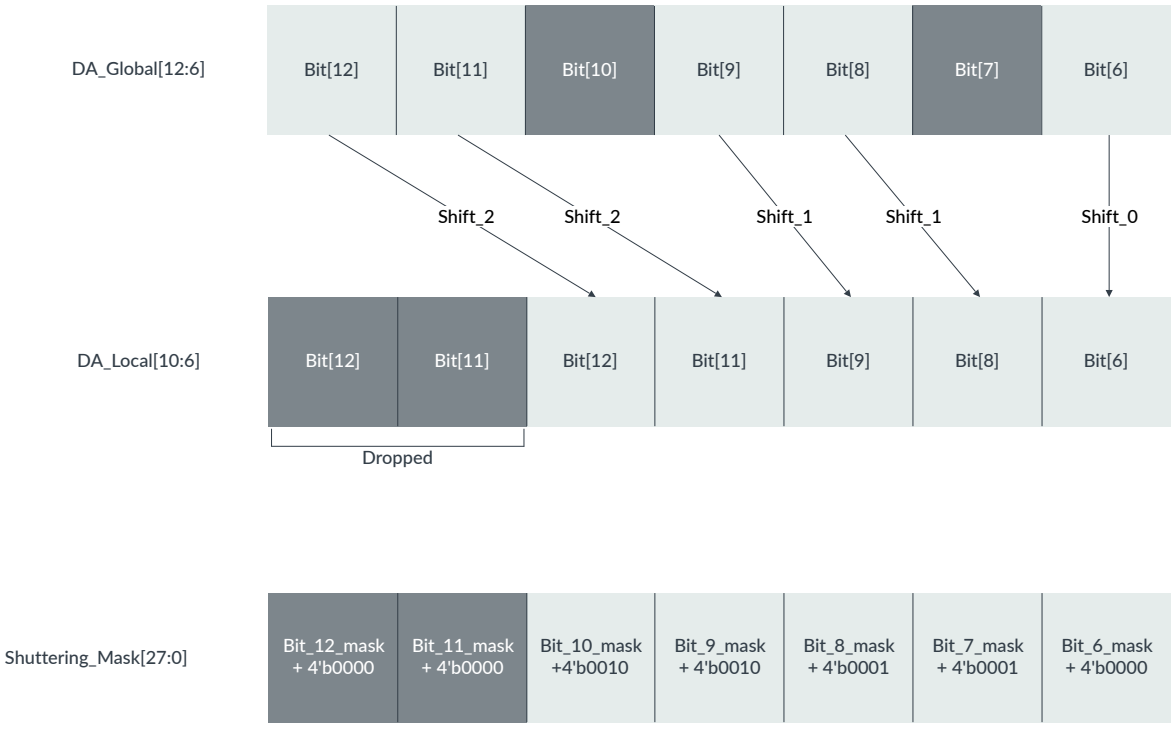
Figure 5-1423: Example address shutter register programming



5.4.7 DT programming

You must follow several programming sequences to set up DTM watchpoints and DTC correctly.

For more information about the CI-700 DT functionality, see 7 Debug trace and PMU on page 1320.

5.4.7.1 Program DTM watchpoint

Use this procedure to program watchpoint N, where N=0..3.

Procedure

1. Program the intended watchpoint matching fields by writing the appropriate values into the por_dtm_wpN_val and por_dtm_wpN_mask registers.
   For example, source ID, target ID and opcode are possible matching fields.
2. Program the WP settings in the following register fields to select the device port and flit CHI channel:
   - wp_dev_sel2 and wp_dev_sel fields of the por_dtm_wpN_config register
   - wp_chn_sel field of the por_dtm_wpN_config register
3. Program the wp_grp field of the por_dtm_wpN_config register to select primary, secondary, or tertiary watchpoint group.

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4. Write 1 to the wp_combine field of the port_dtm_wpN_config register if two watchpoints must be combined.


Note

The wp_combine field is present in WP0 and WP2 only.

5. Program the following register fields if trace packets are to be generated from this watchpoint:
   a) Program the wp_pkt_type field of the por_dtm_wpN_config register.
   b) Write 1 to the wp_pkt_gen field of the por_dtm_wpN_config register.
6. Write 1 to the wp_ctrig_en field of the por_dtm_wpN_config register if a cross trigger must be set up from this watchpoint.
7. Program the wp_dbgtrig_en field of the por_dtm_wpN_config register if a debug watchpoint trigger must be set up from this watchpoint.
8. Set the wp_cc_en field of the por_dtm_wpN_config = 1 if a cycle count is required in the trace packet.
9. Write 1 to the trace_tag_enable field of the por_dtm_control register if a debug watchpoint trace tag must be generated.
10. Write 1 to the dtm_enable field of the por_dtm_control register to enable the WP.

5.4.7.2 Program DTC

Use this procedure to set up the CI-700 debug trace control functionality.

About this task

The **NIDEN** input signal must be asserted for any trace and PMU operations. Before trace and PMU operations can occur, you must first program and enable watchpoint functions in the DTMs. The following registers and register bits are present only in the main DTC (DTC0):

- por_dt_secure_access register
- dt_en field of the por_dt_dtc_ctl register
- wait_for_trigger field of the por_dt_dtc_ctl register
- cc_start field of the por_dt_dtc_ctl register
- pmu_en field of the por_dt_pmcr register
- por_dt_pmsrr register
- ss_cfg_active field of the por_dt_pmssr register
- ss_pin_active field of the por_dt_pmssr register

Procedure

1. Write 1 to the dbgtrigger_en field of the por_dt_dtc_ctl register if DBGWATCHTRIG must be generated for DTM debug watchpoint trigger.
2. Write 1 to the atbtrigger_en field of the por_dt_dtc_ctl register if ATB trigger must be generated for DTM debug watchpoint trigger.

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3. Write 1 to the cc_enable field of the por_dt_trace_control register to enable cycle count.
4. Write 0 to the dt_wait_for_trigger field of the por_dt_dtc_ctl register if no cross trigger is required.
5. Write 1 to the dt_en field of the por_dt_dtc_ctl register.

5.4.8 PMU system programming

You must follow specific programming sequences to set up the PMU, PMU snapshot, and PMU interrupt functionality correctly.

5.4.8.1 Set up PMU counters

Use this procedure to set up the PMU counters correctly.

Procedure

1. Ensure that the **NIDEN** input is asserted for any trace and PMU operations.
2. Program (dev)_pmu_event_sel register in the devices or XP.
3. Program the pmevcnt{0..5}_input_sel fields of the por_dtm_pmu_config register to select PMU event counter inputs.
   The input can be from one of the following:
   - A watchpoint.
   - Selected events from the devices or XP, depending on step 2.
4. Program the following por_dtm_pmu_config register fields to select the paired top global PMU counters:
   - pmevcnt_paired
   - pmevcnt{0..3}_global_num
5. Program the pmevcnt{01, 23}_combined fields of the por_dtm_pmu_config for any combined local PMU counters.
6. Write 1 to the pmu_en field of the por_dtm_pmu_config register.
7. Write 1 to the dtm_enable field of the por_dtm_control register.
8. Program the cntcfg field of the por_dt_pmcr register to pair the 32-bit global counters to make a 64-bit counter.
9. Write 1 to the dt_en field of the por_dt_dtc_ctl register.
10. Write 1 to the ovfl_intr_en field of the por_dt_pmcr register to enable interrupts on **INTREQPMU** on any global counter overflow.
11. Write 1 to the pmu_en field of the por_dt_pmcr register to start PMU operation.

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5.4.8.2 Program PMU snapshot

Use this procedure to set up the PMU snapshot functionality.

Before you begin
The NIDEN input must be asserted for any trace and PMU operation.

About this task
For a system with multiple DTCs, the sub-DTC maintains snapshot status for the DTM within its own domain.

Procedure
1. Program PMU counters as described in 5.4.8.1 Set up PMU counters on page 1294.
2. Write 1 to the ss_req field of the por_dt_pmsrr register.
   This action causes the DTC to send a PMU snapshot instruction. On receiving this instruction, the DTM sends PMU snapshot packets to the DTC.

Results
The DTC updates the ss_status field of the por_dt_pmssr register after receiving PMU snapshot packets. Software can poll this register field to check if the snapshot process is complete.

5.4.8.3 Program PMU counter overflow interrupt

Use this procedure to set up the PMU counter overflow interrupt.

Before you begin
The NIDEN input must be asserted for any trace and PMU operation.

Procedure
1. Program PMU counters as described in 5.4.8.1 Set up PMU counters on page 1294.
2. Write 1 to the ovfl_intr_en field of the por_dt_pmcr register.
   Overflow of any PMU counter causes **INTREQPMU** to assert.
3. Write 1 to the ovfl_intr_en field in the all other por_dt_pmcr registers if your system has multiple DTCs.
4. Poll the pmovsr[7:0] field of the por_dt_pmovsr register when **INTREQPMU** is asserted to see which global counter causes the interrupt.
   For multiple DTCs, all por_dt_pmovsr registers must be polled.
5. Write 1 to the corresponding bit in the pmovsr_clr[7:0] field of the por_dt_pmovsr_clr register to clear **INTREQPMU**.

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6 SLC memory system

This chapter describes the optional SLC memory system which is implemented by HN-Fs in the mesh.

6.1 About the SLC memory system

The SLC memory system consists of the HN-F protocol nodes in CI-700.

There is a configurable number of instances (1-8) of the HN-F. Each HN-F node or slice has the following features:

- 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB of SLC data RAM and tag RAM.
- Combined *Point-of-Coherency* (PoC) and *Point-of-Serialization* (PoS).
- SF size of 512KB, 1MB, 2MB, 4MB, or 8MB.

Each HN-F in CI-700 is configured to manage a specific portion of the total address space. For each portion of the address, each HN-F:

- Can cache data in SLC
- Manages PoC and PoS functionality for ordering and coherency
- Tracks RN-F caching in the SF

The SLC memory system has the following features:

- *Physically Indexed and Physically Tagged* (PIPT)
- Coherency granule is a fixed length of 64B. SLC line size is a fixed length of 64B.
- Both SLC and SF are 16-way set-associative. 12-way for 3MB SLC configurations.
- By default the SLC and SF use a pseudo-random victim selection policy. If there is an invalid way, it is not necessary to select a victim.
- Optionally, CI-700 supports an *enhanced LRU* (eLRU) cache replacement policy that can be enabled by setting a bit in the configuration register. eLRU is Dynamic Biased Replacement Policy. 2 bits per set/way are used to track and predict how soon a cache line is expected to be used again. This information is dynamically adjusted based on a few reference sets.
- SLC and SF arrays:
  - Supports one-cycle, two-cycle, or three-cycle non-pipelined tag array
  - Supports two-cycle or three-cycle non-pipelined data array
  - SLC tag, SF tag, and SLC data arrays are single-ported, supporting one read or write access with no concurrency available
  - SLC tag, SF tag, and SLC data arrays are ECC SECDED protected, with inline ECC checking and correction

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- 16, 32, or 64-entry address and data buffer, which is known as the *PoC Queue* (POCQ), to service:
  - All transactions from the CHI interface
  - SLC evictions to the memory controller
  - SF evictions and associated WriteBacks to the memory controller
- CMO propagation to SN-F or SBSX:
  - Implements improved PCMO flow that is introduced in CHI-D
  - Conditional CMO propagation to the memory controller to support external DRAM caches
  - HN-F must be explicitly programmed using the por_hnf_sam_sn_properties register of the HN-F SAM to allow such propagation to each SN-F
- Supports QoS-based protocol flow control:
  - POCQ resources are allocated or rejected for protocol retry according to the QoS class
  - POCQ resources are watermarked for different QoS classes with user-configurable options
  - Starvation prevention for lower-priority QoS classes
  - QoS-based static grantee selection for CHI architecture credit return
- QoS priority-based request selection to the memory controller
- Supports allocation in the SLC from snoop intervention. This feature enables data sharing through the SLC for multiple sharers.
- SLC state includes a caching LDID to detect dynamic read sharing
- Configurable 34-bit or 40-bit *Physical Address* (PA) support
- PoC and PoS for all snoopable and non-snoopable, and cacheable and non-cacheable address space
- Supports ECC scrubbing for single-bit ECC errors on SF and SLC tag RAMs
- Software-controlled error injection support to enable testing of software error handler routine
- Power management states to support:
  - Full powerdown of the SLC and SF. HN-F only mode when both SLC and SF are powered down
  - Half the SLC ways powered down
  - Retention for SLC and SF
  - SLC full powerdown with SF on, when in SF only mode
- Arm TrustZone® technology support in SLC and SF
- Software-configurable (one, two, four, eight, or 12 ways) memory region locking support in the SLC
- Software-configurable (one, two, four, eight, or 12 ways) OCM support in the SLC
  - OCM memory does not require any physical memory backing
- Supports CHI enhancements for:
  - *Direct Cache Transfer* (DCT)

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- *Direct Memory Transfer* (DMT)
- Cache stashing
- Atomics support
- Data poison
- Data parity (data check)
- Trace tag

- Invisible SLC support:
  - CI-700 HN-F implements an invisible cache. All accesses (cacheable, non-cacheable, and device types) are checked against the SLC and SF. The SLC cannot be cleaned and invalidated (flushed) by software using Arm architecture set/way operations. Software specific to CI-700 would instead be required to flush the SLC, as described in this TRM. Invisible SLC support eliminates the requirement to perform SLC flushes for software context switches from cacheable to non-cacheable.
- Supports up to two memory-region-based SN targets and one or three SN-F address hashing
- Supports MPAM
- Supports MTE

6.2 SLC memory system components and configuration

CI-700 *System Level Cache* (SLC) is a distributed, mostly exclusive last-level cache that is implemented within the HN-F node.

When a sharing pattern is detected between RN-F clusters, the SLC is optimized to eliminate redundancy for private data lines from the RN-F. The SLC also enables redundancy, or pseudo-inclusion. CI-700 SLC also acts as DRAM cache for I/O coherent agents, that is, RN-Is. The SLC enables RN-Is to allocate or not allocate, according to the usage model.

The SF works with the SLC to track coherent lines that are present in the RN-F caches. The SF is fully inclusive of all the lines present in the RN-F caches. SF eviction invalidates the lines from RN-F caches to maintain this inclusion.

Normally, a particular coherent cache line is present only in the system level cache or SF except when the line is shared between RN-F clusters. In the shared case, the line can be present in both the SLC and the SF.

6.2.1 HN-F configurable options

The HN-F can be configured in several ways.

The HN-F has the following configurable parameters:

- SLC size of 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB
- SF size of 512KB, 1MB, 2MB, 4MB, or 8MB

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- One-cycle, two-cycle, or three-cycle tag RAM arrays. For a given configuration, both SLC tag and SF tag have the same latency.
- Two-cycle or three-cycle data RAMs, data, and SF array RAMs. All data RAMs have the same latency.

The HN-F has the following fixed parameters:

- HN-F CHI interface data-VC (DAT) width of 256 bits

6.2.2 Snoop connectivity and control

Each HN-F can send three types of snoop.

The available types of snoop request are:

- Directed, to one RN-F.
- Multicast, to more than one but not all.
- Broadcast, to all RN-Fs.

6.2.3 TrustZone technology support

The HN-F supports TrustZone® technology by treating the Non-secure bit from a request as part of the address.

TrustZone® enables the HN-F to treat Secure and Non-secure as two different areas of the memory space:

- The NS bit is stored in the SLC and SF tags.
- Snoops also propagate the NS bit as part of the message.
- Any request to the memory controller also propagates the NS bit.

6.2.4 HN-F SAM configuration by SN type

CI-700 supports multiple SN types. You must program the HN-F SAM according to the types of SN that the HN-F targets.

You can configure CI-700 to use the following SN types:

- CHI-C, CHI-D, or CHI-E SN-F.
- SBSX.
- MTSX.

To configure SN target types in the HN-F SAM, program the por_hnf_sam_sn_properties register. For the description of this register, see 5.3.4.64 por_hnf_sam_sn_properties on page 465.

The following table shows the bit values that you must program for each SN type.

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Note

The value of <x> describes the specific SN target.

Table 6-1: por_hnf_sam_sn_properties SN type values

SN type	SN<x>_is_chic bit value	SN<x>_is_chie bit value	sn<x>_pcmo_conv_to_pcmo bit value
CHI-C SN-F	0b1	0b0	0b1
CHI-D SN-F	0b0	0b0	0b0
CHI-E SN-F	0b0	0b1	0b0
SBSX or MTSX	0b0	0b1	0b0


Note

- If the AXI memory controller does not support WR+PCMO, then HN-F must be programmed for this SN in CHI-D mode.
- If the AXI memory controller does not support PCMO on AW channel, then HN-F must be programmed as CHI-C SN mode.
- If the system uses CHI-E GrpIDExtn bits and the SN-F is CHI-D, then the sn<x>_pcmo_conv_to_pcmo for HN-F must be set to 0b1.

6.2.5 Hardware-based cache flush engine

The HN-F supports a hardware-based cache flush engine mechanism to flush the SF and SLC. The flush engine ensures that all cache lines in the lower and upper range are flushed from the CI-700 SF and SLC.

Various *Address Based Flush* (ABF) configuration registers per HN-F instance support the cache flush engine:

por_hnf_abf_lo_addr
: ABF lower range address.

por_hnf_abf_hi_addr
: ABF upper range address.

por_hnf_abf_pr
: ABF policy register. Triggers flush start, indicates flush operation type.

por_hnf_abf_sr
: ABF status register. Indicates flush completion and other status information.

The flush engine ensures that all cache lines in the lower and upper range are flushed from the CI-700 SF and SLC. When all cache lines within this range are flushed, a bit in the por_hnf_abf_sr register is set indicating that the flush engine has completed. If enabled, an interrupt (**INTREQPPU**) is then sent.

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Note

Interrupt indication and complete bit in the por_hnf_abr_sr registers are set regardless of normal completion or abort condition. To determine if a flush request completed normally or aborted, check the error bits in the por_hnf_abf_sr register.

To complete the flush sequence, the HN-F carries out the following steps:

1. Flush CI-700 SFs. This operation flushes the lines in the lower-level caches. Lower-level write-backs go to memory and are not allocated to the CI-700 SLC.
2. Flush the CI-700 SLC.
3. On completion of the flush:
   a. The HN-F sets the status bit in the por_hnf_abf_sr register when the flush is complete for that HN-F. If there are error conditions, they are also set in the por_hnf_abf_sr register. This register is cleared when next ABF request starts.
   b. The HN-F sends a completion message to the global Power/Clock/Reset unit, and an optional **INTREQPPU** is asserted when all HN-F instances have completed the flush.

ABF requests are processed in parallel to other ongoing requests from RNs. If an ABF request and another ongoing request target the same address, then no ordering or coherency guarantee is provided. Power management transition requests have higher precedence than ABF requests. An ABF request is only supported when:

- The power management state is in FAM, HAM, or SFONLY mode.
- The retention state is IDLE or RETENTION (not transitionary).

While ABF is in progress, any update to the *Power Policy Register* (PWPR) causes the ABF state machine to abort and the power management request proceeds.

By default, the flush engine writes back any modified data to memory before invalidating the cache line from internal caches. Two more configuration modes are provided for user flexibility. Therefore, the flush engine has the following three modes of operation:

CleanInvalid
: Write back and invalidate (default).

MakeInvalid
: In this mode, modified data is not written back to memory.

CleanShare
: In this mode, modified data is written back to memory but clean data remain in internal caches.

If *On Chip Memory* (OCM) is enabled and the address range overlaps with the ABF range, OCM behavior supersedes ABF. For SLC, this condition means that for CleanInvalid and CleanShare modes, no action is taken. For MakeInvalid, there is no difference in behavior regardless of whether the address is in the OCM range or not. For SF flush, the behavior is the same between an OCM address match and not.

The following tables show a summary for SF and SLC caches for all three modes.

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Table 6-2: SF cache operation

SF state	Hit		Miss	
ABF mode	SNP type to RN-F	Change SF state?	SNP to RN-F	Change SF state?
CleanInvalid	CleanInvalid	Yes	N/A	No
MakeInvalid	MakeInvalid	Yes	N/A	No
CleanShared	CleanShared	Yes	N/A	No

Table 6-3: SLC cache operation

SLC state		Modified		Exclusive or Shared		Invalid	
ABF mode	OCM match?	Evict line?	Change L3 state (final state)	Evict line?	Change L3 state (final state)	Evict line?	Change L3 state (final state)
CleanInvalid	No	Yes	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)
MakeInvalid	No	No	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	Yes (I)	No	Yes (I)	No	No (I)
CleanShared	No	Yes	Yes (E)	No	No (ES)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)


Note

The following assumptions are made:

- To ensure maintenance of coherency and ordering, RNs should not access a cache line within the flush range while ABF is in progress.
- Address ranges and trigger must be programmed for each HN-F in the SCG.
- Do not change ABF-related configuration register bits when the abf_enable bit of the por_hnf_abf_pr register is set, until the flush is done. The abf_complete bit of the por_hnf_abf_sr register indicates that the flush is done.
- HN-F must be in one of the three operational modes (FAM, HAM, SFONLY). When flush starts, any update to the PWPR causes ABF to abort.
- SF must be enabled for the flush engine to operate. If SF is disabled, the flush engine aborts and indicates an error status in the por_hnf_abf_sr register.
- When ABF completes, check the por_hnf_abf_sr to ensure ABF completed without any errors. If ABF aborted for any reasons, then the por_hnf_abf_sr indicates that the flush was aborted.

6.2.6 Software-configurable memory region locking

The HN-F supports variable size memory regions that can be locked in the system level cache with way reservation.

These variable size memory regions ensure that locked lines are not evicted from the SLC. Any access to those lines is guaranteed to hit in the SLC. The variable memory region is calculated as a factor of the total SLC size and number of ways that are locked. For example, consider an SLC that

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is built with 16 ways. In this case, way locking of 1, 2, 4, 8 or 12 yields 1/16, 2/16, 4/16, 8/16 or 12/16 of the SLC size respectively.

Software uses the following mechanism to program the HN-F configuration registers to enable region locking:

- The hnf_slc_lock_ways register specifies the total number of locked HN-F system level cache ways. This register can have a value of 1, 2, 4, 8, or 12.
- The following region base registers specify the base address of the region that is using locked ways:
  - hnf_slc_lock_base0 register
  - hnf_slc_lock_base1 register
  - hnf_slc_lock_base2 register
  - hnf_slc_lock_base3 register
- A combination of the total SLC size, hnf_slc_lock_ways register, and the hnf_slc_lock_base0 register to hnf_slc_lock_base3 register defines the following:
  - The total amount of cache that is locked, calculated as follows:

    Figure 6-1: Total cache locked equation

    $$\frac{\text{Total SLC size x Number of locked ways}}{16}$$

  - Ways are locked beginning with way 0 and then in ascending order
  - The number of valid regions and exactly which regions are valid and included in the HN-F way allocation. This definition therefore indicates which of the hnf_slc_lock_base0 to hnf_slc_lock_base3 registers are valid and included in the HN-F way allocation.
  - The exact location, size, and alignment requirement of each region
- The region alignment is identical to the region size, for example:
  - A 0.5MB region is aligned to any 0.5MB boundary
  - A 4MB region is aligned to any 4MB boundary
- The size and alignment requirement is enforced in hardware, to prevent any errors in software
- Regions can be disjointed or contiguous, to create a larger single region
- All valid regions use all locked ways. There is no application-level way segregation.
- The HN-F must be in the FAM power state. Memory region locking is not supported in other CI-700 power states


Note

The locked regions do not comprehend Secure as opposed to Non-secure memory regions. Therefore, if aliasing is performed between Secure and Non-secure regions, overlocking can occur.

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The following tables specify various combinations of region size and the number of locked ways that software must program. Software can program these values using the hnf_slc_lock_ways register and the hnf_slc_lock_base0 register to hnf_slc_lock_base3 register.

Table 6-4: SLC Region Lock sizes

SLC size	Number of locked ways	Total locked region size	Locked ways	Number of ways per region	Region 0	Region 1	Region 2	Region 3
8MB	1	0.5MB	0	1	0.5MB	-	-	-
8MB	2	1MB	0-1	1, 1	0.5MB	0.5MB	-	-
8MB	4	2MB	0-3	1, 1, 1, 1	0.5MB	0.5MB	0.5MB	0.5MB
8MB	8	4MB	0-7	2, 2, 2, 2	1MB	1MB	1MB	1MB
8MB	12	6MB	0-11	2, 2, 4, 4	1MB	1MB	2MB	2MB

Table 6-5: Settings for hnf_slc_lock_baseX

Region size	Valid bits
0.5MB	[PA_WIDTH-1:19]
1MB	[PA_WIDTH-1:20]
2MB	[PA_WIDTH-1:21]
4MB	[PA_WIDTH-1:22]
8MB	[PA_WIDTH-1:23]

6.2.7 Software-configurable On-Chip Memory

The CI-700 HN-F supports software configurable *On-Chip Memory* (OCM) which allows for the creation of systems without physical DDR memory. It also allows a system to use SLC as scratchpad memory.

In OCM mode, the HN-F does not send requests to the SN-F. To enable OCM, the following requirements must be met:

- The HN-F must be in the FAM power state. Other CI-700 power states are not supported in OCM mode.
- All OCM ways must be same across all HN-Fs in a system cache group.
- OCM mode must be enabled before any non-config accesses are sent to HN-F.

In OCM mode, the following CMOs terminate in the SLC:

- CleanInvalid and CleanShared CMOs terminate in the SLC without invalidation or performing a WriteBack to the SN-F.
- MakeInvalid invalidates the cache line in SLC, and can be used to invalidate the OCM region.

OCM mode can be enabled by programming the hnf_ocm_en bit in the por_hnf_cfg_ctl register. If the hnf_ocm_allways_en bit is set to 1, then all transactions targeting the HN-Fs have OCM behavior. The OCM region must be contiguous and aligned to the total SLC size of the configuration when the hnf_ocm_allways_en is set to 1. If the hnf_ocm_allways_en bit is 0, region

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locking registers define the OCM regions. For more information about these region locking registers, see 6.2.6 Software-configurable memory region locking on page 1302.


Note

Region locking registers do not explicitly control Secure and Non-secure memory regions. Therefore combined Secure and Non-secure memory regions should not exceed the total SLC size that is locked for OCM.

6.2.8 Source-based SLC cache partitioning

HN-F supports a feature to lock SLC ways for requesting nodes RN-F, RN-I, and RN-D.

This feature is an extension of the address-based way locking but the locked ways are based on the requestors instead of the programmed address. CI-700 supports programming of:

- The number of ways that can be locked
- RN devices for which these ways are locked
- Allocation policies in each HN-F

With this feature enabled, the locked SLC ways are only available to the programmed RNs for any new cache line allocations.

Source-based way locking feature can be enabled by programming the por_hnf_rn_region_lock.rn_region_lock_en bit to 1 in each HN-F instance. The requesting nodes, for which these ways are to be locked must also be explicitly enabled in the por_hnf_rn*region_vec registers. The requesting nodes are individually identified using the logical IDs. CI-700 has three RN types: RN-F, RN-I, and RN-D. Each requesting node type has different registers and is uniquely identified in a CI-700 system using logical IDs. The number of ways that are locked are programmed in the por_hnf_slc_lock_ways.ways field.

The region locking feature has two allocation modes:

- Allocating new cache lines for matching RNs only in the locked ways. By doing so, the matching RNs are restricted to allocate to the locked partition only. This mode can be enabled by setting por_hnf_rn_region_lock.rn_pick_locked_ways_only bit to 1.
- Allocating new cache lines for matching RNs to one of the locked or unlocked ways. This mode is the default behavior. In this mode, the locked ways are restricted only to the matching RNs but the unlocked ways are accessible by all the RNs.

Source-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.


Note

The HN-F must be in the FAM power state. Source-based cache partitioning is not supported in other CI-700 power states.

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6.2.9 Way-based SLC cache partitioning

Each SLC cache instance can be partitioned into different regions. This partitioning allows each requesting node (RN-F, RN-I, RN-D) to allocate in one or more regions, each consisting of four consecutive ways.

Each region group has configuration registers that indicate which of the logical RN-F/RN-I/RN-D masters can allocate to the corresponding group of SLC ways. By default, all RNs can allocate all 16 ways, as the following tables show.

Table 6-6: Logical RN-F ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-F ID								
				63	62	61	60	----	3	2	1	0
por_hnf_slcway_partition0_rnf_vec	0xC48	[3:0]	{64'{1'b1}}									
por_hnf_slcway_partition1_rnf_vec	0xC50	[7:4]	{64'{1'b1}}									
por_hnf_slcway_partition2_rnf_vec	0xC58	[11:8]	{64'{1'b1}}									
por_hnf_slcway_partition3_rnf_vec	0xC60	[15:12]	{64'{1'b1}}									

Table 6-7: Logical RN-I ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-I ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rni_vec	0xC68	[3:0]	{32'{1'b1}}									
por_hnf_slcway_partition1_rni_vec	0xC70	[7:4]	{32'{1'b1}}									
por_hnf_slcway_partition2_rni_vec	0xC78	[11:8]	{32'{1'b1}}									
por_hnf_slcway_partition3_rni_vec	0xC80	[15:12]	{32'{1'b1}}									

Table 6-8: Logical RN-D ID requesting node

Register	Address offset	Ways reserved	Default	Logical RN-D ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rnd_vec	0xC88	[3:0]	{32'{1'b1}}									
por_hnf_slcway_partition1_rnd_vec	0xC90	[7:4]	{32'{1'b1}}									
por_hnf_slcway_partition2_rnd_vec	0xC98	[11:8]	{32'{1'b1}}									
por_hnf_slcway_partition3_rnd_vec	0xCA0	[15:12]	{32'{1'b1}}									

The registers in these tables are used to mask the ways that are always available for an RN to allocate to. A value of:

0b1 Indicates that the corresponding Logical RN ID can allocate in this region.
0b0 Indicates that the corresponding Logical RN ID cannot allocate to this region.

To enable the way reservation only to a subset of RNs, the mask in the preceding registers must be programmed as the following example shows:

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Example 6-1: Reserve ways 0-3 for RN-F {0-3}

1. Write `64'h000000000000000F` to por_hnf_slcway_partition0_rnf_vec. This operation enables logical RN-F IDs 0, 1, 2, and 3 to allocate to ways 0-3. All other RN-F IDs (4-63) cannot allocate to these ways.
2. Write `32'h0` to por_hnf_slcway_partition0_rni_vec. This operation disables all 32 RN-Is from allocating to ways 0-3.
3. Write `32'h0` to por_hnf_slcway_partition0_rnd_vec. This operation disables all 32 RN-Ds from allocating to ways 0-3.


Note

The following conditions apply to this example:

- This feature cannot be used if region-based locking, source-based locking, or OCM is enabled.
- The region registers can be changed at runtime.
- When the way partitioning scheme is not being used, the preceding registers must be returned to the default values.
- Each RN should be configured to allocate to at least one partition. Setting the bit for a given RN to 0 in all partition registers defaults it to allocating in any partition.
- RN-I and RN-D each support a maximum logical ID of 32 in the partition mask register.

Way-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.


Note

The HN-F must be in the FAM power state. Cache partitioning is not supported in other CI-700 power states.

6.3 Error reporting and software-configured error injection

HN-F detects and reports several types of errors to the error block.

HN-F supports the following types of errors:

Correctable errors

For example, single-bit ECC error detection and correction in the SLC tag RAM, SF tag RAM, and SLC data RAM

Deferred errors

For example, double-bit ECC error detection in SLC tag RAM and double-bit ECC error detection in SLC data RAM

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Uncorrectable errors

For example, double-bit ECC errors in the SLC tag RAMs

If the DATACHECK_EN parameter is enabled, HN-F can also support data parity error detection in the SLC data RAM. These errors are logged as deferred errors.

For logging and reporting all error types, HN-F follows the procedures described in 4.17 Reliability, Availability, and Serviceability on page 141.

For information regarding the error source, see the ERRSRC field of 5.3.4.24 por_hnf_errmisc on page 416.

6.3.1 Software-configurable error injection

The HN-F supports software-configurable error injection and reporting. This feature enables testing of the software error handler routine for SLC double-bit ECC data errors.

The HN-F configuration register for a particular logical thread enables configurable error injection and reporting.

Any cacheable read for which the HN-F is the source of the data is defined as a system cache hit. If error injection and reporting are enabled, any system cache hit drives the slave error from the system cache pipe and a fault interrupt through the RAS control block for that read. This functionality emulates a double-bit ECC error in the SLC data RAM but does not pollute the SLC data RAM through the fill path.



This mechanism is designed to mimic SLC data ECC errors for SLC hits. SLC misses do not drive any errors or error interrupts. If enabled, this mechanism causes only an error to be logged and optionally an interrupt to be generated. Error injection on SLC hits does not alter the Resp*, Poison, or Data fields in the DAT flit that is returned to the RN.

For more information about configuring error injection, see 5.3.4.25 por_hnf_err_inj on page 418.

6.3.2 Software-configurable parity error injection

The HN-F supports software-configurable parity error injection.

This feature enables testing of the software error handler routine for parity error. For more information about enabling this feature, see 5.3.4.26 por_hnf_byte_par_err_inj on page 419. This register specifies the byte lane from 0-31 in which a parity error is introduced. The memory data is uncorrupted with such injection, but the DataCheck field of the DAT flit that is returned to an RN is altered.

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6.4 Transaction handling in SLC memory system

The CI-700 SLC memory system handles various types of CHI operations and transaction fields. The structure of the overall system and how each component is configured affects how these transactions are handled.

6.4.1 Cache maintenance operations

CI-700 uses several CHI *Cache Maintenance Operations* (CMOs).

The following operations are supported:

- CleanInvalid.
- CleanShared.
- MakeInvalid.
- CleanSharedPersist.
- CleanSharedPersistSep.

These operations always look up the SLC and the SF, and take the following actions:

- Clean and invalidate the line if present in the SLC.
- If the CMO is snoopable, the HN-F sends a snoop to the RN-F post SF lookup if necessary.
- If the cache line is modified in the SLC or in the cache of the RN-Fs, the HN-F initiates a memory controller WriteBack if necessary.


Note

If the CMO is MakeInvalid, there is no WriteBack to the memory controller.

The SF does not track RN-F coherence while the HN-F is in NOSFSLC state. Therefore, the RN-F caches must be flushed before transitioning from NOSFSLC to SFONLY, HAM, or FAM states.

6.4.2 Cacheable and non-cacheable exclusives

The HN-F supports PoC monitor functionality for cacheable and snoopable exclusive operations from the RN-Fs.

The cacheable and snoopable exclusive transactions are:

- ReadShared.
- ReadClean.
- CleanUnique.
- ReadNotSharedDirty.

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The HN-F also supports system monitor functionality for non-cacheable exclusive support. For more information about exclusives, see the *AMBA® 5 CHI Architecture Specification*.



Each HN-F in CI-700 can support tracking of up to 64 logical processors for exclusive operations. The system programmer must ensure that there are no more than 64 logical processors capable of concurrently sending exclusive operations.

6.4.3 DataSource handling

CI-700 populates the DataSource field of a CompData response to specify the source of the data.

DataSource information can be used:

- To determine the usefulness of a PrefetchTgt (memory controller prefetch) transaction.
- To profile and debug software to evaluate and optimize data sharing patterns.

Table 6-9: DataSource encodings

Source of data	Message	Encoding
HN-I	Default (non-memory source)	0b0000
RN-F	Peer processor cache within local cluster	0b0001
RN-F	Local cluster cache	0b0010
HN-F	*System Level Cache* (SLC)	0b0011
RN-F	Peer cluster cache	0b0100
Remote chip	Remote chip caches	0b0101
SN-F, SBSX, or MTSX	PrefetchTgt was useful.	0b0110
SN-F, SBSX, or MTSX	PrefetchTgt was not useful.	0b0111



In MTSX, the indication of the usefulness of PrefetchTgt applies only to the data portion of the transaction. The indication does not apply to tags.

CI-700 drives the DataSource value only when the source of the data is either HN-F or HN-I. For other data sources, CI-700 acts as a conduit.

The encoding that CI-700 uses to indicate a data source is the same as the suggested value in the *AMBA® 5 CHI Architecture Specification*. Any deviation from the specified encodings might result in unexpected behavior.

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6.4.4 CMO and PCMO propagation from HN-F to SN-F or SBSX

CI-700 supports propagation of CMO and PCMO requests for a given cache line to the memory controller. The completion point of these requests is programmable.

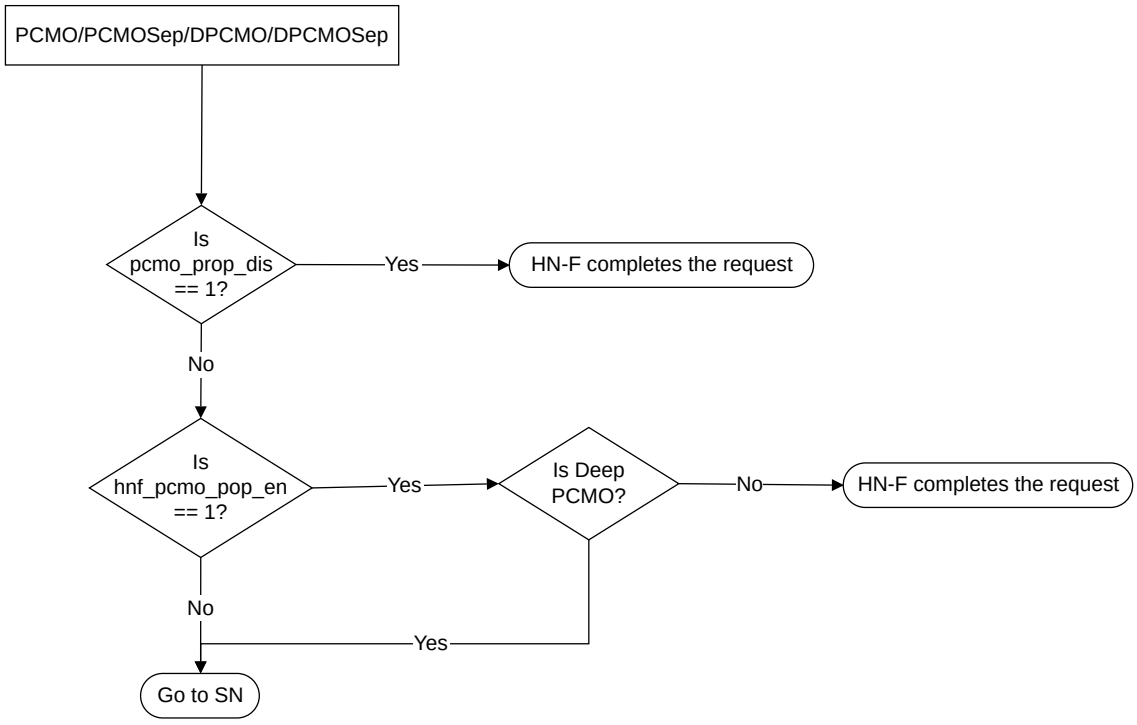
This feature ensures that the cache line has been written to the memory controller and any copies in the CI-700 system have been removed. Conditional CMO and PCMO propagation to the memory controller also supports external DRAM caches. This feature can be enabled or disabled in the por_hnf_sam_sn_properties register bits for each HN-F corresponding to each SN-F. For SBSX with an AXI4 slave memory device, you must disable CMO and PCMO propagation in HN-F.

The following HN-F SAM configuration register bits decide the CleanSharedPersist (PCMO) and CleanSharedPersistSep (PCMOSep) completion point:

- por_hnf_sam_sn_properties.pcmo_prop_dis
- por_hnf_cfg_ctl.hnf_pcmo_pop_en

You can program this behavior per SN. Deep is an attribute in the CHI request flit and applies to PCMO type requests (DPCMOs). HN-Fs use the Deep attribute and the HN-F SAM configuration bits to decide the PCMO request completion point. The following diagram shows the PCMO and PCMOSep request completion point decision process.

Figure 6-2: PCMO and PCMOSep completion point flow diagram



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If both of the following circumstances are true, you must set the por_hnf_sam_sn_properties.X_sn_pcmosep_conv_to_pcmo bit to 1:

- An HN-F is programmed to propagate PCMO requests to an SN-F
- The SN-F does not support PCMOSep requests

This setting allows the HN-F to complete the request by converting PCMOSep type requests to PCMO. The HN-F generates a Persist response to the requestor on receiving a completion of PCMO response from SN-F.



CHI-C and CHI-D SN-Fs do not support the GroupIDExt field in the REQ flit. Therefore, if both of the following criteria are true for your CI-700 system, you must program HN-Fs to terminate persistent CMOs:

- CI-700 contains any CHI-C or CHI-D SN-Fs.
- RNs in the system can issue persistent CMOs.



If the `SBSX_CMO_ON_AW` parameter = 0, you must program the por_hnf_sam_sn_properties.X_sn_pcmosep_conv_to_pcmo configuration bit. Setting this bit prevents HN-F from sending PCMO opcodes that map to two-part PCMOs on AW to SBSX.

You can also program HN-Fs to propagate CleanShared, CleanInvalid, and MakeInvalid CMOs to an SN-F. The following table shows how to program this behavior using the por_hnf_sam_sn_properties register.

Table 6-10: CMO propagation programming in HN-F SAM

HN-F SAM attribute (cmo_prop_en)	CMO completion point
0	HN-F
1	SN

See the following register descriptions for more information:

- 5.3.4.64 por_hnf_sam_sn_properties on page 465
- 5.3.4.5 por_hnf_cfg_ctl on page 386

6.4.5 Memory System Performance Resource Partitioning and Monitoring

CI-700 supports *Memory System Performance Resource Partitioning and Monitoring* (MPAM). MPAM features enable software to optimize the use of memory resources and to monitor how those resources are used.

If MPAM is enabled, then an extra MPAM field is added to the REQ and SNP channels. This field must be stored and propagated to the downstream target.

For more information about MPAM, see the following documents:

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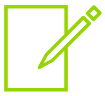
- *AMBA® 5 CHI Architecture Specification*
- *Arm® Architecture Reference Manual Supplement Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A*

6.4.5.1 MPAM propagation

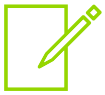
When MPAM is enabled, CI-700 propagates the MPAM fields throughout the network. Various nodes are designed to propagate the MPAM field when processing requests.

The following node types propagate the MPAM field:

- MXP
- RN-I
- HN-F and HN-I
- SBSX
- MTSX



The AXMPAM_EN parameter determines whether MPAM bits are stored and propagated on RN-I, HN-I, and SBSX bridges.



If MPAM support is required in CI-700, set the CHI_MPAM_ENABLE parameter.

When an HN-F node receives a request, it stores the details from the MPAM field. If the request misses in the SLC, then the HN-F must drive the stored MPAM values onto the outgoing request to the memory controller. The MPAM field contents are stored in the SLC_TAG array and propagated into requests that are sent to memory.

When MPAM is enabled, the RN-I has the following extra components:

- Two extra signals on the AXI or ACE-Lite slave port, **ARMPAM[10:0]** and **AWMPAM[10:0]**.
- An extra register field, *_mpam_override_en, which you can program to override the request MPAM value with the set value in the register.



If AXMPAM_EN = 0, then the MPAM override is active by default.

If AXMPAM_EN = 1, the HN-I and SBSX node types propagate **CHI.RXREQ.MPAM** onto the AXI pins.
If AXMPAM_EN = 0, the HN-I and SBSX node types drive 0s onto AXI pins.

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In CI-700, MPAM support is applicable to the SLC.

6.4.5.2 MPAM configuration

CI-700 provides several configuration parameters to configure MPAM features that are used by the interconnect. The MPAM feature ID register, por_hnf_mpam_idr, provides information on what MPAM features are supported in the design.

The number of partitions and the number of performance monitoring groups that are supported is configurable at build time. The default number of partitions is 64 for Non-secure partitions and 16 for Secure partitions. The default number of performance monitoring groups is two.

For more information about the configuration options, see 2.4 Global configuration parameters on page 20 and 2.5 Device-level configuration parameters on page 21.

For more information about supported MPAM features, see 5.3.11.3 por_hnf_mpam_idr on page 1140.

6.4.5.3 Cache portion and capacity partitioning

MPAM support in the interconnect is for the CI-700 SLC. If MPAM is enabled, cache replacement is forced to use an *enhanced Least Recently Used* (eLRU) cache replacement policy.

The SLC supports cache portion partitioning that is based on the following masks:

MPAMCFG_CPBM

The CPBM value for a request PARTID determines which cache portions a request can allocate.

MPAMCFG_CMAX

The CMAX value for a request PARTID determines the percentage of the SLC that a request can use.

Cache portion and capacity partitioning have the following features:

- Number of portions is the same as the number of ways in SLC.
- The hnf_mpam_ccap_idr_cmax_wd field of the por_hnf_mpam_ccap_idr register is set to 6. This setting provides granularity of 1.56% (1 / 2^6) SLC for cache capacity partitioning.
- In HAM mode, portions 15:8 are aliased to portions 7:0. Cache capacity is adjusted for half the cache.
- CI-700 supports address based locking (including OCM) with MPAM. Locked ways are not available for MPAM-based partitioning. Cache capacity is adjusted to account for locked ways.


Note

CI-700 does not support source-based or way-based SLC partitioning with MPAM.

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If using way locking with MPAM, you must program the lock registers first. Then, to determine the number of available portions, read the hnf_mpam_cpor_idr_cpbm_wd field of the por_hnf_mpam_cpor_idr register. Locked ways also reduce cache capacity.

HN-F MPAM counter values are not accurate when exiting retention state and can result in underflow conditions.

6.4.5.4 Cache capacity monitoring

This section describes cache capacity monitoring.

MPAM provides a mechanism for monitoring SLC usage:

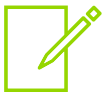
- The HN-F `MPAM_NUM_CSUMON` parameter determines how many monitors are supported.
- The por_hnf_X_msmon_cfg_csu_flt and por_hnf_X_msmon_cfg_csu_ctl registers determine filter and control for each monitor.


Note

The interconnect has two banks for these registers, S and NS, denoted by X in the register or register field name.

The hnf_X_msmon_cfg_csu_ctl_capt_evnt field of the por_hnf_X_msmon_cfg_csu_ctl register supports external capture events 6 and 7:

- External capture event 6 is triggered using **PMUSNAPSHOT** interface or ss_req config bit.
- External capture event 7 is triggered as described in the *Arm® Architecture Reference Manual Supplement Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A*.


Note

Multiple capture events cannot be triggered within 32 cycles of each other.

6.4.5.5 MPAM error logging and reporting

CI-700 implements programmable registers that can enable, disable, and modify MPAM error logging and reporting behavior.

The MPAM error status register, por_hnf_X_mpam_esr, and the MPAM error control register, por_hnf_X_mpam_ecr, define MPAM-related error logging.


Note

The interconnect has two banks for these registers, S and NS, denoted by X in the register or register field name.

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You can enable interrupt generation for MPAM-related errors by setting the hnf_X_mpam_ecr_inten field of the por_hnf_X_mpam_ecr register to `0b1`. If interrupt generation is enabled, level-sensitive interrupts (**INTREQMPAMERRS** or **INTREQMPAMERRNS**) are triggered for defined error cases.


Note

MPAM error reporting has the following exceptions:

- When SLC size is 0K, no errors are detected or reported.
- REQ PARTID or PMG out of range errors are not detected or reported when:
  - HN-F is in SFONLY mode.
  - MPAM features are disabled (by configuring the auxiliary control register).

Except where noted in these exceptions, CI-700 supports MPAM error codes 0-5. For more information about MPAM errors, see *Section 12.2, Error conditions in accessing memory-mapped registers* in the *Arm® Architecture Reference Manual Supplement Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A*.

See the following register descriptions for more information:

- 5.3.11.15 por_hnf_ns_mpam_ecr on page 1155
- 5.3.11.16 por_hnf_ns_mpam_esr on page 1156
- 5.3.12.5 por_hnf_s_mpam_ecr on page 1186
- 5.3.12.6 por_hnf_s_mpam_esr on page 1187

6.4.6 MTE support in HN-F

CI-700 HN-F supports CHI-E *Memory Tagging Extensions* (MTE). For all coherent and non-coherent operations, if requests come with MTE opcodes, HN-F services them by fetching the required tags from SN-F.

In accordance with the CHI-E architecture, HN-F also flushes the dirty tags downstream to SN-F when required.

To disable the MTE handling in HN-F when the software is running without MTE opcodes, program the hnf_mte_mode_dis bit of the por_hnf_cfg_ctl register to 1. In this mode, HN-F ignores any requests for tags and drops dirty tags. For MTE Match requests, HN-F synthesizes a dummy Tag Match response to complete the protocol flow.

6.5 QoS features

The HN-F protocol queue (POCQ) is a key shared system resource that communicates with the memory controller for external memory access.

The HN-F provides QoS capabilities in support of the following traffic classes:

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- Real-time or pseudo-real-time traffic that requires a maximum bounded latency at potentially fixed bandwidth.
- Latency-sensitive traffic, traditionally from a processor device.

CI-700 uses QoS values to designate these traffic classes. Every request to the HN-F has a 4-bit QoS value that is associated with it, with a higher number indicating a higher priority. The four QoS classes are:

- Highest priority (known as HighHigh).
- High priority.
- Medium priority.
- Low priority.

6.5.1 QoS decoding

QoS decoding takes place inside the HN-F.

The QoS decoding is as follows:

- The CHI interface supports a 4-bit QoS value.
- The 4-bit QoS has 16 possible values. For the QoS ranges and class values in HN-F, refer to Table 4-56: QoS classes in HN-F on page 173.
- QoS mapping is fixed, and is shown in the qos_band register.

The POCQ is logically partitioned to service different QoS class traffic. The HN-F also uses the priorities in the table to arbitrate for the following:

- Memory controller request selection in the POCQ control block.
- Data return selection logic, that is, a CompData to a requester.
- Protocol credits that are sent to an RN-F or RN-I following a protocol-layer retry.

6.5.2 QoS class and POCQ resource availability

The POCQ buffers are shared resources for all QoS classes.

The higher the QoS class, the higher the occupancy availability. For example, the *HighHigh* (HH) QoS class can use all the POCQ entries except for the dedicated SF pool.

The following figure shows the availability of POCQ resources for various QoS levels, using a particular QoS pool that is shared between multiple QoS classes.

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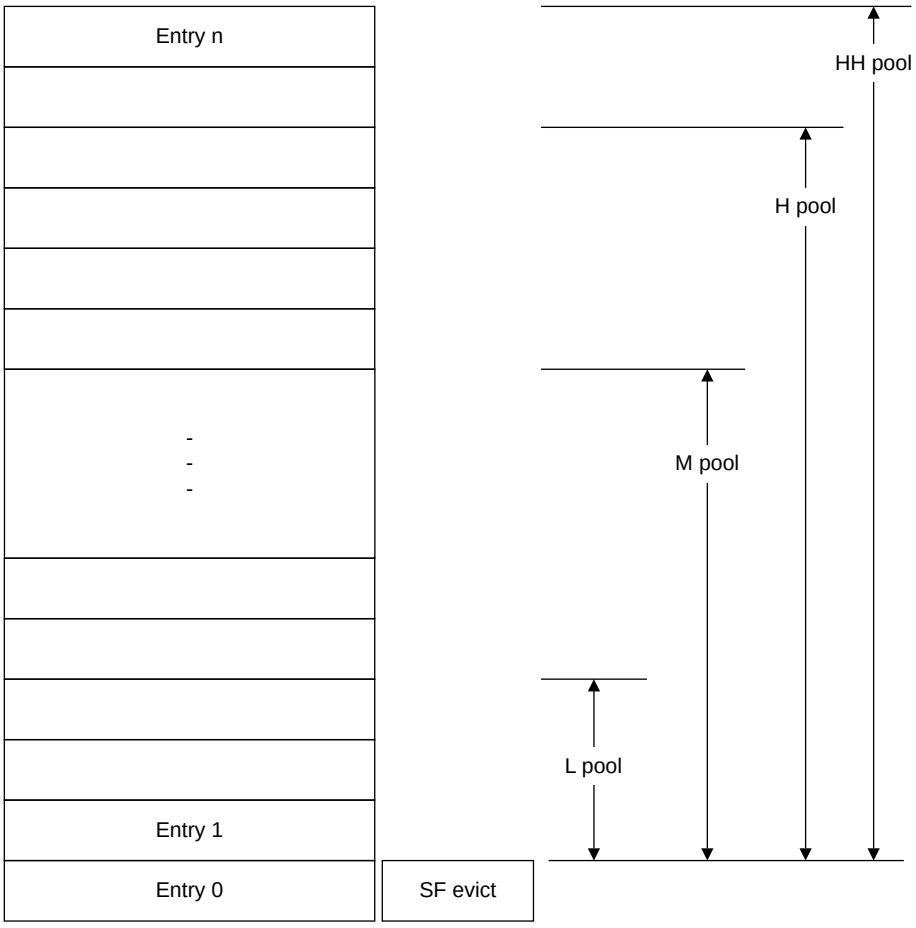
Figure 6-3: POCQ availability and QoS classes



The QoS pools are:

hh_pool Available for HH class.
h_pool Available for H class and HH class.
m_pool Available for M class, H class, and HH class.
l_pool Available for all classes.
seq SF evictions only.

Warning

Register fields must be programmed so that highhigh_qos_max_cnt > high_qos_max_cnt > med_qos_max_cnt > low_qos_max_cnt ≥ 2. The maximum value that is allowed for highhigh_qos_max_cnt = (`NUM_ENTRIES_POCQ` - seq_qos_max_cnt).

This scheme enables a higher-priority QoS class to have more POCQ resources for transaction processing, and prevents a lower-priority QoS from using all the POCQ. The level of POCQ availability decreases for the lower QoS classes.

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QoS pool distribution of the POCQ is software-configurable using the qos_reservation register.

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7 Debug trace and PMU

This chapter describes the *Debug Trace* (DT) and *Performance Monitoring Unit* (PMU) features that CI-700 implements.

7.1 Debug trace system overview

CI-700 provides at-speed self-hosted *Debug Trace* (DT) capabilities.

The CI-700 DT capabilities include:

- Watchpoint-initiated and trace-tag-initiated transaction tracing
- Globally synchronized cycle counters for precise tracing
- CHI trace tag generation
- CoreSight™ ATB trace streaming
- Access to trace data through configuration registers
- Cross trigger support
- Secure debug support
- Event-based interrupts

The CI-700 DT system consists of a set of *Debug Trace Controllers* (DTCs) and *Debug Trace Monitors* (DTMs) distributed across the interconnect. DTCs are located inside HN-Ds and HN-Ts while DTMs are located inside XPs.

All DTCs, including the master DTC, have an ATB interface and the following signals:

- **DBGWATCHTRIGREQ**
- **DBGWATCHTRIGACK**
- **INTREQPMU**

The following signals are only present in the master DTC:

- **NIDEN**
- **SPNIDEN**
- **PMUSNAPSHOTREQ**
- **PMUSNAPSHOTACK**


Note

NIDEN and **SPNIDEN** are propagated from the master DTC to all DTMs. When asserted, they must remain asserted for at least 72 clock cycles. Likewise, when deasserted, they must remain deasserted for at least 72 clock cycles. This

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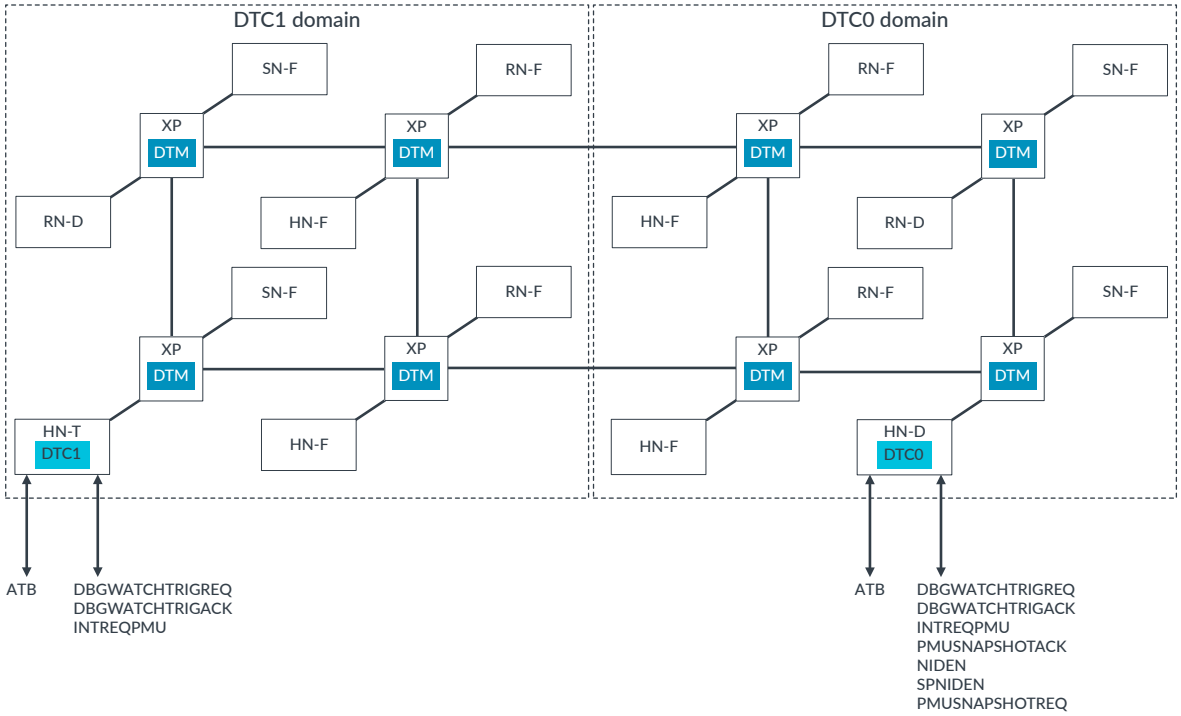
requirement ensures that all internal CI-700 components transit into their debug and trace states correctly.

The following figure shows an example DT system with two DTC domains.

Figure 7-1: Example DT system with two DTC domains



Note

We recommend one DTC domain for CI-700 configurations.

Each DTC is associated with a set of DTMs to form an exclusive DTC domain. When enabled, DTMs within a DTC domain collect trace data and transmit it to the associated DTC. The number of HN-T nodes in the mesh determines the number of DTC domains.

In a DT system comprising multiple DTCs, the DTC that is located inside the HN-D is designated as the master DTC or DTC0. You assign DTMs to DTCs by configuring XP parameters in Socrates IP Tooling platform.

Each DTC domain must be built using contiguous XPs.

The DT system implements the following functions:

- Monitoring of CHI flits at XP device ports using four sets of *WatchPoints* (WPs) in each DTM

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- Flit trace generation and storage at each DTM with control register access to trace packets
- Trace tag generation
- Debug trigger signaling and trace packet streaming over the ATB at each DTC
- Internal event-based cross trigger generation and broadcast to all DTMs
- Globally synchronized cycle counters

7.1.1 DTM changes when using extra device ports

A configuration parameter determines whether DTMs are replicated in MXPs to support extra device ports. Each port is mapped to a specific DTM and both the configuration parameter value and the overall system configuration determines how the ports are mapped.


Note

For a mesh configuration, up to four device ports are permitted per MXP. For a single-MXP configuration, up to six device ports are permitted on the MXP. For more information, see 3.11 Topology considerations when using extra device ports on page 50.

To enable support for multiple DTMs in MXPs, set the `MXP_MULTIPLE_DTM_EN` parameter = 1. If this parameter is set to 1, then the DTM in each MXP is replicated according to the number of device ports on the MXP. Each DTM supports up to two device ports. The different interconnect configurations use the following DTM mappings:

Mesh configuration

- DTM0 supports P0 and P1.
- DTM1 supports P2 and P3.

Single-MXP configuration

- DTM0 supports P0 and P1.
- DTM1 supports P2 and P3.
- DTM2 supports P4 and P5.

If the `MXP_MULTIPLE_DTM_EN` parameter = 0, each MXP has a single DTM. In this case, each DTM supports the following device ports:

Mesh configuration

Single DTM per MXP supports P0, P1, P2, and P3.

Single-MXP configuration

Single DTM per MXP supports P0, P1, P2, P3, P4, and P5.


Note

If a single DTM supports more than two ports, it might not be possible to monitor all the events on different ports at the same time. However, using a single DTM saves on the implementation area.

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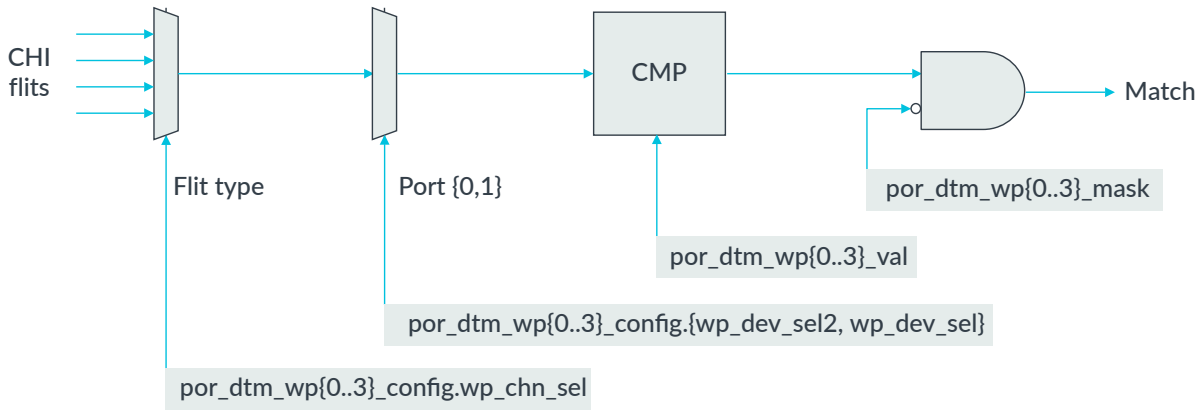
7.1.2 DTM watchpoint

A DTM has four WPs that monitor flit uploads and downloads at XP device ports.

WPs monitor flits by matching on a subset of flit fields that you specify using a pair of val and mask registers. The following figure shows the WP comparator and the registers that control this functionality.

Figure 7-2: DTM WP comparator



A WP can be configured to monitor flits from one of two XP device ports and one of four CHI channels:

- REQ
- RSP
- SNP
- DAT

In addition, you can configure the WP to perform one or more of the following tasks on detecting a flit match:

- Set trace tag bit on the flit
- Generate flit trace
- Generate cross trigger to DTC
- Generate debug trigger to DTC
- Increment PMU counters

Note

You can combine two WPs within a group for complex matching. For example, you can combine WP0 and WP1, just as you can combine WP2 and WP3.

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The four DTM WPs are assigned to flit uploads and downloads according to the following groups:

- WP0 and WP1 are assigned to flit uploads
- WP2 and WP3 are assigned to flit downloads

See 5.4.7.1 Program DTM watchpoint on page 1292 for the DTM watchpoint programming sequence.

7.1.2.1 WP match value and mask register

The WP flit matching criteria are specified using a 64-bit match value register, por_dtm_wpN_val, and a 64-bit mask register, por_dtm_wpN_mask. These registers allow matching of up to 64 bits of the flit.

N = 0, 1, 2, or 3 for the match value and mask registers.

The por_dtm_wpN_config registers also define some of the WP behavior.

To specify the value for matching, write the value into the por_dtm_wpN_val register. The value of the por_dtm_wpN_mask register specifies the bits that must be masked from the match comparison, and therefore ignored. To specify that a bit must be masked, write a 1 into the corresponding bit position in the por_dtm_wpN_mask register.

The CHI flit fields are divided into the following match groups:

REQ channel
: Primary, secondary, and tertiary match groups.

RSP channel
: Primary match group.

SNP channel
: Primary and secondary match group.

DAT channel
: Primary and secondary match group.

The following tables specify the flit fields that belong to each of the groups for the different CHI channels.

Flit matching from two different match groups requires two WPs to be combined. For example, consider if both Opcode and Addr fields of flits that are uploaded on the REQ channel are to be matched. In this situation, WP0 and WP1 must be combined, with Opcode match specified in WP0 and Addr match specified in WP1 or the opposite way. Similarly, consider if both Opcode and Addr fields of flits downloaded on the REQ channel must match. In this case, WP2 and WP3 must be combined in a similar way.

The following table shows REQ channel width and bit ranges for the primary match group.

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Table 7-1: REQ channel: primary match group

Field	Width	Bit range
SRCID/TGTID	11	[10:0]
STASHNID/RETURNNID/SLCREPHINT[6:0]	11	[21:11]
StashTgtValid/Endian/Deep	1	[22:22]
{StashLPValid, StashLP[4:0]}	6	[28:23]
OPCODE	7	[35:29]
SIZE	3	[38:36]
NS	1	[39:39]
ALLOWRETRY	1	[40:40]
ORDER	2	[42:41]
PCRDTYPE	4	[46:43]
LPID	5	[51:47]
GroupIDExt	3	[54:52]
EXPCOMPACK	1	[55:55]
RSVDC	8	[63:56]

The following table shows REQ channel width and bit ranges for the secondary match group.

Table 7-2: REQ channel: secondary match group

Field	Width	Bit range
QOS	4	[3:0]
ADDR	48	[51:4]
Reserved	4	[55:52]
LIKELYSHARED	1	[56:56]
MEMATTR	4	[60:57]
SNPATTR	1	[61:61]
EXCL/SNOOPME	1	[62:62]
TRACETAG	8	[63:63]

The following table shows REQ channel width and bit ranges for the tertiary match group.

Table 7-3: REQ channel: tertiary match group

Field	Width	Bit range
SRCID/TGTID	11	[10:0]
OPCODE	7	[17:11]
MPAM	11	[28:18]
TagOp	2	[30:29]
ADDR[38:6]	33	[63:31]

The following table shows RSP channel width and bit ranges for the primary match group.

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Table 7-4: RSP channel: primary match group

Field	Width	Bit range
QOS	4	[3:0]
SRCID/TGTID	11	[14:4]
OPCODE	5	[19:15]
RESPERR	2	[21:20]
RESP	3	[24:22]
FWDSTATE/DATAPULL	3	[27:25]
CBUSY	3	[30:28]
DBID	12	[42:31]
PCRDTYPE	4	[46:43]
TagOP	2	[48:47]
TRACETAG	1	[49:49]
DEVEVENT	2	[51:50]
Reserved	2	[53:52]

The following table shows SNP channel width and bit ranges for the primary match group.

Table 7-5: SNP channel: primary match group

Field	Width	Bit range
SRCID	11	[10:0]
FWDTXNID/{2'b0, STASHLPIDVALID, STASHLPID[4:0]}/VMIDEXT[7:0]	8	[18:11]
FWDNID	11	[29:19]
OPCODE	5	[34:30]
NS	1	[35:35]
DONOTDATAPULL /DONOTGOTOSD	1	[36:36]
RETTOSRC	1	[37:37]
TRACETAG	1	[38:38]
QOS	4	[42:39]
MPAM	11	[53:43]

The following table shows SNP channel width and bit ranges for the secondary match group.

Table 7-6: SNP channel: secondary match group

Field	Width	Bit range
SRCID	11	[10:0]
ADDR	48	[58:11]
Reserved	1	[59:59]

The following table shows DAT channel width and bit ranges for the primary match group.

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Table 7-7: DAT channel: primary match group

Field	Width	Bit range
QOS	4	[3:0]
SRC/TGTID	11	[14:4]
HOMENID	11	[25:15]
OPCODE	4	[29:26]
RESPERR	2	[31:30]
RESP	3	[34:32]
DATASRC/FWDSTATE/DATAPULL	4	[38:35]
CBUSY	3	[41:39]
DBID	12	[53:42]
CCID	2	[55:54]
DATAID	2	[57:56]
POISON	4	[61:58]
DEVEVENT	2	[63:62]

The following table shows DAT channel width and bit ranges for the secondary match group.

Table 7-8: DAT channel: secondary match group

Field	Width	Bit range
SRC/TGTID	11	[10:0]
OPCODE	4	[14:11]
RESPERR	2	[16:15]
RESP	3	[19:17]
TagOp	2	[21:20]
Tag	8	[29:22]
TU	2	[31:30]
DBID	12	[43:32]
TRACETAG	1	[44:44]
CHUNKV	2	[46:45]
DEVEVENT	2	[48:47]
RSVDC	8	[56:49]

7.1.3 DTM FIFO buffer

Traces captured by the DTM are stored in a four-entry DTM FIFO buffer. Each entry is 176-bits wide.

Entries are allocated to all enabled WPs as required. Trace data from WPs are packed based on the trace data format and stored within each entry to efficiently use the limited buffer storage. Therefore, an entry might contain trace data from multiple flits captured at different times.

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As each FIFO entry is filled, trace data from that entry is sent to the DTC for streaming out through the ATB interface.

7.1.3.1 Trace data format

CI-700 supports several trace data formats.

The 3-bit packet type encoding in the DTM WP configuration register (por_dtm_wp{0..3}_config.wp_pkt_type) specifies the trace data format. The following table shows the supported trace data formats and their packet type encodings.

Table 7-9: Trace data formats

Packet type	Trace data format		Size	Maximum number of traces per FIFO entry
000	TXNID[11:0]		12 bits	14
001	{OPCODE[6:0],TXNID[11:0]}		19 bits	9
010	{3'b000,{TGTID[10:0], SRCID[10:0], OPCODE[6:0],TXNID[11:0]}		44 bits	4
011	Reserved		-	-
100	Control flit (see the following tables for field descriptions).	REQ	170 bits	1
		RSP	77 bits	
		SNP	119 bits	
		DAT	112 bits	
101	DATA[127:0]		-	-
110	DATA[255:128]		-	-
111	Reserved		-	-

Trace data is packed into a DTM FIFO buffer entry so that the higher-order bytes contain older trace data. For example, if the trace data format is set to TXNID (type 0) and three TXNIDs (trace data) are received in the order 0x001, 0x002, 0x003, then the trace FIFO entry is set to:

- 0000_0000_0000_0000_0000_0000_0000_0100_2003

When you set the trace packet type to pack control flit information, the trace data format is different for each type of control flit. The following table shows the REQ control flit format when MPAM is either enabled or disabled.

Table 7-10: REQ control flit

Field	Width	Bit range (MPAM enabled)	Bit range (MPAM disabled)
QoS	4	[3:0]	
TgtID	11	[14:4]	
SrcID	11	[25:15]	
TxnID	12	[37:26]	
StashTgtID / ReturnNID / SLCRepHint[6:0]	11	[48:38]	

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Field	Width	Bit range (MPAM enabled)	Bit range (MPAM disabled)
StashTgtValid / Endian	1	[49:49]	
ReturnTID[9:0] / {4'b0, StashLPValid, StashLP[4:0]}	12	[61:50]	
Opcode	6	[68:62]	
Size	3	[71:69]	
NS	1	[72:72]	
LikelyShared	1	[73:73]	
AllowRetry	1	[74:74]	
Order	2	[76:75]	
PCrdType	4	[80:77]	
MemAttr	4	[84:81]	
SnpAttr	1	[85:85]	
LPID	5	[90:86]	
GroupIDExt	3	[93:91]	
Excl/SnoopMe	1	[94:94]	
ExpCompAck	1	[95:95]	
TagOp	2	[97:96]	
TraceTag	1	[98:98]	
MPAM	11	[109:99]	-
Addr	52	[161:110]	[150:99]
RSVDC	8	[169:162]	[158:151]
Total	170 (MPAM enabled) / 159 (MPAM disabled)	-	

The following table contains RSP control flit information.

Table 7-11: RSP control flit

Field	Width	Bit range
QoS	4	[3:0]
TgtID	11	[14:4]
SrcID	11	[25:15]
TxnID	12	[37:26]
Opcode	5	[42:38]
FwdState / 2'b0, DataPull	3	[45:43]
RespErr	2	[47:46]
Resp	3	[50:48]
CBusy	3	[53:51]
DBID	12	[65:54]
PCrdType	4	[69:66]
TraceTag	1	[70:70]
DEVEVENT	2	[72:71]

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Field	Width	Bit range
Reserved	1	[73:73]
TagOp	2	[75:74]
Reserved	1	[76:76]
Total	77	-

The following table contains SNP control flit information, when MPAM is either enabled or disabled.

Table 7-12: SNP control flit

Field	Width	Bit range (MPAM enabled)	Bit range (MPAM disabled)
QoS	4	[3:0]	
SrcID	11	[14:4]	
TxnID	12	[26:15]	
FWDNID	11	[37:27]	
FWDTXNID[9:0] / {4'b0, StashLPValid, StashLP[4:0]} / {2'b00, VMIDExt[7:0]}	12	[49:38]	
Opcode	5	[54:50]	
NS	1	[55:55]	
DoNotGoToSD / DoNotDataPull	1	[56:56]	
RetToSrc	1	[57:57]	
TraceTag	1	[58:58]	
MPAM	11	[69:59]	-
Addr	49	[118:70]	[108:60]
Total	119 (MPAM enabled) / 108 (MPAM disabled)	-	

The following table contains DAT control flit information.

Table 7-13: DAT control flit

Field	Width	Bit range
QoS	4	[3:0]
TgtID	11	[14:4]
SrcID	11	[25:15]
TxnID	12	[37:26]
HomeNID	11	[48:38]
Opcode	4	[52:49]
RespErr	2	[54:53]
Resp	3	[57:55]
FwdState / {2'b0, DataPull}	4	[61:58]
CBusy	3	[64:62]
DBID	12	[76:65]

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Field	Width	Bit range
CCID	2	[78:77]
DataID	2	[80:79]
TagOp	2	[82:81]
Tag	8	[90:83]
TU	4	[94:81]
TraceTag	1	[95:95]
RSVDC	8	[103:96]
Poison	4	[107:104]
CHUNKV	2	[109:108]
DEVEVENT	2	[111:110]
Total	112	-

See 8.11 DEVEVENT on page 1369 for more information.


Note

CHUNKV[1:0] denotes whether the upper or lower 128 bits of data are valid.

7.1.4 Read mode

Read mode provides an alternate way to access trace data that is stored in the DTM trace FIFO buffer, through configuration register access.

Each entry in the FIFO buffer is mapped to three 64-bit configuration registers, dtm_fifo_entry{0..3}_X, where X = 0, 1, or 2.

To enable read mode, set the trace_no_atb bit in the por_dtm_control register. Setting this bit clears all FIFO entries and resets the por_dtm_fifo_entry_ready register.

In this mode, each FIFO entry is allocated to the corresponding WP. For example, por_dtm_fifo_entry0_{0..2} is allocated to WP0 and por_dtm_fifo_entry1_{0..2} is allocated to WP1.

The availability of WP trace data for each FIFO entry is reflected in the corresponding bit in the por_dtm_fifo_entry_ready register. When a FIFO entry is full, the corresponding status bit is set, indicating that the trace data is ready to be read. Subsequent writes into that FIFO entry are disabled until the status bit is cleared. A write of 1 clears the status bit and enables the corresponding FIFO entry to capture subsequent trace data.

7.1.5 DTC

DTCs control DTMs.

The main features of the DTC are:

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- Trace packing, generation, and streaming through ATB interface
- Time stamping of traces
- Global synchronized cycle counters in all units (16-bit)
- ATB flush of DTM and DTC (**AFREADY** might be asserted several cycles after trace data output as DTC must receive all flush responses from DTMs)
- Watchpoint trigger event-based interrupt
- Eight sets of performance counters (32-bit) with shadow registers, which are paired with one or more DTM local counters
- PMU snapshot of DTM and DTC.
- PMU overflow interrupt.

See 5.4.7.2 Program DTC on page 1293 for the DTC programming sequence.

7.1.6 ATB packets

Each DTC has an ATB interface and generates ATB packets to send downstream through this interface. There are different varieties of ATB packets which are used for different functions.

Each DTC aggregates flit trace data from the DTMs into the DTC trace FIFO, packetizes them, and sends them out on its ATB interface. The DTCs also send other control and debug packets through this interface. There are various packet formats that are used on the ATB interface, which are described in the following sections:

- 7.1.6.1 Trace data packet format on page 1332
- 7.1.6.2 Alignment sync packet format on page 1333
- 7.1.6.3 Time stamp packet format on page 1334
- 7.1.6.4 Cycle counting packet format on page 1334
- 7.1.6.5 Trace stream example on page 1335

7.1.6.1 Trace data packet format

Trace data packet contains a 4B header and a payload of variable size.

The following figure shows the packet header.

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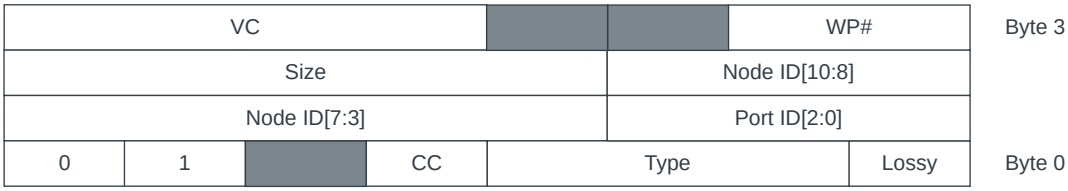
Figure 7-3: Trace data packet header



The packet header contains the following fields:

VC CHI channel.

0b0000	REQ
0b0001	RSP
0b0010	SNP
0b0011	DAT

DEV Device port number (0-5).
WP# Watchpoint number that captured the trace (0-3).
Type Packet format type.
Size Payload size, which is specified as (number of bytes – 1).
NodeID CHI node ID[10:3], which reflects the (X,Y) coordinates of the XP where the trace was captured.
CC Cycle counter. When set, this field indicates that a 2B cycle count is included in the packet after the payload.

The following key points must be observed:

- For packet type `100`, the leading zeros in upper-order bytes of the trace data payload are compressed and not transmitted. The payload Size field in the trace packet header is adjusted accordingly. For example, trace data = `0000_0000_0000_0000_0000_0000_0000_0001_0203` is sent as `01_0203`, with Size = 2 (indicating 3B transferred).
- The WP field selection for match might be different from the type of payload that is generated from the matching. When WPs are combined, the lower watchpoint number is specified as the WP# in the trace packet header.
- Trace data is of variable length. The expected number of bytes, not including the header, is (Size + 1). With CC, another 2B are included at the end of the trace data.
- Whenever the previous packets cannot be transmitted in full, a lossy bit is asserted for the immediate next packet. A separate lossy bit is maintained for each of the watchpoints.

7.1.6.2 Alignment sync packet format

The alignment sync delimits trace start.

The alignment sync packet is 20B long and comprises 15B of zeros followed by `0x80`.

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The alignment sync packet is the first packet that is sent after tracing is enabled. Also, you can configure the DTC to send the alignment sync packet periodically by programming the por_dt_trace_control register.

7.1.6.3 Time stamp packet format

The time stamp packet carries the SoC timer information. The time stamp is used to align the sequence of trace events across the SoC.

The time stamp packet is sent opportunistically under the following circumstances when the DTC FIFO has enough space to accommodate the time stamp packet:

- After each alignment sync packet is sent
- When flush is complete
- Periodically based on the setting of the timestamp_period field of the por_dt_trace_control register and only when trace packets have been sent after the last time stamp packet

The following figure shows the time stamp packet format.

Figure 7-4: Time stamp packet



The time stamp packet contains the following fields:

TS# 3-bit encoding of the size of time stamp that is specified as (number of bytes – 1)

CC When set, indicates that a 2B cycle count is included in the packet after the payload

7.1.6.4 Cycle counting packet format

Trace packets include an **OPTIONAL** attached cycle counter.

Each watchpoint includes a configuration bit. The logical operator AND is used on the configuration bit and global cycle count enable. The following figure shows a typical cycle counting scenario.

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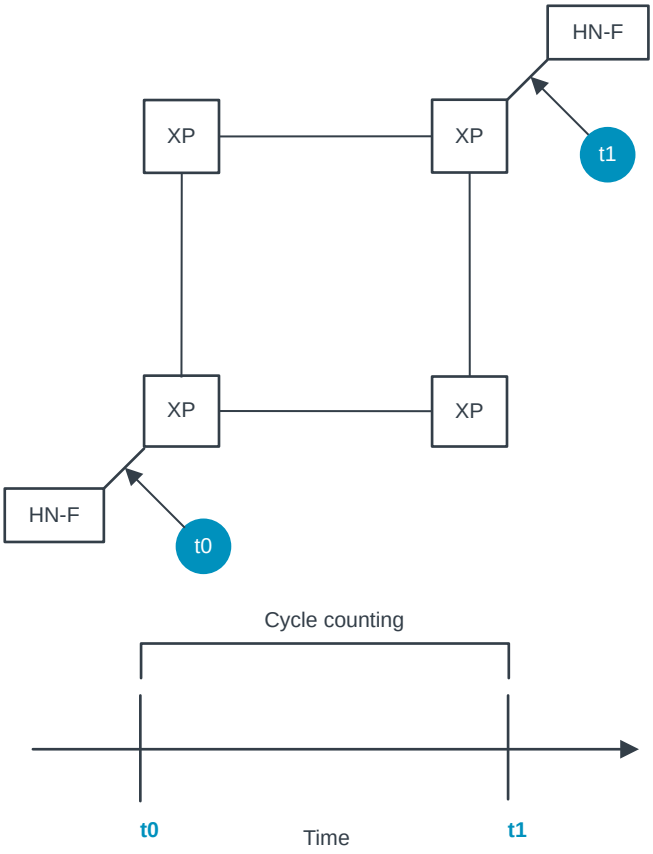
Figure 7-5: Cycle counting



The cycle counter payload is 2B and the CC bit in the trace packet header indicates the cycle counter payload. Cycle counters across the interconnect are turned on and off synchronously. This feature ensures that all of them have the same time stamp value.

7.1.6.5 Trace stream example

DTCs send out trace data on the ATB bus as a trace stream.

The following figure shows an example trace stream. It consists of:

- 4B trace packet header
- <*M*>B trace data
- 2B cycle count
- 1B time stamp header
- <*N*>B time stamp
- 2B cycle count

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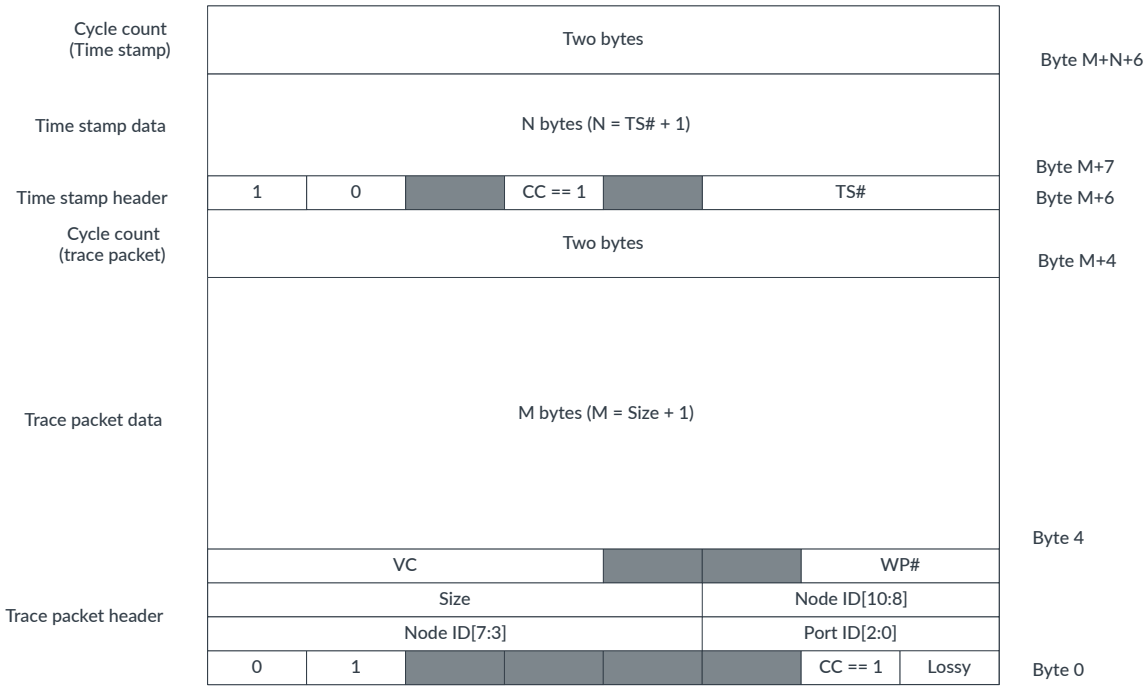
Figure 7-6: Trace stream



7.2 DT usage examples

To help you use the CI-700 DT features, we describe some example use cases of the DT system and example programming for those use cases.

7.2.1 Flit tracing

CI-700 can trace individual flits at device interfaces at each XP.

You can program DTM WPs to monitor flit uploads and downloads at each of the two XP device ports on any of the four CHI channels:

- REQ
- RSP
- SNP
- DAT

You can use a set of value and mask registers to define a subset of flit fields that are then used for matching at the WP.

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On a match, WPs capture and store flit fields into trace buffers so that they can be used for debug. The generated trace can then be streamed out on the ATB interface or accessed using a control register interface.

For more information about the format of the value and mask registers, and the format of trace packets, see 7.1.2.1 WP match value and mask register on page 1324 and 7.1.3.1 Trace data format on page 1328.

7.2.1.1 Flit tracing example

CI-700 can trace individual flits at device interfaces at each XP.

For more information, refer to 5.4.7.1 Program DTM watchpoint on page 1292.

This section shows an example of setting up a simple trace of REQ flits. The example corresponds to a ReadShared transaction to address=X initiated by RN-F2 and sending out the trace packets on the ATB bus.

To monitor REQ flits uploaded from RN-F2, set up watchpoints (WPs) inside XP connected to RN-F2. The Opcode and Addr fields are mapped to the primary and secondary match registers respectively. Therefore, you must set up two WPs, one to monitor the Opcode and the other to monitor the Addr.

To set up these WPs:

1. Program WP0 (upload WP) to monitor REQ.Opcode:
   a. Set por_dtm_wp0_val and por_dtm_wp0_mask registers to match on Opcode=ReadShared
   b. Set por_dtm_wp0_config to:
      1. Select upload device port, {wp_dev_sel2, wp_dev_sel}=RN-F2_port
      2. Select flit channel, wp_chn_sel=REQ
      3. Match format group to primary for Opcode match wp_grp= 0
      4. Set combined mode to gang-up WP0 and WP1, wp_combine = 1
      5. Enable REQ flit trace packet generation, set wp_pkt_type and wp_pkt_gen = 1
2. Program WP1, upload WP, to monitor REQ.Addr as follows:
   a. Set por_dtm_wp1_val and por_dtm_wp1_mask registers to match on Addr = X
   b. Set por_dtm_wp1_config to:
      1. Select upload device port, {wp_dev_sel2, wp_dev_sel} = RN-F2_port
      2. Select flit channel, wp_chn_sel = REQ
      3. Match format group to secondary for Addr match, wp_grp = 1


Note

In combined mode, use WP0 config settings to enable trace generation.

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3. To enable trace generation in the WP, set por_dtm_control.trace_tag_enable = 1
4. Set por_dtm_control.dtm_enable = 1
5. Program por_dt_traceid.traceid according to the *Arm® CoreSight™ Architecture Specification*. The supported range of values is `0x01-0x6F`
6. Program por_dt_dtc_ctl to enable tracing, dt_en = 1

7.2.2 Trace tag

CI-700 can generate trace tags at the device interfaces and propagate them to destination devices.

This feature enables a set of flits corresponding to a specific transaction or set of transactions that match a specific criterion to be tagged for tracing.

For example, using the trace tag mechanism, flits from all four CHI channels can be monitored:

- REQ
- RSP
- SNP
- DAT

An example of a monitored transaction is a memory read transaction to a specific address, which is then tagged for tracing.

7.2.2.1 Trace tag generation

Internal XPs and external RN-F or SN-F devices can generate a trace tag. The generated trace tag is reflected in the TRACETAG field of the uploaded flit.

Inside the XP, DTM WPs generate the trace tag by matching on flits uploaded at the corresponding XP device port. The DTM WPs can be programmed to match on a flit on any of the four CHI channels: REQ, RSP, DAT, and SNP.

The WP generates a trace tag when there is a match and the trace_tag_enable field of the por_dtm_control register is set to 1.

You can program DTM WPs to match on a flit on any CHI channel and on any device port. However, for debug, it is most useful to program WPs to match on REQ flits uploaded at the RN and HN-F device ports. We recommend this programming because REQ flits are the starting flits that originate new transactions. When tagged, subsequent RSP, SNP, and DAT flits that relate to the same transaction carry the trace tag.

If the following conditions are all true, the XP does not generate the trace tag:

- Flit transfer takes place from one device port to the other device port, within the same XP.
- The flit destination device is not an HN.
- The flit transfer to its destination occurs one cycle after the XP receives it.

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7.2.2.2 Trace tag propagation

All CI-700 devices forward on the trace tag, when asserted, from a received flit corresponding to a transaction to all subsequent flits associated with that transaction.

The HN-F also propagates the trace tag from the source transaction to spawned transactions such as SLC evictions and SF back invalidations.

Using the logical operator OR, the trace tag that is generated inside the XP is combined with the TRACETAG field of the received flit. The resultant value is then sent in the TRACETAG field of the flit transmitted to the destination device.

7.2.2.3 Trace tag trace packet generation

If a WP is set up to generate trace packets, then flits with trace tags can trigger trace packet generation. For this process to occur, the flit must also be on the CHI channel and device port that the WP is monitoring.

The wp_pkt_gen field of the por_dtm_wpN_config registers enables trace packet generation for a specific WP. If trace packet generation is enabled, then any flit that the WP sees with the TRACETAG field asserted generates a trace packet. The selected CHI channel and device port determine which flits the WP sees.

The following fields of the por_dtm_wpN_config register determine the CHI channel and device port that the WP monitors:

- The wp_chn_sel field determines the WP CHI channel.
- The wp_dev_sel2 and wp_dev_sel fields determine the WP device port.

If a trace packet is generated, the wp_pkt_type field of the por_dtm_wpN_config register determines the type of trace packet that the WP generates.

This trace packet is generated whenever TRACETAG is asserted in a flit. A WP match on the por_dtm_wpN_val and por_dtm_wpN_mask register values is not required.

7.2.2.4 Trace tag example programming

This example programming outlines a trace tag scenario-based trace generation with synchronized cycle counts.

For more information about watchpoint programming, see 5.4.7.1 Program DTM watchpoint on page 1292.

This example programming sets up a simple trace of REQ flits. The example corresponds to a ReadShared transaction to address = X. RN-F 2 initiates the transaction in the mesh and the WP sends trace packets out on the ATB bus.

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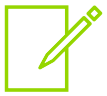
To monitor REQ flits uploaded from RN-F 2, set up WPs inside the XP that RN-F 2 is connected to. For REQ flits, the Opcode and Addr fields are mapped to the primary and secondary match registers respectively. Therefore, you must set up two WPs, one to monitor the Opcode and the other to monitor the Addr.

To set up these WPs:

1. Program WP0, upload WP to monitor REQ.Opcode:
   a. Set por_dtm_wp0_val and por_dtm_wp0_mask registers to match on Opcode = ReadShared
   b. Set por_dtm_wp0_config to:
      1. Select upload device port, wp_dev_sel2,wp_dev_sel} = RN-F 2 port
      2. Select flit channel, wp_chn_sel = REQ
      3. Match format group to primary for Opcode match, wp_grp = 0
      4. Set combined mode to gang-up WP0 and WP1, wp_combine = 1
      5. Enable REQ flit trace packet generation, set wp_pkt_type and wp_pkt_gen = 1
2. Program WP1, upload WP, to monitor REQ.Addr:
   a. Set por_dtm_wp1_val and por_dtm_wp1_mask registers to match on Addr = X
   b. Set por_dtm_wp1_config to:
      1. Select upload device port, {wp_dev_sel2, wp_dev_sel} = RN-F 2 port
      2. Select flit channel, wp_chn_sel = REQ
      3. Match format group to secondary for Addr match, wp_grp = 1


Note

In combined mode, use WP0 config settings to enable trace generation.

3. To enable trace tag generation in the WP, set dtm_control.trace_tag_enable = 1
4. Set dtm_control.dtm_enable = 1
5. Program por_dt_traceid.traceid according to the *Arm® CoreSight™ Architecture Specification*. The supported range of values is `0x01-0x6F`.
6. Program por_dt_dtc_ctl to enable tracing, dt_en = 1

7.2.3 Debug watch trigger events

DTM WPs can be programmed to match on specific flits and generate a debug watch trigger event to the DTC.

You can program the DTC to signal the debug watch trigger event in one or both of the following ways:

- Signal a debug watch trigger interrupt on the **DBGWATCHTRIGREQ**/**DBGWATCHTRIGACK** interface

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Note

This interface is based on a four-phase handshake protocol.

- Signal an ATB trace trigger with ATID `0x7D` on the ATB interface

In a system with multiple DTCs, each DTC has its own ATB interface on which it signals ATB trace triggers from DTMs within its DTC domain. Multiple DTCs also have their own **DBGWATCHTRIGREQ** / **DBGWATCHTRIGACK** interfaces on which they signal debug watch trace interrupts.

7.2.4 Cross trigger

CI-700 can trigger DTMs based on specific events occurring elsewhere in the system.

By default, DTMs start monitoring and tracing flits without waiting for another event. The cross trigger feature allows flit monitoring and tracing to be delayed until after the events of interest are observed in the system.

The cross trigger event is set up in two steps:

1. Set up DTM WPs to monitor flits and generate traces
2. Other DTM WPs (in the same XP or different XPs) are set up to generate a cross trigger on specific events to the DTC. The DTC is programmed to trigger the DTMs in step 1.

7.2.4.1 Cross trigger example programming

CI-700 can trigger DTMs based on specific events occurring elsewhere in the system.

For more information, refer to 5.4.7.1 Program DTM watchpoint on page 1292.

This example uses trace DAT flits corresponding to a ReadShared transaction to address-X that originated at RN-F 2. There have also been 10 WriteNoSnoops uploaded to the HN-D.

1. Set WP or WPs at all DAT download ports to generate DAT flit traces for ReadShare transactions from RN-F 2 to address-X.
   a. Program WP2 and WP3, which are at the DAT download ports, to trace DAT flits:
      1. Set por_dtm_wp2_val/mask and por_dtm_wp3_val/mask registers to match on SRCID = RN-F 2, opcode = ReadShared, and address = X.
      2. Set por_dtm_wp2_config and por_dtm_wp3_config to the respective download device ports ({wp_dev_sel2, wp_dev_sel} = 0 and {wp_dev_sel2, wp_dev_sel} = 1). Select the DAT channel by setting the wp_chn_sel bit to the DAT encoding.
   b. Enable the WP by setting the dtm_enable bit of the por_dtm_control register to 1.
2. Set up WP at HN-D upload port to monitor WriteNoSnoop flits.
   a. Program WP0 (upload WP) to monitor and enable cross trigger REQ. Opcode as follows:

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1. Set por_dtm_wp0_val/mask registers to match on Opcode = WriteNoSnoop.
2. Set dtm_wp0_config to:
   a. Select upload device port ({wp_dev_sel2, wp_dev_sel} = HN-D port).
   b. Flit channel (wp_chn_sel = REQ).
   c. Match format group to primary for Opcode match (wp_grp = 0).
   d. Enable cross trigger (wp_ctrig_en = 1).

b. Enable WP.
- Set the dtm_enable field of the por_dtm_control register = 1.

3. Set up counter in DTC to count ten trigger events from step 3.
- Program por_dt_dtc_ctl as follows:
  a. Set cross trigger count (cross_trigger_count = 10).
  b. Enable waiting for HN-D WP trigger event (dt_wait_for_trigger = 1).
  c. Enable DTC (dt_en = 1).

7.2.4.2 Sample profile

CI-700 supports the Armv8.2 sample extension.

WPs can be programmed to monitor channel, opcode, and related PM items. The sampling interval counter register, por_dtm_pmsicr, counts down with each match. When the counter reaches zero, the trace tag field of the next matched transaction is asserted. At the same time, the counter is reloaded with the programmed value from the sampling interval reload register, por_dtm_pmsirr, and the next countdown cycle begins.

If the CI-700 configuration uses a single DTM per XP, then only one outstanding transaction is expected. Therefore, there is only one set of por_dtm_pmsicr and por_dtm_pmsirr registers per XP. Por_dtm_pmsicr is 24 bits, and the lower 8 bits of por_dtm_pmsirr are zero.


Note

If your configuration uses multiple DTMs per XP, then extra sample profile registers are instantiated.

In general, Secure transactions are allowed to be tagged and traced with the secure_debug_disable field of the por_dt_secure_access register. When this bit is set, Secure transactions are not traced.

7.3 PMU system overview

CI-700 includes *Performance Monitoring Unit* (PMU) capabilities.

The PMU offers the following features:

- Local and global performance counters with shadow registers

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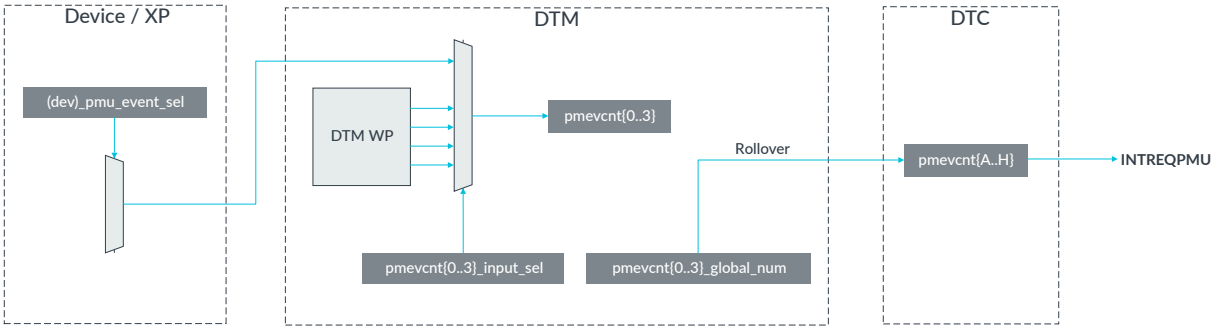
- PMU snapshot across all internal CI-700 devices

The PMU consists of local performance counters in the DTMs and global performance counters in the DTCs. The following figure shows this structure of local and global performance counters.

Figure 7-7: PMU local and global performance counters



For the various PMU programming sequences, see 5.4.8 PMU system programming on page 1294.

The PMU system performs the following tasks:

- Selects PMU event from XP, the local watchpoint, and the devices on XP device ports
- Operates four local PMU counters (4 × 16b)
- Operates eight global PMU counters (8 × 32b) associated with the local counters
- Snapshot
- Overflow interrupt from global PMU counters

The PMU counter value can be copied over into the shadow registers when there is either:

- A request of snapshot through input pin **PMUSNAPSHOTREQ**
- A write into the ss_req field of the por_dt_pmsrr register within the DTC

On receiving a snapshot request, a DTC sends a snapshot request to all DTMs. Multiple snapshot requests are collapsed into a single request. On receiving PMU snapshot packets from all DTMs, rollover information is updated at the global counters, and the counter value is copied to the shadow registers.

7.4 Secure debug support

The **SPNIDEN** input and the value of the secure_debug_disable field of the por_dt_secure_access register control the Secure debug state.

Secure debug is enabled when **SPNIDEN** is asserted, or when the secure_debug_disable bit of the por_dt_secure_access register is set to 0. The default value of this bit is 0.

When Secure debug is enabled, all events can be counted and all flits can be traced.

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When Secure debug is disabled, all events with **UNKNOWN** Secure state are not counted and all flits with **UNKNOWN** Secure state are not traced.

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8 Performance optimization and monitoring

This chapter describes the performance optimization techniques and *Performance Monitoring Unit* (PMU) that system integrators can use to optimize the functionality of the interconnect implementation.

8.1 Performance optimization guidelines

There are some restrictions when optimizing CI-700.

To obtain maximum performance from CI-700, the system integrator must be aware of the following information:

RN-I

When request ordering is not required, transaction requests must be dispatched with non-overlapping IDs to ensure optimal bandwidth operation. Large Burst transactions, in other words transactions larger than 64B, must be split into 64B or smaller Burst transactions. In addition, set **AxSIZE** to the AXI bus width of the RN-I to fully utilize the available bandwidth.

For example, if the AXI bus width is:

128b Set **AxSIZE** = 4 (16B)
256b Set **AxSIZE** = 5 (32B)
512b Set **AxSIZE** = 6 (64B)

Read or write requests to different parts of the same cache line must be combined into a single cache line request. For example, multiple (partial) WriteUnique transactions must be combined into a single WriteUnique or a single WriteLineUnique transaction. In the resultant transaction, all bytes in the cache line must be written.

Based on the transaction attributes, RN-I can enforce more ordering on transactions, targeting device memory downstream of HN-I, affecting the overall achievable bandwidth.

HN-F

High temporal locality of address usage in transactions can cause same-address dependencies to occur for transactions with addresses to overlapping cache lines. This condition results in higher latency because of serialization delays between these transactions. CI-700 is microarchitected to avoid hot spotting in the HN-F partitions or in the memory controllers. However, this condition is unavoidable in cases of temporally local same-address usage.

HN-I

Stream of interleaved reads and writes targeting the same peripheral downstream of HN-I results in higher latencies on these transactions. It also could result in serialization delays between these reads and writes. Arm recommends that read and write transactions are not interleaved when targeting the same peripheral.

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8.2 About the Performance Monitoring Unit

CI-700 provides access to various performance events. Some of these events are unique to and originate in a specific CI-700 component. Some are available by using watchpoints in the DTM watchpoint in the XP where the component is located.

The PMU input source must be configured to select the watchpoint input, according to the instructions in 5.4.8.1 Set up PMU counters on page 1294.

This chapter describes the performance events and the relevant use cases for most of those events. For information about the infrastructure and logic that enable general utility of the performance monitor events, see 7 Debug trace and PMU on page 1320.

8.2.1 Cycle counter

The cycle counter is used to track time.

You can reset this counter to initiate the time interval over which you want to capture the events.

PMU_CYCLE_COUNTER
Cycle counter.

The global clock signal or signals clock the cycle counter. Therefore, the cycle counter is not incremented during periods of HCG when the clocks are stopped.

8.3 HN-F performance events

The HN-F performance analysis counters are used to monitor cache behavior.

For a particular cache, the cache miss or hit rate is used to measure the capacity of the cache, and the location for certain applications. To measure the cache miss rate, the performance monitor counters count the number of instances of cache accesses and cache misses.

8.3.1 Cache performance

Cache performance events are required to calculate the cache miss rate and the cache allocation.

HN-Fs support MPAM-related PMU events. See the *Arm® Architecture Reference Manual Supplement Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A* for more information about configuration.

The following sections describe the cache performance events.

Cache miss rate

The cache events that are required to calculate the cache miss rate are:

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PMU_HN_CACHE_MISS_EVENT

Counts the total cache misses. A miss results from a first-time lookup and is high priority.

PMU_HNSLC_SF_CACHE_ACCESS_EVENT

The total number of cache accesses. An access is first-time and high priority.



The performance counter architecture allows up to four HNs to collect the cache miss rate for each DTC domain. In a system with multiple DTC domains, more than four HNs can collect the cache miss rate. However, because of the CI-700 microarchitecture, the cache miss rate that is measured at one HN-F within an SCG is a good proxy for the cache miss rate of the remaining HN-Fs.

Calculate the cache miss rate as follows:

Figure 8-1: Cache miss rate

$$\text{Cache miss rate (\%)} = \frac{\text{Total cache misses}}{\text{Total cache accesses}} \times 100$$

Certain request types can cause multiple cache accesses:

- Lookup.
- Tag update.
- Victim selection.
- Cache fill.

Event counting is therefore limited to first time accesses only. For example, for a ReadUnique transaction that leads to an SLC hit, PMU_HNSLC_SF_CACHE_ACCESS_EVENT is only counted the first-time cache lookup is performed. The tag update is not counted as a cache access. Similarly, for WriteBack or Write*Unique transactions with an SLC allocate hint, only the first instance of an SLC lookup is counted as an access and hit or miss. The eventual victim selection and cache fill are not counted as further accesses.

Cache allocations

The cache allocation event counts the number of times an HN-F SLC cache is allocated. It provides an approximate cache usage for this particular application over a specific time slice. This event does not check whether the application has any hot sets.

PMU_HN_CACHE_FILL_EVENT

Counts all cache line allocations to SLC cache.

All cache line writes, that is, Write*Unique, WriteBack, and Evictions that are allocated in SLC cache, are counted towards this event.

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8.3.2 HN-F counters

Applications can bottleneck on one or more HN-Fs because they frequently target an address or a stream of addresses.

The following POCQ occupancy and request retry events are used to monitor possible performance loss in the system:

PMU_HN_POCQ_RETRY_EVENT

The total number of requests that have been retried.

PMU_HN_POCQ_REQS_RECVD_EVENT

The total number of requests that the HN-F receives.

Requests that cannot be queued in the POCQ, because of lack of credits, are retried. The HN-F responds with a RetryAck response, and the request waits for a static credit. This wait period indicates whether a lack of credits is causing the bottlenecks, and also shows if the latency of requests is very high.

Calculate the message retry rate as follows:

Figure 8-2: HN-F message retry rate

$$\text{HN-F message retry rate (\%)} = \frac{\text{HN-F total messages retried}}{\text{HN-F total messages received}} \times 100$$

8.3.3 SF events

There are three snoop events that can be counted.

The following sections describe the SF performance events.

SF miss rate

This event measures the amount of memory controller traffic that is generated. It can also be used to measure the efficiency of the SF.

PMU_HN_SF_HIT_EVENT

Measures the number of SF hits.

Calculate the SF hit rate as follows:

Figure 8-3: SF hit rate

$$\text{Snoop filter hit rate (\%)} = \frac{\text{Total snoop filter hits}}{\text{Total SLC lookups}} \times 100$$

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SF accesses are only counted for first-time lookups, and not for the victim selection accesses or SF fills. Because the SLC lookup and SF lookups are parallel, the SLC lookups can be used to calculate the SF hit rate.

SF evictions

This event measures the frequency of SF evictions.

PMU_HN_SF_EVICTIONS_EVENT

Measures the number of SF evictions when cache invalidations are initiated.

Snoops sent and received with hit rate

These events measure the amount of shared data across clusters for a specific application, using snoop hits or misses.

PMU_HN_SNOOPS_SENT_EVENT

Number of snoops sent. Does not differentiate between broadcast or directed snoops.

PMU_HN_SNOOPS_BROADCAST_EVENT

Number of snoop broadcasts sent.

Calculate the snoops sent and received rate as follows:

Figure 8-4: Sent and received snoops rate

$$\text{Shared data (\%)} = \frac{\text{Total snoops broadcast}}{\text{Total snoops sent}} \times 100$$

The number of broadcast and total snoops measures the shared data invalidations.

8.3.4 System-wide events

The *Memory Controller* (MC) request retries determine whether the MC is the bottleneck in the system, which can cause higher request latencies.

The following events can be counted:

PMU_HN_MC_RETRIES_EVENT

Number of requests that are retried to the MC.

PMU_HN_MC_REQS_EVENT

Total number of requests that are sent to the MC.

Calculate the retry rate for requests to the MC as follows:

Figure 8-5: MC message retry rate

$$\text{MC message retry rate (\%)} = \frac{\text{MC total messages retried}}{\text{MC total messages received}} \times 100$$

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8.3.5 Quality of Service

Requests with a HighHigh QoS must be allocated and processed from the POCQ with the highest priority compared to High, Medium, and Low QoS requests.

If the HighHigh requests are retried too frequently, there could be a bottleneck at a particular HN-F, or the POCQ reservation for HighHigh requests requires adjustment.

PMU_HN_QOS_HH_RETRY

How often a HighHigh request is retried.

8.3.6 HN-F MPAM Hard Limit and Soft Limit events

HN-F also implements performance monitoring events for the MPAM Hard Limit and Soft Limit functionality.

HN-F has two performance monitoring events that are related to MPAM Hard Limit and Soft Limit functionality:

PMU_HN_MPAM_REQ_OVER_HARDLIM_EVENT

Number of times a request cannot allocate in SLC as MPAM Hard Limit has been reached.

PMU_HN_MPAM_REQ_OVER_SOFTLIM_EVENT

Number of times a request is above the MPAM Soft Limit. This situation indicates that MPAM PARTID might be close to the Hard Limit.

Both events can be counted in total or filtered according to PARTID. The behavior is programmed through the following registers:

- 5.3.4.162 por_hnf_pmu_mpam_sel on page 673
- 5.3.4.163 por_hnf_pmu_mpam_pardid_mask0 on page 675-5.3.4.170 por_hnf_pmu_mpam_pardid_mask7 on page 683

8.3.7 HN-F PMU event summary

The following table shows a summary of the HN-F PMU events.

Table 8-1: HN-F events

Number	Name	Description
1	PMU_HN_CACHE_MISS_EVENT	Counts total cache misses in first lookup result (high priority).
2	PMU_HNSLC_SF_CACHE_ACCESS_EVENT	Counts number of cache accesses in first access (high priority).
3	PMU_HN_CACHE_FILL_EVENT	Counts total allocations in HN SLC (all cache line allocations to SLC).
4	PMU_HN_POCQ_RETRY_EVENT	Counts number of retried requests.
5	PMU_HN_POCQ_REQS_RECVD_EVENT	Counts number of requests that HN receives.
6	PMU_HN_SF_HIT_EVENT	Counts number of SF hits.
7	PMU_HN_SF_EVICTIONS_EVENT	Counts number of SF eviction cache invalidations initiated.
8	PMU_HN_DIR_SNOOPS_SENT_EVENT	Counts number of directed snoops sent (not including SF back invalidation).

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Number	Name	Description
9	PMU_HN_BRD_SNOOPS_SENTEVENT	Counts number of multicast snoops sent (not including SF back invalidation).
10	PMU_HN_SLC_EVICTION_EVENT	Counts number of SLC evictions (dirty only).
11	PMU_HN_SLC_FILL_INVALID_WAY_EVENT	Counts number of SLC fills to an invalid way.
12	PMU_HN_MC_RETRIES_EVENT	Counts number of retried transactions by the MC.
13	PMU_HN_MC_REQS_EVENT	Counts number of requests that are sent to MC.
14	PMU_HN_QOS_HH_RETRY_EVENT	Counts number of times a HighHigh priority request is protocol-retried at the HN-F.
15	PMU_HNF_POCQ_OCCUPANCY_EVENT	Counts the POCQ occupancy in HN-F. Occupancy filtering is programmed in pmu_occup1_id.
16	PMU_HN_POCQ_ADDRHAZ_EVENT	Counts number of POCQ address hazards on allocation.
17	PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT	Counts number of POCQ address hazards on allocation for atomic operations.
18	PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT	Counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations.
19	PMU_HN_CMP_ADQ_FULL_EVENT	Counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations.
20	PMU_HN_TXDAT_STALL_EVENT	Counts number of times HN-F has a pending **TXDAT** flit but no credits to upload.
21	PMU_HN_TXRSP_STALL_EVENT	Counts number of times HN-F has a pending **TXRSP** flit but no credits to upload.
22	PMU_HN_SEQ_FULL_EVENT	Counts number of times requests are replayed in SLC pipe due to SEQ being full.
23	PMU_HN_SEQ_HIT_EVENT	Counts number of times a request in SLC hit a pending SF eviction in SEQ.
24	PMU_HN_SNP_SENT_EVENT	Counts number of snoops sent including directed, multicast, and SF back invalidation.
25	PMU_HN_SFBI_DIR_SNP_SENT_EVENT	Counts number of times directed snoops were sent due to SF back invalidation.
26	PMU_HN_SFBI_BRD_SNP_SENT_EVENT	Counts number of times multicast snoops were sent due to SF back invalidation.
27	PMU_HN_SNP_SENT_UNTRK_EVENT	Counts number of times snoops were sent due to untracked RN-Fs.
28	PMU_HN_INTV_DIRTY_EVENT	Counts number of times SF back invalidation resulted in dirty line intervention from the RN.
29	PMU_HN_STASH_SNP_SENT_EVENT	Counts number of times stash snoops were sent.
30	PMU_HN_STASH_DATA_PULL_EVENT	Counts number of times stash snoops resulted in data pull from the RN.
31	PMU_HN_SNP_FWDED_EVENT	Counts number of times data forward snoops were sent.

8.4 RN-I performance events

External devices connect at an RN-I bridge.

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8.4.1 Bandwidth at RN-I bridges

External devices connect at an RN-I bridge.

The following events measure bandwidth at the RN-I bridges:

- 8.4.1.1 Requested read bandwidth at RN-I bridges on page 1352.
- 8.4.1.2 Actual read bandwidth on interconnect on page 1352.
- 8.4.1.3 Write bandwidth at RN-I bridges on page 1353.

8.4.1.1 Requested read bandwidth at RN-I bridges

External devices connect to CI-700 at an RN-I bridge.

To monitor the behavior of the system, the following events measure the read bandwidth at each RN-I bridge:

RDataBeats_Port0
: Number of RData beats (**RVALID** and **RREADY**) dispatched on port 0.

RDataBeats_Port1
: Number of RData beats (**RVALID** and **RREADY**) dispatched on port 1.

RDataBeats_Port2
: Number of RData beats (**RVALID** and **RREADY**) dispatched on port 2.

Because CMOs are sent through the read channel, their responses are included in these events.

Calculate the read bandwidth as follows:

Figure 8-6: Read bandwidth calculation

$$\text{Read bandwidth} = \frac{\text{Number RDataBeats_Port}n \times \text{AXIDataBeatSize}}{\text{Cycles}} \times \text{Frequency}$$

Where AXIDataBeatSize is the number of bytes for each AXI beat. Usually, this number is the same size as the AXI bus.


Note

If the data chunking feature is enabled, Read data bandwidth is calculated by counting the number of chunks being transferred on RData. This count is done by looking at **RCHUNKSTRB[n-1:0]** signal, where every bit of **RCHUNKSTRB** represents 16B of data.

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8.4.1.2 Actual read bandwidth on interconnect

RXDATFLITV measures the bandwidth that an RN-I bridge sends to the interconnect.

This event counts the number of received data flit requests that the bridge receives through the data channel. Therefore, this event measure the actual bandwidth that an RN-I bridge sends to the interconnect, and not the useful bandwidth the external devices can use.

RXDATFLITV

Number of **RXDAT** flits received. This event is a measure of the true read data bandwidth. It excludes CMOs, because CMO completions return to the RN-I through the response channel, but includes replayed requests.

This event includes the replayed requests because of the read data buffer decoupled scheme.

Calculate the actual read bandwidth as follows:

Figure 8-7: Actual read bandwidth

$$\text{Actual read bandwidth} = \frac{\text{RXDATFLITV x DataFlitSize}}{\text{Cycles}} \text{x Frequency}$$

8.4.1.3 Write bandwidth at RN-I bridges

TXDATFLITV monitors the number of data flits that the RN-I bridge sends out.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the RN-I bridge sends out. Therefore, this event measures the actual write bandwidth that is sent to the interconnect:

TXDATFLITV

Number of **TXDAT** flits dispatched. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

Figure 8-8: Actual write bandwidth

$$\text{Actual write bandwidth} = \frac{\text{TXDATFLITV x DataFlitSize}}{\text{Cycles}} \text{x Frequency}$$

8.4.2 Bottleneck analysis at RN-I bridges

CI-700 provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system.

This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in the RN-Is, HN-Fs, and memory controllers. In the RN-I bridges, the events monitor the following:

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- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times the read and write tracker is full and therefore cannot accept new requests in the system. This condition can cause delays in the AXI masters.
- The number of read request replays, because of decoupling of the read request buffers and read data buffers in the RN-I system.

8.4.2.1 Request retry rate at RN-I bridges

TXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system.

It does this task by measuring the request retry rate:

TXREQFLITV_RETRIED

Number of retried **TXREQ** flits dispatched. This event is a measure of the retry rate.

Calculate the request retry rate as follows:

Figure 8-9: Retry rate

$$\text{Retry rate} = \frac{\text{TXREQFLITV_RETRIED}}{\text{TXREQFLITV_TOTAL}}$$

8.4.2.2 Read and write delays at RN-I bridges

To monitor the delays for reads and writes, CI-700 lets you monitor how full the read and write trackers are in the RN-I bridges.

When one of the trackers is full, the bridge cannot accept new requests from the AXI master. This condition delays the I/O devices that connect to the AXI master.

There are two measures that, together, can help you to isolate the source of bottlenecks in the system. These measures are: how full the trackers are, and the read and write bandwidth from the RN-I bridge to the interconnect. For example, consider the following situations:

- The read tracker of a specific RN-I bridge is full but the effective read bandwidth from the bridge is not close to the maximum expected. In this case, the interconnect cannot keep up with the read traffic from the specific device.
- The bandwidth is close to maximum, the I/O device can send requests to the maximum of its port bandwidth. In this case, the tracker is full for this reason.

You can also use the measure of how full the trackers are with AXI PMUs to monitor delays to the AXI masters.

The following events monitor the read and write trackers:

RRT_OCCUPANCY

All entries in the read request tracker are occupied. This event is a measure of oversubscription in the read request tracker.

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WRT_OCCUPANCY

All entries in the write request tracker are occupied. This event is a measure of oversubscription in the write request tracker.


Note

For CI-700, when the `NUM_RD_REQ` parameter for an RN-I or RN-D node is configured to 128 or 256, the read tracker is divided into slices of 64 entries each. An ACE-Lite request is allocated into a particular read tracker slice according to:

- A hash of the **ARID** value of the request
- Which of the three ACE-Lite slave interfaces receives the request

Therefore, in these configurations, the maximum number of outstanding same-**ARID** requests from the same ACE-Lite slave interface is 64.

The `RRT_OCCUPANCY` event covers the total occupancy of all read tracker slices.

8.4.3 RN-I PMU event summary

There are 16 RN-I PMU events.

The following table shows a summary of the RN-I PMU events.

Table 8-2: RN-I PMU event summary

Number	Name	Description
1	PMU_RNI_RDATABEATS_P0	Number of RData beats (**RVALID** and **RREADY**) dispatched on port 0. This event measures the read bandwidth, including CMO responses.
2	PMU_RNI_RDATABEATS_P1	Number of RData beats (**RVALID** and **RREADY**) dispatched on port 1. This event measures the read bandwidth, including CMO responses.
3	PMU_RNI_RDATABEATS_P2	Number of RData beats (**RVALID** and **RREADY**) dispatched on port 2. This event measures the read bandwidth, including CMO responses.
4	PMU_RNI_RXDATFLITV	Number of **RXDAT** flits received. This event measures the true read data bandwidth, excluding CMOs.
5	PMU_RNI_TXDATFLITV	Number of **TXDAT** flits dispatched. This event measures the write bandwidth.
6	PMU_RNI_TXREQFLITV	Number of **TXREQ** flits dispatched. This event measures the total request bandwidth.
7	PMU_RNI_TXREQFLITV_RETRIED	Number of retried **TXREQ** flits dispatched. This event measures the retry rate.
8	PMU_RNI_RRT_OCCUPANCY	All entries in the read request tracker are occupied. This event measures oversubscription in the read request tracker.
9	PMU_RNI_WRT_OCCUPANCY	All entries in the write request tracker are occupied. This event measures oversubscription in the write request tracker.
10	PMU_RNI_TXREQFLITV_REPLAYED	Number of replayed **TXREQ** flits. This event measures the replay rate.
11	PMU_RNI_WRCANCEL_SENT	Number of write data cancels sent. This event measures the write cancel rate.
12	PMU_RNI_WDATABEAT_P0	Number of WData beats (**WVALID** and **WREADY**) dispatched on port 0. This event measures write bandwidth on AXI port 0.
13	PMU_RNI_WDATABEAT_P1	Number of WData beats (**WVALID** and **WREADY**) dispatched on port 1. This event measures the write bandwidth on AXI port 1.

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Number	Name	Description
14	PMU_RNI_WDATABEAT_P2	Number of WData beats (**WVALID** and **WREADY**) dispatched on port 2. This event measures the write bandwidth on AXI port 2.
15	PMU_RNI_RRTALLOC	Number of allocations in the read request tracker. This event measures the read transaction count.
16	PMU_RNI_WRTALLOC	Number of allocations in the write request tracker. This event measures the write transaction count.

8.5 SBSX performance events

This section contains SBSX performance event information.

8.5.1 Bandwidth at SBSX bridges

This section contains SBSX bridge bandwidth information.

The following events are used to measure bandwidth at the SBSX bridges:

- 8.5.1.1 Read bandwidth on interconnect at SBSX bridges on page 1356.
- 8.5.1.2 Write bandwidth at SBSX bridges on page 1357.
- 8.5.1.3 Total requested bandwidth at SBSX bridges on page 1357.

8.5.1.1 Read bandwidth on interconnect at SBSX bridges

This section contains information on read bandwidth on interconnect at SBSX bridges.

This event counts the number of received data flits at the SBSX and interconnect:

PMU_SBSX_RXDAT

Number of **RXDAT** flits received at XP from SBSX. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

Figure 8-10: Actual read bandwidth

$$\text{Actual read bandwidth} = \frac{\text{PMU_SBSX_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

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Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.5.1.2 Write bandwidth at SBSX bridges

This section contains information on write bandwidth at SBSX bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the SBSX receives. Therefore, this event measures the actual write bandwidth that is received from the interconnect:

PMU_SBSX_TXDAT

Number of **TXDAT** flits dispatched from XP to SBSX. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

Figure 8-11: Actual write bandwidth

$$\text{Actual write bandwidth} = \frac{\text{PMU_SBSX_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.5.1.3 Total requested bandwidth at SBSX bridges

This section contains information on total requested bandwidth at SBSX bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event. The PMU_SBSX_TXREQ_TOTAL event monitors the number of REQ flits that an SBSX bridge receives:

PMU_SBSX_TXREQ_TOTAL

Number of **TXREQ** flits dispatched from XP to SBSX. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

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Figure 8-12: Total requested bandwidth

$$\text{Total requested bandwidth} = \frac{\text{PMU_SBSX_TXREQ_TOTAL x DataFlitSize}}{\text{Cycles}} \text{ x Frequency}$$

Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.5.2 Bottleneck analysis at SBSX bridges

This section contains information on bottleneck analysis at SBSX bridges.

CI-700 provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system. This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in all CI-700 components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of cycles the bridge is forced to stall due to backpressures on AXI or CHI interface.

The following events are used to measure bottlenecks at the SBSX bridges:

- 8.5 SBSX performance events on page 1356.

8.5.2.1 Request retry rate at SBSX bridges

This section contains information on the request retry rate at SBSX bridges.

RETRYACK_TXRSP monitors the efficiency of using dynamic credits in the system. It does this task by measuring the request retry rate:

RETRYACK_TXRSP

Number of **RXREQ** flits dispatched. This event is a measure of the retry rate. Calculate the retry rate as follows:

Retry rate = RETRYACK_TXRSP / RXREQFLITV_TOTAL

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8.5.2.2 Delays at SBSX bridges due to backpressure

To analyze the delays in SBSX bridges, CI-700 enables you to monitor the source of backpressure.

SBSX might have requests that are ready to be sent to the downstream AXI or ACE-Lite device. However, it cannot send them due to backpressure from the downstream device. In this situation, SBSX holds the request in the *Receive Request Tracker* (RRT). This condition results in the RRT getting full and so the SBSX bridge cannot accept any new requests from RNs impacting system performance.

The following table contains events that monitor such backpressure from the downstream AXI or ACE-Lite device:

Table 8-3: AXI or ACE-Lite downstream monitoring events

Events	Description
ARVALID_NO_ARREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AR channel.
AWVALID_NO_AWREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AW channel.
WVALID_NO_WREADY	Number of cycles the SBSX bridge is stalled due to backpressure on W channel.

If a mesh is congested with many DAT or RSP flits, it might not give link credits to SBSX in timely manner. This situation can cause DAT flits for reads or RSP flits for writes to be stalled in SBSX. The following table describes events monitor in such cases where SBSX bridge is not able to upload DAT/RSP flits on the mesh.

Table 8-4: CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the **TXDAT** flit in SBSX bridge is waiting for link credits.
TXRSPFLITV_NO_LINKCRD	Number of cycles the **TXRSP** flit in SBSX bridge is waiting for link credits.

8.5.2.3 Tracker occupancy analysis

To debug performance issues, more events are provided to measure occupancy of various trackers in SBSX. These trackers include the *Request Received Tracker* (RRT), *Request Dispatch Tracker* (RDT), and *Write Data Buffers* (WDB).

Read, write, and CMO transactions occupy RRT before they are dispatched on the AXI interface. When Read/CMO transactions are dispatched on AXI, they move from RRT to RDT. Writes remain on RRT until the write response is obtained from AXI interface and then deallocated from RRT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker, while RDT is called AXI pending tracker.

The following table contains tracker occupancy information.

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Table 8-5: Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read request tracker occupancy count overflow
RRT_WR_OCCUPANCY_CNT_OVFL	Write request tracker occupancy count overflow
RRT_CMO_OCCUPANCY_CNT_OVFL	CMO request tracker occupancy count overflow
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow
RDT_RD_OCCUPANCY_CNT_OVFL	Read AXI pending tracker occupancy count overflow
RDT_CMO_OCCUPANCY_CNT_OVFL	CMO AXI pending tracker occupancy count overflow

8.5.3 SBSX PMU event summary

This section contains SBSX PMU event summary information.

For more information, see 5.3.10.18 por_sbsx_pmu_event_sel on page 1135.

8.6 MTSX performance events

The MTSX implements all the SBSX performance monitoring events and also MTU-specific performance monitoring events.

Up to four MTSX events can be selected using configuration registers. Given that SBSX and MTU events are combined as MTSX events, each event must be selected in either SBSX or MTU only. If the same event is selected in both SBSX and MTU, the one selected in the SBSX is counted.

For more information about the performance monitoring in the SBSX, see 8.5 SBSX performance events on page 1356.

8.6.1 MTSX TC performance

You can use certain MTSX PMU events to characterize the behavior of the TC and make measurements related to the performance of the TC.

The following events can be used to characterize MTSX TC behavior:

- PMU_TC_LOOKUP_EVENT
- PMU_TC_FILL_EVENT
- PMU_TC_MISS_EVENT

You can calculate the TC miss rate according to the following equation:

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Figure 8-13: TC miss rate

$$\text{TC miss rate (\%)} = \frac{\text{PMU_TC_MISS_EVENT}}{\text{PMU_TC_LOOKUP_EVENT}} \times 100$$

Certain tag requests require multiple accesses to the TC. PMU_TC_LOOKUP_EVENT counts first-time accesses, in other words TC lookup, only.

You can use PMU_TC_FILL_EVENT as an approximation of the TC usage. All TC allocations count toward this event. This event does not count updates to a line already installed in the TC.

8.6.2 MTSX bandwidth

You can use a combination of MTSX PMU events to calculate the MTSX bandwidth.

The following events can be used for MTSX bandwidth information:

- PMU_AXI_RD_REQ_EVENT
- PMU_AXI_WR_REQ_EVENT

You can calculate the actual read bandwidth seen at the MTSX from AXI using the following equation:

Figure 8-14: MTSX actual read bandwidth

$$\text{Actual read bandwidth} = \frac{\text{PMU_AXI_RD_REQ_EVENT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{frequency}$$

You can calculate the actual write bandwidth seen at the MTSX from AXI using the following equation:

Figure 8-15: MTSX actual write bandwidth

$$\text{Actual write bandwidth} = \frac{\text{PMU_AXI_WR_REQ_EVENT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{frequency}$$

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8.6.3 MTSX PMU event summary

The MTSX implements several performance monitoring events to allow you to monitor the performance of the unit.

Both SBSX and MTU-specific PMU events are implemented in MTSX. See 5.3.10.18 por_sbsx_pmu_event_sel on page 1135 for the SBSX PMU events. The following table shows the MTU-specific MTSX PMU events and their encodings.

Table 8-6: MTSX PMU event summary

Number	Name	Description
1	PMU_TC_LOOKUP_EVENT	TC lookup requests. This event measures TC accesses.
2	PMU_TC_FILL_EVENT	TC allocation (Dirty or Clean) requests. This event measures TC allocations.
3	PMU_TC_MISS_EVENT	TC misses. This event measures TC miss rate.
4	PMU_TDB_FORWARD_EVENT	Requests that received data from TDB forwarding.
5	PMU_TCQ_HAZARD_EVENT	TCQ address hazards on allocation
6	PMU_TCQ_RD_ALLOC_EVENT	Read requests allocated in TCQ, including read tag ops and write match tag ops.
7	PMU_TCQ_WR_ALLOC_EVENT	Write requests allocated in TCQ. This event counts write update tag ops.
8	PMU_TCQ_CMO_ALLOC_EVENT	CMO requests allocated in TCQ. This event counts CMOs and writes+CMOs.
9	PMU_AXI_RD_REQ_EVENT	Read requests sent out on AXI. This event measures MTSX AXI read bandwidth.
10	PMU_AXI_WR_REQ_EVENT	Write requests sent out on AXI. This event measures MTSX AXI write bandwidth.
11	PMU_TCQ_OCC_CNT_OVFL_EVENT	TCQ tracker occupancy count overflow. This event measures oversubscription of the TCQ tracker.
12	PMU_TDB_OCC_CNT_OVFL_EVENT	TDB occupancy count overflow. This event measures oversubscription of the TDB.

8.7 HN-I performance events

This section contains HN-I performance event information.

8.7.1 Bandwidth at HN-I bridges

This section contains HN-I bridge bandwidth information.

The following events are used to measure bandwidth at the HN-I bridges:

- 8.7.1.1 Read bandwidth on interconnect at HN-I bridges on page 1362.
- 8.7.1.2 Write bandwidth at HN-I bridges on page 1363.
- 8.7.1.3 Total requested bandwidth at HN-I bridges on page 1364.

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8.7.1.1 Read bandwidth on interconnect at HN-I bridges

This section contains information on read bandwidth on interconnect at HN-I bridges.

This event counts the number of received data flits at the HN-I and interconnect:

PMU_HNI_RXDAT
Number of **RXDAT** flits received at XP from HN-I. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

Figure 8-16: Actual read bandwidth

$$\text{Actual read bandwidth} = \frac{\text{PMU_HNI_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$


Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.7.1.2 Write bandwidth at HN-I bridges

This section contains information on write bandwidth at HN-I bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the HN-I receives. Therefore this event measures the actual write bandwidth that is received from the interconnect:

PMU_HNI_TXDAT
Number of **TXDAT** flits dispatched from XP to HN-I. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

Figure 8-17: Actual write bandwidth

$$\text{Actual write bandwidth} = \frac{\text{PMU_HNI_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

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Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.7.1.3 Total requested bandwidth at HN-I bridges

This section contains information on total requested bandwidth at HN-I bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event. The PMU_HNI_TXREQ_TOTAL event monitors the number of REQ flits that an HN-I bridge receives:

PMU_HNI_TXREQ_TOTAL

Number of **TXREQ** flits dispatched from XP to HN-I. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

Figure 8-18: Total requested bandwidth

$$\text{Total requested bandwidth} = \frac{\text{PMU_HNI_TXREQ} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DTM watchpoint in the XP where the component is located.

8.7.2 Bottleneck analysis at HN-I bridges

This section contains information on bottleneck analysis at HN-I bridges.

Locations where the nodes or bridges are full can cause delays in the rest of the system. CI-700 provides events that observe locations where the nodes or bridges are full. This feature enables you to monitor the current bottlenecks in the system, and checks multiple events in all CI-700 components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times requests are serialized due to ordering requirements.
- The number of cycles the bridge is forced to stall due to backpressures.

The following events are used to measure bottlenecks at the HN-I bridges:

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- 8.7 HN-I performance events on page 1362.

8.7.2.1 Request retry rate at HN-I bridges

This section contains information on the request retry rate at HN-I bridges.

RETRYACK_TXRSP monitors the efficiency of using dynamic credits in the system. It does this task by measuring the request retry rate:

RETRYACK_TXRSP

Number of **RXREQ** flits dispatched. This event is a measure of the retry rate. Calculate the retry rate as follows:

Retry rate = RETRYACK_TXRSP / RXREQFLITV_TOTAL

8.7.2.2 Delays at HN-I bridges because of ordering requirements

When requests are received at an HN-I, there are different ordering guarantees the HN-I bridge must maintain based on the source and attributes of the request.

The requests are sometimes serialized, indicating a lower than expected bandwidth at HN-I, as the following table shows.

Table 8-7: PCIe and non-PCIe RN request information

Request	Description
NONPCIE_SERIALIZED	Number of non-PCIe RN requests that are serialized.
PCIE_SERIALIZED	Number of PCIe RN requests that are serialized.

8.7.2.3 Delays at HN-I bridges because of backpressure

To analyze the delays in HN-I bridges, CI-700 enables you to monitor the source of backpressure.

HN-I might have requests that are ready to be sent to AXI or ACE-Lite downstream. However, it cannot send them due to backpressure from AXI or ACE-Lite downstream. In this situation, HN-I holds the request in the RRT. As a result, the RRT gets full. Therefore, the HN-I bridge cannot accept any new requests from RNs, impacting system performance.

This table describes the events that monitor such backpressure from AXI or ACE-Lite downstream:

Table 8-8: AXI and ACE-Lite downstream events monitor information

Events	Description
ARVALID_NO_ARREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AR channel.
AWVALID_NO_AWREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AW channel.
WVALID_NO_WREADY	Number of cycles the HN-I bridge is stalled due to backpressure on W channel.

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Even if the AXI or ACE-Lite downstream is ready to accept new requests, the HN-I bridge cannot send them downstream while the RDT is full. The lifetime of a request in the RDT depends on response latency from AXI or ACE-Lite downstream and backpressure on **TXDAT** channel.

This table describes the events that monitor cases where an HN-I bridge is unable to send new requests to AXI or ACE-Lite downstream:

Table 8-9: AXI and ACE-Lite downstream events monitor information (no new requests sent)

Events	Description
ARREADY_NO_ARVALID	Number of cycles the AR channel is waiting for new requests from HN-I bridge.
AWREADY_NO_AWVALID	Number of cycles the AW channel is waiting for new requests from HN-I bridge.

If the mesh is congested with many DAT flits, then there might be a delay before it gives link credits to HN-I. This delay results in the stalling of DAT flits for reads in HN-I. This table describes events that monitor cases where an HN-I bridge is not able to upload a DAT flit on the mesh.

Table 8-10: CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the **TXDAT** flit in HN-I bridge is waiting for link credits.

8.7.2.4 Tracker occupancy analysis in HN-I

To debug performance issues, more events are provided to measure occupancy of various trackers in HN-I such as RRT, RDT, and WDB.

Read and write transactions occupy RRT before they are dispatched on the AXI interface. When read and write transactions are dispatched on AXI, they move from RRT to RDT. Reads and writes remain on RDT until all the responses are obtained from the AXI interface. The transactions are then deallocated from RDT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker while RDT is called AXI pending tracker.

The following table contains tracker occupancy information:

Table 8-11: Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RRT
RRT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RRT
RDT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RDT
RDT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RDT
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow event

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8.7.3 HN-I PMU event summary

This section contains HN-I PMU event summary information.

Refer to 5.3.5.21 por_hni_pmu_event_sel on page 716 for more information.

8.8 DN performance events

This section contains DN performance event information.

The following table shows a summary of the DN PMU events.

Table 8-12: DN PMU event summary

Number	Description
1	Number of TLBI DVM op requests
2	Number of BPI DVM op requests
3	Number of PICI DVM op requests
4	Number of VICI DVM op requests
5	Number of DVM sync requests
6	Number of DVM op requests that were filtered using VMID filtering
7	Number of DVM op requests to RN-Ds, BPI, or PICI/VICI, that are filtered.
8	Number of retried REQs
9	Number of SNPs sent to RNs
10	Number of SNPs stalled to RNs due to lack of credits
11	DVM tracker full counter
12	DVM tracker occupancy counter

The pmu_occup1_id field in the por_dn_pmu_event_sel register is used to program the occupancy counter for specific operations types. The following table summarizes the options.

Table 8-13: Field values for pmu_occup1_id

pmu_occup1_id values	Description
0b0000	All
0b0001	DVM ops
0b0010	DVM syncs


Note

In HN-D, DN PMU events can be accessed only when the corresponding HN-I PMU select is 0 (NONE).

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DN events can be accessed through the HN-D. The por_dn_pmu_event_sel register outputs on corresponding TXPMU output only if por_hni_pmu_event_sel bit[5], bit[13], bit[21], and bit[29] are set to 0. Otherwise the value on the HN-I PMU is available.

8.9 XP PMU event summary

This section contains XP PMU event summary information.

Each of the XP PMU events is associated with:

- One of six XP ports:
  - If using a mesh configuration, these ports can be East, West, North, South, device port P0, P1, P2, or P3, depending on the configuration.
  - If using a single-MXP configuration, these ports are device ports P0, P1, P2, P3, P4, and P5.
- One of four CHI channels - REQ, RSP, SNP, or DAT.

Up to four XP PMU Events can be specified using the por_mxp_pmu_event_sel register. For more information about this register, see 5.3.6.22 por_mxp_pmu_event_sel on page 750.

The following table shows a summary of the XP PMU events.

Table 8-14: XP PMU event summary

Number	Name	Description
1	PMU_XP_TXFLIT_VALID	Number of flits that are transmitted on a specified port and CHI channel. This event measures the flit transfer bandwidth from an XP. **Note:** On device ports, this event also includes link flit transfers.
2	PMU_XP_TXFLIT_STALL	Number of cycles when a flit is stalled at an XP waiting for link credits at a specified port and CHI channel. This event measures the flit traffic congestion on the mesh and at the flit download ports.

8.10 Occupancy and lifetime measurement using PMU events

CI-700 has PMU events to measure the average occupancy of a tracker and measure the average lifetime of the requests in that tracker.

This event is implemented for many of the trackers in CI-700 units (HN-F, RN-I, RN-D, HN-I, and others). The following formula measures the average occupancy and lifetime and can be applied to all the trackers where this event is supported:

Occupancy measurement

The formula to measure the occupancy is:

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Figure 8-19: Average occupancy

$$\text{Average Occupancy (entries)} = \frac{\text{PMU_OCCUPANCY_EVENT} << 12}{\text{PMU_CYCLE_COUNTER}}$$

For example, for RN-I RRT average occupancy, the formula is:

Figure 8-20: Average RRT occupancy

$$\text{Average RRT Occupancy (entries)} = \frac{\text{PMU_RNI_RRT_OCCUPANCY_EVENT} << 12}{\text{PMU_CYCLE_COUNTER}}$$

Lifetime measurement

If a tracker supports lifetime event, the formula to measure the lifetime is:

Figure 8-21: Average lifetime

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU_OCCUPANCY_EVENT} << 12}{\text{PMU_NUM_TRACKER_ALLOCATIONS}}$$

For example, for RN-I RRT average lifetime, the formula is:

Figure 8-22: Average RRT lifetime

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU_RNI_RRT_OCCUPANCY} << 12}{\text{PMU_RNI_RRTALLOC}}$$

HN-F supports collecting occupancy according to the request types. The following table describes the opcode filtering types that are supported.

Table 8-15: Supported opcode filtering types

pmu_occup1_id	Opcode type
0b000	All request types
0b001	Read request types
0b010	Write request types
0b011	Atomic request types
0b100	Stash request types

When you enable filtering, pmu_occup1_id must return to the default value to collect occupancy for all request types.

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8.11 DEVEVENT

CI-700 HN-Fs support device-specific events that are collectively called DEVEVENT. These events are sent along with the completion of a transaction.

The completion of a transaction can be a data response (DAT) or completion response (RSP). These events contain information regarding the transaction encountering an SLC hit or miss. The events also include information about snoops sent to resolve coherency actions. You can measure these events using watchpoints on the XP that the RN-F is connected to. Refer to 7.1.2 DTM watchpoint on page 1323 for watchpoint usage.

The following table describes the DEVEVENT encodings from HN-F.

Table 8-16: DEVEVENT encodings from HN-F

Encoding	Description
`2'b00`	Line missed in SLC and no snoops sent
`2'b01`	Line missed in SLC and directed snoop sent
`2'b10`	Line missed in SLC and broadcast snoops sent
`2'b11`	Line hit in SLC and no snoops sent

Other CI-700 device responses have the default `2'b00` encoding as the DEVEVENT value.

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Appendix A Protocol feature compliance

This appendix describes the features that CI-700 implements from different protocol and architecture specifications.

A.1 AXI and ACE-Lite feature support

AXI and ACE-Lite provides optional features through interface properties. CI-700 supports some of these properties and whether a property is supported depends on the node type.

The following table shows the AXI and ACE-Lite properties that the different CI-700 nodes with AXI or ACE-Lite interfaces support.

Table A-1: AXI and ACE-Lite feature support

AXI or ACE-Lite property	Support		
	RN-I	HN-I	SBSX
Wakeup_Signals	Y	Y	Y
Check_Type	N	Y	Y
Poison	Y	Y	Y
Trace_Signals	Y	Y	Y
Unique_ID_Support	Y	Y	Y
QoS_Accept	N	N	N
Loopback_Signals	Y	N	N
Untranslated_Transactions	N	N	N
NSAccess_Identifiers	Y	N	Y
CMO_On_Read	Y	N	Y
CMO_On_Write	Y	N	Y
Persist_CMO	Y	N	Y
Write_Plus_CMO	N	N	Y
DVM_v8 and DVM_v8.1	N	N	N
DVM_v8.4	Y	N	N
Coherency_Connection_Signals	Y	N	N
MPAM_Support	Y	Y	Y
Read_Interleaving_Disabled	N	Y	Y
Read_Data_Chunking	Y	N	N
Cache_Stash_Transactions	Y	N	N
Atomic_Transactions	Y	N	N
DeAllocation_Transactions	Y	N	N
MTE_Support	Y (Basic)	N	Y
WriteEvict_Transaction	N	N	N

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AXI or ACE-Lite property	Support		
	RN-I	HN-I	SBSX
Barrier_Transactions	N	N	N
Ordered_Write_Observation	Y	Y	N
DVM_On_Read	N	N	N
DVM_On_Snoop	Y (RN-D)	N	N
Max_Transaction_Size	Any	64B	64B
Fixed_Burst	Y	N	N
Exclusive_Access	Y	N	N (non-DSA) Y (DSA)
Shareable_Transactions	Y	N	N
Prefetch_Transaction	N	N	Y

A.2 CHI feature support

CHI provides various optional features through interface properties. CI-700 supports some of these properties.

The following table shows the CHI properties that CI-700 supports.

Table A-2: CHI feature support

CHI property	Support	Comments
Atomic_Transactions	Y	-
Cache_Stash_Transactions	Y	-
Direct_Memory_Transfer	Y	-
Direct_Cache_Transfer	Y	-
Data_Poison	Y	-
Data_Check	Y	-
CCF_Wrap_Order	N	True for most of the nodes, but not all.
Req_Addr_Width	Y	-
NodeID_Width	Y	Supported values are 7-11.
Data_Width	N	Fixed to 256
Enhanced_Features	Y	Support enabled for all enhanced features.
CleanSharedPersistSep_Request	Y	-
MPAM_Support	Y	-
DVM_Support	Y	-

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Appendix B Signal descriptions

This appendix describes the external I/O signals that CI-700 implements for connection to other hardware in the system.

B.1 About the signal descriptions

CI-700 signals are composed of a base name along with identifiers that indicate unique product configurations.

Because there are multiple identical interfaces in CI-700, the signal names that this appendix describes are often only root names. The actual signal name includes a port-specific identifier suffix.

The system configuration determines which of the signals are used in a particular system.



Unless specified otherwise, CI-700 signals are active-HIGH.

B.2 Clock and reset signals

The following table shows the CI-700 clock and reset signals.

Table B-1: CI-700 clock and reset signals

Signal	Type	Description	Connection information
GCLK0	Input	Primary CI-700 clock input	Connect to global clock for CI-700.
nSRESET	Input	CI-700 reset, active-LOW	Connect to global reset for CI-700.

B.3 CHI interface signals

CI-700 uses channels that form an inbound and outbound CHI interface for each device using signals that form each channel in a specific interface.

The *AMBA® 5 CHI Architecture Specification* defines four channels:

- *Request* (REQ)
- *Response* (RSP)
- *Snoop* (SNP)

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- *Data* (DAT)

Note

All signal names in this section are only a root name, **RootName**. CI-700 interfaces use **RootName** within a more fully specified signal name as follows:

- CI-700 interface signal name == **RootName_NID#**, where # is the node ID corresponding to the specific interface.

B.3.1 Per-device interface definition

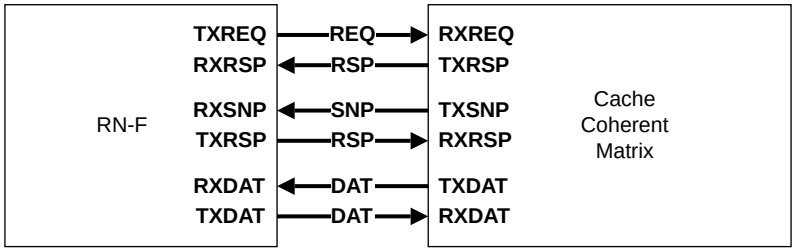
Each CHI device included in a CI-700 system has distinct functionality, and the requirements and configuration of its respective CHI interfaces differ.

The requirements and configuration for the CHI interfaces are as follows:

External RN-F interface

The RN-F interface consists of a request channel, snoop channel, and two response channels, one in each direction, as the following figure shows.

Figure B-1: External RN-F interface



It also has two data channels, one in each direction, for data transfers. CI-700 receives request messages from the RN-F and sends responses to it. CI-700 also sends snoop messages to the RN-F and receives snoop response messages.

External SN-F interface

The SN-F interface consists of a request channel and a response channel as the following figure shows.

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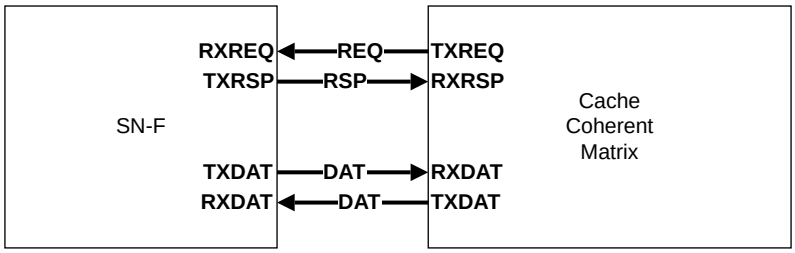
Figure B-2: External SN-F interface



It also has two data channels, one in each direction, for data transfers. The SN-F receives request messages from CI-700 and returns response messages.

B.3.2 Per-channel interface signals

For communication between devices, each channel includes a *Transmit* (TX) and a *Receive* (RX) port, with various interface signals traveling from TX to RX.

Note

Connection of CHI interfaces between two devices requires cross-coupling of the **TX*** and **RX*** signals between the two devices, as required by the CHI architecture.

Signal definitions

Table B-2: Per-channel interface signals

Signal	Direction	Description	Connection information
TXREQFLITPEND	Output	Transmit Request Early Flit Valid hint	Connect to **RXREQFLITPEND** of the corresponding CHI device, if populated.
TXREQFLITV	Output	Transmit Request Flit Valid	Connect to **RXREQFLITV** of the corresponding CHI device, if populated.
TXREQFLIT[n:0][1]	Output	Transmit Request Flit	Connect to **RXREQFLIT** of the corresponding CHI device, if populated.
TXREQLCRDV	Input	Transmit Request channel link layer credit	Connect to **RXREQLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.
TXRSPFLITPEND	Output	Transmit Response Early Flit Valid hint	Connect to **RXRSPFLITPEND** of the corresponding CHI device, if populated.
TXRSPFLITV	Output	Transmit Response Flit Valid	Connect to **RXRSPFLITV** of the corresponding CHI device, if populated.
TXRSPFLIT[n:0][1]	Output	Transmit Response Flit	Connect to **RXRSPFLIT** of the corresponding CHI device, if populated.
TXRSPLCRDV	Input	Transmit Response channel link layer credit	Connect to **RXRSPLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.
TXSNPFLITPEND	Output	Transmit Snoop Early Flit Valid hint	Connect to **RXSNPFLITPEND** of the corresponding CHI device, if populated.
TXSNPFLITV	Output	Transmit Snoop Flit Valid	Connect to **RXSNPFLITV** of the corresponding CHI device, if populated.

[1] The value of `n` is configuration-dependent.

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Signal	Direction	Description	Connection information
TXSNPFLIT[n:0][1]	Output	Transmit Snoop Flit	Connect to **RXSNPFLIT** of the corresponding CHI device, if populated.
TXSNPLCRDV	Input	Transmit Snoop channel link layer credit	Connect to **RXSNPLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.
TXDATFLITPEND	Output	Transmit Data Early Flit Valid hint	Connect to **RXDATFLITPEND** of the corresponding CHI device, if populated.
TXDATFLITV	Output	Transmit Data Flit Valid	Connect to **RXDATFLITV** of the corresponding CHI device, if populated.
TXDATFLIT[n:0][1]	Output	Transmit Data Flit	Connect to **RXDATFLIT** of the corresponding CHI device, if populated.
TXDATLCRDV	Input	Transmit Data channel link layer credit	Connect to **RXDATLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQFLITPEND	Input	Receive Request Early Flit Valid hint	Connect to **TXREQFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQFLITV	Input	Receive Request Flit Valid	Connect to **TXREQFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXREQFLIT[n:0][1]	Input	Receive Request Flit	Connect to **TXREQFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQLCRDV	Output	Receive Request channel link layer credit	Connect to **TXREQLCRDV** of the corresponding CHI device, if populated.
RXRSPFLITPEND	Input	Receive Response Early Flit Valid hint	Connect to **TXRSPFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPFLITV	Input	Receive Response Flit Valid	Connect to **TXRSPFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXRSPFLIT[n:0][1]	Input	Receive Response Flit	Connect to **TXRSPFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPLCRDV	Output	Receive Response channel link layer credit	Connect to **TXRSPLCRDV** of the corresponding CHI device, if populated.
RXSNPFLITPEND	Input	Receive Snoop Early Flit Valid hint	Connect to **TXSNPFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPFLITV	Input	Receive Snoop Flit Valid	Connect to **TXSNPFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXSNPFLIT[n:0][1]	Input	Receive Snoop Flit	Connect to **TXSNPFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPLCRDV	Output	Receive Snoop channel link layer credit	Connect to **TXSNPLCRDV** of the corresponding CHI device, if populated.
RXDATFLITPEND	Input	Receive Data Early Flit Valid hint	Connect to **TXDATFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATFLITV	Input	Receive Data Flit Valid	Connect to **TXDATFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXDATFLIT[n:0][1]	Input	Receive Data Flit	Connect to **TXDATFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATLCRDV	Output	Receive Data channel link layer credit	Connect to **TXDATLCRDV** of the corresponding CHI device, if populated.

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B.3.3 Non-channel-specific interface signals

Every transmit and receive link layer interface includes extra signals that exist only at the interface level and are not channel specific.

Signal definitions

Table B-3: Non-channel-specific interface signals

Signal	Direction	Description	Connection information
RXLINKACTIVEREQ	Input	Receive channel LinkActive request from adjacent transmitter device	Connect to **TXLINKACTIVEREQ** of the corresponding CHI device, if populated, otherwise tie LOW.
RXLINKACTIVEACK	Output	Receive channel LinkActive acknowledgment to adjacent transmitter device	Connect to **TXLINKACTIVEACK** of the corresponding CHI device, if populated.
TXLINKACTIVEREQ	Output	Transmit channel LinkActive request to adjacent receiver device	Connect to **RXLINKACTIVEREQ** of the corresponding CHI device, if populated.
TXLINKACTIVEACK	Input	Transmit channel LinkActive acknowledgment from adjacent receiver device	Connect to **RXLINKACTIVEACK** of the corresponding CHI device, if populated, otherwise tie LOW.
RXSACTIVE	Input	Indication from the adjacent CHI device that it has one or more outstanding protocol-layer transactions. **RXSACTIVE** must remain asserted throughout the lifetime of the transaction.	Connect to **TXSACTIVE** of the corresponding CHI device.
TXSACTIVE	Output	Indication to the adjacent CHI device that CI-700 has one or more outstanding protocol-layer transactions. **TXSACTIVE** remains asserted throughout the lifetime of the transaction.	Connect to **RXSACTIVE** of the corresponding CHI device.
SYSCOREQ	Input	Request to enter CHI coherence domain when asserted and to exit the CHI coherence domain when deasserted. **SYSCOREQ** and **SYSCOACK** implement a four-phase handshake protocol.	Connect to **SYSCOREQ** of corresponding CHI device, if populated, otherwise tie LOW.
SYSCOACK	Output	Acknowledge CHI coherence domain entry/exit request	Connect to **SYSCOACK** of corresponding CHI device, if populated.

B.4 ACE-Lite and AXI interface signals

CI-700 interfaces use **RootName** as the signal name within a more fully specified convention.

All signal names in this section consist of a root name, **RootName**. CI-700 interfaces use **RootName** within a more fully specified signal name as follows:



CI-700 ACE-Lite and AXI interface signal name == **RootName_[S|M]<#a>_NID#b**, where:

S|M Defines either a slave or master interface.

#a Defines an optional interface identifier for a node that can support multiple AMBA interfaces.

#b Defines the node ID corresponding to the specific interface.

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Multi-bit signals append the bit-range identifier included in the **RootName** to the end of the full signal name.

B.4.1 ACE-Lite-with-DVM slave interface signals

This interface is present as the ACE-Lite-with-DVM slave port for an RN-D bridge. The signal descriptions show which signals specific to DVM functionality are not present in an ACE-Lite interface without DVM.

The following table shows the clock and power management signals.

Table B-4: Clock and power management signals

Signal	Type	Description	Connection information
ACLKEN_S	Input	AXI bus clock enable.	Connect to clock enable logic. Tie HIGH if RN-I port is unused.
ACWAKEUP_S	Output	Indication that the interconnect is starting a transaction that is being sent to the DVM master (SMMU).	Connect to corresponding master device, if populated.
AWAKEUP_S	Input	Indication that the master is starting a transaction that is being sent to the interconnect.	Connect to corresponding master device, if populated, otherwise tie LOW.
RNID_SAM_STALL_DIS	Input	Disables RN SAM programming stall for specified RN.	Tie HIGH if boot programming, including RN SAM, is done through this RN-I port. Otherwise, tie LOW.
SYSCOREQ_S	Input	Request to enter DVM domain when asserted and to exit the DVM domain when deasserted. **SYSCOREQ** and **SYSCOACK** implement a four-phase handshake protocol.	Connect to corresponding master device. Tie LOW if the master interface is not populated or if the master interface does not have a **SYSCOREQ_S** output port.
SYSCOACK_S	Output	Acknowledge for DVM domain entry or exit.	Connect to corresponding master device, if populated.

The following table shows the Write Address channel signals.

Table B-5: Write Address channel signals

Signal	Type	Description	Connection information
AWREADY_S	Output	Write address ready.	Connect to corresponding master device, if populated.
AWVALID_S	Input	Write address valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
AWID_S[x:0][2]	Input	Write address ID.	
AWADDR_S[n:0][3]	Input	Write address.	
AWLEN_S[7:0]	Input	Write burst length.	
AWSIZE_S[2:0]	Input	Write burst size.	
AWBURST_S[1:0]	Input	Write burst type.	

[2] The value of `x` = `ID_WIDTH` - 1.
[3] The value of `n` is configuration-dependent.

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Signal	Type	Description	Connection information
AWLOCK_S	Input	Write lock type.	
AWCACHE_S[3:0]	Input	Write memory type.	
AWUSER_S[n:0]	Input. Where n = (REQ_RSVDC_WIDTH-1).	User-defined signal.	
AWPROT_S[2:0]	Input	Write protection type.	
AWQOS_S[3:0]	Input	Write *Quality of Service* (QoS) identifier.	
AWSNOOP_S[3:0]	Input	Write transaction type.	
AWDOMAIN_S[1:0]	Input	Write Shareability domain.	
AWATOP_S[5:0]	Input	Atomic operation.	
AWSTASHNID_S[10:0]	Input	Indicates the node identifier of the physical interface that is the target interface for the cache stash operation.	
AWSTASHNIDEN_S	Input	When asserted, indicates that the **AWSTASHNID** signal is valid and should be used.	
AWSTASHLPID_S[4:0]	Input	Indicates the logical processor subunit that is associated with the physical interface that is the target for the cache stash operation.	
AWSTASHLPIDEN_S	Input	When asserted, indicates that the **AWSTASHLPID** signal is enabled and should be used.	
AWTRACE_S	Input	Trace signal that is associated with the AW Write Address channel.	
AWLOOP_S[1:0]	Input	Loopback signal.	
AWMPAM_S[10:0]	Input	MPAM signal. **AWMPAM[0]** MPAM_NS Security indicator, default = **AWPROT[1].** **AWMPAM[9:1]** PARTID Partition identifier, default = `0x000`. **AWMPAM[10]** PMG Performance monitor group, default = `0b0`.	Connect to corresponding master device, if populated, otherwise tie LOW.
AWIDUNQ_S	Input	Unique ID indicator signal.	
AWNSAID_S[3:0]	Input	Non-secure Access Identifier signal.	
AWCMO_S[1:0]	Input	Type of CMO	
AWTAGOP_S[1:0]	Input	Type of TAGOP	

The following table shows the Write Data channel signals.

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Table B-6: Write Data channel signals

Signal	Type	Description	Connection information
WREADY_S	Output	Write data ready.	Connect to corresponding master device, if populated.
WVALID_S	Input	Write data valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATA_S[n:0][3]	Input	Write data.	
WSTRB_S[d:0] [4]	Input	Write byte lane strobes.	
WLAST_S	Input	Write data last transfer indication.	
WUSER_S[0]	Input	**WDATACHK** valid.	
WTRACE_S	Input	Trace signal.	
WPOISON_S[p:0][5]	Input	Poison signal.	
WDATACHK_S[d:0][4]	Input	Data check signal.	
WTAG_S[m:0][6]		Write tags	
WTAGUPDATE_S[y:0][7]	Input	Tag updates	

The following table shows the Write Response channel signals.

Table B-7: Write Response channel signals

Signal	Type	Description	Connection information
BREADY_S	Input	Write response ready.	Connect to corresponding master device, if populated, otherwise tie LOW.
BVALID_S	Output	Write response valid.	Connect to corresponding master device, if populated.
BID_S[x:0][2]	Output	Write response ID.	
BRESP_S[1:0]	Output	Write response.	
BUSER_S[3:0]	Output	User response signal	
BTRACE_S	Output	Trace signal.	Connect to corresponding master device, if populated.
BLOOP_S[1:0]	Output	Loopback signal.	Connect to corresponding master device, if populated.
BIDUNQ_S	Output	Unique ID indicator signal.	Connect to corresponding master device, if populated.
BCOMP_S	Output	Write/CMO observable	-
BPERSIST_S	Output	Data has been updated in persistent memory.	-

The following table shows the Read Address channel signals.

Table B-8: Read Address channel signals

Signal	Type	Description	Connection information
ARREADY_S	Output	Read address ready.	Connect to corresponding master device, if populated.

[4] The value of `d` = (((n + 1) / 8) - 1).
[5] The value of `p` = ceil(DATA_WIDTH / 64) - 1.
[6] The value of `m` = ((n + 1) / 32) - 1
[7] The value of `y` = ((n + 1) / 128) - 1

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Signal	Type	Description	Connection information
ARVALID_S	Input	Read address valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
ARID_S[x:0][2]	Input	Read address ID.	
ARADDR_S[n:0][3]	Input	Read address.	
ARLEN_S[7:0]	Input	Read burst length.	
ARSIZE_S[2:0]	Input	Read burst size.	
ARBURST_S[1:0]	Input	Read burst type.	
ARLOCK_S	Input	Read lock type.	
ARCACHE_S[3:0]	Input	Read cache type.	
ARUSER_S[n:0]	Input. Where n = (REQ_RSVDC_WIDTH-1).	User-defined signal.	
ARPROT_S[2:0]	Input	Read protection type.	
ARQOS_S[3:0]	Input	Read QoS value.	
ARSNOOP_S[3:0]	Input	Read transaction type.	
ARDOMAIN_S[1:0]	Input	Read Shareability domain.	
ARTRACE_S	Input	Trace signal.	
ARLOOP_S[1:0]	Input	Loopback signal.	
ARMPAM_S[10:0]	Input	MPAM signal. **ARMPAM[0]** MPAM_NS Security indicator, default = **ARPROT[1].** **ARMPAM[9:1]** PARTID Partition identifier, default = `0x000`. **ARMPAM[10]** PMG Performance monitor group, default = `0b0`.	
ARIDUNQ_S	Input	Unique ID indicator signal.	
ARCHUNKEN_S	Input	Chunk enable signal. If asserted, read data for this transaction can be returned out of order, in 128-bit chunks.	
ARNSAID_S[3:0]	Input	Non-secure Access Identifier signal.	
ARTAGOP_S[1:0]	Input	Type of TAGOP	

The following table shows the Read Data channel signals.

Table B-9: Read Data channel signals

Signal	Type	Description	Connection information
RREADY_S	Input	Read data ready.	Connect to corresponding master device, if populated, otherwise tie LOW.

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Signal	Type	Description	Connection information
RVALID_S	Output	Read data valid.	Connect to corresponding master device, if populated.
RID_S[x:0][2]	Output	Read data ID.	
RDATA_S[n:0][3]	Output	Read data.	
RRESP_S[1:0]	Output	Read data response.	
RLAST_S	Output	Read data last transfer indication.	
RUSER_S[0]	Output.	**RDATACHK** valid signal	
RTRACE_S	Output	Trace signal.	
RPOISON_S[p:0][5]	Output	Poison signal.	
RDATACHK_S[d:0][4]	Output	Data check signal.	
RLOOP_S[1:0]	Output	Loopback signal.	
RIDUNQ_S	Output	Unique ID indicator signal.	
RCHUNKV_S	Output	If asserted, **RCHUNKNUM** and **RCHUNKSTRB** are valid for this transfer.	
RCHUNKNUM_S	Output	Indicates the number of chunks being transferred. Chunks are numbered incrementally from zero, according to the data width and base address of the transaction.	
RCHUNKSTRB_S	Output	Indicates which part of read data is valid for this transfer. Each bit corresponds to 128 bits of data. **RCHUNKSTRB[0]** Corresponds to **RDATA[127:0]**. **RCHUNKSTRB[1]** Corresponds to **RDATA[255:128]**.	
RTAG_S[m:0][6]	Output	Read tags	-

The following table shows the Snoop Address channel signals. These signals are not included in an ACE-Lite interface without DVM.

Table B-10: Snoop Address channel signals

Signal	Type	Description	Connection information
ACREADY_S	Input	Snoop address ready.	Connect to corresponding master device, if populated, otherwise tie LOW.
ACVALID_S	Output	Snoop address valid.	Connect to corresponding master device, if populated.
ACADDR_S[n:0][3]	Output	Snoop address.	
ACSNOOP_S[3:0]	Output	Snoop transaction type.	
ACPROT_S[2:0]	Output	Snoop protection type.	
ACVMIDEXT[3:0]	Output	Snoop Address VMID Extension.	
ACTRACE	Output	Snoop address trace.	

The following table shows the Snoop Response channel signals. These signals are not included in an ACE-Lite interface without DVM.

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Table B-11: Snoop Response channel signals

Signal	Type	Description	Connection information
CRREADY_S	Output	Snoop response ready.	Connect to corresponding master device, if populated.
CRVALID_S	Input	Snoop response valid.	Connect to corresponding master device, if populated, otherwise tie LOW.
CRRESP_S[4:0]	Input	Snoop response.	
CRTRACE	Input	Snoop response trace.	


Note

WUSER_S[0] acts as a **WDATACHK** valid signal when DATACHECK_EN parameter is enabled.

- **If WUSER_S[0]**=0, the RN-I or RN-D synthesizes the correct **WDATACHK** value before sending it on CHI write request.
- If **WUSER_S[0]**=1, the RN-I or RN-D uses **WDATACHK** pin value to drive on CHI write request.

If the DATACHECK_EN parameter is disabled, the **WUSER_S[0]** input is ignored.


Note

RUSER_S[0] acts as an **RDATACHK** valid signal. Because the RN-I or RN-D always drives the **RDATACHK** value, **RUSER_S[0]** is set to 1 when DATACHECK_EN parameter is enabled.

If DATACHECK_EN parameter is disabled, **RUSER_S[0]** output is set to 0.

B.4.2 AXI/ACE-Lite master interface signals

HN-I and SBSX have an AXI/ACE-Lite master interface.


Note

For specific configurations, some of the SBSX pins must be tied off to certain values. For more information, see B.4.5 Conditions for tying off AXI/ACE-Lite master interface pins on page 1391.

The following table shows the clock enable signals.

Table B-12: Clock enable signals

Signal	Type	Description	Connection information
ACLKEN_M	Input	AXI Master bus clock enable signal.	Connect to clock-enable logic.
AWAKEUP_M	Output	Indicates that CI-700 is starting an AXI transaction.	Connect to corresponding slave device, if populated.

The following table shows the Write Address channel signals.

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Table B-13: Write Address channel signals

Signal	Type	Description	Connection information
AWREADY_M	Input	Write address ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
AWVALID_M	Output	Write address valid.	Connect to corresponding slave device, if populated.
AWID_M[x:0][8]	Output	Write address ID.	
AWADDR_M[n:0][9]	Output	Write address.	
AWLEN_M[7:0]	Output	Write burst length.	
AWSIZE_M[2:0]	Output	Write burst size.	
AWBURST_M[1:0]	Output	Write burst type.	
AWLOCK_M	Output	Write lock type.	
AWCACHE_M[3:0]	Output	Write cache type.	
AWUSER_M[z:0][10]	Output	User signal. **AWUSER[REQ_RSVDC_WIDTH-1:0]** Propagates REQ **RSVDC** value. **AWUSER[REQ_RSVDC_WIDTH]** Is_CopyBack Only propagated if `DSC_ENABLE` is set. **AWUSER[REQ_RSVDC_WIDTH+1]** Write Is_Dirty Only propagated if `DSC_ENABLE` is set.	
AWPROT_M[2:0]	Output	Write protection type.	
AWQOS_M[3:0]	Output	Write QoS value.	
AWSNOOP_M[3:0]	Output	Shareable write transaction type.	
AWDOMAIN_M[1:0]	Output	Write Shareability domain.	
AWTRACE_M	Output	-	
AWMPAM_M[10:0]	Output	MPAM signal. **AWMPAM[0]** MPAM_NS Security indicator, default = **AWPROT[1]**. **AWMPAM[9:1]** PARTID Partition identifier, default = `0x000`. **AWMPAM[10]** PMG Performance monitor group, default = `0b0`.	-

[8] For HN-I, `x` = 10. For SBSX, `x` = 21. For more information, see B.4.3 SBSX and MTSX AxID signal width and field assignments on page 1388.
[9] The value of `n` is configuration-dependent.
[10] `z` = `REQ_RSVDC_WIDTH` + (`DSC_ENABLE` × 2) - 1

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Signal	Type	Description	Connection information
AWIDUNQ_M	Output	Unique ID indicator signal.	-
AWNSAID_M[3:0]	Output	Non-secure Access Identifier signal.	Connect to corresponding slave device, if populated.
AWCMO_M[1:0]	Output	Type of CMO. This signal is only present on SBSX. It is not present on HN-I.	-
AWTAGOP_M[1:0]	Output	Write request tag operation	-

The following table shows the Write Data channel signals.


Note

WDATA is configurable to 128 bits or 256 bits. **WSTRB** scales accordingly.

Table B-14: Write Data channel signals

Signal	Type	Description	Connection information
WREADY_M	Input	Write data ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
WVALID_M	Output	Write data valid.	Connect to corresponding slave device, if populated.
WDATA_M[n:0][9]	Output	Write data.	
WSTRB_M[n:0][9]	Output	Write byte lane strobes.	
WLAST_M	Output	Write data last transfer indication.	
WUSER_M[0]	Output	**WDATACHK** valid signal.	
WPOISON_M[p:0][11]	Output	Poison signal.	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATACHK_M[d:0][12]	Output	Data check signal.	
WTRACE_M	Output	Trace signal.	
WTAG_M[y:0][13]	Output	The tag that is associated with write data.	-
WTAGUPDATE_M[m:0][14]	Output	Indicates which tags must be written to memory in the case of an Update operation.	-

[11] The value of `p` = ceil((`DATA_WIDTH` / 64) - 1).
[12] The value of `d` = (((n + 1) / 8) - 1).
[13] The value of `y` = (`DATA_WIDTH` / 128) - 1
[14] The value of `m` = (`DATA_WIDTH` / 128) - 1

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The following table shows the Write Response channel signals.

Table B-15: Write Response channel signals

Signal	Type	Description	Connection information
BREADY_M	Output	Write response ready.	Connect to corresponding slave device, if populated.
BVALID_M	Input	Write response valid.	Connect to corresponding slave device, if populated, otherwise tie LOW.
BID_M[x:0][8]	Input	Write response ID.	
BRESP_M[1:0]	Input	Write response.	
BUSER_M[3:0]	Input	User signal.	
BTRACE_M	Input	-	
BIDUNQ_M	Input	Unique ID indicator signal.	Connect to corresponding slave device, if populated, otherwise tie LOW.
BCOMP_M	Input	Write/CMO observable. This signal is only present on SBSX. It is not present on HN-I.	-
BPERSIST_M	Input	Data has been updated in persistent memory. This signal is only present on SBSX. It is not present on HN-I.	-
BTAGMATCH_M[1:0]	Input	Indicates the result of a tag comparison on a write transaction.	-

The following table shows the Read Address channel signals.

Table B-16: Read Address channel signals

Signal	Type	Description	Connection information
ARREADY_M	Input	Read address ready.	Connect to corresponding slave device, if populated, otherwise tie LOW.
ARVALID_M	Output	Read address valid.	Connect to corresponding slave device, if populated.
ARID_M[x:0][8]	Output	Read address ID.	
ARADDR_M[n:0][9]	Output	Read address.	
ARLEN_M[7:0]	Output	Read burst length.	
ARSIZE_M[2:0]	Output	Read burst size.	
ARBURST_M[1:0]	Output	Read burst type.	
ARLOCK_M	Output	Read lock type.	
ARCACHE_M[3:0]	Output	Read cache type.	
ARUSER_M[z:0][10]	Output	User signal. **ARUSER[REQ_RSVDC_WIDTH-1:0]** Propagates REQ **RSVDC** value. **ARUSER[REQ_RSVDC_WIDTH]** Migratable Only propagated if `DSC_ENABLE` is set. **ARUSER[REQ_RSVDC_WIDTH+1]** Accept_dirty Only propagated if `DSC_ENABLE` is set.	

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Signal	Type	Description	Connection information
ARPROT_M[2:0]	Output	Read protection type.	
ARQOS_M[3:0]	Output	Read QoS value.	
ARSNOOP_M[3:0]	Output	Shareable read transaction type.	
ARDOMAIN_M[1:0]	Output	Read Shareability domain.	
ARTRACE_M	Output	-	
ARMPAM_M[10:0]	Output	MPAM signal. **ARMPAM[0]** MPAM_NS Security indicator, default = **ARPROT[1].** **ARMPAM[9:1]** PARTID Partition identifier, default = `0x000`. **ARMPAM[10]** PMG Performance monitor group, default = `0b0`.	Connect to corresponding slave device, if populated.
ARIDUNQ_M	Output	Unique ID indicator signal.	Connect to corresponding slave device, if populated.
ARNSAID_M[3:0]	Output	Non-secure Access Identifier signal.	Connect to corresponding slave device, if populated.
ARTAGOP_M[1:0]	Output	Read request tag operation	-

The following table shows the Read Data channel signals.

Table B-17: Read Data channel signals

Signal	Type	Description	Connection information
RREADY_M	Output	Read data ready.	Connect to corresponding slave device, if populated.
RVALID_M	Input	Read data valid.	Connect to corresponding slave device, if populated, otherwise tie LOW.
RID_M[x:0][8]	Input	Read data ID.	
RDATA_M[127:0]/[255:0]	Input	Read data.	
RRESP_M[1:0]	Input	Read data response.	
RLAST_M	Input	Read data last transfer indication.	

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Signal	Type	Description	Connection information
RUSER_M[1:0]	Input	User signal. **RUSER_M[0]** Datacheck_en **RUSER_M[1]** Dirty bit. This bit is only available if `DSC_ENABLE` is set.	
RPOISON_M[p:0][11]	Input	Poison signal.	
RDATACHK_M[d:0][12]	Input	Data check signal.	Connect to corresponding master device, if populated.
RTRACE_M	Input	Trace signal.	Connect to corresponding master device, if populated, otherwise tie LOW.
RIDUNQ_M	Input	Unique ID indicator signal.	
RTAG_M[y:0][13]	Input	The tag that is associated with read data.	-

Note

RUSER_M[0] acts as an **RDATACHK** valid signal when `DATACHECK_EN` parameter is enabled.

- **If RUSER_M[0]** = 0, the SBSX or HN-I synthesizes the correct **RDATACHK** value before sending it on CHI read data response.
- If **RUSER_M[0]** = 1, the SBSX or HN-I uses the **RDATACHK** pin value to drive CHI read data response.
- If **RUSER_M[1]** = 0, the SBSX drives CompData_UC on the **TXDAT** flit.
- If **RUSER_M[1]** = 1, the SBSX drives CompData_UD_PD on the **TXDAT** flit.

If the `DATACHECK_EN` parameter is disabled, the **RUSER_M[0]** input is ignored.

Note

WUSER_M[0] acts as a **WDATACHK** valid signal. Because the SBSX or HN-I always drives the **WDATACHK** value, **WUSER_M[0]** is set to 1 when `DATACHECK_EN` parameter is enabled.

If the `DATACHECK_EN` parameter is not enabled, the **WUSER_M[0]** output is driven to 0.

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B.4.3 SBSX and MTSX AxID signal width and field assignments

SBSX supports a 24-bit **AxID** signal width. MTSX supports either a 9-bit or 24-bit **AxID** signal width, depending on whether the CI-700 configuration uses *RN-F Direct Slave Access* (DSA-F) mode. An internal parameter determines how the fields of the **AxID** signal are populated.

The value of the `DSA_EN` parameter determines whether DSA-F mode is enabled. This parameter affects the **AxID** signal widths in the following way:

`DSA_EN` = 0
: DSA-F mode is disabled, so all SBSX and MTSX nodes have a 24-bit **AxID** signal.

`DSA_EN` = 1
: DSA-F mode is enabled, so MTSX nodes have a 9-bit **AxID** signal.


Remember

SBSXs do not support DSA-F, so they cannot be present in a DSA-F configuration.

In SBSX and MTSX nodes, an internal extended **AxID** parameter (`EXT_AXID`) determines how the fields of the **AxID** signal are populated. This parameter is set if memory tagging is enabled or DSA-F mode is disabled. This means that, `EXT_AXID` = 1 if `AXMTE_EN` = 1 or `DSA_EN` = 0.

The resulting **AxID** TrkrID field represents different trackers depending on the type of transaction. For write transactions, TrkrID represents the Req tracker entry. For read transactions, TrkrID represents the DART tracker entry. The DART tracker depth must be equal to or larger than the Req tracker depth. Therefore, the DART tracker depth determines the width of the TrkrID field.

24-bit AxID formats

The following properties related to **AxID** formatting apply to a CI-700 configuration with DSA-F mode disabled:

- Exclusives are not supported.
- In MTSX, the MTU bit position in the **AxID** signal colors MTU requests.

If `EXT_AXID` = 1, the 24-bit **AxID** signal fields are formatted in the following way:

AxID = {MTU, Excl, 2-part PCMO, ReturnNID[$\log_2$(NUM(RNF+RNI+RND+HNF))-1:0], GroupIDExt[2:0], PGroupID[4:0], TrkrID[$\log_2$(TrkrDepth)-1:0]}

For example, consider a configuration with:

- A DART tracker that is 128 entries deep
- 64 or less RN-F, RN-I, RN-D, and HN-F nodes in total

In this case, the **AxID** format is:

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AxID[23]
MTU coloring

AxID[22]
Exclusive coloring, 1'b0

AxID[21]
2-part PCMO coloring

AxID[20:15]
ReturnNID[5:0]

AxID[14:12]
GroupIDExt[2:0]

AxID[11:7]
PGroupID[4:0]

AxID[6:0]
TrkrID[6:0]

If EXT_AXID = 0, the 24-bit **AxID** signal fields are formatted in the following way:

AxID = {MTU, Excl, TrkrID[$\log_2$(TrkrDepth)-1:0]}

Using the same configuration as the preceding example, the **AxID** format is:

AxID[23:19]
Unused, tied to 0

AxID[8]
MTU coloring

AxID[7]
Exclusive coloring, 1'b0

AxID[6:0]
TrkrID[6:0]

9-bit AxID formats

The following properties related to **AxID** formatting apply to a CI-700 configuration with DSA-F mode enabled:

- Exclusives are supported. The Excl bit position of the **AxID** signal colors exclusives.
- In MTSX, the MTU bit position in the **AxID** signal colors MTU requests.

For non-exclusive requests, the 9-bit **AxID** signal fields are formatted in the following way:

AxID = {MTU, Excl, TrkrID[$\log_2$(TrkrDepth)-1:0]}

For example, consider a configuration with a DART tracker that is 128 entries deep. In this case, the **AxID** format is:

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AxID[8]
MTU coloring

AxID[7]
Exclusive coloring, 1'b0

AxID[6:0]
TrkrID[6:0]

For exclusive requests, the 9-bit **AxID** signal fields are formatted in the following way:

AxID = {MTU, Excl, LPID[4:0], ReturnNID[$\log_2$(NUM(RNF))-1:0]}

For example, in a configuration with a DART tracker that is 128 entries deep, the **AxID** format is:

AxID[8]
MTU coloring

AxID[7]
Exclusive coloring, 1'b0

AxID[6:2]
LPID[4:0]

AxID[1:0]
ReturnNID[1:0] (supports a maximum of four RN-Fs max)

B.4.4 Special considerations for AxUSER signals

There are special considerations regarding the **AxUSER** signals in CI-700.

The **AxUSER** signals are generally used to propagate CHI.REQ.RSVDC. They have the following overrides:

At the SBSX interface:

AWUSER[0]	WriteEvict hint
AxUSER[1]	Tag versus data
WUSER[9:1]	**WID[8:0]**
WUSER[0]	Parity valid

At the HN-D interface:

WUSER[9:1]	**WID[8:0]**
WUSER[0]	Parity valid

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B.4.5 Conditions for tying off AXI/ACE-Lite master interface pins

Certain CI-700 configuration conditions require some AXI/ACE-Lite master interface pins on certain components to be tied-off to specific values.

The following table shows the conditions under which you must tie off certain pins on specific blocks and the required tie-off values.

Table B-18: Tie-off conditions and values for units with AXI/ACE-Lite master interfaces

Unit	Pins	Tie-off conditions	Tie-off value
SBSX or MTSX	**BCOMP_M**	SBSX `CMO_ON_AW` parameter = 0 & AXI MTE_Support property != Standard	`0b1`
SBSX	**BPERSIST_M**	SBSX `CMO_ON_AW` parameter = 0	`0b0`
SBSX	**BTAGMATCH_M**	AXI MTE_Support property != Standard	`0b0`
SBSX	**RRESP[2]**	AXI Prefetch_Transaction property = 0	`0b0`
MTSX	**BTAGMATCH_M**	Must always be tied off.	`0b0`
MTSX	**RTAG_M**	Must always be tied off.	`0b0`
HN-I, HN-D, or HN-T	**RRESP[2]**	Must always be tied off.	`0b0`

B.4.6 A4S signals

The A4S interface signals are listed in the following tables.

Signal definitions

Table B-19: A4S Transmit and Receive signals

Signal	Direction	Description	Connection information
TXA4STREADY	Input	**TXA4STREADY** indicates that the slave can accept a transfer in the current cycle.	Connect from **RXA4STREADY** of the A4S slave, if populated, otherwise tie LOW.
TXA4STVALID	Output	**TXA4STVALID** indicates that the master is driving a valid transfer. A transfer takes place when both **TXA4STVALID** and **TXA4STREADY** are asserted.	Connect to **RXA4STVALID** of the A4S slave, if populated.
TXA4STDEST[7:0]	Output	`0b00000000`	**TXA4STDEST** is always zero.
TXA4STID[7:0]	Output	**TXA4STID** is the data stream identifier that indicates different streams of data.	Connect to **RXA4STID** of the A4S slave, if populated.
TXA4STDATA[63:0]	Output	**TXA4STDATA** is the primary payload that is used to provide the data that is passing across the interface.	Connect to **RXA4STDATA** of the A4S slave, if populated.
TXA4STSTRB[7:0]	Output	**TXA4STSTRB** is the byte qualifier that indicates whether the content of the associated byte of **TXA4STDATA** is processed as a data byte or a position byte.	Connect to **RXA4STSTRB** of the A4S slave, if populated.

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Signal	Direction	Description	Connection information
TXA4STKEEP[7:0]	Output	**TXA4STKEEP** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as part of the data stream. Associated bytes that have the **TKEEP** byte qualifier deasserted are null bytes and can be removed from the data stream.	Connect to **RXA4STKEEP** of the A4S slave, if populated.
TXA4STLAST	Output	**TXA4STLAST** indicates the boundary of a packet.	Connect to **RXA4STLAST** of the A4S slave, if populated.
RXA4STREADY	Output	**RXA4STREADY** indicates that the slave can accept a transfer in the current cycle.	Connect to **TXA4STREADY** of the A4S master, if populated.
RXA4STVALID	Input	**RXA4STVALID** indicates that the master is driving a valid transfer. A transfer takes place when both **RXA4STVALID** and **RXA4STREADY** are asserted.	Connect from **TXA4STVALID** of the A4S master, if populated, otherwise tie LOW.
RXA4STDEST[7:0]	Input	**RXA4STDEST** provides routing information for the data stream.	Connect from **TXA4STDEST** of the A4S master, if populated, otherwise tie LOW.
RXA4STID[7:0]	Input	**RXA4STID** is the data stream identifier that indicates different streams of data.	Connect from **TXA4STID** of the A4S master, if populated, otherwise tie LOW.
RXA4STRI[7:0]	Input	-	Tie LOW.
RXA4STDATA[63:0]	Input	**RXA4STDATA** is the primary payload that is used to provide the data that is passing across the interface.	Connect from **TXA4STDATA** of the A4S master, if populated, otherwise tie LOW.
RXA4STSTRB[7:0]	Input	**RXA4STSTRB** is the byte qualifier that indicates whether the content of the associated byte of **RXA4STDATA** is processed as a data byte or a position byte.	Connect from **TXA4STSTRB** of the A4S master, if populated, otherwise tie LOW.
RXA4STKEEP[7:0]	Input	**RXA4STKEEP** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as part of the data stream. Associated bytes that have the **TKEEP** byte qualifier deasserted are null bytes and are removed from the data stream.	Connect from **TXA4STKEEP** of the A4S master, if populated, otherwise tie LOW.
RXA4STLAST	Input	**RXA4STLAST** indicates the boundary of a packet.	Connect from **TXA4STLAST** of the A4S master, if populated, otherwise tie LOW.

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B.5 APB interface signals

HN-D nodes have an APB interface to support the connection of an external APB master device.

Signal definitions

Table B-20: APB signals

Signal	Direction	Description	Connection information
PADDR[31:0]	Input	Address that is associated with the APB transaction.	Connect to corresponding ports on external APB master device.
PPROT[2:0]	Input	Protection type of the transaction.	
PSEL	Input	Indicates that the slave device is selected and that a data transfer is required.	
PENABLE	Input	Enable. Indicates the second and subsequent cycles of an APB transfer.	
PWRITE	Input	Indicates that the access is a write when HIGH. Indicates that the access is a read when LOW.	
PWDATA[31:0]	Input	Write data.	
PSTRB[3:0]	Input	Write strobes.	
PREADY	Output	Ready.	
PRDATA[31:0]	Output	Read data.	
PSLVERR	Output	Indicates a transfer failure.	

B.6 Debug, trace, and PMU interface signals

Signals that aid debugging are included in CI-700.



All signal names in this section are only a root name indicated as **RootName**. CI-700 interfaces use **RootName** within a more fully specified signal name as follows:

CI-700 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Signal definitions

Table B-21: Debug, trace, and PMU interface signals

Signal	Direction	Description	Connection information
ATCLKEN_NID<x>	Input	ATB clock enable, where <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-

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Signal	Direction	Description	Connection information
ATREADY_NID<x>	Input	ATB device ready: **0** Not ready **1** Ready <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
AFVALID_NID<x>	Input	FIFO flush request, where <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
ATDATA[31:0]_NID<x>	Output	ATB data bus, where <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
ATVALID_NID<x>	Output	ATB valid data: **0** No valid data **1** Valid data <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
ATBYTES[1:0]_NID<x>	Output	CoreSight ATB device data size: **0b00** 1 byte **0b01** 2 bytes **0b10** 3 bytes **0b11** 4 bytes <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
AFREADY_NID<x>	Output	FIFO flush acknowledge: **0** FIFO flush not complete **1** FIFO flush complete <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
ATID[6:0]_NID<x>	Output	ATB trace source identification, where <x> is the NodeID number for that HN-D DTC or HN-T DTC.	-
DBGWATCHTRIGREQ_NID<x>	Output	Trigger output from DEM indicating assertion of a DT event. **DBGWATCHTRIGREQ** is asynchronous-safe, and operates in a four-phase handshake with **DBGWATCHTRIGACK**. <x> is the NodeID number for that HN-D DTC or HN-T DTC.	Connect to external debug and trace control logic.

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Signal	Direction	Description	Connection information
DBGWATCHTRIGACK_NID<x>	Input	External acknowledgment of receipt of **DBGWATCHTRIGREQ**. **DBGWATCHTRIGACK** must be asynchronous-safe, and operates in a four-phase handshake with **DBGWATCHTRIGREQ**. <x> is the NodeID number for that HN-D DTC or HN-T DTC.	Connect to external debug and trace control logic, or tie LOW if **DBGWATCHTRIGREQ** is unused.
PMUSNAPSHOTREQ	Input	External request that the live PMU counters are snapshot to the shadow registers. **PMUSNAPSHOTREQ** must be asynchronous-safe, and operates in a four-phase handshake with **PMUSNAPSHOTACK**.	Connect to external debug and trace control logic, or tie LOW if unused.
PMUSNAPSHOTACK	Output	Indication that all live PMU counters have been copied to shadow registers and the contents can be read. **PMUSNAPSHOTACK** is asynchronous-safe, and operates in a four-phase handshake with **PMUSNAPSHOTREQ**.	Connect to external debug and trace control logic.
NIDEN	Input	Global enable for all debug, trace, and PMU functionality: **0** Disabled. **1** Enabled.	Tie or drive as appropriate to meet system security requirements.
SPNIDEN	Input	Global enable for Secure debug, trace, and PMU capability. Only applicable when **NIDEN** is enabled. **0** Disabled. **1** Enabled.	
TSVALUEB[63:0]	Input	Global system timestamp value in binary format.	Connect to external system timestamp counter output.

B.7 ATPG interface signals

Signals that support ATPG capabilities are included in CI-700.

Signal definitions

Table B-22: DFT signals

Signal	Direction	Description	Connection information
DFTCLKBYPASS	Input	Select the SLC RAM clock to follow the CI-700 input clock, as applicable for each clock region.	Tie LOW if unused.
DFTCLKDISABLE[3:0]	Input	Disable clock regions during scan shift.	
DFTRAMHOLD	Input	Disable the RAM chip select during scan shift.	
DFTMCPHOLD	Input	Assert to prevent HN-F multicycle RAMs from clocking during capture cycles.	
DFTRSTDISABLE	Input	Disable internal synchronized reset during scan shift.	
DFTCGEN	Input	Scan shift enable. Forces on the clock grids during scan shift.	

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Signal	Direction	Description	Connection information
DFTSCANMODE	Input	During functional mode, the HN-F SLC and SF RAM set address and write data inputs satisfy RAM hold timing constraints using pipeline behavior. The set address and write data are only clocked and enabled the cycle before the RAMs are accessed. They are held the cycle that the RAM clock asserts. The RAM hold constraints are not guaranteed during ATPG test. The constraints are not guaranteed because random data is shifted into the flops that control the set address and write data flop enables. Therefore, the set address and write data to change in the same cycle as a RAM access, violating the RAM hold constraints. This signal addresses the hold constraints during ATPG test. It is used to force the RAM set address and write data flop enables LOW in the cycle that RAM clocks are enabled during ATPG test. The combination of the functional pipeline behavior and this override logic enable holds MCPs to be used on the RAM set address and write data inputs in the implementation flow and during static timing analysis.	

B.7.1 Block-level ATPG signals

CI-700 supports DFT using the ATPG methodology. The design contains signals that are used to carry out ATPG testing.

The following table lists the ATPG signals at the HN-F por_hnf block-level.

Table B-23: HN-F block-level por_hnf ATPG signals

Signal	Direction	Description
DFTCLKBYPASS	Input	Bypasses stretch RAM clock for `STRETCH_L3RAMCLK and STRETCH_MTURAMCLK configuration parameters. Functional mode = 0b0.
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift. Functional mode = 0b0.
DFTCLKDISABLE	Input	Disables clock regions during test to save power. Functional mode = 0b0.
DFTCGEN	Input	Overrides clock gate shift. Functional mode = 0b0.
DFTRAMHOLD	Input	Blocks chip select to RAMs to preserve state. Functional mode = 0b0.
DFTMCPHOLD	Input	Limits number of multicycle path toggles during ATPG delay tests. Functional mode = 0b0.
DFTSCANMODE	Input	Prevents potential RAM input hold violations during ATPG. Functional mode = 0b0.
clk_por	Input	Functional clock.
nSKYRESET	Input	Functional reset. Active-LOW.
nMBISTRESET	Input	MBIST mode entry reset. Functional mode = 0b1. Active-LOW.

The following table lists the ATPG signals at the HN-D block-level (por_hnd), at the HN-I block-level (por_hni), at the HN-T block-level (por_hnt), and at the SBSX block-level (por_sbsx).

Table B-24: HN-D/HN-I/HN-T/SBSX block-level por_hnd/por_hni/por_hnt/por_sbsx ATPG signals

Signal	Direction	Description
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift. Functional mode = 0b0.

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Signal	Direction	Description
DFTCLKDISABLE	Input	Disables clock regions during test to save power. Functional mode = `0b0`.
DFTCGEN	Input	Overrides clock gate shift. Functional mode = `0b0`.
DFTCLKBYPASS	Input	Bypasses stretch RAM clock for `` `STRETCH_L3RAMCLK `` configuration parameter. Functional mode = `0b0`.
clk_por	Input	Functional clock.
nCHIRESET	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals at the MTSX block-level (por_mtsx), at the RN-I block-level (por_rni), and at the RN-D block-level (por_rnd).

Table B-25: MTSX/RN-I/RN-D block-level por_mtsx/por_rni/por_rnd ATPG signals

Signal	Direction	Description
DFTCLKBYPASS	Input	Bypasses stretch RAM clock for `` `STRETCH_L3RAMCLK `` configuration parameter. Functional mode = `0b0`.
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
DFTCLKDISABLE	Input	Disables clock gate regions during test to save power. Functional mode = `0b0`.
DFTCGEN	Input	Overrides clock gate shift. Functional mode = `0b0`.
DFTRAMHOLD	Input	Blocks chip select to RAMs to preserve state. Functional mode = `0b0`.
DFTMCPHOLD	Input	Limits number of multicycle path toggles during ATPG delay tests. Functional mode = `0b0`.
DFTSCANMODE	Input	Prevents violation of the HN-F RAM input multicycle hold paths on data and address RAM inputs. Signal is only present on MTSX ATPG interface.
clk_por	Input	Functional clock.
nCHIRESET	Input	Functional reset. Active-LOW.
nMBISTRESET	Input	MBIST mode entry reset. Functional mode = `0b1`. Active-LOW.

The following table lists the ATPG signals as internal pins for SMXP blocks named por_smxp_*. Arm recommends that you use the drivers of these internal pins for any DFT purposes during synthesis.

Table B-26: SMXP block-level por_smxp_* ATPG signals

Signal	Direction	Description
u_mxp_misc.mxp_dftrstdisable	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
u_mxp_misc.mxp_dftclkdisable	Input	Disables clock regions during test to save power. Functional mode = `0b0`.
u_mxp_misc.mxp_dftcgen	Input	Overrides clock gate shift. Functional mode = `0b0`.
clk_por	Input	Functional clock.
u_mxp_misc.reset_por	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals as internal nets for MCS blocks named por_mcsx and por_mcsy. Arm recommends that you use the drivers of these internal pins for any DFT purposes during synthesis.

Table B-27: MCS block-level por_mcsx/por_mcsy ATPG signals

Signal	Direction	Description
mcs_dftrstdisable	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
mcs_dftcgen	Input	Overrides clock gate shift. Functional mode = `0b0`.
clk_por	Input	Functional clock.

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Signal	Direction	Description
mcs_nporreset	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals as internal nets for DCS blocks named por_dcs_*. Arm recommends that you use the drivers of these internal pins for any DFT purposes during synthesis.

Table B-28: DCS block-level por_dcs_* ATPG signals

Signal	Direction	Description
dcs_dftrstdisable	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
dcs_dftcgen	Input	Overrides clock gate shift. Functional mode = `0b0`.
clk_por	Input	Functional clock.
dcs_nporreset	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals as internal nets for CCS blocks named por_ccs_*. Arm recommends that you use the drivers of these internal pins for any DFT purposes during synthesis.

Table B-29: CCS block-level por_ccs_* ATPG signals

Signal	Direction	Description
ccs_dftrstdisable	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
ccs_dftcgen	Input	Overrides clock gate shift. Functional mode = `0b0`.
clk_por	Input	Functional clock.
ccs_nporreset	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals as internal nets for CAL blocks named por_cal2_*. Arm recommends that you use the drivers of these internal pins for any DFT purposes during synthesis.

Table B-30: CAL block-level por_cal2_* ATPG signals

Signal	Direction	Description
cal_dftrstdisable	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
cal_dftcgen	Input	Overrides clock gate shift. Functional mode = `0b0`.
clk_por	Input	Functional clock.
cal_nporreset	Input	Functional reset. Active-LOW.

The following table lists the ATPG signals at the CDB block-level (cdb_rnf/cdb_snf).

Table B-31: CDB block-level cdb_rnf/cdb_snf ATPG signals

Signal	Direction	Description
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
DFTCGEN	Input	Overrides clock gate shift. Functional mode = `0b0`.
CLK_DEV, CLK_ICN	Input	Functional clocks.
RESETN_DEV, RESETN_ICN	Input	Functional resets. Active-LOW.

The following table lists the ATPG signals at the ADB block-level (adb_*).

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Table B-32: ADB block-level adb_* ATPG signals

Signal	Direction	Description
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift. Functional mode = `0b0`.
DFTCGEN	Input	Overrides clock gate shift. Functional mode = `0b0`.
CLK_S, **CLK_M**	Input	Functional clocks.
RESETN_S, **RESETN_M**	Input	Functional resets. Active-LOW.

B.8 Clock management signals

This section contains information on clock management Q-Channel signals in the CI-700.

Signal definitions

Table B-33: Clock management Q-Channel signals

Signal	Direction	Description	Connection information
QACTIVE_CLKCTL	Output	Indication that CI-700 is active, and that the *External Clock Controller* (ExtCC) must not make a request for CI-700 to prepare to stop the clocks.	Connect to external clock controller.
QREQn_CLKCTL	Input	Request from the ExtCC for the CI-700 to prepare to stop the clocks. Active-LOW.	Connect to external clock controller or tie HIGH if unused.
QACCEPTn_CLKCTL	Output	Positive acknowledgment after receiving **QREQn** assertion indicating that CI-700 has completed preparation to stop the clocks and that the ExtCC can stop the clocks. Active-LOW.	Connect to external clock controller.
QDENY_CLKCTL	Output	Negative acknowledgment after receiving **QREQn** assertion indicating that CI-700 has refused the request from the ExtCC to prepare to stop the clocks.	

B.9 Power management signals

This section contains information on power management signals for the logic power domain.

Signal definitions

Table B-34: Power management signals for logic power domain

Signal	Direction	Description	Connection information
PREQ_LOGIC	Input	Indicates a request for a power state transition.	Connect to external power management controller or tie LOW if unused.
PSTATE_LOGIC[4:0]	Input	The power state to which a transition is requested.	Connect to external power management controller or tie to `5'b01000` if unused.
PACCEPT_LOGIC	Output	Indicates acknowledgment of the power state transition and completion of the power state transition within CI-700.	Connect to external power management controller.

[15] If MCP, the MCP duration must be ≤8 cycles to the last flop to receive this signal. This constraint is a requirement for implementation.

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Signal	Direction	Description	Connection information
PDENY_LOGIC	Output	Indicates denial of the power state transition.	
PACTIVE_LOGIC	Output	Hint that indicates activity across the CI-700. When LOW, indicates the possibility of entering static retention or the OFF state.	

If **PACTIVE_LOGIC** is asserted, the system cannot be powered down.

B.10 Interrupt and event signals

The following table shows the interrupt and event signals.

All signal names in this section are root names, which are specified as **RootName**. CI-700 interfaces use **RootName** within a fully specified signal name as follows:

CI-700 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Signal definitions

Table B-35: Interrupt and event signals

Signal	Direction	Description	Connection information
INTREQPPU	Output	Power state transition complete	Connect to external interrupt control logic or Generic Interrupt Controller.
INTREQPMU_NID<x>	Output	PMU count overflow interrupt. NID indicates node ID where <x> represents the NodeID number for the HN-D DTC or HN-T DTC.	
INTREQERRNS	Output	Non-secure error handling interrupt.	
INTREQERRS	Output	Secure error handling interrupt.	
INTREQFAULTNS	Output	Non-secure fault handling interrupt.	
INTREQFAULTS	Output	Secure fault handling interrupt.	
INTREQMPAMERRNS	Output	Non-secure *Memory System Resource Partitioning and Monitoring* (MPAM) fault handling interrupt.	
INTREQMPAMERRS	Output	Secure MPAM fault handling interrupt.	

B.11 Configuration input signals

The following table shows the configuration input signals.

All of these signals must be stable at least ten cycles before deassertion of reset. These signals must remain stable throughout the operation of CI-700, until a following reset assertion or power down, if any.

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Signal definitions

Table B-36: Configuration input signals

Signal	Direction	Description	Connection information
CFGM_PERIPHBASE [47:x][16]	Input	Base address [47:x][16] of the CI-700 configuration register space.	Tie as required for system memory map.

B.12 Processor event interface signals

Signals that support processor event interface capabilities are included in CI-700. Processor event interface signals are present at RN-F, RN-I, and RN-D node locations.


Note

All signal names in this section are only a root name indicated as **RootName**. CI-700 interfaces use **RootName** within a more fully specified signal name as follows:

CI-700 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

Signal definitions

Table B-37: Processor event interface signals

Signal	Direction	Description	Connection information
EVENTIREQ	Output	Event input request for processor wake up from WFE state. Remains asserted until **EVENTIACK** is asserted, and is not reasserted until **EVENTIACK** is LOW.	Connect to **EVENTIREQ** input of processor.
EVENTIACK	Input	Event input request acknowledge. Must not be asserted until **EVENTIREQ** is HIGH, and then must remain asserted until after **EVENTIREQ** goes LOW.	Connect to **EVENTIACK** output of processor, or tie to **EVENTIREQ** output of CI-700 if unused.
EVENTOREQ	Input	Event output request for processor wake up, triggered by SEV instruction. Must only be asserted when **EVENTOACK** is LOW, and then must remain HIGH until after **EVENTOACK** goes HIGH.	Connect to **EVENTOREQ** output of processor, or tie LOW if unused.
EVENTOACK	Output	Event output request acknowledge. Is not asserted until **EVENTOREQ** is HIGH, and then remains asserted until after **EVENTOREQ** goes LOW.	Connect to **EVENTOACK** input of processor.

1. Event handling logic external to CI-700 must handle **EVENT_OUT** from CHI processor. **EVENT_OUT** is a multicycle pulse. If system integration wants to connect the **EVENT_OUT** to CI-700 **EVENTOREQ** or **EVENTOACK**, then stitching logic is required. It is the responsibility of the integrator to design the necessary logic to stitch **EVENT_OUT** to the four-phase handshake pair, accounting for the asynchronous domain crossing.
2. Event handling logic external to CI-700 can drive **EVENT_IN** of CHI processor.

[16] The value x depends on the configuration:

Mesh configuration

x = 28

Single-MXP configuration

x = 23

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Appendix C Revisions

This appendix describes the technical changes between released issues of this manual.

Table C-1: Issue 0000-02

Change	Location
First release	-

Table C-2: Differences between issue 0000-02 and issue 0100-03

Change	Location
Product branding updates	Throughout document
Added *RN-F Direct Slave Access* (DSA-F) feature to feature list	2.3 Features on page 18
Updated the following top-level configuration options: • Removed specific restriction on DCS number with CCS • Updated possible values for `REQ_RSVDC_WIDTH` parameter • Corrected statement regarding connection of HN-Is, HN-Ds, and HN-Ts to CAL. CI-700 only supports connection of HN-Is to CAL.	Change superseded by later version.
Added r1p0 product revision information	2.8 Product revisions on page 26
Added new section describing DSA-F	4.8 RN-F Direct Slave Access on page 117
Added note describing specific clocking requirements for the P-Channel interface	4.2.2 Power domain control on page 64
Updated table to remove some irrelevant NodeID example information	Table 4-14: Node ID[4:0] encodings for single-MXP configuration with extra device ports on page 82
Updated RN SAM memory region requirements to clarify that partitions must be size-aligned. Added clarification that SCGs can be configured to non-hashed mode.	Change superseded by later version
Updated information regarding SCG configuration to describe the algorithm that distributes nodeIDs between SCG registers, and provide more programming examples	4.5.4 System Cache Groups on page 90
Updated discovery section to remove some information that was unclear. Clarified that node and configuration register offsets can be found in the IP-XACT file for your configuration.	• 4.12.1 Configuration address space organization on page 127 • 4.12.3 Child pointers on page 132
Updated error interrupt handler flow example because the old example was incorrect	4.17 Reliability, Availability, and Serviceability on page 141
Updated description of DVM message handling to clarify that DVM messages are not supported in a DSA-F configuration	4.18.4 Distributed Virtual Memory messages on page 162
Added example for configuring CBusy tracking for previous 128 or 256 transactions. Also, for CBusy handling, clarified that NonCopyBack type requests include write plus (P)CMOs, not all CMOs	4.18.5.1 Advanced CBusy handling in HN-F on page 164
Updated the maximum size of the configuration register address space for single-MXP configurations. This is now 8MB. Also corrected the description of the APB interface addressing scheme.	5.1.1 Node configuration register address mapping on page 179
Added description of the relationship between the first level of discovery and the MXP registers.	5.1.2 Global configuration register region on page 180

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Change	Location
Clarified that the address of the APB interface does not contain the PERIPHBASE offset	5.1.5 Requirements of configuration register reads and writes on page 181
Added sam_generic_regs0 register	5.3.9.100 sam_generic_regs0 on page 1111
Updated description of pmu_event0_id field of por_mxp_pmu_event_sel register	5.3.6.22 por_mxp_pmu_event_sel on page 750
Added new fields to por_rnd_aux_ctl register	5.3.7.7 por_rnd_aux_ctl on page 880
Updated encodings of PMU events in por_rnd_pmu_event_sel register	5.3.7.26 por_rnd_pmu_event_sel on page 909
Added new fields to por_rni_aux_ctl register	5.3.8.7 por_rni_aux_ctl on page 922
Updated encodings of PMU events in por_rni_pmu_event_sel register	5.3.8.26 por_rni_pmu_event_sel on page 952
Updated register reset value of por_sbsx_cfg_ctl register, updated existing register fields, and added new register fields	5.3.10.5 por_sbsx_cfg_ctl on page 1117
Updated reset values of por_hnf_mpam_idr register	5.3.11.3 por_hnf_mpam_idr on page 1140
Updated name of mtu_dram_addr_width field of the por_mtu_unit_info register. The updated field name is mtu_max_dram_addr_width.	5.3.13.4 por_mtu_unit_info on page 1217
Added a new field to the por_mtu_aux_ctl register	5.3.13.6 por_mtu_aux_ctl on page 1220
Increased width and added a new encoding to the memory_map_mode field of the por_mtu_tag_addr_ctl register	5.3.13.9 por_mtu_tag_addr_ctl on page 1223
Added new prerequisites to SAM programming sequence	5.4.3.1 Program the SAM on page 1278
Corrected an inaccuracy in the value of the region1_size field of the non_hash_mem_region_reg1 register in the example memory map programming	Table 5-1430: RN SAM registers and programmed values on page 1281
Added more information about the memory map modes that the por_mtu_tag_addr_ctl register supports	5.4.6.1 Programming MTU tag address generation registers on page 1285
Updated figure showing the relationship between mtu_tag_addr_base and DRAM tag space base address	Figure 5-1421: Relationship between mtu_tag_addr_base and DRAM tag space base address on page 1290
Updated the steps to program DTM watchpoints	5.4.7.1 Program DTM watchpoint on page 1292
Updated description to the SLC handling of CleanInvalid and CleanShared CMOs in OCM mode	6.2.7 Software-configurable On-Chip Memory on page 1304
Updated table showing settings for the hnf_slc_lock_baseX register to show that the contents of the table depend on a configuration parameter value	6.2.6 Software-configurable memory region locking on page 1302
Added more information about the MPAM errors that CI-700 supports	6.4.5.5 MPAM error logging and reporting on page 1315
Updated figure showing the DTM WP comparator to correct the logic	Figure 7-2: DTM WP comparator on page 1323
Updated RSP control flit and DAT control flit trace data format	• Table 7-11: RSP control flit on page 1329 • Table 7-13: DAT control flit on page 1330
Updated cross trigger example programming steps	7.2.4.1 Cross trigger example programming on page 1341
Updated equations to calculate SBSX AxID widths	B.4.3 SBSX and MTSX AxID signal width and field assignments on page 1388
Added new section describing special considerations for **AxUSER** signals	B.4.4 Special considerations for AxUSER signals on page 1391

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Change	Location
Updated description of the **CFGM_PERIPHBASE** signal to provide more detail about differences between mesh and single-MXP configurations	B.11 Configuration input signals on page 1401

Table C-3: Differences between issue 0100-03 and issue 0100-04

Change	Location
Updated node ID mapping example figures to show decimal node ID values and added more textual detail to clarify how node IDs are calculated. Also clarified that, for default node ID mapping scheme, bits[1:0] of the node ID in all formats correspond to the device ID, rather than a hard-coded `0b00`.	• 4.3.1 Default node ID mapping on page 74 • 4.3.2 Node ID mapping for configurations with extra device ports on page 77
Updated description of restrictions on SCG selection. Added description of separate SCG non-hashed mode register.	4.5.6 Configuring SCGs in the RN SAM on page 92
Corrected name of `RXBUF_NUM` parameter in description of flit uploads from RN-F and SN-F.	4.13.2 Flit uploads from RN-F or SN-F on page 137
Corrected example HN-F SAM programming information. Previously, hn_cfg_sam_top_address_bit0 and hn_cfg_sam_top_address_bit1 were in the wrong order in the table.	Table 5-1431: HN-F programming information on page 1282
Updated deferred errors that are supported by HN-F to include double-bit ECC detection in SLC tag RAM.	6.3 Error reporting and software-configured error injection on page 1307
Clarified the trace tag example sequence steps.	7.2.2.4 Trace tag example programming on page 1339
The following changes are for improved content quality. The general technical meaning of the content has not changed.	
Added new components and configuration chapter, which contains some of the information from the introduction and functional description of the previous release.	3 Components and configuration on page 27
Added description of interchangeable terms for XP components.	3.2 Crosspoint (XP) on page 28
Updated description of external interfaces, figure, and table to include more information about the interfaces.	3.3 External interfaces on page 32
Updated components section to add summary tables of external devices, internal devices, and mesh components. Moved description of *CHI Domain Bridge* (CDB) and *AMBA Domain Bridge* (ADB) components to the mesh components table.	3.4 Components on page 34
Updated RN-I description to clarify information that is shared with or related to RN-D.	3.4.1 I/O coherent Request Node (RN-I) and I/O coherent Request Node with DVM support (RN-D) on page 37
Updated HN-I description to add more information about HN-I variants and condense information about colocated blocks.	3.4.3 I/O coherent Home Node (HN-I) on page 38
Updated structure of information about configuring CI-700, to clarify the process. Also added more supporting information regarding the process.	3.5 Configure CI-700 on page 43
Added more supporting information about factors to consider when selecting components.	3.6 System component selection on page 44

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Change	Location
Created separate sections for: • Information on deciding on the size of the mesh • Information on permitted numbers of devices and system resources • Configurable options for mesh structure. Also moved information about support and topology considerations for extra device ports on MXPs here. • Global configuration parameters. Also moved information regarding addressing capabilities alongside global configuration parameters. • Device-level configuration parameters. Also moved guidance on selecting the optimal total SF size across all HN-Fs to this section. Removed information about placing devices in the mesh that was no longer useful.	• 3.7 Deciding on the size of the mesh on page 47 • 3.8 Permitted numbers of devices and system resources in the mesh on page 47 • 3.9 Configurable options for mesh structure on page 49 • 3.10 Support for extra device ports on MXPs on page 50 • 3.11 Topology considerations when using extra device ports on page 50 • 2.4 Global configuration parameters on page 20 • 2.4.1 Addressing capabilities on page 21 • 2.5 Device-level configuration parameters on page 21
Condensed conceptual overview information about the SAM.	4.4 System Address Map on page 82
Added more supporting high-level conceptual information about the RN SAM.	4.5 RN SAM on page 84
Created separate sections and more supporting information for the following: • Information about RN SAM memory regions, target types, and region requirements. Condensed conceptual information regarding memory regions from multiple separate locations. Added clarification about the handling of read and write requests targeting HN-D that do not target the configuration register space. • Condensed conceptual information regarding *System Cache Groups* (SCGs) from multiple separate locations. • Information about RN SAM target ID selection • Information about SCG HN-F hash algorithm • Information about configuring SCGs in the RN SAM. Also clarified that information about hashed target ID allocation in SCG target ID registers is also applicable to SN target IDs.	• 4.5.1 RN SAM memory regions and target types on page 84 • 4.5.3 RN SAM target ID selection on page 89 • 4.5.4 System Cache Groups on page 90 • 4.5.5 SCG HN-F hash algorithm on page 91 • 4.5.6 Configuring SCGs in the RN SAM on page 92
Divided tables showing RN SAM and HN-F SAM memory partition sizes for GIC regions and hashed/non-hashed regions for clarity.	• Table 4-15: RN SAM and HN-F SAM configuration register GIC memory region sizes on page 88 • Table 4-16: RN SAM and HN-F SAM configuration register hashed and non-hashed memory region sizes on page 88
Added more supporting high-level information about the HN-F SAM.	4.6 HN-F SAM on page 98
Created separate sections and more supporting information for the following: • Information about mapping SN targets in the HN-F SAM • Information about HN-F SAM target ID selection • Examples of 3-SN, 5-SN, and 6-SN mode configurations	• 4.6.1 Mapping SN targets in the HN-F SAM on page 98 • 4.6.2 HN-F SAM target ID selection on page 99 • 4.6.4 Examples of 3-SN and 6-SN mode configurations on page 102
Added more supporting high-level information about the HN-I SAM.	4.7 HN-I SAM on page 107

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Change	Location
Created separate sections and more supporting information for: • Information about HN-I SAM address region 0 • Information about configuring HN-I SAM address regions and order regions	• 4.7.1 HN-I SAM address region 0 on page 108 • 4.7.2 Configuring HN-I SAM address regions and order regions on page 109
Updated description of HN-I SAM example configuration to clarify information about the configuration.	4.7.3 HN-I SAM example configuration on page 110
Condensed conceptual overview information about QoS regulators.	4.20.2.1 QoS regulators on page 170

Table C-4: Differences between issue 0100-04 and 0200-05

Change	Location
Added *Downstream Exclusive Cache* (DSC) support to feature list and product revisions list.	• 2.3 Features on page 18 • 2.8 Product revisions on page 26
Added details of `DSC_ENABLE` parameter, which enables DSC functionality, to global configuration parameters.	Table 2-1: Global configuration parameters on page 20
Reversed the ordering of bits in example HN-I SAM programming tables for consistency with the ordering of bits in register references.	• Table 4-28: Example por_hni_sam_addrregion0_cfg register programming on page 112 • Table 4-29: Example por_hni_sam_addrregion1_cfg register programming on page 113 • Table 4-30: Example por_hni_sam_addrregion2_cfg register programming on page 115 • Table 4-31: Example por_hni_sam_addrregion3_cfg register programming on page 116
Added new section describing DSC functionality.	4.10 Downstream Exclusive Cache support on page 118
Corrected the maximum permitted number of source-target MXP pairs which you can use for non-XY routing. Previously the maximum was listed as eight, when it should be 16.	• 4.11.2 Non-XY routing on page 121 • 4.11.2.1 Configuring non-XY routing behavior on page 122 • 5.4.4 Program non-XY routing registers on page 1283
Updated description of support for exclusive accesses in HN-I to clarify that the number of exclusive monitors supported is configuration-dependent.	4.18.2.2 Exclusive accesses in HN-I on page 161
Reversed the ordering of bits in advanced CBusy handling tables for consistency with the ordering of bits in register references.	• Table 4-50: por_hnf_cbusy_limit_ctl register for CBusy thresholds (all requests or read types) on page 164 • Table 4-51: Register for CBusy thresholds (write requests) on page 165 • Table 4-53: por_hnf_cbusy_resp_ctl register for configuring CBusy value on responses on page 167 • Table 4-54: Register for identifying SN groups on page 167 • Table 4-55: por_hnf_cbusy_sn_ctl register for CBusy sampling control on page 167
Added warning describing programming restrictions on POCQ availability and QoS classes.	• 4.20.2.4 HN-F QoS support on page 173 • 6.5.2 QoS class and POCQ resource availability on page 1317
Added r2p0 revision encoding to the periph_id_2 field of the por_cfgm_periph_id_2_periph_id_3 register.	5.3.1.3 por_cfgm_periph_id_2_periph_id_3 on page 209
Added new dsc_en field to the por_info_global register.	5.3.1.43 por_info_global on page 250

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Change	Location
Added the following new fields to the por_hnf_r2_aux_ctl register: • hnf_dsc_wr_noalloc_mode_en • hnf_dsc_accept_dirty_dis • hnf_donotgotosd_in_snpstash	5.3.4.7 por_hnf_r2_aux_ctl on page 393
Updated width of the OPCODE field of the por_hni_errmisc and por_hni_errmisc_ns registers.	• 5.3.5.15 por_hni_errmisc on page 705 • 5.3.5.20 por_hni_errmisc_NS on page 714
Added details of `3'b110` and `3'b111` encodings to the tc_size field of the por_mtu_unit_info register.	5.3.13.4 por_mtu_unit_info on page 1217
Added warnings describing circumstances in which you must program HN-Fs to terminate persistent CMOs.	6.4.4 CMO and PCMO propagation from HN-F to SN-F or SBSX on page 1310
Removed details of device population signals that were no longer applicable.	B Signal descriptions on page 1373
Updated AXI/ACE-Lite master interface signals to add details of DSC related attributes, signal width calculations, and behavior. Affects **AxUSER_M** and **RUSER_M** signals.	B.4.2 AXI/ACE-Lite master interface signals on page 1383
Updated description of how **AxID** signal widths are calculated and formatted in SBSX and MTSX for different configuration scenarios.	B.4.3 SBSX and MTSX AxID signal width and field assignments on page 1388

Table C-5: Differences between issue 0200-05 and 0300-06

Change	Location
Added section describing "MTSX slice channel configuration"	4.9 MTSX slice channel configuration on page 118
Added MTSX slice channel configuration support to feature list and product revisions list.	• 2.3 Features on page 18 • 2.8 Product revisions on page 26

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