Arm Cortex-M23 Processor Datasheet

Datasheet

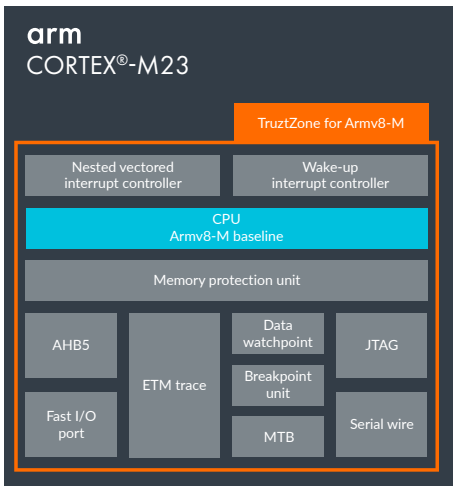

Figure 1: Block diagram of the Cortex-M23 processor

Overview

The Arm Cortex-M23 processor is a very compact, two-stage pipelined processor that supports the Armv8-M baseline architecture. Cortex-M23 with TrustZone is the ideal processor for the most constrained IoT and embedded applications where security is a key requirement.

TrustZone for Armv8-M provides hardware-enforced isolation between the trusted and the untrusted resources on the Cortex-M23 device, while maintaining the efficient exception handling and determinism that have been the hallmark of all Cortex-M processors.

Features

Feature	Description
Architecture	Armv8-M Baseline
Pipeline	2-stage
Bus Interface	AMBA 5 AHB (Von Neumann bus architecture) Optional single-cycle I/O interface
ISA Support	Thumb/Thumb-2 instruction subset
Software Security	Optional Arm TrustZone Technology Optional Security Attribution Unit (SAU) of up to 8 regions Stack limit checking for Secure stack pointers
Memory Protection	Optional Memory Protection Unit (MPU) with up to 16 regions per security state
Interrupts	Non-maskable Interrupt (NMI) and up to 240 physical interrupts with 4 priority levels
Wake-up Interrupt (WIC)	Optional for waking up the processor from state retention power gating or when all clocks are stopped
Sleep Modes	Integrated Wait For Event (WFE) and Wait For Interrupt (WFI) instructions with Sleep On Exit functionality
Enhanced Instructions	Hardware single-cycle (32×32) multiply and fast (32/32) divide option
Debug	Optional JTAG and Serial Wire Debug ports Up to 4 Breakpoints and 4 Watchpoints
Trace	Optional Embedded Trace Macrocell (ETM) and Micro Trace Buffer (MTB)

About the Processor

The Cortex-M23 processor is a low gate count, two-stage, and highly energy efficient processor. It is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor for use in environments where security is an important consideration.

The interfaces in the processor for external access include:

- External AMBA® AHB5 interface
- Debug Access Port (DAP)
- Optional single-cycle I/O port

The processor has optional:

- Arm TrustZone technology, using the Armv8-M Security Extension supporting Secure and Non-secure states
- Secure and Non-secure MPUs which you can configure to protect regions of memory
- Support for ETM and MTB trace

The processor is highly configurable and is intended for a wide range of high-performance, deeply embedded applications that require fast interrupt response features.

Block Diagram

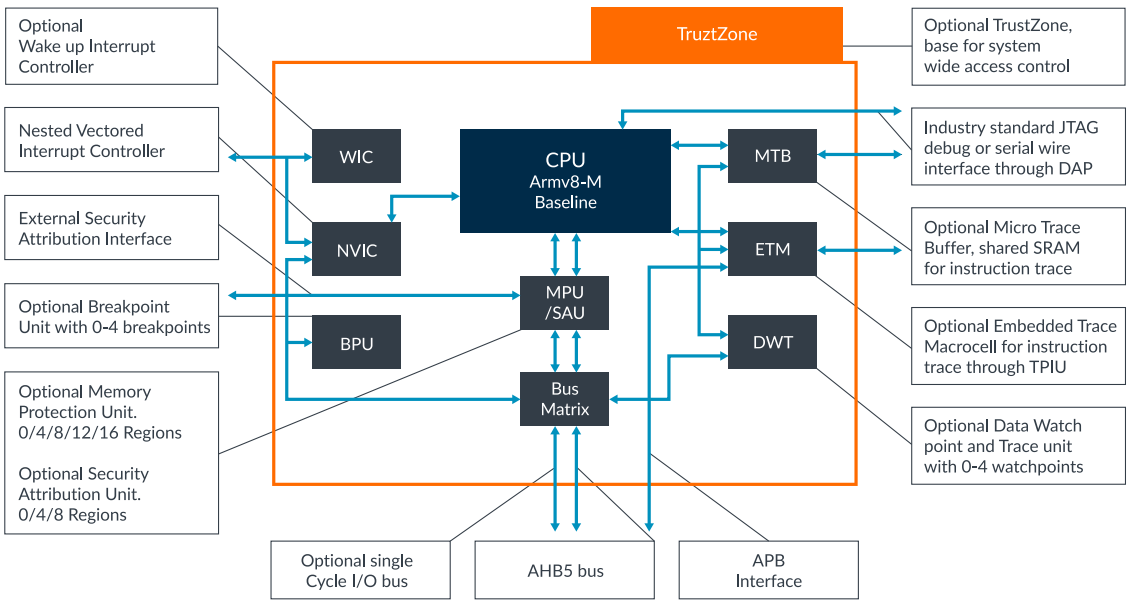

Figure 2: Cortex-M23 processor components

Cortex-M23 Components

Processor Overview

The processor provides:

- Limited dual-issue of common 16-bit instruction pairs
- Single cycle 32×32-bit multiplier
- Integer divide unit with support for operand-dependent early termination
- Support for interrupted continuable load and store multiple operations
- Load and store operations that both support precise bus errors

Security Attribution and Memory Protection

The Cortex-M23 processor supports the Armv8-M Protected Memory System Architecture (PMSA) that provides programmable support for memory protection using software controllable regions.

Memory regions can be programmed to generate faults when accessed inappropriately by unprivileged software reducing the scope of incorrectly written application code. The architecture includes fault status registers to allow an exception handler to determine the source of the fault and to apply corrective action or notify the system.

The Cortex-M23 processor also includes optional support for defining memory regions as Secure or Non-secure, as defined in the Armv8-M Security Extension, and protecting the regions from accesses with an inappropriate level of security.

Nested Vectored Interrupt Controller

The Nested Vectored Interrupt Controller (NVIC) is closely integrated with the core to achieve low-latency interrupt processing.

Functions of the NVIC include:

- External interrupts, configurable from 1 to 240 with four configurable levels of interrupt priority
- Dedicated NMI input
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Optional WIC, providing ultra-low power sleep mode support

Cross Trigger Interface Unit

The optional Cross Trigger Interface (CTI) enables the debug logic, MTB, and ETM to interact with each other and with other CoreSight components.

Embedded Trace Macrocell

- Provides a complete instruction trace solution
- Configurable by an APB slave
- For more information see the Arm CoreSight ETM-M23 Technical Reference Manual

Micro Trace Buffer

- Provides a simple execution trace capability for the processor
- Offers a lower-cost alternative that has certain imitations compared to ETM
- For more information see the Arm CoreSight MTB-M23 Technical Reference Manual

External Interfaces

AMBA 5 AHB interface

- Transactions on the AMBA 5 AHB interface are always marked as non-sequential.
- Processor accesses and debug accesses share the same external interface to external AHB peripherals. The processor accesses take priority over debug accesses.
- Any vendor-specific components can populate this bus.

Single-cycle I/O port

The processor optionally implements a single-cycle I/O port that provides high-speed access to tightly coupled peripherals, such as General-Purpose I/O (GPIO). The port is accessible both by loads and stores, from the processor and from the debugger. You cannot execute code from the I/O port.

Debug Access Port

The processor is implemented with either a low gate count Debug Access Port (DAP) or a full CoreSight DAP.

The low gate count DAP provides a Serial Wire or JTAG debug port. It connects to the processor slave port to provide full system-level debug access.

The full CoreSight DAP system enables the processor to provide full multiprocessor debug with simultaneous halt and release cross-triggering capabilities.

For more information on:

- Serial Wire or JTAG debug port, see the ADI v5.1 version of the ARM® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2.
- CoreSight DAP, see the Arm® CoreSight™ SoC-400 Technical Reference Manual

Cortex-M23 Pipeline

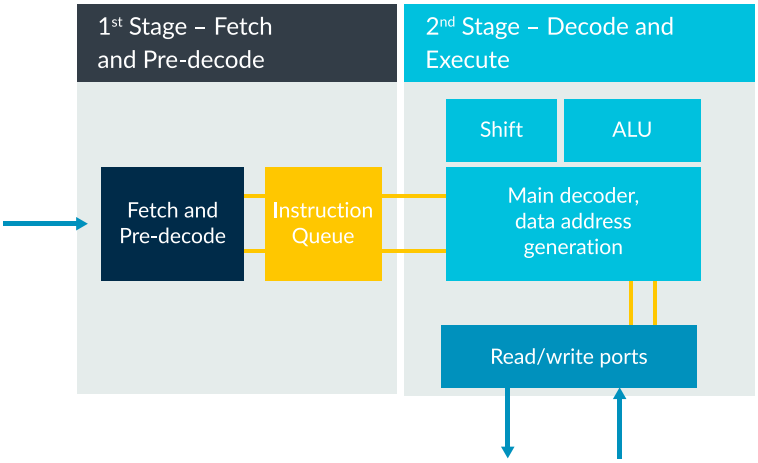

Figure 3: Cortex-M23 processor pipeline

Corstone Reference Design

Corstone Reference Designs provide an ideal starting point for any System on Chip (SoC) design, with the lowest risk and development cost. It includes various system IP components and a reference design integrating the processor, security and system IP, as well as having a range of software and development tools available.

Corstone features include:

- Implementation of an Arm-defined subsystem architecture
- Integration of the main components
- Extensively verified
- Broad software roadmap
- Build your SoC on top of it
- Configurable and modifiable
- Tailor it to specific needs
- PSA-certification ready
- Silicon-proven

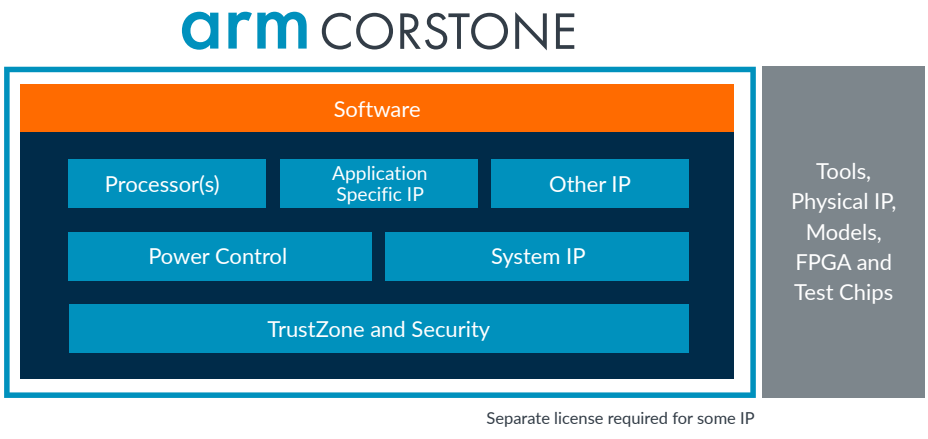

Figure 4: Corstone reference design diagram

Processor Configuration Options

The Cortex-M23 processor has configurable options that you can set during the implementation and integration stages to match your functional requirements.

Feature	Options
TrustZone	No TrustZone for Armv8-M
	TrustZone for Armv8-M Security Extension
Non-secure MPUs	0 region, 4 regions, 8 regions, 12 regions, or 16 regions
Secure MPUs	0 region, 4 regions, 8 regions, 12 regions, or 16 regions when TrustZone is included
SAU	0 region, 4 regions, or 8 regions when TrustZone is included
SysTick timers	✣ If the Security Extension is not implemented, can be present or absent. ✣ If the Security Extension is implemented, 0, 1, or 2 SysTick timers can be present. If only one SysTick timer is present, then software can configure whether this SysTick is Secure or Non-secure.
Vector Table Offset Register (VTOR)	✣ If the Security Extension is not implemented, can be present or absent. ✣ If the Security Extension is implemented, can be either present or absent for both security states.
Reset all registers	Present or absent
Multiplier	Fast (one cycle) or slow (32 cycles)
Divider	Fast (17 cycles) or slow (34 cycles)
Interrupts	External interrupts 1-240
Instruction fetch width	16-bit or 32-bit
Single-cycle I/O port	Present or absent
Architectural clock gating present	When set, architectural clock gating cells are instantiated
Data endianness	Little-endian or byte-invariant big-endian
Halting debug support	Present or absent
Wake-up interrupt controller	Supported or not supported
Number of breakpoint comparators	0, 1, 2, 3, 4
Number of watchpoint comparators	0, 1, 2, 3, 4
CTI	Present or absent
MTB	Present or absent
ETM	Present or absent
JTAG SW debug protocol	Selects between JTAG or Serial-Wire interfaces for the DAP
Multi-drop support for Serial Wire	Present or absent
Slave port support for AHB DAP	When set, includes slave port support for any AHB DAP implementation. Otherwise, supports only the low area DAP.

Instruction Set

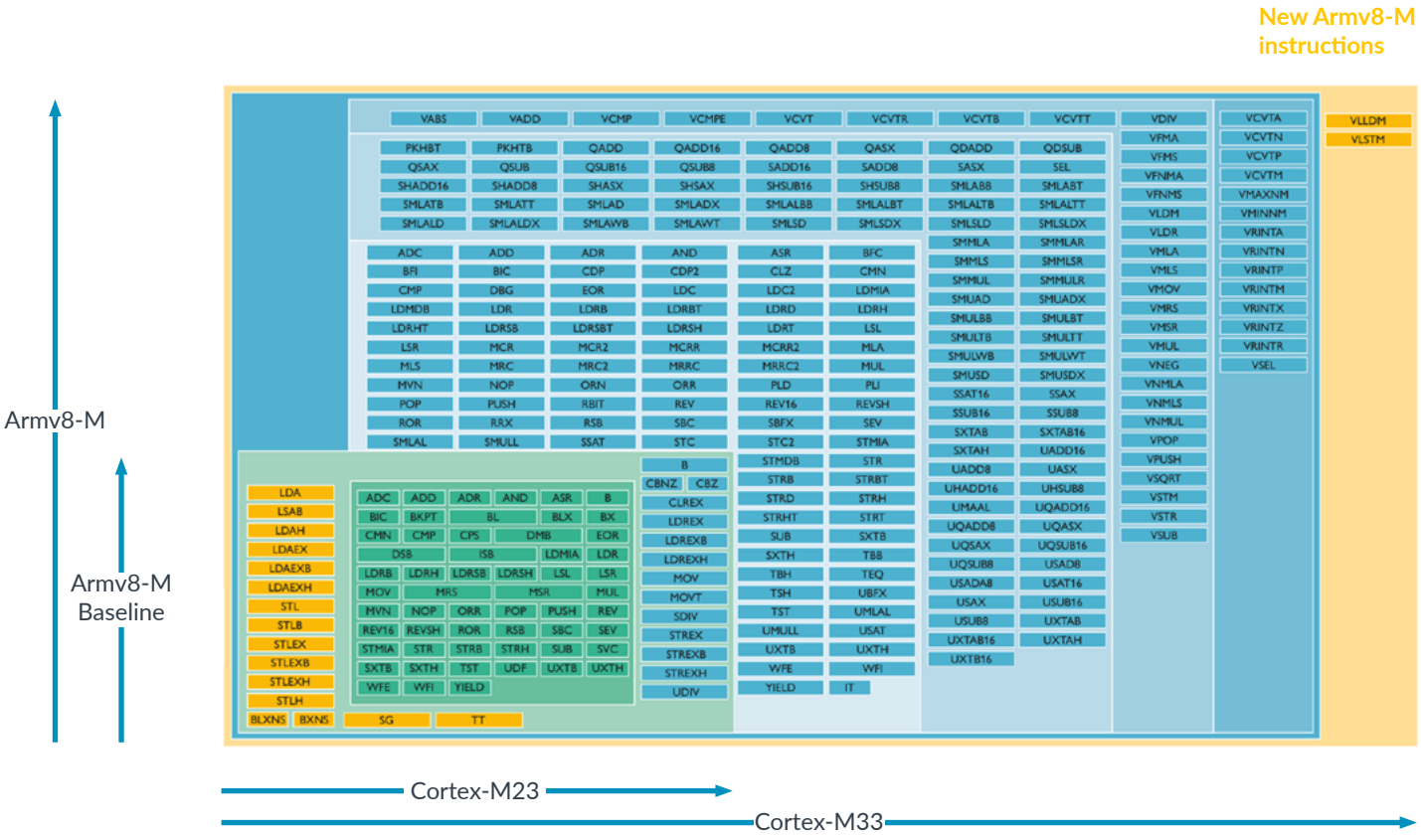

Figure 5: Instruction set

Power, Performance and Area

DMIPS	CoreMark/MHz
0.98	2.64

Configuration	40LP Arm SC9 RVT C50 SS 0.99V, -40°C		28HT Arm SC7MC PP140Z SVT HD C40 SSG 0.81V 0°C	
	Area mm^2	Power µW/MHz	Area mm^2	Power µW/MHz
Minimum Configuration*	0.009	3.86	0.004	2.26
Feature Rich with TrustZone**	0.034	8.66	0.014	5.07

Max Freq	40LP Arm 40LP SC12 RVT C50 SS 0.99V, -40°C
Feature Rich Configuration with TrustZone**	155MHz

*SECEXT 0; CPIF 0; MPU_NS 0; MPU_S 0; SAU 0; NUMIRQ 1; IRQLVL 3; IRQLATENCY 4294967295; IRQDIS 0; DBGLVL 0; ETM 0; MTB 0; MTBAWIDTH 0; WIC 0; WICLINES 0; CTI 0; RAR 0;

**SECEXT 1; CPIF 0; MPU_NS 8; MPU_S 8; SAU 0; NUMIRQ 32; IRQLVL 3; IRQLATENCY 4294967295; IRQDIS 0; DBGLVL 2; ETM 1; MTB 0; MTBAWIDTH 0; WIC 1; WICLINES 35; CTI 0; RAR 0;
;

Additional Technical documents

1. Cortex-M23 Technical Reference Manual - TRM

2. Cortex-M23 Integration and Implementation Manual – available as part of the Bill of Materials

3. Armv8-M Architecture Reference Manual - ARM

4. CoreSight ETM-M23 Technical Reference Manual - ETM

5. CoreSight MTB-M23 Technical Reference Manual - MTB

Glossary of Terms

AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CTI	Cross Trigger Interface
ETM	Embedded Trace Macrocell
IDAU	Implementation Defined Attribution Unit
JTAG	Joint Test Action Group
MPU	Memory Protection Unit
MTB	Micro Trace Buffer
NMI	Non-maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
PMSA	Protected Memory System Architecture
PSA	Platform Security Architecture
SAU	Security Attribution Unit
WFE	Wait for event
WFI	Wait for interrupt
WIC	Wake-up Interrupt Controller

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