ACPI for CoreSight™ Performance Monitoring Unit Architecture 1.0

Platform Design Document

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About this document

Terms and abbreviations

Term	Meaning
ACPI	Advanced Configuration and Power Interface specification
GSIV	Global System Interrupt Vector
HID	ACPI Hardware Identifier
MSI	Message Signaled Interrupt
SMMU	Arm System Memory Management Unit
UID	ACPI Unique Identifier

References

This section lists publications by Arm and by third parties.

See Arm Developer (http://developer.arm.com) for access to Arm documentation.

[1] *Arm® CoreSight™ Performance Monitoring Unit Architecture, Arm IHI 0091*. Arm Limited.

[2] *Advanced Configuration and Power Interface Specification*. UEFI Forum.

[3] *Arm® Architecture Reference Manual ARMv8, for the ARMv8-A architecture profile, Arm DDI 0487*. Arm Limited.

Feedback

Arm welcomes feedback on its documentation.

If you have comments on the content of this manual, send an e-mail to errata@arm.com. Give:

- The title (ACPI for CoreSight™ Performance Monitoring Unit Architecture).
- The document ID and version (DEN0117 1.0).
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Arm also welcomes general suggestions for additions and improvements.

1 Introduction

This document specifies the ACPI description of Performance Monitoring Unit (PMU) support in an Arm-based system that consists of components that implement the CoreSight Performance Monitoring Unit (PMU) architecture that is described in [1].

2 The ACPI Arm Performance Monitoring Unit table

The ACPI Arm Performance Monitoring Unit (APMT) table describes the properties of PMU support implemented by components in an Arm-based system, where the PMU block design conforms to the CoreSight PMU architecture [1]. The APMT table is intended for an OS driver or equivalent OS-based entity that in turn provides system performance monitoring interfaces to its clients.

The APMT table does not cover architectural PMU support in the Arm PEs, or in system components such as the SMMU. The APMT table is strictly intended for Arm IPs as well as vendor-specific IPs that incorporate a PMU block that is based on the CoreSight PMU architecture.

The table format is described in Table 3.

Table 3: The APMT table

Field	Byte length	Byte offset	Description
Header			Standard ACPI format for header.
Signature	4	0	‘APMT’, Arm Performance Monitoring Unit table.
Length	4	4	Length of this table in bytes.
Revision	1	8	Must be 0 for version 1.0 of this specification.
Checksum	1	9	The entire table must sum to zero.
OEM ID	6	10	OEM ID.
OEM Table ID	8	16	The table ID is the manufacture model ID.
OEM Revision	4	24	OEM revision of the APMT table for the supplied OEM Table ID.
Creator ID	4	28	The vendor ID of the utility that created the table.
Creator Revision	4	32	The revision of the utility that created the table.
Body			
Array of PMU node structures	–	36	An array of PMU node structures that describes PMUs in the system.

2.1 Arm PMU node structure

Table 4: APMT node

Field	Byte length	Byte offset	Description
Length	2	0	Length of this APMT node structure in bytes.
Node flags	1	2	See Table 5.
Node type	1	3	The component that this PMU is associated with. Node types are defined in Section 2.1.3.
Identifier	4	4	Unique identifier for this node.
Node Instance primary	8	8	Node instances are specific to the node type. Section 2.1.3 provides details on node instances.

Field	Byte length	Byte offset	Description
Node Instance secondary	4	16	Node instances are specific to the node type. Section 2.1.3 provides details on node instances.
Base address 0	8	20	Base address of Page 0 of the PMU. If the PMU is a single-page implementation, then this field also serves as the base address of Page 1 registers of the PMU. PMU pages and registers are described in [1].
Base address 1	8	28	Base address of Page 1 of the PMU, if the PMU implements the dual-page extension described in [1].
Overflow interrupt	4	36	Identifier for the overflow interrupt if the PMU supports event overflows. A value of zero indicates that the overflow interrupt is not implemented by this PMU. For wired interrupts, this field represents the GSIV of the interrupt.
Reserved1	4	40	Reserved, must be zero.
Overflow interrupt flags	4	44	See Table 6.
Processor affinity	4	48	Processor affinity for this PMU. This field must match the ACPI Processor ID of the PPTT Type 0 structure that represents the processor or processor container that this PMU is associated with.
Implementation ID	4	52	This field is used for specifying the identity of the implementer of this PMU and the implementer-assigned product code for it. This field has the same format as the PMIIDR register [1]. This field must be set to 0 and ignored if the PMIIDR or PMPIDR register is present in this PMU implementation.

2.1.1 Node Flags

Table 5: Node flags

Field	Bit length	Bit offset	Description
Dual-page extension	1	0	• 1b if the PMU supports the dual-page mode. • 0b if the PMU supports single-page mode.

Field	Bit length	Bit offset	Description
Processor affinity type	1	1	• 1b to indicate that the Processor affinity field specifies a processor container. • 0b to indicate that the Processor affinity field specifies a processor.
64-bit single copy atomicity supported	1	2	• 1b if single copy atomicity is supported for accesses to this PMU. • 0b if single copy atomicity is not supported for accesses to this PMU.
Reserved	5	3	Must be zero.

2.1.2 Interrupt Flags

Table 6: Interrupt flags

Field	Bit length	Bit offset	Description
Interrupt mode	1	0	• 1 if interrupt is edge-triggered • 0 if interrupt is level-triggered Other values are reserved.
Interrupt type	2	1	• 00b if this is a wired interrupt. Other values are reserved.
Reserved	29	3	Must be zero.

2.1.3 Node type

Arm CoreSight Architecture PMUs provide standard events and event masks for specific components. The Node type field in Section 2.1 specifies the SoC component that this PMU is associated with.

The OS should use this information to understand what standard events are supported by a given PMU. For more details on standard events and event masks, please see [1].

Table 7: Node types

Node type value	Description	Primary Node instance field	Secondary Node instance field
0x00	Memory controller	Must be set to the proximity domain of the ACPI SRAT table entry that describes the memory ranges that belong to the memory controller that this PMU is associated with.	Must be set to 0.

Node type value	Description	Primary Node instance field	Secondary Node instance field
0x01	SMMU	Must be set to the Identifier field of the IORT table node that describes the SMMU or unit within an SMMU that this PMU is associated with.	Must be set to 0.
0x02	PCIe root complex	This field must be set to the Identifier field of the IORT table node that describes the root complex that this PMU is associated with.	Must be set to 0.
0x03	ACPI device	Specifies the _HID of the device object in DSDT that describes the component that this PMU is associated with.	Specifies the _UID of the component.
0x04	CPU cache	Must be set to 0.	Must be set to the Cache ID field of the Type 1 (Cache) structure in the ACPI PPTT table, that describes this cache. This specification requires that the PPTT table must be based on ACPI specification versions 6.4 or higher.
0x05-0xFF	Reserved for future use by this specification.		

2.2 ACPI Identifier for CoreSight PMU Architecture PMU

If a PMU implementation based on the CoreSight PMU Architecture specification has properties in addition to the canonical properties described in the APMT PMU node, then those properties might be described by means of an ACPI device object in the DSDT.

For example, the PMU device object might be used to express power state dependencies of the PMU.

This specification reserves an ACPI _HID value of “ARMHE001” for the CoreSight PMU architecture PMU. Device objects carrying properties of a PMU based on the CoreSight PMU Architecture specification, must include a _HID object that must be set to “ARMHE001”. Additionally, the device object must carry a _UID value that must match the Identifier field of the APMT PMU node that describes the canonical properties of the PMU. The APMT PMU node is defined in Section 2.1.