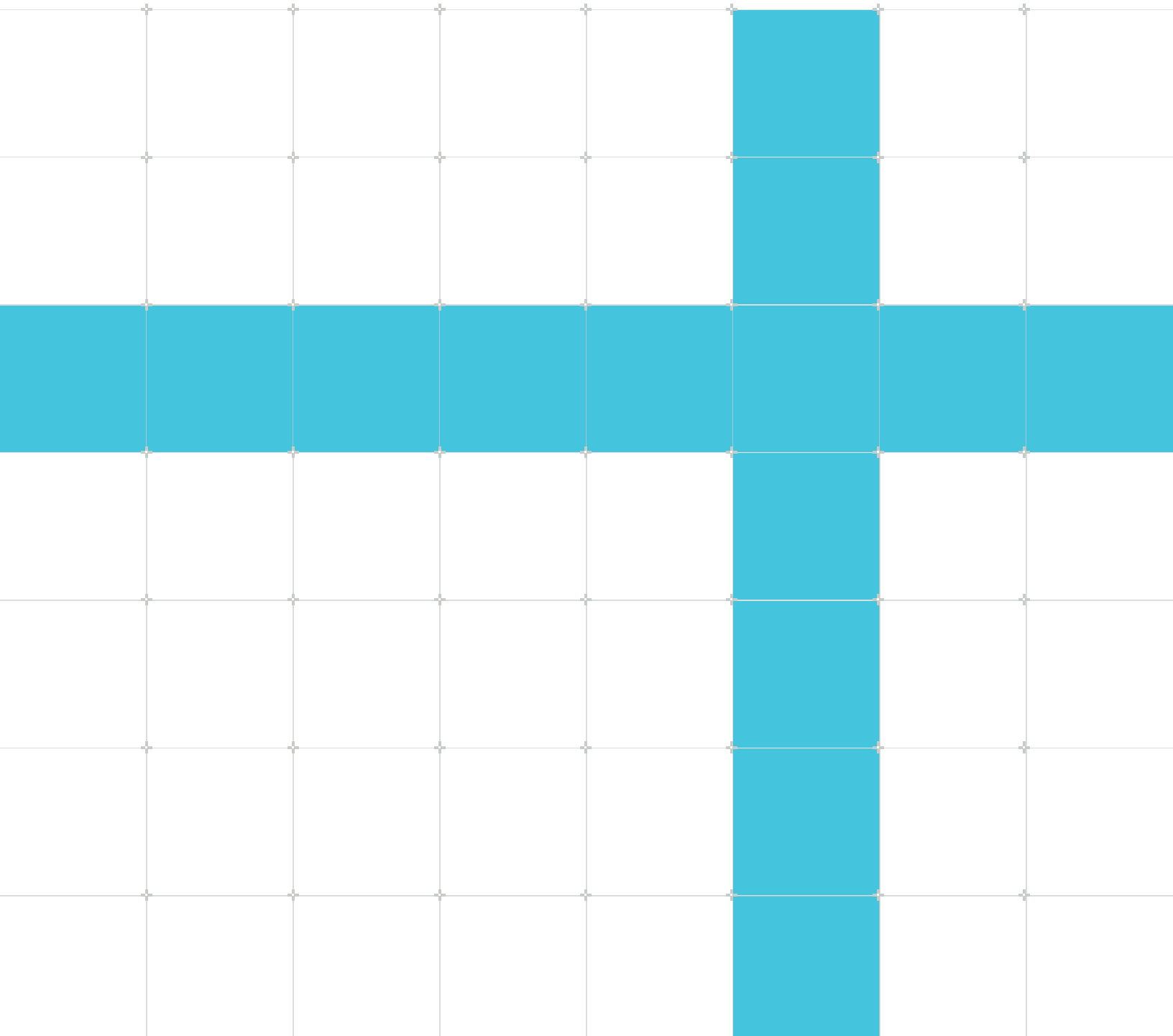
# Morello Platform Model

Version 2.0

# Reference Guide



**Issue 00**
102225_0200_00_en



# Morello Platform Model

## Reference Guide



## Release Information

### Document history

| Issue | Date | Confidentiality | Change |
|---|---|---|---|
| 0100-00 | 29 October 2020 | Non-Confidential | First release |
| 0101-00 | 11 December 2020 | Non-Confidential | Update for Morello Platform Model version 1.1 |
| 0102-00 | 26 February 2021 | Non-Confidential | Update for Morello Platform Model version 1.2 |
| 0103-00 | 14 May 2021 | Non-Confidential | Update for Morello Platform Model version 1.3 |
| 0200-00 | 6 October 2021 | Non-Confidential | Update for Morello Platform Model version 2.0 |

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(LES-PRE-20349)

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# Contents

# 1 Introduction

## 1.1 Conventions

The following subsections describe conventions used in Arm documents.

### Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

### Typographic conventions

| Convention | Use |
|---|---|
| *italic* | Introduces citations. |
| **bold** | Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate. |
| `monospace` | Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code. |
| **`monospace bold`** | Denotes language keywords when used outside example code. |
| `monospace underline` | Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. |
| `<and>` | Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>` |
| SMALL CAPITALS | Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE. |
|   | This represents a recommendation which, if not followed, might lead to system failure or damage. |
|   | This represents a requirement for the system that, if not followed, might result in system failure or damage. |
|   | This represents a requirement for the system that, if not followed, will result in system failure or damage. |
|   | This represents an important piece of information that needs your attention. |
|   | This represents a useful tip that might make it easier, better or faster to perform a task. |

| Convention | Use |
|---|---|
| Remember | This is a reminder of something important that relates to the information you are reading. |

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If you have comments on content then send an e-mail to errata@arm.com. Give:

- The title Morello Platform Model Reference Guide.
- The number 102225_0200_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

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Note

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## 1.3 Other information

See the Arm® website for other relevant information.

- Arm® Developer.
- Arm® Documentation.
- Technical Support.
- Arm® Glossary.

# 2 Introduction to the Morello Platform Model

This chapter contains a high-level description of the Morello Platform Model, and gives links to further information.

## 2.1 About the Morello Platform Model

The Morello Platform Model is a software model of the Morello System on Chip (SoC) hardware platform.

It is freely available for download from the Arm® Developer website, does not require a license, and runs on Linux host machines only.

The Morello Platform Model is a Fixed Virtual Platform (FVP). An FVP is a pre-built model that consists of a hierarchy of model components connected together to form a system. Although the composition of an FVP is fixed, you can configure its behavior using parameters. You can also load plug-in libraries to provide extra functionality.

FVPs enable applications and operating systems to be written and debugged without the need for real hardware. They work by translating Arm® instructions into the instruction set of the host dynamically and use optimization techniques to improve performance. So, while they are functionally accurate, they do not provide accurate timing information or cycle counts.

FVPs have several benefits over the hardware they model:

**Early availability**
: FVPs are available much earlier than hardware, which enables software development ahead of hardware availability.

**Software compatibility**
: As the same software stack runs on both the model and the hardware, you can use the same toolchain to build for both targets.

**Configurable**
: FVPs can be easily customized by using parameters to test different configurations. To see the available parameters, run the FVP with the `--list-params` option.

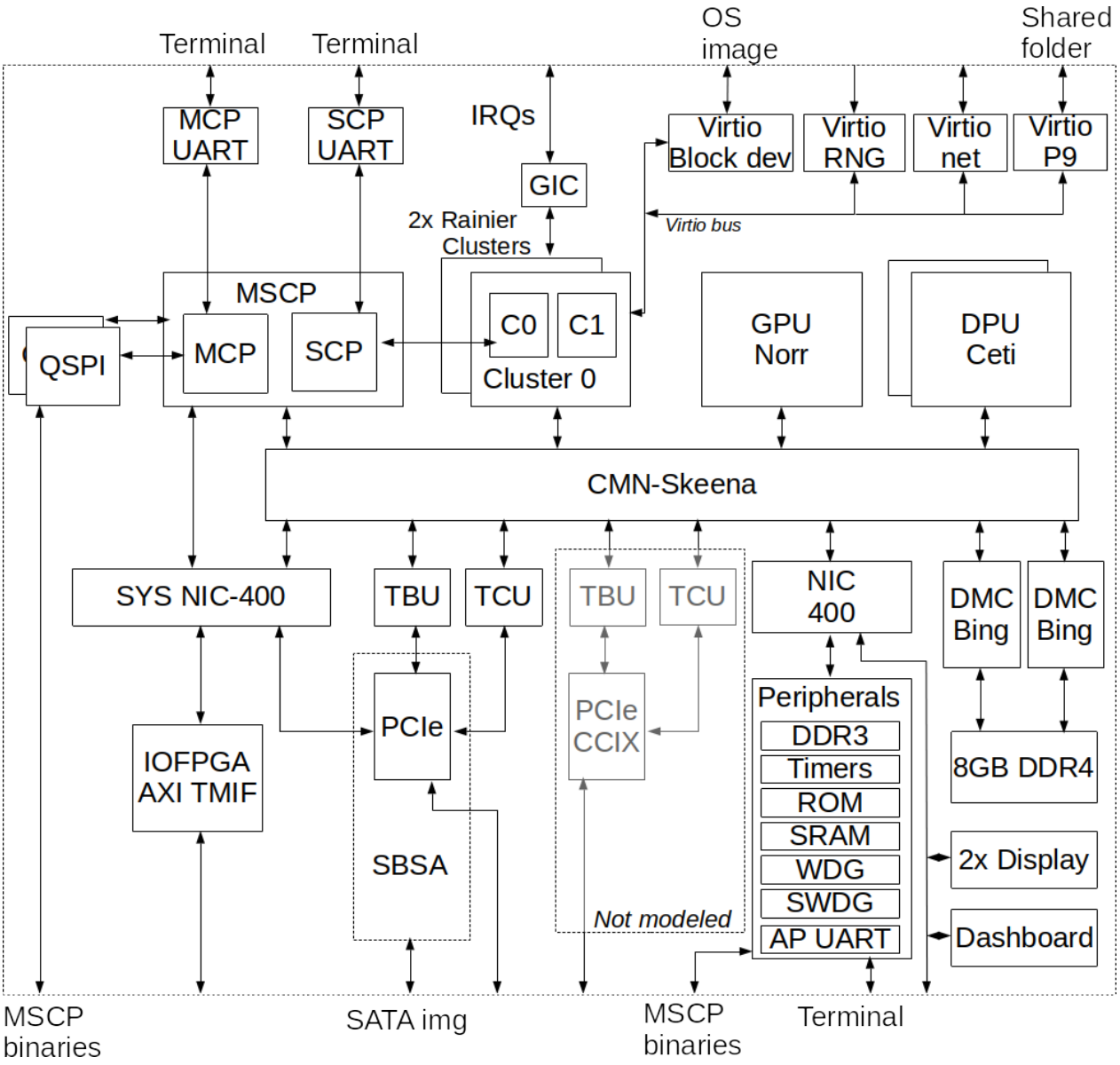
**Debuggable**
: The Morello Platform Model supports the CADI interface which enables debuggers to connect to it and debug it. You can use Arm Debugger in the Arm® Development Studio Morello Edition to work with the Morello Platform Model.

**Trace support**
: The Morello Platform Model supports Model Trace Interface (MTI), which enables you to use plug-ins to output trace information from the FVP. The Morello Platform Model package includes several pre-built trace plug-ins.

## 2.2 High-level block diagram

This simplified block diagram shows the SoC and board peripherals.

**Figure 2-1: Morello Platform Model system block diagram**



## 2.3 Host prerequisites

The Morello Platform Model supports the following host operating systems and compilers.

**Operating system**

The FVP requires a Linux x86-64 host. It has been tested with Ubuntu 18.04 but should also work with later versions.

The following GCC-6.4 compatible libraries must be installed on the host:

- `/lib64/ld-linux-x86-64.so.2`
- `libatomic.so.1`
- `libc.so.6`
- `libdbus-1.so.3`
- `libdl.so.2`
- `libgcc_s.so.1`
- `libgcrypt.so.20`
- `libgpg-error.so.0`
- `liblz4.so.1`
- `liblzma.so.5`
- `libm.so.6`
- `libpthread.so.0`
- `librt.so.1`
- `libstdc++.so.6`
- `libsystemd.so.0`
- `linux-vdso.so.1`

**Other requirements**

- A shell compatible with `sh`, such as `bash` or `tcsh`. If you want to change terminals use the `terminal_command` parameter to select a different console program.
- If you want to use the host GPU for rendering pixels, you must install the Mali™ OpenGL ES emulator from OpenGL ES Emulator Downloads. Follow the steps described in the documentation included in the download package.

## 2.4 Additional reading

This section lists other publications and websites from Arm that are relevant to the Morello Platform Model.

- To learn more about the Morello program and architecture, see Arm Morello Program.

- To learn more about the Open Source Software targeting this FVP, see Morello Project.
- A preliminary Technical Reference Manual (TRM) for this FVP is available at Arm® Morello System Development Platform (SDP) Preliminary Technical Reference Manual.
- To learn about software development for Morello using Arm Development Studio, read Arm Development Studio Morello Edition Getting Started Guide and Arm Development Studio Morello Edition User Guide.
- To learn more about Fast Models, see Fast Models on Arm Developer.

# 3 Get started

This chapter describes how to download and install the Morello Platform Model package, and verify the installation.

## 3.1 Install the package

The Morello Platform Model package is installed using a command-line installer.

### About this task

Follow these steps to download and install the package:

### Procedure

1. Download the package from the Arm Ecosystem FVPs page.
2. Uncompress the tarball:
   ```
   tar -xzf FVP_Morello_x.xx_xxx.tgz
   ```
   where `x` indicates the model version number. For example, `FVP_Morello_0.10_310.tgz`.
3. Run the installation shell script:
   ```
   ./FVP_Morello.sh
   ```
4. Read and agree to the terms and conditions and select the directory to install to.
5. When installation has finished, the model, called `FVP_Morello`, can be found in `<install_directory>/FVP_Morello/models/Linux64_GCC-x.x/`.
   where `x` indicates the GCC version number. For example, `/Linux64_GCC-6.4`.

### Results

To uninstall the package, remove the installation folder.

## 3.2 What is in the package?

The package contains the FVP binary, libraries that it uses, documentation, and some plug-in libraries.

The contents of the Morello Platform Model installation are:

```
FVP_Morello/
├── doc
│   ├── Morello_FVP_ReleaseNotes.txt
│   └── morello_platform_model_rg_102225_0200_00_en.pdf
├── fmtplib
│   ├── libstdc++.so.6
│   ├── libstdc++.so.6-gdb.py
│   └── LICENSE
├── install_history
```

```
├── license_terms
│   ├── license_agreement.txt
│   ├── redistributables.txt
│   ├── supplementary_terms.txt
│   └── third_party_licenses.txt
├── models
│   └── Linux64_GCC-6.4
│       ├── checkerrcode.ini
│       ├── cmn600_morello_skeena_topology.yml
│       ├── FVP_Morello
│       ├── FVP_Morello.so
│       ├── libarmctmodel.so
│       ├── libMAXCOREInitSimulationEngine.3.so
│       ├── libnomali.so
│       ├── libReconciler.so
│       ├── libSDL2-2.0.so.0.10.0
│       ├── settings.ini
│       └── Sidechannel.so
├── plugins
│   └── Linux64_GCC-6.4
│       ├── ArchMsgTrace.so
│       ├── GDBRemoteConnection.so
│       ├── GenericCounter.so
│       ├── GenericTrace.so
│       ├── ListTraceSources.so
│       ├── MTS.so
│       ├── TarmacText.so
│       ├── TarmacTrace.so
│       └── ToggleMTIPlugin.so
└── sw
    └── ARM_Fast_Models_FVP_Morello
        └── rev
9 directories, 31 files
```

**doc**

Contains release notes and a PDF version of the Morello Platform Model Reference Guide (this document).

**fmtplib**

Contains GCC runtime libraries to allow you to run the FVP on older Linux distributions.


The `runtime.sh` script that installed these libraries in previous releases is no longer required. The model now searches for the libraries in the `fmtplib` directory.

**license-terms**

Contains the copyright and license information for third-party software, and the standard FVP end-user license agreement.

**models**

Contains the GCC build of the Morello Platform Model, `FVP_Morello`, and the libraries that it requires.

**plugins**

Plug-ins are libraries that provide extra functionality for the FVP, for instance trace output. To load a plug-in, specify it when launching the FVP using the `--plugin` command-line option, or use the `FM_TRACE_PLUGINS` environment variable.

The following plug-ins are included in the Morello Platform Model package. Most of them are documented in the Fast Models Reference Manual, see Plug-ins for Fast Models for details.

**ArchMsgTrace**

Prints warnings and error messages to stdout or to a file when the core executes code that is unsafe or not recommended.

**GDBRemoteConnection**

Allows the model to be debugged using GDB.

**GenericCounter**

At the end of the simulation prints to stdout the number of occurrences of a specific trace source.

**GenericTrace**

Prints trace information, specified using a comma-separated list of trace sources, to `stdout` or to a file.

**ListTraceSources**

Displays a list of the trace sources that the model provides, without running the model.

**MTS**

Used by Arm® Debugger in Arm® Development Studio Morello Edition to report instructions and exceptions that were captured during the simulation.

**TarmacText**

Extracts the architectural execution trace, known as Tarmac trace, of the processor. This might include instructions, program flow, or memory accesses. TarmacText extracts the trace in a textual form and saves it in a file.

**TarmacTrace**

Prints Tarmac trace information to stdout or to a file. Parameters control the amount and type of information that is traced. The Tarmac trace file format is documented in the Fast Models Reference Manual, see TarmacTrace file format. Some changes to the file format have been made for Morello. For details, see 4.4 Morello-specific changes to tarmac trace on page 22.

**ToggleMTIPlugin**

Toggles trace generation on or off during the simulation. See 4.5 ToggleMTIPlugin on page 24 for details.

## 3.3 Verify the installation

Run the FVP manually from the command line to verify that it has installed correctly on the host machine.

### About this task


Note

You would not typically launch the Morello Platform Model in this way. For most expected use cases, the FVP requires the Open Source Software stack and is launched using a script to simplify the process, see 3.4 What software is available? on page 15 for details.

### Procedure

1. In the terminal, change to the directory where you installed the Morello Platform Model. For example: `cd ~/FVP_Morello/models/Linux64_GCC-6.4`
2. Launch the Morello Platform Model with the `--list-params` option, for example: `./FVP_Morello --list-params`.
   The `--list-params` option prints a list of model parameters to the terminal. For a description of all the available command-line options, see 4.2 Command-line options on page 17.

## 3.4 What software is available?

The Morello Platform Model is typically used with a compatible Open Source Software (OSS) stack.

- Arm provides an integrated OSS stack for the Morello platform with scripts to build and run it.
- Arm Development Studio Morello Edition provides comprehensive support for all software development projects on the Morello platform. It also provides a selection of examples to help you get started with the Morello platform.
- An LLVM compiler with Morello support is available, with Morello code examples included.

To find out more about the OSS stack configurations supported on the model and the Morello-aware LLVM toolchain, see the Morello software page.


Note

For technical support, see the Morello forum on Arm Community.

# 4 Reference information

This chapter provides reference information for the Morello Platform Model including differences between the model implementation and the Morello specification, command-line options, and a list of model component instances.


Note

- For more information about the Morello program see the Arm Morello Program page.
- For the Morello Platform memory maps and interrupt maps, see Chapter 4 Programmers model, in the Arm® Morello System Development Platform (SDP) Preliminary Technical Reference Manual.
- For information about additional devices available in the Morello Platform Model, see 4.1 Morello Platform Model notes and limitations on page 16.

## 4.1 Morello Platform Model notes and limitations

The model is implemented according to the Morello TRM with some exceptions.

- Dual DPU Ceti has been integrated into the model.
- PCIe CCIX has not been integrated into the model.

**Trace**

- Several Morello-specific trace sources have been added, and some extra fields have been added to existing trace sources. To display the list of available trace sources and their fields, use the `ListTraceSources` plug-in as described in the Fast Models Reference Manual.
- Some changes have been made to the TarmacTrace format to represent Morello-specific state and events. These are documented in 4.4 Morello-specific changes to tarmac trace on page 22.
- Some Morello-specific states are not fully captured in the trace:
  - The clearing of capability tags performed by non-capability stores is not reflected in the trace.
  - Executive/Restricted (both transitions and the current state) are not directly reflected in the trace, although can be deduced from the traced value of PCC.
  - Writes to `x` registers are sometimes inconsistently traced as writes to the corresponding `c` register. When they are traced as writes to the `x` register, zero-extension into the upper bits of the capability is implicit. The `OLD_VALUE` field might be incorrect between writes to the same `x` and `c` register.
  - The squashing of mutable permissions and the tag of a capability loaded from memory using a capability without `LoadCap` or `MutableLoad` permissions is not reflected in the trace. Instead, the traced value can

either include or exclude the squashing, controlled by the cluster parameter `trace_squashed_mutable_perms_and_tag_in_loads`.
These issues are expected to be addressed in a future release of the model.

### Performance

The performance of model version 1.x when using Morello features, in particular memory accesses, was reduced. Model version 2.0 is 2x faster than previous versions by implementing Direct Memory Interface (DMI) in the Rainier CPU model.

### Rainier IMPLEMENTATION DEFINED registers and behavior

The Rainier CPU model supports the Morello-specific `IMPLEMENTATION DEFINED` Performance Monitor Unit (PMU) events. For details about these events, see the Morello prototype architecture specifications.

### Additional devices

The following devices are present in the Morello Platform Model but are not present in the hardware:

**Table 4-1: Additional devices in the model**

| Device | Memory range | IRQ |
|---|---|---|
| `virtioblockdevice` | `0x1C17_0000` to `0x1C17_FFFF` | 96 |
| `virtio_net` | `0x1C18_0000` to `0x1C18_FFFF` | 102 |
| `virtio_rng` | `0x1C19_0000` to `0x1C19_FFFF` | 101 |
| `virtio_p9` [1] | `0x1C1A_0000` to `0x1C1A_FFFF` | 103 |

## 4.2 Command-line options

Use these options to configure the FVP when launching it from the command line. Each table groups together related options. For a listing of these options with brief descriptions, run the model with `--help`.

**Table 4-2: CADI-related options**

| Short form | Long form | Description |
|---|---|---|
| `-S` | `--cadi-server` | Start a CADI server. This option allows a CADI-enabled debugger to connect to targets in the simulation. To shut down the server, return to the command window that you used to start the model and press **Ctrl+C**. |
| `-R` | `--run` | Run the simulation immediately after the CADI server is started.<br><br>Use this option with `--cadi-server`.<br><br>The default is to wait until the debugger has connected before running the simulation. |

[1] The `virtio_p9` device allows you to share a folder between the host and the FVP. See the Morello Platform Model release notes for instructions on building a guest OS that enables the `virtio_p9` device. For further instructions on how to configure and use it, see VirtioP9Device in the Fast Models Reference Manual.

| Short form | Long form | Description |
|---|---|---|
| `-L` | `--cadi-log` | Log all CADI function calls made during the simulation into XML files.<br><br>One log file is created for each CADI target. The log files are created in the current working directory.<br><br>The filename format is:<br><br>`CADIlog-<TargetInstanceName>-<ProcessID>.xml` |
| `-p` | `--print-port-number` | Print the port number on which the CADI server is listening.<br><br>**Tip:**<br>This option can be useful if you need to specify the port number when you connect a client to the debug server. |

**Table 4-3: Output-related options**

| Short form | Long form | Description |
|---|---|---|
| | `--list-instances` | Print a list of model instances to standard output, then exit the simulation.<br><br>Use this option to help identify the correct syntax for configuration files, and to find out what instances the target supplies. |
| `-l` | `--list-params` | Print a list of model parameters to standard output, then exit the simulation.<br><br>**Tip:**<br>If you load a plug-in, this option also lists the plug-in parameters. |
| | `--list-regs` | Print model register information to standard output, then exit the simulation. |
| | `--check-regs` | Same as `--list-regs` but with extra consistency checks on the CADI register API. |
| | `--list-memory` | Print memory information to standard output, then exit the simulation. |
| `-o` | `--output` *filename* | Redirect output from the `--list-instances`, `--list-memory`, `--list-params`, and `--list-regs` options to a file.<br><br>If this option is used with `--list-params`, the contents of the output file are formatted correctly for use as input by the `--config-file` option. |
| | `--dump` *file@addr,size* | Dump a section of memory to a file at model shutdown. This option can be specified multiple times. The full syntax is:<br><br>`--dump [instance=]file@[memspace:]address,size`<br><br>**Tip:**<br>To see the list of instances and memory spaces, use the `--list-memory` option. |
| | `--data` *file@addr* | Write raw data contained in *file* to the specified address. This option can be specified multiple times. The full syntax is:<br><br>`--data [instance=]file@[memspace:]address` |
| | `--log` *filename* | Log all SystemC reports into *filename*. |

| Short form | Long form | Description |
|---|---|---|
| | `--stat` | Print the following performance statistics on simulation exit:<br>**Simulated time**<br>An estimate of the time that the workload would have taken on the modeled hardware.<br>**User time**<br>Time in wall clock seconds that the host CPU spent running in user mode.<br>**System time**<br>Time in wall clock seconds that the host CPU spent running in system mode.<br>**Wall time**<br>Time in wall clock seconds between the simulation starting and stopping.<br>**Performance index**<br>An estimate of the accuracy of the simulation performance. This value is Simulated time divided by Wall time. |
| `-P` | `--prefix` | Prefix each line of semihosting output with the name of the target instance. |
| `-h` | `--help` | Print the help message and exit. |
| | `--version` | Print version information. |
| `-q` | `--quiet` | Suppress informational output. |

**Table 4-4: Run control options**

| Short form | Long form | Description |
|---|---|---|
| | `--cpulimit` *n* | Maximum number of wall-clock seconds for the simulation process to be active. This value excludes simulation startup and shutdown.<br><br>This option is ignored if a debug server is started.<br><br>The default is unlimited. |
| | `--cyclelimit` *n* | Maximum number of cycles to run.<br><br>This option is ignored if a debug server is started.<br><br>The default is unlimited. |
| `-T` | `--timelimit` *n* | Maximum number of wall-clock seconds for the simulation to run, excluding startup and shutdown. To terminate the model immediately after initialization, specify `--timelimit 0`. |
| | `--simlimit` *n* | Maximum number of seconds to simulate.<br><br>This option is ignored if a debug server is started.<br><br>The default is unlimited.<br><br>Like the `Simulated time` value output by `--stat`, this value is measured in simulation seconds, not wall-clock seconds. |

| Short form | Long form | Description |
|---|---|---|
| `-b` | `--break [`*`instance`*`=] `*`addr` | Set a program breakpoint on the address of an instruction.<br><br>This option can be specified multiple times.<br><br>For an FVP with multiple cores, you must specify an instance, for example:<br><br>`-b FVP_Morello.cluster0.cpu0=0x80000278` |
| | `--start [`*`instance`*`=] `*`addr` | Set the initial PC value to this address, overriding the `.axf` start address.<br><br>**Note:**<br>• Use this option if you do not want the CPU to start executing at the default reset address. You do not normally need to do this if you are loading an ELF file using `--application`.<br>• This option can be used with `--data` to load binary data that is not in an ELF file. |

**Table 4-5: Timing and performance options**

| Short form | Long form | Description |
|---|---|---|
| | `--cpi-file` *`filename`* | Use *`filename`* to set the Cycles Per Instruction (CPI) class.<br><br>For more information, see CPI files in Fast Models User Guide. |
| `-Q` | `--quantum` *`n`* | Number of ticks to simulate for each quantum. The default is 10000. |
| `-M` | `--min-sync-latency` *`n`* | Number of ticks to simulate before synchronizing. Events that occur at a higher frequency than this value are missed. The default is 100. |

**Table 4-6: Configuration options**

| Short form | Long form | Description |
|---|---|---|
| `-C` | `--parameter` *`instance.param=value`* | Set a parameter. This option can be specified multiple times. Specify the full hierarchical name of the parameter.<br><br>This option is also used to set plug-in parameters. |
| `-f` | `--config-file` *`filename`* | Load parameters from a configuration file. |

**Table 4-7: Options for loading a plug-in or application**

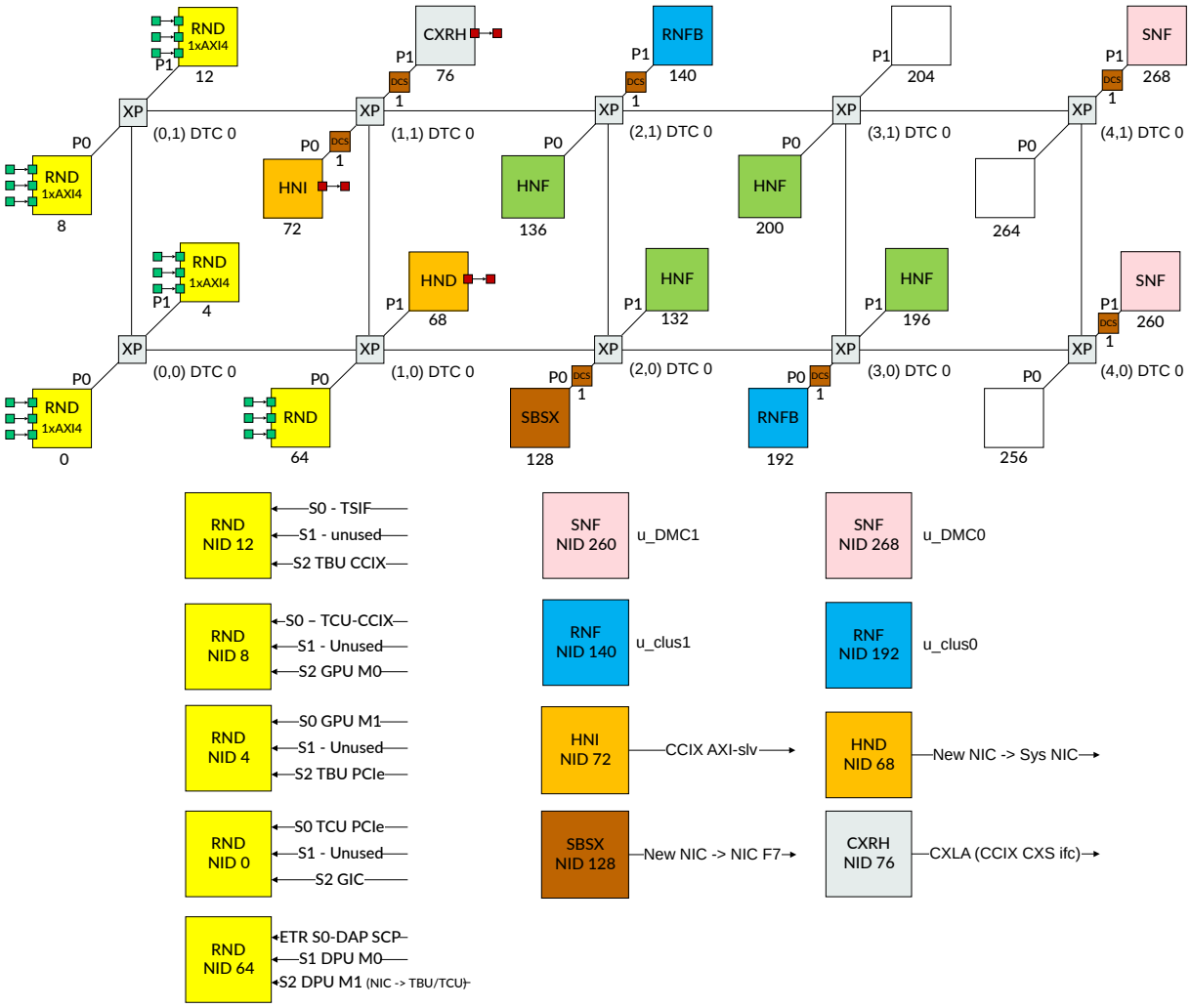
| Short form | Long form | Description |
|---|---|---|
| `-a` | `--application [`*`instance`*`=] `*`filename` | Load an application.<br><br>Specify the core instance to load the application image onto, or use `*` to load it on multiple cores, for example:<br><br>`-a cluster0.cpu*=`*`file` |

| Short form | Long form | Description |
|---|---|---|
| | `--plugin` *`filename`* | Load the plug-in *`filename`*. This option can be specified multiple times. You can also load plug-ins using the `FM_TRACE_PLUGINS` environment variable.<br><br>For more information, see Plug-ins for Fast Models in Fast Models Reference Manual. |
| | `--trace-plugin` *`filename`* | Load a trace plug-in.<br><br>**Note:**<br>This option is deprecated. Use `--plugin` instead. |

# 4.3 CMN-Skeena topology configuration and connection diagram

This figure shows the CMN-Skeena topology configuration diagram and a list of external connections.

**Figure 4-1: CMN-Skeena topology configuration and connection overview**



# 4.4 Morello-specific changes to tarmac trace

Tarmac trace is a format for tracing code executing on an Arm® core, for example branches, memory accesses, or cache hits or misses. Examining tarmac trace is a useful technique in debugging software.

To generate tarmac trace on the FVP, you must load the `TarmacTrace.so` plug-in at simulation startup. The plug-in attaches to the model and registers for specific trace events that might occur during the simulation.

The TarmacTrace plug-in file format is documented in TarmacTrace in the Fast Models Reference Manual. The following topics describe the changes that have been made to TarmacTrace for Morello.

### Related information

TarmacTrace

## 4.4.1 File format changes

New syntax has been added for 129-bit addresses derived from a capability in Morello.

As stated in the Fast Models Reference Manual, 64-bit addresses are written as either:

- 8 hex digits, if the value can be represented in 32 bits.
- 16 hex digits otherwise.

When Morello is enabled, for 129-bit addresses derived from a capability, the value is written as up to 33 hex digits representing the 129 bits of the capability. The tag and the bottom 64 bits are separated using a vertical bar (`|`). The bottom 64 bits are written as described for a 64-bit address. When a physical address is present, the virtual address is surrounded by parentheses.

The following example shows a virtual address derived from a capability with a value of `0x1ffffc0000001000500000000080000000`, and a corresponding physical address of `0x90000000`:

```
(1|ffffc00000010005|80000000):90000000
```

Refer to TarmacTrace file format in the Fast Models Reference Manual.

## 4.4.2 Instruction trace changes

An extra instruction set specifier, `c`, for C64 has been added for Morello.

The new syntax is:

```
[A|T|X|O|C]
```

Refer to Instruction trace in the Fast Models Reference Manual.

### 4.4.3 Register trace changes

New syntax has been added for 129-bit capability registers in Morello.

The following example output shows how these registers are traced when the value changes:

```
61 clk IT (61) 1|ffffc00000010005|80010bc0 c2984120 O EL3h_s : MRS      c0,DDC_EL0
61 clk R C0 1|ffffc00000010005|0000000000000000
```

These registers have the same format as 64-bit registers, with the addition of a vertical bar (|) separating the capability tag, bits [127:64], and bits [63:0].

Refer to Register trace in the Fast Models Reference Manual.

### 4.4.4 Processor memory access trace changes

New syntax has been added for capability tag transfers in Morello.

The new syntax is:

```
<time> <scale> {<cpu>} [M|C]<rw><sz><attrib> <addr> <data>
```

The changes for Morello are:

**[M|C]**

**M** Data transfer.
**C** Capability tag transfer, when Morello is enabled.

**<sz>**

For data transfers, the size of the data transfer in bytes, 1, 2, 4, or 8.

For capability tag transfers, the size of the capability tag transfer in bits. That is, the number of capability tags transferred.

**<data>**

Hexadecimal value of the data transferred. The data padding is according to the size of the transfer. Data of 64 bits or more contains an underscore (_) separator every eight characters (32 bits).

For capability tag transfers, each digit represents a single tag. For example, 1111 represents four tags, each with a value of 1.

Refer to Processor memory access trace in the Fast Models Reference Manual.

## 4.5 ToggleMTIPlugin

Generating trace throughout the simulation can result in very large trace files and slow down the simulation. To help avoid these problems, ToggleMTIPlugin enables you to turn trace generation on or off during the simulation.

ToggleMTIPlugin is enabled, like other plug-ins, using the `--plugin` parameter. If you are enabling multiple plug-ins on the command line, ToggleMTIPlugin must be specified last.

There are two alternative ways to use the plug-in:


Note

You cannot use both of these methods in the same simulation session.

- Using the plug-in parameters `use_hlt = 1` and `hlt_imm16 = #`*`imm16`*.

  This pair of plug-in parameters is used in combination with the application using `HLT #`*`imm16`* for toggling Model Trace Interface (MTI) callbacks. For these parameters to take effect, you must also set the corresponding parameters on the core model that is running the application:

  **enable_trace_special_hlt_imm16**

  If true, enables the parameter `trace_special_hlt_imm16`.

  **trace_special_hlt_imm16**

  Specifies an integer which, when used as the operand to an `HLT` instruction, causes the usual `HLT` execution to be skipped. If the integer matches the value specified in `hlt_imm16`, tracing is turned on or off.

- Using the plug-in parameter `disable_mti_runtime = true`.

  You can set or unset this parameter at runtime using a CADI client, for instance Model Debugger. When set to `true`, trace is disabled.

Each parameter is prefixed with `TRACE.ToggleMTIPlugin`, for example:

```
TRACE.ToggleMTIPlugin.disable_mti_runtime
```

**Table 4-8: ToggleMTIPlugin parameters**

| Parameter | Type | Allowed values | Default value | Runtime | Description |
|---|---|---|---|---|---|
| `diagnostics` | `bool` | `true, false` | `false` | `false` | Print diagnostics. |
| `disable_mti_from_start` | `bool` | - | `false` | `false` | Enable or disable MTI callbacks from start of simulation. |
| `disable_mti_runtime` | `bool` | `true, false` | `false` | `true` | Enable or disable MTI callbacks at runtime. |
| `hlt_imm16` | `int` | - | `0xf000` | `false` | 16-bit integer used in `HLT` instructions that is used by this plug-in. |

| Parameter | Type | Allowed values | Default value | Runtime | Description |
|---|---|---|---|---|---|
| use_hlt | bool | - | true | false | If true, use HLT #imm16 instruction to toggle MTI behavior. |

### Example

For example, the following plug-in parameters cause tracing to begin when HLT #1 is executed:

```
-C TRACE.ToggleMTIPlugin.use_hlt=1 \
-C TRACE.ToggleMTIPlugin.hlt_imm16=1 \
-C TRACE.ToggleMTIPlugin.disable_mti_from_start=1
```

## 4.6 Morello Platform Model instances

FVP_Morello contains the following instances:

**Table 4-9: FVP_Morello instances**

| Name | Type | Description |
|---|---|---|
| Morello_Top | Morello_Top | Top level component of Morello platform model. |
| Morello_Top.board | N1SDP_Morello_Board | The Morello development board. |
| Morello_Top.board.CLUSREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.CPU0REFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.CPU1REFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.DMCREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.DPUREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.GPUREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.HDLCDPLL | PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.board.HDLCDPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.INTREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.IOFPGA_CLK24M | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.IOFPGA_PXLCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.PXLREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.REFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.S32KCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.SYSREFCLK | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.ddr3 | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.ddr_spd | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.dram | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.dual_timer_0_1 | SP804_Timer | Arm Dual-Timer Module(SP804). |
| Morello_Top.board.d\ual_timer_0_1.clk_div0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.d\ual_timer_0_1.clk_div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.d\ual_timer_0_1.counter0 | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.board.d\ual_timer_0_1.counter1 | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.board.dual_timer_2_3 | SP804_Timer | Arm Dual-Timer Module(SP804). |
| Morello_Top.board.d\ual_timer_2_3.clk_div0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.d\ual_timer_2_3.clk_div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.d\ual_timer_2_3.counter0 | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.board.d\ual_timer_2_3.counter1 | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.board.dual_timer_clk | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.dvi_i2c | DummyAPB | DummyAPB. |
| Morello_Top.board.emmc | MMC | Generic Multimedia Card. |
| Morello_Top.board.emmc_config | PL180_MCI | Arm PrimeCell Multimedia Card Interface (PL180). |
| Morello_Top.board.gic400 | GIC_400 | GIC-400 Generic Interrupt Controller. |
| Morello_Top.board.gpio_0 | PL061_GPIO | Arm PrimeCell General Purpose Input/Output(PL061). |
| Morello_Top.board.gpio_1 | PL061_GPIO | Arm PrimeCell General Purpose Input/Output(PL061). |
| Morello_Top.board.hdlcd | PL370_HDLCD | Arm PrimeCell HD Color LCD Controller (Nominal Designation PL370). |
| Morello_Top.board.hdlcd.timer | ClockTimerThread | A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.board.hdlcd.timer.timer | ClockTimerThread64 | A ClockTimerThread(64) is a drop-in replacement for ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.hdl\cd.timer.timer.thread | SchedulerThread | A SchedulerThread instance represents a co-routine thread in the simulation. |
| Morello_Top.board.hdl\cd.timer.timer.thread_event | SchedulerThreadEvent | A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on. |
| Morello_Top.board.hostbridge | HostBridge | Host Socket Interface Component. |
| Morello_Top.board.i3c | DummyAPB | DummyAPB. |
| Morello_Top.board.mcp_back\up_boot_mem | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.mscp_qspi | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.board.mscp_qspi_loader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.board.msd_config | PL180_MCI | Arm PrimeCell Multimedia Card Interface (PL180). |
| Morello_Top.board.msd_mmc | MMC | Generic Multimedia Card. |
| Morello_Top.board.pcie_i2c | DummyAPB | DummyAPB. |
| Morello_Top.board.pl050_kmi0 | PL050_KMI | Arm PrimeCell PS2 Keyboard/Mouse Interface(PL050). |
| Morello_Top.board.pl050_kmi0.clk_di\vider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.pl050_kmi1 | PL050_KMI | Arm PrimeCell PS2 Keyboard/Mouse Interface(PL050). |
| Morello_Top.board.pl050_kmi1.clk_di\vider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.ps2keyboard | PS2Keyboard | Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component. |
| Morello_Top.board.ps2mouse | PS2Mouse | Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component. |
| Morello_Top.board.qspi_config | DummyAPB | DummyAPB. |
| Morello_Top.board.rtc | PL031_RTC | Arm PrimeCell Real Time Clock(PL031). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.s100hz_clk | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.scp_back\ up_boot_mem | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.smc | DummyAPB | DummyAPB. |
| Morello_Top.board.smsc_91c111 | SMSC_91C111 | SMSC 91C111 ethernet controller. |
| Morello_Top.board.sram | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.board.sys_ctrl | SP810_SysCtrl | Only EB relevant functionalities are fully implemented. |
| Morello_Top.board.sys_ctrl.clkdi\ v_clk0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.sys_ctrl.clkdi\ v_clk1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.sys_ctrl.clkdi\ v_clk2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.sys_ctrl.clkdi\ v_clk3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.sys_regs | Morello_SysRegs | Morello Development Board System Registers. |
| Morello_Top.board.tbgp | TestbedGPIOConnector | Tool for receiving GPIO signals and reporting test success/failure. |
| Morello_Top.board.terminal_uar\ t0_board | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.board.terminal_uar\ t1_board | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.board.uart0 | PL011_Uart | Arm PrimeCell UART(PL011). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.board.uart0.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.uart1 | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.board.uart1.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.board.virtioblockdevice | VirtioBlockDevice | virtio block device. |
| Morello_Top.board.watchdog | SP805_Watchdog | Arm Watchdog Module(SP805). |
| Morello_Top.css | N1SDP_Morello_CSS | N1SDP Compute Subsystem. |
| Morello_Top.css.ap_refclk | MemoryMappedGenericTimer | Arm Generic Timer. |
| Morello_Top.css.c0ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c0ClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0ClkCtrl.clkDiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkDiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c0ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelec\t.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0ClkCtrl.clkSelect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c0core0ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c0core0ClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkDiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core0ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core0ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c0core0ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core0_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c0core1ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core1ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core1ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c0core1ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core1_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c0core2ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core2ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c0core2ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core2ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core3ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core3ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c0core3ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c1ClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1ClkCtrl.clkDiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1ClkCtrl.clkDiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkDiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c1ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c1ClkCtrl.clkSelec\t.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelec\t.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelec\t.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelec\t.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1ClkCtrl.clkSelec\t.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c1core0ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core0ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c1core0ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core0_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c1core1ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core1ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c1core1ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core1_clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.c1core2ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core2ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core2ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c1core2ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core2ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl | ScalableClockControl | Clock control allows input selection, rate control and gating. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core3ClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core3ClkCtrl.clk\Div7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Div9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.c1core3ClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.c1core3ClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.clock24MHz | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.cluster0 | Cluster_ARM_Morello | Arm Morello Cluster CT model. |
| Morello_Top.css.cluster0.cpu0 | ARM_Morello | Arm Morello CT model. |
| Morello_Top.css.cluster0.cpu0.dtlb | TlbCadi | TLB - instruction, data or unified. |
| Morello_Top.css.cluster0.cpu0.l1d\cache | PVCache | PV Cache. |
| Morello_Top.css.cluster0.cpu0.l1i\cache | PVCache | PV Cache. |
| Morello_Top.css.clus\ter0.cpu0.l2cache | PVCache | PV Cache. |
| Morello_Top.css.cluster0.cpu1 | ARM_Morello | Arm Morello CT model. |
| Morello_Top.css.cluster0.cpu1.dtlb | TlbCadi | TLB - instruction, data or unified. |
| Morello_Top.css.cluster0.cpu1.l1d\cache | PVCache | PV Cache. |
| Morello_Top.css.cluster0.cpu1.l1i\cache | PVCache | PV Cache. |
| Morello_Top.css.clus\ter0.cpu1.l2cache | PVCache | PV Cache. |
| Morello_Top.css.cluster1 | Cluster_ARM_Morello | Arm Morello Cluster CT model. |
| Morello_Top.css.cluster1.cpu0 | ARM_Morello | Arm Morello CT model. |
| Morello_Top.css.cluster1.cpu0.dtlb | TlbCadi | TLB - instruction, data or unified. |
| Morello_Top.css.cluster1.cpu0.l1d\cache | PVCache | PV Cache. |
| Morello_Top.css.cluster1.cpu0.l1i\cache | PVCache | PV Cache. |
| Morello_Top.css.clus\ter1.cpu0.l2cache | PVCache | PV Cache. |
| Morello_Top.css.cluster1.cpu1 | ARM_Morello | Arm Morello CT model. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.cluster1.cpu1.dtlb | TlbCadi | TLB - instruction, data or unified. |
| Morello_Top.css.cluster1.cpu1.l1d\ cache | PVCache | PV Cache. |
| Morello_Top.css.cluster1.cpu1.l1i\ cache | PVCache | PV Cache. |
| Morello_Top.css.clus\ ter1.cpu1.l2cache | PVCache | PV Cache. |
| Morello_Top.css.cmn600 | CMN600 | CCN CMN600 Interconnect. |
| Morello_Top.css.cmn600.cmn600_cache | CMN600Cache | CMN600 Interconnect Cache. |
| Morello_Top.css.debugUnit | Ashbrook_DebugUnit | currently all stubs with IDs. |
| Morello_Top.css.debugUnit.dum\ my_coresight_registers | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.css.debugUnit.dum\ my_etrsmmu_registers | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_0 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_1 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_2 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_3 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_4 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_5 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_6 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_7 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_8 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_9 | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_abm_a | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_cpm_b | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_mctlr | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_mpm_c | DummyAPB | DummyAPB. |
| Morello_Top.css.debugUnit.dum\ my_sysprof_registers | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.css.debugUnit.re\ served_Mem | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.display_processor | D71 | Arm D71 Display Processor. |
| Morello_Top.css.dp_msi_rewriter_pcie | MSIRewriter | Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does. |
| Morello_Top.css.dp_msi_rewriter_smmu | MSIRewriter | Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does. |
| Morello_Top.css.dpuClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.dpuClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.dpuClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelec\t.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpuClkCtrl.clkSelect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.dpu_smmu | MMU_600 | SMMUv3 compliant device. |
| Morello_Top.css.exclusive_monitor_0 | PVBusExclusiveMonitor | Global exclusive monitor. |
| Morello_Top.css.exclusive_monitor_1 | PVBusExclusiveMonitor | Global exclusive monitor. |
| Morello_Top.css.exclusive_monitor_4 | PVBusExclusiveMonitor | Global exclusive monitor. |
| Morello_Top.css.exclusive_monitor_5 | PVBusExclusiveMonitor | Global exclusive monitor. |
| Morello_Top.css.exclusive_monitor_6 | PVBusExclusiveMonitor | Global exclusive monitor. |
| Morello_Top.css.generic_watchdog | MemoryMappedGenericWatchdog | Arm Generic Watchdog. |
| Morello_Top.css.gic_distributor | GIC600 | GIC-600. |
| Morello_Top.css.gpu | Mali_G76 | Arm Mali-G76 GPU. |
| Morello_Top.css.gpuClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.gpuClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.gpuClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.gpuClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.gpuClkCtrl.clkSelec\t.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.hni_logger | PVBusLogger | Bus Logger. |
| Morello_Top.css.mcp | SGI_575_MCP | - |
| Morello_Top.css.mcp.AP2MCP_MHU | Juno_SCP_MHU | Juno Message Handling Unit. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.mcp.AP2M\CP_NONSEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.AP2MCP_SEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.DTCRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.GenericTimerRef | MemoryMappedGenericTimer | Arm Generic Timer. |
| Morello_Top.css.mcp.ITCRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.ROM | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.css.mcp.ROMloader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.css.mcp.SCP2MCP_MHU | Juno_SCP_MHU | Juno Message Handling Unit. |
| Morello_Top.css.mcp.SCP2M\CP_NONSEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.SCP2MCP_SEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.mcp.armcortexm7ct | ARM_Cortex-M7 | Arm CORTEXM7 CT model. |
| Morello_Top.css.mcp.clock24MHz | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.mcp.cmsdk_watchdog | CMSDK_Watchdog | Arm Watchdog Module. |
| Morello_Top.css.mcp.exclu\sive_squasher | PVBusExclusiveSquasher | Squashes the exclusive attribute on bus transactions. |
| Morello_Top.css.mcp.mcpClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.mcp.mcpClkCtrl.clk\Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clk\Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.mcp.mcpClkCtrl.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcpClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.mcp_addr_tran | Kits2_AddrTran | Address Translator for Ashbrook Subsystem. |
| Morello_Top.css.mcp.mcp_pik | PIK_MCP_Ashbrook | Ashbrook MCP Power Integration Kit. |
| Morello_Top.css.mcp.m\cp_pik.ws1_timer | Kits2_Timer | Kits2 Timer. |
| Morello_Top.css.mcp.m\cp_pik.ws1_timer.clk_div | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.mcp.m\cp_pik.ws1_timer.counter | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.css.mcp.pl011_uart0_mcp | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.css.mcp.pl011_uart0_m\cp.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.pl011_uart1_mcp | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.css.mcp.pl011_uart1_m\cp.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.mcp.reserved_Mem | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.css.mcp.secure_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mcp.secure_squasher | PVBusSecureSquasher | Squashes the secure attributes on bus transactions. |
| Morello_Top.css.mcp.terminal_uart0 | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.mcp.terminal_uart1 | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.mcp_sec_ctrl | Kits2_Privileged_to_Se\cure_Mapper | Kits2 Security Enabler. |
| Morello_Top.css.mem | SGI_575_MemoryElement | Memory Element with Config of DMC # Check. |
| Morello_Top.css.mem.apb_chn_filter0 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.apb_chn_filter1 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.apb_chn_filter2 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.apb_chn_filter3 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.dmc0 | Infra_MemoryElement_DM\C_Bing | Memory Element with DMC-Bing. |
| Morello_Top.css.mem.dmc0.dmc | DMC_Bing | Arm DMC-Bing Dynamic Memory Controller. |
| Morello_Top.css.mem.dmc0.dmc.metada\ta_controller | PVMetadataController | MetaData controller that provides end-point storage to metadata in a system. |
| Morello_Top.css.mem.dmc0.dmcMgr | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc0.dmcProf | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc0.dmcSensor | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc1 | Infra_MemoryElement_DM\C_Bing | Memory Element with DMC-Bing. |
| Morello_Top.css.mem.dmc1.dmc | DMC_Bing | Arm DMC-Bing Dynamic Memory Controller. |
| Morello_Top.css.mem.dmc1.dmc.metada\ta_controller | PVMetadataController | MetaData controller that provides end-point storage to metadata in a system. |
| Morello_Top.css.mem.dmc1.dmcMgr | DummyAPB | DummyAPB. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.mem.dmc1.dmcProf | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc1.dmcSensor | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc2 | Infra_MemoryElement_DMC_Bing | Memory Element with DMC-Bing. |
| Morello_Top.css.mem.dmc2.dmc | DMC_Bing | Arm DMC-Bing Dynamic Memory Controller. |
| Morello_Top.css.mem.dmc2.dmc.metadata_controller | PVMetadataController | MetaData controller that provides end-point storage to metadata in a system. |
| Morello_Top.css.mem.dmc2.dmcMgr | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc2.dmcProf | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc2.dmcSensor | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc3 | Infra_MemoryElement_DMC_Bing | Memory Element with DMC-Bing. |
| Morello_Top.css.mem.dmc3.dmc | DMC_Bing | Arm DMC-Bing Dynamic Memory Controller. |
| Morello_Top.css.mem.dmc3.dmc.metadata_controller | PVMetadataController | MetaData controller that provides end-point storage to metadata in a system. |
| Morello_Top.css.mem.dmc3.dmcMgr | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc3.dmcProf | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.dmc3.dmcSensor | DummyAPB | DummyAPB. |
| Morello_Top.css.mem.interruptOrGate0 | OrGate | Or Gate. |
| Morello_Top.css.mem.interruptOrGate1 | OrGate | Or Gate. |
| Morello_Top.css.mem.interruptOrGate2 | OrGate | Or Gate. |
| Morello_Top.css.mem.interruptOrGate3 | OrGate | Or Gate. |
| Morello_Top.css.mem.mem_chn_filter0 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mem_chn_filter1 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mem_chn_filter2 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mem_chn_filter3 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mgr_chn_filter0 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mgr_chn_filter1 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mgr_chn_filter2 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.mgr_chn_filter3 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.prof_chn_filter0 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.prof_chn_filter1 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.prof_chn_filter2 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.prof_chn_filter3 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.sensor_chn_filter0 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.sensor_chn_filter1 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.sensor_chn_filter2 | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.mem.sensor_chn_filter3 | TZFilterUnit | TrustZone Filter Unit. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.msi_rewriter_pcie | MSIRewriter | Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does. |
| Morello_Top.css.msi_rewriter_smmu | MSIRewriter | Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does. |
| Morello_Top.css.nic400 | N1SDP_Morello_CSS_NIC400 | N1SDP Morello CSS NIC-400 component. |
| Morello_Top.css.nic400.core\ sight_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.nic400.nic_buslogger | PVBusLogger | Bus Logger. |
| Morello_Top.css.nic400.reserved_Mem | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.css.nic400.secure_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.nic400.se\ cure_scp_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.nic400_buslogger | PVBusLogger | Bus Logger. |
| Morello_Top.css.nonTrustedROM | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.css.nonTrustedROMloader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.css.nonTrustedSRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.pl011_sec_uart_ap | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.css.pl011_sec_uar\ t_ap.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pl011_uart1_ap | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.css.pl011_uar\ t1_ap.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pl011_uart_ap | PL011_Uart | Arm PrimeCell UART(PL011). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.pl011_uar\ t_ap.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.powerStateGate | Kits2_PowerStateGate | Power State Gate to filter the access to SYSTOP domain. |
| Morello_Top.css.pxlClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.pxlClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.pxlClkCtrl.clk\ Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.pxlClkCtrl.clkSelec\ t.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\ t.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.pxlClkCtrl.clkSelec\t.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp | N1SDP_Morello_SCP | - |
| Morello_Top.c\ss.scp.AP2SCP_NONSEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.scp.AP2SCP_SEC_RAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.scp.CS_Counter | MemoryMappedCounterMod\ule | Memory Mapped Counter Module for Generic Timers. |
| Morello_Top.css.scp.DTCRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.scp.GenericTimerRef | MemoryMappedGenericTimer | Arm Generic Timer. |
| Morello_Top.css.scp.ITCRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.scp.ROM | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.css.scp.ROMloader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.css.scp.armcortexm7ct | ARM_Cortex-M7 | Arm CORTEXM7 CT model. |
| Morello_Top.css.scp.c0_pik | Kits3_PIK_Cluster | Kits3 SCP Cluster Power Integration Kit for v8.2 cores. |
| Morello_Top.css.scp.c0_pik.ppu_clus\ter | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core0 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core1 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core2 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core3 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core4 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core5 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core6 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c0_pik.ppu_core7 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.scp.c0_tem | Temperature | Component to synthesis the temperature value of the connected core. |
| Morello_Top.css.scp.c1_pik | Kits3_PIK_Cluster | Kits3 SCP Cluster Power Integration Kit for v8.2 cores. |
| Morello_Top.css.scp.c1_pik.ppu_clus\ter | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core0 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core1 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core2 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core3 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core4 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core5 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core6 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_pik.ppu_core7 | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.c1_tem | Temperature | Component to synthesis the temperature value of the connected core. |
| Morello_Top.css.scp.clock24MHz | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.clockWatcher | FrequencyProbe | Clock Frequency observer. |
| Morello_Top.css.scp.cluster_ppu_Or\Gate | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.cluster_ppu_Or\Gate0 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.cmsdk_watchdog | CMSDK_Watchdog | Arm Watchdog Module. |
| Morello_Top.css.scp.cpu_ppu_OrGate | WideOrGate_12x4 | Or Gate with up to 48 inputs and support to num_cores. |
| Morello_Top.css.scp.debug_pik | PIK_Debug | Kits Debug Power Integration Kit. |
| Morello_Top.css.scp.debug_pik.p\pu_debug_top | PowerPolicyUnit | Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.display_pik | Mobile4_PIK_Display | Mobile4 Display Power Integration Kit. |
| Morello_Top.css.scp.display_pik.p\pu_dpu_top | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.exclu\sive_squasher | PVBusExclusiveSquasher | Squashes the exclusive attribute on bus transactions. |
| Morello_Top.css.scp.gen_timer_Or\Gate0 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.gen_timer_Or\Gate00 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.gpu_pik | Mobile4_PIK_GPU | Mobile4 GPU Power Integration Kit. |
| Morello_Top.css.scp.gpu_pik.ppu_g\pu_top | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.scp.pl011_uart_scp | PL011_Uart | Arm PrimeCell UART(PL011). |
| Morello_Top.css.scp.pl011_uar\ t_scp.clk_divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.pll_lock_OrGate | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.pll_unlock_Or\ Gate | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.proc_n_gener\ ic_timer_ref0 | MemoryMappedGenericTimer | Arm Generic Timer. |
| Morello_Top.css.scp.refcounter | MemoryMappedCounterMod\ ule | Memory Mapped Counter Module for Generic Timers. |
| Morello_Top.css.scp.reserved_Mem | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.css.scp.scpClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.scp.scpClkCtrl.clk\ Div1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clk\ Div2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clk\ Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.scp.scpClkCtrl.clk\ Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\ elect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.scp.scpClkCtrl.clkS\ elect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scpClkCtrl.clkS\elect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.scp.scp_addr_tran | Kits2_AddrTran | Address Translator for Ashbrook Subsystem. |
| Morello_Top.css.scp.scp_mhu0 | Juno_SCP_MHU | Juno Message Handling Unit. |
| Morello_Top.css.scp.scp_mhu1 | Juno_SCP_MHU | Juno Message Handling Unit. |
| Morello_Top.css.scp.scp_mhu_CPU_IN\TR_H_OrGate | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.scp_mhu_CPU_IN\TR_H_OrGate0 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.scp_mhu_CPU_IN\TR_H_OrGate1 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.scp_mhu_CPU_IN\TR_S_OrGate | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.scp_mhu_CPU_IN\TR_S_OrGate0 | WideOrGate | Or Gate with up to 8 inputs. |
| Morello_Top.css.scp.scp_pik | PIK_SCP_SGI_575 | SGI_575 SCP Power Integration Kit. |
| Morello_Top.c\ss.scp.scp_pik.ws1_timer | Kits2_Timer | Kits2 Timer. |
| Morello_Top.c\ss.scp.scp_pik.ws1_timer.clk_div | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.scp.scp_pik.ws1_timer.counter | CounterModule | Internal component used by SP804 Timer module. |
| Morello_Top.css.scp.secure_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.scp.securitycontrol_unit | Kits4_SecurityControlUnit | Security Control Unit in Kits4(Clark). |
| Morello_Top.css.scp.system_pik | PIK_System_SGI_575 | SGI-575 System Power Control. |
| Morello_Top.css.scp.system_pik.pu_sys_logic | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.system_pik.pu_sys_sram | PPUv1 | Arm Power Policy Unit (PPU) architectural model. |
| Morello_Top.css.scp.terminal_uart_aon | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.scp_filter | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.css.smmu | MMU_600 | SMMUv3 compliant device. |
| Morello_Top.css.tcuClkCtrl | SwitchedClockControl | Clock control allows input selection, rate control and gating. |
| Morello_Top.css.tcuClkCtrl.clkDiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkDiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkGate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.css.tcuClkCtrl.clkGate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect | ClockSelector | ClockSignal Selector. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.tcuClkCtrl.clkSelect.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.css.terminal_sec_uart_ap | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.terminal_uart1_ap | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.terminal_uart_ap | TelnetTerminal | Telnet terminal interface. |
| Morello_Top.css.trustedBootROM | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.css.trustedBootROMloader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.css.trustedSRAM | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.css.trusted_watchdog | MemoryMappedGenericWatchdog | Arm Generic Watchdog. |
| Morello_Top.pci | BasePlatformPCIAHCI | PCI addon for the Base Platform. |
| Morello_Top.pci.ahci | AHCI_PCI | - |
| Morello_Top.pci.ahci.ahci | AHCI_SATA | AHCI controller with attached SATA disks and PCIe interface. |
| Morello_Top.pci.ahci.buslogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcidevice | PCIDevice | PCI Wrapper for memory mapped components. |
| Morello_Top.pci.ahci.pcidevice.dmalogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcidevice.incoming_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcidevice.lost_mastered_transactions | PVBusLogger | Bus Logger. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.pci.ahci.pcide\vice.lost_transactions_to_pcie | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcidevice.m\six_pba_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcidevice.m\six_table_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.ahci.pcide\vice.to_client_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.dma330x4 | DMA330x4 | - |
| Morello_Top.pci.dma330x4.dmac0 | PL330_DMAC | Arm PrimeCell DMA Controller(PL330). |
| Morello_Top.pci.dma330x4.dmac0.timer | ClockTimerThread | A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac0.timer.timer | ClockTimerThread64 | A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac0.timer.timer.thread | SchedulerThread | A SchedulerThread instance represents a co-routine thread in the simulation. |
| Morello_Top.pci.dma330x4.d\mac0.timer.timer.thread_event | SchedulerThreadEvent | A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on. |
| Morello_Top.pci.dma330x4.dmac1 | PL330_DMAC | Arm PrimeCell DMA Controller(PL330). |
| Morello_Top.pci.dma330x4.dmac1.timer | ClockTimerThread | A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.pci.dma330x4.d\mac1.timer.timer | ClockTimerThread64 | A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac1.timer.timer.thread | SchedulerThread | A SchedulerThread instance represents a co-routine thread in the simulation. |
| Morello_Top.pci.dma330x4.d\mac1.timer.timer.thread_event | SchedulerThreadEvent | A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on. |
| Morello_Top.pci.dma330x4.dmac2 | PL330_DMAC | Arm PrimeCell DMA Controller(PL330). |
| Morello_Top.pci.dma330x4.dmac2.timer | ClockTimerThread | A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac2.timer.timer | ClockTimerThread64 | A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac2.timer.timer.thread | SchedulerThread | A SchedulerThread instance represents a co-routine thread in the simulation. |
| Morello_Top.pci.dma330x4.d\mac2.timer.timer.thread_event | SchedulerThreadEvent | A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on. |
| Morello_Top.pci.dma330x4.dmac3 | PL330_DMAC | Arm PrimeCell DMA Controller(PL330). |

| Name | Type | Description |
|---|---|---|
| Morello_Top.pci.dma330x4.dmac3.timer | ClockTimerThread | A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac3.timer.timer | ClockTimerThread64 | A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64). |
| Morello_Top.pci.dma330x4.d\mac3.timer.timer.thread | SchedulerThread | A SchedulerThread instance represents a co-routine thread in the simulation. |
| Morello_Top.pci.dma330x4.d\mac3.timer.timer.thread_event | SchedulerThreadEvent | A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on. |
| Morello_Top.pci.pci_smmuv3 | SMMUv3_FOR_PCIE | System MMUv3 configured for PCI-E Sub-system. |
| Morello_Top.pci.pci_smmuv3.mmu | SMMUv3AEM | SMMUv3 AEM. |
| Morello_Top.pci.pci_smmuv3_m\sirewriter | MSIRewriter | Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does. |
| Morello_Top.pci.pcidevice0 | PCIDevice | PCI Wrapper for memory mapped components. |
| Morello_Top.pci.pcidevice0.dmalogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice0.incom\ing_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice0.lost_mas\tered_transactions | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcide\vice0.lost_transactions_to_pcie | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice0.msix_p\ba_logger | PVBusLogger | Bus Logger. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.pci.pcidevice0.msix_ta\ble_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice0.to_clien\t_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1 | PCIDevice | PCI Wrapper for memory mapped components. |
| Morello_Top.pci.pcidevice1.dmalogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1.incom\ing_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1.lost_mas\tered_transactions | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcide\vice1.lost_transactions_to_pcie | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1.msix_p\ba_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1.msix_ta\ble_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcidevice1.to_clien\t_memory_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pcivirtioblockde\vice0 | VirtioPCIBlockDevice | virtio PCI block device. |
| Morello_Top.pci.pcivirtioblockde\vice1 | VirtioPCIBlockDevice | virtio PCI block device. |
| Morello_Top.pci.pvbus2pci | PVBus2PCI | PVBus to PCI Bridge. |
| Morello_Top.pci.pvbus2pci.cfglogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pvbus2pci.devicelog\ger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.pvbus2pci.dmalogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.smmulogger | PVBusLogger | Bus Logger. |
| Morello_Top.pci.tbu0_pre_smmu_logger | PVBusLogger | Bus Logger. |
| Morello_Top.pci_logger0 | PVBusLogger | Bus Logger. |
| Morello_Top.soc | N1SDP_Morello_SoC | Morello SoC model. |
| Morello_Top.soc.CLUSPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.CLUSPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.CPU0PLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.CPU0PLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.soc.CPU1PLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.CPU1PLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.DMCPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.DMCPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.DPUPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.DPUPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.GPUPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.GPUPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.INTPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.INTPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.PXLPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.PXLPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.soc.SYSAPBCLKClk | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelect | ClusterClockControl | Cluster clock control allows input selection, rate control and gating. |
| Morello_Top.soc.SYSAPBCLKSelect.clk\Gate | ClockGate | Clock gate for dis/enabling the clock. |
| Morello_Top.soc.SYSAPBCLKSelect.clk\Gate.divider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector | ClockSelector | ClockSignal Selector. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv0 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv1 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv10 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv2 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv3 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv4 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv5 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv6 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv7 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv8 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdiv9 | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.soc.SYSAPBCLKSelec\t.clkSelector.clkdivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelect.ref\ClkDiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelec\t.sysClkDiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSAPBCLKSelect.x\ClkDiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.SYSPLL | Infra1_PLLControl | Simulate PLL clock frequency control logic. |
| Morello_Top.soc.SYSPLL.clkdiv | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.soc.buslogger | PVBusLogger | Bus Logger. |
| Morello_Top.soc.dummyAPB | DummyAPB | DummyAPB. |
| Morello_Top.soc.mcp_i2c_0 | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.soc.mcp_i2c_1 | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.soc.mcp_qspi | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.soc.mcp_qspi_loader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.soc.mscp_soc_reserved | WarningMemory | Memory that prints warnings, and RAZ/WIs or aborts. |
| Morello_Top.soc.pci_phy | DummyAPB | DummyAPB. |
| Morello_Top.soc.pcie_macro | DummyAPB | DummyAPB. |
| Morello_Top.soc.pcie_rootport | DummyAPB | DummyAPB. |
| Morello_Top.soc.scc | Morello_SoC_SCC | Morello SoC System Configuration Controller. |
| Morello_Top.soc.scp_i2c_0 | RAMDevice | RAM device, can be dynamic or static ram. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.soc.scp_i2c_1 | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.soc.scp_i2c_2 | RAMDevice | RAM device, can be dynamic or static ram. |
| Morello_Top.soc.scp_qspi | IntelStrataFlashJ3 | Intel Strata Flash J3 LISA+ model. |
| Morello_Top.soc.scp_qspi_loader | FlashLoader | A device that can preload a gzipped image into flash at startup. |
| Morello_Top.soc.sensors | DummyAPB | DummyAPB. |
| Morello_Top.soc.soc_gpio | PL061_GPIO | Arm PrimeCell General Purpose Input/ Output(PL061). |
| Morello_Top.soc.sys_nic | TZFilterUnit | TrustZone Filter Unit. |
| Morello_Top.vis_dashboard | Visualisation_sdl2 | Display window for VE using sdl2 Visualisation library. |
| Morello_Top.vis_dashboard.recorder | VisEventRecorder | Event recorder component for visualisation component (allows to playback and record interactive GUI sessions). |
| Morello_Top.vis_dash\ board.recorder.playbackDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_dash\ board.recorder.recordingDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_dp0 | Visualisation_sdl2 | Display window for VE using sdl2 Visualisation library. |
| Morello_Top.vis_dp0.recorder | VisEventRecorder | Event recorder component for visualisation component (allows to playback and record interactive GUI sessions). |
| Morello_Top.vis_dp0.recorder.play\ backDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_dp0.recorder.record\ ingDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_dp1 | Visualisation_sdl2 | Display window for VE using sdl2 Visualisation library. |

| Name | Type | Description |
|---|---|---|
| Morello_Top.vis_dp1.recorder | VisEventRecorder | Event recorder component for visualisation component (allows to playback and record interactive GUI sessions). |
| Morello_Top.vis_dp1.recorder.playbackDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_dp1.recorder.recordingDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_hdlcd | Visualisation_sdl2 | Display window for VE using sdl2 Visualisation library. |
| Morello_Top.vis_hdlcd.recorder | VisEventRecorder | Event recorder component for visualisation component (allows to playback and record interactive GUI sessions). |
| Morello_Top.vis_hdlcd.recorder.playbackDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |
| Morello_Top.vis_hdlcd.recorder.recordingDivider | ClockDivider | A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters. |