arm

Arm® Corstone[™] SSE-300 with Cortex®-M55 and Ethos[™]-U55 : Example Subsystem for MPS3

Revision: C

Application Note AN547

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Arm® Corstone[™] SSE-300 with Cortex®-M55 and Ethos[™]-U55 : Example Subsystem for MPS3 Application Note AN547

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Release information

Document history

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| А | 30 November 2020 | Confidential | First Issue |
| В | 29 January 2021 | Non-Confidential | Confidentiality status changed to Non-Confidential |
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DELIVERABLES

Part A

Hardware Binaries:

Encrypted FPGA bitstream file containing various the Arm technology including:

SSE-300 Subsystem

Cortex-M55 Processor

Ethos-U55 Embedded ML Inference processor.

Software Binaries:

Motherboard Configuration Controller binary (mbb_vxxx.ebf), including Keil[®] USB and SD card drivers, and Analog Devices FMC EEPROM reader.

selftest binary (an547_st.axf) for Cortex-M55 in Corstone™ SSE-300.

Documentation:

Documentation, provided as PDF

Part B

Text configuration files (.txt) in the <install_dir>/Boardfiles/MB/HBI0309x/ directory: /board.txt /AN547/an547_vx.txt /AN547/images.txt

Part C

None

Part D

None

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1 Introduction

1.1 Intended audience

This application note document is written for experienced hardware, System-on-Chip (SoC) and software engineers who might or might not have experience with Arm products. Such engineers typically have experience in writing Verilog and of performing synthesis but might have limited experience of integrating and implementing Arm products.

1.2 Conventions

The following subsections describe conventions used in Arm documents.

1.2.1 Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: https://developer.arm.com/glossary.

1.2.2 Typographical conventions

| Convention | Use |
|------------------------|---|
| italic | Introduces citations. |
| bold | Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate. |
| monospace | Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code. |
| monospace bold | Denotes language keywords when used outside example code. |
| monospace underline | Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. |
| <and></and> | Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: MRC p15, 0, <rd>, <crn>, <crm>, <opcode_2></opcode_2></crm></crn></rd> |
| SMALL CAPITALS | Used in body text for a few terms that have specific technical meanings, that are defined in the Arm [®] Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE. |
| Caution | This represents a recommendation which, if not followed, might lead to system failure or damage. |
| Warning | This represents a requirement for the system that, if not followed, might result in system failure or damage. |
| Danger | This represents a requirement for the system that, if not followed, will result in system failure or damage. |
| Note | This represents an important piece of information that needs your attention. |
| - Č | This represents a useful tip that might make it easier, better or faster to perform a task. |
| Remember | This is a reminder of something important that relates to the information you are reading. |

1.3 Additional reading

This document contains information that is specific to this product. See the following documents for other relevant information:

| Document name | Document ID | Licensee only |
|--|-------------|------------------------------|
| Arm® MPS3 FPGA Prototyping Board Technical Reference Manual | 100765 | No |
| Arm® Corstone™ SSE-300 Example Subsystem Technical Reference Manual | 101773 | No |
| Arm® Corstone™ SSE-300 Example Subsystem Configuration and Integration Manual | 101774 | Yes |
| Arm® Ethos™-U55 NPU Technical reference manual | 101885 | No |
| Arm® CoreLink™ SIE-200 System IP for Embedded Technical Reference Manual | DDI 0571 | No |
| Arm® CoreLink™ SIE-300 AXI5 System IP for Embedded Technical Reference Manual | 101526 | No |
| Arm® Cortex®-M System Design Kit Technical Reference Manual | DDI 0479 | No |
| Arm® CoreLink™ XHB-500 Bridge Technical Reference Manual | 101375 | No |
| MCBQVGA-TS-Display-v12 – Keil MCBSTM32F200 display board schematic | - | No |
| Arm® MPS3 FPGA Prototyping Board Getting Started Guide | - | No |
| | | Table 1-1 · Arm Publications |

Table 1-1: Arm Publications

1.4 Feedback

Arm welcomes feedback on this product and its documentation.

1.4.1 Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

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- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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If you have comments on content, send an email to errata@arm.com and give:

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- The number DAI 0547C.
- If applicable, the page number(s) to which your comments refer.
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1.4.3 Other information

- Arm Documentation, https://developer.arm.com/documentation/
- Arm Technical Support Knowledge Articles, https://www.arm.com/support/technical-support
- Arm Support, https://www.arm.com/support
- Arm Glossary, https://developer.arm.com/documentation/aeg0014/g

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

2 Preface

2.1 Purpose of this application note

This application note describes the features and functionality of the AN547 Soft Macrocell Model (SMM), or AN547 subsystem. The AN547 SMM is an FPGA image that is a Single Cortex-M55 FPGA implementation of the Corstone SSE-300 with Cortex-M55 and Ethos[™]-U55 Example Subsystem. The example subsystem uses SIE-300 and SIE-200 components with CMSDK peripherals to provide a reference design.

2.2 Terms and abbreviations

| AHB | Advanced High-performance Bus |
|--------|---|
| APB | Advanced Peripheral Bus |
| BRAM | Block Random Access Memory |
| CMSDK | Cortex-M System Design Kit |
| DMA | Direct Memory Access |
| DTCM | Data Tightly Coupled Memory |
| EAM | Exclusive Access Controller |
| FPGA | Field Programmable Gate Array |
| IDAU | Implementation Defined Attribution Unit |
| ITCM | Instruction Tightly Coupled Memory |
| KB | Kilobyte |
| MB | Megabyte |
| MCC | Motherboard Configuration Controller |
| MPC | Memory Protection Controller |
| MSC | Manager Security Controller |
| PPC | Peripheral Protection Controller |
| RAM | Random Access Memory |
| RAZ/WI | Read As Zero/Write Ignored |
| RTC | Real Time Clock |
| RTL | Register Transfer Level |
| SCC | Serial Configuration Controller |
| SMM | Soft Macrocell Model system implemented as an FPGA image and described in this AN |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| TPIU | Trace Port Interface Unit |
| TRM | Technical Reference Manual |
| | |

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2.3 Arm IP version details

The following IP packages have been used in this Product.

| Version | Description |
|-------------|---|
| rOpO | Arm® Corstone [™] SSE-300 The Arm® Corstone [™] SSE-300 Example Subsystem is a collection of pre-assembled elements to use as the basis of an Internet of Things (IoT) System on Chip (SoC). |
| r1p0 | Arm® Ethos™-U55 NPU The Arm® Ethos™-U55 is a Neural Processing Unit (NPU) which improves the inference performance of neural networks. |
| r1p0 | Arm® CoreLink [™] SIE-300 The SIE-300 AXI5 System IP for Embedded provides a set of configurable AXI5 security- aware components. |
| r3p1 | Arm® CoreLink [™] SIE-200 The CoreLink SIE-200 System IP for Embedded product is a collection of interconnect, peripheral, and TrustZone® controller components for use with a processor that complies with the ARMv8-M processor architecture. |
| BP210 | Cortex-M System Design Kit Full version of the design kit supporting Cortex-M0, Cortex-M0 DesignStart [®] , Cortex- M0+, Cortex-M3 and Cortex-M4. Also contains the AHB Bus Matrix and advanced AHB components. |
| r1p3-00rel1 | Arm® PrimeCell Synchronous Serial Port (PL022) Arm PrimeCell Synchronous Serial Port |

Figure 2-1: Arm IP versions

2.4 Encryption key

Arm supplies the MPS3 prototyping board with a decryption key programmed into the FPGA. This key is needed to enable loading of prebuilt encrypted images.

<u>Note</u>

The FPGA programming file that is supplied as part of the bundle is encrypted.

Caution

A battery supplies power to the key storage area of the FPGA. Any keys stored in the FPGA might be lost when battery power is lost. If this happens you must return the board to Arm for reprogramming of the key.

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3 Overview

The AN547 SMM is a Single Cortex-M55 FPGA implementation of the Corstone SSE-300 with Cortex-M55 and Ethos-U55 Example Subsystem. The example subsystem uses SIE-300 and SIE-200 components with CMSDK peripherals to provide a reference design.

3.1 System block diagram

The following high-level block diagram shows the full MPS3 FPGA System :



Figure 3-1 : MPS3 System Overview

3.2 SSE-300 Configuration

The following tables show the configuration settings of the SSE-300 subsystem in the AN547 SMM. See the Arm® Corstone[™] SSE-300 Example Subsystem Configuration and Integration Manual for full details of each configuration option.

3.2.1 Render Settings

| Configuration Define | SSE-300 Default Value | AN547 Value |
|-----------------------------------|--------------------------|-------------|
| NUMCPU | 0 | 0 |
| PILEVEL | 1 | 1 |
| CPUOTYPE | 3 | 3 |
| CPU1TYPE | 0 | 0 |
| CPU2TYPE | 0 | 0 |
| CPU3TYPE | 0 | 0 |
| NUMNPU | 1 | 1 |
| NPUOTYPE | 1 | 1 |
| NPU1TYPE | 0 | 0 |
| NPU2TYPE | 0 | 0 |
| NPU3TYPE | 0 | 0 |
| NPU0_NUM_MACS | 128 | 128 |
| NPU1_NUM_MACS | 256 | 256 |
| NPU2_NUM_MACS | 32 | 32 |
| NPU3_NUM_MACS | 64 | 64 |
| NUM_AXI_SLAVES_EXP_MI | 2 | 2 |
| NUM_AHB_SLAVES_EXP_PIHL | 1 | 1 |
| NUM_AHB_SLAVES_EXP_PILL | 1 | 1 |
| EXPLOGIC_PRESENT | 1 | 1 |
| VMMPCBLKSIZE | 7 | 11 |
| CPU0_INITNSVTOR_ADDR_INIT | 0x00000000 | 0x00000000 |
| CPUOEXPNUMIRQ | 64 | 100 |
| CPU0EXPIRQDIS | 64b0 | 100b0 |
| CPU0_EXP_IRQTIER | 65b1 | 100b1 |
| CPU0_INT_IRQTIER | 32b1 | 32b1 |
| CPU0_EXP_IRQ_PULSE_SPT_PRESENT | 64b0 | 100b0 |
| CPU0_EXP_IRQ_SYNC_TO_CPU_PRESENT | 65b1 | 100b1 |
| CPU0_EXP_IRQ_SYNC_TO_EWIC_PRESENT | 65b1 | 100b1 |
| CPU0_EXP_NMI_PULSE_SPT_PRESENT | 0 | 0 |
| CPU0_EXP_NMI_SYNC_TO_CPU_PRESENT | 1 | 1 |
| CPU0_EXP_NMI_SYNC_TO_EWIC_PRESENT | 1 | 1 |
| DEBUGLEVEL | 0 | 2 |
| CPU0_ITM_PRESENT | 1 | 1 |
| CPU0_ETM_PRESENT | 2 | 1 |
| CPU0_FPU_PRESENT | 1 | 1 |
| CPU0_MVE_CONFIG | 2 | 2 |
| SECEXT | 1 | 1 |
| CPU0_MPU_S | 8 | 16 |
| CPU0_MPU_NS | 8 | 16 |

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| CPU0_SAUDISABLE | 0 | 0 |
|-------------------------|---------|---------|
| CPU0_NUM_SAU_CONFIG | 8 | 8 |
| CPU0_DBGLVL | 2 | 2 |
| HASCPUOCPIF | 1 | 0 |
| CPU0_INSTR_CACHE_SIZE | Ob01111 | 0b01111 |
| CPUO DATA CACHE SIZE | Ob01111 | 0b01111 |
| CPUO IRQLVL | 3 | 3 |
| CPU0_ITGUBLKSZ | 7 | 8 |
| CPU0_DTGUBLKSZ | 7 | 8 |
| CPU0_RAR | 1 | 1 |
| CPU0_LOCKSTEP | 0 | 0 |
| CPU0_CFGITCMSZ | 0b1001 | 0b1010 |
| CPU0_CFGDTCMSZ | 0b1001 | 0b1010 |
| CPUOMCUROMADDR | OxEOOFE | OxEOOFE |
| CPU0MCUROMVALID | 1 | 1 |
| SOCVAR | OxO | 0x0 |
| SOCREV | OxO | 0x0 |
| SOCPRTID | 0x7E0 | Ox7E0 |
| SOCIMPLID | 0x43B | 0x43B |
| IMPLVAR | OxO | 0x0 |
| IMPLREV | 0x0 | 0x0 |
| IMPLPRTID | 0x74A | 0x74A |
| IMPLID | 0x43B | 0x43B |
| INITTCMEN | Ob11 | Ob11 |
| INITPAHBEN | 1 | 1 |
| LOCKDCAIC | 0 | 0 |
| TCM MID WIDTH | 5 | 5 |
| s mid width | 5 | 6 |
| TCM ID WIDTH | 5 | 5 |
| XS_ID_WIDTH | 6 | 6 |
| S HMASTER WIDTH | 5 | 4 |
| XOM USER SIGNAL PRESENT | 0 | 0 |
| CPU0_PMC_PRESENT | 0 | 0 |
| NUMVMBANK | 2 | 2 |
| VMADDRWIDTH | 18 | 21 |
| HASCRYTO | 0 | 0 |
| HASCSS | 0 | 0 |
| LOGIC_RETENTION_PRESENT | 0 | 0 |
| NSMSCEXPRST | 0xA5A5 | 0xA5A5 |
| MPCEXPDIS | 0x5A5A | 0x5A5A |
| MSCEXPDIS | 0x5A5A | 0x5A5A |
| BRGEXPDIS | 0x5A5A | 0x5A5A |
| PERIPHPPCEXP3DIS | 0x5A5A | OxFFFE |
| PERIPHPPCEXP2DIS | 0x5A5A | 0xF000 |
| PERIPHPPCEXP1DIS | 0x5A5A | 0xFE00 |
| PERIPHPPCEXPODIS | 0x5A5A | 0x1FCC |
| MAINPPCEXP3DIS | 0x5A5A | 0x5A5A |
| MAINPPCEXP2DIS | 0x5A5A | 0x5A5A |
| MAINPPCEXP1DIS | 0x5A5A | OxFFF1 |
| MAINPPCEXPODIS | 0x5A5A | 0xBE00 |
| | | |

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| CPU0 LOCKPAHB | 1 | 1 |
|--|------------------|------------------|
| PERIPHERAL_INTERCONNECT_ARBITRATION_SCHEME CPU0 CFGPAHBZE | "round" 0b010 | "round" 0b010 |
| CPU0_INITECCEN | 0 | 0 |
| CFGMEMALIAS | 0b10000 | 0b10000 |
| CFGBIGEND | 0 | 0 |
| CPU0_CTI_PRESENT | 1 | 1 |
| ECC_PRESENT | 0 | 0 |
| BUSPROT_PRESENT | 0 | 0 |
| COLDRESET_MODE | 0 | 0 |
| CPU0CPUIDRST | 0 | 0 |
| HASCPUOIWIC | 0 | 0 |
| PDCMQCHWIDTH | 4 | 4 |

Table 3-1 : SSE-300 Render Configuration Settings

3.2.2 Subsystem static input values

The SSE-300 subsystem in AN547 has several inputs which are tied off and therefore static, at the subsystem top level. These are detailed in the below table.

| Input | Tie Off Value |
|-----------------------------|--------------------|
| CPU0_INITSVTOR ¹ | 25'h020000 |
| CPUOCFGFPU | 1'b1 |
| CPU0CFGMVE | 2'b10 |
| CPUOMPUNSDISABLE | 1'b0 |
| CPUOMPUSDISABLE | 1'b0 |
| CPUOCFGSSTCALIB | 25'h0270FF |
| CPUOCFGNSSTCALIB | 25'h0270FF |
| CPU0INITL1RSTDIS | 1'b0 |
| | Table 3-2 : Subsys |



CPU0_INITSVTOR is the value for INITSVTORORST specified in the SSE-300 TRM.

3.3 SIE-300 Components

This system uses the following SIE-300 components:

• AXI5 Memory Protection Controller.

There are 3 MPCs implemented in the FPGA and these are configured with the following block sizes:

| MPC | Block size |
|----------|------------|
| SRAM MPC | 16KB |
| QSPI MPC | 64KB |
| DDR4 MPC | 1MB |

3.4 SIE-200 Components

This system uses the following SIE-200 components:

- TrustZone AHB5 peripheral protection controller
- TrustZone AHB5 Manager security controller
- AHB5 bus matrix
- AHB5 to AHB5 synchronous bridge
- AHB5 to APB synchronous bridge
- TrustZone APB4 peripheral protection controller
- AHB5 default subordinate

3.5 CoreLink XHB-500

This system implements one CoreLink XHB-500, configured for AHB to AXI mode.

3.6 Memory Protection

The SIE-300 MPC, and SIE-200 PPC components can affect memory and I/O security management and must be configured as required for your application. See Arm[®] SIE-200 System IP Technical Reference Manual and Arm[®] CoreLink[™] SIE-300 AXI5 System IP for Embedded Technical Reference Manual.

0x5000_0000 0x6000_0000

3.7 Memory Map Overview

The following figure shows the AN547 memory map and how it relates to the Armv8-M reference memory map. The figure includes IDAU security information for memory regions.

See the Arm® CoreLink[™] SIE-200 System IP for Embedded Technical Reference Manual for more information.

| | | | | | | Reserved | 0x5000_0000 | 0x6000_0000 |
|------------------------------|--|--|---|---|---------------------------------------|---|---|---|
| | | | | | | PDM | 0x4930_D000 | 0x5930_D000 |
| | | | | | | RTC | 0x4930_C000 | 0x5930_C000 |
| | | | | | | CLCD | 0x4930_B000 | 0x5930_B000 |
| | | | | | | | 0x4930_A000 | 0x5930_A000 |
| | Arm®v8-M | | AN547 | | | Reserved | 0x4930 9000 | 0x5930 9000 |
| | Ref Memory map | | Memory map | | | UART 3 | 0x4930 8000 | 0x5930 8000 |
| | | | | | | UART Shield1 | 0x4930 7000 | 0x5930 7000 |
| · · · · · | | 0xFFFF FFFF | | 7 | | UART Shield0 | 0x4930 6000 | 0x5930 6000 |
| | | | | on | S | UART 2 | 0x4930 5000 | 0x5930 5000 |
| 0xFFFF_FFFF | | | | Š | ect | UART 1 | 0x4930_5000 | 0x5930_5000 |
| | Vendor_SYS | | Vendor_SYS | эси | Jre | UART 0 | 0x4930_4000 0x4930_3000 | 0x5930_4000 0x5930_3000 |
| | | | | re | H | FPGAIO | | |
| | | 0xE010_0000 | | Hig | g, I | I2S Audio | 0x4930_2000 | 0x5930_2000 |
| 0.5040.0000 | Private Peripheral Bus. | _ | | 5 | Lat | SCC | 0x4930_1000 | 0x5930_1000 |
| 0xE010_0000 | Local to Each CPU. | | Private Peripheral Bus | ate | enc | Reserved | 0x4930_0000 | 0x5930_0000 |
| | | 0xE000 0000 | | anc | Ϋ́Γ | I2C DDR4 EEPROM | 0x4920_9000 | 0x5920_9000 |
| | | 0x2000_0000 | DDR 4 | P | er | USER APB | 0x4920_8000 | 0x5920_8000 |
| 0xE000_0000 | | 0xD000_0000 | | erip | hd | I2C Shield1 | 0x4920_7000 | 0x5920_7000 |
| | | | DDR 4 | ohe | era | | 0x4920_6000 | 0x5920_6000 |
| | External Device | 0xC000_0000 | | ra l | R | I2C Shield0 | 0x4920_5000 | 0x5920_5000 |
| | | 0xB000_0000 | DDR 4 | Non-Secure High Latency Peripheral Regior | Secure High Latency Peripheral Region | SPI Shield1 | 0x4920_4000 | 0x5920_4000 |
| | Instruction and data accesses | 0.000_0000 | DDR 4 | oiĐ | n | SPI Shield0 | 0x4920_3000 | 0x5920_3000 |
| | performed on M-AXI | 0xA000_0000 | | 5 | | SPI ADC | 0x4920 2000 | 0x5920 2000 |
| | | | DDR 4 | | | I2C (Audio Conf) | 0x4920_2000 | 0x5920_2000 |
| | | 0x9000_0000 | | | | I2C (Touch) | 0x4920_0000 | 0x5920_0000 |
| | | 0.0000 0000 | DDR 4 | | | Reserved | 0x4320_0000 0x4810 4000 | 0x5810 4000 |
| 0x8000_0000 | External RAM | 0x8000_0000 | DDR 4 | | | U55 TIMING ADAPTER 1 | 0x4810_4000 0x4810_3000 | 0x5810_4000 0x5810_3000 |
| | Instruction and data accesses | 0x7000_0000 | DBR 4 | | | U55 TIMING ADAPTER 0 | _ | _ |
| | performed on M-AXI | 0000_0000 | DDR 4 | | | Reserved | 0x4810_2000 | 0x5810_2000 |
| 0x6000_0000 | | 0x6000_0000 | Secure High Latency | | | Subsystem Peripherals | 0x4810_0000 | 0x5810_0000 |
| | | | Peripheral Region | | | | 0x4800_0000 | 0x5800_0000 |
| | Peripheral | 0x5800_0000 | Secure Low Latency | | | | Non-Secure | Secure |
| | | 0x5000_0000 | Peripheral Region | | | | | |
| | Instruction and data accesses | 0x3000_0000 | Non-Secure High Latency | | | | | |
| | performed on P-AHB or M-AXI | 0x4800_0000 | Peripheral Region Non-Secure Low Latency | | | | 0x4800 0000 | 0x5800 0000 |
| | | | Peripheral Region | | | Reserved | 0x4180_2000 | 0x5180 2000 |
| 0x4000_0000 | | 0x4000_0000 | | | | QSPI WRITE CONFIG | 0x4180_2000 | 0x5180 1000 |
| | | 0x3880 0000 | Reserved | | | QSPI XIP CONFIG | 0x4180_1000 | 0x5180_1000 |
| | | 0x3660_0000 | QSPI (8MB) | | | Reserved | _ | |
| | | 0x3800 0000 | | | | USER APB 3 | 0x4170_4000 | 0x5170_4000 |
| | | _ | Reserved | | | USER APB 2 | 0x4170_3000 | 0x5170_3000 |
| | | 0x3200_0000 | | | | USER APB 1 | 0x4170_2000 | 0x5170_2000 |
| | | 0.0100.0000 | Internal SRAM (2 x 2MB) | Q | ~ | USER APB 0 | 0x4170_1000 | 0x5170_1000 |
| | SRAM | 0x3100_0000 | DTCM (4 x 128KB) | 1 | ě | Reserved | 0x4170_0000 | 0x5170_0000 |
| | | | D'TOWI (4 X TZOND) | | 0 | | | |
| | | 0x3000 0000 | | Sect | cure | | 0x4160_0000 | 0x5160_0000 |
| | All accesses performed on | 0x3000_0000 | Reserved | Secure | cure Lo | USB | 0x4160_0000 0x4150_0000 | 0x5150_0000 |
| | All accesses performed on DTCM or M-AXI | 0x3000_0000 0x2880_0000 | | Secure Lo | cure Low I | USB ETHERNET | | |
| | All accesses performed on DTCM or M-AXI | 0x2880_0000 | Reserved QSPI (8MB) | Secure Low L | cure Low Late | USB ETHERNET Reserved | 0x4150_0000 | 0x5150_0000 |
| | All accesses performed on DTCM or M-AXI | | QSPI (8MB) | Secure Low Late | cure Low Latenc | USB ETHERNET Reserved DMA 3 | 0x4150_0000 0x4140_0000 | 0x5150_0000 0x5140_0000 |
| | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 | | Secure Low Latency | cure Low Latency F | USB ETHERNET Reserved DMA 3 DMA 2 | 0x4150_0000 0x4140_0000 0x4120_4000 | 0x5150_0000 0x5140_0000 0x5120_4000 |
| | All accesses performed on DTCM or M-AXI | 0x2880_0000 | QSPI (8MB) | Secure Low Latency P | cure Low Latency Peri | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_3000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 |
| | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) | Secure Low Latency Perip | cure Low Latency Periphe | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_3000 0x4120_2000 0x4120_1000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_2000 |
| | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 | QSPI (8MB) Reserved | Secure Low Latency Periphe | cure Low Latency Peripheral | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_3000 0x4120_2000 0x4120_1000 0x4120_0000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_1000 0x5120_0000 |
| 0x2000_0000 - | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 | OSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) | Secure Low Latency Peripheral | Secure Low Latency Peripheral Re | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_3000 0x4120_2000 0x4120_1000 0x4120_0000 0x4110_8000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_1000 0x5120_0000 0x5110_8000 |
| 0x2000_0000 - | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) | Secure Low Latency Peripheral Re | cure Low Latency Peripheral Regi | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 2 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_3000 0x4120_2000 0x4120_1000 0x4120_0000 0x4110_8000 0x4110_7000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_1000 0x5120_1000 0x5110_8000 0x5110_7000 |
| 0x2000_0000 - | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 | OSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved | Secure Low Latency Peripheral Regio | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_2000 0x4120_2000 0x4120_0000 0x4110_0000 0x4110_7000 0x4110_6000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_0000 0x5110_0000 0x5110_7000 0x5110_6000 |
| 0x2000_0000 - | DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 | OSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) | Non-Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 2 | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_2000 0x4120_2000 0x4120_0000 0x4120_0000 0x4110_8000 0x4110_6000 0x4110_5000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_0000 0x5110_8000 0x5110_6000 0x5110_5000 |
| 0x2000_0000 - | All accesses performed on DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 | OSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 2 USER AHB 1 USER AHB 0 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_3000 0x4120_2000 0x4120_1000 0x4110_8000 0x4110_8000 0x4110_6000 0x4110_5000 0x4110_4000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_1000 0x5110_8000 0x5110_8000 0x5110_7000 0x5110_6000 0x5110_5000 0x5110_4000 |
| 0x2000_0000 - | DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) ITCM (512KB) | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 2 USER AHB 1 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_2000 0x4120_2000 0x4120_0000 0x4110_8000 0x4110_6000 0x4110_5000 0x4110_5000 0x4110_3000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_2000 0x5120_1000 0x5110_8000 0x5110_8000 0x5110_6000 0x5110_6000 0x5110_4000 0x5110_4000 |
| 0x2000_0000 - | DTCM or M-AXI CODE All accesses performed on | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 0x1100_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 3 USER AHB 1 USER AHB 1 USER AHB 0 GPIO 3 GPIO 2 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_3000 0x4120_2000 0x4120_0000 0x4110_0000 0x4110_7000 0x4110_5000 0x4110_5000 0x4110_3000 0x4110_2000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_1000 0x5120_0000 0x5110_8000 0x5110_7000 0x5110_5000 0x5110_4000 0x5110_3000 0x5110_3000 |
| 0x2000_0000 · | DTCM or M-AXI | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 0x1100_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) ITCM (512KB) Reserved | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 3 USER AHB 1 USER AHB 1 USER AHB 0 GPIO 3 GPIO 2 GPIO 1 | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_2000 0x4120_2000 0x4120_0000 0x4110_0000 0x4110_6000 0x4110_6000 0x4110_4000 0x4110_4000 0x4110_2000 0x4110_2000 0x4110_1000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_0000 0x5110_0000 0x5110_6000 0x5110_6000 0x5110_4000 0x5110_4000 0x5110_2000 0x5110_2000 |
| 0x2000_0000 - | DTCM or M-AXI CODE All accesses performed on | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 0x1100_0000 0x1000_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) ITCM (512KB) | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 3 USER AHB 1 USER AHB 1 USER AHB 0 GPIO 3 GPIO 2 GPIO 1 GPIO 0 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_3000 0x4120_2000 0x4120_0000 0x4110_0000 0x4110_7000 0x4110_5000 0x4110_5000 0x4110_3000 0x4110_2000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_1000 0x5120_0000 0x5110_8000 0x5110_7000 0x5110_5000 0x5110_4000 0x5110_3000 0x5110_3000 |
| 0x2000_0000 | DTCM or M-AXI CODE All accesses performed on | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 0x1100_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) ITCM (512KB) Reserved | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 3 USER AHB 1 USER AHB 1 USER AHB 0 GPIO 3 GPIO 2 GPIO 1 GPIO 0 Reserved | 0x4150_0000 0x4140_0000 0x4120_4000 0x4120_2000 0x4120_2000 0x4120_0000 0x4110_0000 0x4110_6000 0x4110_6000 0x4110_4000 0x4110_4000 0x4110_2000 0x4110_2000 0x4110_1000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_2000 0x5120_2000 0x5120_0000 0x5110_0000 0x5110_6000 0x5110_6000 0x5110_4000 0x5110_4000 0x5110_2000 0x5110_2000 |
| 0x2000_0000 - 0x0000_0000 | DTCM or M-AXI CODE All accesses performed on | 0x2880_0000 0x2800_0000 0x2200_0000 0x2100_0000 0x2000_0000 0x1E00_0000 0x1100_0000 0x1000_0000 | QSPI (8MB) Reserved Internal SRAM (2 x 2MB) DTCM (4 x 128KB) Reserved FPGA SRAM (2MB) ITCM (512KB) Reserved FPGA SRAM (2MB) | Secure Low Latency Peripheral Region | cure Low Latency Peripheral Region | USB ETHERNET Reserved DMA 3 DMA 2 DMA 1 DMA 0 Reserved USER AHB 3 USER AHB 3 USER AHB 1 USER AHB 1 USER AHB 0 GPIO 3 GPIO 2 GPIO 1 GPIO 0 | 0x4150_0000 0x4140_0000 0x4120_3000 0x4120_3000 0x4120_2000 0x4120_0000 0x4110_8000 0x4110_8000 0x4110_6000 0x4110_5000 0x4110_4000 0x4110_3000 0x4110_2000 0x4110_1000 0x4110_0000 | 0x5150_0000 0x5140_0000 0x5120_4000 0x5120_3000 0x5120_1000 0x5120_1000 0x5110_8000 0x5110_8000 0x5110_6000 0x5110_6000 0x5110_4000 0x5110_3000 0x5110_3000 0x5110_1000 |

Figure 3-2: Memory Map

The following table shows the memory map.

| RO | Ad | dress | | Region | | Alias | IDAU | Region V | alues |
|---------|-------------|-------------|--------|--------------------|--|----------------|----------|------------|------------|
| W ID | From | То | Size | Name | Description | with Row ID | Security | IDAU ID | NSC |
| 1 | 0x0000_0000 | 0x0007_FFFF | 512KB | Code | ITCM ³ | 5 | | | |
| 2 | 0x0008_0000 | 0x00FF_FFFF | 15.5MB | Reserved | Reserved | | NG | 0 | 0 |
| 3 | 0x0100_0000 | 0x011F_FFFF | 2MB | Code | FPGA SRAM (2MB) ¹ | 7 | NS | 0 | 0 |
| 4 | 0x0120_0000 | 0x0FFF_FFFF | 238MB | Reserved | Reserved | | | | |
| 5 | 0x1000_0000 | 0x100F_FFFF | 512KB | Code | ITCM ³ | 1 | - | | |
| 6 | 0x1010_0000 | 0x10FF_FFFF | 15.5MB | Reserved | Reserved | | - S | 1 | CODE |
| 7 | 0x1100_0000 | Ox111F_FFFF | 2MB | Code | FPGA SRAM (2MB) ¹ | 3 | - | Ţ | NSC |
| 8 | 0x1120_0000 | Ox1FFF_FFFF | 238MB | Reserved | Reserved | | | | |
| 9 | 0x2000_0000 | 0x2007_FFFF | 512KB | SRAM | DTCM (4 x banks of 128KB) ³ | 15 | NS | | |
| 10 | 0x2008_0000 | 0x20FF_FFFF | 15.5MB | Reserved | Reserved | | | | |
| 11 | 0x2100_0000 | 0x213F_FFFF | 4MB | SRAM | Internal SRAM Area (SSE- 300 implements 2x2MB) ³ | 17 | | | |
| 12 | 0x2140_0000 | 0x27FF_FFFF | 108MB | Reserved | Reserved | | | | |
| 13 | 0x2800_0000 | 0x287F_FFFF | 8MB | SRAM | QSPI (8MB) ¹ | 19 | | | |
| 14 | 0x2880_0000 | 0x2FFF_FFFF | 120MB | Reserved | Reserved | | | | |
| 15 | 0x3000_0000 | 0x303F_FFFF | 512KB | SRAM | DTCM (4 x banks of 128KB) ³ | 9 | S | 3 | RAM NSC |
| 16 | 0x3040_0000 | 0x30FF_FFFF | 15.5MB | Reserved | Reserved | | | | |
| 17 | 0x3100_0000 | 0x313F_FFFF | 4MB | SRAM | Internal SRAM Area (SSE- 300 implements 2x2MB) ³ | 11 | | | |
| 18 | 0x3140_0000 | 0x37FF_FFFF | 108MB | Reserved | Reserved | | | | |
| 19 | 0x3800_0000 | 0x387F_FFFF | 8MB | SRAM | QSPI (8MB) ¹ | 13 | | | |
| 20 | 0x3880_0000 | 0x3FFF_FFFF | 120MB | Reserved | Reserved | | | | |
| 21 | 0x4000_0000 | 0x47FF_FFFF | 128MB | Peripheral | Non-Secure Low Latency Peripheral Region | 23 | NS | 4 | 0 |
| 22 | 0x4800_0000 | 0x4FFF_FFFF | 128MB | Peripheral | Non-Secure High Latency Peripheral Region | 24 | NS | 4 | 0 |
| 23 | 0x5000_0000 | 0x57FF_FFFF | 128MB | Peripheral | Secure Low Latency Peripheral Region | 21 | S | 5 | 0 |
| 24 | 0x5800_0000 | Ox5FFF_FFFF | 128MB | Peripheral | Secure High Latency Peripheral Region | 22 | S | 5 | 0 |
| 25 | 0x6000_0000 | 0x6FFF_FFFF | 256MB | External RAM | DDR4 ¹ | | NS | 6 | 0 |
| 26 | 0x7000_0000 | 0x7FFF_FFFF | 256MB | External RAM | DDR4 ¹ | | S | 7 | 0 |
| 27 | 0x8000_0000 | 0x8FFF_FFFF | 256MB | External device | DDR4 ¹ | | NS | 8 | 0 |

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| RO | Ad | Address | | Region | | Alias | IDAU | Region Va | alues |
|---------|-------------|-------------|-------|--------------------|---|----------------|----------|------------|-------|
| W ID | From | То | Size | Name | Description | with Row ID | Security | IDAU ID | NSC |
| 28 | 0x9000_0000 | 0x9FFF_FFFF | 256MB | External device | DDR4 ¹ | | S | 9 | 0 |
| 29 | 0xA000_0000 | OxAFFF_FFFF | 256MB | External device | DDR4 ¹ | | NS | А | 0 |
| 30 | 0xB000_0000 | OxBFFF_FFFF | 256MB | External device | DDR4 ¹ | | S | В | 0 |
| 31 | 0xC000_0000 | 0xCFFF_FFFF | 256MB | External device | DDR4 ¹ | | NS | С | 0 |
| 32 | 0xD000_0000 | 0xDFFF_FFFF | 256MB | External device | DDR4 ¹ | | S | D | 0 |
| 33 | 0xE000_0000 | 0xE00F_FFFF | 1MB | EPPB | External Private Peripheral Bus | | | Exempt | |
| 34 | 0xE010_0000 | 0xE01F_FFFF | 1MB | Vendor_SYS | Reserved | | NS | E | 0 |
| 35 | 0xE020_0000 | OxEFFF_FFFF | 254MB | Vendor_SYS | Maps to HMSTEXPPILL Expansion Interface ² | | NS | E | 0 |
| 36 | 0xF000_0000 | 0xF00F_FFFF | 1MB | Vendor_SYS | Reserved | | | Exempt | |
| 37 | 0xF010_0000 | 0xF01F_FFFF | 1MB | Vendor_SYS | Reserved | | S | F | 0 |
| 38 | 0xF020_0000 | OxFFFF_FFFF | 254MB | Vendor_SYS | Maps to HMSTEXPPILL Expansion Interface ² | | S | F | 0 |

Table 3-3: Memory map overview

This table outlines the main FPGA memories and their positions within the memory map.

Note¹: Security Access is controlled by MPC.

Note²: Accesses to these addresses results in an AHB5 error response.

Note³ : For security settings, control and features please refer to the Arm® Corstone[™] SSE-300 Documentation.

3.8 Expansion System peripherals

All FPGA peripherals are mapped to four areas of the memory map. The addresses and interfaces to access the four regions are:

Non-secure Low Latency region:

- 0x4000_0000 0x47FF_FFF
- Manager Peripheral Expansion Low Latency Interface HMSTEXPPILL

Non-secure High Latency region:

- 0x4800_0000 0x4FFF_FFF
- Manager Peripheral Expansion High Latency Interface HMSTEXPPIHL

Secure Low Latency region:

- 0x5000_0000 0x57FF_FFF
- Manager Peripheral Expansion Low Latency Interface HMSTEXPPILL

Secure High Latency region:

- 0x5800_0000 0x5FFF_FFF
- Manager Peripheral Expansion High Latency Interface HMSTEXPPIHL

To support TrustZone-Arm v8M and allow Software to map these peripherals to Secure or Non-secure address space, all peripherals are mapped twice and either an APB PPC or an AHB PPC gates access to these peripherals.

3.8.1 Manager Peripheral Expansion Low Latency Interface Memory Map (HMSTEXPPILL)

The following table shows the FPGA peripheral mapping to the Non-secure Low Latency region

| ROW | Add | ress | C: | Description | Alias with | Deut |
|-----|-------------|-------------|------|-----------------------|------------|------|
| ID | From | То | Size | Description | ROW ID | Port |
| 1 | 0x4000_0000 | 0x400F_FFFF | | Subsystem peripherals | | |
| 2 | 0x4010_0000 | 0x410F_FFFF | | Reserved | | |
| 3 | 0x4110_0000 | 0x4110_0FFF | 4KB | GPIO 0 | 30 | |
| 4 | 0x4110_1000 | 0x4110_1FFF | 4KB | GPIO 1 | 31 | |
| 5 | 0x4110_2000 | 0x4110_2FFF | 4KB | GPIO 2 | 32 | |
| 6 | 0x4110_3000 | 0x4110_3FFF | 4KB | GPIO 3 | 33 | |
| 7 | 0x4110_4000 | 0x4110_4FFF | 4KB | AHB USER 0 | 34 | AHB |
| 8 | 0x4110_5000 | 0x4110_5FFF | 4KB | AHB USER 1 | 35 | |
| 9 | 0x4110_6000 | 0x4110_6FFF | 4KB | AHB USER 2 | 36 | |
| 10 | 0x4110_7000 | 0x4110_7FFF | 4KB | AHB USER 3 | 37 | |
| 11 | 0x4110_8000 | Ox411F_FFFF | | Reserved | | |
| 12 | 0x4120_0000 | 0x4120_0FFF | | Reserved | | |
| 13 | 0x4120_1000 | 0x4120_1FFF | 4KB | DMA 1 | 40 | |
| 14 | 0x4120_2000 | 0x4120_2FFF | 4KB | DMA 2 | 41 | AHB |
| 15 | 0x4120_3000 | 0x4120_3FFF | 4KB | DMA 3 | 42 | |
| 16 | 0x4120_4000 | 0x413F_FFFF | | Reserved | | |
| 17 | 0x4140_0000 | Ox414F_FFFF | 1MB | Ethernet | 44 | |
| 18 | 0x4150_0000 | 0x415F_FFFF | 1MB | USB | 45 | AHB |

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| ROW | Add | ress | C: | Description | Alias with | Dout |
|-----|-------------|-------------|------|-------------|------------|-------|
| ID | From | То | Size | Description | ROW ID | Port |
| 19 | 0x4160_0000 | 0x416F_FFFF | | Reserved | | |
| 20 | 0x4170_0000 | 0x4170_0FFF | 4KB | User APB0 | 47 | |
| 21 | 0x4170_1000 | 0x4170_1FFF | 4KB | User APB1 | 48 | APB |
| 22 | 0x4170_2000 | 0x4170_2FFF | 4KB | User APB2 | 49 | (Mem) |
| 23 | 0x4170_3000 | 0x4170_3FFF | 4KB | User APB3 | 50 | |
| 24 | 0x4170_4000 | 0x417F_FFFF | | Reserved | | |
| 25 | 0x4180_0000 | 0x4180_0FFF | 4KB | QSPI Config | 52 | |
| 26 | 0x4180_1000 | 0x4180_1FFF | 4KB | QSPI Write | 53 | AHB |
| 27 | 0x4180_2000 | 0x47FF_FFFF | | Reserved | | |
| | | | | | | - |

Table 3-2: MSTEXPPILL Non-secure Peripheral Map

The following table shows the FPGA peripheral mapping to the Secure Low Latency region

| ROW | Add | ress | Size | Description | Alias with | Port |
|-----|-------------|-------------|------|--|------------|-------|
| ID | From | То | Size | Description | ROW ID | Port |
| 28 | 0x5000_0000 | 0x500F_FFFF | | Subsystem peripherals | | |
| 29 | 0x5010_0000 | 0x510F_FFFF | | Reserved | | |
| 30 | 0x5110_0000 | 0x5110_0FFF | 4KB | GPIO 0 | 3 | |
| 31 | 0x5110_1000 | 0x5110_1FFF | 4KB | GPIO 1 | 4 | |
| 32 | 0x5110_2000 | 0x5110_2FFF | 4KB | GPIO 2 | 5 | |
| 33 | 0x5110_3000 | 0x5110_3FFF | 4KB | GPIO 3 | 6 | AHB |
| 34 | 0x5110_4000 | 0x5110_4FFF | 4KB | AHB USER 0 | 7 | АПБ |
| 35 | 0x5110_5000 | 0x5110_5FFF | 4KB | AHB USER 1 | 8 | |
| 36 | 0x5110_6000 | 0x5110_6FFF | 4KB | AHB USER 2 | 9 | |
| 37 | 0x5110_7000 | 0x5110_7FFF | 4KB | AHB USER 3 | 10 | |
| 38 | 0x5110_8000 | 0x511F_FFFF | | Reserved | | |
| 39 | 0x5120_0000 | 0x5120_0FFF | | Reserved | | |
| 40 | 0x5120_1000 | 0x5120_1FFF | 4KB | DMA 1 | 13 | |
| 41 | 0x5120_2000 | 0x5120_2FFF | 4KB | DMA 2 | 14 | AHB |
| 42 | 0x5120_3000 | 0x5120_3FFF | 4KB | DMA 3 | 15 | |
| 43 | 0x5120_4000 | 0x513F_FFFF | | Reserved | | |
| 44 | 0x5140_0000 | 0x514F_FFFF | 1M | Ethernet | 17 | |
| 45 | 0x5150_0000 | 0x515F_FFFF | 1M | USB | 18 | AHB |
| 46 | 0x5160_0000 | 0x516F_FFFF | | Reserved | | |
| 47 | 0x5170_0000 | 0x5170_0FFF | 4KB | User APB0 | 20 | |
| 48 | 0x5170_1000 | 0x5170_1FFF | 4KB | User APB1 | 21 | APB |
| 49 | 0x5170_2000 | 0x5170_2FFF | 4KB | User APB2 | 22 | (Mem) |
| 50 | 0x5170_3000 | 0x5170_3FFF | 4KB | User APB3 | 23 | |
| 51 | 0x5170_4000 | 0x517F_FFFF | | Reserved | | |
| 52 | 0x5180_0000 | 0x5180_0FFF | 4KB | QSPI Config | 25 | |
| 53 | 0x5180_1000 | 0x5180_1FFF | 4KB | QSPI Write | 26 | AHB |
| 54 | 0x5180_2000 | 0x56FF_FFFF | | Reserved | | |
| 55 | 0x5700_0000 | 0x5700_0FFF | 4KB | SRAM Memory Protection Controller (MPC) | | APB |
| 56 | 0x5700_1000 | 0x5700_1FFF | 4KB | QSPI Memory Protection Controller (MPC) | | (Mem) |

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| ROW | Add | ress | Size | Description | Alias with | Port |
|-----|-------------|-------------|------|--|-----------------|------|
| ID | From | То | Size | Description | ROW ID | Port |
| 57 | 0x5700_2000 | 0x5700_2FFF | 4KB | DDR4 Memory Protection Controller (MPC) | | |
| 58 | 0x5700_3000 | 0x57FF_FFFF | | Reserved | | |
| | | | | Table 3-3: MSTEXPPILL Secu | re Peripheral M | 1ap |



Reserved regions respond with RAZ/WI when accessed.

3.8.2 MSTEXPPIHL Peripheral Map

| ROW ID | | ress T- | Size | Description | Alias with ROW ID | Port |
|-----------|-----------------|-------------|-------|--------------------------------|----------------------|------|
| שו | From | То | Non-S | ecure Region | KOWID | |
| 1 | 0x4800 0000 | 0x480F_FFFF | | Subsystem peripherals | | |
| 2 | 0x4810 0000 | | | Reserved | | |
| 3 | 0x4810_2000 | 0x4810_2FFF | 4KB | Ethos - U55 APB | 31 | |
| 4 | 0x4810_3000 | 0x4810_31FF | 0.5KB | U55 timing adapter 0 APB | 32 | APB0 |
| 5 | 0x4810_3200 | 0x4810_33FF | 0.5KB | U55 timing adapter 1 APB | 33 | |
| 6 | 0x4810_3400 | 0x491F_FFFF | | Reserved | | |
| 7 | 0x4920_0000 | 0x4920_0FFF | 4KB | FPGA - SBCon I2C (Touch) | 35 | |
| 8 | 0x4920_1000 | 0x4920_1FFF | 4KB | FPGA - SBCon I2C (Audio Conf) | 36 | |
| 9 | 0x4920_2000 | 0x4920_2FFF | 4KB | FPGA - PL022 (SPI ADC) | 37 | |
| 10 | 0x4920_3000 | 0x4920_3FFF | 4KB | FPGA - PL022 (SPI Shield0) | 38 | |
| 11 | 0x4920_4000 | 0x4920_4FFF | 4KB | FPGA - PL022 (SPI Shield1) | 39 | APB0 |
| 12 | 0x4920_5000 | 0x4920_5FFF | 4KB | SBCon (I2C - ShieldO) | 40 | |
| 13 | 0x4920_6000 | 0x4920_6FFF | 4KB | SBCon (I2C – Shield1) | 41 | |
| 14 | 0x4920_7000 | 0x4920_7FFF | 4KB | USER APB | 42 | |
| 15 | 0x4920_8000 | 0x4920_8FFF | 4KB | FPGA - SBCon I2C (DDR4 EEPROM) | 43 | |
| 16 | 0x4920_9000 | 0x492F_FFFF | | Reserved | | |
| 17 | 0x4930_0000 | 0x4930_0FFF | 4KB | FPGA - SCC registers | 45 | |
| 18 | 0x4930_1000 | 0x4930_1FFF | 4KB | FPGA - I2S (Audio) | 46 | |
| 19 | 0x4930_2000 | 0x4930_2FFF | 4KB | FPGA - IO (System Ctrl + I/O) | 47 | |
| 20 | 0x4930_3000 | 0x4930_3FFF | 4KB | UARTO - UART_F[0] | 48 | |
| 21 | 0x4930_4000 | 0x4930_4FFF | 4KB | UART1 - UART_F[1] | 49 | |
| 22 | 0x4930_5000 | 0x4930_5FFF | 4KB | UART2 - UART_F[2] | 50 | APB1 |
| 23 | 0x4930_6000 | 0x4930_6FFF | 4KB | UART3 - UART Shield O | 51 | APDI |
| 24 | 0x4930_7000 | 0x4930_7FFF | 4KB | UART4 - UART Shield 1 | 52 | |
| 25 | 0x4930_8000 | 0x4930_8FFF | 4KB | UART5 - UART_F[3] | 53 | |
| 26 | 0x4930_9000 | 0x4930_9FFF | 4KB | Reserved | | |
| 27 | 0x4930_A000 | 0x4930_AFFF | 4KB | CLCD Config Reg | 55 | |
| 28 | 0x4930_B000 | 0x4930_BFFF | 4KB | RTC | 56 | |
| 29 | 0x4930_C000 | 0x4FFF_FFFF | | Reserved | | |

Table 3-4: MSTEXPPIHL Non-secure Peripheral Map

| ROW | Add | lress | Size | Description | Alias with | Port |
|-----|-------------|-------------|-------|---------------------------------------|------------|------|
| ID | From | То | | · · · · · · · · · · · · · · · · · · · | ROW ID | PUIL |
| | | | Sec | ure Region | | |
| 30 | 0x5800_0000 | 0x5810_1FFF | | Subsystem peripherals | | |
| 31 | 0x5810_2000 | 0x5810_2FFF | 4KB | Ethos - U55 APB | 3 | |
| 32 | 0x5810_3000 | 0x5810_31FF | 0.5KB | U55 timing adapter O APB | 4 | APB0 |
| 33 | 0x5810_3200 | 0x5810_33FF | 0.5KB | U55 timing adapter 1 APB | 5 | |
| 34 | 0x5810_3400 | 0x591F_FFFF | | Reserved | | |
| 35 | 0x5920_0000 | 0x5920_0FFF | 4KB | FPGA - SBCon I2C (Touch) | 7 | |
| 36 | 0x5920_1000 | 0x5920_1FFF | 4KB | FPGA - SBCon I2C (Audio Conf) | 8 | |
| 37 | 0x5920_2000 | 0x5920_2FFF | 4KB | FPGA - PL022 (SPI ADC) | 9 | |
| 38 | 0x5920_3000 | 0x5920_3FFF | 4KB | FPGA - PL022 (SPI ShieldO) | 10 | |
| 39 | 0x5920_4000 | 0x5920_4FFF | 4KB | FPGA - PL022 (SPI Shield1) | 11 | APB0 |
| 40 | 0x5920_5000 | 0x5920_5FFF | 4KB | SBCon (I2C - ShieldO) | 12 | |
| 41 | 0x5920_6000 | 0x5920_6FFF | 4KB | SBCon (I2C - Shield1) | 13 | |
| 42 | 0x5920_7000 | 0x5920_7FFF | 4KB | USER APB | 14 | |
| 43 | 0x5920_8000 | 0x5920_8FFF | 4KB | FPGA - SBCon I2C (DDR4 EEPROM) | 15 | |
| 44 | 0x5920_9000 | 0x592F_FFFF | | Reserved | | |
| 45 | 0x5930_0000 | 0x5930_0FFF | 4KB | FPGA - SCC registers | 17 | |
| 46 | 0x5930_1000 | 0x5930_1FFF | 4KB | FPGA - I2S (Audio) | 18 | |
| 47 | 0x5930_2000 | 0x5930_2FFF | 4KB | FPGA - IO (System Ctrl + I/O) | 19 | |
| 48 | 0x5930_3000 | 0x5930_3FFF | 4KB | UARTO - UART_F[0] | 20 | |
| 49 | 0x5930_4000 | 0x5930_4FFF | 4KB | UART1 - UART_F[1] | 21 | |
| 50 | 0x5930_5000 | 0x5930_5FFF | 4KB | UART2 - UART_F[2] | 22 | |
| 51 | 0x5930_6000 | 0x5930_6FFF | 4KB | UART3 - UART Shield O | 23 | APB1 |
| 52 | 0x5930_7000 | 0x5930_7FFF | 4KB | UART4 - UART Shield 1 | 24 | |
| 53 | 0x5930_8000 | 0x5930_8FFF | 4KB | UART5 - UART_F[3] | 25 | |
| 54 | 0x5930_9000 | 0x5930_9FFF | 4KB | Reserved | | |
| 55 | 0x5930_A000 | 0x5930_AFFF | 4KB | CLCD Config Reg | 27 | |
| 56 | 0x5930_B000 | 0x5930_BFFF | 4KB | RTC | 28 | |
| 57 | 0x5930_C000 | 0x5FFF_FFFF | | Reserved | | |

Table 3-5: MSTEXPPIHL Secure Peripheral Map

<u>Note</u>

Reserved regions respond with RAZ/WI when accessed.

3.9 FPGA Utilization

This application note is designed for MPS3 board. The board will use a a Xilinx Kintex Ultrascale XCKU115 FPGA. The FPGA features up to 8MB BRAM (2160 BlocRAM tiles) and up to 663360 LUTs. Full part number: **XCKU115-FLVB1760-1-C**.

3.9.1 Total design utilization

The following table shows the total number of LUTs and BRAMs currently used in the provided image.

| Site Type | Used | Util% | |
|---------------|--------|-------|--|
| LUTs | 270540 | 40 | |
| BlockRAM Tile | 1851 | 86 | |

Note : These numbers relate to the complete image, not individual IP blocks. The numbers must not be used to infer IP size, or the relative sizes of different IP blocks, because the implementation and system design can significantly differ.

4 Programmers Model

This programmers model is supplemental to the CMSDK, SIE-200 and SIE-300 documentation which covers many of the included components in more detail. The connectivity of the system is shown in MPS3 System Overview Diagram.

4.1 ITCM

The primary boot memory is an ITCM which is implemented with 512KB of FPGA SRAM connected to the ITCM interface of the Cortex-M55 inside the subsystem.

- Size: 512KB FPGA SRAM
- Address Range: 0x0000_0000 0x0007_FFFF
- Alias Range: 0x1000_0000 0x1007_FFFF

4.2 FPGA SRAM

The code memory is extended with 2MB of internal FPGA SRAM.

- Size: 2MB FPGA SRAM
- Address Range: 0x0100_0000 0x011F_FFFF
- Alias Range: 0x1100_0000 0x111F_FFFF

4.3 **DTCM**

The primary data memory is provided by DTCM made up of 4 banks, each implemented as 128KB of internal FPGA SRAM connected to the 4 DTCM interfaces of the Cortex-M55 inside the subsystem.

- Size: 4 x 128KB FPGA SRAM
- Address Range: 0x2000_0000 0x2007_FFFF
- Alias Range: 0x3000_0000 0x3007_FFFF

4.4 QSPI

The SMM provides 8MB of external Flash memory which is accessed through a QSPI interface.

- Size: 8MB fitted
- Address Range: 0x2800_0000 0x287F_FFFF
- Alias Range: 0x3800_0000 0x387F_FFFF

4.5 DDR4

The SMM provides access to 2GB of External DDR4 memory through the DDR4 controller.

- Size: 2GB DDR4 (4GB fitted only 2GB accessible)
- Address Range: 0x6000_0000 0xDFFF_FFF

4.6 AHB GPIO

The SMM uses four CMSDK AHB GPIO blocks, each providing 16 bits of I/O. These are connected to the two Arduino compatible headers shield 0 and 1 as follows:

| Shield | GPIO |
|----------------|-------------|
| SH0_IO [15:0] | GPIO0[15:0] |
| SH0_IO [17:16] | GPIO2[1:0] |
| SH1_IO [15:0] | GPIO1[15:0] |
| SH1_IO [17:16] | GPIO2[3:2] |

Table 4-1: GPIO Mapping

The GPIO alternative function lines select whether peripherals or GPIOs are available on each pin. See **Shield Support Section** for mappings.

4.7 SPI

The SMM implements three PL022 SPI modules:

- One general purpose SPI module (SPI ADC) is used for communication with an onboard ADC. The analog pins of the Shield headers are connected to the input channels of the ADC.
- Two general purpose SPI modules connect to the Shield headers and provide an SPI interface on each header. These are alt-functions on the GPIO ports. See **Shield Support Section** for mappings.

4.8 SBCon (I²C)

The SMM implements five SBCon serial modules:

- One SBCon module for use by the Color LCD touch interface.
- One SBCon module to configure the audio controller.
- Two general purpose SBCon modules that connect to ShieldO and Shield1 and provide an I²C interface on each header. These are alt-functions on the GPIO ports. See Shield Support Section for mappings.
- One SBCon module is used to read EEPROM from DDR4 SODIMM.

The selftest software provided with the MPS3 includes example code for the color LCD module control and audio interfaces.

The following table lists the control registers for the two-wire SBCon in offset order from the base memory address. For example, the Touchscreen SBCon non-secure base address is 0x4920_0000 and the secure base address is 0x5920_0000.

| | | - | |
|---------|-------------|--------|--------------------------|
| Address | Name | Access | Description |
| 0x000 | SB_CONTROL | Read | Read serial control |
| | | | bits: |
| | | | Bit [0] is SCL |
| | | | Bit [1] is SDA |
| 0x000 | SB_CONTROLS | Write | Set serial control bits: |
| | | | Bit [0] is SCL |
| | | | Bit [1] is SDA |
| 0x004 | SB_CONTROLC | Write | Clear serial control |
| | | | bits: |
| | | | Bit [0] is SCL |
| | | | Bit [1] is SDA |
| | | | Table 4 2 SDC on D |

Table 4-2 SBCon Register Map

4.9 UART

The SMM implements six CMSDK UARTs:

- UART 0 FPGA_UARTO
- UART 1 FPGA_UART1
- UART 2 FPGA_UART2
- UART 3 Shield 0
- UART 4 Shield 1
- UART 5 FPGA_UART3

UART 3 and 4 are alt-functions on the GPIO ports. See Shield Support for mappings.

4.10 Color LCD parallel interface

The color LCD module has two interfaces:

- Parallel bus for sending image data to the LCD.
- I²C to transfer data input from the touch screen.

This is a custom peripheral that provides an interface to a STMicroelectronics STMPE811QTR Port Expander with Advanced Touch Screen Controller on the Keil MCBSTM32C display board. See MCBQVGA-TS-Display-v12 – Keil MCBSTM32F200 display board schematic. The Keil display board contains an AM240320LG display panel and uses a Himax HX8347-D LCD controller.

The selftest software provided with the MPS3 includes drivers and example code for both interfaces.

The following table lists CLCD control and data registers in offset order from the base memory address.

The CLCD non-secure base address is 0x4930A000, the secure base address is 0x5930A000.

| Address | Name | Туре | Information |
|---------|----------|--|---|
| 0x000 | CHAR_COM | Write command, read busy status. | A write to this address causes a write to the LCD command register. A read from this address causes a read from the LCD busy register. |
| 0x004 | CHAR_DAT | Write data RAM, Read data RAM. | A write to this address causes a write to the LCD data register. A read from this address causes a read from the LCD data register. |
| 0x008 | CHAR_RD | Captured data from an earlier read command | Bits [31:8] : Reserved. Bits [7:0] : contain the data from last request read, valid only when bit 0 is set in CHAR_RAW. |

| Address | Name | Туре | Information |
|---------|-----------|---|--|
| 0x00C | CHAR_RAW | Write to reset access complete flag Read to determine if data in CHAR_RD is valid | Bits [31:1] : Reserved Bit [0] : indicates Access Complete (write O to clear). The bit is set if read data is valid. |
| 0x010 | CHAR_MASK | Write interrupt mask | Set bit 0 to 0b1 to enable Access Complete to generate an interrupt. |
| 0x014 | CHAR_STAT | Read status | Bits [31:1] : Reserved |
| | | | Bit [0] : is the state of Access Complete ANDed with the CHAR_MASK. |
| 0x04C | CHAR_MISC | Miscellaneous Control | Bit Field Description : Bits [31:7] : Reserved Bit [6] : CLCD_BL Bit [5] : CLCD_RD Bit [4] : CLCD_RS Bit [3] : CLCD_RESET Bit [2] : RESERVED Bit [1] : CLCD_WR Bit [0] : CLCD_CS |

 Table 4-3: LCD control and data registers

4.11 Ethernet

The SMM design connects to an SMSC LAN9220 device through a static memory interface.

The selftest software includes example code for an internal loopback operation.

4.12 USB

The SMM design connects to a Hi-Speed USB OTG controller (ISP1763) device through a static memory interface.

The selftest software includes example code for an internal loopback operation.

4.13 RTC

The SMM uses PL031 PrimeCell Real Time Clock Controller. A counter in the Controller is incremented every second. The RTC can therefore be used as a basic alarm function or long timebase counter.

4.14 Audio I²S

The I²S interface supports transfer of digital audio to and from the Audio CODEC.

The following table shows the register memory map for I²S Audio registers in address offset order from the base memory address. The I2S non-secure base address is 0x49301000, the secure base address is 0x59301000.

| 0x000 CONTROL Control Register Bits [31:18] Reserved Bit [17] Audio codec reset control (output pin) Bit [16] FIFO reset Bit [15] Reserved Bits [14:12] Rx Buffer IRQ Water Level - Default 2 (IRQ triggers when less than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [11:1] Reserved Bit [2] Rx Enable Bit [2] Rx Enable Bit [1] Tx Interrupt Enable Bit [2] Rx Buffer Full Bit [3] Tx Buffer Full Bit [2] Tx Buffer Full Bit [2] Tx Buffer Alert (Depends on Water level) Ox008 ERROR Error Status Register | Offset | Name | Description | |
|--|--------|----------|--|---|
| Bit [17] Audio codec reset control (output pin) Bit [16] FIFO reset Bit [15] Reserved Bits [14:12] Rx Buffer IRQ Water Level - Default 2 (IRQ triggers when less than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [11] Reserved Bit [2] Rx Enable Bit [2] Rx Enable Bit [1] Tx Interrupt Enable Bit [2] Tx Enable Bit [3] Rx Buffer Full Bit [3] Tx Buffer Full Bit [2] Tx Buffer Al | 0x000 | CONTROL | Control Regist | ler |
| Bit [16] FIFO reset Bit [15] Reserved Bits [14:12] Rx Buffer IRQ Water Level - Default 2 (IRQ triggers when less than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] Rx Enable Bits [10:8] Rx Enable Bit [2] Rx Enable Bit [1] Tx Interrupt Enable Bits [31:6] Reserved Bits [31:6] Reserved Bit [2] Tx Buffer Full Bit [2] Tx Buffer Full Bit [2] Tx Buffer Alert (Depends on Water level) DX008 ERROR Error Status Register Bits [31:2] </td <td></td> <td></td> <td>Bits [31:18]</td> <td>Reserved</td> | | | Bits [31:18] | Reserved |
| Bit [15]ReservedBits [14:12]Rx Buffer IRQ Water Level - Default 2 (IRQ triggers when less than two-word space is available)Bits [11]ReservedBits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [31:6]Rx Interrupt EnableBit [2]Rx Buffer EnableBit [2]Rx EnableOx004STATUSStatus Register Bits [31:6]Bits [31:6]ReservedBit [4]Rx Buffer FullBit [2]Tx Buffer FullBit [2]Tx Buffer Alert (Depends on Water level)Ox004ERRORError Status Register Bits [31:2]Bits [31:2]ReservedBit [1]Rx overrun. Set this bit to clear.Ox005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10]Bits [21:1]ReservedBits [21:1]ReservedBits [21:1]ReservedBits [21:1]ReservedBits [21:1]Reserved <tr< td=""><td></td><td></td><td>Bit [17]</td><td>Audio codec reset control (output pin)</td></tr<> | | | Bit [17] | Audio codec reset control (output pin) |
| Bits [14:12] Rx Buffer IRQ Water Level - Default 2 (IRQ triggers when less than two-word space is available) Bit [11] Reserved Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available) Bits [10:8] Rx Interrupt Enable Bit [2] Rx Enable Bit [1] Tx Interrupt Enable Bit [0] Tx Enable Ox004 STATUS Status Register Bits [31:6] Bits [31:1] Rx Buffer Full Bit [2] Tx Buffer Full Bit [2] Tx Buffer IRPty Bit [1] Rx Buffer Alert (Depends on Water level) Ox008 ERROR Error Status Register Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. | | | Bit [16] | FIFO reset |
| two-word space is available)Bit [11]ReservedBits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [7:4]ReservedBits [7:4]ReservedBits [7:4]ReservedBit [2]Rx Interrupt EnableBit [2]Rx EnableBit [1]Tx Interrupt EnableBit [0]Tx EnableBits [1:6]ReservedBits [31:6]ReservedBits [31:6]ReservedBits [31:6]ReservedBits [31:7]Rx Buffer FullBit [2]Tx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Ox008ERRORError Status Register Bits [31:2]Bits [31:2]ReservedBit [0]Tx overrun or underrun. Set this bit to clear.Ox000DIVIDEClock Divide Ratio Register (for left or right clock)Bits [31:10]ReservedBits [31:10] | | | Bit [15] | Reserved |
| Bit [11]ReservedBits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [7:4]ReservedBit [3]Rx Interrupt Enable Bit [2]Bit [1]Tx Interrupt Enable Bit [0]Bit [1]Tx Interrupt Enable Bit [0]Dx004STATUSStatus Register Bits [31:6]Bits [31:6]Reserved Bit [3]Bit [2]Rx Buffer Full Bit [3]Bit [2]Tx Buffer Empty Bit [3]Bit [2]Tx Buffer Full Bit [2]Bit [2]Tx Buffer Alert (Depends on Water level) Bit [1]DX008ERRORError Status Register Bits [31:2]Bits [31:2]Reserved Bit [1]Bit [0]Tx overrun or underrun. Set this bit to clear.DX000DIVIDECkcb Divide Ratio Register (for left or right clock) Bits [31:10]Reserved Bits [9:0]LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48KHz / 2*(L+R) = 128. | | | Bits [14:12] | |
| Bits [10:8]TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than two-word space is available)Bits [7:4]ReservedBit [3]Rx Interrupt EnableBit [2]Rx EnableBit [1]Tx Interrupt EnableBit [1]Tx Interrupt EnableBit [0]Tx EnableOx004STATUSStatus RegisterBits [31:6]ReservedBit [3]Rx Buffer FullBit [4]Rx Buffer FullBit [2]Tx Buffer FullBit [2]Tx Buffer FullBit [2]Tx Buffer FullBit [2]Tx Buffer Alert (Depends on Water level)Bit [1]Rx Buffer Alert (Depends on Water level)Bit [1]Rx Overrun or underrun. Set this bit to clear.DX006ERRORError Status Register Bits [31:2]Bit [0]Tx overrun or underrun. Set this bit to clear.DX007DIVIDEDIVIDEBits [31:10]Reserved Bits [31:2]Bits [31:2]Reserved Bits [31:2]Bits [31:2]Reserved Bits [2]Bits [31:10]Reserved Bits [31:10]Bits [31:10]Reserved Bits [31:10]Bits [2]:11]Reserved Bits [2]:12]Bits [31:10]Reserved Bits [31:10]Bits [2]:12]Reserved Bits [2]:12]Bits [2]:12]Reserved Bits [2]:12]Bits [3]:12]Reserved Bits [3]:12]Bits [3]:12]Reserved Bits [3]:12]Bits [3]:12]Reserved Bits [3]:12]Bits [3]:12]Reserved Bits [3] | | | Bit [11] | |
| Bits [7:4] Reserved Bit [3] Rx Interrupt Enable Bit [2] Rx Enable Bit [1] Tx Interrupt Enable Bit [0] Tx Enable Ox004 STATUS Status Register Bits [31:6] Reserved Bit [5] Rx Buffer Full Bit [3] Tx Buffer Full Bit [2] Tx Buffer Allert (Depends on Water level) Bit [0] Tx Buffer Allert (Depends on Water level) Bit [0] Tx Buffer Allert (Depends on Water level) Bit [0] Tx Buffer Allert (Depends on Water level) Bit [0] Tx Suffer Allert (Depends on Water level) Bit [0] Tx Suffer Allert (Depends on Water level) Bit [1] Reserved Bit [1] Reserved Bit [1] Reserved Bit [1] Roverrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. Bit [31:10] Reserved Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | | |
| Bit [2]Rx Enable Bit [1]Tx Interrupt Enable Bit [0]0x004STATUSStatus Register Bits [31:6]Reserved Reserved Bit [5]0x04STATUSStatus Register Bits [31:6]Reserved Reserved Bit [5]0x05STATUSStatus Register Bit [2]Rx Buffer Full Rx Buffer Full Bit [2]0x06ERRORError Status Register Bit [3]Reserved Bit [3]0x002DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:0]Reserved Reserved Bits [31:10]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10]Reserved Reserved Bits [31:10]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10]Reserved Reserved Bits [31:20]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10]Reserved Reserved Bits [31:20]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:20]Reserved Reserved Reserved Bits [31:20]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:20]Reserved Reserved Reserved Bits [31:20]0x005DIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:20]Reserved Reserved Reserved Bits [31:20] | | | Bits [7:4] | |
| Bit [1]Tx Interrupt Enable Bit [0]0x004STATUSStatus Register Bits [31:6]0x004STATUSStatus Register Bits [31:6]Bits [31:6]Reserved Bit [5]Bit [5]Rx Buffer Full Bit [3]Bit [3]Tx Buffer Empty Bit [3]Bit [2]Tx Buffer Full Bit [2]Bit [1]Rx Buffer Alert (Depends on Water level) Bit [0]0x008ERRORError Status Register Bits [31:2]Bits [31:2]Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0]0x00CDIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [31:10]0x00CDIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [31:2]0x00CDIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [31:10] Reserved Bits [9:0]0x00CDIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [31:2]0x00CDIVIDEClock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [31:10] Clock Lip = 128. | | | Bit [3] | |
| Bit [0]Tx Enable0x004STATUSStatus RegisterBits [31:6]ReservedBit [5]Rx Buffer FullBit [5]Rx Buffer EmptyBit [3]Tx Buffer FullBit [2]Tx Buffer FullBit [2]Tx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Bit [1]Rx Buffer Alert (Depends on Water level)0x008ERRORError Status RegisterBits [31:2]ReservedBit [0]Tx overrun. Set this bit to clear.Bit [0]Tx overrun or underrun. Set this bit to clear.0x00CDIVIDEClock Divide Ratio Register (for left or right clock)Bits [31:10]ReservedBits [9:0]LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [2] | |
| Ox004 STATUS Status Register Bits [31:6] Reserved Reserved Bit [5] Bit [5] Rx Buffer Full Bit [4] Rx Buffer Empty Bit [3] Tx Buffer Full Bit [2] Bit [2] Tx Buffer Alert (Depends on Water level) Bit [0] Tx Buffer Alert (Depends on Water level) Ox008 ERROR Error Status Register Bits [31:2] Reserved Reserved Bit [1] Ox00C DIVIDE Clock Divide Ratio Register Bits [31:10] From Status Register Reserved Bits [31:10] Ox00C DIVIDE Clock Divide Ratio Register Bits [31:10] Reserved Reserved Bits [9:0] DIVIDE Clock Divide Ratio Register Bits [31:10] Reserved Reserved Bits [9:0] | | | | • |
| Bits [31:6]ReservedBits [31:6]Rx Buffer FullBit [5]Rx Buffer EmptyBit [3]Tx Buffer FullBit [2]Tx Buffer EmptyBit [1]Rx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Ox008ERRORError Status RegisterBits [31:2]ReservedBit [0]Tx overrun. Set this bit to clear.Bit [0]Tx overrun or underrun. Set this bit to clear.Ox000DIVIDEClock Divide Ratio Register (for left or right clock)Bits [31:10]ReservedBits [9:0]LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | | |
| Bit [5]Rx Buffer FullBit [4]Rx Buffer EmptyBit [3]Tx Buffer FullBit [2]Tx Buffer EmptyBit [1]Rx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Ox008ERRORError Status ResisterBits [31:2]ReservedBit [0]Tx overrun. Set this bit to clear.Bit [0]Tx overrun or underrun. Set this bit to clear.Ox00CDIVIDEClock Divide Ratio Register (for left or right clock)Bits [31:10]ReservedBits [9:0]LRDIV (Left/Right). The default value is Ox80. 12.288MHz / 48kHz / 2*(L+R) = 128. | 0x004 | STATUS | - | <u>r</u> |
| Bit [4]Rx Buffer EmptyBit [3]Tx Buffer FullBit [2]Tx Buffer EmptyBit [1]Rx Buffer Alert (Depends on Water level)Bit [0]Tx Buffer Alert (Depends on Water level)Ox008ERRORError Status RegisterBits [31:2]ReservedBit [1]Rx overrun. Set this bit to clear.Bit [0]Tx overrun or underrun. Set this bit to clear.Ox00CDIVIDEClock Divide Ratio Register (for left or right clock)Bits [31:10]ReservedBits [9:0]LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | | - |
| Bit [3] Tx Buffer Full Bit [2] Tx Buffer Empty Bit [1] Rx Buffer Alert (Depends on Water level) Bit [0] Tx Buffer Alert (Depends on Water level) Ox008 ERROR Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. Ox00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [5] | Rx Buffer Full |
| Bit [2] Tx Buffer Empty Bit [2] Tx Buffer Alert (Depends on Water level) Bit [0] Tx Buffer Alert (Depends on Water level) 0x008 ERROR Error Status Register Bits [31:2] Reserved Bit [0] Tx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [4] | Rx Buffer Empty |
| Bit [1] Rx Buffer Alert (Depends on Water level) Bit [0] Tx Buffer Alert (Depends on Water level) 0x008 ERROR Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [3] | Tx Buffer Full |
| Bit [0] Tx Buffer Alert (Depends on Water level) 0x008 ERROR Error Status Register Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | | Tx Buffer Empty |
| Ox008 Error Status Register Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. Ox00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [1] | Rx Buffer Alert (Depends on Water level) |
| Bits [31:2] Reserved Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [O] | Tx Buffer Alert (Depends on Water level) |
| Bit [1] Rx overrun. Set this bit to clear. Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | 800x0 | ERROR | <u>Error Status R</u> | egister |
| Bit [0] Tx overrun or underrun. Set this bit to clear. 0x00C DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bits [31:2] | Reserved |
| OxOOC DIVIDE Clock Divide Ratio Register (for left or right clock) Bits [31:10] Reserved Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [1] | Rx overrun. Set this bit to clear. |
| Bits [31:10]ReservedBits [9:0]LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | | | Bit [O] | Tx overrun or underrun. Set this bit to clear. |
| Bits [9:0] LRDIV (Left/Right). The default value is 0x80. 12.288MHz / 48kHz / 2*(L+R) = 128. | 0x00C | DIVIDE | <u>Clock Divide Ratio Register</u> (for left or right clock) | |
| 2*(L+R) = 128. | | | Bits [31:10] | Reserved |
| | | | Bits [9:0] | |
| 0x010 TXBUF <u>Transmit Buffer FIFO Data Register</u> . This is a write-only register. | 0x010 | TXBUF | Transmit Buffe | er FIFO Data Register. This is a write-only register. |
| Bits [31:16] Left channel | | | Bits [31:16] | Left channel |
| Bits [15:0] Right channel | | | Bits [15:0] | Right channel |
| 0x014 RXBUF <u>Receive Buffer FIFO Data Register</u> . This is a read-only register. | 0x014 | RXBUF | Receive Buffer | r FIFO Data Register. This is a read-only register. |
| Bits [31:16] Left channel | | | Bits [31:16] | Left channel |
| Bits [15:0] Right channel | | | Bits [15:0] | Right channel |
| 0x018- RESERVED - | 0x018- | RESERVED | - | |

| Offset | Name | Description | | |
|--------|-------|---------------|------------------------------|--|
| 0x2FF | | | | |
| 0x300 | ITCR | Integration T | <u>est Control Register</u> | |
| | | Bits [31:1] | Reserved | |
| | | Bit [O] | ITCR | |
| 0x304 | ITIP1 | Integration T | est Input Register <u>1</u> | |
| | | Bits [31:1] | Reserved | |
| | | Bit [O] | SDIN | |
| 0x308 | ITOP1 | Integration T | est Output Register <u>1</u> | |
| | | Bits [31:4] | Reserved | |
| | | Bit [3] | IRQOUT | |
| | | Bit [2] | LRCK | |
| | | Bit [1] | SCLK | |
| | | Bit [O] | Sdout | |

Table 4-4 Audio I2S Register Map

4.15 Audio Configuration

The SMM implements a simple SBCon interface based on I²C. It configures the Cirrus Logic Low Power Codec with Class D Speaker Driver, CS42L52 part on the MPS3 board.

4.16 FPGA system control and I/O

The AN547 SMM implements an FPGA system control block with non-secure base address 0x49302000 and secure base address 0x59302000.

The following table shows the register memory map in offset order from the base memory address.

| Offset | Name | Information | |
|--------|---------------------|-----------------|--|
| 0x000 | FPGAIO->LED0 | LED connections | |
| | | Bits [31:10] | Reserved |
| | | Bits [9:0] | LED |
| 0x004 | FPGAIO-> M55DBGCTRL | Cortex-M55 | Control signals |
| | | Bits [31:4] | Reserved |
| | | Bit [3] | SPNIDEN |
| | | Bit [2] | SPIDEN |
| | | Bit [1] | NIDEN |
| | | Bit [0] | DBGEN |
| 0x008 | FPGAIO->BUTTON | Buttons | |
| | | Bits [31:2] | Reserved |
| | | Bits [1:0] | Buttons |
| 0x00C | FPGAIO->GPIOALT2 | GPIO Alt Fun | action 2 select: |
| | | Bits [31:0] | Reserved |
| 0x010 | FPGAIO->CLK1HZ | 1Hz up count | er |
| 0x014 | FPGAIO->CLK100HZ | 100Hz up cou | unter |
| 0x018 | FPGAIO->COUNTER | | unter - Increments when 32-bit prescale counter |
| | | | nd automatically reloads. |
| 0x01C | FPGAIO->PRESCALE | Prescale Relo | |
| | | Bits [31:0] | Reload value for prescale counter. |
| 0x020 | FPGAIO->PSCNTR | Prescale Cou | |
| | | Bits [31:0] | Current value of the prescale counter. The |
| | | | prescale counter is reloaded with PRESCALE after reaching 0. |
| 0x024 | RESERVED | _ | |
| 0x028 | FPGAIO->SWITCH | Switches | |
| | | Bits [31:8] | Reserved |
| | | Bits [7:0] | Switches |
| 0x04C | FPGAIO->MISC | Misc. control | |
| | | Bits [31:3] | Reserved |
| | | Bit [2] | SHIELD1 SPI_nCS |
| | | Bit [1] | SHIELDO_SPI_nCS |
| | | Bit [0] | ADC SPI_nCS |
| | | | Table 4.5. System Control and I/O Degisters |

 Table 4-5 : System Control and I/O Registers

4.17 Serial Configuration Controller (SCC)

The SMM implements communication between the MCC and the FPGA system through an SCC interface.



FPGA

Figure 4-1: Diagram of the SCC Interface

The read-addresses and write-addresses of the SCC interface do not use bits [1:0] All address words are word-aligned.

The following table shows SCC registers in offset order from the base address. The non-secure base address in 0x49300000, the secure is 0x59300000.

| Address | Name | Information | |
|---------------|-----------------|--------------|--|
| | | Bits [31:2] | Reserved |
| 0x000 | CFG_REG0 | Bit [1] | CPU_WAIT ctrl |
| | | Bit [O] | Reserved |
| 0x004 | CFG_REG1 | Bits [31:0] | DATA RW |
| 0,000 | | Bits [31:1] | Reserved |
| 0x008 | CFG_REG2 | Bit [0] | QSPI Select signal |
| 0x00C | CFG_REG3 | Bits [31:0] | Reserved |
| 0x010 | CFG_REG4 | Bits [31:4] | Reserved |
| | | Bits [3:0] | Board Revision [r] |
| 0x014 | CFG_REG5 | Bits [31:0] | ACLK Frequency in Hz |
| 0x018 - 0x09C | RESERVED | - | |
| 0x0A0 | SYS_CFGDATA_RTN | Bits [31:0] | DATA RW |
| 0x0A4 | SYS_CFGDATA_OUT | Bits [31:0] | DATA RW |
| 0.010 | | Bit [31] | Start (generates interrupt on write to this bit) |
| 0x0A8 | SYS_CFGCTRL | Bit [30] | RW access |
| | | Bits [29:26] | Reserved |

| Address | Name | Information | |
|---------------|-------------|---------------|--|
| | | Bits [25:20] | Function value |
| | | Bits [19:12] | Reserved |
| | | Bits [11:0] | Device (value of 0/1/2 for supported clocks) |
| | | Bits [31:2] | Reserved |
| 0x0AC | SYS_CFGSTAT | Bit [1] | Error |
| | | Bit [O] | Complete |
| 0x0B0 – 0xFF4 | RESERVED | - | |
| | | SCC AID regi | ster is read only |
| | | Bits [31:24] | FPGA build number |
| 0xFF8 | SCC_AID | Bits [23:20] | V2M-MPS3 target board revision (A = 0, B = 1, C = 2) |
| | | Bits [19:8] | Reserved |
| | | Bits [7:0] | Number of SCC configuration register |
| | | SCC ID regist | ter is read only |
| | | Bits [31:24] | Implementer ID: 0x41 = Arm |
| OxFFC | SCC_ID | Bits [23:20] | Reserved |
| | | Bits [19:16] | IP Architecture: 0x5 =AXI |
| | | | Primary part number in Binary Coded |
| | | Bits [15:4] | Decimal (BCD): Default value 0x547 = |
| | | | AN547 |
| | | Bits [3:0] | Reserved |

Table 4-6: SCC Register memory map
5 Clock architecture

5.1 Clocks

The following sections list clocks entering the FPGA and generated by the SMM.

5.1.1 Source clocks

The following clocks are inputs to the FPGA from source clocks on the board.

| Clock | Input Pin | Frequency | Note |
|--------------|----------------|--------------------|---|
| REFCLK24MHZ | OSCCLK[0] | 24MHz | 24MHz reference |
| ACLK | OSCCLK[1] | 32MHz | Programmable oscillator |
| MCLK | OSCCLK[2] | 50MHz | Programmable oscillator |
| GPUCLK | OSCCLK[3] | 50MHz | Programmable oscillator |
| AUDCLK | OSCCLK[4] | 24.576MHz | Programmable oscillator |
| HDLCDCLK | OSCCLK[5] | 23.75MHz | Programmable oscillator |
| DBGCLK | CS_TCK | Set by debugger | JTAG input |
| CFGCLK | CFG_CLK | Set by MCC | SCC register clock from MCC |
| DDR4_REF_CLK | c0_sys_clk_p/n | 100MHz | Differential input clock to DDR4 controller |
| SMBM_CLK | SMBM_CLK | Set by MCC (40MHz) | SMB clock from MCC |

Table 5-1: Source clocks

5.1.2 Generated clocks

The following clocks are generated inside the FPGA from the source clocks on the board.

| Clock | Source | Frequency | Note |
|-----------|-------------|------------|---|
| MAINCLK | OSCCLK[1] | 32MHz | Clock source for SSE-300 and all non- APB peripherals in the design |
| PERIF_CLK | OSCCLK[3] | 25MHz | Clock source for APB peripherals |
| AUDMCLK | AUDCLK | 12.29MHz | - |
| AUDSCLK | AUDCLK | 3.07MHz | - |
| SDMCLK | REFCLK24MHZ | 50MHz | - |
| CLK32KHZ | REFCLK24MHZ | 32kHz | - |
| CLK100HZ | REFCLK24MHZ | 100Hz | - |
| CLK1HZ | REFCLK24MHZ | 1Hz | - |
| CFGCLK | CFG_CLK | Set by MCC | SCC register clock from MCC |

Table 5-2: Generated internal clocks

5.1.3 SSE-300 clocks

The following clocks generated within the FPGA are connected to the SSE-300 subsystem.

| SSE-300 Clock Input | FPGA Clock | Frequency | Note |
|---------------------|------------|-----------|-------------------|
| SYSCLK | MAINCLK | 32MHz | Main System clock |
| CPUOCLK | MAINCLK | 32MHz | CPUclock |
| AONCLK | MAINCLK | 32MHz | Always On clock |
| CNTCLK | MAINCLK | 32MHz | Counter clock |
| SLOWCLK | CLK32KHZ | 32KHz | Slow clock |

Table 5-3: SSE-300 clocks

6 FPGA Secure Privilege Control

The SSE-300 Subsystem Secure Privilege and Non-Secure Privilege Control Block provide expansion security control signals to control the security gating units outside the subsystem. The following table lists the connectivity of the system security extension signals.

| Component Name | Component signals | Security Expansion Signals | |
|----------------|-------------------|----------------------------|--|
| | msc_irq | SMSCEXPSTATUS[3:1] | |
| USER MSC | msc_irq_clear | SMSCEXPCLEAR[3:1] | |
| | cfg_nonsec | NSMSCEXP[0] | |
| | apb_ppc_irq | SPERIPHPPCEXPSTATUS[0] | |
| | apb_ppc_clear | SPERIPHPPCEXPCLEAR[0] | |
| APB PPC EXP 0 | cfg_sec_resp | SECRESPCFG | |
| | cfg_non_sec | PERIPHNSPPCEXP0[15:0] | |
| | cfg_ap | PERIPHPPPCEXP0[15:0] | |
| | apb_ppc_irq | SPERIPHPPCEXPSTATUS[1] | |
| | apb_ppc_clear | SPERIPHPPCEXPCLEAR[1] | |
| APB PPC EXP 1 | cfg_sec_resp | SECRESPCFG | |
| | cfg_non_sec | PERIPHNSPPCEXP1[15:0] | |
| | cfg_ap | PERIPHPPPCEXP1[15:0] | |
| | apb_ppc_irq | SPERIPHPPCEXPSTATUS[2] | |
| | apb_ppc_clear | SPERIPHPPCEXPCLEAR[2] | |
| APB PPC EXP 2 | cfg_sec_resp | SECRESPCFG | |
| | cfg_non_sec | PERIPHNSPPCEXP2[15:0] | |
| | cfg_ap | PERIPHPPPCEXP2[15:0] | |
| | ahb_ppc_irq | SMAINPPCEXPSTATUS[0] | |
| | ahb_ppc_clear | SMAINPPCEXPCLEAR[0] | |
| AHB PPC EXP 0 | cfg_sec_resp | SECRESPCFG | |
| | cfg_non_sec | MAINNSPPCEXP0[15:0] | |
| | chg_ap | MAINPPPCEXP0[15:0] | |
| | ahb_ppc_irq | SMAINPPCEXPSTATUS[1] | |
| | ahb_ppc_clear | SMAINPPCEXPCLEAR[1] | |
| AHB PPC EXP 1 | cfg_sec_resp | SECRESPCFG | |
| | cfg_non_sec | MAINNSPPCEXP1[15:0] | |
| | chg_ap | MAINPPPCEXP1[15:0] | |
| MPC SSRAM | secure_error_irq | SMPCEXPSTATUS[2] | |

Table 6-1: Security Expansion signals connectivity

The following table lists the peripherals that are controlled by SMSCEXP. Each MSC <n> interface is controlled by SMSCEXPSTATUS[n] and SMSCEXPCLEAR [n].

| SMSCEXP Interface Number <n></n> | Name |
|----------------------------------|----------|
| 0 | Reserved |
| 1 | DMA 1 |
| 2 | DMA 2 |
| 3 | DMA 3 |
| 15:4 | Reserved |

Table 6-2: Mapping of APB PPC EXP 0

The following table lists the peripherals that are controlled by PERIPHERAL PPC EXP 0. Each APB <n> interface is controlled by PERIPHNSPPCEXP0[n] and PERIPHPPPCEXP0[n].

| APB PPC EXP 0 Interface Number <n></n> | Name |
|--|--|
| 0 | USER MEM APBO |
| 1 | USER MEM APBO |
| 3:2 | Reserved |
| 4 | NPU APBO |
| 5 | NPU APB1 |
| 12:6 | Reserved |
| 13 | SSRAM Memory Protection Controller (MPC) |
| 14 | QSPI Memory Protection Controller (MPC) |
| 15 | DDR4 Memory Protection Controller (MPC) |
| | |

Table 6-3 : Peripherals Mapping of APB PPC EXP 0

The following table lists the peripherals that are controlled by PERIPHERAL PPC EXP 1. Each APB <n> interface is controlled by PERIPHNSPPCEXP1[n] and PERIPHPPPCEXP1[n].

| APB PPC EXP 1 Interface Number <n></n> | Name |
|--|-------------------------------|
| 0 | FPGA - SBCon I2C (Touch) |
| 1 | FPGA - SBCon I2C (Audio Conf) |
| 2 | FPGA - PL022 (SPI ADC) |
| 3 | FPGA - PL022 (SPI Shield 0) |
| 4 | FPGA - PL022 (SPI Shield1) |
| 5 | SBCon (I2C - Shield0) |
| 6 | SBCon (I2C – Shield1) |
| 7 | Reserved |
| 8 | I2C DDR4 EPROM |
| 15:9 | Reserved |

Table 6-4: Peripherals Mapping of APB PPC EXP 1

The following table lists the peripherals that are controlled by PERIPHERAL PPC EXP 2. Each APB <n> interface is controlled by PERIPHNSPPCEXP2[n] and PERIPHPPPCEXP2[n].

| APB PPC EXP 2 Interface Number <n></n> | Name |
|--|-------------------------------|
| 0 | FPGA - SCC registers |
| 1 | FPGA - I2S (Audio) |
| 2 | FPGA - IO (System Ctrl + I/O) |
| 3 | UARTO - UART_F[0] |
| 4 | UART1-UART_F[1] |
| 5 | UART2 - UART_F[2] |
| 6 | UART3 - UART ShieldO |
| 7 | UART4 - UART Shield1 |
| 8 | UART5 - UART_F[3] |
| 9 | Reserved |
| 10 | CLCD |
| 11 | RTC |
| 15:12 | Reserved |

Table 6-5 : Peripherals Mapping of APB PPC EXP 2

The following table lists the peripherals that are controlled by MAIN PPC EXP 0. Each APB <n> interface is controlled by MAINNSPPCEXP0[n] and MAINPPPCEXP0[n].

| AHB PPC EXP 0 Interface Number <n></n> | Name |
|--|----------------------|
| 0 | GPIO_0 |
| 1 | GPIO_1 |
| 2 | GPIO_2 |
| 3 | GPIO_3 |
| 4 | User AHB interface 0 |
| 5 | User AHB interface 1 |
| 6 | User AHB interface 2 |
| 7 | User AHB interface 3 |
| 8 | Ethernet and USB |
| 15:9 | Reserved |

Table 6-6 : Peripherals Mapping of AHB PPC EXP 0

The following table lists the peripherals that are controlled by MAIN PPC EXP 1. Each APB <n> interface is controlled by MAINNSPPCEXP1[n] and MAINPPPCEXP1[n].

| AHB PPC EXP 1 Interface Number <n></n> | Name |
|--|----------|
| 0 | Reserved |
| 1 | DMA 1 |
| 2 | DMA 2 |
| 3 | DMA 3 |
| 15:4 | Reserved |

Table 6-7: Peripherals Mapping of AHB PPC EXP 1

7 Interrupt Map

The following table shows how the interrupts in this SMM extend the SSE-300 interrupt map by adding to the expansion area.

| Interrupt Input | Interrupt Source | Source |
|-----------------|--|-----------|
| IRQ[0] | Non-secure Watchdog reset Request | |
| IRQ[1] | Non-secure Watchdog Interrupt | _ |
| IRQ[2] | SLOWCLK Timer | _ |
| IRQ[3] | Timer 0 | _ |
| IRQ[4] | Timer 1 | _ |
| IRQ[5] | Timer 2 | _ |
| IRQ[6] | Reserved | T |
| IRQ[7] | Reserved | _ |
| IRQ[8] | Reserved | _ |
| IRQ[9] | MPC Combined (Secure) | |
| IRQ[10] | PPC Combined (Secure) | |
| IRQ[11] | MSC Combined (Secure) | |
| IRQ[12] | Bridge Error Combined Interrupt (Secure) | |
| IRQ[13] | Reserved | |
| IRQ[14] | MGMT_PPU | _ |
| IRQ[15] | SYS_PPU | - |
| IRQ[16] | CPU0_PPU | - SSE-300 |
| IRQ[17] | Reserved | |
| IRQ[18] | Reserved | |
| IRQ[19] | Reserved | |
| IRQ[20] | Reserved | |
| IRQ[21] | Reserved | |
| IRQ[22] | Reserved | |
| IRQ[23] | Reserved | |
| IRQ[24] | Reserved | |
| IRQ[25] | Reserved | |
| IRQ[26] | DEBUG_PPU | _ |
| IRQ[27] | TIMER 3 AON | |
| IRQ[28] | CPUOCTIIRQO | |
| IRQ[29] | CPU0CTIIRQ01 | |
| IRQ[30] | Reserved | |
| IRQ[31] | Reserved | |
| IRQ[32] | System timestamp counter interrupt | |
| IRQ[33] | UART 0 Receive Interrupt | |
| IRQ[34] | UART O Transmit Interrupt | FPGA |
| IRQ[35] | UART 1 Receive Interrupt | System |
| IRQ[36] | UART 1 Transmit Interrupt | _ |
| IRQ[37] | UART 2 Receive Interrupt | |

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| Interrupt Input | Interrupt Source | Source |
|-----------------|-----------------------------------|----------------|
| IRQ[38] | UART 2 Transmit Interrupt | |
| IRQ[39] | UART 3 Receive Interrupt | |
| IRQ[40] | UART 3 Transmit Interrupt | |
| IRQ[41] | UART 4 Receive Interrupt | |
| IRQ[42] | UART 4 Transmit Interrupt | |
| IRQ[43] | UART 0 Combined Interrupt | |
| IRQ[44] | UART 1 Combined Interrupt | |
| IRQ[45] | UART 2 Combined Interrupt | |
| IRQ[46] | UART 3 Combined Interrupt | |
| IRQ[47] | UART 4 Combined Interrupt | |
| IRQ[48] | UART Overflow (0, 1, 2, 3, 4 & 5) | |
| IRQ[49] | Ethernet | |
| IRQ[50] | Audio I ² S | |
| IRQ[51] | Touch Screen | |
| IRQ[52] | USB | |
| IRQ[53] | SPLADC | |
| IRQ[54] | SPI (Shield 0) | |
| IRQ[55] | SPI (Shield 1) | |
| IRQ[56] | U55 Interrupt | |
| IRQ[59:57] | Reserved | FRCA |
| IRQ[60] | DMA 1 Error Interrupt | FPGA System |
| IRQ[61] | DMA 1 Terminal Count Interrupt | |
| IRQ[62] | DMA 1 Combined Interrupt | |
| IRQ[63] | DMA 2 Error Interrupt | |
| IRQ[64] | DMA 2 Terminal Count Interrupt | |
| IRQ[65] | DMA 2 Combined Interrupt | |
| IRQ[66] | DMA 3 Error Interrupt | |
| IRQ[67] | DMA 3 Terminal Count Interrupt | |
| IRQ[68] | DMA 3 Combined Interrupt | |
| IRQ[69] | GPIO 0 Combined Interrupt | |
| IRQ[70] | GPIO 1 Combined Interrupt | |
| IRQ[71] | GPIO 2 Combined Interrupt | |
| IRQ[87:72] | GPIO 3 Combined Interrupt | |
| IRQ[103:88] | GPIO 0 individual interrupts | |
| IRQ[119:104] | GPIO 1 individual interrupts | |
| IRQ[123:120] | GPIO 2 individual interrupts | |
| IRQ[124] | GPIO 3 individual interrupts | |
| IRQ[125] | UART 5 Receive Interrupt | |
| IRQ[126] | UART 5 Transmit Interrupt | |
| IRQ[127] | UART 5 Combined Interrupt | |
| IRQ[130:128] | Reserved | |

Table 7-1: Combined SSE-300 and FPGA System Interrupt Map

7.1 UART Interrupts

There are six CMSDK UARTs in the system, each with the following interrupt pins:

- TXINT
- RXINT
- TXOVRINT
- EXOVRINT
- UARTINT

The TXINT, RXINT and UARTINT interrupt signals of each UART drive a single interrupt input of the SSE-300 Example Subsystem. In addition, the TXOVERINT and EXOVRINT interrupt signals of all six UARTs, twelve signals in all, are logically ORed together to drive IRQ[47].

8 Shield Support

This SMM supports external shield devices. To enable the Shield support, two SPI, two UART and two I²C interfaces are multiplexed with GPIO over the Shield Headers.



Figure 8-1: Shield Device Expansion

Multiplexing is controlled by the alternative function output from the associated GPIO Register. An experimental second alternative function is multiplexed for pins 1-9 of Shield 0 and these are controlled through GPIOALT2 in the FPGAIO Registers at address offset 0x0C.

The second ALT function is unused on AN547 and is not shown in the following table.

| MPS3 | GPIO | ALT Function 1 | ALT Description 1 |
|----------|----------|---------------------|--------------------------|
| SH0_IO0 | GPIO0_0 | UART3 RXD - SHO_RXD | Shield O UART Receive |
| SH0_IO1 | GPIO0_1 | UART3 TXD - SHO_TXD | Shield O UART Transmit |
| SH0_IO2 | GPIO0_2 | - | - |
| SH0_IO3 | GPIO0_3 | - | - |
| SH0_IO4 | GPIO0_4 | - | - |
| SH0_105 | GPIO0_5 | - | - |
| SH0_IO6 | GPIO0_6 | - | - |
| SH0_IO7 | GPIO0_7 | - | - |
| SH0_IO8 | GPIO0_8 | - | - |
| SH0_IO9 | GPIO0_9 | - | - |
| SH0_IO10 | GPIO0_10 | SPI3 SS - SHO_nCS | Shield O SPI Chip Select |

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| MPS3 | GPIO | ALT Function 1 | ALT Description 1 |
|----------|----------|----------------------|--------------------------|
| SH0_IO11 | GPIO0_11 | SPI3 MOSI – SH0_DO | Shield 0 SPI Data Out |
| SH0_IO12 | GPIO0_12 | SPI3 MISO - SHO_DI | Shield 0 SPI Data In |
| SH0_IO13 | GPIO0_13 | SPI3 SCK - SHO_CLK | Shield 0 SPI Clock |
| SH0_IO14 | GPIO0_14 | SBCON2 SDA - SH0_SDA | Shield 0 I2C Data |
| SH0_IO15 | GPIO0_15 | SBCON2 SCL - SH0_SCL | Shield 0 I2C Clock |
| SH1_IO0 | GPIO1_0 | UART4 RXD - SH1_RXD | Shield 1 UART Receive |
| SH1_IO1 | GPIO1_1 | UART4 TXD - SH1_TXD | Shield1 UART Transmit |
| SH1_IO2 | GPIO1_2 | - | - |
| SH1_IO3 | GPIO1_3 | - | - |
| SH1_IO4 | GPIO1_4 | - | - |
| SH1_IO5 | GPIO1_5 | - | - |
| SH1_IO6 | GPIO1_6 | - | - |
| SH1_IO7 | GPIO1_7 | - | - |
| SH1_IO8 | GPIO1_8 | - | - |
| SH1_IO9 | GPIO1_9 | - | - |
| SH1_IO10 | GPIO1_10 | SPI4 SS - SH1_nCS | Shield 1 SPI Chip Select |
| SH1_IO11 | GPIO1_11 | SPI4 MOSI - SH1_DO | Shield 1 SPI Data Out |
| SH1_IO12 | GPIO1_12 | SPI4 MISO - SH1_DI | Shield 1 SPI Data In |
| SH1_IO13 | GPIO1_13 | SPI4 SCK - SH1_CLK | Shield 1 SPI Clock |
| SH1_IO14 | GPIO1_14 | SBCON3 SDA - SH1_SDA | Shield 1 I2C Data |
| SH1_IO15 | GPIO1_15 | SBCON3 SCL - SH1_SCL | Shield 1 I2C Clock |

Table 8-1: Shield Alternative Function Pinout

9 ZIP Bundle Description

9.1 Overall Structure

The accompanying .zip bundle contains:

- This Application Note Document.
- An example Keil® MDK Version 5.31 software project, that can be run on the MPS3 board peripherals and interfaces.
- Boardfiles/ directory containing the directory structure and files to be loaded onto the MPS3 SD Card. This is required to configure the MPS3 board to load and run this implementation.

9.2 Bundle Directory Tree/Structure

The directory tree structure of the bundle is shown below.

```
|-- Boardfiles
L
  |-- MB
    | |-- HBI0309B
L
      |-- HBI0309C
Т
    1
   |-- SOFTWARE
L
    | |-- an547 st.axf
L
    |-- config.txt
L
|-- Docs
    |-- DAI0547C SSE300 with Cortex-M55 and Ethos-U55 FPGA for mps3.pdf
|-- Software
Т
    |-- selftest
|-- apaaci
L
        |-- apclcd
L
        |-- apgpio
        |-- aplan
        |-- apleds
L
        |-- apmain
L
        |-- apmem
L
       |-- apqspi
        |-- aprtc
L
```

- | |-- apssp
- | |-- aptimer
- | |-- aptsc
- | |-- apuart
- | |-- apusb
- | |-- RTE
- | |-- v2m_mps3
- | |-- an547_st.axf
- | |-- move.bat
- | |-- selftest_mpb.uvoptx
- | |-- selftest_mpb.uvprojx
- |-- Licence.pdf
- |-- Release_Notes.txt
- |-- revision history.txt

10 Board Revision And Support

10.1 Identifying the MPS3 board revision

The bundle supports MPS3 board revisions B and C. The board revision, if not known, can be identified from the silk screen text, inside a marked box, on the board as shown in the diagram below :



Board Part Number and Revision-

Figure 10-1: MPS3 board revision identifier

In this picture the part number is "HBI0309**B**", which indicates that the board is revision B.

10.2 Bundle support for specific MPS3 board revisions.

There are two subdirectories in the Boardfiles/MB/ directory that correspond to the two supported revisions:

- HBI0309B
- HBI0309C

The contents of each of these directories, within the provided .zip bundle, are identical but the MCC only uses the contents from the directory name that matches the board part number and revision in use. See 10.1 for further details on how to identify the board part number and revision.



Only files modified within the directory name that align with the MPS3 board part number and revision are used by the MCC. Care must be taken to ensure that the correct directory contents are modified if required.

11 Using AN547 on the MPS3 Board

11.1 Pre-Requisites

Before attempting to use the board, you must:

- Read the Arm® MPS3 FPGA Prototyping Board Technical Reference Manual.
 - In particular, become familiar with the description of the configuration and boot flow.

You must be able to:

- Connect a PC to the MPS3 board using a USB connection (which is required to load files onto the MPS3 board SD card to run the built .bit file from the FPGA build flow).
- Power the MPS3 board.
- The MPS3 board appears as a mapped drive named "V2M_MPS3".
- Understand how to power up, reset and establish a serial terminal over the USB connection to a host PC.

11.2 Loading a prebuilt image onto the MPS3 Board

To load the prebuilt AN547 image, follow these steps:

- 1. Power up the MPS3 board using the PBON push button and wait for the V2M_MPS3 drive to appear.
- 2. Format the V2M_MPS3 drive and copy the contents of <install_dir>/Boardfiles and paste them into the root directory of the attached V2M_MPS3 drive.

Note: You might want to manually modify and merge the contents for certain configuration files. Alternatively, you can restore the existing configuration files from the /Boardfiles directory. The affected configuration files are:

- a. <install_dir>/Boardfiles/config.txt
- b. <install_dir>/Boardfiles/MB/HBI0309C/board.txt
- 3. Eject the V2M_MPS3 volume from your computer to unmount the drive.
- 4. Power cycle the MPS3 board using the PBRST push button and then launch MCC firmware update and FPGA configuration by pressing PBON push button. The LEDs flash rapidly to indicate that a new MCC firmware is being downloaded, (this only occurs the first time the MCC firmware is updated), and that the prebuilt image is being downloaded onto the board. When the bar LEDs next to PBRST button show green and user LED's UL0-7 are alternatively lit, the FPGA is programmed.
- 5. The color LCD touch screen shows the MPS3 splash screen. Simultaneously, if you have configured the UART to run, the debug UART terminal shows the selftest menu for Application Note AN547.
- 6. If the MPS3 board does not boot correctly, refer to the log.txt in the root directory of the MPS3 board which provides a log file of the files loaded at bootup.

11.3 UART Serial Ports

Four serial ports are supported on this implementation and are accessible through the MPS3 board Debug USB port:

- Serial Port 0 is connected to the MCC and outputs debug information about the status of the MCC.
- Serial Port 1 is connected to the UART 0.
- Serial Port 2 is connected to the UART 1.
- Serial Port 3 is connected to the UART 2.



The logical <> physical mapping of the Serial Ports on a host PC can be confusing due to the way the driver may allocate the port numbers. The Serial Port presented with the lowest number aligns to Serial Port 0 above.

11.4 UART Serial Port Terminal Emulator Settings

All serial ports on this implementation use the following terminal/serial port settings:

- Baud Rate: 115200 bps
- New-Line: CR (Serial port 0) And LF (Serial Port 1,2 and 3 Only)
- Data: 8 bits
- Parity: none
- Stop: 1 bit
- Flow control: none

11.5 MPS3 USB Serial port drivers for Windows

For information on installing drivers to support USB serial port on MPS3 see:

https://community.arm.com/dev-platforms/w/docs/381/accessing-mps3-serial-ports-in-windows-10

11.6 MCC Memory mapping

The MCC on the MPS3 has some visibility into the memory for initiating boot memory areas and configuring peripherals if needed. This access is limited to just 4x 64MB, so it is unable to cover the whole map, hence only those regions which are necessary for the design functionality are mapped.

The following table shows the memory map as viewed from the MCC.

| CS | MCC SMB Address | MCC Internal | SSE-300 Address | Size | IOFPGA |
|----|---------------------------|---------------------------|---------------------------|--------|--------------------------------|
| 4 | 0.0000.0000.0.0007.FFF | 0 (000 0000 0 (007 FFF | 0.0000.0000.0.0007.FFFF | E4014D | |
| 1 | 0x0000_0000 - 0x0007_FFFF | 0x6000_0000 - 0x6007_FFFF | 0x0000_0000 - 0x0007_FFFF | 512KB | ITCM NS |
| | 0x0100_0000 - 0x011F_FFFF | 0x6100_0000 - 0x6107_FFFF | 0x1000_0000 - 0x1007_FFFF | 512KB | ITCM S |
| | 0x0200_0000 - 0x0207_FFFF | 0x6200_0000 - 0x621F_FFFF | 0x0100_0000 - 0x011F_FFFF | 2MB | FPGA SRAM NS |
| | 0x0300_0000 - 0x031F_FFFF | 0x6300_0000 - 0x631F_FFFF | 0x1100_0000 - 0x111F_FFFF | 2 MB | FPGA SRAM S |
| 2 | 0x0400 0000 - 0x04FF FFFF | 0x6400 0000 - 0x64FF FFFF | 0x4100 0000 - 0x41FF FFFF | 16 MB | Low Latency |
| | | | | | Peripherals NS |
| | 0x0500_0000 - 0x05FF_FFFF | 0x6500_0000 - 0x65FF_FFFF | 0x4900_0000 - 0x49FF_FFFF | 16 MB | High Latency Peripherals NS |
| | 0x0600_0000 - 0x06FF_FFFF | 0x6600_0000 - 0x66FF_FFFF | 0x5100_0000 - 0x51FF_FFFF | 16 MB | Low Latency Peripherals S |
| | 0x0700_0000 - 0x07FF_FFFF | 0x6700_0000 - 0x67FF_FFFF | 0x5900_0000 - 0x59FF_FFFF | 16 MB | High Latency Peripherals S |
| | | | | | |
| 3 | 0x0800_0000 - 0x0BFF_FFFF | 0x6800_0000 - 0x6BFF_FFFF | 0x6000_0000 - 0x63FF_FFFF | 64 MB | DDR4 NS |
| | | | | | |
| 4 | 0x0C00_0000 - 0x0FFF_FFFF | 0x6C00_0000 - 0x6FFF_FFFF | 0x7000_0000 - 0x73FF_FFFF | 64 MB | DDR4 S |

Table 11-1: MCC memory map table

12 Software

12.1 Rebuilding software

Requirements:

- The software directory from the download
- Keil µVision® 5.31 or later

The following instructions apply to the software package provided:

- 1. Navigate to <install dir>/Software/selftest/
- 2. Load selftest_mpb.uvprojx in Keil uVision
- 3. Once loaded, the project can be rebuilt by selecting either:
 - o Project > Build Target
 - Project > Rebuild all target files
- The output can then be found in <install_dir>/Software/selftest/an547_st.axf

12.2 Loading software on the MPS3 board

Requirements:

- MPS3 board powered and USB cable connected
- MPS3 USB mass storage open in a file explorer

The following instructions apply to all versions of software:

- Copy the software <install_dir>/Software/selftest/an547_st.axf to the board <MPS3 dir>/Software folder
- 2. Navigate to <MPS3_dir>MB/HBI0309C/AN547 and open the images.txt file in a text editor
- 3. Add a new line for the new software you wish to run and make sure the other lines are commented out, for example :

;IMAGEOFILE: \SOFTWARE\selftest.axf; - selftest uSD IMAGEOFILE: \SOFTWARE\an547_st.axf ; - selftest uSD

(the compiled an 547_st.axf image is uncommented, which is therefore selected and selftest.axf is commented out)

The MPS3 can now be booted according to the instructions in the Arm® MPS3 FPGA Prototyping Board Getting Started Guide that is supplied with the MPS3 board.

13 Debug

In this SMM, the subsystem includes an example debug infrastructure that instances DAP-Lite2, debug timestamp generator, Cortex-M55 TPIU, and MCU debug ROM table. The DAP-Lite2 is compliant with Arm® Debug Interface Architecture Specification ADIv6.0.

For more information about debug infrastructure, see the Arm® Corstone™ SSE-300 Example Subsystem Technical Reference Manual.

13.1 Debug Connectivity

The following table shows the supported connectivity between the MPS3 Board debug connectors and the supported debug in the SMM. See **Figure 13-3 : MPS3 Board Debug Connector Locations** for the locations of the debug connectors on the board.

| Debug Connector Type | P-JTAG Debug | SWD | 4-bit Trace | 16-bit Trace |
|-----------------------------|-----------------|-----|-------------|--------------|
| 20 pin Cortex debug and ETM | Yes | Yes | No | No |
| 20 pin IDC | Yes | Yes | No | No |
| Mictor 38 | Yes | Yes | Yes | No |

Table 13-1: Debug Connectivity and Support

13.2 Debug support for Keil MDK

Debug has been tested using Keil uVision 5.31 with Arm Keil ULINK[™] Pro Armv8-M Debugger and CMSIS-DAP Armv8-M Debugger.

Apply the following debug settings if using a ULINK Pro Armv8-M Debugger:

- Port: JTAG
- Reset: Autodetect
- Connect: Normal

Arm® Corstone[™] SSE-300 with Cortex®-M55 and Ethos[™]-U55 : Example Subsystem for MPS3 - Application Note AN547

| ULINK USB - JTAG/SW Ad | lapter J | AG Device Chain - | | | _ |
|--|-----------|--|------------------------|-------------------|----------|
| Serial No: Any | - | IDCODE | Device Name | IR len | Move |
| ULINK Version: ULINKpro | T | DO 💿 0x4BA06 | 477 ARM Core Sight JTA | G-DP 4 | Up |
| Device Family: Cortex-M | _ | ГDI | | | Down |
| Firmware Version: V1.59 SWJ Port: JTAG Max Clock: 1MHz | • | Automatic Detect Manual Configura Add Delete | 1 | AP: 0 | 00000000 |
| Debug Connect & Reset Options | | | Cache Options | - Download Option | 15 |
| Connect: Normal | Reset: AL | todetect 👻 | Cache Code | Verify Code I | |
| | | _ | Cache Memory | Download to | Flach |

Figure 13-1:Keil MDK debug configuration

Arm® Corstone™ SSE-300 with Cortex®-M55 and Ethos™-U55 : Example Subsystem for MPS3 - Application Note AN547

Apply the following debug settings if using CMSIS-DAP Armv8-M Debugger:

- Port: SW
- Reset: Autodetect
- Connect: Normal

| | V Device | Device Name | Move |
|--|--|----------------|---|
| | /DIO O 0x4C013477 | Derive Haine | Up Down |
| V SWJ POR SW V | Automatic Detection Manual Configuratio Add Delete | | AP: 0x0000000 |
| Debug Connect & Reset Options Connect: Normal Reset: Au | todetect 💌 | I Cache Code □ | vnload Options Verify Code Download Download to Flash |

Figure 13-2 :Keil MDK debug configuration

13.3 Trace support for Keil MDK

It is planned to include trace support for SSE-300 in future versions of the Keil Tool. Please follow the announcements of tool and pack updates related to the platform.

13.4 Debug and Trace support for Arm Development Studio

Development Studio 2020.1 Silver edition or better is required as this provides the support for the subsystem in this implementation and was the version used for testing of this application note.

13.4.1 Establishing a Debug Session

To estalish a debug connection to the Cortex-M55 processor, follow these steps:

Steps:

- 1. Ensure the Arm DSTREAM debug probe is :
 - a. Powered, and connected to the host running the Development Studio software.
 - b. Connected to the MPS3 using the 20-pin Cortex / 20-pin IDC / Mictor 38 port on the MPS3 as shown below:



Figure 13-3: MPS3 Board Debug Connector Locations

- 2. Open the Debug Configurations dialog box, by right-clicking in the Debug Control window and selecting debug configurations. This will open the debug configuration window.
 - a. Double left click on the Generic Arm C/C++ application, this will create a new configuration.
 - b. In the connection tab, in the search bar, enter "MPS3", and select the Cortex-M55 under Cortex-M Prototyping System (MPS3) Cortex-M55 (SSE-300 Subsystem) as shown in the example below.

| reate, manage, and run configurat | ions re Metal Debug' is not valid - Connection cannot be empty. |
|---|---|
| | |
|] 🖻 🖗 🗊 🗙 🖪 🏹 🔹 | Name: New_configuration |
| type filter text | 🥦 Connection 🛛 📓 Files 👫 Debugger 🆓 OS Awareness 🕬 Arguments 🚾 Environment 🛃 Export |
| CMSIS C/C++ Application Generic Arm C/C++ Application ARM-MPS3_AN547 ARM-MPS3_SSE300 | Select target Select the manufacturer, board, project type and debug operation to use. Currently selected: Arm / Cortex-M Prototyping System (MPS3) Cortex-M55 (SSE-300 Subsystem) / Bare Met Cortex-M55 |
| | MPS3 |
| | Arm Cortex-M Prototyping System (MPS3) Corstone-700 Cortex-M Prototyping System (MPS3) Cortex-M33 (SSE-200 Subsystem) Cortex-M Prototyping System (MPS3) Cortex-M33 IoT Cortex-M Prototyping System (MPS3) Cortex-M55 (SSE-300 Subsystem) Bare Metal Debug Cortex-M55 Cortex-M Prototyping System (MPS3) Cortex-R52x2 DesignStart A5 (MPS3) Arm SubSystem FVP Cortex SSE-300 (MPS3) Bare Metal Debug Cortex-M55 |
| | Target Connection DSTREAM Family V |
| | Arm Debugger will connect to a DSTREAM to debug a bare metal application. |
| | Connections Bare Metal Debug Connection DTSL Options Edit., Configure DSTREAM trace or other target options. Using "default" confi |
| | < |

Figure 13-4: Arm DS debug configurations - Connection

c. Next, in the Debugger tab, make sure that the run control is set to Connect only

| | | | < |
|---|--|--|----------------|
| 1 10 11 11 11 11 11 11 11 11 11 11 11 11 | Name: New_configuration | | |
| pe filter text | 🖇 Connection 🔚 Files 🏘 Debugger 🏾 🍪 OS Awareness 🚧 Arguments 🗮 Envi | ironment 🛃 Export | |
| CMSIS C/C++ Application Generic Arm C/C++ Application | | | |
| ARM-MPS3_AN547 | Run control | | |
| ARM-MPS3_SSE300 | Connect only Debug from entry point O Debug from symbol main Run target initialization debugger script (.ds / .py) | | |
| Wew_configuration Java Application | C Run target initialization debugger script (.ds / .py) | The Party of the P | 141. 1 |
| Jython run | | File System | Workspace |
| Launch Group | Run debug initialization debugger script (.ds / .py) | and the second | |
| Launch Group (Deprecated) | | File System | Workspace |
| | Execute debugger commands | | |
| | | | |
| | Host working directory Actions to perform after the con | nection is established | v |
| | Host working directory Actions to perform after the con | nection is established | v |
| | | nection is established File System | V Workspace |
| | Use default | | |
| | S{workspace_loc} | | |
| | Use default S(workspace_loc) Paths Source search directory | | |
| | Use default S(workspace_loc) Paths Source search directory ~ | | |
| | ✓ Use default S(workspace_loc) Paths Source search directory ✓ File System Workspace | | |
| | Use default S(workspace_loc) Paths Source search directory ~ | | |
| | ✓ Use default S(workspace_loc) Paths Source search directory ✓ File System Workspace | | |

Figure 13-5 : Arm DS debug configurations - Debugger

d. Next, a connection to the DSTREAM needs to be setup. To do this, select the connection tab, select Browse (highlighted in red), a new window will open giving a list of all possible DSTREAM's. Choose your DSTREAM and click select (highlighted in blue).

| 8 🕫 🗎 🗶 🖻 | 8. | Name: New_configuration |
|---|--|--|
| filter text CMSIS C/C++ App Generic Arm C/C+ ARM-MPS3_AN ARM-MPS3_SSI | + Application 1547 E300 | Image: Select target Select target Select target Select the manufacturer, board, project type and debug operation to use. Currently selected: Arm / Cortex-MPrototyping System (MPS3) Cortex-M55 (SSE-300 Subsystem) / Bare Metal Debug / Cortex-M35 |
| Wew_configura Java Application | tion | Filter platforms |
| Launch Group (De | Connection Brows Select a target conn | Start |
| | DSTREAM USB:003307 | 0 Subsystem) 0 Subsystem) Select Cancel |
| | USB:003307 | 0 Subsystem) |
| | USB:003307 | 0 Subsystem) |

Figure 13-6 : Arm DS connection browser

- e. Now click the Apply button followed by the Debug button to start your debug session.
- 3. Program execution at this stage can be either single-stepped or set to Run ▶.

13.4.2 Trace in Debug session

Follow steps in section 13.4.1 and before step 2. e. implement the following steps :

1. Click the Edit button next to "DTSL Options" shown below. Connect the debug probe to either 20-pin IDC / Mictor 38 for trace to work.

| E Debug Configurations | | | < |
|---|--|----------------|---|
| Create, manage, and run configurations | | Ś | - |
| Image: Construction Image: Constructi | Name: New_configuration Image: Select target Select target Select target Cortex-M Prototyping System (MPS2+) Cortex-M32 IoT > Cortex-M Prototyping System (MPS3) Cortex-M33 IoT Cortex-M Prototyping System (MPS3) Cortex-M33 (SSE-200 Subsystem) > Cortex-M Prototyping System (MPS3) Cortex-M33 (SSE-300 Subsystem) Select target > Cortex-M Prototyping System (MPS3) Cortex-M33 (SSE-300 Subsystem) Select target > Cortex-M Prototyping System (MPS3) Cortex-M35 SEE-300 Subsystem) > Cortex-M Prototyping System (MPS3) Cortex-M35 SEE-300 Subsystem) > Co | | |
| Filter matched 15 of 28 items | Revert | Apply Close | |

Figure 13-7 : Arm DS debug configurations – DTSL Options

2. A new window will open, on the first tab select "DSTREAM 4GB Trace Buffer" as shown below:

| B Debug and Trace Services Layer | r (DTSL) Configuration for DSTREAM | | □ × |
|----------------------------------|--|----------------------------------|--------|
| | er (DTSL) Configuration for DS uration for file : dtsl_config_script.py | | 6 |
| 💠 🗎 🗙 🖄 🖒 | Name of configuration: defa | ult | |
| default | Trace Capture Cortex-M5 | мп | |
| | Timestamp frequency | 25000000 | |
| | Trace capture method | None | ~ |
| | | None DSTREAM 4GB Trace Buffer | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | Apply | Revert |
| ? | | ОК | Cancel |

| • 🖹 X ≧ ⊿ | Name of configuration: def | fault | |
|-----------|----------------------------|--------------------------|---|
| efault | Trace Capture Cortex-M5 | is) ITM) | |
| | Timestamp frequency | 25000000 | |
| | Trace capture method | DSTREAM 4GB Trace Buffer | ~ |
| | Off-Chip Trace | | |
| | TPIU Port Width | 4 bit | ~ |
| | | | |
| | | | |

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3. On the Cortex-M55 tab, check the "Enable Cortex-M55 core trace" box and then click Apply and then OK

| - | ayer (DTSL) Configuration for DSTREAM | | |
|------------------------------|--|-------|--------|
| id, edit or choose a DISL co | nfiguration for file : dtsl_config_script.py, class : DtslScript | | |
| ▶ 🗋 🗙 थे 🖒 | Name of configuration: default | | |
| efault | Trace Capture Codex M55 ITM | | |
| | Enable Cortex-M55 core trace | | |
| | Enable Cortex-M55 trace | | |
| | Cycle Accurate | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | Apply | Revert |
| | | ОК | Cancel |

| Debug and Trace Services Laye | r (DTSL) Configuration for DSTREAM | | × |
|-------------------------------|--|--------|---|
| | er (DTSL) Configuration for DSTREAM uuration for file : dtsl_config_script.y, class : DtslScript | | |
| default | Name of configuration: default Trace Capture Cortex-M55 ITM Enable Cortex-M55 core trace Enable Cortex-M55 trace Enable ETM Timestamps Cycle Accurate Cycle Accurate | Pevert | |
| ? | ОК | Cance | 2 |

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