ARM® DS-5™

Version 5

Setting up the ARM RVI™ Hardware

ARM®

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ARM DS-5
Setting up the ARM RVI Hardware

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
May 2010	A	Non-confidential	First release
November 2010	B	Non-confidential	Second release
30 April 2011	C	Non-Confidential	DSTREAM and RVI v4.2.1 Release
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29 February 2012	F	Non-Confidential	Update 1 for DS-5
29 July 2012	G	Non-Confidential	Update 2 for DS-5
12 October 2012	H	Non-Confidential	Update 3 for DS-5

Proprietary Notice

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling ARM RVI equipment.

The ARM RVI module generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- ensure attached cables do not lie across the target board
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

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Chapter 1
Conventions and feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

`monospace` Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

`mono`space Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

`monospace italic`

Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

`monospace bold`

Denotes language keywords when used outside example code.

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names. Also used for emphasis in descriptive lists, where appropriate, and for ARM® processor signal names.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

- your name and company

- the serial number of the product
- details of the release you are using
- details of the platform you are using, such as the hardware platform, operating system type and version
- a small standalone sample of code that reproduces the problem
- a clear explanation of what you expected to happen, and what actually happened
- the commands you used, including any command-line options
- sample output illustrating the problem
- the version string of the tools, including the version number and build numbers.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- the title
- the number, ARM DUI 0515H
- if viewing online, the topic names to which your comments apply
- if viewing a PDF version of a document, the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

ARM periodically provides updates and corrections to its documentation on the ARM Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- ARM Information Center, http://infocenter.arm.com/help/index.jsp
- ARM Technical Support Knowledge Articles, http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html
- ARM Support and Maintenance, http://www.arm.com/support/services/support-maintenance.php
- ARM Glossary, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Chapter 2
Introduction to the RVI Debug Unit

The following topics introduce ARM® RVI™, and describe the software components:

- *About the RVI debug unit* on page 2-2
- *RVI product contents* on page 2-3
- *RVI availability and compatibility* on page 2-4
- *Introduction to EmbeddedICE logic and debug extensions* on page 2-5
- *Debug extensions to the ARM processor* on page 2-6
- *EmbeddedICE debug architecture and debug monitor differences* on page 2-7
- *Introduction to the RVI components* on page 2-8
- *The RVI debug unit* on page 2-9
- *RVI hardware variants - end panel elements* on page 2-11
- *RVI hardware variants - v2 LVDS probe* on page 2-12
- *Installing the USB drivers for your debug hardware unit* on page 2-14
- *The RVI firmware* on page 2-15
- *The RVI host software* on page 2-16.

2.1 About the RVI debug unit

The ARM RVI debug unit enables your debugger to connect to ARM processor-based targets using JTAG or *Serial-Wire Debug* (SWD).

RVI provides the software and hardware interface between a debugger running on a Windows or Red Hat Linux host computer, and a *Joint Test Action Group* (JTAG) *IEEE Standard 1149.1-2001* port on the target hardware.

RVI also supports a SWD connection to the *Debug Access Port* (DAP). SWD is an alternative protocol to JTAG for connecting to CoreSight™ processors, and has the advantage of requiring fewer pins than previous probes. It also supports higher data rates.

You can use RVI with systems that contain one or more ARM processors. RVI also supports the *Embedded Trace Buffer*™ (ETB™) for capturing small amounts of trace information at high processor clock speeds.

2.1.1 See also

Concepts

- *RVI product contents* on page 2-3
- *RVI availability and compatibility* on page 2-4
- *Introduction to EmbeddedICE logic and debug extensions* on page 2-5
- *Introduction to the RVI components* on page 2-8.

Reference

Using the Debug Hardware Configuration Utilities:

- Chapter 7 *Using Trace*.

2.2 RVI product contents

The ARM RVI product comprises:

- An RVI debug unit that connects to your target board over a JTAG interface and to your PC using either USB or Ethernet.
- Mains cables and a power supply that powers the RVI unit.
- An Ethernet cable.
- A USB cable.
- Two alternative cables that connect RVI to the target JTAG connector:
  - a short 20-way ribbon cable
  - a long 40-way ribbon cable and a *Low Voltage Differential Signaling* (LVDS) 40-way to 20-way probe.
- A TI adaptor board.
- A 20-way to 14-way adaptor, for targets that use a 14-way *Insulation Displacement Connector* (IDC) box header.

  Caution

  Before using this adaptor, see *Using nonstandard connectors* for more information.

- Software on CD-ROM that enables a debugger to communicate with the RVI unit, and to configure and manage the RVI unit.
- Documentation, including:
  - online versions of this document in Eclipse browser and PDF formats
  - a packing list.

2.2.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5
- *Using nonstandard connectors* on page 3-8.

Concepts

- *About the RVI debug unit* on page 2-2
- *RVI availability and compatibility* on page 2-4
- *Introduction to EmbeddedICE logic and debug extensions* on page 2-5
- *Introduction to the RVI components* on page 2-8.

2.3 RVI availability and compatibility

RVI is available from ARM and its resellers.

Contact ARM directly regarding OEM licenses.

The RVI software for the host computer is compatible with 32-bit versions of the following operating systems:

- Windows XP Professional (Service Pack 2, or later)
- Windows Vista Business Edition and Windows Vista Enterprise Edition
- Red Hat Enterprise Linux 4 and Red Hat Enterprise Linux 5.

RVI provides:

- The ability to access the target hardware.
- Tools to configure your debugger so that it can connect to the target through RVI. Your debugger provides the user interface items, such as register windows and disassemblers, that make it possible to debug your application.

For more information on compatibility with target hardware, see the documentation supplied with your hardware.

2.3.1 See also

Concepts

- *About the RVI debug unit* on page 2-2
- *Introduction to EmbeddedICE logic and debug extensions* on page 2-5
- *Introduction to the RVI components* on page 2-8.

Other information

- Patch downloads, `http://www.arm.com/support`

2.4 Introduction to EmbeddedICE logic and debug extensions

The EmbeddedICE® logic and the ARM processor debug extensions enable RVI to debug software running on an ARM processor. The basic principles of this operation are described in the following:

- *Debug extensions to the ARM processor* on page 2-6
- *EmbeddedICE debug architecture and debug monitor differences* on page 2-7.

Note

To determine whether a specific ARM processor has support for JTAG debugging, see the datasheet or Technical Reference Manual for that processor.

2.4.1 See also

Concepts

- *About the RVI debug unit* on page 2-2
- *RVI availability and compatibility* on page 2-4
- *Debug extensions to the ARM processor* on page 2-6
- *EmbeddedICE debug architecture and debug monitor differences* on page 2-7
- *Introduction to the RVI components* on page 2-8.

Reference

Using the Debug Hardware Configuration Utilities:

- Chapter 7 *Using Trace*.

2.5 Debug extensions to the ARM processor

The debug extensions consist of several scan chains around the processor, and some additional signals that are used to control the behavior of the processor for debug purposes. The most significant of these additional signals are:

BREAKPT This processor signal enables external hardware to halt processor execution for debug purposes. When HIGH during an instruction fetch, the instruction is tagged as breakpointed, and the processor stops if this instruction reaches the execute stage of the pipeline.

DBGRQ This processor signal is a level-sensitive input that causes the processor to enter debug state when the current instruction has completed.

DBGACK This processor signal is an output from the processor that goes HIGH when the processor is in debug state so that external devices can determine the current state of the processor.

RVI uses these, and other signals, through the debug interface of the processor, for example by writing to the control register of the EmbeddedICE logic. For more details, see the topic that describes the debug interface support of the ARM datasheet or technical reference manual for your processor (for example, the *ARM7TDMI (Rev 4) Technical Reference Manual*).

2.5.1 See also

Concepts

- *EmbeddedICE debug architecture and debug monitor differences* on page 2-7.

2.6 EmbeddedICE debug architecture and debug monitor differences

A debug monitor is an application that runs on your target hardware in conjunction with your application, and requires target resources (for example, memory, access to exception vectors, and timers) to be available.

The EmbeddedICE debug architecture requires almost no resources. Rather than being an application on the board, it works by using:

- additional debug hardware within the processor, to enable the host to communicate with the target
- an external run control unit that buffers and translates the processor signals into something that is usable by a host computer.

The EmbeddedICE debug architecture enables debugging to be as non-intrusive as possible:

- the target being debugged requires very little special hardware to support debugging
- in most cases you do not have to set aside memory for debugging in the system being debugged and you do not have to incorporate special software into the application
- execution of the system being debugged is only halted when a breakpoint unit is triggered, or you request that execution is halted.

2.6.1 See also

Concepts

- *Debug extensions to the ARM processor* on page 2-6.

2.7 Introduction to the RVI components

The following topics introduce the components of the RVI product, and describe how they fit together:

- *The RVI debug unit* on page 2-9
- *The RVI firmware* on page 2-15
- *The RVI host software* on page 2-16.

2.7.1 See also

Concepts

- *About the RVI debug unit* on page 2-2
- *RVI availability and compatibility* on page 2-4
- *Introduction to EmbeddedICE logic and debug extensions* on page 2-5.

Reference

Using the Debug Hardware Configuration Utilities:

- Chapter 7 *Using Trace*.

2.8 The RVI debug unit

The RVI debug unit provides the hardware to enable a computer to control multiple JTAG capable devices. The unit has ports at one end for connecting to the host computer and to a power source. These ports are shown in the following figure:

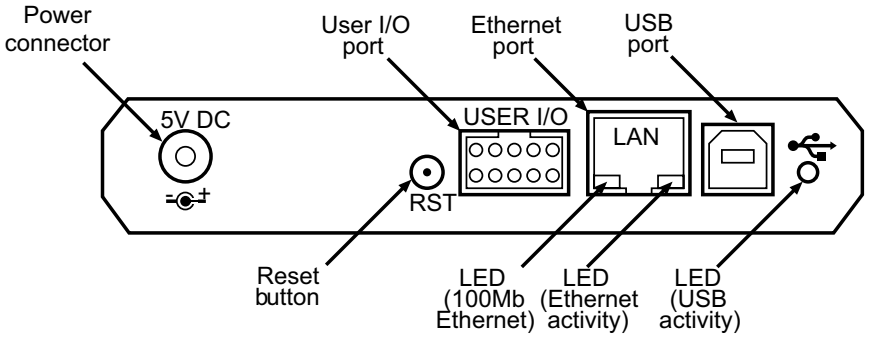

Figure 2-1 Ports for connecting to the host computer

The RST button is used to reset the RVI unit when required, and returns RVI to its power-up state. Using the RST button in this way does not reset the target. This button must not be confused with the Reset button that might be implemented on your target, located on the target board itself.

Note

When using v3.0 or later RVI hardware in conjunction with a v2 *Low Voltage Differential Signaling* (LVDS) probe, resetting RVI or power-cycling RVI does not cause a target reset. Any other hardware combination, however, might cause a target reset.

The LEDs at the bottom of the Ethernet port display information about Ethernet speed and activity:

- The green LED shows the Ethernet speed. When Off, it indicates a speed of 10Mbps, and when On indicates a speed of 100Mbps.
- The yellow LED indicates that activity is taking place.

The ports at the other end of the unit connect to the target hardware, and are shown in the following figure:

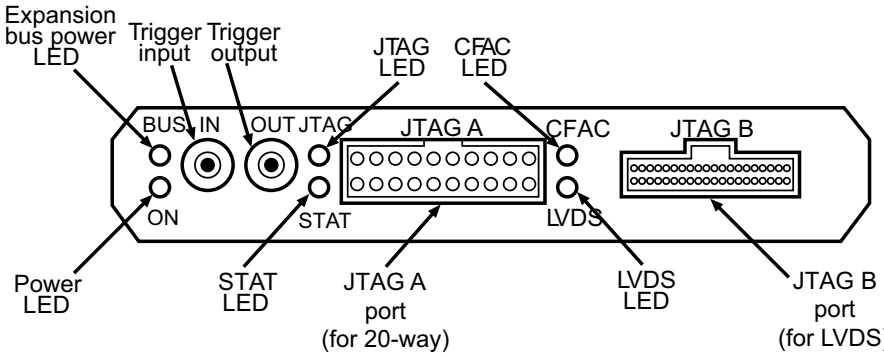

Figure 2-2 Ports for connecting to the target hardware

Cables are supplied to connect the run control unit to the host computer, and to the target hardware.

Note

RVI does not currently support the Trigger input and Trigger output signals.

If the RVI unit detects an internal hardware or software failure from which it cannot recover, the four LEDs JTAG, STAT, CFAC and LVDS flash continuously. You must reboot RVI before you can continue using it. To do this, press the RST button.

During installation of an update or a patch, the CFAC LED lights up, denoting that *Compact Flash Activity* (CFAC) is taking place. While this is happening, you must not disconnect power from the run control unit, and must wait until this LED has extinguished. The CFAC LED also lights up when a debugger connects, and during *Dynamic Host Configuration Protocol* (DHCP) lease renewal.

The RVI unit contains an internal cooling fan that operates to control the internal temperature when necessary. The ventilation panels on the top and bottom of the RVI unit must not be obscured.

2.8.1 See also

Tasks

Using the Debug Hardware Configuration Utilities:

- *Installing a firmware update or patch release* on page 4-5

Concepts

- *RVI hardware variants - end panel elements* on page 2-11
- *RVI hardware variants - v2 LVDS probe* on page 2-12
- *The RVI firmware* on page 2-15
- *The RVI host software* on page 2-16.

Reference

Using the Debug Hardware Configuration Utilities:

- *Debugging with a target reset* on page 8-21.

2.9 RVI hardware variants - end panel elements

Depending on the hardware unit that you are using, it is possible that the features of your unit might be different in appearance or functionality from those generally referred to. In units used with software ealrier than RVI v3.0, the end panel elements of the unit for the host computer port connections are arranged as shown in the following figure:

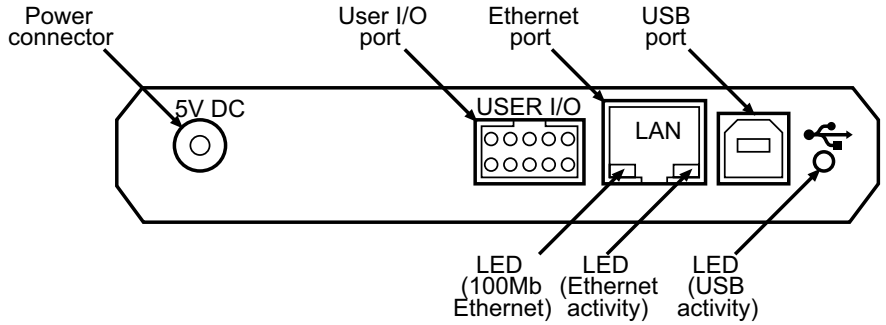

Figure 2-3 Pre-v3.0 host computer ports end panel

An example of the target hardware ports of the end panel of the unit is shown in the following figure:

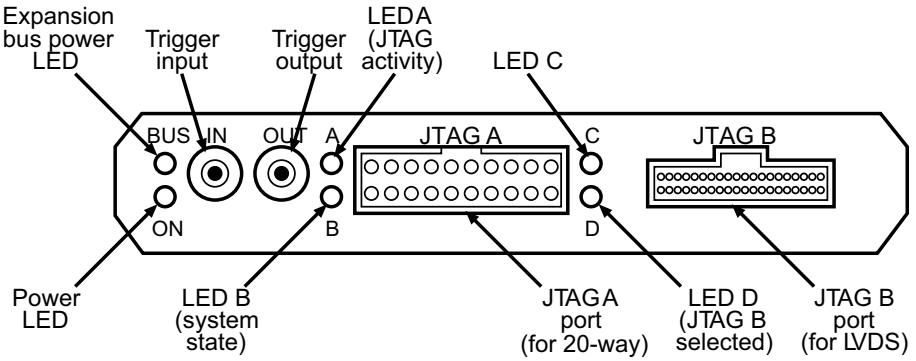

Figure 2-4 Target hardware ports end panel

2.9.1 See also

Concepts

- *The RVI debug unit* on page 2-9.

2.10 RVI hardware variants - v2 LVDS probe

The RVI unit comprises a v2 *Low Voltage Differential Signaling* (LVDS) probe. The probe is visibly different by the presence of two colored LEDs that signify the status of the activity taking place.

The functionality of the v3.1 probe enables you to make a *Serial Wire Debug* (SWD) connection to the *Debug Access Port* (DAP).

The following figure shows the dimensions of the LVDS probe and its LED locations:

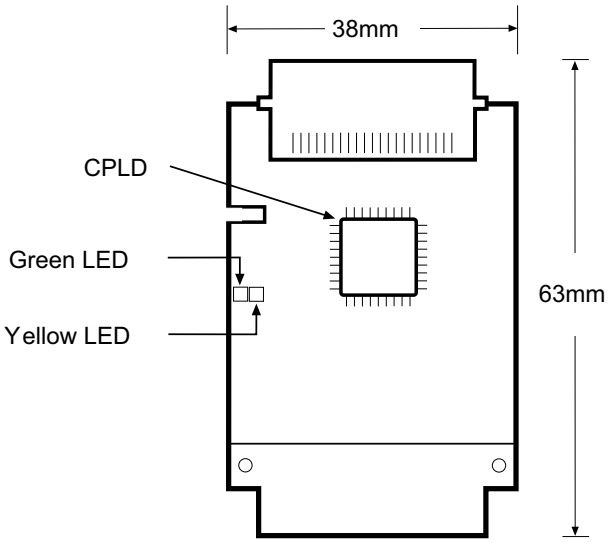

Figure 2-5 LVDS probe LEDs and dimensions

The following table provides a diagnostic means to determine the type of activity taking place, according to the permutations of the green and yellow LEDs:

Table 2-1 Diagnostic table

Green	Yellow	Power	CPLD OK	JTAG mode	SW Mode	JTAG Activity	SW Activity
Off	Off	No	N/A	N/A	N/A	N/A	N/A
Dim	Dim	Yes	No	N/A	N/A	N/A	N/A
On	On	Yes	Yes	N/A	N/A	N/A	N/A
Off	On	Yes	Yes	Yes	No	No	N/A
Flicker	On	Yes	Yes	Yes	No	Yes	N/A
On	Off	Yes	Yes	No	Yes	N/A	No
On	Flicker	Yes	Yes	No	Yes	N/A	Yes

RVI v4.0 supports the SWD debugging protocol as an alternative to JTAG. SWD can only be used with the LVDS probe, and without using the JTAG ribbon cable. The probe must be a v2 type as described, and you might have to upgrade its firmware.

As shown in the previous figure, compatible probes have two LEDs on their front left-hand side. At power-up, both LEDs are lit. If only the yellow LED is lit, you must upgrade the probe to make it SWD-capable.

In addition, if your probe does not appear to have a CPLD located as shown in the previous figure, it means that your probe is of the v1.5 type, and must be replaced if SWD-compatibility is required. To upgrade your probe to the v2 type, contact ARM for more information.

SWD supports only a single DAP and not a chain of devices. The graphical representation of the target system changes to represent this when SWD is selected.

Note

The v2 LVDS probe is supplied as standard with RVI v3.1 and later units. The probe can also be used with a RVI v3.0 unit, if you update it with a firmware patch that provides support for the v3.1 probe.

2.10.1 See also

Reference

ARM RVI™ System and Interface Design Reference:

- Chapter 5 *Serial Wire Debug*.

Using the Debug Hardware Configuration Utilities:

- *Installing a firmware update or patch release* on page 4-5
- *Upgrading an LVDS probe* on page 4-10.

2.11 Installing the USB drivers for your debug hardware unit

When you connect your debug hardware unit to a USB port for the first time after installing ARM DS-5, the Found New Hardware Wizard is displayed.

To install the USB drivers for your debug hardware unit:

1. Click **Next**.
2. Select **Install from a list or a specific location (Advanced)**.
3. Click **Next**.
4. Select **Search for the best driver in these locations**.
5. Select **Include this location in the search:**.
6. Enter the following path in the text box:
   install_directory\sw\driver_files*platform*
   where:
   install_directory
   is the DS-5 installation directory
   platform is either x64 or x86.
7. After the USB drivers are installed, click **Finish**.

2.12 The RVI firmware

The RVI firmware is located in the RVI debug unit. It receives commands from the RVI host software and translates them into JTAG accesses. The RVI firmware contains specific sections of code for each ARM processor. These are called templates.

You can update the RVI firmware using the RVI Update application in the following ways:

- for firmware fixes, you can obtain firmware patches from the ARM web site
- for firmware updates that add new functionality, such as additional templates, you must obtain a new CD that also contains updates to the host software

2.12.1 See also

Concepts

- *The RVI debug unit* on page 2-9
- *The RVI host software* on page 2-16.

Using the Debug Hardware Configuration Utilities:

- Chapter 4 *Managing the firmware on your debug hardware unit*.

Other information

- ARM patch downloads, `http://www.arm.com/support`

2.13 The RVI host software

The RVI host software provides the interface between your debugger and the RVI unit that controls the JTAG devices. It translates debugger commands, such as start, stop, and download, into JTAG control sequences for a particular processor. The RVI software provides support for debugging on a wide range of ARM processors. To see a list of supported processors, open the RVI Update application and expand the **JTAG Templates** and **ARM** trees. A list of templates for all supported processors is displayed.

The RVI software can address each JTAG device individually, without affecting other devices on the board. It uses this ability to create virtual connections for each of the JTAG devices on the board. Your debugger can attach to one of these virtual connections, and perform debugging operations with no knowledge of the other devices on the board.

The RVI software enables multiple concurrent connections. You can debug multiprocessor systems, and for more information see the documentation that accompanies your debugger. The software can also perform a synchronized start or stop of processors, for debugging multiprocessor systems where the processors interact with each other.

The RVI software also supports connections across a network, so that you can run the debugging software on several different computers.

2.13.1 See also

Concepts

- *The RVI debug unit* on page 2-9
- *The RVI firmware* on page 2-15.

Using the Debug Hardware Configuration Utilities:

- Chapter 4 *Managing the firmware on your debug hardware unit*.

Chapter 3
System requirements for using RVI

The following topics describe the system requirements for ARM® RVI™, and how to connect the RVI hardware to your host computer and target system. The topics also describe how to use some common parts of the RVI software:

- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Connecting the RVI hardware* on page 3-5
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

3.1 Host software requirements

RVI software for the host computer runs under the following operating systems:

- Windows XP Professional (Service Pack 2, or later)
- Windows Vista Business Edition and Windows Vista Enterprise Edition
- Red Hat Enterprise Linux 4 and Red Hat Enterprise Linux 5.

3.1.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

3.2 Host hardware requirements

The minimum recommended hardware requirements for installing and running the RVI software on a host computer are defined here.

If you carry out a full installation of the software, you require up to 100MB of hard disk space.

To use the RVI software on Windows, you require the following:

- a minimum specification PC with a 1GHz Pentium III class processor and 512MB of memory. The recommended specification is a Pentium 4 class machine with 1GB of memory.
- DVD-ROM drive (this can be a networked CD-ROM drive)
- an unused USB port, if direct connection to the run control unit is required
- a TCP/IP connection, if remote connection to the run control unit is required.

To use the RVI software on Red Hat Linux, you require the following:

- a minimum specification PC with a 1GHz Pentium III class processor and 512MB of memory. The recommended specification is a Pentium 4 class machine with 1GB of memory.
- DVD-ROM drive (this can be a networked CD-ROM drive)
- an unused USB port, if direct connection to the run control unit is required
- a TCP/IP connection, if remote connection to the run control unit is required.

3.2.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host software requirements* on page 3-2
- *Target hardware requirements* on page 3-4
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

3.3 Target hardware requirements

RVI has the following target hardware requirements:

- A device interface conforming to the IEEE Std. 1149.1-2001 (JTAG) specification.
- Electronic signals available to the interface, and within the limits of design-specific current and voltage ranges.
- One of the following *Insulation Displacement Connector* (IDC) box headers on the target hardware:
  - a 20-way header that conforms to the current ARM® JTAG connection standard
  - a 14-way header that conforms to the previous ARM JTAG connection standard (as used by the ARM EmbeddedICE® run control unit)
  - a 14-way TI adaptor.

  To use any other connectors, you must construct an appropriate adaptor or cable yourself.
- A maximum cable length between the target hardware and the RVI unit of:
  - 30cm if you are using a 20-way ribbon cable
  - 3m if you are using a 40-way ribbon cable with the supplied *Low Voltage Differential Signaling* (LVDS) probe.
- One or more ARM architecture CPUs that has supporting debug logic linked into a scan chain or behind a *Debug Access Port* (DAP). This includes most ARM7, ARM9, ARM10 and ARM11 processor families. It does not include the StrongARM® and XScale processors.

You can use the installed Update utility to find out which processors are supported by the version of RVI that you are using. To do this, start the Update utility and select **Version Info...** from the **RVI** menu.

3.3.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

Reference

ARM RVI™ System and Interface Design Reference:

- Chapter 2 *RVI Debug Unit System Design Guidelines*
- Chapter 3 *JTAG Interface Connections*.

3.4 Connecting the RVI hardware

The procedures described in this topic provide information on how to set up the hardware for the RVI unit.

3.4.1 Prerequisites

Before setting up the RVI hardware, ensure that you have all the relevant items that comprise the RVI product kit.

You must also provide the following items:

- a host computer that conforms to the host software and hardware requirements.
- some target hardware containing a JTAG-capable device supported by RVI.

3.4.2 Procedure

To connect the RVI run control unit to your host computer and to the target hardware:

1. Ensure the RVI software is installed on the host computer.
2. Connect the host computer to the RVI run control unit, using either the USB port or an Ethernet connection, as required. The following figure shows connections using both the USB and Ethernet cables, and the JTAG 20-way ribbon cable:

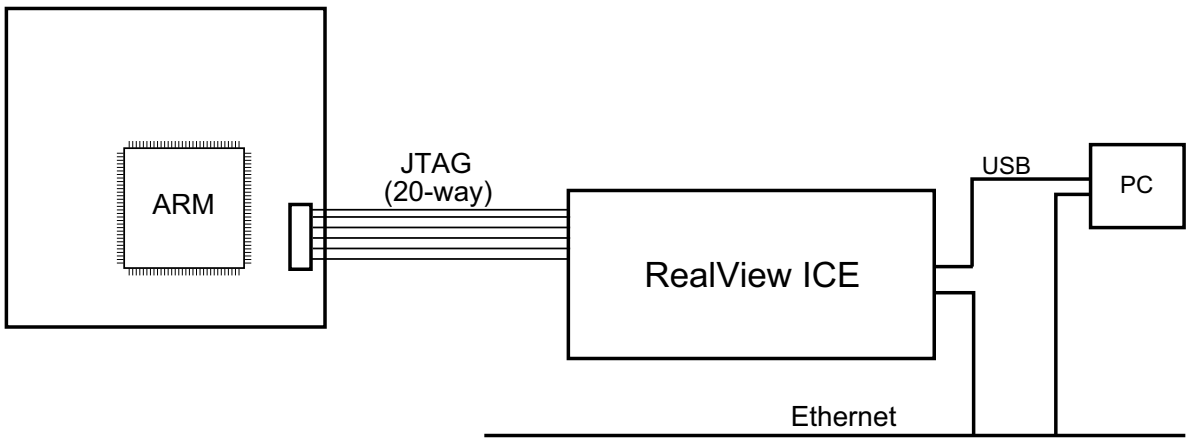

Figure 3-1 Connecting the RVI hardware

Connect the host computer to the RVI run control unit as shown in the figure above, using either the USB port or an Ethernet connection, as required:

- If you are connecting using the USB port, connect one end of the supplied USB cable to a USB port on the host computer, and the other end of the cable to the USB port on the run control unit.

  Note

  The USB drivers are installed with the RVI host software.

- If you are connecting across an Ethernet network, connect the Ethernet port of the run control unit to a socket for the Ethernet network using the supplied RJ-45 Ethernet cable.
- If you are using the cross-over cable, connect one end of the cross-over cable to the Ethernet port of the host computer, and the other end to the Ethernet port of the run control unit.

3. Connect the RVI run control unit to the target hardware, using the appropriate cable:
   - If you want to use the highest JTAG clock speeds, or if you cannot position the run control unit close to the target hardware, use the *Low Voltage Differential Signaling* (LVDS) cable and probe:
     — connect one end of the supplied LVDS cable to the 40-way connector on the probe
     — connect the other end of the LVDS cable to the 40-way *JTAG B* socket on the RVI run control unit.
     — plug the supplied LVDS probe into the 20-way JTAG header on the target hardware

     Note

     Cable selection is performed when the RVI run control unit boots. If you change the cable, you must reboot the unit.

   - Otherwise, use the JTAG cable:
     — connect one end of the supplied JTAG cable to the 20-way JTAG header on the target hardware
     — connect the other end of the cable to the 20-way *JTAG A* socket on the RVI run control unit.

   The *Insulation Displacement Connector* (IDC) connectors used for these cables are keyed using a small protrusion that must be matched up with a slot in the header or socket.
4. Power up the target hardware.
5. Connect the external power supply to the RVI run control unit, and to the mains electricity.
6. Switch on the power supply. The power LED and the expansion bus power LED both switch on.
7. The RVI run control unit firmware is based on an embedded Linux kernel. Therefore, the unit takes a short time to boot up and establish either a network or USB connection. When the unit is booting:
   - The *Compact Flash Activity* (CFAC) LED lights up, and the STAT LED flashes. As the RVI run control unit boots, the STAT LED flash rate increases.
   - The unit detects which JTAG socket has a cable attached:
     — If RVI detects that the LVDS cable and probe are connected to JTAG B socket, it uses them. It also switches on the LVDS LED.
     — If RVI detects that a JTAG cable is connected to the JTAG A socket, the LVDS LED remains unlit.
   - When the STAT LED is permanently On, the RVI run control unit has finished booting, and is ready to use.
8. If your RVI unit is connected to a network, you must now run the installed Config IP utility to configure the network settings.

   Note

   You have only to do the network configuration once.

   If the RVI unit is powered up with only a USB connection, it uses an IP address of 127.0.0.0. However, if a network cable is also attached, the IP address associated with the USB connection is the IP address that you have assigned to the RVI unit, or that it obtains from a *Dynamic Host Configuration Protocol* (DHCP) server.

Warning

Do not obstruct the ventilation grills on the top and bottom of the RVI unit, because doing so causes the unit to overheat.

3.4.3 See also

Concepts

- *RVI product contents* on page 2-3
- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

3.5 Using nonstandard connectors

RVI is supplied with cables that each terminate in a 20-way *Insulation Displacement Connector* (IDC) connector, wired to the current ARM® JTAG connection standard. Box headers suitable for this connector are fitted on all current ARM target hardware, and on several third-party targets.

Some target hardware is fitted instead with a 14-way IDC box header:

- Older ARM target hardware uses the previous ARM JTAG connection standard (as used by EmbeddedICE). This is signal-compatible with the current ARM standard. Use the supplied adaptor card to connect to these targets.
- Some other targets instead use the *Texas Instruments* (TI) JTAG connection standard, which has a different signal assignment to the ARM standards. This adaptor enables RVI to connect to these targets, and is provided.

Caution

If you use the wrong 20-way to 14-way adaptor, you might damage the target hardware.

If you are not certain of the connection standard that your target hardware uses, you *must* check the reference manual for the target *before* you connect it to the RVI run control unit. This is especially important if you are using a target that has a 14-way IDC box header, or that is not manufactured by ARM.

If the target that you are using does not use an ARM style connector, or if you are designing target hardware, contact ARM for more information.

3.5.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Hot-plugging and unplugging the JTAG cable* on page 3-9
- *Using RVI* on page 3-10.

Reference

ARM RVI™ System and Interface Design Reference:

- Chapter 3 *JTAG Interface Connections*.

Using the Debug Hardware Configuration Utilities:

- *Debugging with a target reset* on page 8-21.

3.6 Hot-plugging and unplugging the JTAG cable

You can plug and unplug the JTAG cable without affecting the target. This is because the RVI debug unit includes power conditioning and switching circuitry.

You might want to do this if you have a target that is operating without a RVI run control unit connected and you want to examine the target to find out why it is behaving in a particular way. To do this, you must power up the RVI run control unit and configure the connection without disturbing the state of the target. This requires that the RVI run control unit is powered before it is connected to the target.

When unplugging the JTAG connector, you must be aware of the following:

- If you are using an RTCK system, make sure that no communication is taking place between the system and the RVI run control unit. Otherwise, if the RVI unit is waiting for a return clock, it might lock up. In this case, you must power down the RVI unit, and power it back up again.
- If you are not using an RTCK system, the RVI software can handle this situation. However, you must arrange to do a TAP reset using the debugger when you next plug the RVI unit into a target.

3.6.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Using nonstandard connectors* on page 3-8
- *Using RVI* on page 3-10.

Reference

Using the Debug Hardware Configuration Utilities:

- Chapter 7 *Using Trace*
- *Configuring the debug hardware Advanced settings* on page 5-46.

3.7 Using RVI

After connecting RVI to your host computer, you are ready to begin using RVI for debugging, and for capturing trace if an ETB is present on the target. See the DS-5 Debugger documentation for information.

When you install the RVIsoftware, it adds capabilities to your debugger to enable you to configure a RVI connection using the Debug Hardware Config utility.

If you have to update the RVI firmware at a later date, for example to extend the capabilities of the RVI unit, you must use the RVI Update utility.

3.7.1 See also

Tasks

- *Connecting the RVI hardware* on page 3-5.

Concepts

- *Host software requirements* on page 3-2
- *Host hardware requirements* on page 3-3
- *Target hardware requirements* on page 3-4
- *Using nonstandard connectors* on page 3-8
- *Hot-plugging and unplugging the JTAG cable* on page 3-9.

Reference

Using the Debug Hardware Configuration Utilities:

- Chapter 4 *Managing the firmware on your debug hardware unit*
- Chapter 5 *Creating debug hardware target configurations*
- Chapter 7 *Using Trace*

Other information

- *Using the Debugger*, `http://infocenter.arm.com/help/topic/com.arm.doc.dui0446-/index.html`
- *Debugger Command Reference*, `http://infocenter.arm.com/help/topic/com.arm.doc.dui0452-/index.html`
- Patch downloads, `http://www.arm.com/support`.