CoreSight ETM-M33
Software Developer Errata Notice

This document contains all errata known at the date of issue, in releases up to, and including, revision r0p2.

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ARM Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

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Confidentiality Status

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Product Status

The information in this document is for a product in development and is not final.

Web address

http://www.arm.com/.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on this document

If you have comments on content then send an e-mail to errata@arm.com giving:

- The document title.
- The document number: SDEN-756496.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Contents

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A (Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B (Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Change control

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The errata summary table on page 7 identifies errata that have been fixed in each product revision.

09/May/17: Changes in document version 4.0
No new or updated errata in this document version.

02/Feb/17: Changes in document version 3.0				
ID	Status	Area	Cat	Summary of erratum
787178	New	Programmer	CatC	ETM Authentication status register reports Secure debug present in all configurations

08/Dec/16: Changes in document version 2.0
No new or updated errata in this document version.

28/Sep/16: Changes in document version 1.0
No errata in this document version.

Errata summary table

The errata associated with this product affect product versions as below.

ID	Cat	Summary	Found in versions	Fixed in version
787178	CatC	ETM Authentication status register reports Secure debug present in all configurations	r0p0	r0p1

Errata descriptions

Category A

There are no errata in this category.

Category A (rare)

There are no errata in this category.

Category B

There are no errata in this category.

Category B (rare)

There are no errata in this category.

Category C

787178

ETM authentication status register reports Secure debug present in all configurations

Status

Affects: CoreSight ETM-M33
Fault Type: Programmer Category C
Fault Status: Present in r0p0

Description

When the processor is configured with the ETM present, but without the Security Extension, the ETM authentication status register SNID bits will always read 0b10, indicating that Secure non-invasive debug is disabled. The expected behavior is that these bits should read 0b00, indicating that the trace unit does not implement support for Secure non-invasive debug.

Configurations affected

This erratum affects configurations of the Cortex-M33 processor with the ETM present, but without the Security Extension.

Conditions

The ETM authentication status register is read.

Implications

Tools might infer that they are able to enable Secure non-invasive debug, and could potentially deadlock attempting to enable this state. There is no area impact for implementation of the processor or the ETM in this configuration.

Workaround

Tools can check the processor authentication status register SNID bits to identify if Secure non-invasive debug is supported.