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Juno ARM Development Platform

Software Developers Errata Notice

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This document contains all errata known at the date of issue in releases up to and including revision c.

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- The document title
- The document number, ARM-EPM-008857
- The page numbers affected
- A concise explanation of your comments

General suggestions for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a 'work-around' where possible.

Categorization of Errata

Errata recorded in this document are split into the following levels of severity:

Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for most use-cases and applications.
Category A (rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most use-cases and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many use-cases and applications.
Category B (rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most use-cases and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Revisions

This document refers to Juno by Board Revision. The relationship between Board Revision and variant is as follows:

Board Revision	Juno variant	Juno product
A, B	Juno r0	Big.LITTLE development
C	Juno r1	PCI-Express development

Change Control

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The errata summary table on page 12 identifies errata that have been fixed in each product revision.

15 Jun 2015: Changes in Document v2

Page	Status	ID	Area	Cat	Rare	Summary of Erratum
14	New	849969	Other	CatA		Juno r1 does not support big.LITTLE MP Global Task Scheduling Model
15	New	849970	Other	CatB		Board IRQs do not wake-up the SoC when VSYS is powered down

22 Jul 2014: Changes in Document v1

Page	Status	ID	Area	Cat	Rare	Summary of Erratum
13	New	832219	Other	CatA		APB port security breaks SBSA compliance
15	New	831273	Other	CatB	Rare	Cores in WFE power state might not wake for multiple SEVs in close succession
17	New	832319	Other	CatB	Rare	Unexpected behavior when changing clock frequency
18	New	831269	Other	CatC		HWEVENT bridges, slave side, have incorrect clocks and resets
19	New	831270	Other	CatC		Juno NIC blocking transaction from the Cortex-M3 processor in multi-core environment
20	New	831271	Other	CatC		PID2 and MSIIR register Architecture revision fields read as 0x1
21	New	831272	Other	CatC		CoreSight Access to ETF/ETB hangs
23	New	831276	Other	CatC		System Profiler Errata
24	New	831319	Other	CatC		S32kCLK Generic Counter and SCP Firmware Watchdog can only be halted using level sensitive triggers
25	New	832220	Other	CatC		System deadlock if an ATB flush request is received when clusters in reset

Cortex A57 Processor Errata

The following table shows a list of all the Cortex-A57 'Programmer' errata and whether they affect Juno. Additional detail can be found in the The Cortex A57 MPCore Software Developers Errata Notice document, available on InfoCenter, contains additional information.

Table 1 Cortex A57 Errata

ID	Category	Summary of Erratum	Affects Juno r0	Affects Juno r1
806969	B Rare	A57 may send WriteEvict or Evict transaction for cache line that is still valid when using Write-Back No-Allocate memory	N	N
808671	C	ETM might not output an Address packet immediately after a Trace Information packet.	Y	N
808870	B	Unconditional VLDM instructions might cause an alignment fault even though the address is aligned	Y	N
808871	C	Double bit ECC error on an invalid L1 data cache line can incorrectly trigger an imprecise abort	Y	N
809370	C	Watchpoint might be incorrectly taken on first half of unaligned ld/st crossing a 64-byte-aligned boundary	Y	N
809371	B	Domain fault might be missed when executing specific AT instructions	Y	N
811120	A Rare	Back-pressure on AMBA 5 CHI TXRSP link can cause data corruption	N	N
811619	C	Return stack erroneous match for not taken indirect branch	Y	N
811671	B	A57 issues multiple concurrent DVMOp(Sync) transactions on AMBA 5 CHI interconnect	N	N
811672	C	When a single-bit ECC error occurs in the L2, uncorrected data might be returned	Y	N
812170	C	Erroneous LR_mon on monitor trap of T32 ACTLR-disabled write accesses	Y	N
812171	C	Erroneous ESR ISV for ARMv8-added A32/T32 load/store acquire/release exclusive instructions	Y	N
812319	B	TLBIIPAS2IS, TLBIIPAS2LIS, TLBIIPAS2, TLBIIPAS2L instructions might not invalidate targeted IPA cache entry.	Y	N
813419	B	TLB maintenance instructions targeting EL3 may not invalidate the targeted EL3 TLB entries	Y	N
813420	B	A57 DCCMVA or DCCSW targeting L2 cache might cause data corruption or deadlock	N	N
814669	C	L2 ECC error might cause a device memory type load to stall until the next timer interrupt	Y	N
814670	C	A57 DMB barrier does not guarantee observation of the effects of a cache maintenance operation	Y	N

ID	Category	Summary of Erratum	Affects Juno r0	Affects Juno r1
817169	B	DSB instruction in processor power down sequence might not drain all required transactions	Y	N
817170	C	Continuous streaming stores to device memory might block older stores	Y	N
817171	B	AMBA 5 CHI systems using SCLKEN may hang following link deactivation	N	N
817172	C	Double-bit ECC error during hardware correction of a single-bit ECC error might cause data corruption	Y	N
817722	C	Read after read memory ordering requirements might be violated with specific sequences of exclusive stores and loads	Y	N
821570	C	Read following a write of a Timer TVAL register might return incorrect value	Y	Y
821571	C	Read or write of ICC_SRE_EL1(NS) might incorrectly generate an undefined exception	N	N
822224	C	A57 might deadlock or have data corruption if the page attribute of a current page is remapped by another processor	Y	Y
822227	C	Using unsupported 16K translation granules might cause Cortex-A57 to incorrectly trigger a domain fault	Y	Y
822369	C	HSR.EC might be incorrect for certain accesses when HCR.TGE=1	Y	Y
823969	C	Halting debug event occurring while ITSTATE is non-zero might cause subsequent instructions from the ITR to execute	Y	Y
825570	C	Access to Debug EDSCR.STATUS[5:2] register bits is Read-Write instead of Read-Only	Y	Y
826974	B Rare	Cortex-A57 might violate memory order between an older store and a younger load when executing DMB ALL/ALL instruction	Y	?
826975	C	Cortex-A57 might livelock because of exclusive load to non-shared memory location with mismatched attributes	Y	Y
826977	B	L2 Data RAM corruption might occur because of a streaming write to Device-GRE memory which detects a hazard	Y	Y
826978	C	Cortex-A57 might violate read-after-read memory ordering on a load forwarding from a store crossing a 16-byte boundary	Y	N
828023	C	Cortex-A57 might violate read-after-read memory ordering when the memory accesses of loads are not single-copy atomic	Y	Y
828024	B Rare	TLB maintenance operations might not be synchronized by DSB instruction	Y	Y
829520	B	Code bounded by indirect conditional branch might corrupt instruction stream	Y	Y
832075	B	Cortex-A57 might deadlock when WB exclusive load/store instructions are mixed with device loads	Y	Y
832076	C	AuxReg field of ID_MMFR0 reports incorrect value	Y	Y

ID	Category	Summary of Erratum	Affects Juno r0	Affects Juno r1
832569	C	Cortex-A57 L1 prefetch works inefficiently for a load stream whose address is mapped to a page size of 64K or larger	Y	Y
832769	C	HSTR.{T7,T8,T15} and HSTR_EL2.{T7,T8,T15} bits incorrectly trap CDP instructions	Y	Y
833069	C	Disabling MMU Translation with CPUACTLR_EL1 "Enable Invalidates of BTB" bit set can cause Invalidate by PA or VA to fail	Y	Y
844270	C	Syndrome value incorrect for software-induced Virtual Abort exception	Y	Y
833471	B	VMSR FPSCR functional failure or deadlock	Y	Y
834921	B	Code sequence continuously hitting the L1 cache can block snoop	Y	Y
834220	B rare	Stage 2 translation fault might be incorrectly reported in presence of a stage fault	Y	Y
833472	C	PMU events 0x73 and 0x77 are not incremented for certain instructions	Y	Y
834221	C	Trace packet might be corrupted in certain cases	Y	Y
834469	C	PMU event counters are incorrectly permitted to count events	Y	Y
834528	C	PMU event BUS_CYCLES might be incorrect in some cases	Y	Y
834920	C	Write of JMCR in EL0 does not generate an undefined exception	Y	Y

Cortex A53 Processor Errata

The following table shows a list of all the Cortex-A53 'Programmer' errata and whether they affect Juno. The Cortex A53 MPCore Software Developers Errata Notice document, available from InfoCenter, contains additional information.

Table 2 Cortex A53 Errata

ID	Category	Summary of Erratum	Affects Juno r0	Affects Juno r1
810919	B	Clearing of the global exclusive monitor can fail to set the event register	N	N
811819	C	A 64-bit load to Device memory which crosses a 64-byte boundary can access more data than is permitted	N	N
812869	A	Instruction stream might be corrupted	N	N
814270	B	Misaligned PC and out-of-range address aborts might be taken to incorrect exception level	Y	N
814271	C	CPUMERRSR register might be updated incorrectly after multiple ECC/parity errors	N	N
819472	B	Store exclusive instructions might cause data corruption	Y	N
821523	A	Hazarding snoop request might cause deadlock	Y	N
822769	C	Mismatched aliases might cause deadlock	Y	N
823273	A Rare	Load or store which fails condition code check might cause data corruption	Y	N
823819	B	A snoop request to a core coincident with retention entry might cause deadlock	N	N
824069	B	Cache line might not be marked as clean after a CleanShared snoop	Y	N
826319	B Rare	System might deadlock if a write cannot complete until read data is accepted	Y	N
827319	B	Data cache clean instructions might cause overlapping transactions to the interconnect	N	N
827971	C	Store release might not be multi-copy atomic	Y	Y
829070	A	Speculative data reads might be performed to Device memory	Y	Y
831920	C	HCR.DC being set when HCR.VM not set does not correctly affect Data Cache Invalidate by MVA/VA behaviour	Y	Y
831921	C	AuxReg field of ID_MMFR0 reports incorrect value	Y	Y
835769	A	AArch64 multiply-accumulate instruction might produce incorrect result	Y	Y
836870	C	Non-allocating reads might prevent a store exclusive from passing	Y	Y
836919	C	Write of JMCR in EL0 does not generate an UNDEFINED exception	Y	Y
845719	B	A load might read incorrect data	Y	Y
845819	C	Instruction sequences containing AES instructions might produce incorrect results	Y	Y

ID	Category	Summary of Erratum	Affects Juno r0	Affects Juno r1
843419	A	A load or store might access an incorrect address	Y	Y
843819	B	Memory locations might be accessed speculatively due to instruction fetches when HCR.VM is set	Y	Y

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell marked with **X** indicates that the erratum affects the revision shown at the top of that column.

Table 3 Errata on each product version

ID	Area	Cat	Rare	Summary of Erratum	r0	r1
832219	Other	CatA		APB port security breaks SBSA compliance	X	
849969	Other	CatA		Juno r1 does not support big.LITTLE MP Global Task Scheduling Model		X
832319	Other	CatB	Rare	Unexpected behavior when changing clock frequency	X	X
831273	Other	CatB	Rare	Cores in WFE power state might not wake for multiple SEVs in close succession	X	
849970	Other	CatB		Board IRQs do not wake-up the SoC when VSYS is powered down	X	X
832220	Other	CatC		System deadlock if an ATB flush request is received when clusters in reset	X	X
831319	Other	CatC		S32kCLK Generic Counter and SCP Firmware Watchdog can only be halted using level sensitive triggers	X	
831276	Other	CatC		System Profiler Errata	X	
831272	Other	CatC		CoreSight Access to ETF/ETB hangs	X	
831271	Other	CatC		PID2 and MSIIR register Architecture revision fields read as 0x1	X	
831270	Other	CatC		Juno NIC blocking transaction from the Cortex-M3 processor in multi-core environment	X	
831269	Other	CatC		HWEVENT bridges, slave side, have incorrect clocks and resets	X	

General Errata

Category A

832219: APB port security breaks SBSA compliance

Status

Affects: Juno Platform

Fault Type: Other Category A

Fault Status: Present in: b Fixed in c.

Description

Juno includes a system-level wakeup timer. This is an implementation of the ARM Generic Timer architecture. Working with the GIC-400, this timer can schedule wakeup when all application processors are powered down.

The timer contains three register frames:

- **CNTCTL** at address `0x00_2A81_0000`.
- **CNTBase0** at address `0x00_2A82_0000`.
- **CNTBase1** at address `0x00_2A83_0000`.

The Generic Timer architecture defines the secure access permissions of the registers in each of these frames. The **CNTCTL** frame contains some registers that are accessible using a Non-Secure access. Juno incorrectly limits these accesses to Secure access only.

The following registers in the **CNTCTL** frame are affected:

- **Counter Timer ID Register, CNTTIDR**.
- **Counter Access Control Register 1, CNTACR1**.

Implications

Non-Secure software is unable to:

- Use **CNTTIDR** to discover the capabilities of the Generic Timer.
- Use **CNTACR1** to configure the access permissions of the **CNTBase1** timer frame.

This means that Non-Secure software that makes use of the wakeup timer is system-specific, and not portable to other systems.

Workaround

Non-Secure software must use the wakeup timer without using the read-only information in **CNTTIDR**, making this software system-specific.

If **CNTACR1** is required to have a value other than the default, then Secure firmware must pre-initialize it.

849969: Juno r1 does not support big.LITTLE MP Global Task Scheduling Model

Status

Affects: Juno Platform

Fault Type: Other Category A

Fault Status: Present in: c Open.

Description

Due to a silicon implementation issue on the A53 cluster in Juno r1 which limited the cluster to a reduced frequency range and fixed voltage the Juno r1 software does not support the big.LITTLE MP Global Task Scheduling Mode.

Category A (Rare)

There are no errata in this category

Category B

849970: Board IRQs do not wake-up the SoC when VSYS is powered down

Status

Affects: Juno Platform

Fault Type: Other Category B

Fault Status: Present in: b, c. Open.

Description

The SCP contained within the Juno development platform SoC contains an IRQ which is a logical OR of the V2M-Juno r1 motherboard IRQs. This provides a mechanism to enable the system to be woken from a low power state when a corresponding board IRQ is generated and VSYS is powered down.

All motherboard IRQs connect to the GIC-400 in the Juno development platform SoC through the IOFPGA. The IOFPGA clock which is used in conjunction with these external interrupts is incorrectly gated when VSYS is powered down and therefore is not capable of generating a wakeup IRQ to the SCP when the system is in this state.

Implications

Board IRQs will be unable to wake-up the SoC when VSYS is powered down.

Workaround

When using board IRQs, ensure VSYS is not powered down.

Category B (Rare)

831273: Cores in WFE power state might not wake for multiple SEVs in close succession

Status

Affects: Juno Platform

Fault Type: Other Category B Rare

Fault Status: Present in: b Fixed in c.

Description

The ARM architecture includes a Wait For Event (WFE) mechanism that enables cores to enter a low-power state. To enter the low-power state, the core executes a WFE instruction, and if the Event Register is clear, the PE can enter the low-power state.

If the core enters the low-power state, it remains in that low-power state until it receives a WFE wake-up event. One type of wake-up event is an SEV instruction executed by any core in the multiprocessor system. The two clusters in Juno provide signals so that wake-up events can be communicated between them. Juno also signals wake-up events between the Cortex-M3 System Control Processor and the two clusters.

The intended use case of the WFE mechanism is to enable a core to enter a low power state when waiting for a spinlock. A core that fails to obtain a lock executes a WFE instruction to request entry to a low-power state, at the time when the exclusive monitor is set holding the address of the location holding the lock. When any core

releases a lock, the write to the lock location causes the exclusive monitor of any core monitoring the lock location to be cleared. This clearing of the exclusive monitors generates a WFE wake-up event for each of those cores. Then, these PEs can attempt to obtain the lock again.

For additional information about this mechanism, see the ARM Architecture Reference Manual, ARMv8, for ARMv8-A architecture profile (ARM DDI 0487).

Because the two clusters and the SCP are all in different clock and power domains, Juno includes a bridge to transmit events across clock and power domain boundaries. The bridge incorrectly only transmits rising edges on the event signals between the two clusters and the SCP. Two or more separate SEVs might therefore be indistinguishable if they happen in very close succession on cores within the same cluster, or on the Cortex-M3 processor. If the tight sequence of SEVs contains instructions that occur after another core has executed a WFE instruction, the core that executed the WFE might not wake.

Implications

Cores that are in a WFE low power state might not wake as expected when several SEVs are executed in close succession, including when these are executed on different cores within the same cluster.

Workaround

When used as part of a spinlock mechanism, this erratum is very unlikely to occur. However, the following mechanisms can be used to avoid any possibility of a core remaining in WFE low power state indefinitely:

- For the Cortex-A57 cluster, either:
  - Configure the Generic Timer for each core to generate an Event Stream. This imposes a time-out on the WFE polling loop, and software might already use it to guard against programming errors.
  - Set bit 7 in the CPUACTLR_EL1 register to force WFE instructions to be executed as a NOP. This might result in increased power consumption during spinlocks.
- For the Cortex-A53 cluster:
  - Configure the Generic Timer for each core to generate an Event Stream as described above for the Cortex-A57 cluster.
- For the Cortex-M3 processor cluster:
  - SCP firmware does not use events from the clusters. However, if this is required, you can use interrupts from the SCP timers to periodically cause the Cortex-M3 to wake.

832319: Unexpected behavior when changing clock frequency

Status

Affects: Juno Platform

Fault Type: Other Category B Rare

Fault Status: Present in: b, c Open.

Description

Juno supports 12 individually configurable clocks, each feeding a major block and programmable through a Clock Control Register. For each register, the **CLKDIVxxx** bits set the divide ratio. The divide value is equal to the contents of these bits, plus one.

It is possible that individual bits could be synchronized in different phases and that an incorrect divide ratio could be used for one cycle of the output clock.

Implications

If a low divide ratio is unintentionally loaded, this could generate one cycle of an unexpectedly fast clock. If that clock exceeds the maximum supported frequency of that block then data corruption or system deadlock could occur.

For example

- The input clock is 2 GHz.
- Initial conditions are that the divider is set at /15 and the output clock is 133.3 MHz
- To request an output frequency 1 GHz the divider would be set at /2. The value programmed into the divide bits would change from `1110` to `0001`.
- If the last bit were to be synchronised later than the first three, that would produce a transition from `1110` to `0000` to `0001`, resulting in a 2 GHz output clock for one clock cycle

The likelihood of this problem occurring is extremely remote and is unlikely ever to be observed on registers set once at boot. However, it is expected that Dynamic Voltage and Frequency Scaling (DVFS) is to be used on the Cortex-A53 processor, Cortex-A57 processor and Mali-T624 GPU, increasing the potential to observe this problem.

Workaround

A two stage transition might be used to ensure that it is not possible to produce an unexpectedly high clock frequency if this problem occurs. In the above example, this workaround would take the following form:

- The divide bits should change from `1110` to `1111` and then `0001`.
- The output frequency changes from 133.3 MHz to 125 MHz to 1 GHz.

Category C

831269: HWEVENT bridges, slave side, have incorrect clocks and resets

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

The slave side of async event bridge for **SYS CTI0** trigger connections, **TRIGOUT[4]** & **[5]**, to **STM HWEVENT**s interface, **HWEVENTS[3:0]**, is being driven from the incorrect **PCLKDBG** domain instead of the **ATCLK** domain.

The issue is likely to be seen when **ATCLK** and **PCLKDBG** are not running at a 1:1 ratio. Trigger events go missing from the STM trace because the events fail to be detected at the **HWEVENT**s interface.

Implications

SYS CTIO triggers directed to the **STM HWEVENT**s interface for tracing can be missed when **ATCLK** and **PCLKDBG** are running in a ratio other than 1:1.

Workaround

There is no workaround because a hardware fix is required but it is recommended that trigger tracing over STM **HWEVENT**s be performed with **ATCLK** and **PCLKDBG** configured to run 1:1. These clocks are always synchronous.

Because of the following mitigating factors, it should be acceptable to run **ATCLK** and **PCLKDBG** in 1:1 or 2:1 clock ratio under normal operation.

For all other clock ratios the following mitigating factors apply:

- All channels on **SYS_CTI0** are fully handshaken and these are unlikely to cause pulse trigger on **TRIGOUT[4 & 5]**. Therefore this is relatively safe.
- Other trigger sources on **SYS_CTI0** (ETF/ETR/TPIU/STM) are not typically used for **HWEVENTS** tracing because they are traced elsewhere. Therefore, under normal usage, you can ignore these for **HWEVENTS**.

831270: Juno NIC blocking transaction from the Cortex-M3 processor in multi-core environment

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

It is possible to flood certain NIC-400 interfaces with transactions on a single Virtual Network (VN), causing other virtual networks to be starved for the duration of the traffic.

This can occur when traffic on a single virtual network is consistently only read transactions or consistently only write transactions, and exceeds the acceptance capability of the attached slave.

This can occur on the following NIC-400 interfaces:

- To the PL354 Static Memory Controller (SMC), Juno NIC.
- To the System Profiler Master Controller (SP MCTLR), Columbus64 NIC.
- To the Global Interrupt Controller (GIC), Columbus64 NIC.
- To the Message Sensitive Interrupt block (MSI), Columbus64 NIC.
- To the CoreSight System Trace Macrocell (STM), Columbus64 NIC.

Implications

During periods of constant traffic generation, transactions on some virtual networks are blocked in NIC-400 introducing significant latency.

Workaround

The software workaround is to raise the QoS priority value for the starved master(s) above the QoS value for the more aggressive master.

831271: PID2 and MSIIR register Architecture revision fields read as 0x1

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

Juno includes a Message Signaled Interrupt (MSI) Unit that is an implementation of the GICv2m architecture. The GICv2m architecture expands the GICv2 architecture by providing additional register frames used the mapping of PCIe MSIs, MSI and MSI-X, to GIC Shared Peripheral Interrupts (SPIs). The Juno MSI Unit contains the read-only PID2 and MSIIR registers that contain an architecture version field. This provides the version number of the GICv2m architecture that has been implemented. The GICv2m architecture defines `0x0` as the only legal value for this field. However, both registers in the Juno MSI unit return `0x1`.

Configurations affected

This erratum affects Juno when using PCIe.

Implications

Software that reads the architecture version from the PID2 or MSIIR registers receive `0x1` instead of `0x0`.

Workaround

Only a single version of the GICv2m architecture is defined, so software can function correctly without reading the architecture version value. Subsequent versions of the GICv2m architecture are not expected to be defined.

831272: CoreSight Access to ETF/ETB hangs

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

For Juno, the debug subsystem (CSSYS: contains debug, trace and cross-trigger components such as ETF, ETR, TPIU, CTIs, funnels, APB-IC, DAP APB-AP and does not include core macro debug and trace components) is powered up and clocks set running as part of a debugger connecting and performing a power-up request. These components are clocked by either **ATCLK** only (ETR, ETF, Funnels) or **PCLKDBG** only (APB-IC, CTIs, DAP APB-AP) or both (TPIU). **ATCLK** and **PCLKDBG** are always N:1 synchronous. In Juno, **PCLKDBG** is a divided version of **ATCLK** and always synchronous.

For components clocked from **ATCLK** only, the debug interface is run with the aid of an enable signal **PCLKDBGEN** that informs the component when to send the data relative to **PCLKDBG**.

If **ATCLK=PCLKDBG** then **PCLKDBGEN=**`1'b1` for example. In Juno, an auto-enable generator block is used that monitors the ratio of **ATCLK** and **PCLKDBG** and generates an enable **PCLKDBGEN**. The block does not support dynamic changing of the input **ATCLK** and **PCLKDBG** clock ratios and its behavior is unpredictable under such circumstances.

For Juno, the Debug power-up request is an interrupt to the Cortex-M3 processor and is handled in the SCP boot code (boot ROM) and this performs the following:

- Request power-on of the **DBGSYS**.
- Runs clocks, releases **ATCLK**, **PLCKDBG**. Out of reset, **ATCLK** = **REFCLK**/16 and **PCLKDBG** = **ATCLK**/16. This is where the **PCLKDBGEN** is appropriately locked for **ATCLK**:**PCLKDBG** ratio of 16:1.
- Switches the **ATCLK** input from **REFCLK** to **SYSINCLK**. This step does not affect the **ATCLK**:**PCLKDBG** clock ratio and this remains 16:1. **PCLKDBGEN** remains the same as in the previous step.
- Program **ATCLK** divider such that **ATCLK = SYSINCLK**/4. This still does not affect the **ATCLK**:**PCLKDBG** ratio as **PCLKDBG** remains **ATCLK**/16. Therefore, **PCLKDBGEN** remains the same as before.
- Program the **PCLKDBG** divider to make **ATCLK=PCLKDBG**. This changes the ratio of these two clocks but the auto-enable generator for **PCLKDBGEN** is locked onto the initial 16:1 clock ratio set out of reset.

Therefore, because the ratio of the input clocks to the auto-enable generator is changed dynamically, its behavior becomes unpredictable.

Implications

Debug APB access to **ATCLK** components such as ETF, ETR, funnels, and replicator, results in a lock-up.

Workaround

Because the boot ROM cannot be updated, you can perform the following workarounds in software:

- Use alternate boot and ensure that your interrupt handler for debug powerup request performs a manual reset of the debug subsystem when it sets the **PCLKDBG** divider.
- If you use the Juno built-in boot ROM, ensure that trace is not used when the SCP is executing boot code, from SCP ROM. Also, ensure that the run-time boot code, SCP firmware, and debug power up request

interrupt handler perform a manual reset of the debug subsystem to ensure that **PCLKDBGEN** is locked on to the correct clock ratios.

831276: System Profiler Errata

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

The System Profiler within the ADP has the following issues:

1) Enabling filtering of AXI transactions by the AxSIZE parameter has no effect on the value of filtered events.
2) Not enabling the latency threshold filter, for read and write transactions, causes certain ABM counter events to never increment.
3) If no transactions end within a sample window and a counter is configured to count read or write minimum latency the counter value is `0x0` instead of `0xFFFF`.
4) A write of all zeros to the ID Filter Mask register of an ABM causes an update instead of being ignored.

Implications

The implications of these issues are:

1) Filtering by the size of the AXI transactions has no effect on the values of the filtered counters. The ABM behaves as though size filtering is disabled.
2) Unless latency threshold filtering is enabled the following ABM counter events do not update.
   - End of transactions for filtered transactions, `0x14`.
   - Sum of latency for filtered transactions, `0x15`.
   - Maximum latency for filtered transactions, `0x16`.
   - Minimum latency for filtered transactions, `0x17`.
3) The counter has the value of `0x0` instead of `0xFFFF` if counting minimum latency and no transactions ended within the sample window.
4) A write of all zeros to the ID Filter Mask register of an ABM causes the ID that is filtered to be treated as though the filter was disabled.

Workaround

The following workarounds are available:

1) No work around exists. Software should never enable size filtering.
2) Software should configure latency filtering to filter all transactions with a latency greater than 0. This enables the counters to update without causing any transactions to be filtered out.
3) Software should treat a value of `0x0` the same as a value of `0xFFFF` when reading a counter counting read or write minimum latency.
4) Software should never write all 0s to the ID Filter Mask register of an ABM.

831319: S32kCLK Generic Counter and SCP Firmware Watchdog can only be halted using level sensitive triggers

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b Fixed in c.

Description

The System Control Processor (SCP) contains a S32K_CLK Counter and an SCP Firmware Watchdog timer. These can be halted when they receive a trigger from the Cross Trigger Interface (CTI). The CTI can be programmed to select which trigger source should be used to halt the counter and watchdog by routing the source to **CTITIGOUT[1]** of the SCP CTI.

Juno contains an erratum that means pulse trigger events or short level events that are routed to halt the counter or watchdog might fail to halt them.

Implications

Trigger sources, **CTITRIGIN**s of all CTIs, that are active for a period, shorter than one 32kHz clock cycle, are unable to halt the 32kHz_CLK Counter and SCP Firmware Watchdog. When the counter is not halted, the 32kHz Generic Timer or SCP Firmware Watchdog might generate and interrupt or reset when the SCP is halted for debug.

Workaround

The primary use case for halting counters and watchdog timers is to support halted debug. For the Cortex-M3 SCP, this is achieved by programming the CTI to route the level sensitive **HALTED** signal to the counter and watchdog. Because this signal is level sensitive this functionality works correctly.

When not using halted debug, you can use the Cortex-M3 to manually control the value of **CTITRIGOUT[1]**, by performing the following operations:

- Unlock the CTI inside SCP by writing `0xC5ACCE55` to the CTI **Lock Access Register**, Offset: `0xFB0`.
- Enable the CTI by writing `0x1` to the **CTICONTROL** register, Offset:0x000.
- Enabling the **CTITRIGIN[0]** and map on to **CTICHOUT[0]** by writing `0x1` to **CTIINEN0** register, Offset: `0x020`. Use CTI channel 1/2/3 if channel 0 is used for other triggers.
- Enabling the **CTICHIN[0]** and map on to **CTITRIGOUT[1]** by writing `0x1` to **CTIOUTEN1** register, Offset: `0xA4`. Use the same channel as previous step.

832220: System deadlock if an ATB flush request is received when clusters in reset

Status

Affects: Juno Platform

Fault Type: Other Category C

Fault Status: Present in: b, c Open.

Description

The ATB asynchronous bridge resets **AFREADY** LOW when it should be reset HIGH. This affects the Cortex-A53 and Cortex-A57 cluster traces but not the following trace sources:

- Trace sources in the SCP sub-system. These are not reset when the system is running.
- STM and SP. These cannot be reset independently from the system.
- Both 64-bit ATB extension interfaces. These are tied-off with **AFREADYM** HIGH.

Implications

Any flush request (**AFVALID**) made to an ATB component with trace flush interface held in reset will result in system deadlock because the flush request never succeeds; **AFREADY** never goes HIGH, unless reset is released. However, it does not cause any adverse effect when a power domain is power-gated as the clamp values are correct in Juno and **AFREADY** is clamped HIGH.

Workaround

Check that both Cortex-A53 and Cortex-A57 clusters are out of reset before issuing flushes. Software running on DS-5 must check that the clusters are out of reset before issuing flushes.