Morello Platform Model

Version 1.0

Reference Guide

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Morello Platform Model

Reference Guide

Release Information

Document History

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1000-00	29 October 2020	Non-Confidential	First release

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Contents
Morello Platform Model Reference Guide

Preface

This preface introduces the *Morello Platform Model Reference Guide*.

It contains the following:

About this book

This document describes the Morello Platform Model, which is a software reference platform based on real hardware that enables partners and developers to develop applications using the CHERI-based security features in Morello.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter contains a high-level description of the Morello Platform Model, and gives links to further information.

Chapter 2 Get started

This chapter describes how to download and install the Morello Platform Model package, and verify the installation.

Chapter 3 Reference information

This chapter provides reference information for the FVP including command-line options, lists of model components, and a list of differences between the FVP implementation and the Morello specification.

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See the *Arm® Glossary* for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`

Denotes language keywords when used outside example code.

`<and>`

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

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- *Technical Support*.
- *Arm® Glossary*.

Chapter 1
Introduction

This chapter contains a high-level description of the Morello Platform Model, and gives links to further information.

It contains the following sections:

1.1 About the Morello Platform Model

The Morello Platform Model is a software model of the Morello System on Chip (SoC) hardware platform.

It is freely available for download from the Arm Developer website, does not require a license, and runs on Linux host machines only.

The Morello Platform Model is a Fixed Virtual Platform (FVP). An FVP is a pre-built model that consists of a hierarchy of model components connected together to form a system. Although the composition of an FVP is fixed, you can configure its behavior using parameters. You can also load plug-in libraries to provide extra functionality.

FVPs enable applications and operating systems to be written and debugged without the need for real hardware. They work by translating Arm instructions into the instruction set of the host dynamically and use optimization techniques to improve performance. So, while they are functionally accurate, they do not provide accurate timing information or cycle counts.

FVPs have several benefits over the hardware they model:

Early availability
FVPs are available ahead of hardware, and unlike hardware, availability is not limited.

Software compatibility
As the same software stack runs on both the model and the hardware, you can use the same toolchain to build for both targets.

Configurable
FVPs can be easily customized by using parameters to test different configurations. To see the available parameters, run the FVP with the `--list-params` option.

Debuggable
The Morello Platform Model supports the CADI interface which enables debuggers to connect to it and debug it. You can use Arm Debugger in the Arm Development Studio Morello Edition to work with the Morello Platform Model.

Trace support
The Morello Platform Model supports Model Trace Interface (MTI), which enables you to use plug-ins to output trace information from the FVP. The Morello Platform Model package includes several pre-built trace plug-ins.

1.2 High-level block diagram

A simplified block diagram showing the SoC and board peripherals.

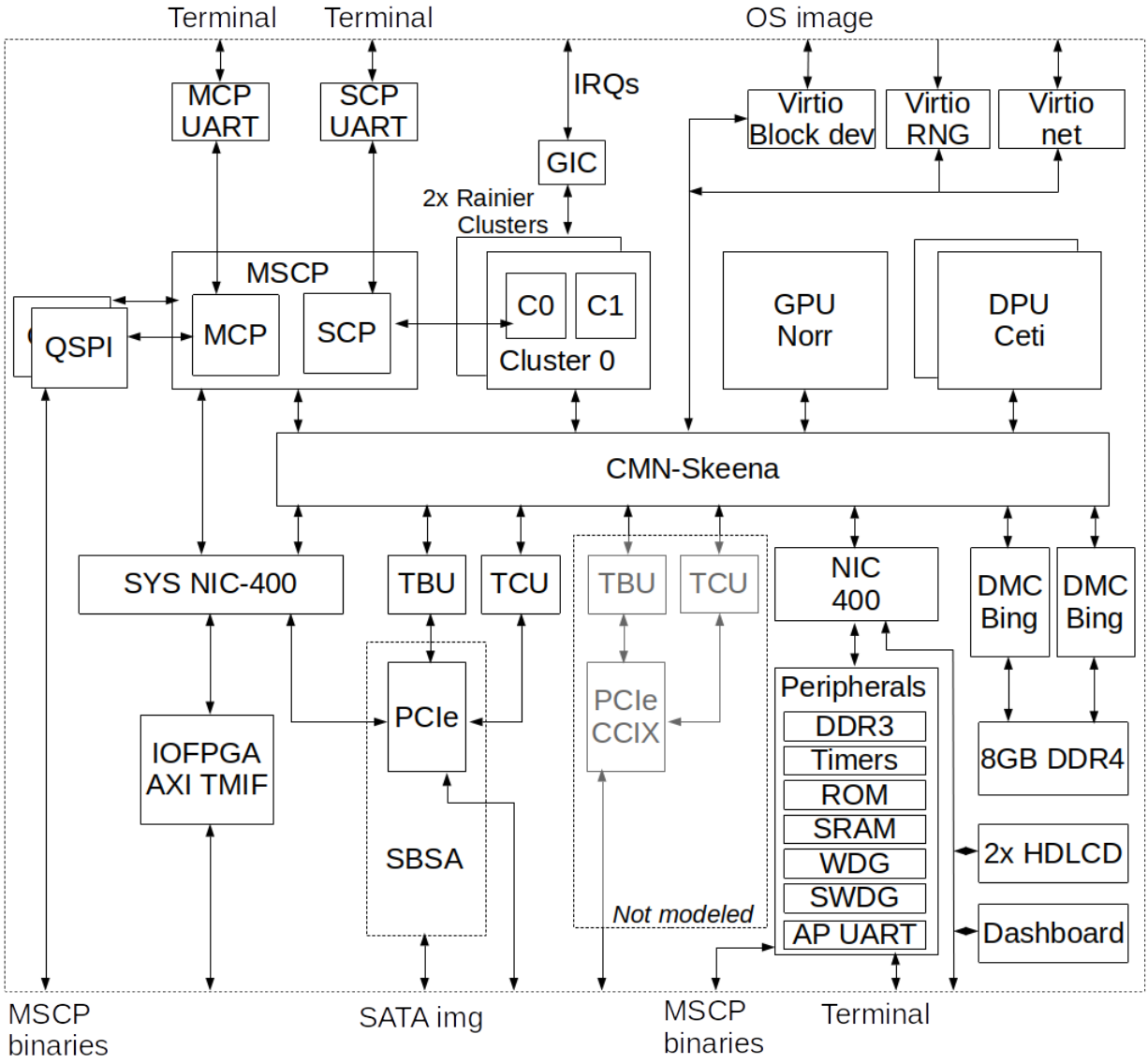

Figure 1-1 Morello Platform Model system block diagram

1.3 Host prerequisites

The Morello Platform Model supports the following host operating systems and compilers.

Operating system

The FVP requires a Linux x86-64 host. It has been tested with Ubuntu 18.04 but should also work with later versions.

The following GCC-6.4 compatible libraries must be installed on the host:

- `/lib64/ld-linux-x86-64.so.2`
- `libatomic.so.1`
- `libc.so.6`
- `libdbus-1.so.3`
- `libdl.so.2`
- `libgcc_s.so.1`
- `libgcrypt.so.20`
- `libgpg-error.so.0`
- `liblz4.so.1`
- `liblzma.so.5`
- `libm.so.6`
- `libpthread.so.0`
- `librt.so.1`
- `libstdc++.so.6`
- `libsystemd.so.0`
- `linux-vdso.so.1`

Other requirements

- A shell compatible with `sh`, such as `bash` or `tcsh`. If you want to change terminals use the `terminal_command` parameter to select a different console program.
- If you want to use the host GPU for rendering pixels, you must install the Mali™ OpenGL ES emulator from *OpenGL ES Emulator Downloads*. Follow the steps described in the documentation included in the download package.

1.4 Additional reading

This section lists other publications and websites from Arm that are relevant to the Morello Platform Model.

- To learn more about the Morello program and architecture, see *Arm Morello Program*.
- To learn more about the Open Source Software targeting this FVP, see *Morello Project*.
- Morello Technical Reference Manual (TRM) at *Arm Ecosystem FVPs*.
- To learn about software development for Morello using Arm Development Studio, read *Arm Development Studio Morello Edition Getting Started Guide* and *Arm Development Studio Morello Edition User Guide*.
- To learn more about Fast Models, see *Fast Models* on Arm Developer.

Chapter 2
Get started

This chapter describes how to download and install the Morello Platform Model package, and verify the installation.

It contains the following sections:

2.1 Install the package

The Morello Platform Model package is installed using a command-line installer.

Follow these steps to download and install the package:

Procedure

1. Download the package from the *Morello Development Tools* page.
2. Uncompress the tarball:

   ```
   tar -xzf FVP_Morello_x.xx_xxx.tgz
   ```

   Where `x` indicates the version number. For example, `FVP_Morello_0.10_310.tgz`.
3. Run the installation shell script:

   ```
   ./FVP_Morello.sh
   ```
4. Read and agree to the terms and conditions and select the directory to install to.
5. When installation has finished, the model, called `FVP_Morello`, can be found in `<install_dir>/models/Linux64_GCC-x.x/`.

   Where `x` indicates the version number. For example, `/Linux64_GCC-6.4`.

To uninstall the package, remove the installation folder.

2.2 What is in the package?

The package installs the FVP binary, libraries that it requires, and some useful plug-ins.

The contents of the Morello Platform Model installation are:

```
FVP_Morello/
├── doc
│   ├── Morello_FVP_ReleaseNotes.txt
│   └── morello_platform_model_rg_102225_0100_00_en.pdf
├── install_history
├── license_terms
│   ├── license_agreement.txt
│   ├── redistributables.txt
│   ├── supplementary_terms.txt
│   └── third_party_licenses.txt
├── models
│   └── Linux64_GCC-6.4
│       ├── checkerrcode.ini
│       ├── cmn600_morello_skeena_topology.yml
│       ├── FVP_Morello
│       ├── FVP_Morello.so
│       ├── libarmctmodel.so
│       ├── libMAXCOREInitSimulationEngine.3.so
│       ├── libnomali.so
│       ├── libReconciler.so
│       ├── libSDL2-2.0.so.0.10.0
│       ├── settings.ini
│       └── Sidechannel.so
├── plugins
│   └── Linux64_GCC-6.4
│       ├── ArchMsgTrace.so
│       ├── GDBRemoteConnection.so
│       ├── GenericCounter.so
│       ├── GenericTrace.so
│       ├── ListTraceSources.so
│       ├── MTS.so
│       ├── TarmacText.so
│       ├── TarmacTrace.so
│       └── ToggleMTIPlugin.so
└── sw
    └── ARM_Fast_Models_FVP_Morello
        └── rev
8 directories, 28 files
```

doc

Contains release notes and a PDF document of the Morello Platform Model Reference Guide (This document).

license-terms

Contains the copyright and license information for third-party software, and the standard FVP end-user license agreement.

models

Contains the GCC build of the Morello Platform Model, `FVP_Morello`, and the libraries that it needs to run.

plugins

Plug-ins are libraries that provide extra functionality for the FVP, for instance trace output. To load a plug-in, specify it when launching the FVP using the `--plugin` command-line option, or use the `FM_TRACE_PLUGINS` environment variable.

The following plug-ins are included in the Morello Platform Model package. Most of them are documented in the Fast Models Reference Manual, see *Plug-ins for Fast Models* for details.

ArchMsgTrace

Prints warnings and error messages to stdout or to a file when the core executes code that is unsafe or not recommended.

GDBRemoteConnection

Allows the model to be debugged using GDB.

GenericCounter
At the end of the simulation prints to stdout the number of occurrences of a specific trace source.

GenericTrace
Prints trace information, specified using a comma-separated list of trace sources, to `stdout` or to a file.

ListTraceSources
Displays a list of the trace sources that the model provides, without running the model.

MTS
Used by Arm Debugger in Arm Development Studio Morello Edition to report instructions and exceptions that were captured during the simulation.

TarmacText
Extracts the architectural execution trace, known as tarmac, of the processor. This might include instructions, program flow, or memory accesses. TarmacText extracts the trace in a textual form and saves it in a file.

TarmacTrace
Prints tarmac trace information to stdout or to a file. Parameters control the amount and type of information that is traced. The tarmac trace file format is documented in the Fast Models Reference Manual, see *TarmacTrace file format*. Some changes to the file format have been made for Morello. For details, see *3.4 Morello-specific changes to tarmac trace* on page 3-26.

ToggleMTIPlugin
Toggles trace generation on or off during the simulation. See *3.5 ToggleMTIPlugin* on page 3-28 for details.

2.3 Verify the installation

Run the FVP manually from the command line to verify that it has installed correctly on the host machine.

Note

You would not typically launch the Morello Platform Model in this way. For most expected use cases, the FVP requires the Open Source Software stack and is launched using a script to simplify the process, see *2.4 What software is available?* on page 2-18 for details.

Procedure

1. In the terminal, change to the directory where you installed the Morello Platform Model. For example: `cd ~/FVP_Morello/models/Linux64_GCC-6.4`
2. Launch the Morello Platform Model with the `--list-params` option, for example: `./FVP_Morello --list-params`.

   The `--list-params` option prints a list of model parameters to the terminal. For a description of all the available command-line options, see *3.1 Command-line options* on page 3-20.

2.4 What software is available?

The Morello Platform Model is typically used with a compatible Open Source Software (OSS) stack.

- Arm provides an integrated OSS stack for the Morello platform with scripts to build and run it.
- Arm Development Studio Morello Edition provides comprehensive support for all software development projects on the Morello platform. It also provides a selection of examples to help you get started with the Morello platform.
- An LLVM compiler with Morello support is available, with Morello code examples included.

To find out more about the OSS stack configurations supported on the model and the Morello-aware LLVM toolchain, see the *Morello software page*.

Note

For technical support, see the *Morello forum* on Arm Community.

Chapter 3
Reference information

This chapter provides reference information for the FVP including command-line options, lists of model components, and a list of differences between the FVP implementation and the Morello specification.

Note

- For more information about the Morello program see the *Arm Morello Program page*.
- For the Morello platform memory maps and interrupt maps, see the Morello Technical Reference Manual (TRM).
  - For the memory maps, see chapter 4.2.
  - For the interrupt maps, see chapter 4.3.
- For information about additional devices available on the Morello Platform Model, see *3.3 Morello Platform Model notes and limitations* on page 3-25.

It contains the following sections:

3.1 Command-line options

Use these options to configure the FVP when launching it from the command line. Each table groups together related options. For a listing of these options with brief descriptions, run the model with `--help`.

Table 3-1 CADI related

Short form	Long form	Description
`-S`	`--cadi-server`	Start a CADI server. This option allows a CADI-enabled debugger to connect to targets in the simulation. To shut down the server, return to the command window that you used to start the model and press **Ctrl+C**.
`-R`	`--run`	Run the simulation immediately after the CADI server is started. Use this option with `--cadi-server`. The default is to wait until the debugger has connected before running the simulation.
`-L`	`--cadi-log`	Log all CADI function calls made during the simulation into XML files. One log file is created for each CADI target. The log files are created in the current working directory. The filename format is: `CADIlog-<TargetInstanceName>-<ProcessID>.xml`
`-p`	`--print-port-number`	Print the port number on which the CADI server is listening. **Tip** This option can be useful if you need to specify the port number when you connect a client to the debug server.

Table 3-2 Outputting information

Short form	Long form	Description
	`--list-instances`	Print a list of model instances to standard output, then exit the simulation. Use this option to help identify the correct syntax for configuration files, and to find out what instances the target supplies.
`-l`	`--list-params`	Print a list of model parameters to standard output, then exit the simulation. **Tip** If you load a plug-in, this option also lists the plug-in parameters.
	`--list-regs`	Print model register information to standard output, then exit the simulation.
	`--check-regs`	Same as `--list-regs` but with extra consistency checks on the CADI register API.
	`--list-memory`	Print memory information to standard output, then exit the simulation.

Table 3-2 Outputting information (continued)

Short form	Long form	Description
`-o`	`--output` *`filename`*	Redirect output from the `--list-instances`, `--list-memory`, `--list-params`, and `--list-regs` options to a file. If this option is used with `--list-params`, the contents of the output file are formatted correctly for use as input by the `--config-file` option.
	`--dump` *`file@address,size`*	Dump a section of memory to a file at model shutdown. This option can be specified multiple times. The full syntax is: `--dump [instance=]file@[memspace:]address,size` **Tip** To see the list of instances and memory spaces, use the `--list-memory` option.
	`--data` *`file@address`*	Write raw data contained in *`file`* to the specified address. This option can be specified multiple times. The full syntax is: `--data [instance=]file@[memspace:]address`
	`--log` *`filename`*	Log all SystemC reports into *`filename`*.
	`--stat`	Print the following performance statistics on simulation exit: **Simulated time** An estimate of the time that the workload would have taken on the modeled hardware. **User time** Time in wall clock seconds that the host CPU spent running in user mode. **System time** Time in wall clock seconds that the host CPU spent running in system mode. **Wall time** Time in wall clock seconds between the simulation starting and stopping. **Performance index** An estimate of the accuracy of the simulation performance. This value is Simulated time divided by Wall time.
`-P`	`--prefix`	Prefix each line of semihosting output with the name of the target instance.
`-h`	`--help`	Print the help message and exit.
	`--version`	Print version information.
`-q`	`--quiet`	Suppress informational output.

Table 3-3 Run control

Short form	Long form	Description
	`--cpulimit` *n*	Maximum number of wall-clock seconds for the simulation process to be active. This value excludes simulation startup and shutdown. This option is ignored if a debug server is started. The default is unlimited.
	`--cyclelimit` *n*	Maximum number of cycles to run. This option is ignored if a debug server is started. The default is unlimited.
`-T`	`--timelimit` *n*	Maximum number of wall-clock seconds for the simulation to run, excluding startup and shutdown. To terminate the model immediately after initialization, specify `--timelimit 0`.
	`--simlimit` *n*	Maximum number of seconds to simulate. This option is ignored if a debug server is started. The default is unlimited. Like the `Simulated time` value output by `--stat`, this value is measured in simulation seconds, not wall-clock seconds.
`-b`	`--break` [*instance*=] *address*	Set a program breakpoint on the address of an instruction. This option can be specified multiple times. For an FVP with multiple cores, you must specify an instance, for example: `-b FVP_Morello.cluster0.cpu0=0x80000278`
	`--start` [*instance*=] *address*	Set the initial PC value to this address, overriding the `.axf` start address. **Note** • Use this option if you do not want the CPU to start executing at the default reset address. You do not normally need to do this if you are loading an ELF file using `--application`. • This option can be used with `--data` to load binary data that is not in an ELF file.

Table 3-4 Timing and performance

Short form	Long form	Description
	`--cpi-file` *filename*	Use *filename* to set the Cycles Per Instruction (CPI) class. For more information, see *CPI files* in Fast Models User Guide.
`-Q`	`--quantum` *n*	Number of ticks to simulate for each quantum. The default is 10000.
`-M`	`--min-sync-latency` *n*	Number of ticks to simulate before synchronizing. Events that occur at a higher frequency than this value are missed. The default is 100.

Table 3-5 Model configuration

Short form	Long form	Description
`-C`	`--parameter` *`instance.parameter=value`*	Set a parameter. This option can be specified multiple times. Specify the full hierarchical name of the parameter. This option is also used to set plug-in parameters.
`-f`	`--config-file` *`filename`*	Load parameters from a configuration file.

Table 3-6 Loading a plug-in or application

Short form	Long form	Description
`-a`	`--application` [*`instance`*=] *`filename`*	Load an application. Specify the core instance to load the application image onto, or use * to load it on multiple cores, for example: `-a cluster0.cpu*=`*`file`*
	`--plugin` *`filename`*	Load the plug-in *`filename`*. This option can be specified multiple times. You can also load plug-ins using the `FM_TRACE_PLUGINS` environment variable. For more information, see *Plug-ins for Fast Models* in Fast Models Reference Manual.
	`--trace-plugin` *`filename`*	Load a trace plug-in. **Note** This option is deprecated. Use `--plugin` instead.

3.2 CMN-Skeena topology configuration and connection diagram

This figure shows the CMN-Skeena topology configuration diagram and a list of external connections.

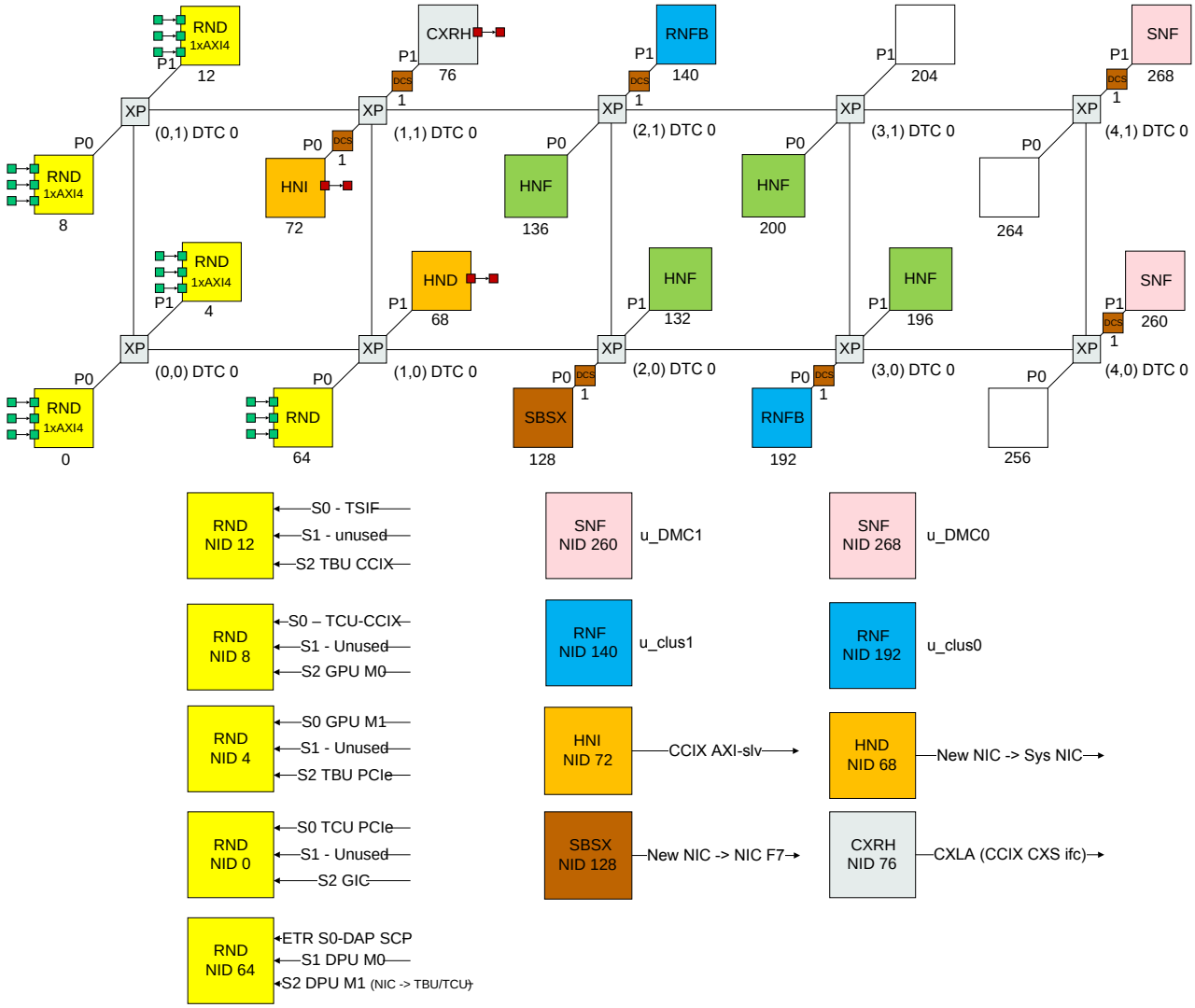

Figure 3-1 CMN-Skeena topology configuration and connection overview

3.3 Morello Platform Model notes and limitations

The model is implemented according to the Morello TRM with some exceptions.

- Dual DPU Ceti has been integrated into the model.
- PCIe CCIX has not been integrated into the model.

Trace

- A number of Morello-specific trace sources have been added, as well as additional fields to existing trace sources. For details about the trace sources, use the `ListTraceSources` plugin as explained in the *Fast Models Reference Manual*.
- A number of changes have been made to the TarmacTrace format to represent Morello-specific state and events. These are documented in the *Morello Technical Reference Manual*.
- Some Morello-specific states are not fully captured in the trace:
  - The clearing of capability tags performed by non-capability stores is not reflected in the trace.
  - Executive/Restricted (both transitions and the current state) are not directly reflected in the trace, although can be deduced from the traced value of PCC.
  - Writes to `X` registers are sometimes inconsistently traced as writes to the corresponding `C` register. When they are traced as writes to the `X` register, zero-extension into the upper bits of the capability is implicit. The `OLD_VALUE` field may be incorrect between writes to the same `X` and `C` register.
  - The squashing of mutable permissions and the tag of a capability loaded from memory using a capability without `LoadCap` or `MutableLoad` permissions is not reflected in the trace. Instead, the traced value can either include or exclude the squashing, controlled by the cluster parameter `trace_squashed_mutable_perms_and_tag_in_loads`.

    These issues are expected to be addressed in a future release of the model.

Performance

The performance of the model, and in particular memory accesses, when making use of Morello features, is reduced. This is expected to be addressed in a future release of the model

Rainier implementation-defined registers and behavior

For details of the Morello-specific `IMPLEMENTATION DEFINED` Performance Monitor Unit (PMU) events, see the *Morello program and architecture details*.

Additional devices

Additional devices present in the Morello Platform Model but which are not present in the hardware:

Device	Memory map	IRQ
`virtioblockdevice`	`0x1C17_0000` to `0x1C17_FFFF`	96
`virtio_net`	`0x1C18_0000` to `0x1C18_FFFF`	102
`virtio_rng`	`0x1C19_0000` to `0x1C19_FFFF`	101

3.4 Morello-specific changes to tarmac trace

Tarmac trace is a format for tracing code executing on an Arm core, for example branches, memory accesses, or cache hits or misses. Examining tarmac trace is a useful technique in debugging software.

To generate tarmac trace on the FVP, you must load the `TarmacTrace.so` plug-in at simulation startup. The plug-in attaches to the model and registers for specific trace events that might occur during the simulation.

The TarmacTrace plug-in file format is documented in *TarmacTrace* in the Fast Models Reference Manual. The following topics describe the changes that have been made to TarmacTrace for Morello.

This section contains the following subsections:

3.4.1 File format changes

New syntax has been added for 129-bit addresses derived from a capability in Morello.

As stated in the Fast Models Reference Manual, 64-bit addresses are written as either:

- 8 hex digits, if the value can be represented in 32 bits.
- 16 hex digits otherwise.

When Morello is enabled, for 129-bit addresses derived from a capability, the value is written as up to 33 hex digits representing the 129 bits of the capability. The tag and the bottom 64 bits are separated using a vertical bar (`|`). The bottom 64 bits are written as described for a 64-bit address. When a physical address is present, the virtual address is surrounded by parentheses.

The following example shows a virtual address derived from a capability with a value of `0x1ffffc0000001000500000000080000000`, and a corresponding physical address of `0x90000000`:

```
(1|ffffc00000010005|80000000):90000000
```

Refer to *TarmacTrace file format* in the Fast Models Reference Manual.

3.4.2 Instruction trace changes

An extra instruction set specifier, `C`, for C64 has been added for Morello.

The new syntax is:

```
[A|T|X|O|C]
```

Refer to *Instruction trace* in the Fast Models Reference Manual.

3.4.3 Register trace changes

New syntax has been added for 129-bit capability registers in Morello.

The following example output shows how these registers are traced when the value changes:

```
61 clk IT (61) 1|ffffc00000010005|80010bc0 c2984120 O EL3h_s : MRS      c0,DDC_EL0
61 clk R C0 1|ffffc00000010005|0000000000000000
```

These registers have the same format as 64-bit registers, with the addition of a vertical bar (`|`) separating the capability tag, bits [127:64], and bits [63:0].

Refer to *Register trace* in the Fast Models Reference Manual.

3.4.4 Processor memory access trace changes

New syntax has been added for capability tag transfers in Morello.

The new syntax is:

```
<time> <scale> {<cpu>} [M|C]<rw><sz><attrib> <addr> <data>
```

The changes for Morello are:

[M|C]

M Data transfer.

C Capability tag transfer, when Morello is enabled.

<sz>

For data transfers, the size of the data transfer in bytes, 1, 2, 4, or 8.

For capability tag transfers, the size of the capability tag transfer in bits. That is, the number of capability tags transferred.

<data>

Hexadecimal value of the data transferred. The data padding is according to the size of the transfer. Data of 64 bits or more contains an underscore (_) separator every eight characters (32 bits).

For capability tag transfers, each digit represents a single tag. For example, 1111 represents four tags, each with a value of 1.

Refer to *Processor memory access trace* in the Fast Models Reference Manual.

Related information

TarmacTrace

3.5 ToggleMTIPlugin

Generating trace throughout the simulation can result in very large trace files and slow down the simulation. ToggleMTIPlugin enables you to turn trace generation on or off during the simulation to avoid these problems.

There are two alternative ways to use the plug-in:

Note

You cannot use both of these methods in the same simulation session.

- Using the plug-in parameters `use_hlt = 1` and `hlt_imm16 = #imm16`.

  This pair of plug-in parameters is used in combination with the application using `HLT #imm16` for toggling Model Trace Interface (MTI) callbacks. For these parameters to take effect, you must also set the corresponding parameters on the core model that is running the application:

  enable_trace_special_hlt_imm16
  : If true, enables the parameter `trace_special_hlt_imm16`.

  trace_special_hlt_imm16
  : Specifies an integer which, when used as the operand to an `HLT` instruction, causes the usual `HLT` execution to be skipped. If the integer matches the value specified in `hlt_imm16`, tracing is turned on or off.

- Using the plug-in parameter `disable_mti_runtime = true`.

  You can set or unset this parameter at runtime using a CADI client, for instance Model Debugger. When set to `true`, trace is disabled.

Each parameter is prefixed with `TRACE.ToggleMTIPlugin`, for example:

```
TRACE.ToggleMTIPlugin.diagnostics
```

Table 3-7 ToggleMTIPlugin parameters

Parameter	Type	Allowed values	Default value	Runtime	Description
`diagnostics`	`bool`	`true`, `false`	`false`	`false`	Print diagnostics.
`disable_mti_from_start`	`bool`	-	`false`	`false`	Enable or disable MTI callbacks from start of simulation.
`disable_mti_runtime`	`bool`	`true`, `false`	`false`	`true`	Enable or disable MTI callbacks at runtime.
`hlt_imm16`	`int`	-	`0xf000`	`false`	16-bit integer used in `HLT` instructions that is used by this plug-in.
`use_hlt`	`bool`	-	`true`	`false`	If true, use `HLT #imm16` instruction to toggle MTI behavior.

Example

For example, the following plug-in parameters cause tracing to begin when `HLT #1` is executed:

```
-C TRACE.ToggleMTIPlugin.use_hlt=1 \
-C TRACE.ToggleMTIPlugin.hlt_imm16=1 \
-C TRACE.ToggleMTIPlugin.disable_mti_from_start=1
```

3.6 Morello Platform Model instances

FVP_Morello contains the following instances:

Table 3-8 FVP_Morello instances

Name	Type	Description
Morello_Top	Morello_Top	Top level component of Morello platform model.
Morello_Top.board	N1SDP_Morello_Board	The Morello development board.
Morello_Top.board.CLUSREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.CPU0REFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.CPU1REFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.DMCREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.DPUREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.GPUREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.HDLCDPLL	PLLControl	Simulate PLL clock frequency control logic.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.board.HDLCDPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.INTREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.IOFPGA_CLK24M	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.IOFPGA_PXLCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.PXLREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.REFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.S32KCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.SYSREFCLK	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.board.ddr3	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.ddr_spd	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.dram	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.dual_timer_0_1	*SP804_Timer*	Arm Dual-Timer Module(SP804).
Morello_Top.board.dual_timer_0_1.clk_div0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.dual_timer_0_1.clk_div1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.dual_timer_0_1.counter0	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.board.dual_timer_0_1.counter1	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.board.dual_timer_2_3	*SP804_Timer*	Arm Dual-Timer Module(SP804).
Morello_Top.board.dual_timer_2_3.clk_div0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.dual_timer_2_3.clk_div1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.dual_timer_2_3.counter0	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.board.dual_timer_2_3.counter1	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.board.dual_timer_clk	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.dvi_i2c	*DummyAPB*	DummyAPB.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.board.emmc	*MMC*	Generic Multimedia Card.
Morello_Top.board.emmc_config	*PL180_MCI*	Arm PrimeCell Multimedia Card Interface (PL180).
Morello_Top.board.gic400	*GIC_400*	GIC-400 Generic Interrupt Controller.
Morello_Top.board.gpio_0	*PL061_GPIO*	Arm PrimeCell General Purpose Input/Output(PL061).
Morello_Top.board.gpio_1	*PL061_GPIO*	Arm PrimeCell General Purpose Input/Output(PL061).
Morello_Top.board.hdlcd	*PL370_HDLCD*	Arm PrimeCell HD Color LCD Controller (Nominal Designation PL370).
Morello_Top.board.hdlcd.timer	*ClockTimerThread*	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.board.hdlcd.timer.timer	*ClockTimerThread64*	A ClockTimerThread(64) is a drop-in replacement for ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.board.hdlcd.timer.timer.thread	*SchedulerThread*	A SchedulerThread instance represents a co-routine thread in the simulation.
Morello_Top.board.hdlcd.timer.timer.thread_event	*SchedulerThreadEvent*	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
Morello_Top.board.hostbridge	*HostBridge*	Host Socket Interface Component.
Morello_Top.board.i3c	*DummyAPB*	DummyAPB.
Morello_Top.board.mcp_backup_boot_mem	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.mscp_qspi	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.board.mscp_qspi_loader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.board.msd_config	*PL180_MCI*	Arm PrimeCell Multimedia Card Interface (PL180).
Morello_Top.board.msd_mmc	*MMC*	Generic Multimedia Card.
Morello_Top.board.pcie_i2c	*DummyAPB*	DummyAPB.
Morello_Top.board.pl050_kmi0	*PL050_KMI*	Arm PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.board.pl050_kmi0.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.pl050_kmi1	*PL050_KMI*	Arm PrimeCell PS2 Keyboard/Mouse Interface(PL050).
Morello_Top.board.pl050_kmi1.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.ps2keyboard	*PS2Keyboard*	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
Morello_Top.board.ps2mouse	*PS2Mouse*	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
Morello_Top.board.qspi_config	*DummyAPB*	DummyAPB.
Morello_Top.board.rtc	*PL031_RTC*	Arm PrimeCell Real Time Clock(PL031).
Morello_Top.board.s100hz_clk	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.scp_backup_boot_mem	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.smc	*DummyAPB*	DummyAPB.
Morello_Top.board.smsc_91c111	*SMSC_91C111*	SMSC 91C111 ethernet controller.
Morello_Top.board.sram	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.board.sys_ctrl	*SP810_SysCtrl*	Only EB relevant functionalities are fully implemented.
Morello_Top.board.sys_ctrl.clkdiv_clk0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.board.sys_ctrl.clkdiv_clk1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.sys_ctrl.clkdiv_clk2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.sys_ctrl.clkdiv_clk3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.sys_regs	Morello_SysRegs	Morello Development Board System Registers.
Morello_Top.board.tbgp	TestbedGPIOConnector	Tool for receiving GPIO signals and reporting test success/failure.
Morello_Top.board.terminal_uart0_board	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.board.terminal_uart1_board	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.board.uart0	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.board.uart0.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.uart1	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.board.uart1.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.board.virtioblockdevice	*VirtioBlockDevice*	virtio block device.
Morello_Top.board.watchdog	*SP805_Watchdog*	Arm Watchdog Module(SP805).
Morello_Top.css	N1SDP_Morello_CSS	N1SDP Compute Subsystem.
Morello_Top.css.ap_refclk	*MemoryMappedGenericTimer*	Arm Generic Timer.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c0ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c0ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c0core0ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c0core0ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core0ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c0core0ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core0_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c0core1ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c0core1ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core1ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c0core1ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core1_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c0core2ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c0core2ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core2ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c0core2ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core2ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c0core3ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core3ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core3ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c0core3ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c1ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c1ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c1core0ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core0ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core0ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c1core0ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core0ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core0_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c1core1ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c1core1ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core1ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c1core1ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core1ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core1_clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.c1core2ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c1core2ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core2ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c1core2ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core2ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl	ScalableClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.c1core3ClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core3ClkCtrl.clkDiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkDiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.c1core3ClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.c1core3ClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.clock24MHz	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.cluster0	Cluster_ARM_Morello	Arm Morello Cluster CT model.
Morello_Top.css.cluster0.cpu0	ARM_Morello	Arm Morello CT model.
Morello_Top.css.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
Morello_Top.css.cluster0.cpu0.l1dcache	*PVCache*	PV Cache.
Morello_Top.css.cluster0.cpu0.l1icache	*PVCache*	PV Cache.
Morello_Top.css.cluster0.cpu0.l2cache	*PVCache*	PV Cache.
Morello_Top.css.cluster0.cpu1	ARM_Morello	Arm Morello CT model.
Morello_Top.css.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
Morello_Top.css.cluster0.cpu1.l1dcache	*PVCache*	PV Cache.
Morello_Top.css.cluster0.cpu1.l1icache	*PVCache*	PV Cache.
Morello_Top.css.cluster0.cpu1.l2cache	*PVCache*	PV Cache.
Morello_Top.css.cluster1	Cluster_ARM_Morello	Arm Morello Cluster CT model.
Morello_Top.css.cluster1.cpu0	ARM_Morello	Arm Morello CT model.
Morello_Top.css.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
Morello_Top.css.cluster1.cpu0.l1dcache	*PVCache*	PV Cache.
Morello_Top.css.cluster1.cpu0.l1icache	*PVCache*	PV Cache.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.cluster1.cpu0.l2cache	*PVCache*	PV Cache.
Morello_Top.css.cluster1.cpu1	ARM_Morello	Arm Morello CT model.
Morello_Top.css.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
Morello_Top.css.cluster1.cpu1.l1dcache	*PVCache*	PV Cache.
Morello_Top.css.cluster1.cpu1.l1icache	*PVCache*	PV Cache.
Morello_Top.css.cluster1.cpu1.l2cache	*PVCache*	PV Cache.
Morello_Top.css.cmn600	*CMN600*	CCN CMN600 Interconnect.
Morello_Top.css.cmn600.cmn600_cache	CMN600Cache	CMN600 Interconnect Cache.
Morello_Top.css.debugUnit	Ashbrook_DebugUnit	currently all stubs with IDs.
Morello_Top.css.debugUnit.dummy_coresight_registers	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.debugUnit.dummy_etrsmmu_registers	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_0	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_1	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_2	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_3	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_4	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_5	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_6	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_7	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_8	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_9	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_abm_a	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_cpm_b	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_syspr of_mctlr	*DummyAPB*	DummyAPB.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.debugUnit.dummy_sysprof_mpm_c	*DummyAPB*	DummyAPB.
Morello_Top.css.debugUnit.dummy_sysprof_registers	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.debugUnit.reserved_Mem	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.display_processor	*D71*	Arm D71 Display Processor.
Morello_Top.css.dp_msi_rewriter_pcie	*MSIRewriter*	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
Morello_Top.css.dp_msi_rewriter_smmu	*MSIRewriter*	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
Morello_Top.css.dpuClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.dpuClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.dpuClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpuClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.dpu_smmu	*MMU_600*	SMMUv3 compliant device.
Morello_Top.css.exclusive_monitor_0	*PVBusExclusiveMonitor*	Global exclusive monitor.
Morello_Top.css.exclusive_monitor_1	*PVBusExclusiveMonitor*	Global exclusive monitor.
Morello_Top.css.exclusive_monitor_4	*PVBusExclusiveMonitor*	Global exclusive monitor.
Morello_Top.css.exclusive_monitor_5	*PVBusExclusiveMonitor*	Global exclusive monitor.
Morello_Top.css.exclusive_monitor_6	*PVBusExclusiveMonitor*	Global exclusive monitor.
Morello_Top.css.generic_watchdog	*MemoryMappedGenericWatchdog*	Arm Generic Watchdog.
Morello_Top.css.gic_distributor	*GIC600*	GIC-600.
Morello_Top.css.gpu	*Mali_G76*	Arm Mali-G76 GPU.
Morello_Top.css.gpuClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.gpuClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.gpuClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.gpuClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.hni_logger	*PVBusLogger*	Bus Logger.
Morello_Top.css.mcp	SGI_575_MCP	-
Morello_Top.css.mcp.AP2MCP_MHU	Juno_SCP_MHU	Juno Message Handling Unit.
Morello_Top.css.mcp.AP2MCP_NONSEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.AP2MCP_SEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.DTCRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.GenericTimerRef	*MemoryMappedGenericTimer*	Arm Generic Timer.
Morello_Top.css.mcp.ITCRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.ROM	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.css.mcp.ROMloader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.css.mcp.SCP2MCP_MHU	Juno_SCP_MHU	Juno Message Handling Unit.
Morello_Top.css.mcp.SCP2MCP_NONSEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.SCP2MCP_SEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.mcp.armcortexm7ct	ARM_Cortex-M7	Arm CORTEXM7 CT model.
Morello_Top.css.mcp.clock24MHz	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.mcp.cmsdk_watchdog	CMSDK_Watchdog	Arm Watchdog Module.
Morello_Top.css.mcp.exclusive_squasher	*PVBusExclusiveSquasher*	Squashes the exclusive attribute on bus transactions.
Morello_Top.css.mcp.mcpClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.mcp.mcpClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.mcp.mcpClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.mcp.mcpClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcpClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcp_addr_tran	Kits2_AddrTran	Address Translator for Ashbrook Subsystem.
Morello_Top.css.mcp.mcp_pik	PIK_MCP_Ashbrook	Ashbrook MCP Power Integration Kit.
Morello_Top.css.mcp.mcp_pik.ws1_timer	Kits2_Timer	Kits2 Timer.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.mcp.mcp_pik.ws1_timer.clk_div	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.mcp_pik.ws1_timer.counter	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.css.mcp.pl011_uart0_mcp	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.mcp.pl011_uart0_mcp.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.pl011_uart1_mcp	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.mcp.pl011_uart1_mcp.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.mcp.reserved_Mem	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.mcp.secure_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mcp.secure_squasher	PVBusSecureSquasher	Squashes the secure attributes on bus transactions.
Morello_Top.css.mcp.terminal_uart0	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.mcp.terminal_uart1	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.mcp_sec_ctrl	Kits2_Privileged_to_Secure_Mapper	Kits2 Security Enabler.
Morello_Top.css.mem	SGI_575_MemoryElement	Memory Element with Config of DMC # Check.
Morello_Top.css.mem.apb_chn_filter0	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.apb_chn_filter1	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.apb_chn_filter2	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.apb_chn_filter3	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.dmc0	Infra_MemoryElement_DMC_Bing	Memory Element with DMC-Bing.
Morello_Top.css.mem.dmc0.dmc	DMC_Bing	Arm DMC-Bing Dynamic Memory Controller.
Morello_Top.css.mem.dmc0.dmc.metadata_controller	PVMetadataController	MetaData controller that provides end-point storage to metadata in a system.
Morello_Top.css.mem.dmc0.dmcMgr	*DummyAPB*	DummyAPB.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.mem.dmc0.dmcProf	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc0.dmcSensor	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc1	Infra_MemoryElement_DMC_Bing	Memory Element with DMC-Bing.
Morello_Top.css.mem.dmc1.dmc	DMC_Bing	Arm DMC-Bing Dynamic Memory Controller.
Morello_Top.css.mem.dmc1.dmc.metadata_controller	PVMetadataController	MetaData controller that provides end-point storage to metadata in a system.
Morello_Top.css.mem.dmc1.dmcMgr	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc1.dmcProf	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc1.dmcSensor	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc2	Infra_MemoryElement_DMC_Bing	Memory Element with DMC-Bing.
Morello_Top.css.mem.dmc2.dmc	DMC_Bing	Arm DMC-Bing Dynamic Memory Controller.
Morello_Top.css.mem.dmc2.dmc.metadata_controller	PVMetadataController	MetaData controller that provides end-point storage to metadata in a system.
Morello_Top.css.mem.dmc2.dmcMgr	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc2.dmcProf	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc2.dmcSensor	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc3	Infra_MemoryElement_DMC_Bing	Memory Element with DMC-Bing.
Morello_Top.css.mem.dmc3.dmc	DMC_Bing	Arm DMC-Bing Dynamic Memory Controller.
Morello_Top.css.mem.dmc3.dmc.metadata_controller	PVMetadataController	MetaData controller that provides end-point storage to metadata in a system.
Morello_Top.css.mem.dmc3.dmcMgr	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc3.dmcProf	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.dmc3.dmcSensor	*DummyAPB*	DummyAPB.
Morello_Top.css.mem.interruptOrGate0	*OrGate*	Or Gate.
Morello_Top.css.mem.interruptOrGate1	*OrGate*	Or Gate.
Morello_Top.css.mem.interruptOrGate2	*OrGate*	Or Gate.
Morello_Top.css.mem.interruptOrGate3	*OrGate*	Or Gate.
Morello_Top.css.mem.mem_chn_filter0	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mem_chn_filter1	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mem_chn_filter2	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mem_chn_filter3	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mgr_chn_filter0	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mgr_chn_filter1	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.mgr_chn_filter2	*TZFilterUnit*	TrustZone Filter Unit.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.mem.mgr_chn_filter3	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.prof_chn_filter0	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.prof_chn_filter1	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.prof_chn_filter2	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.prof_chn_filter3	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.sensor_chn_filter0	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.sensor_chn_filter1	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.sensor_chn_filter2	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.mem.sensor_chn_filter3	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.msi_rewriter_pcie	*MSIRewriter*	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
Morello_Top.css.msi_rewriter_smmu	*MSIRewriter*	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
Morello_Top.css.nic400	N1SDP_Morello_CSS_NIC400	N1SDP Morello CSS NIC-400 component.
Morello_Top.css.nic400.coresight_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.nic400.nic_buslogger	*PVBusLogger*	Bus Logger.
Morello_Top.css.nic400.reserved_Mem	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.nic400.secure_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.nic400.secure_scp_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.nic400_buslogger	*PVBusLogger*	Bus Logger.
Morello_Top.css.nonTrustedROM	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.css.nonTrustedROMloader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.css.nonTrustedSRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.pl011_sec_uart_ap	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.pl011_sec_uart_ap.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.pl011_uart1_ap	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.pl011_uart1_ap.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pl011_uart_ap	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.pl011_uart_ap.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.powerStateGate	Kits2_PowerStateGate	Power State Gate to filter the access to SYSTOP domain.
Morello_Top.css.pxlClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.pxlClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.pxlClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.pxlClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp	N1SDP_Morello_SCP	-
Morello_Top.css.scp.AP2SCP_NONSEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.scp.AP2SCP_SEC_RAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.scp.CS_Counter	*MemoryMappedCounterModule*	Memory Mapped Counter Module for Generic Timers.
Morello_Top.css.scp.DTCRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.scp.GenericTimerRef	*MemoryMappedGenericTimer*	Arm Generic Timer.
Morello_Top.css.scp.ITCRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.scp.ROM	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.css.scp.ROMloader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.css.scp.armcortexm7ct	ARM_Cortex-M7	Arm CORTEXM7 CT model.
Morello_Top.css.scp.c0_pik	Kits3_PIK_Cluster	Kits3 SCP Cluster Power Integration Kit for v8.2 cores.
Morello_Top.css.scp.c0_pik.ppu_cluster	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core0	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core1	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core2	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core3	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core4	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core5	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_pik.ppu_core6	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.scp.c0_pik.ppu_core7	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c0_tem	Temperature	Component to synthesis the temperature value of the connected core.
Morello_Top.css.scp.c1_pik	Kits3_PIK_Cluster	Kits3 SCP Cluster Power Integration Kit for v8.2 cores.
Morello_Top.css.scp.c1_pik.ppu_cluster	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core0	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core1	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core2	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core3	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core4	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core5	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core6	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_pik.ppu_core7	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.c1_tem	Temperature	Component to synthesis the temperature value of the connected core.
Morello_Top.css.scp.clock24MHz	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.clockWatcher	FrequencyProbe	Clock Frequency observer.
Morello_Top.css.scp.cluster_ppu_OrGate	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.cluster_ppu_OrGate0	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.cmsdk_watchdog	CMSDK_Watchdog	Arm Watchdog Module.
Morello_Top.css.scp.cpu_ppu_OrGate	WideOrGate_12x4	Or Gate with up to 48 inputs and support to num_cores.
Morello_Top.css.scp.debug_pik	PIK_Debug	Kits Debug Power Integration Kit.
Morello_Top.css.scp.debug_pik.ppu_debug_top	PowerPolicyUnit	Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.display_pik	Mobile4_PIK_Display	Mobile4 Display Power Integration Kit.
Morello_Top.css.scp.display_pik.ppu_dpu_top	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.exclusive_squasher	*PVBusExclusiveSquasher*	Squashes the exclusive attribute on bus transactions.
Morello_Top.css.scp.gen_timer_OrGate0	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.gen_timer_OrGate00	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.gpu_pik	Mobile4_PIK_GPU	Mobile4 GPU Power Integration Kit.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.scp.gpu_pik.ppu_gpu_top	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.pl011_uart_scp	*PL011_Uart*	Arm PrimeCell UART(PL011).
Morello_Top.css.scp.pl011_uart_scp.clk_divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.pll_lock_OrGate	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.pll_unlock_OrGate	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.proc_n_generic_timer_ref0	*MemoryMappedGenericTimer*	Arm Generic Timer.
Morello_Top.css.scp.refcounter	*MemoryMappedCounterModule*	Memory Mapped Counter Module for Generic Timers.
Morello_Top.css.scp.reserved_Mem	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.css.scp.scpClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.scp.scpClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.scp.scpClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scpClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scp_addr_tran	Kits2_AddrTran	Address Translator for Ashbrook Subsystem.
Morello_Top.css.scp.scp_mhu0	Juno_SCP_MHU	Juno Message Handling Unit.
Morello_Top.css.scp.scp_mhu1	Juno_SCP_MHU	Juno Message Handling Unit.
Morello_Top.css.scp.scp_mhu_CPU_INTR_H_OrGate	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.scp_mhu_CPU_INTR_H_OrGate0	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.scp_mhu_CPU_INTR_H_OrGate1	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.scp_mhu_CPU_INTR_S_OrGate	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.scp_mhu_CPU_INTR_S_OrGate0	WideOrGate	Or Gate with up to 8 inputs.
Morello_Top.css.scp.scp_pik	PIK_SCP_SGI_575	SGI_575 SCP Power Integration Kit.
Morello_Top.css.scp.scp_pik.ws1_timer	Kits2_Timer	Kits2 Timer.
Morello_Top.css.scp.scp_pik.ws1_timer.clk_div	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.scp.scp_pik.ws1_timer.counter	*CounterModule*	Internal component used by SP804 Timer module.
Morello_Top.css.scp.secure_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.scp.securitycontrolunit	Kits4_SecurityControlUnit	Security Control Unit in Kits4(Clark).

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.scp.system_pik	PIK_System_SGI_575	SGI-575 System Power Control.
Morello_Top.css.scp.system_pik.ppu_sys_logic	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.system_pik.ppu_sys_sram	*PPUv1*	Arm Power Policy Unit (PPU) architectural model.
Morello_Top.css.scp.terminal_uart_aon	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.scp_filter	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.css.smmu	*MMU_600*	SMMUv3 compliant device.
Morello_Top.css.tcuClkCtrl	SwitchedClockControl	Clock control allows input selection, rate control and gating.
Morello_Top.css.tcuClkCtrl.clkDiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkDiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.css.tcuClkCtrl.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect	ClockSelector	ClockSignal Selector.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.css.tcuClkCtrl.clkSelect.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.tcuClkCtrl.clkSelect.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.css.terminal_sec_uart_ap	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.terminal_uart1_ap	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.terminal_uart_ap	*TelnetTerminal*	Telnet terminal interface.
Morello_Top.css.trustedBootROM	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.css.trustedBootROMloader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.css.trustedSRAM	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.css.trusted_watchdog	*MemoryMappedGenericWatchdog*	Arm Generic Watchdog.
Morello_Top.pci	BasePlatformPCIAHCI	PCI addon for the Base Platform.
Morello_Top.pci.ahci	AHCI_PCI	-
Morello_Top.pci.ahci.ahci	*AHCI_SATA*	AHCI controller with attached SATA disks and PCIe interface.
Morello_Top.pci.ahci.buslogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice	PCIDevice	PCI Wrapper for memory mapped components.
Morello_Top.pci.ahci.pcidevice.dmalogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.incoming_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.lost_mastered_transactions	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.lost_transactions_to_pcie	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.msix_pba_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.msix_table_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.ahci.pcidevice.to_client_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.dma330x4	DMA330x4	-
Morello_Top.pci.dma330x4.dmac0	*PL330_DMAC*	Arm PrimeCell DMA Controller(PL330).

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.pci.dma330x4.dmac0.timer	*ClockTimerThread*	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac0.timer.timer	*ClockTimerThread64*	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac0.timer.timer.thread	*SchedulerThread*	A SchedulerThread instance represents a co-routine thread in the simulation.
Morello_Top.pci.dma330x4.dmac0.timer.timer.thread_event	*SchedulerThreadEvent*	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
Morello_Top.pci.dma330x4.dmac1	*PL330_DMAC*	Arm PrimeCell DMA Controller(PL330).
Morello_Top.pci.dma330x4.dmac1.timer	*ClockTimerThread*	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac1.timer.timer	*ClockTimerThread64*	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac1.timer.timer.thread	*SchedulerThread*	A SchedulerThread instance represents a co-routine thread in the simulation.
Morello_Top.pci.dma330x4.dmac1.timer.timer.thread_event	*SchedulerThreadEvent*	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.pci.dma330x4.dmac2	*PL330_DMAC*	Arm PrimeCell DMA Controller(PL330).
Morello_Top.pci.dma330x4.dmac2.timer	*ClockTimerThread*	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac2.timer.timer	*ClockTimerThread64*	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac2.timer.timer.thread	*SchedulerThread*	A SchedulerThread instance represents a co-routine thread in the simulation.
Morello_Top.pci.dma330x4.dmac2.timer.timer.thread_event	*SchedulerThreadEvent*	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
Morello_Top.pci.dma330x4.dmac3	*PL330_DMAC*	Arm PrimeCell DMA Controller(PL330).
Morello_Top.pci.dma330x4.dmac3.timer	*ClockTimerThread*	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac3.timer.timer	*ClockTimerThread64*	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
Morello_Top.pci.dma330x4.dmac3.timer.timer.thread	*SchedulerThread*	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.pci.dma330x4.dmac3.timer.timer.thread_event	*SchedulerThreadEvent*	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
Morello_Top.pci.pci_smmuv3	SMMUv3_FOR_PCIE	System MMUv3 configured for PCI-E Sub-system.
Morello_Top.pci.pci_smmuv3.mmu	*SMMUv3AEM*	SMMUv3 AEM.
Morello_Top.pci.pci_smmuv3_msirewriter	*MSIRewriter*	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
Morello_Top.pci.pcidevice0	PCIDevice	PCI Wrapper for memory mapped components.
Morello_Top.pci.pcidevice0.dmalogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.incoming_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.lost_mastered_transactions	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.lost_transactions_to_pcie	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.msix_pba_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.msix_table_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice0.to_client_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1	PCIDevice	PCI Wrapper for memory mapped components.
Morello_Top.pci.pcidevice1.dmalogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.incoming_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.lost_mastered_transactions	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.lost_transactions_to_pcie	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.msix_pba_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.msix_table_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcidevice1.to_client_memory_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pcivirtioblockdevice0	*VirtioPCIBlockDevice*	virtio PCI block device.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.pci.pcivirtioblockdevice1	*VirtioPCIBlockDevice*	virtio PCI block device.
Morello_Top.pci.pvbus2pci	PVBus2PCI	PVBus to PCI Bridge.
Morello_Top.pci.pvbus2pci.cfglogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pvbus2pci.devicelogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.pvbus2pci.dmalogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.smmulogger	*PVBusLogger*	Bus Logger.
Morello_Top.pci.tbu0_pre_smmu_logger	*PVBusLogger*	Bus Logger.
Morello_Top.pci_logger0	*PVBusLogger*	Bus Logger.
Morello_Top.soc	N1SDP_Morello_SoC	Morello SoC model.
Morello_Top.soc.CLUSPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.CLUSPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.CPU0PLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.CPU0PLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.CPU1PLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.CPU1PLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.DMCPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.DMCPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.DPUPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.soc.DPUPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.GPUPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.GPUPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.INTPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.INTPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.PXLPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.
Morello_Top.soc.PXLPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKClk	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect	ClusterClockControl	Cluster clock control allows input selection, rate control and gating.
Morello_Top.soc.SYSAPBCLKSelect.clkGate	ClockGate	Clock gate for dis/enabling the clock.
Morello_Top.soc.SYSAPBCLKSelect.clkGate.divider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector	ClockSelector	ClockSignal Selector.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv0	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv1	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv10	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv2	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv3	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv4	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv5	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv6	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv7	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv8	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdiv9	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.clkSelector.clkdivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.refClkDiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.sysClkDiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSAPBCLKSelect.xClkDiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.SYSPLL	Infra1_PLLControl	Simulate PLL clock frequency control logic.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.soc.SYSPLL.clkdiv	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.soc.buslogger	*PVBusLogger*	Bus Logger.
Morello_Top.soc.dummyAPB	*DummyAPB*	DummyAPB.
Morello_Top.soc.mcp_i2c_0	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.soc.mcp_i2c_1	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.soc.mcp_qspi	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.soc.mcp_qspi_loader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.soc.mscp_soc_reserved	*WarningMemory*	Memory that prints warnings, and RAZ/WIs or aborts.
Morello_Top.soc.pci_phy	*DummyAPB*	DummyAPB.
Morello_Top.soc.pcie_macro	*DummyAPB*	DummyAPB.
Morello_Top.soc.pcie_rootport	*DummyAPB*	DummyAPB.
Morello_Top.soc.scc	Morello_SoC_SCC	Morello SoC System Configuration Controller.
Morello_Top.soc.scp_i2c_0	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.soc.scp_i2c_1	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.soc.scp_i2c_2	*RAMDevice*	RAM device, can be dynamic or static ram.
Morello_Top.soc.scp_qspi	*IntelStrataFlashJ3*	Intel Strata Flash J3 LISA+ model.
Morello_Top.soc.scp_qspi_loader	*FlashLoader*	A device that can preload a gzipped image into flash at startup.
Morello_Top.soc.sensors	*DummyAPB*	DummyAPB.
Morello_Top.soc.soc_gpio	*PL061_GPIO*	Arm PrimeCell General Purpose Input/Output(PL061).
Morello_Top.soc.sys_nic	*TZFilterUnit*	TrustZone Filter Unit.
Morello_Top.vis_dashboard	Visualisation_sdl2	Display window for VE using sdl2 Visualisation library.
Morello_Top.vis_dashboard.recorder	*VisEventRecorder*	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
Morello_Top.vis_dashboard.recorder.playbackDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_dashboard.recorder.recordingDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-8 FVP_Morello instances (continued)

Name	Type	Description
Morello_Top.vis_dp0	Visualisation_sdl2	Display window for VE using sdl2 Visualisation library.
Morello_Top.vis_dp0.recorder	*VisEventRecorder*	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
Morello_Top.vis_dp0.recorder.playbackDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_dp0.recorder.recordingDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_dp1	Visualisation_sdl2	Display window for VE using sdl2 Visualisation library.
Morello_Top.vis_dp1.recorder	*VisEventRecorder*	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
Morello_Top.vis_dp1.recorder.playbackDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_dp1.recorder.recordingDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_hdlcd	Visualisation_sdl2	Display window for VE using sdl2 Visualisation library.
Morello_Top.vis_hdlcd.recorder	*VisEventRecorder*	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
Morello_Top.vis_hdlcd.recorder.playbackDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
Morello_Top.vis_hdlcd.recorder.recordingDivider	*ClockDivider*	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.