ARM Embedded Trace Macrocell CoreSight™ ETM™ –M7(TM975)

Product Revision r0

Software Developers Errata Notice

Non-Confidential - Released

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- the document title
- the document number, ARM-EPM-064410
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Release Information

Errata are listed in this section if they are new to the document, or marked as “updated” if there has been any change to the erratum text in Chapter 2. Fixed errata are not shown as updated unless the erratum text has changed. The summary table in section 2.2 identifies errata that have been fixed in each product revision.

04 Dec 2014: Changes in Document v3

Page	Status	ID	Cat	Rare	Summary of Erratum
7	New	832869	CatB		NDSM not inserted during periodic synchronization
9	Updated	830976	CatC		ATB Flush acknowledged too early
12	New	833819	CatC		Exception entry directly followed by Multiple wrongly traced
13	New	835371	CatC		Exception level change not traced for exception
14	New	836619	CatC		Data events lost in overflow
15	New	836624	CatC		Preferred exception return address traced incorrectly on System Error exceptions

Contents

Chapter 1.
Introduction

This chapter introduces the errata notice for the ARM CoreSight ETM-M7 Embedded Trace Macrocell.

1.1. Scope of this document

This document describes errata categorized by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

This document describes errata that may impact anyone who is developing software that will run on implementations of this ARM product.

1.2. Categorization of errata

Errata recorded in this document are split into the following levels of severity:

Table 1 Categorization of errata

Errata Type	Definition
Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A(Rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B(Rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Chapter 2.
Errata Descriptions

2.1. Product Revision Status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

2.2. Revisions Affected

Table 2 below lists the product revisions affected by each erratum. A cell marked with **X** indicates that the erratum affects the revision shown at the top of that column.

This document includes errata that affect revision r0 only.

Refer to the reference material supplied with your product to identify the revision of the IP.

Table 2 Revisions Affected

ID	Cat	Rare	Summary of Erratum	r0p0	r0p1
832869	CatB		NDSM not inserted during periodic synchronization	X	
836624	CatC		Preferred exception return address traced incorrectly on System Error exceptions	X	
836619	CatC		Data events lost in overflow	X	
835371	CatC		Exception level change not traced for exception	X	
833819	CatC		Exception entry directly followed by Multiple wrongly traced	X	
830977	CatC		Single Shot comparator behaves incorrectly for data address and value matches near store exclusive operations	X	
830976	CatC		ATB Flush acknowledged too early	X	
829621	CatC		Data Address comparison mismatch	X	

2.3. Category A

There are no errata in this category

2.4. Category A (Rare)

There are no errata in this category

2.5. Category B

832869: NDSM not inserted during periodic synchronization

Category B
Products Affected: ETM-M7.
Present in: r0p0

Description

NDSM packets are not inserted in either the instruction or data trace streams when periodic synchronization is requested.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions

A periodic synchronization request occurs and data tracing is enabled.

Implications

If the trace is captured in a circular buffer and trace has been discarded since the ETM was enabled, or since the most recent trace overflow, then the trace analyzer will not be able to associate the data trace stream with the instruction trace stream.

This does not affect the analysis of the instruction stream and there is no corruption of the trace streams.

Workaround

There is no software workaround.

2.6. Category B (Rare)

There are no errata in this category

2.7. Category C

829621: Data Address comparison mismatch

Category C
Products Affected: ETM-M7.
Present in: r0p0

Description

This erratum might occur if the ETM is programmed to perform data value comparisons. The erratum happens when the programmed and accessed data addresses as well as the programmed and accessed data values match, but the accessed address is not aligned appropriately for the data value size that the data value comparator is programmed with. The comparator will incorrectly fire.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions

All of the following must occur:

1) TRCACATR programming
   - ETM programmed to perform data value comparison: TRCACATR.DATAMATCH == 2'b01 or 2'b11
   - The data value comparator is programmed with a halfword or word data value: TRCACATR.DATASIZE == 2'b01 or 2'b10
   - Comparator programmed to perform data comparison: TRCACATR.TYPE == 2'b01 or 2'b10 or 2'b11
   - The accessed address is executed at an exception level that the comparator is configured to match against according to TRCACATR.EXLEVEL_S.
   - If the trace unit uses the single address comparator for data value comparison (TRCACATR.DATARANGE == 1'b0), the data transfer size is bigger or equal to the programmed data value size OR If the trace unit uses the address range comparator for data value comparison (TRCACATR.DATARANGE == 1'b1), the data transfer size is equal to the programmed data value size.
2) The alignment of the accessed data value:
   - If TRCACATR.DATASIZE == 2'b01 (halfword) and the incoming data address is byte-aligned.
   - If TRCACATR.DATASIZE == 2'b10 (word) and the incoming data address is halfword-aligned or byte-aligned.
3) If the accessed address region [accessed_address + access_size; accessed_address] overlaps with the programmed address of the single-address comparator if (TRCACATR.DATARANGE == 1'b0) or with the programmed address range of the address range comparator if (TRCACATR.DATARANGE == 1'b1)
4) The programmed and accessed data values are identical.

Implications

The data address comparator might match incorrectly. This match can propagate and make the single-shot comparator controls fire. Depending on the resource selectors and event selectors programming, it can also decrement the counters or change the state of the sequencer or request a timestamp to be inserted in the trace stream or trace extra instructions or data (through ViewInst/ViewData events) or output extra external events.

However, the trace stream is not corrupted.

Workaround

There is no software workaround.

830976: ATB Flush acknowledged too early

Category C
Products Affected: ETM-M7.
Present in: r0p0

Description

This erratum might occur if the ETM is flushing because of an ATB instruction or data interface FIFO flush request. The flush might be acknowledged by AFREADY while all the data have not been flushed yet.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions 1

There is an ATB data flush request and a trace trigger is sent on the ATB data bus one clock cycle before the last 64 bits of data.

Conditions 2

The following sequence must happen:

1) The ETM becomes disabled.
2) An ATB data flush request occurs before the ETM data FIFO has finished draining.
3) The ETM is re-enabled.
4) An internal flush is initiated due to one of the following:
   - The Cortex-M7 enters Debug state.
   - The ETM initiates entry to low power state.
5) An ATB data flush request occurs before the internal flush is completed and any data trace is generated between the internal flush and ATB data flush.

Conditions 3

The following sequence must happen:

1) The ETM becomes disabled.
2) An ATB instruction flush request occurs before the ETM instruction FIFO has finished draining.
3) The ETM is re-enabled.
4) An internal flush is initiated due to one of the following:
   - The Cortex-M7 enters Debug state.
   - The ETM initiates entry to low power state.
5) An ATB instruction flush request occurs before the internal flush is completed and any instruction trace is generated between the internal flush and ATB instruction flush.

Conditions 4

The following sequence must happen:

1) The I-side is already flushing because of an ATB instruction flush request
2) The Cortex-M7 enters Debug state initiating a flush of both instruction and data pipes.
3) There is an ATB data flush request while the ATB instruction flush is still ongoing then this ATB data flush will be acknowledged too early if anything was traced in the data side between the Debug state entry flush request and the ATB data flush request.

Conditions 5

The following sequence must happen:

1) The ETM initiates an internal flush before entering low power state.
2) An ATB instruction flush request occurs before the ETM instruction FIFO has finished draining.
3) The ETM leaves low power state.
4) An internal flush is initiated because of one of the following:
   - The Cortex-M7 enters Debug state.
   - The ETM initiates entry to low power state.
5) An ATB instruction flush request occurs before the internal flush is completed and any instruction trace is generated between the internal flush request and the ATB instruction flush.

The ATB instruction flush might be acknowledged early.

Conditions 6

The following sequence must happen:

1) An ATB instruction flush request occurs.
2) The Cortex-M7 enters Debug state, initiating an internal flush request, before the ATB instruction flush request is acknowledged.
3) An ATB data flush request occurs before the internal flush is completed.

The ATB data flush might be acknowledged early.

Implications

The ATB instruction or data flush is acknowledged too early. If a trace capture device stops capturing data on receipt of the flush acknowledgement, this erratum means that some data might not be captured.

Workaround

There is no software workaround.

830977: Single Shot comparator behaves incorrectly for data address and value matches near store exclusive operations

Category C

Products Affected: ETM-M7.

Present in: r0p0

Description

This erratum might occur if the ETM is programmed to perform data address and/or value comparisons and if the results of the comparisons are used by the single-shot comparator controls.

The single-shot comparator control might fire incorrectly or not fire at all for data address or value matches near store exclusive operations.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions

Registers TRCSSCCR0 or TRCSSPCICR0 must be programmed so that the single-shot selects comparators (ETM comparators or processor comparators) matching on data address or data value.

When selecting ETM comparators, TRCACATRn (0<=n<=7) registers must be programmed to fire on data address (TRCACATRn.TYPE = 2'b01 or 2'b10 or 2'b11).

The erratum occurs when either of the following happens:

- The comparator matches on the data address or data value associated with a store exclusive transfer and there are no empty cycles between the store exclusive and the following instruction, then the single-shot will fire even if the store exclusive transfer failed.
- The comparator matches on the data transfer associated with one of the two instructions directly following a store exclusive instruction and there are no empty cycles in between the store exclusive and the following instructions then the single-shot might not fire.

Implications

The single-shot comparator control will fire incorrectly for a data address or data value match on a failing store exclusive transfer or will not fire for a data address match on an instruction directly following a store exclusive transfer.

Workaround

There is no software workaround.

833819: Exception entry directly followed by Multiple wrongly traced

Category C
Products Affected: ETM-M7.
Present in: r0p0

Description

This erratum might occur when an exception entry is immediately followed by a load/store multiple instruction. In some scenarios, the data transfers for the load/store multiple instruction might be associated with the exception entry.

If the first traced data transfer of the multiple has an index equal to the (last traced index of the previous stack push) + 1 then the data transfer of the multiple might be associated with the stack push operation.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions

The following conditions must occur:

- Data tracing is enabled.
- An exception occurs, where one or more data transfers are traced from the stack push operation.
- A load/store multiple instruction is the first instruction at the exception handler, and one or more data transfers are traced.
- The first data transfer of the load/store multiple is not traced, because either it has been filtered out using the the ViewData function or it has been suppressed because of data suppression.
- The first traced data transfer of the load/store multiple instruction has an index value which is exactly one more than the final traced data transfer of the exception entry stack push operation.

Implications

The data transfers associated with the load/store multiple are incorrectly associated with the exception entry stack push instead of the load/store multiple instruction.

The data addresses and data values traced are not affected.

This erratum is contained to only the first instruction at the exception handler and future instructions are not affected.

Workaround

There is no software workaround.

835371: Exception level change not traced for exception

Category C
Products Affected: ETM-M7.
Present in: r0p0

Description

This erratum occurs if an exception is taken at the target of an exception return from Handler to Thread mode. The Exception Level is traced incorrectly by the ETM.

Configurations affected

This erratum affects both the instruction only and the instruction and data configurations of the ETM.

Conditions

1) An exception return occurs, returning from Handler to Thread mode.
2) No instructions are executed at the exception return target in Thread mode.
3) An exception entry occurs, returning to Handler mode.

Implications

The Exception Level in the trace, which indicates Thread or Handler mode, is incorrectly traced as Handler for both:

- The target address of the exception return.
- The preferred return address of the new exception.

Workaround

There is no software workaround.

836619: Data events lost in overflow

Category C
Products Affected: ETM-M7.
Present in: r0p0

Description

This erratum occurs if the instruction trace FIFO overflows, and no P1, P2 or Event elements have been traced in the data trace stream. Data Event elements occurring while the instruction trace FIFO is recovering from overflow might be lost.

Configurations affected

This erratum only affects the instruction and data configuration of the ETM.

Conditions

- No P1, P2 or Event elements have been generated in the data trace stream.
- The instruction trace FIFO overflows, which forces the data trace stream to overflow.
- A data Event element occurs without any P1 or P2 data trace being generated.

While recovering from the overflow, the data trace stream will not include an Overflow element or Event elements.

Implications

Data Event elements occurring while the I-side overflows might be lost.

Workaround

There is no software workaround.

836624: Preferred exception return address traced incorrectly on System Error exceptions

Category C

Products Affected: ETM-M7.

Present in: r0p0

Description

This erratum might occur if the ETM enters in a restricted region, and the exception that occurs on entry to the restricted region is traced. If the ETM is disabled then re-enabled, and a System Error exception is traced immediately after the ETM is re-enabled, then the preferred return address of the System Error exception might be traced incorrectly.

Configurations affected

This erratum affects both the instruction only and the instruction and data configurations of the ETM.

Conditions

1) The ETM enters a restricted region and traces the exception associated with the entry to the restricted region.
2) The ETM is disabled.
3) System errors are programmed to be traced:
   - TRCVICTLR.TRCERR == 1'b1.
4) The ETM is enabled.
5) A System Error exception occurs as the first execution after the ETM is enabled.

Implications

The ETM will trace an incorrect preferred return address with the System Error exception. The address traced is the preferred return address of the exception on entry to the restricted region. If a debug tool uses the preferred exception return address to infer the cause of the System Error exception, this cause might be incorrectly inferred.

Workaround

There is no software workaround.