Arm® CoreLink™ CMN-600 Coherent Mesh Network

Revision: r3p0

Technical Reference Manual

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Arm® CoreLink™ CMN-600 Coherent Mesh Network

Technical Reference Manual

Release Information

Document History

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Arm Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

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The information in this document is Final, that is for a developed product.

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Appendix C Revisions

Preface

This preface introduces the *Arm® CoreLink™ CMN-600 Coherent Mesh Network Technical Reference Manual*.

It contains the following:

About this book

This book is for the Arm® CoreLink™ CMN-600 Coherent Mesh Network product.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses Coherent Mesh Network CMN-600.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter describes the CMN-600 product.

Chapter 2 Functional Description
This chapter describes the functionality of the CMN-600 product.

Chapter 3 Programmers Model
This chapter describes the programmers model.

Chapter 4 SLC Memory System
This chapter describes the SLC memory system.

Chapter 5 Debug trace and PMU
This chapter describes the *Debug Trace* (DT) and *Performance Monitoring Unit* (PMU) features.

Chapter 6 Performance Optimization and Monitoring
This chapter describes performance optimization techniques for use by system integrators, and the *Performance Monitoring Unit* (PMU).

Appendix A Signal Descriptions
This section describes the CMN-600 I/O signals.

Appendix B CXS Specification
This appendix describes the Coherent Multichip Link product.

Appendix C Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
: Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
: Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`
: Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
: Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
: Denotes language keywords when used outside example code.

`<and>`
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

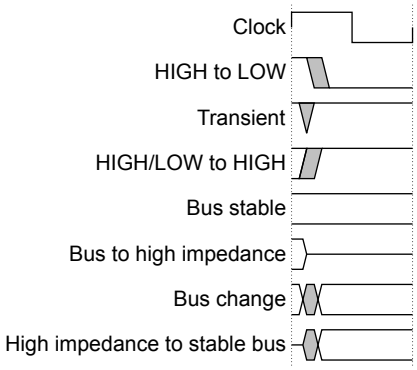

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Arm® AMBA® AXI and ACE Protocol Specification* (ARM IHI 0022).
- *Arm®AMBA® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *Arm®AMBA® 4 AXI4-Stream Protocol* (ARM IHI 0051A).
- *Arm®AMBA® 5 CHI ArchitectureSpecification* (ARM IHI 0050).
- *Arm® Architecture Reference Manual ARMv7-A and ARMv7-R Edition* (ARM DDI 0406).
- *Arm® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile* (ARM DDI 0487).
- *Arm® Architecture Specification for ARMv8.4 architecture profile* (ARM ECM 0126602).

The following confidential books are only available to licensees:

- *Arm® CoreLink™ CMN-600 Coherent Mesh Network Configuration and Integration Manual*(ARM 100613).
- *Arm® CoreLink™ CMN-600 User Guide* (ARM 101402).

Other publications

- *JEDEC Standard Manufacturer's Identification Code*, JEP106, *http://www.jedec.org*.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm CoreLink CMN-600 Coherent Mesh Network Technical Reference Manual*.
- The number 100180_0300_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

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Chapter 1
Introduction

This chapter describes the CMN-600 product.

It contains the following sections:

1.1 About CMN-600

The CMN-600 product is a scalable configurable coherent interconnect that is designed to meet the *Power, Performance, and Area* (PPA) requirements for coherent mesh network systems that are used in high-end networking and enterprise compute applications.

The CMN-600 product provides the following key features:

- Scalable mesh interconnect:
  - From one to 32 processor compute clusters.
- Configurable with Socrates™ IP Tooling platform which is an environment for the configuration and integration of Arm and other IP-XACT enabled IP:
  - Custom interconnect size and device placement.
  - Optional *System Level Cache* (SLC).
- CMN-600 R2 supports AMBA 5 CHI Issue C, including the following new features:
  - Separate Read Data and Comp Responses for DMT.
  - Combined CompAck with WriteData.
- Supports AMBA 5 CHI Issue B, including the following features:
  - Far atomic operations.
  - Cache-stashing to improve data locality.
  - Direct data transfer to reduce latency.
- System alignment:
  - *Quality of Service* (QoS).
  - *Reliability, Availability, and Serviceability* (RAS).
  - *Debug and Trace* (DT).
- IP compatibility:
  - *Dynamic Memory Controller* (DMC).
  - *Generic Interrupt Controller* (GIC).
  - *Memory Management Unit* (MMU).
  - CMN-600 is compatible with Armv8.0 and Armv8.2-A processors.
- Optional *Coherent Multichip Link* (CML) feature:
  - Supports up to four SoCs in a coherent system.
  - Compliant with CCIX standard.

A system that is built using the CMN-600 product can contain the following protocol nodes/devices:

RN-F (*Fully coherent Requesting Node*)
A fully coherent master device that supports either CHI Issue A, CHI Issue B, or CHI Issue C protocols. One CMN-600 instance supports:

- All CHI.A RN-Fs, or
- All CHI.B RN-Fs, or
- All CHI.C RN-Fs (CMN-600 R2)

Note

All RN-Fs need to be of same type; they can not be mixed and matched.

RN-I (*I/O coherent Requesting Node*) bridge
An I/O-coherent master device. This is a CHI bridge device acting as an RN-I proxy for one or more AXI/ACE-Lite master devices that are connected to it.

RN-D (*I/O coherent Requesting Node with DVM support*) bridge
An I/O coherent master device that supports accepting DVM messages on the snoop channel.

HN-F (*Fully coherent Home Node*)

A device that acts as a home node for a coherent region of memory, accepting coherent requests from RN-Fs and RN-Is, and generating snoops to all applicable RN-Fs in the system as required to support the coherency protocol.

HN-I (*I/O Home Node*)

A device that acts as a home-node for the slave I/O subsystem, responsible for ensuring proper ordering of requests targeting the slave I/O subsystem. HN-I supports AMBA AXI or ACE-Lite.

HN-D (*HN-I + DVM Node*)

A device that includes HN-I, *DVM Node* (DN), *Configuration Node* (CFG), Global Configuration Slave, and the *Power/Clock Control Block* (PCCB).

——— **Note** ———

Only one HN-D is allowed per CMN-600 instance.

———————————

SN-F (*CHI Slave Node*)

A device which solely is a recipient of CHI commands, limited to fulfilling simple read, write, and CMO requests targeting normal memory.

SBSX bridge

A CHI bridge device that converts simple CHI read, write, and CMO commands to an ACE-Lite slave memory device.

CXG bridge

A CXG device bridges between CHI and CXS (CCIX port) and contains:

1. *CCIX Request Agent* (**CXRA**) proxy and *CCIX Home Agent* (**CXHA**) proxy functionality.
2. *CXS Link Agent* (**CXLA**) functionality which is external to the CMN-600 hierarchy.

1.2 Compliance

The CMN-600 product is based on the AMBA 5 CHI Issue B architecture specification.

——— **Note** ———

CMN-600 R2 supports AMBA 5CHI Issue C architecture specification.

———————————

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

AMBA 5 CHI architecture

The CMN-600 product implements the following architecture capabilities:

- Fully compliant with CHI interconnect architecture.
- Non-blocking coherence protocol.
- Packet-based communication.
- The following four types of channels:
  - *Request* (REQ).
  - *Response* (RSP).
  - *Snoop* (SNP).
  - *Data* (DAT).
- Credited end-to-end protocol-layer flow-control with a retry-once mechanism for flexible bandwidth and resource allocation.
- Integrated end-to-end *Quality-of-Service* (QoS) capabilities.

See the *Arm® AMBA® 5 CHI Architecture Specification* for more information.

CCIX architecture

The CML CCIX implementation is compliant with CCIX PRL Rev1.0 ver 0.9 dated October 20, 2017.

1.3 Features

The CMN-600 product provides the following key features:

- Highly scalable mesh network topology configurable up to an 8 × 8 mesh.
- Custom mesh size and device placement.
- Supports a programmable *System Address Map* (SAM).
- Supports up to 32 RN-F interfaces for CHI-based compute clusters, accelerators, graphic processing units, or other cache coherent masters.
  - For CMN-600 R2, supports up to 64 RN-F interfaces with CAL.
- Supports up to eight memory controllers (on-chip memory or DDR).
  - For CMN-600 R2, supports up to 16 memory controllers.
- Supports up to 32 RN-Is with up to three ACE5-Lite ports each (96 total):

  Note

  Additional devices are supported by using more levels of interconnect hierarchy, such as the CoreLink NIC-450 Network Interconnect.

- Data channel: a pair of 256-bit data channels, one for each direction.
- DVM message transport between masters.
- QoS regulation for shaping traffic profiles.
- A *Performance Monitoring Unit* (PMU) to count performance-related events.
- High-performance distributed SLC and SF up to 32 HN-Fs with cache sizes of 0-128MB total:
  - For CMN-600 R2, supports up to 64 HN-Fs with CAL with cache sizes of 0-256MB total.
  - The HN-F includes an integrated *Point-of-Serialization* (PoS) and *Point-of-Coherency* (PoC) and its SLC (also referred to as Agile System Cache) can be used both for compute and I/O caching.
  - *Snoop Filter* (SF) up to 256MB of tag RAM for increased coherency scalability consisting of up to 32 partitions (one per HN-F). For CMN-600 R2, supports up to 64 partitions.
- Up to eight HN-Is, each with an ACE-Lite master port.
- Supports *Device Credited Slices* (DCSs) used for register slices at device interfaces, allowing flexibility in device placement.
- Supports *Mesh Credited Slices* (MCSs) used for X-Y register slices, allowing flexibility in mesh floorplanning.
- Support for *Component Aggregation Layer* (CAL) for device interface port expansion.
- For CMN-600 R2, support for *CAL Credited Slices* (CCSs), allowing flexibility in mesh floorplanning in configurations that use the CAL.
- *On-Chip Memory* (OCM) allows for the creation of CMN-600 systems without physical DDR memory.
- RAS features including transport parity, optional data path parity, SECDED ECC, and data poisoning signaling.
- Supports up to two CCIX ports, supporting one, two, or three CCIX links for chip-to-chip coherent communication. Each CCIX port has a CXS interface that transports CCIX TLP.
  - For CMN-600 R2, supports up to four CCIX ports.

This section contains the following subsections:

1.3.1 R2 Features

CMN-600 R2 provides the following major changes:

- Support for *Address Based Flush* (ABF). Refer to *4.9 CMN-600 Hardware-based cache flush engine* on page 4-1089 for more information.
- Support for way-based SLC partitioning. Refer to *4.15 Way-based SLC cache partitioning* on page 4-1097 for more information.
- Support for sourced-based way locking. Refer to *4.14 Source-based SLC cache partitioning* on page 4-1096 for more information.
- *System Address Mapping* (SAM) enhancements.
- CAL and CCS support.
- AXI4 Stream support.

1.3.2 R3 Features

CMN-600 R3 provides the following major changes.:

- Support for CCIX Slave Agent support in CML mode.
- Support for 256 RNI read tracker entries.
- Added support for Atomics in RN-I.
- Increased support for hashed & non-hashed regions in SAM.

1.3.3 CML Properties, Support, and Requirements

This section provides CCIX, CXS, and CHI information for CML support.

CXS Support

Refer to the tables found in *1.3.4 CCIX and CXS property support* on page 1-19 for details.

CCIX Support

Refer to this section and the tables found in *1.3.4 CCIX and CXS property support* on page 1-19 for details.

CHI Support

The following table contains CHI support for CML settings.

Table 1-1 CHI support for CML

CHI Feature	CML Support		Comments
	Local	Remote	
Coherency	Yes	Yes	-
Ordering	Yes	Yes	-
Atomics	Yes	Yes	-
Exclusive Accesses	Yes	SMP Mode Only	Remote Support: Only RN-F exclusives are supported and can only target HN-F. In non-SMP mode, any read exclusive access is downgraded to a non-exclusive read and write exclusive is terminated at CXRA and “Non-Data Error” response is sent.
Cache Stashing	Yes	No	-
DVM Operations	Yes	SMP Mode Only	-
Error Handling			-
-Response Error	Yes	Yes	-
-Data Check	Yes	No	-
-Poison	Yes	Yes	Mandatory for CMN-600.
QoS			-
- Request	Yes	Yes	-
- Snoop	Yes	No	-
Data Return from Shared Clean	Yes	No	-

Table 1-1 CHI support for CML (continued)

CHI Feature	CML Support		Comments
	Local	Remote	
Direct Cache Transfer (DCT)	Yes	No	Local support includes local RN-F sending data directly to CCIX gateway block.
Direct Memory Transfer (DMT)	Yes	No	Local support includes local SN-F sending data directly to CCIX gateway block.
I/O Deallocation Transactions	Yes	Yes	-
CleanSharedPersist CMO	Yes	Yes	-
Prefetch Target	Yes	No	Remote Support: This request is supposed to target SN and hence is not expected at CXRA.
Trace Tag	Yes	SMP Mode Only	-
System Coherency Interface (SYSCOREQ/ACK)	Yes	Yes (using s/w bits)	-
Partial Cache State	Yes	No	CXRA, inside CML block, does not accept the following requests and responses: WriteBackPtl, WriteCleanPtl (only in CHI-A), SnpRespDataPtl*
Streaming and Optimized Streaming of Ordered WriteUniques	Yes	No	WriteUnique* request with “Request Order” and “ExpCompAck” attributes set, RN must send the “CompAck” as soon as it receives a “Comp” response for that write request and must not create any dependencies on other outstanding writes.
CHI-A RN-F	No	No	Remote Support: CXRA relies on CHI snoop's "DoNotGoToSD" field to map CCIX snoop request SnpToSC and hence does not support CHI-A RN-Fs. Because of this, CHI-A RN-F will also not be supported for local traffic.

CML Requirement

Each CML Port requires a minimum of one request and one data credit more than the total number of “reservations” enabled using CXRA’s configuration control register (**por_cxg_ra_cfg_ctl**).

This requirement applies to each enabled CCIX link at a given CCIX Port. For example, in the SMP mode, since by default all the reservations are enabled, a minimum four request and four data credits are required to be granted per CCIX link. These credits are used by certain traffic types, such as QoS-15, to make forward progress in a loaded system. See configuration register **por_cxg_ra_cfg_ctl** for more details.

1.3.4 CCIX and CXS property support

This section provides CCIX and CXS information for CML support.

The following table contains CXS property settings.

Table 1-2 CXS property support

CXS property	Support
TX/RX CXSDATAFLITWIDTH	256
TX/RX CXSMAXPKTPERFLIT	2
TX CXSCONTINUOUSDATA	True
RX CXSCONTINUOUSDATA	False

Table 1-2 CXS property support (continued)

CXS property	Support
TX/RX CXSERRORFULLPKT	True
TX/RX CXSDATACHECK	None
TX/RX CXSREPLICATION	None

CCIX features not supported

- Memory expansion. HN-Fs and their associated SN-Fs must be on the same chip.
- Snoop chaining outbound.
- CCIX snoop multicast (inbound and outbound).
- Snoop broadcast outbound.

The following table contains CCIX property settings for CML.

Table 1-3 CCIX property settings for CML

Property	Permitted values	Support
NoCompAck	True, False	False
PartialCacheStates	True, False	False
CacheLineSize	64B, 128B	64B
AddrWidth	48b, 52b, 56b, 60b, 64b	48b
PktHeader	Compatible, Optimized	Both
MaxPacketSize	128B, 256B, 512B	All
NoMessagePack	True, False	Both (True is the Default)

1.4 Interfaces

The following figure shows the interfaces of the CMN-600 product.

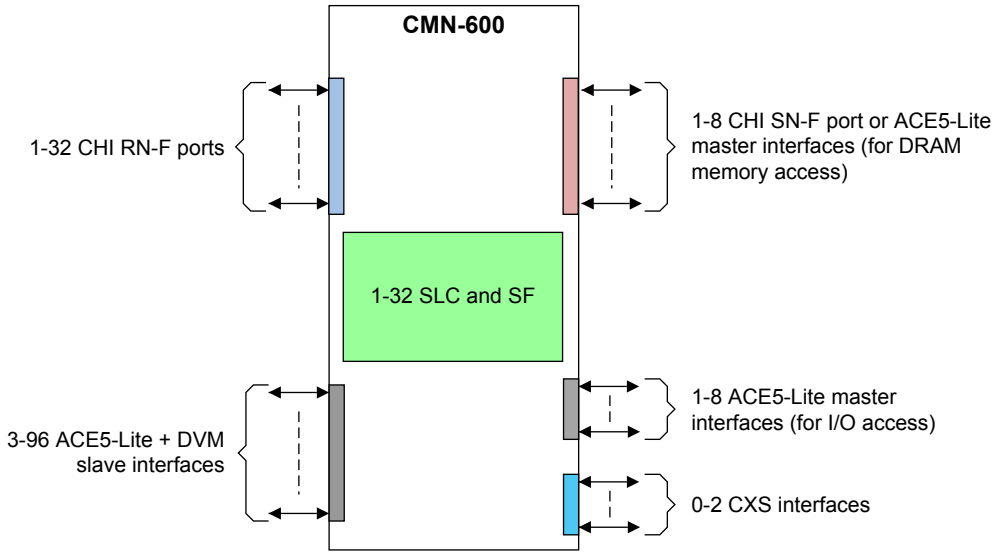


Figure 1-1 CMN-600 interfaces

For CMN-600 R2, the following items are supported:

- 1-64 CHI RN-F ports
- 1-16 CHI SN-F ports
- 0-4 CXS interfaces
- 1-64 SLC and SF

1.5 Configurable options

The basic structure of CMN-600 is a configurable rectangular grid comprised of network routers referred to as *Crosspoints* (XPs) and CHI-compliant devices. Each XP connects horizontally and vertically to other XPs, creating a two-dimensional mesh structure. Each XP has up to two ports to which CHI-compliant devices can be connected.

CMN-600 provides several configurable parameters that can be configured to meet various system requirements. Use Socrates IP Tooling to initially auto-populate the device(s) throughout the mesh. Then refine the mesh design and/or device placement keeping in mind these guidelines:

CMN-600 is configured in three steps:

1. System component selection. In this step, system components are determined, including:
   - The number and type of processors.
   - I/O interfaces.
   - Number of HN-Fs.
   - Amount of SLC.
   - Memory interfaces.
2. Mesh sizing and top-level configuration. This step includes specifying the following:
   - The number of rows and columns.
   - Global configuration parameters.
3. Device placement and configuration. This step involves:
   - Placement of devices and credited repeater slices between XPs based on floorplan needs.
   - Configuration of devices.

This section contains the following subsections:

- *1.5.1 System component selection* on page 1-22.
- *1.5.2 Mesh sizing and top-level configuration* on page 1-23.
- *1.5.3 Device placement and configuration* on page 1-26.

1.5.1 System component selection

This section describes the selection of system components comprising a CMN-600 system.

Requesting masters (RNs)

Requesting masters reside outside of the mesh and connect to CMN-600 ports.

Requesting masters with coherent caches (processors, GPUs, or processing elements with internal caches) are referred to as RN-F devices. They connect directly to the CMN-600 interconnect mesh using a CHI RN-F port.

I/O requesting masters without coherent caches (I/O masters, processing elements without internal caches, or with internal caches that are not hardware coherent) connect to RN-I bridge devices located within CMN-600 using ACE-Lite ports. The RN-I bridge device is located between the ACE-Lite interface and the internal CHI interface. Each RN-I bridge device has three ACE-Lite interfaces.

While an I/O requesting master can connect directly to a CMN-600 ACE-Lite port, multiple masters may share a single ACE-Lite port using external AMBA interconnect components. Consider traffic bandwidth requirements and physical floorplan trade-offs to determine whether I/O masters share 1-3 ACE-Lite ports or an RN-I.

Home nodes (HNs)

In CHI, each byte of memory is assigned to a single home node which is responsible for handling all memory transactions associated with that byte.

There are two types of home node devices within the CMN-600 system: HN-F and HN-I.

HN-F device instances are the home nodes for all coherent memory. HN-F also supports non-coherent memory accesses. Memory that is mapped to an HN-F targets DRAM. Each HN-F can contain an SF and an SLC slice. The amount of SLC should determine the number of HN-Fs.

The total amount of SLC needed divided by the number of HN-F instances determines the recommended SLC size for each HN-F instance. Generally, each HN-F partition has the same SLC size.

Note

The amount of SLC and number of HN-Fs are configured separately.

For best performance, the total SF size should be twice the total exclusive cache size for all RN-Fs. For example, for a 32MB RN-F total cache size, the recommended SF size would be 64MB.

HN-I device instances are the home nodes for all memory targeted at an ACE-Lite slave device or subsystem. HN-I does not support coherent memory. However, cacheable transactions can be sent to HN-I. Each HN-I instance contains a single ACE-Lite master port to send bus transactions to one or more slaves through an AMBA interconnect. The number of HN-I instances needed should be determined by the total ACE-Lite master bandwidth and slave peripherals' physical placement.

Note

HN-I instances with additional functionality are referred to by different names. For example, an HN-I that has a debug trace controller is called an HN-T. An HN-I that has a debug trace controller, DVM node and configuration slave is called an HN-D. The CMN-600 interconnect can have zero or more HN-I and HN-T instances. However, it must have exactly one HN-D instance.

CML interfaces

The CMN-600 interconnect supports up to four CXS (CCIX port) interfaces. A CXG device bridges between CHI and CXS, and contains CCIX *Request Agent* (RA) proxy and *Home Agent* (HA) proxy functionality. The CXG device also contains CXS *Link Agent* (LA) functionality, which is external to the CMN-600 hierarchy.

Memory interfaces

The CMN-600 interconnect supports two types of memory interface ports:

1. CHI SN port: Used to connect a native CHI.B, or CHI.C for CMN-600 R2, memory controller such as the CoreLink DMC-620 Dynamic Memory Controller.
2. AXI port: Used to connect an AXI memory controller via an SBSX bridge. See *Table 1-4 Device types* on page 1-24 for details.

1.5.2 Mesh sizing and top-level configuration

The size of the CMN-600 mesh primarily depends on the number of connected devices.

The minimum number of XPs is determined by the number of devices divided by two (rounded up). Additionally, the product of the X and Y mesh dimensions must be greater than or equal to the required number of XPs. For example, if seven XPs are needed, a 2×4 or 4×2 mesh would be acceptable.

The following table lists the device types that CMN-600 supports.

Table 1-4 Device types

Device	Name	Description
RN-I	Request Node I/O	A non-caching request node, bridging I/O master requests from 1-3 AXI or ACE-Lite interfaces
RN-D	DVM Request Node	An RN-I node that can accept DVM messages on the snoop channel
RNF_CHIA	Request Node Full with built-in SAM. CHI Issue A compliant.	CHI Issue A compliant processor, cluster, GPU or other request node with a coherent cache and a built-in SAM
RNF_CHIA_ ESAM	Request Node Full without a built-in SAM. CHI Issue A compliant.	CHI Issue A compliant processor, cluster, GPU or other request node with a coherent cache but without a built-in SAM
RNF_CHIB	Request Node Full with built-in SAM. CHI Issue B compliant.	CHI Issue B compliant processor, cluster, GPU or other request node with a coherent cache and a built-in SAM
RNF_CHIB_ ESAM	Request Node Full without a built-in SAM. CHI Issue B compliant.	CHI Issue B compliant processor, cluster, GPU or other request node with a coherent cache but without a built-in SAM
RNF_CHIC	Request Node Full with built-in SAM. CHI Issue C compliant.	CHI Issue C compliant processor, cluster, GPU or other request node with a coherent cache and a built-in SAM
RNF_CHIC_ ESAM	Request Node Full without a built-in SAM. CHI Issue C compliant.	CHI Issue C compliant processor, cluster, GPU or other request node with a coherent cache but without a built-in SAM
HN-F	Home Node Full	A fully coherent home node, typically configured with SLC and/or SF
HN-I	Home Node I/O	A non-coherent home node, bridging I/O slave requests to an ACE-Lite interface
HN-T	Home Node I/O with debug trace control	An HN-I with a built-in debug trace controller
HN-D	DVM Home Node	An HN-I with a built-in debug trace controller, *DVM Node* (DN), *Configuration Node* (CFG), Global Configuration Slave, and the *Power/Clock Control Block* (PCCB)
SN-F	Slave Node	A memory controller consisting of a native CHI SN interface
SBSX	CHI to AXI bridge	A CHI to AXI bridge that allows an AXI memory controller to be connected to CMN-600
CXG	CHI to CXS (CCIX port) bridge	A CHI to CXS (CCIX port) bridge that enables CML **Note** It comprises two entities: an internal CXRH device, including RA and HA functionality inside the CMN-600 hierarchy, and an external CXLA device.

The following table shows configurable options for mesh size, component counts, and top-level configuration (including associated parameters).

Table 1-5 Top-level configurable options

Feature	Parameter	Description	Values (Default)	Comments
Mesh dimensions	Mesh X dimension	Number of mesh columns	1-8	Mesh configurations not supported: • 1 × 1 • 1 × 2 • 2 × 1
	Mesh Y dimension	Number of mesh rows	1-8	
	MCSX count	Number of credited slices on a XP-XP mesh link in X dimension	0-4	This count is per link and can be different for each link.
	MCSY count	Number of credited slices on a XP-XP mesh link in Y dimension	0-4	
	DCS count	Number of credited slices on a device-XP link	0-4 without CCS 0-2 with CCS (CMN-600 R2)	
	CCS count	Number of credited slices on a CAL-XP link	0-2 (CMN-600 R2)	
Global parameter	PA_WIDTH	System Physical Address width	34, 44, 48 (48)	PA width of 48 is not supported in CMN-600 system with RNF_CHIA or RNF_CHIA_ESAM devices.
	CHIC_MODE_EN	CHI.C mode enable	0, 1	-
	R2_ENABLE	Enables CMN-600 R2 features.	0, 1	-
	REQ_ADDR_WIDTH	Width of Address field in REQ flit	44, 48 (48)	Address width of 48 is not supported in CMN-600 system with RNF_CHIA or RNF_CHIA_ESAM devices. REQ_ADDR_WIDTH must be set equal to or greater than PA_WIDTH.
	REQ_RSVDC_WIDTH	Width of RSVDC field in REQ flit	4, 8 (8)	-
	DATACHECK_EN	Datacheck enable	0, 1 (False)	Datacheck refers to data byte parity checking.
	FLIT_PAR_EN	Flit parity enable	0, 1 (True)	-
	NUM_REMOTE_RNF	Number of RN-Fs for CML configurations on all remote chips combined	0-64 (0)	-
	RNSAM_NUM_ADD_HASHED_TGT	Number of additional hashed target IDs supported by the RN SAM, beyond the local HN-F count	0, 2, 4, 8, 16, 32 (0)	-

Table 1-5 Top-level configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
Processor resources	Number of RN-Fs	The number of RN-Fs in the system. RN-Fs can be one of the following four types: • RNF_CHIA • RNF_CHIA_ESAM • RNF_CHIB • RNF_CHIB_ESAM • RNF_CHIC (CMN-600 R2) • RNF_CHIC_ESAM (CMN-600 R2)	1-32 without CAL 2-64 with CAL	All RN-Fs must be of the same type. **Note** When CAL is present, the number of RN-Fs must be even, and the RN-F type must be RNF_CHIB or RNF_CHIB_ESAM.
I/O resources	Number of RN-Is	The number of RN-I instances in the system	0-32	At least one RN-I or RN-D must be present. The total count of RN-Is and RN-Ds must not exceed 32.
	Number of RN-Ds	The number of RN-D instances in the system	0-32	
	Number of HN-Is	The number of HN-I instances in the system. This count includes the HN-D which is always present.	1-8	-
Debug resources	Number of DTCs	The total number of Debug Trace Controller domains.	1-4	The number of DTCs must not exceed the number of HN-Is.
System cache	Number of HN-Fs	The total number of HN-F instances in the system. The number of HN-Fs referred to by a given cache group (hashed entry in the SAM) must be a power of two.	1-32 without CAL 2-64 with CAL	Refer to *Chapter 4 SLC Memory System* on page 4-1078 for more details. **Note** When CAL is present, the number of HN-Fs must be even.
Memory resources	Number of SN-Fs	The number of SN-Fs (CHI interfaces)	0-8 For CMN-600 R2, 0-16 SN-Fs are supported.	At least one SN-F or SBSX must be present. The total count of SN-Fs and SBSXs must not exceed 16.
	Number of SBSXs	The number of SBSX instances (AXI interfaces)	0-8 For CMN-600 R2, 0-16 SBSXs are supported.	

1.5.3 Device placement and configuration

When the devices are enumerated and the mesh dimensions are determined, the placement of each device, or node, in the mesh must be specified.

While there are no constraints on a device's mesh location, optimal device placement is driven by floorplanning and performance constraints, and is outside the scope of this document.

Individual CMN-600 devices can be configured using the options shown in the following table.

Note

When CAL is present, both devices connected to it are configured identically.

Table 1-6 CHI device configurable options

Feature	Parameter	Description	Values (Default)	Comments
RN-F port, SN-F port	DEV_POISON_EN	Data poison enable (RN-F port only)	0, 1 (1)	Must be set to 0 for RNF_CHIA or RNF_CHIA_ESAM device
	DEV_DATACHECK_EN	Datacheck enable (RN-F port only) **Note** DEV_DATACHECK_EN must be set to 0 when global parameter DATACHECK_EN is 0.	0, 1 (0)	End-to-end data byte parity enable. Must be set to 0 for RNF_CHIA or RNF_CHIA_ESAM device.
	RXBUF_NUM_ENTRIES	Number of receive flit buffers inside CMN-600 on this port. To achieve full bandwidth operation, this number must equal the CHI credit return latency (in cycles) for flit transfers from RN-F or SN-F to the interconnect. **Note** The credit return latency is 1 cycle in the interconnect. This must be added to the credit latency in the RN-F or SN-F to arrive at the total credit return latency.	2-4 (3)	The minimum value of 2 corresponds to a credit return latency of 1 cycle in the interconnect and 1 cycle in the RN-F or SN-F.

Table 1-6 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
RN-I, RN-D	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	NUM_WR_REQ	Number of Write Request Tracker entries	4, 16, 24, 32 (32)	For CMN-600 R2, 64 Write Req Tracker entries are supported.
	NUM_RD_REQ	Number of Read Request Tracker entries	4, 32, 64, 96, 128 (32)	For CMN-600 R3, 256 Read Req Tracker entries are supported. **Note** If NUM_RD_BUF is 128 or 256, NUM_RD_REQ needs to be same value. **Note** The number of tracker entries needs to be the same or larger than data buffer entries. NUM_RD_REQ >= NUM_RD_BUF.
	NUM_RD_BUF	Number of read data buffers	4, 16, 24, 32, 64, 96, 128 (24)	For CMN-600 R3, 256 Read data buffers are supported. **Note** NUM_RD_BUF > 64 will instantiate RAM for data buffer.
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (1)	-
	FORCE_RDB_PREALLOC	Force read data buffer pre-allocation	0, 1 (0)	-

Table 1-6 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
HN-F	SLC_SIZE	Size of system cache	0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, 4MB (2MB)	-
	SF_SIZE	Size of SF tag RAM	512KB, 1MB, 2MB, 4MB, 8MB (4MB)	-
	SLC_TAG_RAM_LATENCY	Latency of system cache tag RAM	1-3 cycles (2)	Valid Tag:Data RAM latency combinations: • 1:2 • 2:2 • 3:3
	SLC_DATA_RAM_LATENCY	Latency of system cache data RAM	2-3 cycles (2)	
	NUM_ENTRIES_POCQ	Number of entries in the POCQ tracker	32, 64 (32)	
HN-I, HN-D	NUM_AXI_REQS	Number of Request Tracker entries	8, 32, 64 (32)	-
	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (0)	-
	DVM_V8_1_EN	Enable Armv8.1-A DVMs (HN-D only)	0, 1 (1)	-
	DN_NUM_VMF_PARAM	Number of VMID filter registers	4, 16 (4)	CMN-600 R2 feature only.
SBSX	AXDATA_WIDTH	Data width on ACE-Lite/AXI interface	128, 256 (128)	-
	AXDATAPOISON_EN	Data poison enable on ACE-Lite/AXI interface	0, 1 (1)	-
	NUM_DART	Number of Tracker entries	64, 128 (64)	-
	NUM_WR_BUF	Number of write buffers	8, 16 (8)	-

Table 1-6 CHI device configurable options (continued)

Feature	Parameter	Description	Values (Default)	Comments
CXG	RA_NUM_REQS	Depth of Request Tracker	64, 128, 256 (256)	-
	RA_NUM_RDBUF	Depth of Read Data Buffer	16, 24, 32 (16)	-
	RA_NUM_WRBUF	Depth of Write Data Buffer	16, 24, 32 (24)	-
	RA_NUM_SNPREQS	Depth of Snoop Tracker	64, 128, 256 (128)	-
	RA_NUM_SNPBUF	Depth of Snoop Data Buffer	16, 24, 32 (32)	-
	HA_NUM_REQS	Depth of request tracker	128, 192, 256 (192)	-
	HA_NUM_WRBUF	Depth of Write Data Buffer	96, 128 (96)	-
	HA_NUM_SNPREQS	Depth of Snoop Tracker. This indicates the number of outstanding snoop request HA can have on CCIX	96, 128, 256 (96)	-
	HA_NUM_SNPBUF	Depth of Snoop Data Buffer	16, 24, 32 (24)	-
	HA_SSB_DEPTH	This depth indicates the maximum number of remote snoop requests from the local chip that can be sunk at this HA.	96, 128, 256 (96)	This value must be at least as large as HA_NUM_SNPREQS
	DB_FIFO_DEPTH	FIFO Depth in CXLA Domain Bridges - CXDB, PDB	6, 8 (8)	-

MCS

The CMN-600 mesh is designed to operate with a single cycle of latency between XPs. However, depending on the fabrication process and the distance between XPs, a single-cycle XP-XP connection may limit frequency. In this case, one or more register slices can be added to lengthen the XP-XP links. Register slices add link transfer latency, but the frequency gained can justify the trade-off.

To add an extra cycle between two XPs, a *Mesh Credited Slice* (MCS) is specified. One to four MCSs can be added to any link between XPs.

An MCS placed between adjacent XPs in the same row is called an MCSX. Similarly, one placed between adjacent XPs in the same column is called an MCSY.

DCS

A credited slice placed between a device and an XP is called a *Device Credited Slice* (DCS). One to four DCSs can be added to any link between a device and an XP.

The following figure shows an example configuration including an MCSX, MCSY, and DCS.

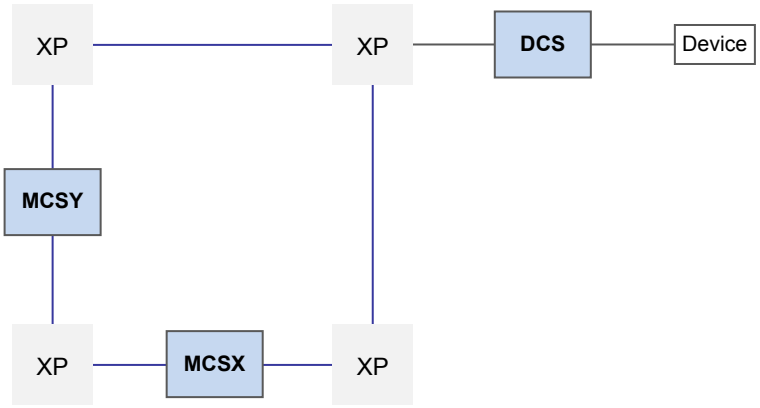


Figure 1-2 Example MSCX, MSCY, and DCS configuration

CAL and CCS

A *Component Aggregation Layer* (CAL) can be placed at an XP port for port expansion. CAL allows up to two devices of the same type to be connected to a single XP port.

A credited slice placed between a CAL and an XP is called a *CAL Credited Slice* (CCS). One to two CCSs can be added to any link between a CAL and an XP.

Note

When CCS is used (with CMN-600 R2 only), the number of DCSs between CAL and device is limited to a maximum of two.

The following figure shows an example configuration including an MCSX, MCSY, DCS, CAL, and CCS.

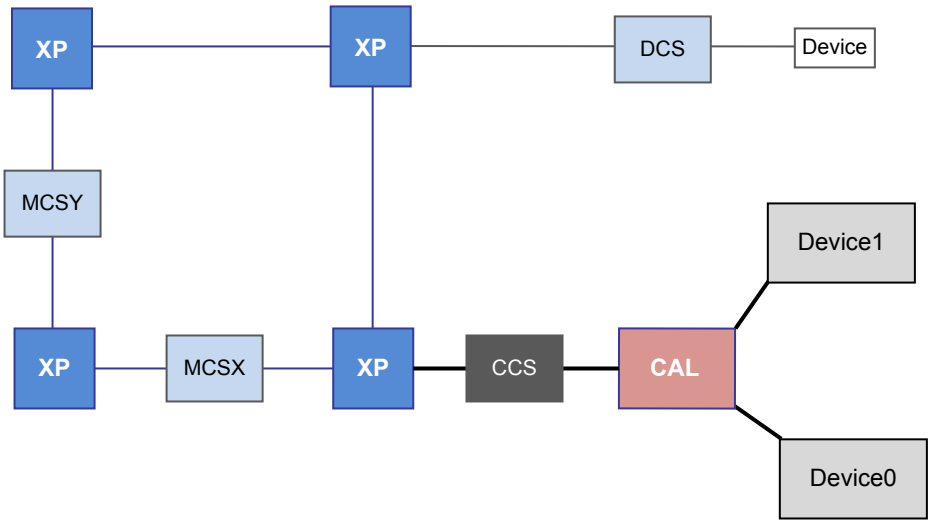


Figure 1-3 Example MSCX, MSCY, CCS, and DCS configuration

1.6 Test features

The CMN-600 product includes several test features.

See the *Arm® CoreLink™ CMN-600 Coherent Mesh Network Configuration and Integration Manual* for information about the test features.

1.7 Product documentation and design flow

This section describes the CMN-600 books and how they relate to the design flow.

Documentation

The CMN-600 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of CMN-600. It is required at all stages of the design flow. The choices you make in the design flow can mean that some behavior described in the TRM is not relevant. If you are programming the CMN-600 product, contact:

- The implementer to determine:
  - The build configuration of the implementation.
  - What integration, if any, was performed before implementing the CMN-600 product.
- The integrator to determine the pin configuration of the device that you are using.

Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes how to integrate the CMN-600 product into an SoC. It includes a description of the pins that the integrator must tie off to configure the macrocell for the required integration. Some of the integration affected by the configuration options used when implementing the CMN-600 product include:

- The available build configuration options and related issues in selecting them.
- How to configure the *Register Transfer Level* (RTL) with the build configuration options.
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The Arm product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by Arm are example reference implementations. Contact your EDA vendor for EDA tool support.

User Guide

The *User Guide* describes how to use Socrates to configure and integrate a custom mesh interconnect. Configurables include size and device placement and an optional System Level Cache (SLC).

——— **Note** ———

The User Guide is part of the **Socrates IP tooling** product download bundle.

———————————

Design flow

CMN-600 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer configures and synthesizes the RTL to produce a hard macrocell. This process includes integrating RAMs into the design.

Integration

The integrator connects the implemented design into an SoC. This process includes connecting a memory system and peripherals.

Programming

This is the last process. The system programmer develops the software required to configure and initialize the CMN-600 product, and tests the required application software.

Each process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the CMN-600 product.

The operation of the final device depends on:

Build configuration
The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

Configuration inputs
The integrator configures some features of the CMN-600 product by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration
The programmer configures the CMN-600 product by programming particular values into registers. These configurables affect the behavior of the CMN-600 product.

——— **Note** ———

This manual refers to implementation-defined features that are applicable to build configuration options. Reference to a feature that is included means that the appropriate build and pin configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

———————————

1.8 Product revisions

This section describes the differences in functionality between successive product revisions of the CMN-600 product.

r0p0
First release.

r1p1 (LAC)
First release: includes CML (Alpha product status) content.

r1p0 (EAC)
First release: includes CML (Beta product status) content.

r1p1 (EAC)
First release: includes CML (Beta product status) content.

r1p2 (EAC)
First release: includes CML (LAC product status) content.

r1p3 (EAC)
First release: includes CML (EAC product status) content.

r2p0 (EAC)
Second release: includes CML (EAC product status) content.

Chapter 2
Functional Description

This chapter describes the functionality of the CMN-600 product.

It contains the following sections:

2.1 About the functions

CMN-600 allows creation of a complete SoC system that includes more devices than those described in this section.

This section contains the following subsections:

2.1.1 Crosspoint

The *crosspoint* (XP) is a switch, or router logic module. It is the fundamental component building block of the CMN-600 transport mechanism.

The CMN-600 mesh interconnect is built using a set of XP modules arranged in a two-dimensional rectangular mesh topology. Each XP can connect to up to four neighboring XPs using mesh ports, shown as dotted lines in the following figure. Each XP also has two device ports for connecting devices: P0 and P1.

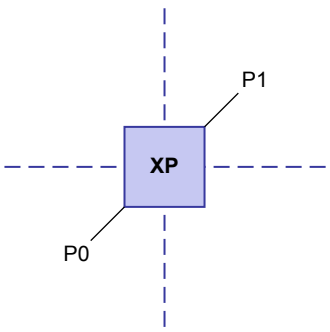


Figure 2-1 Crosspoint

Each XP supports these four CHI channels for transporting flits across the mesh from a source device to a destination or target device:

- *Request* (REQ).
- *Response* (RSP).
- *Snoop* (SNP).
- *Data* (DAT).

The maximum size CMN-600 mesh is built using 64 XPs arranged in an 8 × 8 grid. Each XP in the grid is referenced using an (X,Y) coordinate system. (0,0) represents the bottom-left corner, and a maximum coordinate of (7,7) represents the upper right corner. The following figure shows the maximum 8 × 8 mesh configuration, and some (X,Y) coordinate values.

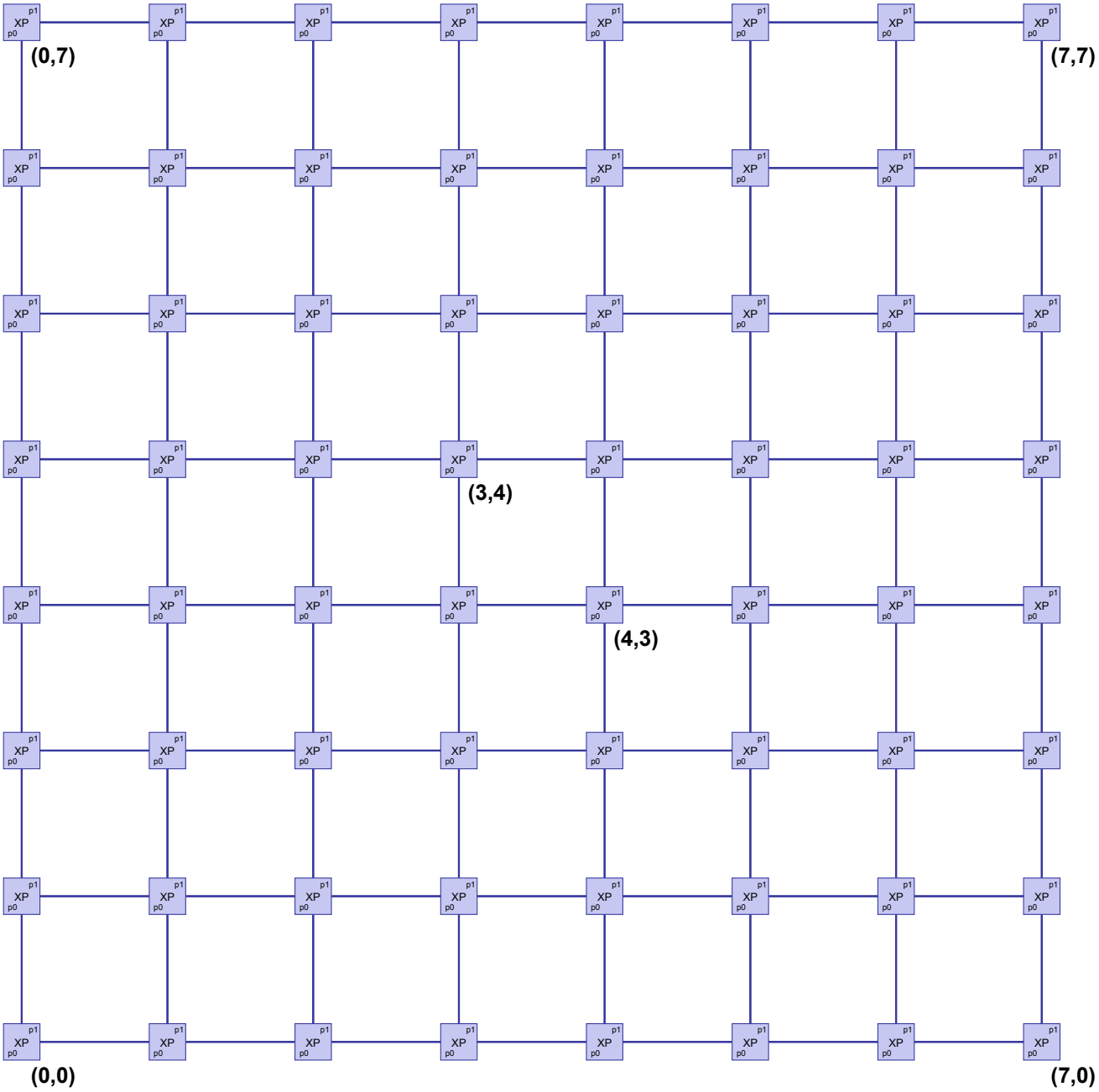


Figure 2-2 8 × 8 maximum mesh configuration

The following figure shows an example 6 × 6 mesh configuration, with devices attached to XP ports.

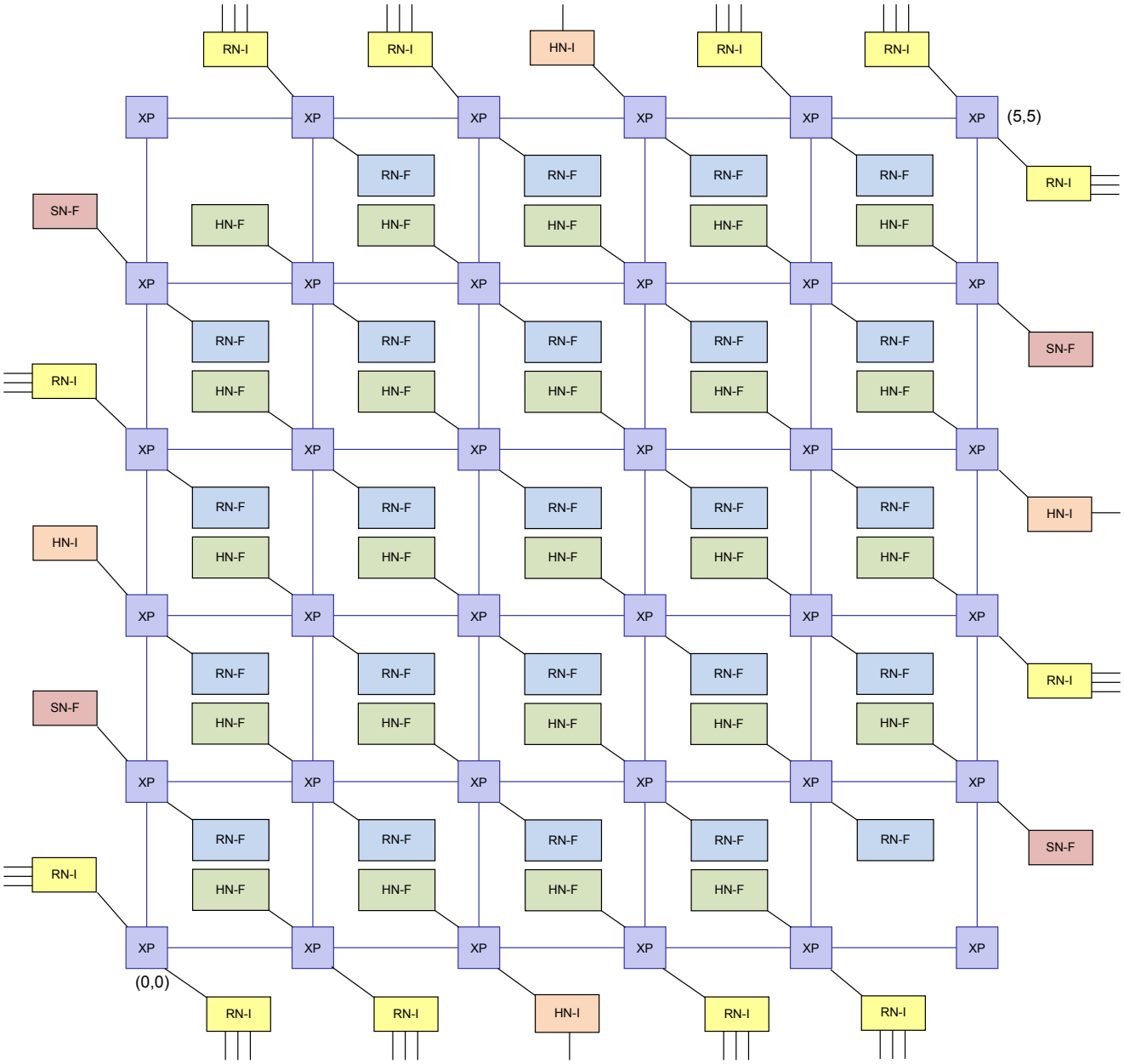


Figure 2-3 Example 6 × 6 mesh configuration

2.1.2 Request node I/O bridge

The *I/O-coherent Request Node* (RN-I) bridge connects I/O-coherent AMBA masters to the rest of the CMN-600 system.

An RN-I bridge includes up to three ACE-Lite/ACE-Lite+DVM slave ports.

The RN-I bridge can act as a proxy only for masters that do not contain hardware-coherent caches, because there is no capability to issue snoop transactions to them.

2.1.3 Fully coherent home node

The *Fully coherent Home Node* (HN-F) is responsible for managing part of the address space.

The HN-F consists of the following:

System Level Cache The system level cache is a last-level cache. The system level cache-allocation policy is exclusive for data lines, except where sharing patterns are detected and pseudo-inclusive for code lines, as indicated by the RN-Fs. All code lines can be allocated into the system level cache on the initial request.

Combined PoS/PoC The combined *Point-of-Serialization/Point-of-Coherency* (PoS/PoC) is responsible for the ordering of all memory requests sent to the HN-F. This includes serialization of multiple outstanding requests and actions to the same line, and request ordering as required by the RN-F.

Snoop filter The snoop filter reduces snoop traffic in the system by tracking cache lines that are present in the RN-Fs, generally favoring directed snoops over snoop broadcasts when possible. This substantially reduces the snoop response traffic that might otherwise be required.

Each HN-F in the system is configured to manage a specific portion of the overall address space.

The entire DRAM space is managed through the combination of all HN-Fs in the system.

Note

The HN-F is architecturally defined to manage only well-behaved memory. Well-behaved memory refers to memory without any possible side effects. The HN-F includes microarchitectural optimizations to exploit this architectural guarantee.

2.1.4 Home node I/O bridge

The *I/O Home Node* (HN-I) is a home node for all CHI transactions targeting AMBA slave devices.

The HN-I acts as a proxy for all the RNs of CMN-600, converting CHI transactions to ACE5-Lite transactions. The HN-I includes support for the correct ordering of Arm device types.

The HN-I does not support caching of any data read from or written to the downstream ACE5-Lite I/O slave subsystem. This means that any cacheable request sent to the HN-I does not result in any snoops being sent to RN-Fs in the system, but is instead converted to the appropriate ACE5-Lite read or write command and sent to the downstream ACE5-Lite subsystem. If an RN-F does cache data read from or written to the downstream ACE5-Lite I/O slave subsystem, coherency is not maintained, and any subsequent access to that data reads from or writes to the ACE5-Lite I/O slave subsystem directly, ignoring the cached data.

2.1.5 SBSX

The *AMBA 5 CHI to ACE5-Lite bridge* (SBSX) enables an ACE5-Lite slave device such as a CoreLink DMC-400 Dynamic Memory Controller, to be used in a CMN-600 system.

2.1.6 CXG

A CXG device bridges between CHI and CXS.

A CXG device bridges between CHI and CXS (CCIX port) and contains:

1. *CCIX Request Agent* (**CXRA**) proxy and *CCIX Home Agent* (**CXHA**) proxy functionality.
2. *CXS Link Agent* (**CXLA**) functionality which is external to the CMN-600 hierarchy.

2.1.7 Configuration node

The *Configuration node* (CFG), co-located with the HN-D node, is responsible for handling configuration accesses, error reporting and signaling, interrupt generation, and centralized debug and performance monitoring (PMU) support features.

The CFG includes the following dedicated ports:

- Ports to collect error signals from CHI components within CMN-600.
- A configuration bus which connects to all the nodes to handle internal configuration register reads and writes.

The CFG does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

2.1.8 Power/Clock Control Block

The *Power/Clock Control Block* (PCCB), co-located with the HN-D node, provides separate communication channels. These channels pass information about the power and clock management between the SoC and the network.

The PCCB acts as an aggregator to convey information between the SoC and the other CMN-600 components, in the following manner:

- The PCCB receives transaction activity indicators from other relevant CMN-600 components and conveys that information to the external power and clock control units.
- When the PCCB receives a power or clock control management request from the external power or clock control units, it conveys that request to the relevant CMN-600 components, where applicable.
- The PCCB waits for the appropriate responses from the relevant CMN-600 components, and conveys an aggregated response to the external power and clock control units.

The PCCB does not have a dedicated CHI port. It shares a device port with the HN-D node in the mesh.

2.1.9 System Address Map overview

All CHI commands must include a fully resolved network address. the address must include a source and target ID. Target IDs are achieved by passing a request address through a *System Address Map* (SAM), which effectively maps a memory or I/O address to the target device.

The SAM functionality is required for each requesting device.

The SAM consists of two logical units:

- An RN SAM for each RN to map addresses to HN-F, HN-I, and HN-D target IDs.
- An HN-F SAM in the HN-F, that maps addresses to *Memory Controller* (MC) target IDs.

CMN-600 has software-configurable SAM blocks which allow a single implementation of CMN-600 to support programmable mappings of addresses to HNs and SNs.

The RN SAM supports generating an MC target ID. This target ID can be used to issue PrefetchTgt operations from the RN directly to the MC.

2.1.10 Debug and Trace Controller

The *Debug and Trace Controller* (DTC) controls distributed *Debug and Trace Monitors* (DTM) and generates time stamped trace via ATB interface.

The DTC generates event or PMU-based interrupt. The main functions are:

- Receive packets from DTM and pack into ATB format trace.
- Time stamp trace with SoC timer input.
- Generate alignment sync for the ATB trace output.
- Handle ATB flush request.
- Handle debug and secure debug external request.
- Provide a consistent view of distributed and central PMU counters.
- Handle PMU snapshot request.
- Generate interrupt **INTREQPMU** assertion on overflow of PMU counters.

2.1.11 QoS regulator

CMN-600 supports end-to-end *Quality-of-Service* (QoS) which guarantees using QoS mechanisms distributed throughout the system.

The QoS provision uses the QoS field in each RN request packet to influence arbitration priority at every QoS decision point. The QoS field is then propagated through all secondary packets issued by a request packet. RNs must either self-modulate their QoS priority depending on how well their respective QoS requirements are being met, or make use of the integrated QoS regulators at ingress points to CMN-600.

It is possible to include non-QoS-aware devices in the system, but still have these devices meet the QoS modulation requirement of the QoS architecture. To enable this, CMN-600 includes inline regulators that perform the QoS functionality without the requesting device requiring any awareness of QoS. A *QoS Regulator* (QR) provides an interstitial layer between an RN and the interconnect. The QR monitors how the bandwidth and latency requirements of the RN are met, and does in-line replacement of the RN-provided QoS field, adjusting upwards to gain additional priority in the system, and downwards to reduce priority.

2.1.12 Credited slices

Optional credited slices can be placed between XPs or at any given XP or device interface to assist in timing closure in a CMN-600 system.

Credited slices enable synchronous but higher latency communication at any point in the system.

Refer to *1.5 Configurable options* on page 1-22 for more information on credited slices.

2.1.13 Component Aggregation Layer

The *Component Aggregation Layer* (CAL) allows up to two RN-F_CHIB, RN-F_CHIB_ESAM, or HN-F devices to be connected to a device port on the XP.

Both devices must be of the same type and must be configured identically. The following image shows a CAL sample configuration.

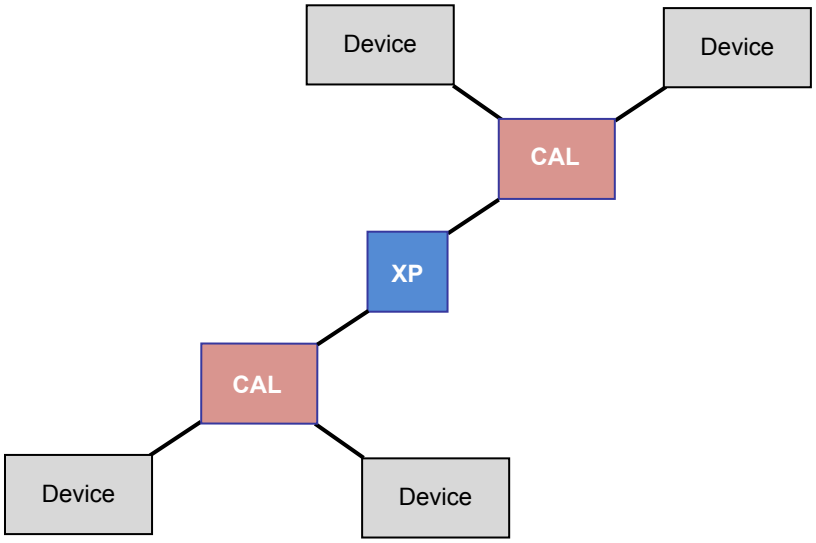


Figure 2-4 CAL Sample configuration

In addition, CAL must be used consistently across all devices of the same type in the interconnect. For example, if HN-Fs require a CAL, then all HN-F instances in the interconnect must be connected to the XP using a CAL.

2.2 System configurations

This section provides CMN-600 system configuration examples.

Small configuration

The following figure shows a 1 × 3 mesh for a small system configuration containing single instances of RN-F, HN-F, RN-D, SN-F, and HN-D.

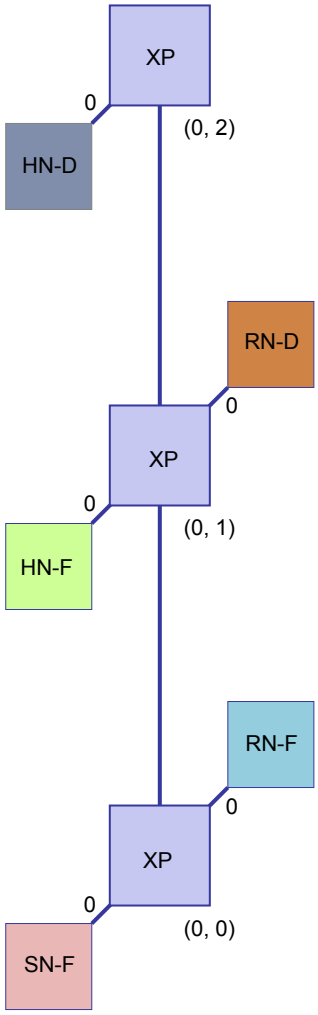


Figure 2-5 1 × 3 mesh example

Medium configuration

The following figure shows a 4 × 2 mesh for a medium system configuration with single and multiple instances.

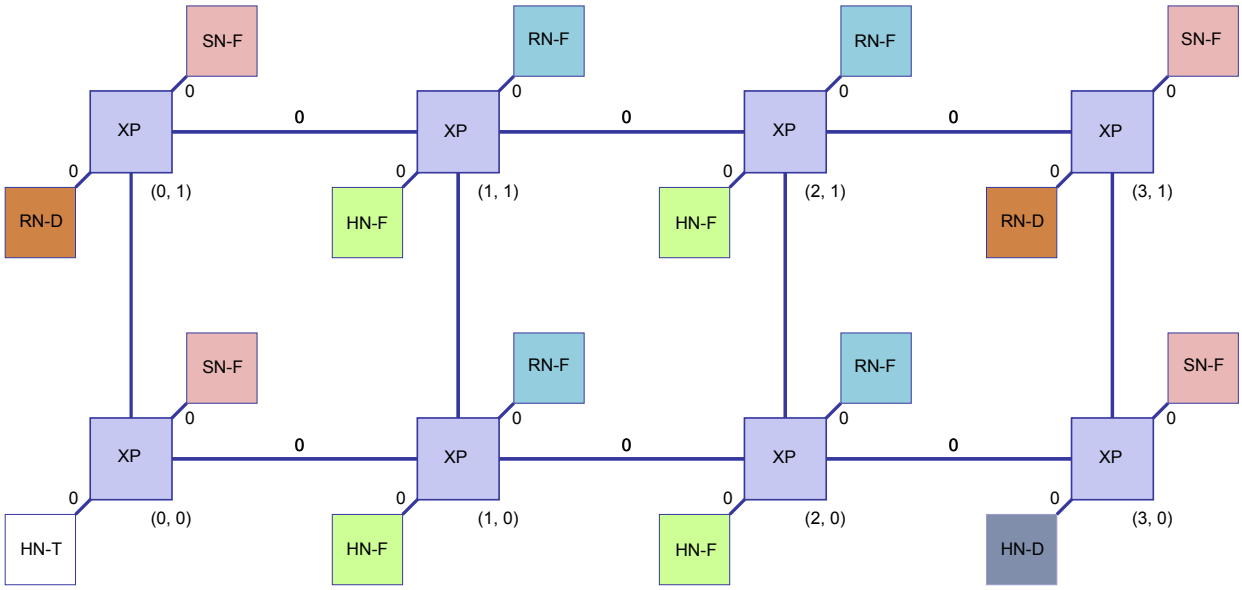


Figure 2-6 4 × 2 mesh example

Large configuration

The following figure shows a 3 × 5 mesh for a medium system configuration with multiple instances.

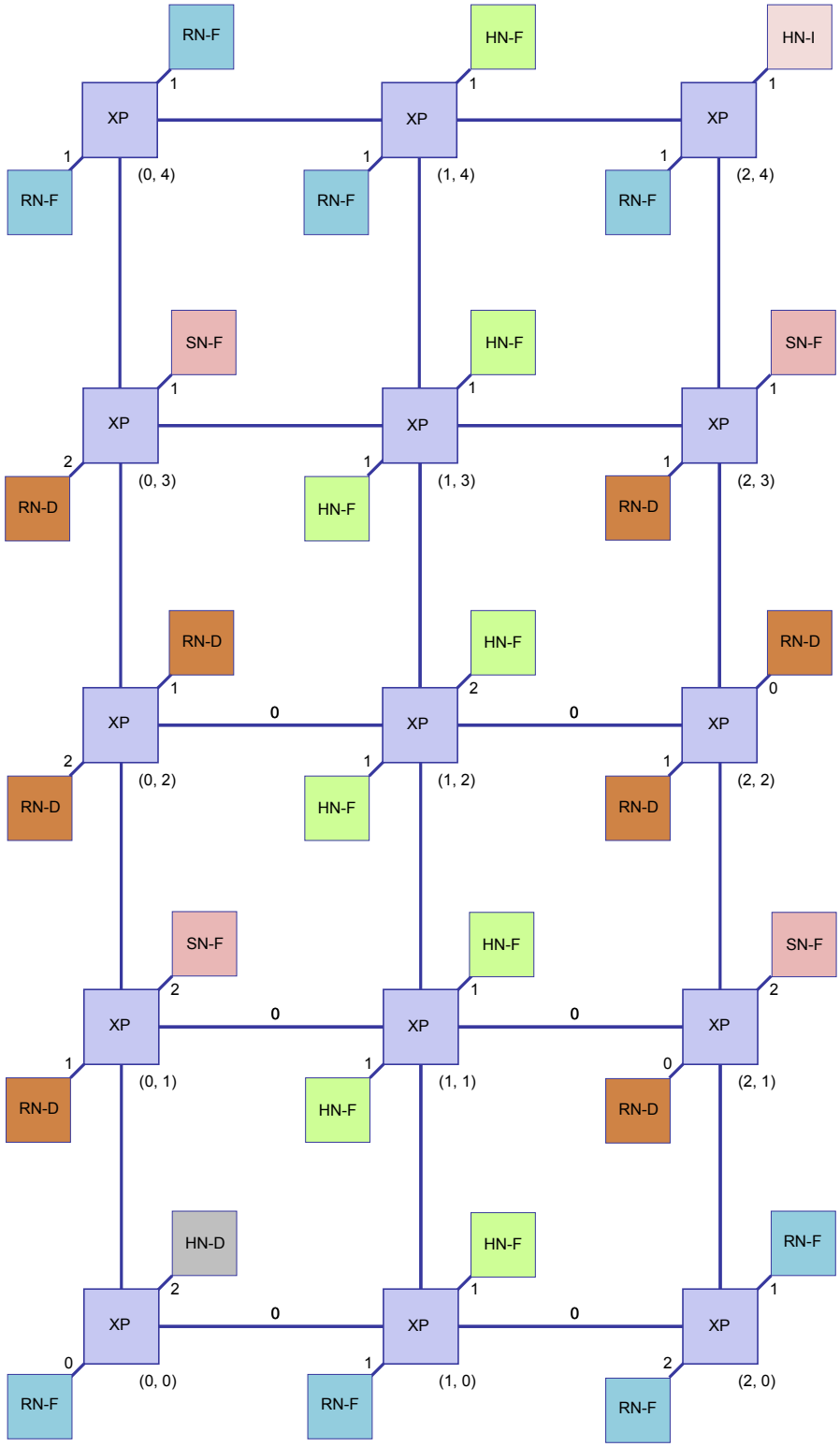


Figure 2-7 3 × 5 mesh example

Medium configuration with R2 CAL

The following figure shows a 2 × 4 mesh for a medium system configuration with RN-F and HN-F CAL in the gray highlighted areas.

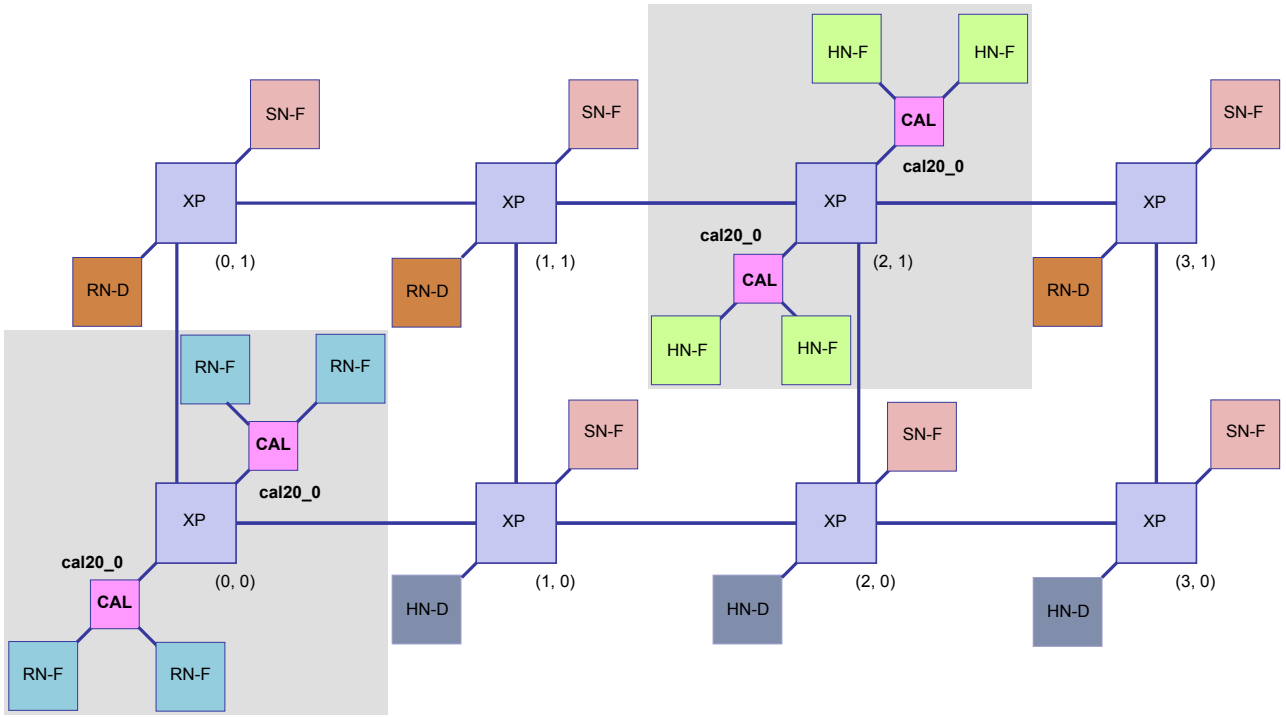


Figure 2-8 2 × 4 mesh example with R2 CAL

2.3 CML system configurations

This section provides CML system configuration examples.

Single CML configuration

The following figure shows a 4 × 2 mesh with a single CXG instance.

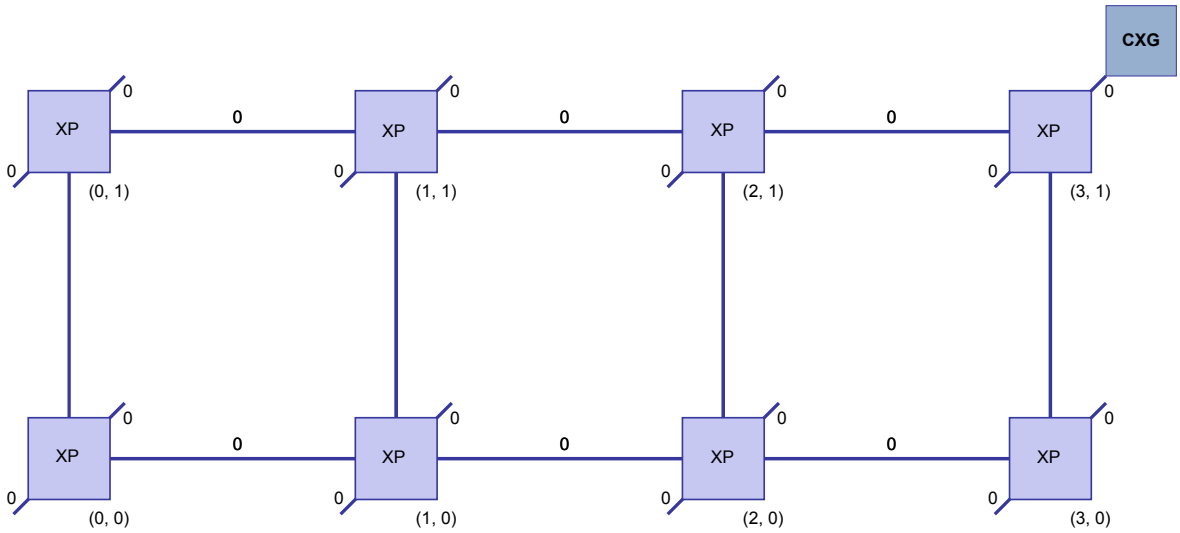


Figure 2-9 4 × 2 single CML mesh example

Double CML configuration

The following figure shows a 4 × 2 mesh with two CXG instances.

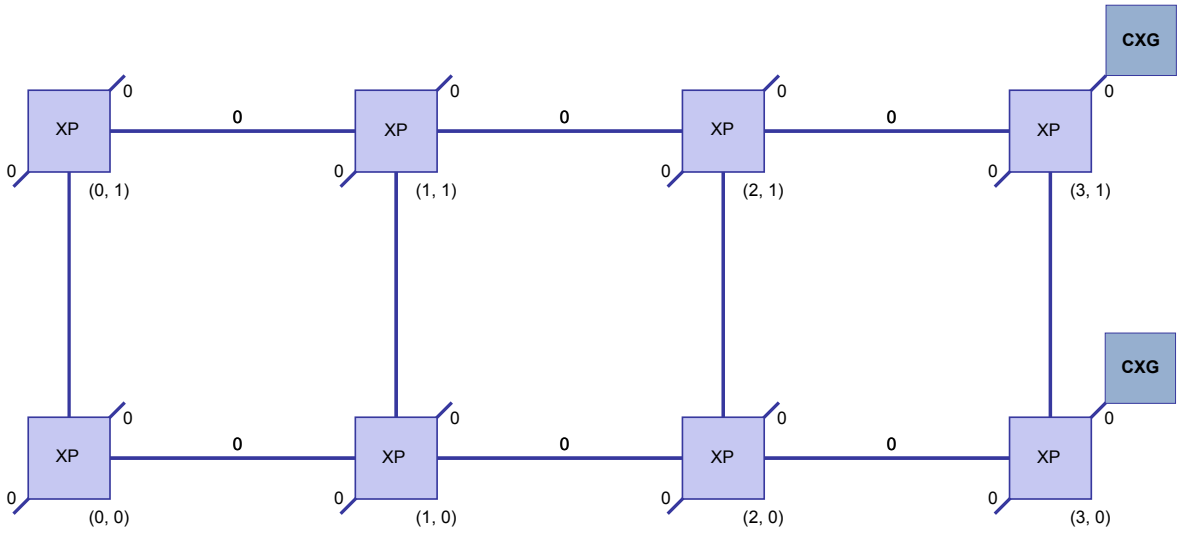


Figure 2-10 4 × 2 double CML mesh example

CXG components

A CXG device bridges between CHI and CXS, and contains CCIX *Request Agent* (RA) proxy and *Home Agent* (HA) proxy functionality. The CXG device also contains CXS *Link Agent* (LA) functionality, which is external to the CMN-600 hierarchy. A simple CXG block diagram is shown in the following figure.

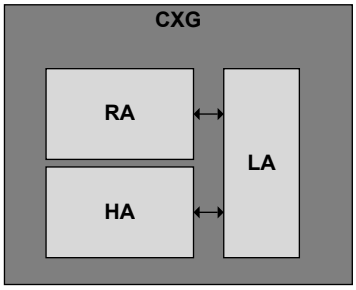


Figure 2-11 CXG block diagram with RA, HA, and LA

CCIX topologies

The following figure shows three simplified CCIX topology examples.

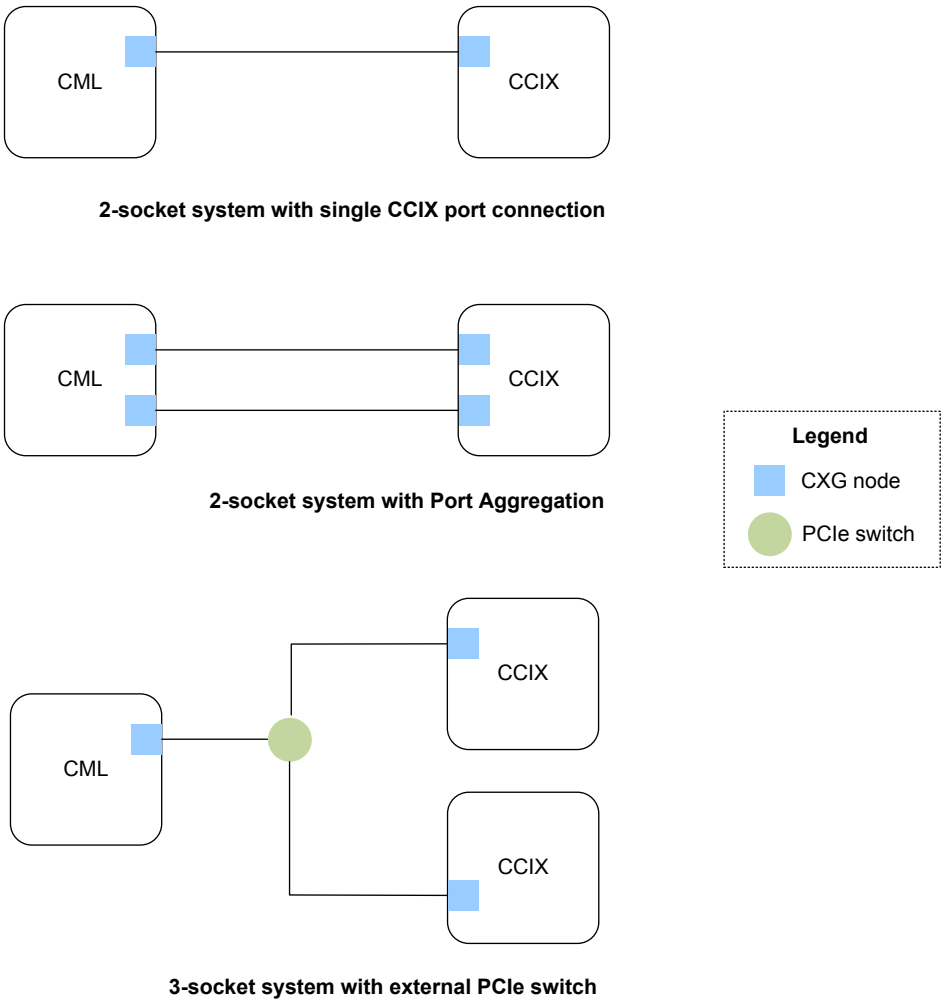


Figure 2-12 CCIX topologies

2.4 Node ID mapping

CMN-600 node ID mapping to devices is based on their physical positions on the mesh.

The physical position of a device connected to an XP is determined by the XP's X and Y coordinates and the XP port (0 or 1) it is connected to. The device node ID is mapped to: (X, Y, Port, `2'b00`).

Note

1. The bit widths of the X and Y parameters are dependent on the configured size of the mesh.
2. The naming convention for I/O signals uses decimal values of the node ID. For example, `RXREQFLIT_NIDxxx` uses `xxx` values in decimal.

The node ID size depends on the X and Y dimensions of the CMN-600 mesh. The larger of the X and Y dimensions determines the size as shown in the following table.

Table 2-1 Example CMN-600 system with node IDs

Mesh X dimension	Mesh Y dimension	Node ID size
X_dim <= 4	Y_dim <= 4	7 bits
4 < X_dim <= 8	Y_dim <= 8	9 bits
X_dim <= 8	4 < Y_dim <= 8	

The following tables contain the different node ID formats.

Table 2-2 7-bit node ID format

NodeID[6:5]	NodeID[4:3]	NodeID[2]	NodeID[1:0]
2-bit X position	2-bit Y position	Port	`2'b00`

Table 2-3 9-bit node ID format

NodeID[8:6]	NodeID[5:3]	NodeID[2]	NodeID[1:0]
3-bit X position	3-bit Y position	Port	`2'b00`

An example CMN-600 system with 7-bit node IDs in (X, Y, Port, `2'b00`) format is provided in the following figure.

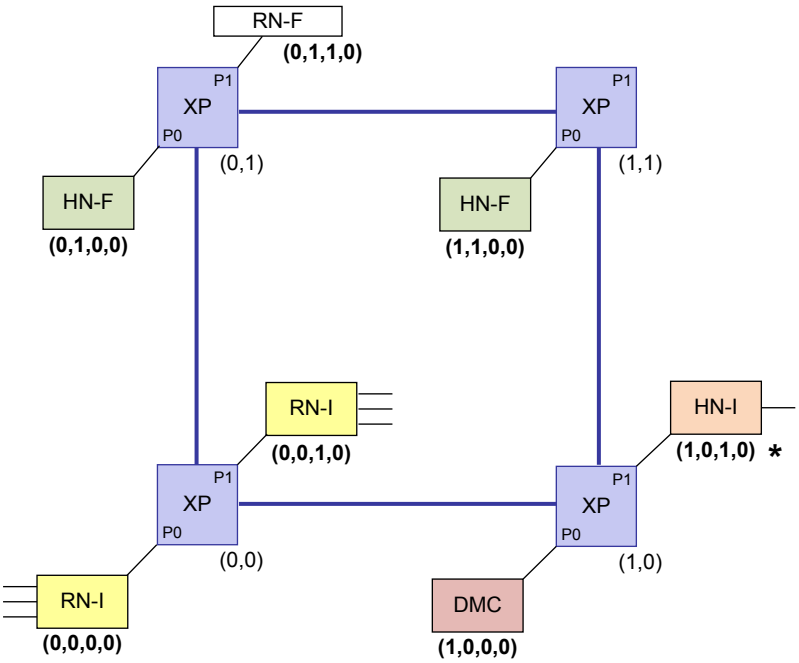


Figure 2-13 Example system with 7-bit node IDs

The 7-bit node ID format is (X, Y, Port, DevID). For the HN-I connected to XP (1,0), the node ID reads as (1, 0, 1, 0). This is equivalent to (`2'b01`, `2'b00`, `1'b1`, `2'b00`) or `0x24`.

When CAL is present, the two devices connected to the CAL are assigned consecutive node IDs where one device is assigned NodeID[1:0]=2'b00 and the other device is assigned NodeID[1:0]=2’b01. An example CMN-600 system with CAL and 7-bit node IDs in (X, Y, Port, DevID) format is provided in the following figure.

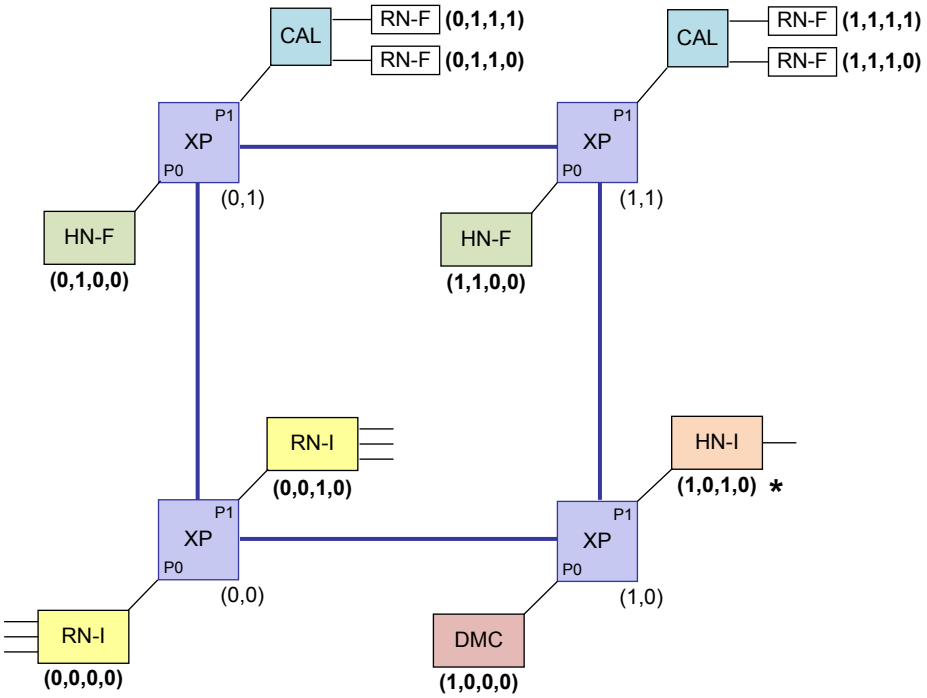


Figure 2-14 Example system with 7-bit node IDs with CAL

2.5 Discovery

Discovery is a software algorithm used to discover the configuration of CMN-600.

Software uses the discovery mechanism to identify the location (CHI NodeID) and logical ID corresponding to all the node types: DVM, Global CFG, DTC, HN-F, HN-I, RN-D, RN SAM, RN-I, SBSX, and XP. For CML, logical node types also include CXRA, CXHA, and CXLA.

The discovery process also provides information whether the discovered node in question is external or internal to CMN-600.

The following figure shows a sample configuration. At the end of the discovery process, software should have enough information to know the location of the global configuration registers, the configuration registers for each XP, the HN-F, and the RN SAM corresponding to the RN-F.

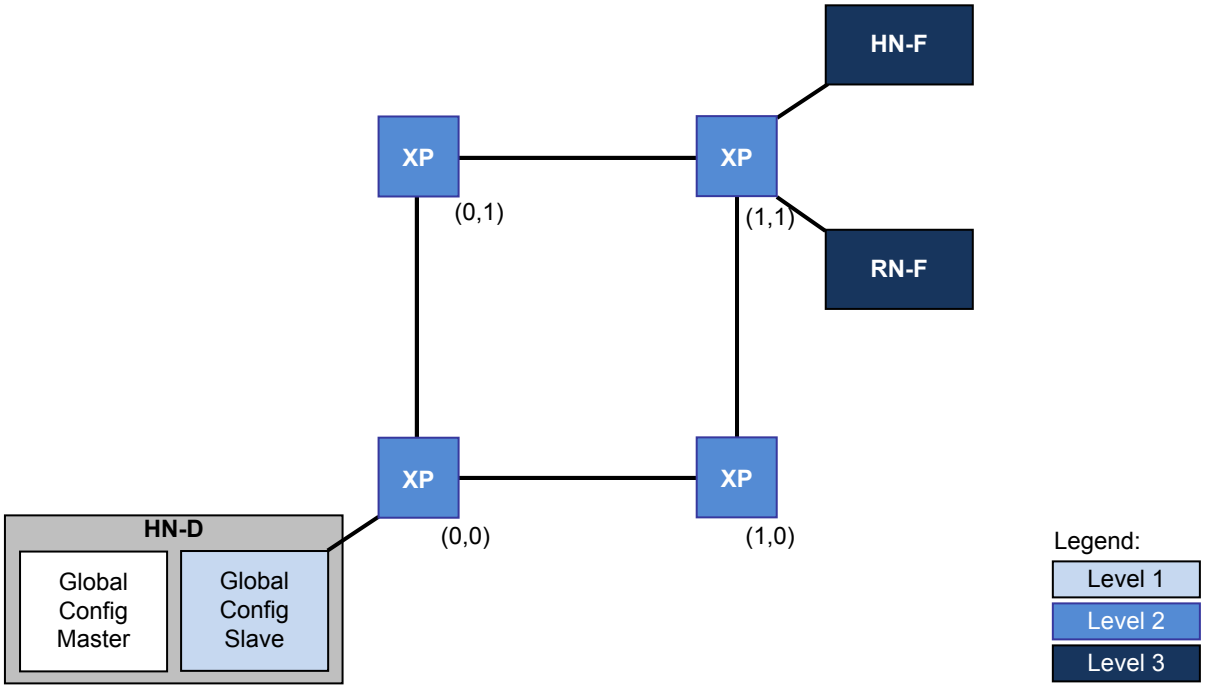


Figure 2-15 2x2 Register Tree Example

This section contains the following subsections:

- *2.5.1 Configuration address space organization* on page 2-54.
- *2.5.2 Configuration register node structure* on page 2-57.
- *2.5.3 Child pointers* on page 2-60.
- *2.5.4 Discovery tree structure* on page 2-64.

2.5.1 Configuration address space organization

This section contains configuration address space organization information. It describes two system addresses, PERIPHBASE and ROOTNODEBASE, that are required for this process.

PERIPHBASE

All CMN-600 configuration registers are mapped to an address range, starting at PERIPHBASE address aligned to 64MB with a maximum size of 64MB for a system with the X and Y dimensions of four or less. PERIPHBASE address should be aligned to 256MB and the register address range is maximum 256 MB if one of the mesh dimensions is more than four.

ROOTNODEBASE

The address to the Root Node where the discovery process can start. The configuration registers at ROOTNODEBASE contain global information and configuration, as well as the first level of discovery information for components in the system.

Discovery determines specific addresses for individual system blocks that have implementation-defined register spaces as illustrated in the following figure.

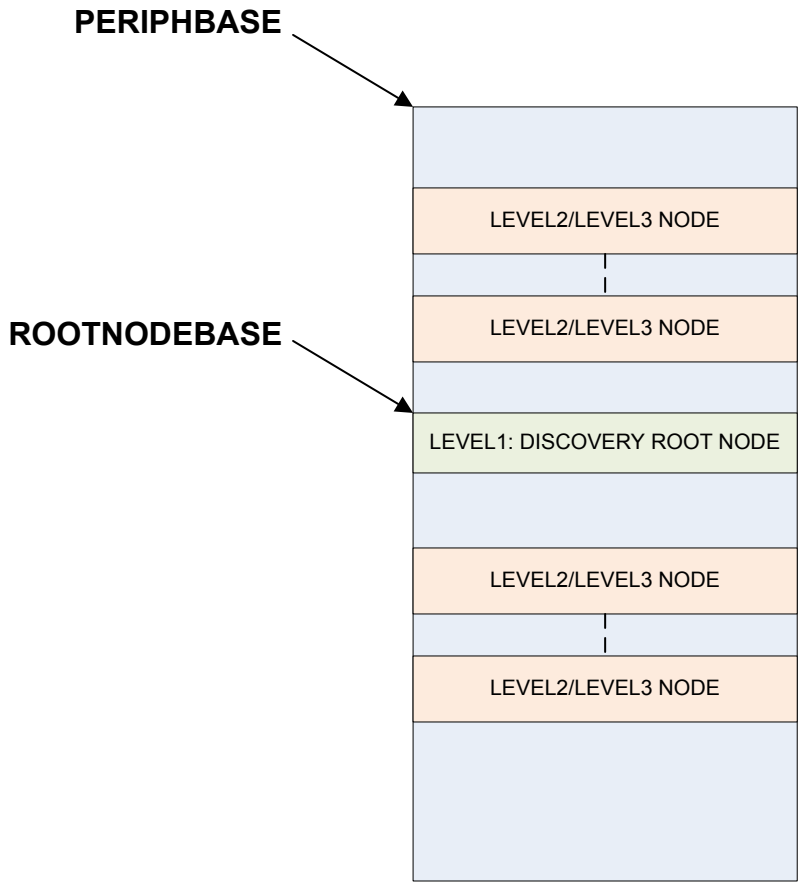


Figure 2-16 PERIPHBASE and ROOTNODEBASE addresses

Register organization consists of:

- CMN-600 supports 4-byte and 8-byte software accessible registers.
- Software using 32-bit and 64-bit register reads.

All registers are organized into several register-blocks as nodes. A node:

- Is a register block with the size of 16KB.
- Is associated with a logical block in the design.
- Has implementation-specific information and configuration for that block.

A node can be:

- Pure hierarchy: No device info. Just children.
- Leaf: No children. Just device info.
- General: Device info, plus children.

A node can have pointers to one or more child nodes. If a node has zero child nodes, it is a leaf and has only device information such as configuration data. If a node has more than one child, the node provides:

- The number of children.
- A pointer to each child.

Root Node Base

The following figure shows an example ROOTNODEBASE structure.

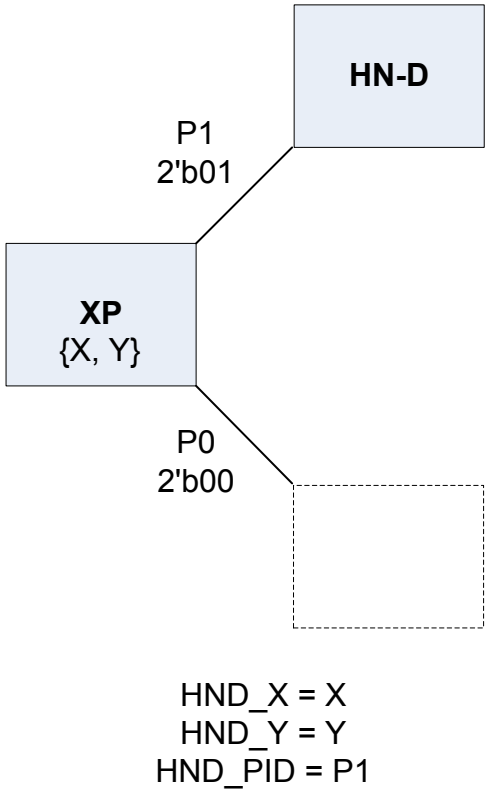


Figure 2-17 Example ROOTNODEBASE pointer

The ROOTNODEBASE structure is defined by three items as shown in the following figure.

ROOT_NODE_BASE:

PERIPHBASE	ROOT NODE POINTER	REGISTER OFFSET

Figure 2-18 ROOTNODEBASE structure

The Register Offset is `14'b0`.

The Root Node Pointer uses 12 bits.

The node ID format is selected based on the largest of the X or Y mesh dimensions, as shown in the following table.

Table 2-4 Node ID mapping

Mesh width in X dimension	Mesh width in Y dimension	Number of bits used to encode X, Y
X <= 4	Y <= 4	2 bits for X, 2 bits for Y
4 < X <= 8	Y <= 8	3 bits for X, 3 bits for Y
X <= 8	4 < Y <= 8	3 bits for X, 3 bits for Y

Refer to *2.4 Node ID mapping* on page 2-51 for more information regarding node ID structure for various mesh dimensions.

The following tables contain the Root Node pointer details for various XID and YID widths.

Table 2-5 12-bit: XID_WIDTH and YID_WIDTH = 2

Bit assignments							
11:10	9	8	7	6	5:2	1	0
`1'b0`	HND_X[1]	HND_X[0]	HND_Y[1]	HND_Y[0]	`1'b0`	HND_PID[1]	HND_PID[0]

Table 2-6 12-bit: XID_WIDTH and YID_WIDTH = 3

Bit assignments								
11	10	9	8	7	6	5:2	1	0
HND_X[2]	HND_X[1]	HND_X[0]	HND_Y[2]	HND_Y[1]	HND_Y[0]	`1'b0`	HND_PID[1]	HND_PID[0]

2.5.2 Configuration register node structure

Read-only registers that are organized into several register blocks are referred to as nodes.

Nodes are aligned on 8-byte boundary (16KB-aligned). There are two required registers:

1. Node info: Identifies product or node-type, and CHI node ID.
2. Child info: Provides child count and offset for the first register containing child node pointers.

Note

Node info and child info are at fixed offsets for ALL nodes.

Optional registers for child pointers use eight bytes per register. A basic node structure is provided in the following figure.

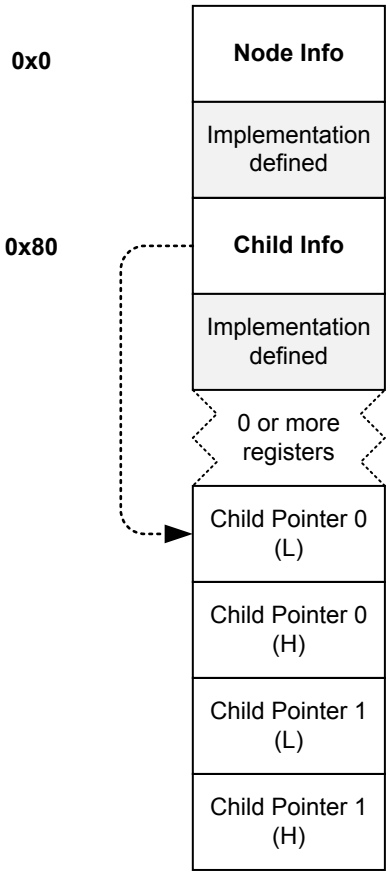


Figure 2-19 Basic node structure with fixed offsets

The node structure detail for child_count indicates the number of children. This value must be zero for a leaf node (no children). This value is the lower 16 bits of child_info and is an unsigned integer. The *child_count* field in **Child Info** register provides number of functional units connected to current unit on next level of discovery process.

The node structure detail for child_ptr_offset is the offset in bytes for child pointers. This value must be zero for a leaf node (no children). This value is the upper 16 bits of child_info and is an unsigned integer. The *child_ptr_offset* field in **Child Info** register provides offset from **Node Info** register address in bytes for **Child Pointer 0** register.

The **Child Info** register with zero value indicates that there is no other units, related to the current one on next level of discovery process.

The following figure provides the node structure detail.

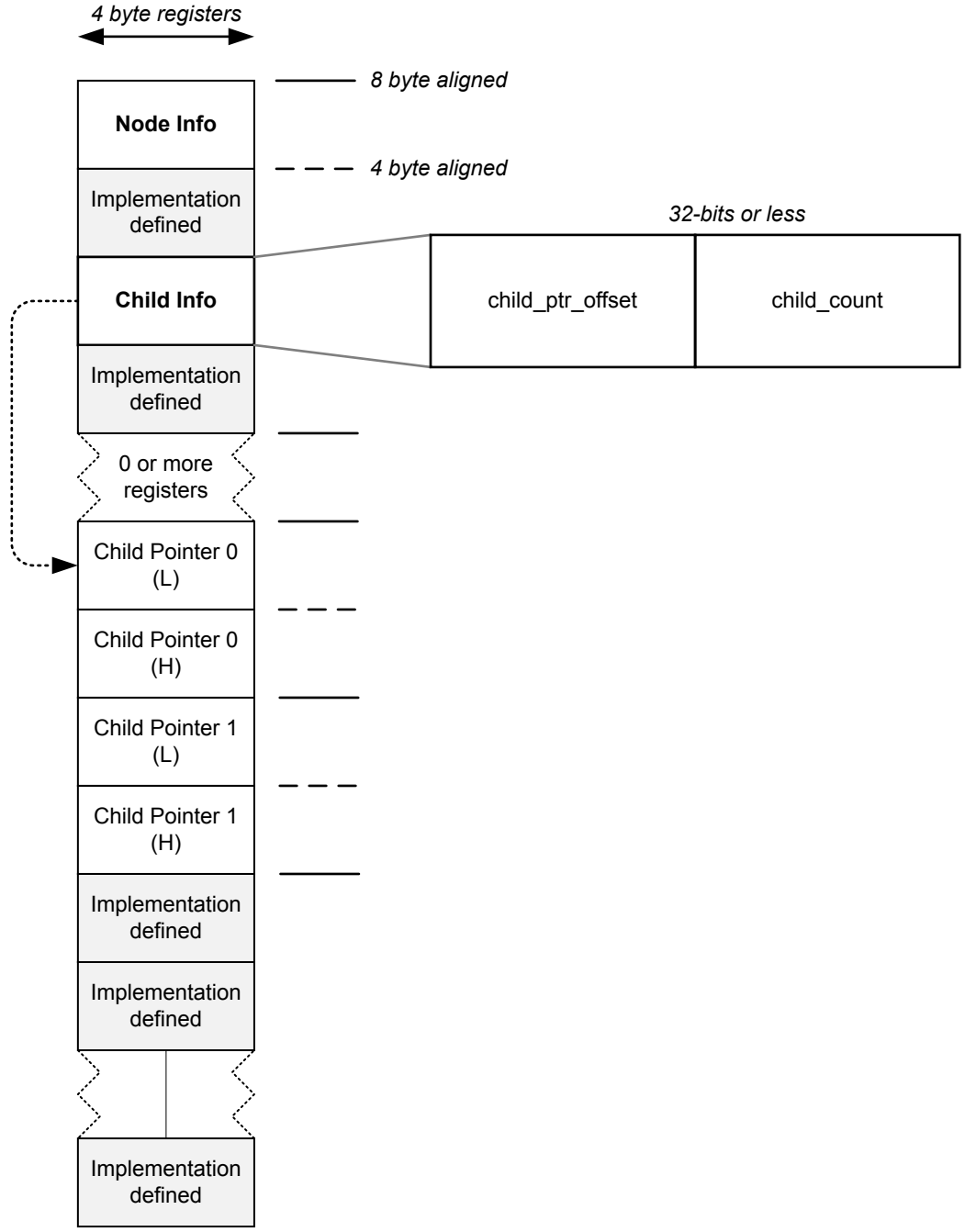


Figure 2-20 Node structure detail

The following table contains Node Info register Node_Type values.

Table 2-7 Node Info register Node_Type values

POR_NODE_INFO_NODE_TYPE	Value
Invalid	16'h0000
DVM	16'h0001
CFG	16'h0002
DTC	16'h0003

Table 2-7 Node Info register Node_Type values (continued)

POR_NODE_INFO_NODE_TYPE	Value
HN-I	16'h0004
HN-F	16'h0005
XP	16'h0006
SBSX	16'h0007
RN-I	16'h000A
RN-D	16'h000D
RN-SAM	16'h000F

The following table contains CML Node Info register Node_Type values.

Table 2-8 CML Node Info register Node_Type values

CML POR_NODE_INFO_NODE_TYPE	Value
CXRA	16'h0100
CXHA	16'h0101
CXLA	16'h0102

2.5.3 Child pointers

There is one child pointer register per child node.

The address of the register containing the first child pointer is computed as:

Base node address (of the current 16KB block) + the `child_ptr_offset` value (from the **child_info** register).

Each subsequent child pointer register is eight bytes higher. See the figure *Figure 2-20 Node structure detail* on page 2-59 for more information.

For example:

- Base node address = `0x4000`
- **Child_ptr_offset** in child info register = `0x100`
- Address of first child pointer register (child pointer 0) = Base node address + child_ptr_offset = `0x4100`
- Address to child pointer 1 = Address of child pointer `0` + `0x8` = `0x4100` + `0x8` = `0x4108`

Child pointers are 32 bits or less and are contained in the low register. The high register is zero. Child pointer contents include:

- The child node address offset from PERIPHBASE (bits 0-27) which is an unsigned integer (positive offset).
- Three reserved bits (bits 28-30).
- An External Child Node indicator (bit 31).

For example:

- Address to 16KB block of the child node = PERIPHBASE + child pointer register [27:0]

The child node address offset relative to PERIPHBASE includes Node Pointer and Register offset, in addition to the other bits, are provided in the following table.

Table 2-9 Child Pointer register

External Child Node	Reserved	Child node address offset relative to PERIPHBASE	
31	30:28	27:14	13:0
1 = External, 0 = Internal	Not used	NODE POINTER [13:0]	REGISTER OFFSET[13:0]

The External Child Node (bit 31) behaves as follows:

- `1'b1`: Indicates that this CHILD POINTER is pointing to a Config Node external to CMN-600.
- `1'b0`: Indicates that this CHILD POINTER is pointing to a Config Node internal to CMN-600.

For CMN-600, external child nodes are only used for RN-SAM and CXLA Config Node. The software performing the discovery can use two pieces of information:

1. The NODE POINTER information (X, Y, port ID (P0 or P1), device ID (D0, D1, D2, or D3)) to determine the CHI NodeID corresponding to the Config child node in question.
2. Once the port (P0 or P1) is determined using the information above, read the corresponding XP register to determine the device type connected to that specific port.
   a. por_mxp_device_port_connect_info_p0
   b. por_mxp_device_port_connect_info_p1

The device type corresponding to that child node will help the discovery s/w determine if the child node is RNF/RN-SAM or CXLA. If the device type is CXRH, CXHA, or CXRA, then the external child node is CXLA as every CXRH, CXHA, or CXRA node has a corresponding external CXLA node. It is the responsibility of the discovery s/w to ensure that the external child node is powered ON before sending any config accesses to it.

The NODE POINTER (bits 27:14) is processed as follows:

- If External Child Node is set to 1, then software can use the information in the NODE POINTER to extract the X dimension, Y dimension, port ID and device ID corresponding to that Child Node.

The REGISTER OFFSET (bits 13:0) are always 0.

Depending on the size of the mesh (X and Y dimensions), CMN-600 supports two different widths for encoding the X and Y dimension. The number of bits needed is selected based on the larger of the X and Y values.

Table 2-10 Mesh size and encoding bits

Mesh width in X dimension	Mesh width in Y dimension	Number of bits used to encode X, Y
X <= 4	Y <= 4	2 bits for X, 2 bits for Y
4 < X <= 8	Y <= 8	3 bits for X, 3 bits for Y
X <= 8	4 < Y <= 8	3 bits for X, 3 bits for Y

For mesh widths using 2 bits each for X,Y encoding, the details of the NODE POINTER structure are provided in the following table.

Table 2-11 Mesh widths using 2 encoding bits

NODE POINTER: XID_WIDTH and YID_WIDTH = 2					
13:10	9	8	7	6	5:0
4'b0	XID[1]	XID[0]	YID[1]	YID[0]	DeviceID

Mapping between NODE POINTER and CMN-600 NodeID for that processor or cluster:

- NodeID[1:0] = DeviceID[3:2]
- NodeID[2] = DeviceID[0]
- NodeID[4:3] = NODE POINTER[7:6]
- NodeID[6:5] =NODE POINTER[9:8]

For mesh widths using 3 bits each for X,Y encoding, the details of the NODE POINTER structure are provided in the following table.

Table 2-12 Mesh widths using 3 encoding bits

NODE POINTER: XID_WIDTH and YID_WIDTH = 3							
13:12	11	10	9	8	7	6	5:0
2’b0	XID[2]	XID[1]	XID[0]	YID[2]	YID[1]	YID[0]	DeviceID

Mapping between NODE POINTER and CMN-600 NodeID for that processor or cluster:

- NodeID[1:0] = DeviceID[3:2]
- NodeID[2] = DeviceID[0]
- NodeID[5:3] = NODE POINTER[8:6]
- NodeID[8:6] = NODE POINTER[11:9]

A sample child pointer design is provided in the following figure.

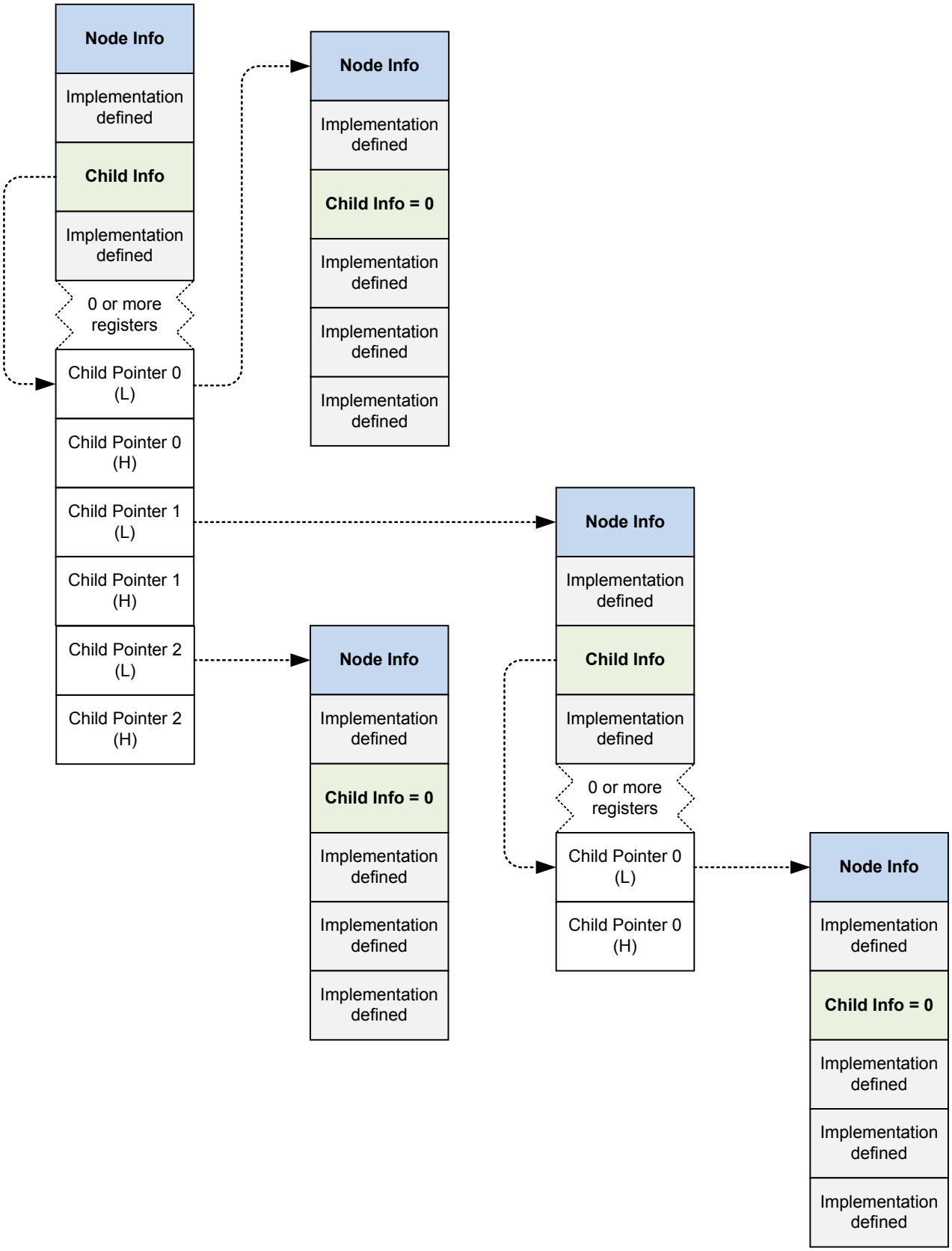


Figure 2-21 Child pointers

2.5.4 Discovery tree structure

This section describes the discovery tree structure used in CMN-600.

The discovery tree structure consists of three levels:

1. Level 1: Root Node: The HN-D containing the Global Configuration Slave
2. Level 2: XP layer
3. Level 3: Leaf layer with one or two devices

The one-time discovery process creates a lookup table containing addresses for all CMN-600 configured devices. A 2×2 mesh configuration example with highlighted discovery tree levels is shown in the following figure.

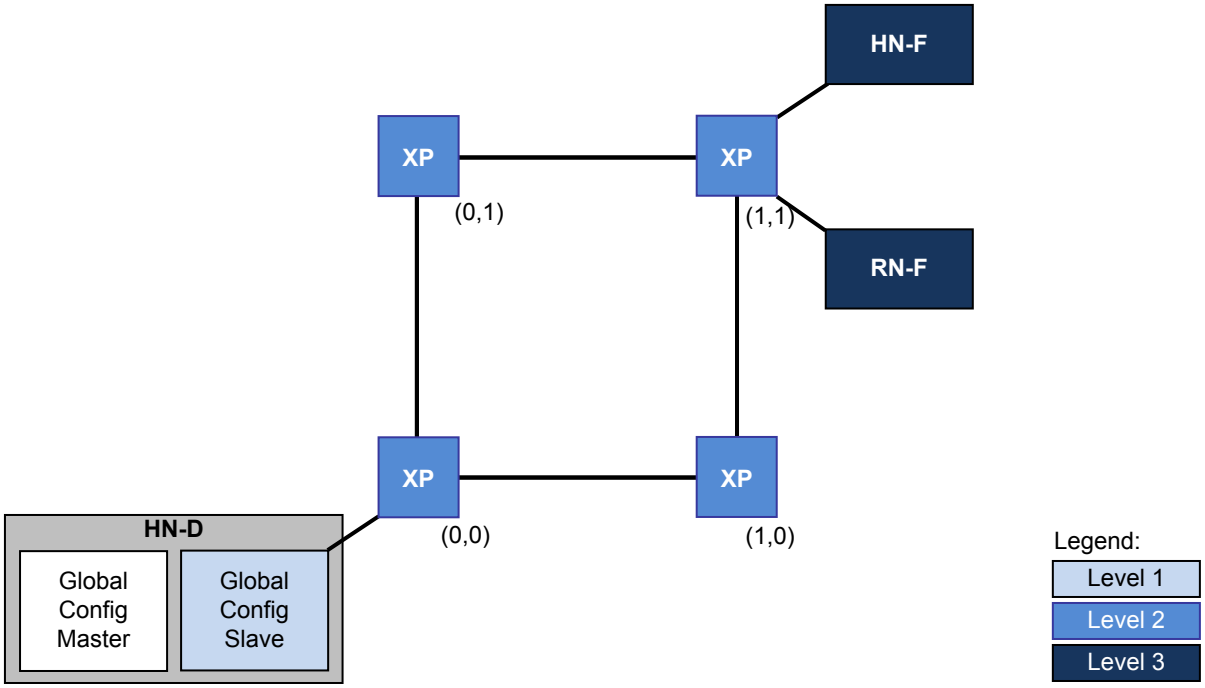


Figure 2-22 2x2 Discovery Tree Example

The discovery tree structure for this 2×2 mesh configuration is shown in the following figure.

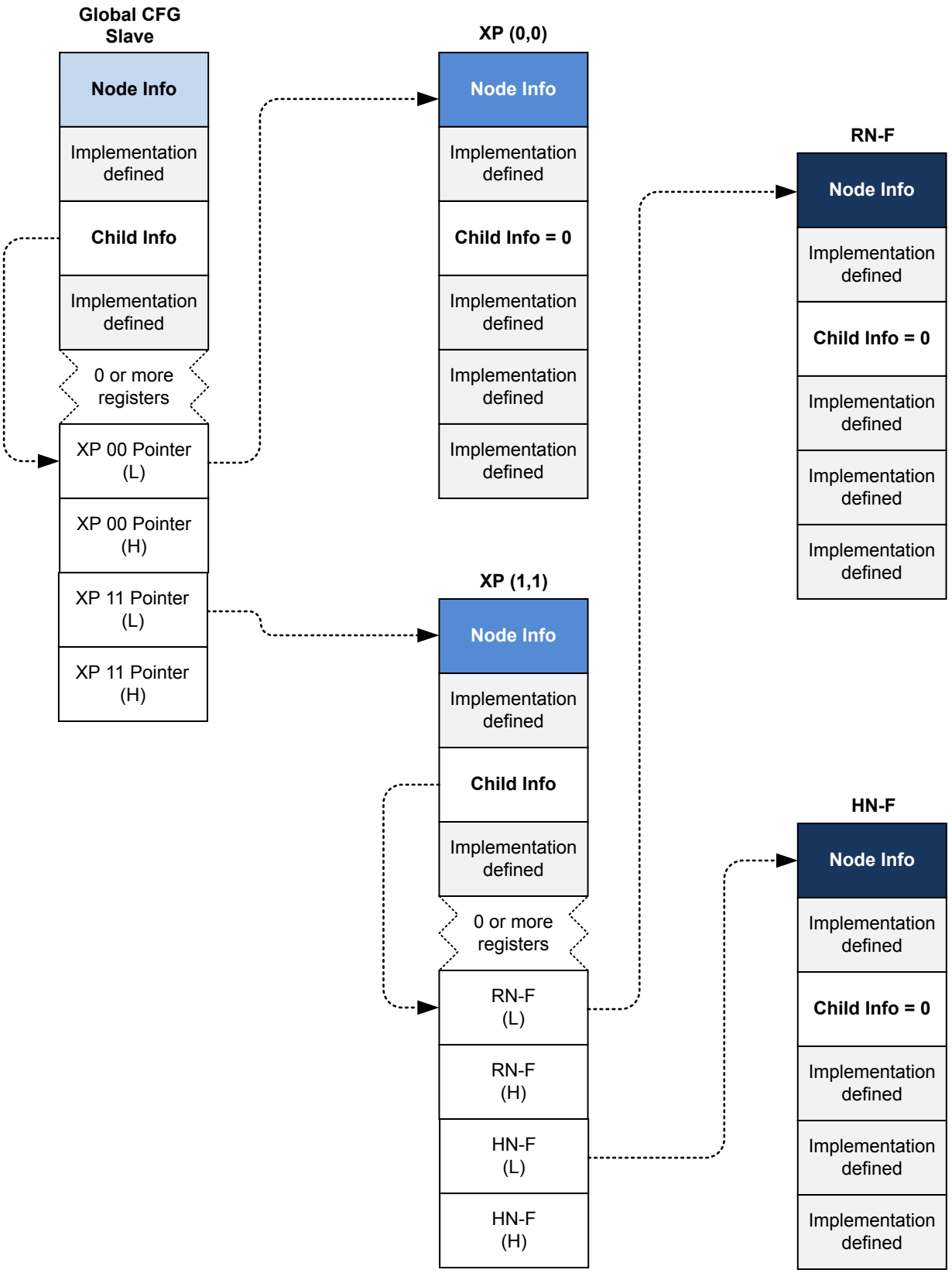


Figure 2-23 2x2 Discovery Tree Structure

2.6 Addressing capabilities

CMN-600 supports a 34-bit, 44-bit, or 48-bit physical address width. This defines the physical address space for which read and write transactions are supported in the interconnect. This is configured using Socrates and results in the PA_WIDTH global parameter in the CMN-600 RTL.

CHI interfaces in CMN-600 support 44-bit and 48-bit address field widths for flits on the REQ channel. This is also configured using Socrates and results in the REQ_ADDR_WIDTH global parameter in the CMN-600 RTL.

The address field width for flits on the SNP channel is derived automatically based on the REQ_ADDR_WIDTH global parameter.

The legal combinations of physical address widths and flit address widths are shown in the following table.

Table 2-13 Legal combinations of physical address and flit address widths

Physical address width	REQ flit address width	SNP flit address width (derived)
34b	44b	41b
34b	48b	45b
44b	44b	41b
44b	48b	45b
48b	48b	45b

2.7 Atomics

CMN-600 supports atomic accesses to both cacheable and non-cacheable memory locations.

This section contains the following subsections:

2.7.1 HN-F

The HN-F completes all CHI atomic requests that it receives, both for cacheable and non-cacheable transactions.

For cacheable transactions, the HN-F completes any appropriate coherent actions and if necessary obtain the targeted cache line from memory. The HN-F then completes the required atomic operation and issues the appropriate response with or without data.

For non-cacheable transactions, the HN-F does not send an atomic request to the SN. As the final PoS/PoC for all memory traffic, the HN-F is able to issue a read to the SN, atomically update the copy of the data in the HN-F, and then write back the result to the SN. This means the SN never receives CHI atomic requests, as the HN-F completely handles the requests.

2.7.2 SN

The SN node (CHI memory controller or SBSX bridge) does not process atomic requests.

2.7.3 HN-I

The HN-I does not complete atomic transactions.

Upon receiving an atomic request, the HN-I generates an appropriate error response to the originating master.

2.7.4 RN-I

RN-I supports atomic transactions in CMN-600 R3 version and is capable of receiving atomics from AXI-5 masters and translate it on CHI before sending it to HN-F, HN-I, or CXRH node.

Atomics and write transactions share the same write tracker for processing in RN-I.

Note

For atomic transactions arriving at RN-I from AXI-5 masters, all write strobes within **AWSIZE** must be set as RN-I do not allow sparse write strobes for atomic transactions.

2.8 Exclusive accesses

CMN-600 supports exclusive accesses to both Shareable and Non-shareable locations as described in the CHI architecture specification.

This section contains the following subsections:

2.8.1 HN-F

The HN-F supports exclusive access on ReadNoSnp, WriteNoSnp, ReadShared, ReadClean, ReadNotSharedDirty, and CleanUnique transactions to any address that maps to the HN-F.

The RN-F generates ReadNoSnp and WriteNoSnp Exclusives for memory locations that are marked Non-cacheable or Device. ReadShared, ReadClean, and CleanUnique exclusives are used for shareable and coherent memory locations. Each HN-F partition includes 64 exclusive monitors for tracking of these transaction types, with each monitor capable of acting as both a PoC monitor and System monitor, as defined by the AMBA 5 CHI protocol.

Only 64 unique logical threads, designated by a unique combination of SrcID and LPID, can concurrently access the HN-F exclusive monitors.

2.8.2 HN-I

HN-Is support exclusive access on ReadNoSnp and WriteNoSnp transactions to any address that maps to an HN-I.

Each HN-I partition includes 32 exclusive monitors as defined in the AMBA 5 CHI protocol for tracking of these transaction types. Only 32 unique logical threads, either processor or device threads, designated by a unique combination of SrcID and LPID, can concurrently access the HN-I system exclusive monitors.

All exclusives targeting the HN-I are terminated at the HN-I and are not propagated downstream, regardless of the value of the HN-I PoS Control Register and Auxiliary Control Register.

2.8.3 CML Exclusive Support

In the SMP Mode, CMN-600 CML will support remote exclusive accesses from RN-Fs.

Constraints include:

1. Remote exclusive accesses from an RN-I or RN-D is not supported.
2. Remote exclusive accesses targeting with an HN-I or HN-D is not supported.

Support for remote exclusive accesses in *CCIX Gateway* (CXG) blocks include these constraints:

1. CXRA in local CXG block will pass Excl and LPID fields of incoming CHIC request on CCIX request message USER (Ext) field.
2. CXHA in the remote CCIX gateway (CXG) block will extract these bits from CCIX request message USER (Ext) field and send them on respective CHIC Excl and LPID fields. CXHA will set the source type as RN-F based on its RAID to LDID register.
3. Exclusive OK (EXOK) response is sent as 2'b01 on CCIX RespErr field.

——— **Note** ———

2'b01 is a reserved encoding in RespErr field and this field is sent as an CCIX extension (Ext6).

———————————

HN-F handling of exclusives:

- For exclusive access from remote RN-Fs, the HN-F uses the existing monitors and will monitor the LDID and LPID of the incoming request.

2.8.4 RN-I, RN-D

RN-I supports up to two active exclusive threads at any given AXI port and provides a per port 11-bit mask to extract the bit from AxID which can be used to differentiate the exclusive threads.

The 11-bit mask `por_{rni,rnd}_s<X>_port_control` can be found in RN-I, RN-D respective AXI port control registers.

2.9 Processor events

CMN-600 supports communicating processor events to all processors in the system.

Refer to the processor event interface signals described in *A.14 Processor event interface signals on page Appx-A-1185*.

When a processor generates an output event triggered by an SEV instruction, it is broadcast to all processors in the system. Similarly, anytime an exclusive monitor within HN-F or HN-I is cleared, an output event is broadcast to all processors in the system.

The logical operator OR is used to combine the EVENT signals, then the result is broadcast to the processors.

2.10 Quality of Service

CMN-600 includes end-to-end QoS capabilities which support latency and bandwidth requirements for different types of devices.

The QoS device classes are:

Devices with bounded latency requirements

These are primarily real-time or isochronous devices that require some or all of their transactions be complete within a specific time period to meet overall system requirements. These devices are typically highly latency-tolerant within the bounds of their maximum latency requirement. Examples of this class of device include networking I/O devices and display devices.

Latency-sensitive devices

These are devices whose performance is highly impacted by the response latency incurred by their transactions. Processors are traditionally highly latency-sensitive devices, although a processor can also be a bandwidth-sensitive device depending on its workload.

Bandwidth-sensitive devices

These are devices that have a minimum bandwidth requirement to meet system requirements. An example of this class of device is a video codec engine, which requires a minimum bandwidth to sustain real-time video encode and decode throughput.

Bandwidth-hungry devices

These are devices that have significant bandwidth requirements and can use as much system bandwidth as is made available, to the limits of the system. These devices determine the overall scalability limits of a system, with the devices and system scaling until all available bandwidth is consumed.

Note

A device may be classified into one or more of these classes, depending on its workload requirements.

Support for these different types of devices and their resulting traffic is included in the AMBA 5 CHI protocol and in the entirety of CMN-600 microarchitecture. Each component in CMN-600 contributes to the overall QoS microarchitecture.

This section contains the following subsections:

- *2.10.1 Architectural QoS support* on page 2-71.
- *2.10.2 Microarchitectural QoS support* on page 2-71.
- *2.10.3 QoS configuration* on page 2-76.

2.10.1 Architectural QoS support

The AMBA 5 CHI protocol includes a 4-bit *QoS Priority Value* (QPV) with all message flits.

The QPV of the originating message must propagate for all messages in a transaction. The QPV is defined as higher values being higher priority and lower values being lower priority. All CMN-600 components use the QPV to provide prioritized arbitration and to prevent head-of-line-blocking based on the QPV.

2.10.2 Microarchitectural QoS support

The QPV of RN requests must be modulated depending on how well or poorly their respective QoS requirements are met.

QoS regulators

Although the QoS-modulation capability can be integrated into the RN, CMN-600 enables system designers to include non-QoS-aware devices in the CMN-600 system, but still have these devices meet the QoS-modulation requirements of the CMN-600 QoS microarchitecture.

CMN-600 includes inline QoS regulators that perform QoS modulation without requiring any QoS-awareness by the requesting device. A QoS regulator introduces an interstitial layer between an RN and the interconnect that monitors whether the bandwidth and latency requirements of the RN are being met. It also performs in-line replacement of the RN-provided QPV field as required, adjusting upwards to increase priority or downwards to reduce priority in the system.

The QoS regulators are present at all entry points into CMN-600:

- For AMBA 5 CHI ports, the regulator is present in the XP.
- For ACE-Lite/AXI4 slave interfaces, the regulator is present at the ACE-Lite/AXI4 side of the protocol bridge.

CMN-600 QoS regulators have three operating modes, controlled through memory-mapped configuration registers:

1. Pass-through.
2. Programmed QoS value.
3. Regulation.

QoS regulator operation

The values of the base QPV, **AxQOS** for ACE-Lite/AXI interfaces or RXREQFLIT.QOS for AMBA 5 CHI ports are inputs to the QoS subblock.

When latency regulation or period regulation is enabled, these values are replaced by the values generated by the regulators. For an RN-F, a single QoS regulator monitors CHI transactions that return data to the RN-F such as reads, atomics and snoop stash responses. The regulated QPV is applied to all CHI requests from that RN-F. For an RN-I or RN-D, separate QoS regulators exist for AR and AW channels.

The QoS regulators can operate in either latency regulation mode or period regulation mode. The registers to configure the QoS regulators exist in each RN-I, RN-D, and XP.

Latency regulation mode

When configured for latency regulation, the QoS regulator increases the QPV whenever actual transaction latency is higher than the target, and decreases the QPV when it is lower:

- For every cycle that the latency of a transaction is more than the target latency, the QPV is increased by a fractional amount, determined by the scale factor K_i.
- For every cycle that the latency of a transaction is less than the target latency, the QPV is decreased by the same fractional amount, determined by the scale factor K_i.

The QoS Latency Target register specifies the target transaction latency in cycles.

The QoS Latency Scale register specifies the scale factor K_i. It is coded in powers of two, so that a programmed value of `0x0` = 2^{-3} and a programmed value of `0x7` = 2^{-10}.

The QoS regulator can be programmed to operate in latency regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to 1.
- Set the lat_en bit to 1.
- Set the reg_mode bit to 0.
- Set the pqv_mode bit to 0.

Period regulation mode for bandwidth regulation

When configured for period regulation, the QoS regulator increases the QPV whenever the period between transactions is larger than the target, and decreases the QPV when it is lower:

- For every cycle that the period between transactions (as measured at dispatch time) is more than the target period, the QPV is increased by a fractional amount, the scale factor K_i.
- For every cycle that the period between transactions is less than the target period, the QPV is decreased by the same fractional amount, the scale factor K_i.

The QoS Latency Target register specifies the target period in cycles.

The QoS Latency Scale register specifies the scale factor K_i. It is coded in powers of two, so that a programmed value of `0x0` = 2^{-3} and a programmed value of `0x7` = 2^{-10}.

The QoS regulator can be programmed to operate in period regulation mode by programming the following bits in the QoS Control register:

- Set the qos_override_en bit to 1.
- Set the lat_en bit to 1.
- Set the reg_mode bit to 1.

There are two modes of period regulation:

- In normal mode, the QPV neither increases nor decreases when there are zero outstanding transactions.
- In quiesce high mode, the QPV increases by a fractional amount, determined by the scale factor K_i, in every cycle where there are zero outstanding transactions.

The mode of period regulation can be selected by programming the pqv_mode bit in the QoS Control register.

RN-I/RN-D bridge QoS support

In addition to the QoS regulators, the RN-I/RN-D bridge provides QoS-aware arbitration mechanisms.

To simplify arbitration logic, all transactions are split into two QoS Priority Classes (QPCs), high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.

Port multiplexer arbitration

An RN-I/RN-D bridge includes three ACE-Lite/ACE-Lite+DVM ports. The RN-I/RN-D bridge selects between these ports for allocation into its transaction tracker, which makes the allocated transaction a candidate for issuing to a home node. The port multiplexer is arbitrated using the following strategy:

- High QPC first, then the low QPC.
- Round-robin arbitration among the AMBA ports within a QPC.

Tracker allocation

When transactions are allocated into the tracker, they are scheduled for issuance to a home node based on QPC, following the same strategy as port mux arbitration.

- High QPC first, then the low QPC.
- Round-robin arbitration in a QPC among the issuable transactions.

HN-F QoS support

The HN-F is a key shared system resource used for system caching and for communication with the memory controller for external memory access.

The HN-F includes the following QoS support mechanisms:

QoS decoding in HN-F

The HN-F interprets the 4-bit QPV at a coarser granularity, as the following table shows.

Table 2-14 QoS classes in HN-F

QoS value range	QoS Class	Class mnemonic	Priority
15	HighHigh	HH	Highest
14-12	High	H	High
11-8	Med	M	Medium
7-0	Low	L	Low

QoS class and POCQ resource availability

The HN-F includes a 32-entry or 64-entry structure, the *Point-of-Coherency Queue* (POCQ), from which all transaction ordering and scheduling is performed. The POCQ buffers are shared resources for all QoS classes, with one entry being reserved for internal use. The higher the QoS class, the higher the occupancy availability. As the following figure shows, the POCQ is partitioned so that higher priority requests are able to use a larger percentage of the POCQ buffering, ensuring bandwidth and latency requirements of higher priority transactions are met.

The number of entries available for use by each QoS class is defined in the HN-F QoS Reservation register, and is software-programmable.

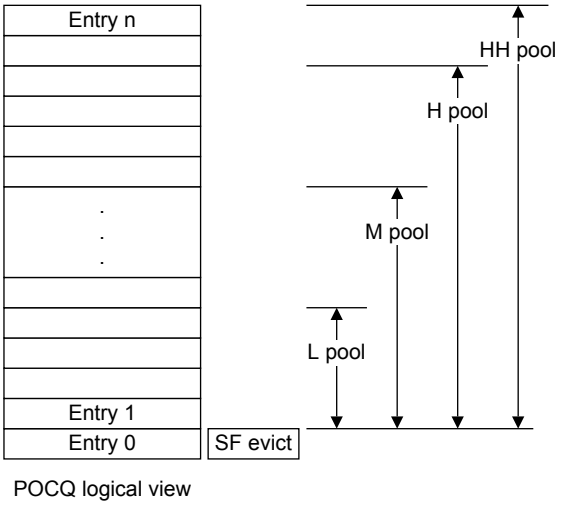


Figure 2-24 POCQ availability and QoS classes

The QoS pools are:

hh_pool Available for HH class.

h_pool Available for H class and HH class.

m_pool Available for M class, H class, and HH class.

l_pool Available for all classes.

seq SF evictions only.

POCQ allocation policies

Allocation into POCQ entries can follow either of two paths:

- Immediate allocation on receipt of the initial request by the HN-F
- Allocation of a retried request after a protocol-layer retry of the initial request

The first case is the expected common case and is always the case in a reasonably uncongested system. If the POCQ has an available buffer corresponding to the QoS class of an arriving request, that request allocates in the POCQ.

However, in case of a congested system in which a POCQ entry corresponding to the QoS class of an arriving request is not available at the time of arrival, the AMBA 5 CHI protocol requires that the arriving request receive a protocol-layer retry. The transaction flow in this case is as follows:

1. A request arrives at a congested HN-F.
2. The HN-F does not have an available POCQ buffer corresponding to the QoS class of the new transaction.
3. The HN-F increments a credit counter for the specific QoS class of the specific RN and sends a RetryAck response to the RN.
4. On receiving a RetryAck response, the RN subsequently waits for a follow-on PCreditGrant response.
5. 5. When a POCQ entry becomes available, the HN-F reserves that buffer for the highest-priority RN with a non-zero credit-counter and sends a PCreditGrant response to the selected RN.
6. On receiving a PCreditGrant, the RN re-issues the transaction, which is guaranteed to be allocated into the HN-F.

This mechanism serves as prioritized arbitration based on QoS values for requests sent to the HN-F.

POCQ scheduler policies

When transactions are allocated into the POCQ, they are scheduled for issuance based on the QPV as follows, in descending order of priority:

- Starved transactions. These are lower-priority transactions that have made no forward progress for a number of cycles specified in the respective fields in the RN Starvation Register.
- Highest QoS class.
- Round-robin arbitration within a QoS class among the issuable transactions.

HN-I/SBSX QoS support

The HN-I bridge provides QoS-aware arbitration mechanisms for static grants and AMBA requests.

To simplify arbitration logic, all transactions are split into two QPCs, high and low. QoS-15 transactions make up the high class. All other transactions are considered to be in the low class.

——— **Note** ———

SBSX QoS support is identical to that of the HN-I.

———————————

Dynamic credit tracker allocation

Requests allocate into the tracker until it is full, after which requests are then retried and the HN-I increments a credit counter for the affected RNs in an internal retry bank.

When a tracker entry is cleared, the HN-I checks the retry bank for any retried transactions. If any are present, the newly available tracker entry is reserved and a static credit grant is sent to an RN chosen using the following algorithm:

- Choose an RN marked as high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Scheduling to AMBA interface

When transactions are allocated into the tracker, they are scheduled for issue on the AMBA interface based on QPC following a similar strategy to static credit allocation:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

Write data buffers are also allocated based on QPC class. For write requests that are ready to issue:

- Choose high QPC first, then the low QPC.
- Use round-robin arbitration within a QPC.

2.10.3 QoS configuration

This example configuration demonstrates the QoS mechanisms and their contribution to the overall QoS solution.

It is the responsibility of the SoC designer and system programmer to configure CMN-600 to meet the specific requirements of the system and expected workloads.

System operating conditions

The example QoS configuration assumes the following:

- Four processor clusters:
  - Bimodal operation. A processor cluster is latency-sensitive when bandwidth per cluster is ≤ 2GB/s, and bandwidth-hungry, and therefore latency-tolerant, when bandwidth per cluster is > 2GB/s.
  - 16 outstanding combined reads and writes.
  - 10GB/s maximum bandwidth per cluster.
  - 25GB/s maximum aggregate bandwidth across all processor clusters.
- Four peripheral devices with bounded latency requirements:
  - Each device is the sole device connected to ACE-Lite interface 0 on four different RN-I bridges.
  - 1 microsecond maximum latency requirement.
  - 4GB/s maximum bandwidth per device.
  - 210GB/s maximum aggregate bandwidth across all devices.
- 14 peripheral bandwidth-hungry devices:
  - Connected to all remaining RN-I ACE-Lite interfaces.
  - 12GB/s read or write bandwidth per device, with a combined maximum of 24GB/s.
  - 60GB/s maximum aggregate bandwidth across all devices.
- All devices can be concurrently active.
- 80GB/s maximum aggregate bandwidth across all devices.

HN-F QoS classes

Refer to *Table 2-14 QoS classes in HN-F* on page 2-74 for the QoS ranges and class values in HN-F.

QoS regulator settings

To meet the bandwidth/latency requirements of the system configuration described, CMN-600 QoS regulators can be configured with the settings as described in the following table.

Table 2-15 QoS regulation settings

Device	Regulation type	Regulation parameter	QoS range	QoS scale
Processor	Latency	60ns max latency	11-13	8-9
Real-time peripheral	Override (constant value)	Constant	15	n/a
High-bandwidth peripheral	Override (constant value)	Constant	8	n/a

The latency specification for real-time peripherals must be sufficiently far below the maximum real-time constraint to allow the control loop in the QoS regulator to adjust based on achieved latency, without violating the maximum latency requirement.

To meet the bandwidth and latency requirements of the system configuration described, HN-F QoS reservation values can be configured (based on 32-entry POCQ with one entry for SF back invalidations) as summarized in the following table.

Table 2-16 QoS class and reservation value settings

QoS class	QoS reservation value
Highhigh	31
High	30
Medium	15
Low	5

These settings enable the following system functionality:

- Real-time devices are QPV-15, ensuring their transactions meet their bounded latency requirements.
- The processor QPV is higher than the bandwidth-hungry devices, second only to the real-time devices, and therefore generally achieves minimum latency, except in the event of high-bandwidth real-time traffic.
- Real-time devices have all of the HN-F POCQ buffering available to them, to prevent bandwidth limitations from impacting achieved latency.
- Real-time devices always have buffering available to them throughout the entirety of CMN-600 preventing head-of-line-blocking from lower-priority or higher-latency transactions.

2.11 Barriers

Barriers are deprecated in CHI.B. All masters (fully coherent and I/O coherent) must handle barriers at the source.

When memory barrier ordering or completion guarantees are required, masters must wait for the responses from all required previous transactions that are issued into the interconnect. No barrier requests can be issued into the interconnect.

All requesting devices that are attached to an interconnect must have a configuration option or strap that prevents issuing of any barriers. If a barrier is issued into the interconnect, the results are unpredictable.

Note

The DVM_SYNC command, the DVM synchronization that might be initiated by an Arm DSB instruction, is sent to the DVM block and executes appropriately.

For more information about barriers, see the *Arm® AMBA® 5 CHI Architecture Specification* and the *Arm® AMBA® AXI and ACE Protocol Specification*.

2.12 DVM messages

If an RN-F supports *Distributed Virtual Memory* (DVM) messages, it can send DVM requests and receive DVM snoops.

A DVM message from an RN-F is sent to the HN-D. Upon receiving the DVM message, the HN-D:

- Forwards the DVM message as a snoop to the participating RNs. To do this, the HN-D uses a static list to replace the DVM Domain Control register used with legacy products.
- Collects the individual snoop responses.
- Sends a single response back to the RN-F that originated the DVM message transaction.

The SYSCO REQ/ACK mechanism provides proxy snoop responses in scenarios when the RN is powered down. Refer to *2.30 RN entry to and exit from Snoop and DVM domains* on page 2-163 for more SYSCO REQ/ACK information.

Note

- An RN that issues DVM messages must also be able to receive DVM messages. If this requirement is violated, the system must not rely on the DVM message causing any DVM snoops.
- An RN-F can issue only one outstanding DVMOp (Sync).

For more information about DVM messages, see the *Arm® AMBA® 5 CHI Architecture Specification*.

2.13 PCIe integration

CMN-600 supports integration of a PCIe *Root Complex* (RC) or *EndPoint* (EP).

This section contains the following subsections:

2.13.1 CMN-600 PCIe master and slave restrictions and requirements

This section describes PCIe master and slave restrictions and requirements.

The restrictions and requirements are:

- Peer-to-peer PCIe traffic, that is, one PCIe EP talking to another PCIe EP, must not pass through the CMN-600. Requests from the PCIe master can only target memory through the HN-F, CMN-600 configuration space, or an I/O slave device downstream of the HN-I. These requests must not target any PCIe slave downstream of the HN-I.
- The PCIe master must not create same-**AWID** dependency between *Non-Posted Write* (NPR-Wr) and *Posted Write* (P-Wr) transactions sent on the RN-I AXI/ACE-Lite slave port.
- The flow control requirements are:

  CMN-600 to PCIe slave

  The PCIe slave must be able to sink at least one NPR-Wr from the CMN-600, sent on the HN-I AXI/ACE-Lite master port. This requirement guarantees that the HN-I AW channel remains unblocked, which enables P-Wrs from PCIe master targeting the I/O slave device to make progress, as required by the PCIe ordering rules.

  PCIe master to CMN-600

  If a *System Memory Management Unit* (SMMU) is in the path between the PCIe master interface and the RN-I slave interface, there are two possible options:

  — *Non-Posted Read*s (NPR-Rds) from the PCIe master must not target the HN-I.

  — Use a separate master interface port in the SMMU for page table walks (TCU in MMU-500 and beyond) and connect this port to a different RN-I which does not send any requests to the HN-I. None of the masters connected to this RN-I can talk to the HN-I.

Note

This option is only available with the MMU-500 Memory Management Unit and beyond.

2.13.2 CMN-600 System requirements

This section describes system requirements.

The system requirements are as follows:

- All non-PCIe I/O slave devices must complete all writes without creating any dependency on a transaction in the PCIe subsystem.
- All non-PCIe I/O masters connected to the same RN-I as a PCIe master, if any, must not send any transactions which target or apply to I/O slave devices downstream of the HN-I.
- If an SMMU is placed in the path between the PCIe master interface and the RN-I slave interface, table-walk requests from the SMMU can only be sent to memory through the HN-F.
- Interrupt translation table-walk requests from GIC-ITS can only be sent to memory through the HN-F.

2.13.3 RN-I and HN-I programming sequence

The RN-I and HN-I must be programmed as described in this section to ensure proper PCIe functionality.

The following programming must be completed before any non-configuration access to the HN-I or RN-I.

RN-I programming

1. If there is a PCIe RC attached to an RN-I, set **por_rni_cfg_ctl.pcie_mstr_present** to indicate that one or more PCIe masters are present upstream.

HN-I programming

1. Entire PCIe configuration space of an RC is required to be mapped to a single HN-I address region. HN-I has a SAM that can be configured for up to three address regions. Address space not configured into these three regions is considered the default address region. To achieve this, program the HN-I SAM Address Region registers (**por_hni_sam_addrregion{0,1,2,3}_cfg**) such that the PCIe configuration space falls under one of the four address regions. Please refer to *2.22 HN-I SAM* on page 2-124 for more details on HN-I SAM programming.
2. For Address Region X in which PCIe configuration space is mapped above, set one of the following bits using **por_hni_sam_addrregionX_cfg**.
   - If PCIe configuration space is marked as Arm memory type of Device-nGnRnE, set **ser_devne_wr**. If this bit is set, HN-I serializes all Device-nGnRnE writes to Address Region X, and does not send any other write requests with the same AWID as an outstanding Device-nGnRnE write.
   - If PCIe configuration space cannot be marked as Arm memory type of Device-nGnRnE, set **ser_all_wr**. If this bit is set, HN-I serializes all writes targeting Address Region X.
3. For Address Region Y in which PCIe EP memory space (posted traffic) is programmed, clear **por_hni_sam_addrregionY_cfg.pos_early_wr_comp_en**. If this bit is cleared, HN-I does not give early write completions for any write requests targeting Address Region Y.

Note

X or Y can be any of the four address regions (0, 1, 2, or 3).

2.14 Error handling

The CMN-600 RAS features are implemented as set of of distributed logging and reporting registers and a central interrupt handling unit. The distributed logging and reporting registers are associated with devices that can detect errors: XP, HN-I, HN-F, SBSX, and CXHA. The central interrupt handling logic is located in the HN-D.

Each device that can detect errors logs the error in local registers and sends error information to the central interrupt handling logic in the HN-D. The HN-D contains four error groups, a secure and non-secure group for error and fault type errors. Each is represented in an *ERRor Group Status Register* (ERRGSR).

- **por_cfgm_errgrs0 - por_cfgm_errgrs4 - error group, secure**
- **por_cfgm_errgrs5 - por_cfgm_errgrs9 - fault group, secure**
- **por_cfgm_errgrs0_NS - por_cfgm_errgrs4_NS - error group, non secure**
- **por_cfgm_errgrs5_NS - por_cfgm_errgrs9_NS - fault group, non secure**

The following figure shows the four error groups, and the four respective interrupt request signals, with XP connections highlighted. The HN-I, HN-F, SBSX, and CXHA use the same input/output structure.

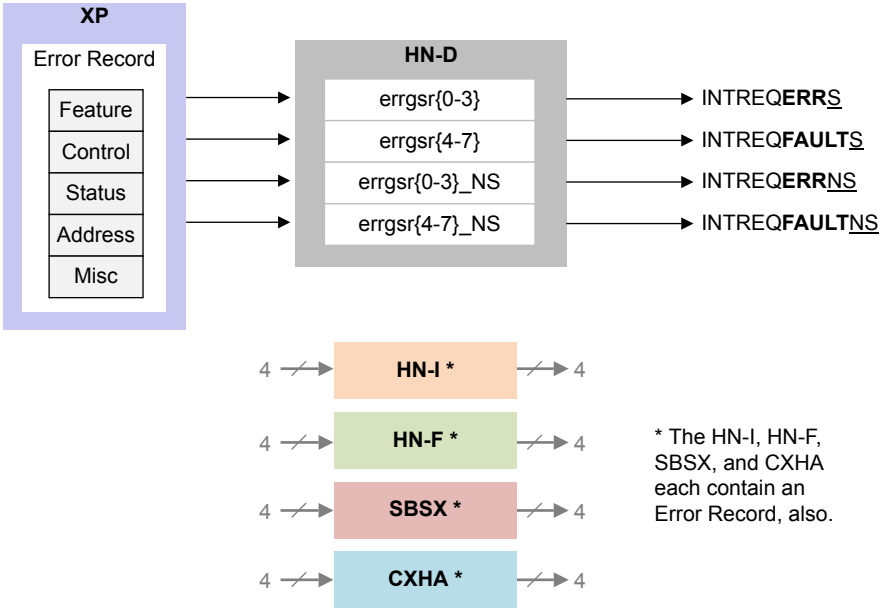


Figure 2-25 Error top-level diagram

Each **errgsr** register is partitioned by device type, with a 64-bit vector representing each device instance's logical ID, as shown in the following figure.

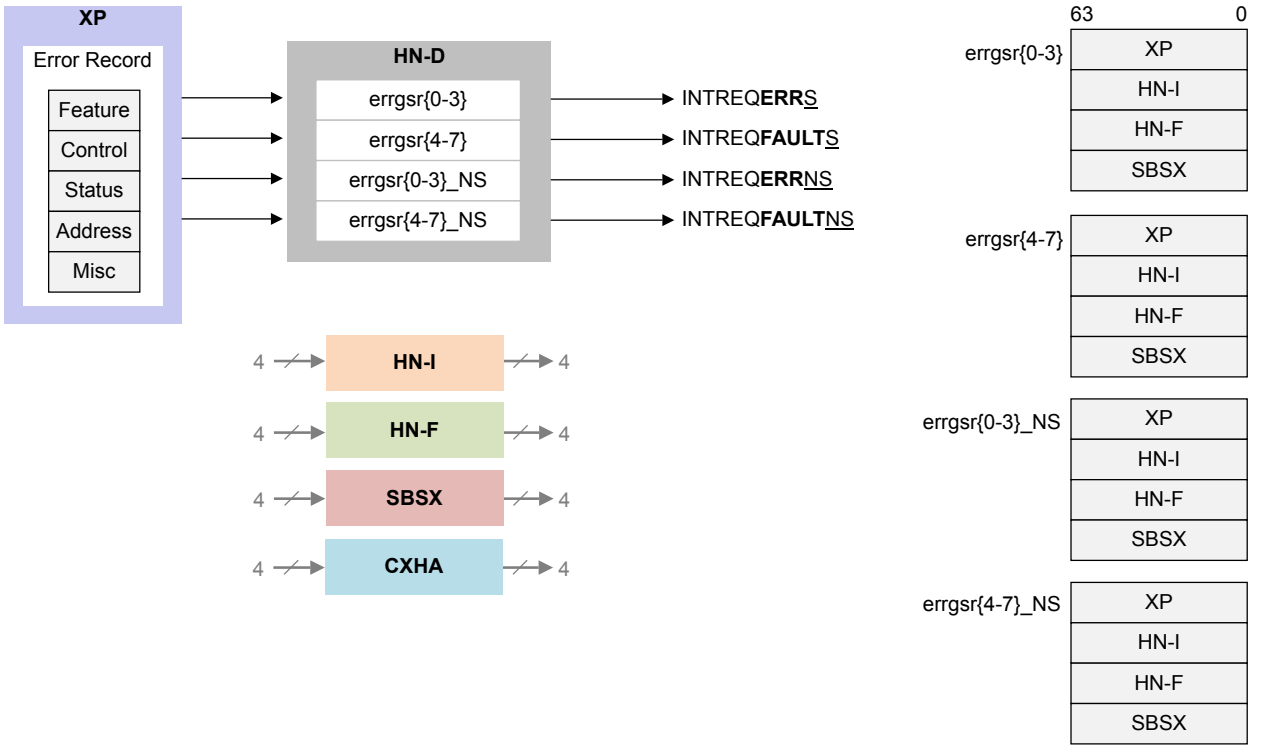


Figure 2-26 256-bit error handling structure

Each device that can detect errors has five Error Record registers that contain the error type, along with other information such as the address and opcode. Error types include *Corrected Error* (CE), *Deferred Error* (DE), and *Uncorrected Error* (UE).

Refer to *2.14.1 Error types* on page 2-85 for more information on error types.

See also *3.3 Register descriptions* on page 3-194 for register details.

Error interrupt handler flow example

The following sequence of events and figure describe the process for determining the error source and type of an HN-I generating an interrupt request:

1. The HN-D generates an interrupt for one of the five error group types.
2. The error group indicates the error source device type, which can be:
   - XP.
   - HN-I (used in this example).
   - HN-F.
   - SBSX.
   - CXHA.
3. The bit location within the error group indicates the logical ID of that device type. In this case, it reveals an HN-I error, the HN-I Error Record Status block for this example.
4. The Status block of the Error Record for the specific XP, HN-I, HN-F, SBSX, or CXHA reveals the type of error.
5. The Address and Misc blocks of the Error Record provide further details regarding error root cause, in this case a Corrected Error.
6. The Valid bit is also asserted.
7. To clear the asserted interrupt on the pin, the valid bit of the error status has to be cleared.

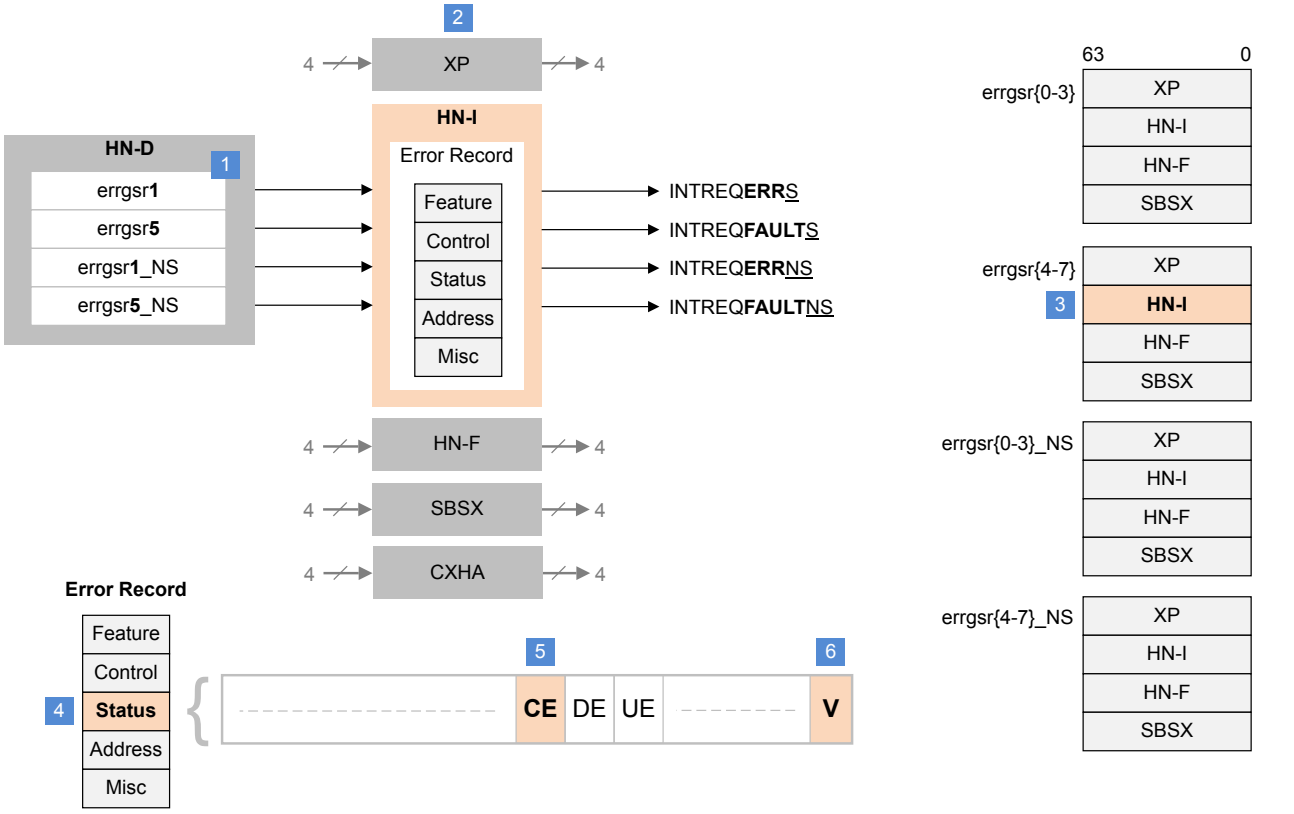


Figure 2-27 Error interrupt handler flow example

This section contains the following subsections:

2.14.1 Error types

CMN-600 supports several error types.

The supported errors are:

- *Corrected Error* (CE).
- *Deferred Error* (DE).
- *Uncorrected Error* (UE).

——— **Note** ———

CEs, DEs, and UEs can occur simultaneously.

———————————

There may be cases when an error occurs and sets the status register, however, the interrupt reporting is not enabled. For other cases where the interrupt asserts, the interrupt request is generated immediately when enabled. Otherwise, any interrupt is cleared if interrupt reporting is disabled and the error remains logged with UE, DE, and CE.

——— **Note** ———

If both **errctlr.UI** (uncorrected interrupt) and **errctlr.FI** (fault interrupt) are set and an uncorrected error occurs, both fault and error interrupts are delivered from CMN-600.

———————————

Correctable errors

These errors can be corrected using *Error Correction Code* (ECC) or other methods. They include:

- A single-bit ECC error.
- An error that is recovered by replaying the transaction in the pipeline.

The system handles these errors as follows:

1. Detects the error and increments **errmisc.CEC** counter. Sets **errstatus.AV** and **errstatus.MV**. Logs the attributes in the **erraddr** and **errmisc** registers.
2. If CEC counter overflowed, the system updates **errstatus.V** and **errstatus.CE**. Sets **errmisc.CECOF**.
3. Masks signaling of the error to the RAS control block using **errctlr.CFI**.
4. If there are multiple CEC overflows, then the system sets **errstatus.OF**.

Deferred errors

These are UEs detected in one node of CMN-600, but the data is not used within the same node, and poison bits are set for the data. The errors can be either fatal or non-fatal errors as described in this section. These errors are not correctable, but the system can operate for a period of time without being corrupted. These errors can be contained and the system might be able to recover using software means. They include:

- A data double bit ECC error in the SLC Data RAM.
- Datacheck error detected in SLC.

The system handles these errors as follows:

1. Logs the error information in the applicable **errstatus**, **erraddr**, and **errmisc** registers.
2. Sets **errstatus.V** and **errstatus.DE**.
3. Masks signaling of the error to the RAS control block using **errctlr.FI** and **errctlr.UI**.
4. If there are multiple DEs, then the system sets **errstatus.OF**.

Uncorrectable fatal errors

These are errors in the control logic at a node. Continuing operation might corrupt the system beyond recovery. They include:

- A double-bit ECC error in SLC tag.
- Flit parity error.
- *Non-Data Error* (NDE) in a response packet.

The system handles these errors as follows:

1. Logs the error information in the applicable **errstatus**, **erraddr**, and **errmisc** registers.
2. Sets **errstatus.V** and **errstatus.UE**.
3. Masks signaling of the error to the RAS control block using **errctlr.UI**.
4. If there are multiple UEs, then the system sets **errstatus.OF**.

A component may not respond to further messages after an error is signaled. In this case, for the error handling routine to be successful, the component must still respond to configuration access requests from the configuration bus.

CMN-600 follows the Arm *Reliability, Availability, and Serviceability* (RAS) Specification for mapping of the different error types to the interrupt. The following table summarizes the mapping of various error types.

Table 2-17 Mapping of various error types

Interrupt types vs error types	UE	DE	CE
Fault handling interrupt	Yes (if **errctlr.FI**=1)	Yes (if **errctlr.FI**=1)	Yes (if **errctlr.CFI**=1)
Error recovery interrupt	Yes (if **errctlr.UI**=1)	No	No

2.14.2 Error detection and deferred error values

For XP, the default values of *Error Detection* (ED) and DE depend on build time parameters.

Only the HN-F has CE counters implemented in the **errmisc** register. The default values of **UI**, **FI**, and **CFI** are `2'b10`, which enables control for the interrupt generation. The following table contains various values of ED and DE for XP.

Table 2-18 Default values of ED and DE for XP

POR_FLIT_PAR_EN	POR_DATACHECK_EN	MXP_DEV_DATACHECK_EN		ED	DE
		P0	P1		
0	0	0	0	`2'b00`	`2'b00`
0	1	0	0	`2'b01`	`2'b01`
		0	1	`2'b01`	`2'b01`
		1	0	`2'b01`	`2'b01`
		1	1	`2'b00`	`2'b00`
1	0	0	0	`2'b01`	`2'b00`
1	1	0	0	`2'b01`	`2'b01`
		0	1	`2'b01`	`2'b01`
		1	0	`2'b01`	`2'b01`
		1	1	`2'b01`	`2'b00`

For SBSX, the default values of ED and DE are `2'b01` if SBSX_AXDATAPOISON_EN_PARAM is not set. If the parameter is set, the default values are `2'b00`.

For HN-I and HN-F, the default values of ED and DE are always `2'b01`.

All fields are required, even though only HN-F has CE counters implemented in **errmisc**.

The default values of **UI**, **FI**, and **CFI** must be `2'b10`, indicating that the interrupt generation is controllable.

2.14.3 Error detection, signaling, and reporting

Each CMN-600 component that is connected to a configuration bus can be included in the local error reporting mechanism.

Error handling protocol is as follows:

Error overflow

The overflow is set when different types of errors are detected. It is also asserted when multiple errors of equal priority are detected.

- `1'b1`: More than one error has been detected.
- `1'b0`: Only one error of the most significant type described by **errstatus.{UE, CE, DE}** has been detected.

This bit is read/write-one-to-clear.

Note

Errstatus.OF is only for the highest priority error. For example, if another DE follows the first DE, **errstatus.OF** is set. When the next UE happens, **errstatus.OF** is cleared because at the time, UE is the highest priority error in the system, and it is the first occurrence of UE.

The following table shows the **errstatus.OF** value after errors occur at t0, t1, and t2.

Table 2-19 Errstatus.OF value after errors

Error at			Status of OF after error		
t0	t1	t2	t0	t1	t2
CE	CE	CE	0	1	1
CE	CE	DE	0	1	0
CE	CE	UE	0	1	0
CE	DE	CE	0	0	0
CE	DE	DE	0	0	1
CE	DE	UE	0	0	0
CE	UE	CE	0	0	0
CE	UE	DE	0	0	0
CE	UE	UE	0	0	1
DE	CE	CE	0	0	0
DE	CE	DE	0	0	1
DE	CE	UE	0	0	0
DE	DE	CE	0	1	1
DE	DE	DE	0	1	1
DE	DE	UE	0	1	0
DE	UE	CE	0	0	0
DE	UE	DE	0	0	0
DE	UE	UE	0	0	1
UE	CE	CE	0	0	0
UE	CE	DE	0	0	0
UE	CE	UE	0	0	1
UE	DE	CE	0	0	0
UE	DE	DE	0	0	0
UE	DE	UE	0	0	1
UE	UE	CE	0	1	1

Table 2-19 Errstatus.OF value after errors (continued)

Error at			Status of OF after error		
t0	t1	t2	t0	t1	t2
UE	UE	DE	0	1	1
UE	UE	UE	0	1	1

Errmisc fields

Errmisc is the secondary error syndrome register. The fields of this register differ for ECC, parity, and other errors. The following tables summarize all the valid fields for each unit.

Table 2-20 Errmisc register bits

Bit	Component				
	XP	HN-I	HN-F	SBSX	CXHA (CML only)
63	-	-	CECOF	-	-
62			SETMATCH		
61			-		
60			ERRSET[12:0]		
59					
58	TGTID[10:0]				
57					
56		LPID[4:0]			
55					ERRSET[7:0]
54					
53					
52					
51		-			
50					
49		ORDER[1:0]			
48					
47	-	-	CEC[15:0]		-
46					
45					
44					
43					
42					
41					
40					
39					
38					
37					
36					
35					
34					
33					
32					

Table 2-20 Errmisc register bits (continued)

Bit	Component				
	XP	HN-I	HN-F	SBSX	CXHA (CML only)
31	-	-	-	-	-
30		SIZE[2:0]		SIZE[2:0]	
29					
28					
27		MEMATTR[3:0]		MEMATTR[3:0]	
26					
25					
24					
23		-		-	
22					
21	OPCODE[5:0]	OPCODE[5:0]			
20					
19					
18					
17			OPTYPE[1:0]		
16				OPTYPE	
15	-	-	-	-	
14	SRCID[10:0]	SRCID[10:0]	SRCID[10:0]	SRCID[10:0]	
13					
12					
11					
10					
9					SRCRAID[5:0]
8					
7					
6					
5					
4					
3	-	ERRSRC[3:0]	ERRSRC[3:0]	-	-
2	ERRSRC[2:0]				
1					ERRSRC[1:0]
0					

Error log clearing

In addition to the error syndrome registers, each component has a write-only error syndrome clear register. Write the applicable mask bits to clear the **first_err_vld** and **mult_err** bits of the Error Syndrome 0 register.

2.14.4 Error handling requirements

This section describes the specific error handling behaviors of CMN-600.

Error reporting rules

CMN-600 uses specific error reporting rules.

The rules regarding error reporting in CMN-600 are:
- Any error originating in CMN-600 is reported.
- Any error originating outside CMN-600 but corrupting CMN-600 is reported.
- The HN-I can report an error in a response packet from outside CMN-600 if it does not propagate the response any further.
- All non-posted write errors are propagated where possible.

2.14.5 HN-F error handling

Errors are reported at the HN-F for various reasons.

Request Errors at HN-F

The HN-F detects:
- ECC errors in SF Tag, SLC Tag and Data RAMs.
- Datacheck and poison errors on DAT flits.
- *Non-Data Errors* (NDEs) on responses.

ECC errors in SF Tag, SLC Tag, and Data RAMs

HN-F detects single-bit and double-bit ECC errors in the SF Tag, SLC Tag, and Data RAMs. It can correct single-bit ECC errors. Such errors are logged and reported as CEs.

Double-bit ECC errors detected in the SLC Data RAM are logged and reported as DEs. Such errors are propagated to the consumer of the data in the form of data poison.

Double-bit ECC errors detected in SF Tag RAM are logged and reported as DEs. But such errors are not propagated to the requestor. The SF Tag RAM in the HN-F is disabled following the first occurrence of the double-bit ECC error.

Double-bit ECC errors detected in the SLC Tag RAM are fatal. They are logged and reported as UEs. Such errors are propagated to the requestor as NDEs in the responses.

Datacheck and poison errors on DAT flits

If data is allocated by the HN-F, the HN-F detects datacheck errors and poison error on the data flits. In such cases, HN-F logs and reports the datacheck error as a DE. If HN-F allocated the data in SLC Data RAM, it converts the datacheck error into data poison for all subsequent requests to this cacheline.

If **por_hnf_aux_ctl.hnf_poison_intr_en** = 1, then the poison errors originating from HN-F are logged and reported as UEs.

NDEs on responses

HN-F may receive NDEs from other data and response sources such as RN-F, RN-I, and SN-F. If the cache line was allocated in SLC Data RAM, it is logged and reported as a UE. If the cache line is not allocated in HN-F SLC, it propagates the errors to the requestor as an NDE.

2.14.6 HN-I error handling

Errors are reported at the HN-I for various reasons.

Request errors at HN-I

The HN-I detects errors on receiving following requests and sends an NDE response to the requesting RN. It logs request information in the error logging registers, **por_hni_erraddr(_NS)** and **por_hni_errmisc(_NS)**. They are marked as DEs in the error status register, **por_hni_errstatus(_NS)**:

1. Coherent Read.
2. CleanUnique/MakeUnique.
3. Coherent/CopyBack Write.
4. Atomic.
5. Illegal Configuration Read/Write.

The configuration bit, **por_hni_cfg_ctl.reqerr_cohreq_en**, can enable or disable the sending of NDE responses and logging of error information for following request types. By default, this bit is enabled. It can only be programmed during boot time to any one of the following:

1. Coherent Read.
2. CleanUnique/MakeUnique.
3. Coherent/CopyBack Write.

The following table lists all the requests a HN-I detects as errors and the support of **reqerr_cohreq_en**.

Table 2-21 HN-I request errors and support for configuration bit

Request type	Reqerr_cohreq_en controls sending of NDE and log error
Coherent Read	Yes
CleanUnique/MakeUnique	Yes
Coherent/CopyBack Write	Yes
Atomics	No
Illegal Configuration Read/Write	No

- Coherent reads are downgraded to ReadNoSnp and sent downstream (AXI/ACE-Lite slave).
- Coherent/Copyback writes are downgraded to WriteNoSnp and sent downstream (AXI/ACE-Lite slave).
- Illegal Configuration Read is sent as ReadNoSnp to downstream (AXI/ACE-Lite slave).
- CleanUnique, MakeUnique, Atomics, and Illegal Configuration Writes are handled within HN-I.
- StashOnceShared, StashOnceUnique, and PrefetchTgt are completed within HN-I without any errors.

Data Errors at HN-I

The HN-I only detects errors on write data if it does not detect an error on that request.

To summarize:

- For AXI/ACE-Lite write requests with no request error, on receiving Poison error on data, HN-I detects the error and logs request information in **por_hni_erraddr(_NS)** and **por_hni_errmisc(_NS)** if downstream does not support poison. They are marked as UEs in the error status register, **por_hni_errstatus(_NS)**.
- For configuration write requests with no request error, on receiving write data with Partial ByteEnable error, Datacheck error, or Poison, HN-I detects and sends an NDE response to the requesting RN. It logs the SrcID and TxnID of the request and drops the write. They are marked as DEs in the error status register, **por_hni_errstatus(_NS)**.

  ——— **Note** ———

  StashOnceShared, StashOnceUnique and PrefetchTgt are completed within HN-I without any errors.

  ———————————

Response Errors at HN-I

The HN-I only detects errors on write response if it does not detect an error on that request.

To summarize:

- For AXI/ACE-Lite write requests with early completions from HN-I and no request error, on receiving *Slave Error* (SLVERR), or *Decode Error* (DECERR) on downstream write response (BRESP), HN-I detects the error. It logs request information in **por_hni_erraddr(_NS)** and **por_hni_errmisc(_NS)**. They are marked as UEs in the error status register, **por_hni_errstatus(_NS)**.
- For AXI/ACE-Lite write requests with downstream completions and no request error, SLVERR, or DECERR on downstream write response (BRESP) are passed on to the requesting RN as CHI DEs or NDEs.
- For AXI/ACE-Lite read requests, SLVERR and Poison (if supported by downstream) are both converted to Poison within the CMN-600 system, independent of error on request. DECERR on downstream read responses are passed on to the requesting RN.

HN-I summary on sending NDE and DE

The HN-I sends NDE scenarios for certain situations.

The HN-I sends NDE in the following cases:

- Request error.
  - Coherent Read (if **reqerr_cohreq_en** is set to 1).
  - CleanUnique/MakeUnique (if **reqerr_cohreq_en** is set to 1).
  - Coherent/CopyBack Write (if **reqerr_cohreq_en** is set to 1).
  - Atomic.
  - Illegal Configuration Read/Write.

  ——— **Note** ———

  Refer to *3.1.5 Requirements of configuration register reads and writes* on page 3-171 for legal format of configuration read/write request.

  ———————————

- Write Data Error for configuration write request.
  - Partial ByteEnable error.
  - Datacheck error.
  - Poison.
- AXI/ACE-Lite Response Error.
  - DECERR on downstream write response (BRESP) for writes with downstream completions.
  - DECERR on downstream read response (RRESP).

The HN-I sends DE in the following cases:

- AXI/ACE-Lite Response Error.
  - SLVERR on downstream write response (BRESP) for writes with downstream completions.

HN-I summary on logging errors

The HN-I logs an error as deferred or uncorrected in certain conditions.

The HN-I logs an error as deferred in the following cases:

- Request error.
  - Coherent Read (if **reqerr_cohreq_en** is set to 1).
  - CleanUnique/MakeUnique (if **reqerr_cohreq_en** is set to 1).
  - Coherent/CopyBack Write (if **reqerr_cohreq_en** is set to 1).
  - Atomic.
  - Illegal Configuration Read/Write.

Note

Refer to *3.1.5 Requirements of configuration register reads and writes* on page 3-171 for legal format of configuration read/write request.

- Write Data Error for configuration write request.
  - Partial ByteEnable error.
  - Datacheck error.
  - Poison.

The HN-I logs an error as uncorrected in the following cases:

- Write Data Error for AXI/ACE-Lite write requests.
  - Poison error on data if downstream doesn't support poison.
- AXI/ACE-Lite Write Response Error.
  - SLVERR or DECERR on downstream write response (BRESP) for writes that were sent early completions.

CML configuration with HN-I

In CML configuration, HNI must be configured to report NDE response on Coherent Requests.

This is accomplished by setting `bit[0] (reqerr_cohreq_en)` of **por_hni_cfg_ctl register**. This action is required in CML mode so NDE error responses are not missed on CCIX because of early completion responses from the CXG block.

2.14.7 SBSX error handling

Errors are reported at the SBSX for various reasons.

Error cases:

1. If the AXI memory controller downstream of SBSX does not support POISON (indicated by **por_sbsx_unit_info.axdata_poison_en** = 0), and if CHI Write Data has Poison set, then SBSX detects and logs this error.
2. If **por_sbsx_cfg_ctl.sbsx_rpt_err_on_poison_rd** = 1, and if SBSX receives Poison on read data from downstream, then SBSX detects and logs this error.

Note

SBSX does not have opcode based Request/Response Error class as does HN-I.

SBSX summary on sending NDE/DE is shown in the following table.

Table 2-22 SBSX summary on sending NDE/DE

Case No.	Source of error	SBSX error response
1	Decode Error on RDATA from AXI side	NDE on COMP_DATA on CHIE side
2	Slave Error on RDATA from AXI side	Poison on COMP_DATA on CHIE side
3	Decode Error on BRESP from AXI side	NDE on COMP for CMOs or Writes with EWA=0
4	Slave Error on BRESP from AXI side	DE on COMP for CMOs or Writes with EWA=0

2.14.8 RN-I error handling

RN-I does not report any errors.

Coherent transactions received at RN-I from AXI/ACE-Lite master which are targeted for HN-I are downgraded to non-coherent transactions. For example, **ReadOnce** is downgraded to **ReadNoSnp** and **WriteUnique** is downgraded to **WriteNoSnp**.

2.14.9 XP error handling

Errors are reported at the XP for various reasons.

The following errors are detected in the XP:

- Flit parity error.
- Datacheck error (DAT channel only).

Flit parity error

Flit parity is generated on a flit upload from a device port to a mesh port, for both internal and external devices. Flit parity check is done on a flit download from a mesh port to a device port.

Flit parity is neither generated nor checked when a flit is bypassed or looped back across the device ports on the same XP.

Data check error

Datacheck is enabled in the XP using the DATACHECK_EN parameter.

Datacheck (Data Byte Parity) bits are generated corresponding to each byte of data on a DAT flit upload from a device port when the corresponding device does not support Datacheck (indicated by DEV_DATACHECK_EN = 0).

Datacheck is accomplished on a flit download to a device which does not support Datacheck.

Datacheck bits are generated and checked when a DAT flit is bypassed or looped back across the device ports on the same XP when the corresponding devices involved do not support DataCheck.

Error reporting and logging

Flit parity and Datacheck errors are reported to the *RAS Control Block* (RCB). The following table contains flit fields logged in the XP configuration register.

Table 2-23 XP configuration register flit fields

Error Source	Errstatus					Errmisc			
-	DE	CE	MV	UE	V	ERRSRC	SRCID	OPCODE	TGTID
Data Parity P0 Req channel	1	0	1	0	1	3'b000	v	v	v
Data Parity P1 Req channel	1	0	1	0	1	3'b001	v	v	v
Data Parity P0 Rsp channel	1	0	1	0	1	3'b010	v	v	v
Data Parity P1 Req channel	1	0	1	0	1	3'b011	v	v	v
Data Parity P0 Snp channel	1	0	1	0	1	3'b100	v	v	0
Data Parity P1 Snp channel	1	0	1	0	1	3'b101	v	v	0
Data Parity P0 Dat channel	1	0	1	0	1	3'b110	v	v	v
Data Parity P1 Dat channel	1	0	1	0	1	3'b111	v	v	v
FLIT Parity P0 Req channel	0	0	1	1	1	3'b000	v	v	v
FLIT Parity P1 Req channel	0	0	1	1	1	3'b001	v	v	v
FLIT Parity P0 Rsp channel	0	0	1	1	1	3'b010	v	v	v
FLIT Parity P1 Req channel	0	0	1	1	1	3'b011	v	v	v
FLIT Parity P0 Snp channel	0	0	1	1	1	3'b100	v	v	0
FLIT Parity P1 Snp channel	0	0	1	1	1	3'b101	v	v	0
FLIT Parity P0 Dat channel	0	0	1	1	1	3'b110	v	v	v
FLIT Parity P1 Dat channel	0	0	1	1	1	3'b111	v	v	v

If the device supports Poison (indicated by DEV_POISON_EN = 1), the Datacheck error is factored in the **POISON** field of the DAT flit. Else, it is factored in as DataError in the **RESPERR** field.

2.14.10 CXHA error handling

Errors are reported at the CXHA for various reasons.

CXHA uses RAMs as buffers for storing the Read and Write data. The contents of the RAM are protected using byte parity. CXHA reports errors if there is an error detected when the contents of the Data RAMs are read. These detected errors are of two types:

- Parity error on Byte-Enable (BE) fields of the Write Data RAM.
- Parity error on Data and Poison fields of the Read and Write Data RAM.

Parity error on Byte-Enable fields of the Write Data RAM

The Write Data buffer RAM stores BE. Parity errors detected on BE are treated as UEs. Upon detecting an error, CXHA does the following:

- Logs the error as UE.

Parity error on Data and Poison fields of the Read and Write Data RAM

The Read and Write data buffer RAMs contain the Data and Poison fields. Errors detected on these fields are treated as DEs. If an error is detected on Data fields, then the CXHA does the following:

- Logs the error as DE.
- Poisons the data (per CHI specification) by setting the corresponding poison bit of the data.

If an error is detected on Poison fields, then the CXHA does the following:

- Logs the error as DE.
- All Poison bits are set to `1'b1`.

2.14.11 CCIX PER messaging support

CMN-600 CML support sending of CCIX *Protocol Error* (PER) message to the CCIX Error Agent present on the Host chip.

CMN-600 includes configuration registers, present in CXLA, and mechanism to trigger a CCIX PER message. It is expected that an external Error Aggregator/Handler present outside CMN-600 will collect/consolidate all the errors and use these registers to trigger a CCIX PER message to the CCIX Error Agent.

CXLA Configuration Registers:

- CCIX PER Message Payload
  - por_cxla_permsg_pyld_0_63
  - por_cxla_permsg_pyld_64_127
  - por_cxla_permsg_pyld_128_191
  - por_cxla_permsg_pyld_192_255
- CCIX PER Message Control
  - por_cxla_permsg_ctl
- CCIX Error Agent ID
  - por_cxla_err_agent_id

Mechanism:

- Error Aggregator external to CMN-600
  - Writes the PER payload in CCIX PER Message Payload registers (por_cxla_permsg_pyld_*)
  - Sets per_msg_vld_set bit in CCIX PER Message Control register (por_cxla_permsg_ctl). When set, a PER message is sent on the given CCIX link determined by the Target ID

  It is the responsibility of CCIX discovery software to program CCIX Error Agent ID in CCIX Error Agent ID **por_cxla_err_agent_id** register. This programming should happen during initial system bring up and the programmed ID is used as the target ID on CCIX PER message.

  PER message is supported only in non-SMP mode and therefore **smp_mode_en bit in por_cxla_aux_ctl** register must be cleared during initial system start up. Please refer to *2.32 CML Symmetric Multi-Processor (SMP) Support* on page 2-168 for more details on SMP mode.

  By default, *Error SourceID* (ESID) field from PER message payload (bit [53:48]) is used as source ID on PER message. **per_msg_srcid_ovrd** and **per_msg_srcid** fields in CCIX PER message control register **por_cxla_permsg_ctl** can be used to override source ID sent on PER message.

  ——— **Note** ———

  CMN-600 CML does not implement a CCIX Error Agent. It can accept the incoming PER messages, but these messages are dropped at CXLA.

  ———————————

2.15 System Address Map

Every master connected to CMN-600 has the same view of memory.

The entire addressable space can be partitioned into subregions, and each partition must be designated as:

- I/O space, or
- DDR space.

Note

Unmapped addresses are routed to the HN-D.

Requests to the I/O space are serviced by HN-I, HN-D, and HN-T. Requests to DDR space are serviced by HN-F, SN-F, and SBSX.

Each HN-F covers a mutually exclusive portion of the system address space.

- Each HN-F can contain a System Level Cache (SLC).
- HN-Fs can be combined into System Cache Groups (SCG).
- Each HN-F in an SCG must have the same SLC partition size.
- The target HN-F within an SCG is determined by an address hash function.

All CHI transactions require a target ID to route packets from source to destination. For addressable requests, the target ID is determined by a *System Address Map* (SAM). A SAM is located in each node that can generate a CHI addressable request. These SAMs include:

- RN SAM: Present in all RNs. Generates a target ID for requests to HN-F, HN-I, HN-D, HN-T, SBSX, and SN-F.
- CXRA SAM: Present in all CCIX request agent nodes. Generates a target ID for requests to CCIX home agent nodes.
- HN-F SAM: Present in all HN-Fs. Generates a target ID for requests to SN-F and SBSX.
- HN-I SAM: Present in all HN-Is. Maps the incoming CHI request's address to an I/O subregion for ordering purposes.

2.16 RN SAM

Transactions from an RN must pass through an RN SAM in order to generate a CHI target ID.

RN-Is and CXHA have an RN SAM that is internal to CMN-600. CHI RN-Fs can use an RN SAM external or internal to CMN-600. This is a configuration option. Instantiating a SAM internal to CMN-600 for CHI.A RN-Fs is also a configuration option. If this option is not selected, an external SAM must be created and integrated for the CHI.A RN-F, and must be configurable without relying on the use of the CMN-600 programmable register space. Such an external RN SAM for CHI.A masters is not provided by Arm.

This section contains the following subsections:

2.16.1 Target IDs

This section describes how the target ID is determined.

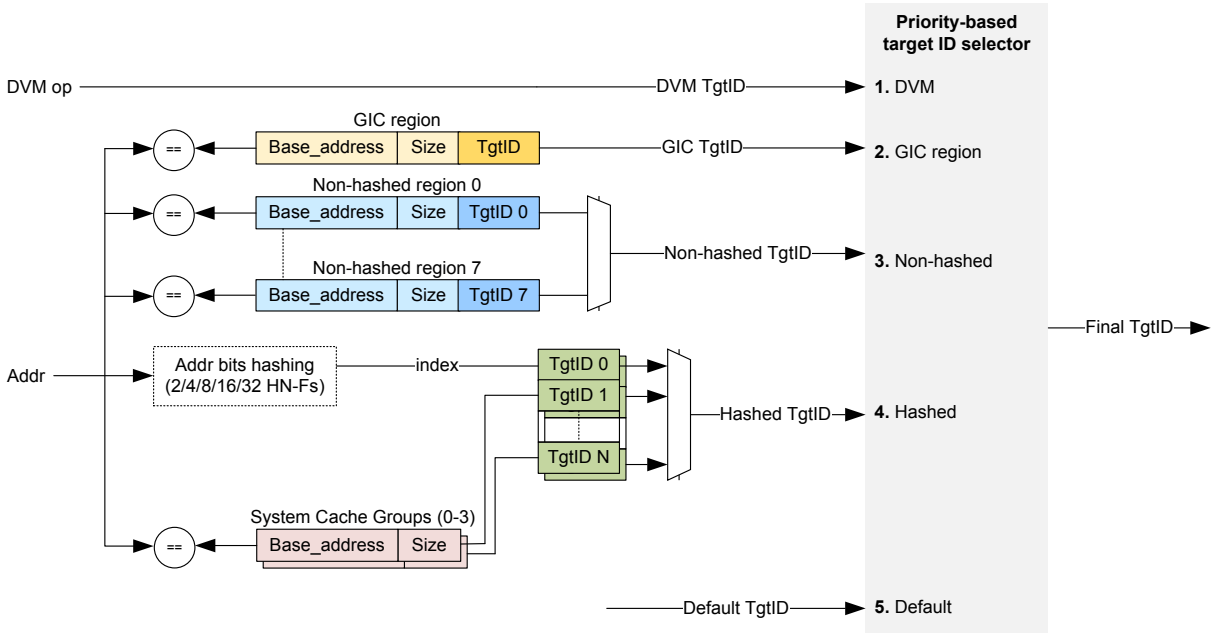


Figure 2-28 CMN-600 RN SAM target ID selection policy

Default target ID

Until the RN SAM has been fully programmed, all addressable transactions use the default target ID. RN SAMs that are internal to CMN-600 define the HN-D node ID as their default target ID. RN SAMs that are external to CMN-600 must be configured with a default target ID, likely via a strap input. Once the RN has been programmed, the default target ID is only selected for addressable requests that do not fall within one of the programmed address regions.

Hashed and non-hashed regions

A given memory partition can be:

- Distributed (hashed) across many target devices, or
- Assigned to an individual device (non-hashed).

A hashed region can overlap with a non-hashed region. Whether a given region is configured as hashed or non-hashed affects the target ID selection policy for that address range. The SCG region registers support up to four hashed regions. The non-hashed region registers support up to eight non-hashed regions.

The I/O space (HN-I, HN-D, and HN-T) is intended to be the target of non-hashed regions. The DRAM space (HN-F), however, can be the target of either non-hashed or hashed regions. It is also possible to classify a region that only targets one HN-F as hashed. Additional configuration scenarios include:

- Using an SCG region register for an HN-I, HN-D, and HN-T target. This may be useful if all the non-hashed region registers have already been used. The region can optionally be classified as a non-hashed region (except for SCG region 0).
- Using a non-hashed region register for an HN-F target. This may be useful if all the SCG region registers have already been used. For target ID selection purposes, this HN-F is classified as a non-hashed region.

GIC target ID

RN SAMs also support a Global Interrupt Controller (GIC) memory region which can be used to select GIC-related addresses to a specific target ID. The GIC region can overlap with hashed and non-hashed regions.

RN SAM target ID selection policy

RN SAMs support priority-based target ID selection. The order of priority is when selecting a target ID is:

1. GIC memory region (highest priority).
2. Non-hashed memory region.
3. Hashed memory region.
4. Default memory region (lowest priority).

DVM target ID

DVM transactions are assigned the DVM target ID. RN SAMs that are internal to CMN-600 define the HN-D's node ID as the DVM target ID. RN SAMs that are external to CMN-600 must be configured with a DVM target ID, likely via a strap input.

2.16.2 Memory region requirements

This section describes the RN SAM memory region requirements.

Each of the programmed region sizes must be a power of two and the partition must be size-aligned. The region size can range from 64MB–256TB. For example, a 1GB partition must start at a 1GB-aligned boundary.

It is possible to support complex memory maps where DRAM region sizes are not a power of two or are not size-aligned. For example, the figure below shows a memory map where the entire address is assigned to a hashed region. Then, non-hashed regions can be individually programmed, given their higher target ID selection priority. Accesses to addresses in a hashed region that are not actually backed by physical memory must be prevented by software. Refer to the *Principles of Arm Memory Maps White Paper* for more information.

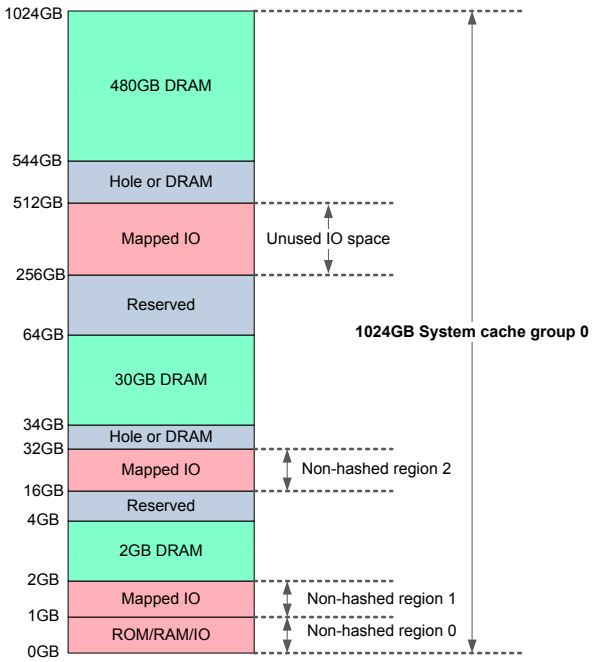


Figure 2-29 Example memory map

2.16.3 System Cache Groups

This section provides System Cache Group configuration information.

A System Cache Group (SCG) is a group of HN-Fs that share a contiguous address region. However, the addresses covered by each HN-F in an SCG are mutually exclusive. An HN-F belonging to an SCG is selected as the target based on a hash function.

An SGC supports hashing over 1, 2, 4, 8, 16, or 32 HN-Fs, using bits [MSB:6] of the physical address of the request. If CMN-600 has been configured to implement fewer than 48 physical address bits, the unused upper bits are assumed to be zero. The hash algorithm calculates a pointer in the HN-F ID table in the RN SAM. The hash function is explicitly given below. All the numbers on the right-hand side of the equations below are bit positions within the physical address (e.g. 17 corresponds to physical address bit [17]). In the equations, ^ represents XOR.

- 2 HN-Fs
  - Number of bits in select: 1
  - select [0] = (6^7^8^…^47)
- 4 HN-Fs
  - Number of bits in select: 2
  - select [0] = (6^8^10^…^46)
  - select [1] = (7^9^11^…^47)
- 8 HN-Fs
  - Number of bits in select: 3
  - select [0] = (6^9^12^…^45)
  - select [1] = (7^10^13^…^46)
  - select [2] = (8^11^14^…^47)
- 16 HN-Fs
  - Number of bits in select: 4
  - select [0] = (6^10^14^…^46)
  - select [1] = (7^11^15^…^47)

  - select [2] = (8^12^16^…^44)
  - select [3] = (9^13^17^…^45)
- 32 HN-Fs
  - Number of bits in select: 5
  - select [0] = (6^11^16^…^46)
  - select [1] = (7^12^17^…^47)
  - select [2] = (8^13^18^…^43)
  - select [3] = (9^14^19^…^44)
  - select [4] = (10^15^20^…^45)

System Cache Group (SCG) configuration

Up to four SCGs are supported, depending on the number of HN-Fs in each SCG. The following table shows the restrictions on SCG selection when there are 16 or 32 HN-Fs in a given SCG.

Table 2-24 Permitted allocation of HN-Fs into SCGs

SysCacheGroup HN-F/SN-F counts	1 HN-F	2 HN-F	4 HN-F	8 HN-F	16 HN-F	32 HN-F
SysCacheGroup 0	Y	Y	Y	Y	Y	Y
SysCacheGroup 2	Y	Y	Y	Y	Y	N
SysCacheGroup 1	Y	Y	Y	Y	N	N
SysCacheGroup 3	Y	Y	Y	Y	N	N

The following table shows how hashed target IDs are programmed in each SCG. For example, if SCG0 has 32 HN-Fs, then it uses all the available node ID registers and other SCGs cannot be used. However, if SCG0 is only using 16 HN-Fs, then SCG2 and SCG3 can still be used with eight each HN-F target IDs. This table is also applicable to the SN-F target ID registers if PrefetchTgt is supported in the RN SAM.

Table 2-25 Target ID programming

SCG target ID Regs (32 hashed targets)	Number of HN-Fs per SCG			
	32	16	8	4, 2, 1
scg_nodeid_reg0	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs
scg_nodeid_reg1				-
scg_nodeid_reg2			SCG1_NIDs	SCG1_NIDs
scg_nodeid_reg3				-
scg_nodeid_reg4		SCG2_NIDs	SCG2_NIDs	SCG2_NIDs
scg_nodeid_reg5				-
scg_nodeid_reg6			SCG3_NIDs	SCG3_NIDs
scg_nodeid_reg7				-

The following table contains an example mapping of 25 HN-Fs to three SCGs.

Table 2-26 25 HN-Fs to three SCGs programming example

SCG number	Number of HN-Fs	Node ID
SCG0	16	NID0-15
SCG2	8	NID16-23
SCG3	1	NID24

The following table contains an example programming for the 25 HN-Fs.

Table 2-27 Example programming for the 25 HN-Fs

SCG target ID registers	Number of HN-Fs per SCG			
	32	16	8	1
scg0_nodeid_reg0	-	SCG0 NID0-15	-	-
scg0_nodeid_reg1				
scg1_nodeid_reg0				
scg1_nodeid_reg1				
scg2_nodeid_reg0		-	SCG2 NID16-23	
scg2_nodeid_reg1				
scg3_nodeid_reg0			-	SCG3 NID24
scg3_nodeid_reg1				-

2.16.4 PrefetchTgt RN SAM

The RN SAM supports CHI PrefetchTgt operations.

These operations are sent from RN-F directly to SN-F, bypassing the HN-F. To support such requests, the RN SAM integrates the functionality of HN-F SAM to determine the appropriate SN-F target ID for a given address. RN-Fs that integrate the PrefetchTgt RN SAM only use the SN-F target ID for PrefetchTgt requests. The PrefetchTgt RN SAM programming must match the HN-F SAM with respect to SN-F target IDs.

The registers used for programming the PrefetchTgt RN SAM are:

- **por_rnsam_sys_cache_grp_sn_attr**
- **por_rnsam_sys_cache_grp_sn_nodeid_reg{0-7}**
- **por_rnsam_sys_cache_grp_sn_sam_cfg{0-1}**

2.17 CXRA SAM

All CCIX Requesting Agents (CXRA) in CMN-600 require a CCIX RA SAM to determine the target CCIX Home Agent ID (HAID). This HAID is used as the target ID to route the CCIX Request.

The Requesting Agent System Address Map (RA SAM) uses configuration registers to specify address regions and corresponding HAIDs. Each address region is configured by programming the base address and corresponding size of the address region (or programming the address limit). Each valid address region is marked using a valid bit. The incoming address is compared against programmed valid address regions to generate a specific HAID.

The following figure shows a CCIX RA SAM block diagram.

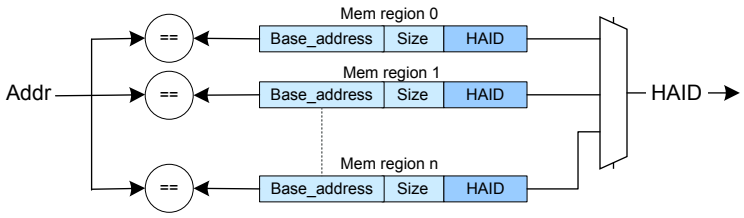


Figure 2-30 RA SAM block diagram

Address region requirements

Each of the programmed address region size must be a power of two and must be naturally aligned to its size. For example, a 1GB partition must start at 1GB boundary. That is, 0GB-1GB or 1GB-2GB and so forth, but it cannot start from 1.5GB or 2.5GB.

Refer to *2.23 Cross chip routing and ID mapping* on page 2-134 for details on how CCIX messages are routed based on the CXRA SAM programming.

2.18 HN-F SAM

Transactions from an HN-F to an SN must pass through an HN-F SAM to generate a CHI target ID.

The following figure shows how the target ID is determined.

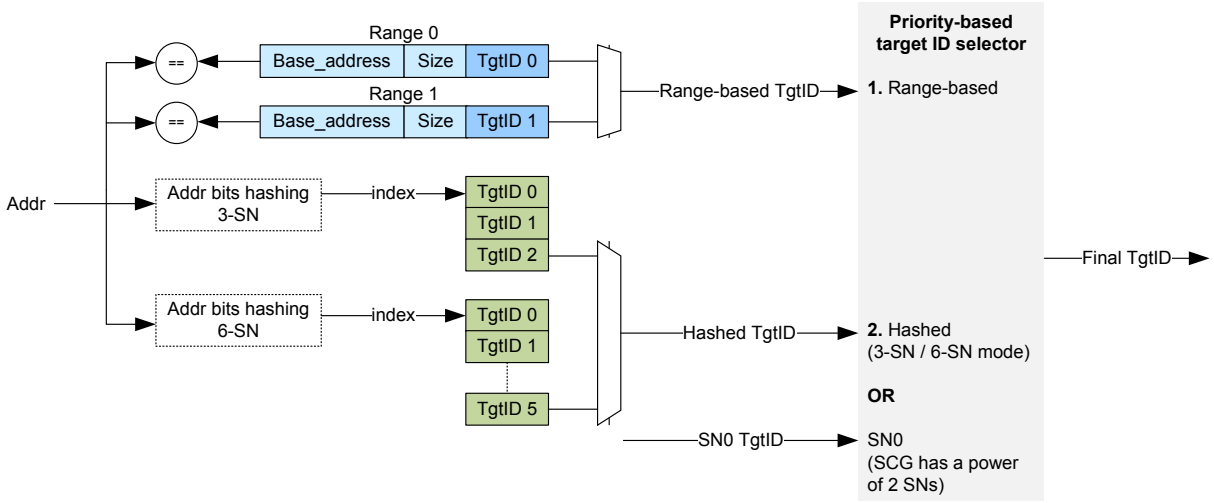


Figure 2-31 CMN-600 HN-F SAM block diagram

Range-based mapping is an address-based target ID generation policy. Up to two address regions can be created, each targeting a single HN. This mode is useful where a partition of memory from the global DRAM is mapped explicitly to an individual SN (for example, an on-chip SRAM).

The HN-F SAM supports two address striping modes for SN target ID selection, which can only be used when three or six SNs are targeted by the SCG:

- 3-SN mode: Addresses from a given HN-F are striped across the three SNs.
- 6-SN mode: Addresses from a given HN-F are striped across the six SNs.

Addresses within the SCG's address range are striped at a 256B granularity between the selected SNs. The stripe function uses address bits [16:8], and an additional two (3-SN) or three (6-SN) user-defined address bits.

Direct SN mapping is used if the SCG targets 1, 2, 4, or 8 SNs. In this case, the SN0 target ID is used. Distributing accesses across the SNs targeted by the SCG is achieved by programming each HN-F's SN0 field to the SN node ID it targets. For example, if an SCG with eight HN-Fs targets eight SNs, each HN-F's SN0 field would be programmed with a different SN node ID. If that same SCG with eight HN-Fs targeted four SNs instead, every two HN-F nodes would have the same SN0 field value.

HN SAMs support priority-based target ID selection. The order of priority is when selecting a target ID is:

1. Range-based mapping (highest priority).
2. Striped target ID (3-SN or 6-SN mode), or SN0 (SCG has a power of 2 SNs).

This section contains the following subsections:

- *2.18.1 3 SN-F and 6 SN-F memory striping* on page 2-106.
- *2.18.2 SN contiguous address spaces* on page 2-110.

2.18.1 3 SN-F and 6 SN-F memory striping

CMN-600 supports both 3 SN-F and 6 SN-F memory striping.

3 SN-F memory striping

The traffic is distributed evenly among the three SNs using a function based on physical address (PA[16:8]) and two higher bits in the physical address referred to **top_address_bit1** and **top_address_bit0**. The top address bits are selected such that three of the four combinations of the top address bits appear evenly in the selected address space, and the fourth combination never appears (in some situations, a top bit may be the inverse of the selected PA bit).

For each physical address, one of the three SNs is selected using the following formula:

```
SN = { ADDR[10:8] + ADDR[13:11] + ADDR[16:14] + ((top_addr_bit1<<1) |
top_addr_bit0) } % 3
```

General SN distribution behavior example

For a simple case with a 3GB flat address space starting at address `0x0`, **top_address_bit1** is PA[31], and **top_address_bit0** is PA[30]. With increasing physical address, the function steps between SNs at a 256-byte granularity. As the physical address iterates from 0-128KB, with **top_address_bit1** = **top_address_bit0** = 0, the first three terms distribute the traffic relatively evenly among the SNs. Of the 512 blocks (256B each) in the first 128KB, the distribution is:

- SN[0] => 170 blocks 33.2%
- SN[1] => 171 blocks 33.4%
- SN[2] => 171 blocks 33.4%

This pattern repeats over each 128KB until 1GB, where **top_address_bit0** toggles. With **top_address_bit1** = 0 and **top_address_bit0** = 1, the pattern is shifted. For each 128KB:

- SN[0] => 171 blocks 33.4%
- SN[1] => 170 blocks 33.2%
- SN[2] => 171 blocks 33.4%

At 2GB, when **top_address_bit1** = 1 and **top_address_bit0** = 0, the pattern shifts again:

- SN[0] => 171 blocks 33.4%
- SN[1] => 171 blocks 33.4%
- SN[2] => 170 blocks 33.2%

Over the full 3GB, exactly the same number of lines are distributed to each SN.

The HN-F uses the **hn_cfg_three_sn_en** bit in its **por_hnf_sam_control** register to enable routing to three SNs. In the **por_hnf_sam_control** register, the **hn_cfg_sam_top_address_bit0** and **hn_cfg_sam_top_address_bit1** fields must be configured at boot time. These two address bits are decoded, and used in combination with a hashing function to determine the target SN-F.

6 SN-F memory striping

Similar to 3-SN hashing, 6-SN extends the function to equally distribute the addresses between six SNs. For each physical address, one of the six SNs is selected using the following formula:

```
SN = { ADDR[10:8] + ADDR[13:11] + ADDR[16:14] + ((top_addr_bit2<<2) |
(top_addr_bit1<<1) | top_addr_bit0) } % 6
```

HN-F SAM uses the **hn_cfg_six_sn_en** bit in its **por_hnf_sam_control** register to enable striping across all six SN-Fs. In 6 SN-F hashed mode, HN-F SAM also uses **hn_cfg_sam_top_address_bit2** field in the **por_hnf_sam_control** register along with **hn_cfg_sam_top_address_bit1** and **hn_cfg_sam_top_address_bit0** to hash the incoming address.

3 SN-F and 6 SN-F configurations

The valid top address bits for Arm PDD Memory Map are shown in the below table. Refer to the *Principles of Arm Memory Maps White Paper* for more information. This ensures equal distribution of requests across all SN-Fs and prevents memory aliasing. The SAM also provides an

inv_top_address_bit configuration bit, which can be used in combination with top address bits as shown in the following table:

Table 2-28 3-SN top address bits [bit 1, bit 0]

Combination 1 (inv_top_address_bit set to 1'b0)	Combination 2 (inv_top_address_bit set to 1'b0)	Combination 3 (inv_top_address_bit set to 1'b1)	Combination 4 (inv_top_address_bit set to 1'b1)
[0, 0]	[1, 1]	[0, 0]	[0, 0]
[0, 1]	[0, 1]	[1, 0]	[0, 1]
[1, 0]	[1, 0]	[1, 1]	[1, 1]

Note

The **inv_top_address_bit**, when set to `1'b1`, forces the SAM to invert the top most significant top address bit (0 to 1, or 1 to 0). For 3-SN, **top_address_bit1** is inverted. For 6-SN, **top_address_bit2** is inverted.

The following table shows the valid combinations for the address bits for 6-SN with PDD memory map.

Table 2-29 6-SN top address bits [bit 2, bit 1, bit 0]

Combination 1 (inv_top_address_bit set to 1'b0)	Combination 2 (inv_top_address_bit set to 1'b0)	Combination 3 (inv_top_address_bit set to 1'b1)
[0, 0, 0]	[0, 1, 0]	[0, 0, 0]
[0, 0, 1]	[0, 1, 1]	[0, 0, 1]
[0, 1, 0]	[1, 0, 0]	[0, 1, 0]
[0, 1, 1]	[1, 0, 1]	[0, 1, 1]
[1, 0, 0]	[1, 1, 0]	[1, 1, 0]
[1, 0, 1]	[1, 1, 1]	[1, 1, 1]

Example for PDD memory map

Assume a system supports three SN-Fs with 32GB of DRAM at each SN-F port and all three SN-Fs are used for SCG 0. Since the DRAM space is non-contiguous in this memory map (2GB + 30GB + 480GB), the base addresses for each DRAM partition are:

1. a. `000_8000_0000` to `000_FFFF_FFFF` (2GB)
   b. `008_8000_0000` to `00F_FFFF_FFFF` (30GB)
2. `088_0000_0000` to `08F_FFFF_FFFF` (32GB)
3. `090_0000_0000` to `097_FFFF_FFFF` (32GB)

The first two regions together comprise a 32GB region, while the remaining two regions are 32GB each. The following table breaks down the address bits for the above regions.

Table 2-30 Address region example bit settings: 3-SN example

Region	39	38	37	36	35	34	33	32	31
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	1	x	x	x	1

Table 2-30 Address region example bit settings: 3-SN example (continued)

Region	39	38	37	36	35	34	33	32	31
2	1	0	0	0	1	x	x	x	x
3	1	0	0	1	0	x	x	x	x

From the address bit breakdown, the selected top address bits must make sure both regions marked as Region 1 have the same values to ensure no aliasing in memory. For this memory map and DRAM size, there are no address bits that directly give us Combination 1 or Combination 2 as shown in *Table 2-28 3-SN top address bits [bit 1, bit 0]* on page 2-108. However, if bits [39, 36] are used along with **inv_top_address_bit** = 1, then Combination 3 is possible. This ensures that the memory requests are equally distributed across the 3 SN-Fs without memory aliasing.

The following figure shows the Arm proposed memory map.

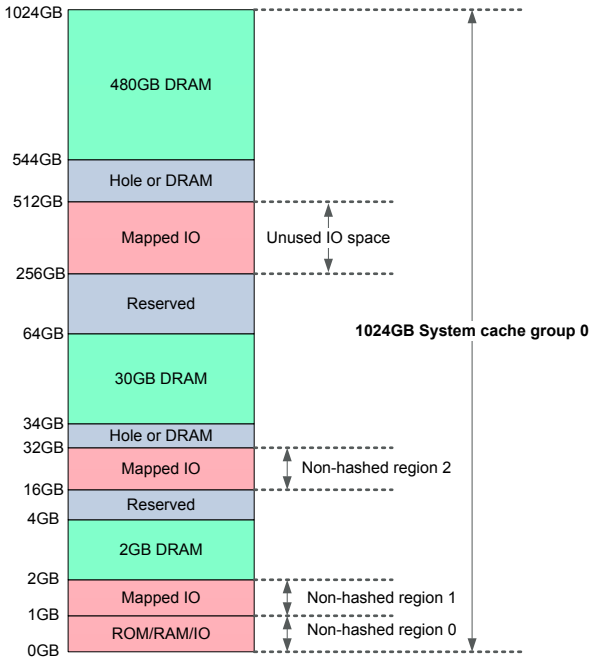


Figure 2-32 Example memory map programming

The following tables provide example address bits that are known to provide equal distribution of memory across all SN-Fs in 3 SN-F and 6 SN-F hashed modes.

Table 2-31 3-SN DRAM size settings

3-SN DRAM size at each SN-F port	Top address bits [bit 1, bit 0]	Inv_top_address_bit value
1GB (Total 3GB)	[35, 30]	`1'b0`
2GB (Total 6GB)	[35, 31]	`1'b0`
4GB (Total 12GB)	[33, 32]	`1'b0`
8GB (Total 24GB)	[34, 33]	`1'b0`
16GB (Total 48GB)	[39, 34]	`1'b0`
32GB (Total 96GB)	[39, 36]	`1'b1`

Table 2-31 3-SN DRAM size settings (continued)

3-SN DRAM size at each SN-F port	Top address bits [bit 1, bit 0]	Inv_top_address_bit value
64GB (Total 192GB)	[37, 36]	1'b0
128GB (Total 384GB)	[38, 37]	1'b0

Table 2-32 6-SN DRAM size settings

6-SN DRAM size at each SN-F port	Top address bits [bit 2, bit 1, bit 0]	Inv_top_address_bit value
1GB (Total 6GB)	[35, 31, 28]	1'b0
2GB (Total 12GB)	[33, 32, 28]	1'b0
4GB (Total 24GB)	[34, 33, 28]	1'b0
8GB (Total 48GB)	[39, 34, 33]	1'b0
16GB (Total 96GB)	[39, 36, 28]	1'b1
32GB (Total 192GB)	[37, 36, 28]	1'b0
64GB (Total 384GB)	[38, 37, 28]	1'b0

2.18.2 SN contiguous address spaces

This section describes which physical address bits must be connected to an SN-F for various configurations.

If all HN-Fs send their cache misses to a single SN-F, that SN-F sees the full address space. However, it is common for a system to have two or more SN-Fs, with each HN-F sending its cache misses to a single SN-F. In this scenario, each SN-F receives only part of the address space. SN-F typically removes one or more address bits in order to retain a contiguous address map. The full physical address is presented to each SN-F for every request. This is necessary so that any SN-F based memory protection logic can function. However, the actual mapping to RAM locations can be done with the modified address. The address modification depends on multiple factors:

- Number of HN-Fs in the cache group.
- Number of SN-Fs in the cache group.
- Which HN-Fs share SN-Fs.

2^n-SN address striping

The following table provides HN-F and SN-F combinations supported within a cache group, along with the address bits that should be removed.

Table 2-33 HN-F and SN-F combinations supported within a cache group

Number of HN-Fs	Number of SN-Fs	Bits to strip from full PA
2	1	None
	2	[6]
4	1	None
	2	[7]
	4	[7, 6]

Table 2-33 HN-F and SN-F combinations supported within a cache group (continued)

Number of HN-Fs	Number of SN-Fs	Bits to strip from full PA
8	1	None
	2	[8]
	4	[8, 7]
	8	[8, 7, 6]
16	1	None
	2	[9]
	4	[9, 8]
	8	[9, 8, 7]
	16	[9, 8, 7, 6]
32	1	None
	2	[10]
	4	[10, 9]
	8	[10, 9, 8]
	16	[10, 9, 8, 7]
	32	[10, 9, 8, 7, 6]

The method used to calculate the bits stripped is as follows:

- The highest bit removed is the least significant address bit used in the XOR function for the most significant bit of the HN-F select hash function.
  - 32 HN-Fs: PA[10]
  - 16 HN-Fs: PA[9]
  - 8 HN-Fs: PA[8]
  - 4 HN-Fs: PA[7]
  - 2 HN-Fs: PA[6]
- The number of bits stripped is $\log_2$(number of SN-Fs), sequentially below the highest bit.

This approach to bit stripping assumes that HN-Fs that share SN-Fs are sequential in the RN SAM cache group HN-F table. For example, if there are eight HN-Fs and two SN-Fs, the bottom four HN-Fs in the RN SAM table would share an SN-F, and the top four HN-Fs would share an SN-F.

3-SN and 6-SN address striping

As 3-SN and 6-SN address hashing implements modulo function, based on the top address bits used, the SN-F must remove these bits to achieve a contiguous memory map in the DRAM.

- 3-SN mode: The SN-F must remove **top_address_bit1** and **top_address_bit0**.
- 6-SN mode: The SN-F must remove **top_address_bit2**, **top_address_bit1**, and **top_address_bit0**.

2.19 RN and HN-F SAM programming

This section describes the various encodings and operating modes of registers in the RN and HN-F SAM.

This section contains the following subsections:

2.19.1 SAM programming sequence

This section describes the SAM programming sequence.

1. Memory map definition

- Define hashed memory regions (targeting HN-Fs).
  - Partition the hashed memory regions into SCGs, if applicable.
- Define non-hashed memory regions (likely targeting HN-I or HN-D).
- Define non-hashed regions with HN-I or HN-D mapping.

  Note

  HN-F may also be used in non-hashed mode if one HN-F is the target.

- Define GIC memory region, if present.
- Define HN-F SAM memory regions, if applicable.
- Define HN-F to SN-F mapping in direct, 3-SN, or 6-SN modes.

2. Check for memory map rules

- Ensure there are no overlapping non-hashed memory regions.
- Ensure there are no overlapping hashed memory regions.
- Check that the memory regions are size aligned.

3. Programming sequence

- For each HN-F SAM:
  - For each SN-F ID, program the appropriate properties based on the features supported in the por_hnf_sam_sn_properties register.
    - The attributes for each SN-F contain the interface width (128b/256b), CMO and PCMO support.
  - If the HN-F is directly mapped to an SN-F:
    - Program the SN0 target ID and corresponding attributes.
  - Else, if the HN-F is in 3-SN or 6-SN mode:
    - Program all SN-F target IDs and the attributes for each SN-F.
    - Program the mode of operation as 3-SN or 6-SN.
    - Program the top address bits.
  - If the HN-F has memory-region-based SN-F partitioning:
    - Program the memory region registers, including the target ID associated with each region.
- For each RN-F RN SAM (or RN-F ESAM within CMN-600):
  - For each SCG:
    - Program the SCG memory region registers.
    - Program the SCG HN-F count registers.
    - Program the SCG HN-F target ID registers.
    - If PrefetchTgt ops are enabled, then:

        - Program the SN-F target ID registers for SCG.
        - Program the SN-F target ID selection mode for SCG.
        - If 3-SN or 6-SN modes are used, program the top address bits.
    - Program the non-hashed memory region registers.
    - Program the non-hashed target ID registers.
    - Program the **rnsam_status** register to disable the default target ID mode.
- For each RN-I RN SAM and RN-D RN SAM:
    - For each SCG:
        - Program the SCG memory region registers.
        - Program the SCG HN-F count registers.
        - Program the SCG HN-F target ID registers.
    - Program the non-hashed memory region registers.
    - Program the non-hashed target ID registers.
    - Program the **rnsam_status** register to disable the default target ID mode.

2.19.2 Region size configuration

This section describes the supported region sizes and their encodings in various programmable registers.

RN SAM and HN-F SAM support memory partition sizes from 64MB to maximum addressable space (2^{48}) for hashed and non-hashed memory partitions. The GIC memory region supports 64KB, 128KB, 256KB and 512KB region sizes. Each partition must be individually programmed in the SAM registers using the following size encodings.

Note

Refer to *3.3 Register descriptions* on page 3-194 for RN SAM register description details.

Table 2-34 RN SAM and HN-F SAM configuration register memory partitions

regionX_size [5 bits]	Memory partition size (hashed and non-hashed regions)	GIC memory partition size
5'b00000	64MB	64KB
5'b00001	128MB	128KB
5'b00010	256MB	256KB
5'b00011	512MB	512KB

Table 2-34 RN SAM and HN-F SAM configuration register memory partitions (continued)

regionX_size [5 bits]	Memory partition size (hashed and non-hashed regions)	GIC memory partition size
5'b00100	1GB	N/A
5'b00101	2GB	
5'b00110	4GB	
5'b00111	8GB	
5'b01000	16GB	
5'b01001	32GB	
5'b01010	64GB	
5'b01011	128GB	
5'b01100	256GB	
5'b01101	512GB	
5'b01110	1TB	
5'b01111	2TB	
5'b10000	4TB	
5'b10001	8TB	
5'b10010	16TB	
5'b10011	32TB	
5'b10100	64TB	
5'b10101	128TB	
5'b10110	256TB	

The RN SAM also outputs the target type of the device along with the target ID for the RN to use in various optimizations. The target type encodings are listed in the following table.

Table 2-35 Target type encodings

Target type [2 bits]	Device type
2'b00	HN-F
2'b01	HN-I
2'b10	CXRA
2'b11	Reserved

The following table contains RA SAM configuration register memory partition sizes and encodings.

Table 2-36 RA SAM configuration register memory partition sizes and encodings

regionX_size	Memory partition size
6'b000000	64KB
6'b000001	128KB
6'b000010	256KB
6'b000011	512KB

Table 2-36 RA SAM configuration register memory partition sizes and encodings (continued)

regionX_size	Memory partition size
6'b000100	1MB
6'b000101	2MB
6'b000110	4MB
6'b000111	8MB
6'b001000	16MB
6'b001001	32MB
6'b001010	64MB
6'b001011	128MB
6'b001100	256MB
6'b001101	512MB
6'b001110	1GB
6'b001111	2GB
6'b010000	4GB
6'b010001	8GB
6'b010010	16GB
6'b010011	32GB
6'b010100	64GB
6'b010101	128GB
6'b010110	256GB
6'b010111	512GB
6'b011000	1TB
6'b011001	2TB
6'b011010	4TB
6'b011011	8TB
6'b011100	16TB
6'b011101	32TB
6'b011110	64TB
6'b011111	128TB
6'b100000	256TB

2.19.3 Example memory map programming

This section describes an example memory map and how to program it in the RN SAM and HN-F SAM.

The following figure shows an example memory map with 1024GB addressable size. It is based on the Arm 40-bit proposed address map. It has three separate DRAM regions (from 2-4GB, 34-64GB and 544-1024GB) and four I/O regions, which must be mapped to specific targets. It is assumed that the I/O region 256-512GB is unused and no requests are sent to this address.

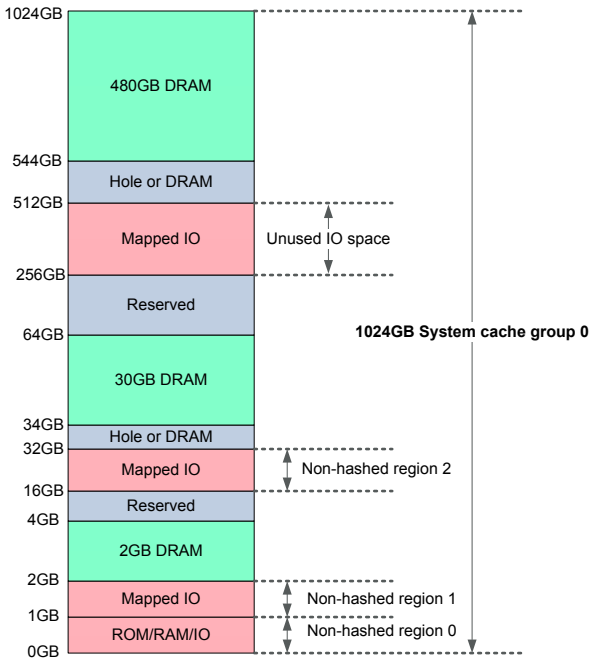


Figure 2-33 CMN-600 example memory map

Assuming we have eight HN-Fs in the system and all HN-Fs are being used for one SCG (group 0), use the following steps to program the RN SAM.

- Since the DRAM regions are non-contiguous and we are assigning the entire DRAM space to one system cache group, it is ideal to map the full 1024GB memory map to the system cache group.
- Each of the non-hashed regions can then be carved out of the full 1024GB memory map as shown in the above figure and assigned to individual non-hashed targets.
- Once the RN SAM programming is done, we need to turn ON the region-based target ID selection by disabling the default mode of the RN SAM.

The following table shows the RN SAM registers and the corresponding programmed values.

Table 2-37 RN SAM registers and programmed values

Register name	Field name	Value	Description
sys_cache_grp_region_reg0	region0_base_address	`0x0_0000`	Base address [47:26]
	region0_size	`5'b01110`	1024GB size
	region0_target_type	`2'b00`	HN-F target type
	region0_valid	`1'b1`	Region 0 is valid
sys_cache_grp0_nodeid_reg0	nodeid_0	<hnf0_node_id>	Physical node IDs of the HN-Fs in the system from HN-F 0 to HN-F 7
	nodeid_1	<hnf1_node_id>	
	nodeid_2	<hnf2_node_id>	
	nodeid_3	<hnf3_node_id>	
sys_cache_grp0_nodeid_reg1	nodeid_4	<hnf4_node_id>	
	nodeid_5	<hnf5_node_id>	
	nodeid_6	<hnf6_node_id>	
	nodeid_7	<hnf7_node_id>	

Table 2-37 RN SAM registers and programmed values (continued)

Register name	Field name	Value	Description
sys_cache_group_hnf_count	scg0_num_hnf	0x08	Total of eight HN-Fs in this system cache group
non_hash_mem_region_reg0	region0_base_address	0x0_0000	1GB from [47:26] 0x0_0000_0000
	region0_size	5'b00100	1GB size
	region0_target_type	2'b01	HN-I target type
	region0_valid	1'b1	Region 0 is valid
	region1_base_address	0x0_0010	1GB region from 0x0_4000_0000
	region1_size	5'b00001	1GB size
	region1_target_type	2'b01	HN-I target type
	region1_valid	1'b1	Region 1 is valid
non_hash_mem_region_reg1	region2_base_address	0x0_0100	16GB region from 0x4_0000_0000
	region2_size	5'b01000	16GB size
	region2_target_type	2'b01	HN-I target type
	region2_valid	1'b1	Region 2 is valid
non_hash_tgt_nodeid0	nodeid_0	<hni0_node_id>	Node ID of HN-I 0 corresponding to non-hashed region 0
	nodeid_1	<hni1_node_id>	Node ID of HN-I 1 corresponding to non-hashed region 1
	nodeid_2	<hni2_node_id>	Node ID of HN-I 2 corresponding to non-hashed region 2
rnsam_status	nstall_req	1'b1	Unstall any operations that are dependent on SAM programming.
	default_target	1'b0	Disable default mode and use the programmed ranges for new incoming addresses.

Similarly to RN SAM, HN-F SAM must also be programmed so that it can select the correct SN-F target ID. All HN-F SAMs within SCG 0 must have the same programming as shown in the following table, including the attributes of each SN-F.

Table 2-38 HN-F programming information

Register name	Field name	Value	Description
por_hnf_sam_control	hn_cfg_sn0_nodeid	<sn0_node_id>	Node ID of SN-F 0
	hn_cfg_sn1_nodeid	<sn1_node_id>	Node ID of SN-F 1
	hn_cfg_sn2_nodeid	<sn2_node_id>	Node ID of SN-F 2
	hn_cfg_three_sn_en	1'b1	Enable 3-SN
	hn_cfg_sam_top_address_bit0	39	Bit 39 of address
	hn_cfg_sam_top_address_bit1	36	Bit 36 of address
	hn_cfg_sam_inv_top_address_bit	1'b1	Invert top address bit

2.19.4 Support for CCIX Port Aggregation

RN-SAM supports *CCIX Port Aggregation* (CPA).

Requests from an RN to a remote chip can be striped across multiple CCIX gateway blocks based on address bits. The following figure shows this functionality.

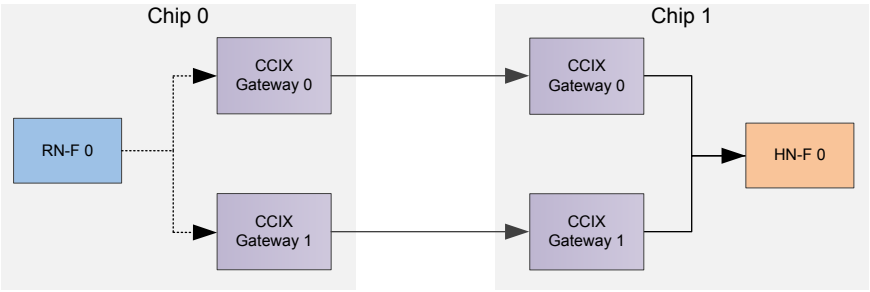


Figure 2-34 RN SAM CCIX Port Aggregation

This striping is achieved by hashing physical address bits[47:6]. The RN-SAM CCIX can hash incoming addresses across two or four gateway blocks forming a CCIX Port Aggregation Group (CPAG). RNSAM can support up to two such CPAGs. RN-SAM also has an address mask for each CPA which can be used to remove certain bits from the hashing. For example, to stripe the incoming address at 512B granularity, the address mask bits[47:6] can be set to `42'3FFFFFFFF8`. With this mask setup, the logical operator AND is applied to all incoming addresses before hashing the address bits. See the RN SAM registers for details on programming.

HN-F support for CCIX Port Aggregation

HN-F also supports CPA for snoop requests going to a remote chip. HN-F uses the same hashing as RN SAM so that a given address always goes to the same CCIX gateway block. HN-F uses the RN-F's ID to determine if CPA is enabled. Please refer to the logical to physical ID conversion registers in HN-F to enable CPA for each RN-F's ID.

Guidelines for enabling CPA in RN SAM and HN-F

Certain rules apply when enabling the CPA in RN SAM and HN-F:

- The CPA is only applicable to SCG and non-hashed ranges.
- Each non-hashed memory range can be explicitly enabled to use CPA or use a single non-hashed target ID.
- Each SCG's targetID can be explicitly enabled to be use CPA.
- The HN-F, when participating as a CPA target for traffic from a remote RN-F, must not receive non-CPA traffic from the same remote RN-F (that is, an RN-F cannot send CPA and non-CPA traffic to the same remote HN-F).
- Each SCG in RN-SAM may contain only one CPA group along with local HN-F target IDs.

CPA programming sequence

Both RN-SAM and HN-F SAM must be programmed to enable CPA.

RN SAM CPA programming sequence:

1. Each non-hashed memory region in the RN SAM has a corresponding Port Aggregation enable bit in **cml_port_aggr_mode_ctrl_reg**. If a non-hashed memory region belonging to a remote chip is required to use CPA, then the corresponding enable bit (**region<n>_pag_en**) must be set to `1'b1`.
2. CPA hashes address bits [47:6] to distribute the traffic between the CCIX gateways. If certain bits are not to be used in the hashing, the **cml_port_aggr_grp0_add_mask** register must be programmed accordingly. Write `1'b0` to the corresponding address bit in the mask.
3. The number of CCIX ports (CCIX gateways) must be programmed in **cml_port_aggr_grp<m>_reg.num_cxg_pag0**. The CCIX gateway's CHI node ID must be programmed in the same register's **pag0_tgtid** field. If two CCIX gateways are being used, then both node IDs must be programmed in this register. This programming is used by all regions that have CPA enabled.
4. Repeat the above steps for all RN SAMs in the chip.

To determine if CPA is enabled, RN SAM uses the address ranges and HN-F SAM uses the RN-F's logical ID. As explained in *2.23 Cross chip routing and ID mapping* on page 2-134, HN-F contains the *Logical ID* (LDID) to physical node ID conversion table as shown in *Table 2-48 Example program* on page 2-137 in the Example Programming table. This table, along with the CHI node ID and valid fields, also contains **remote**, **cpa_en**, and **cpa_grpid** bits. By using these bits, HN-F can determine if the RN-F is enabled to use CPA, and sends the snoops through appropriate ports by hashing the address bits.

Note

The CPA group ID control bits for non-hash region 7 are aligned differently from other regions. Refer to **region7_pag_grpip** field's index in the **cml_port_aggr_mode_ctrl_reg**.

HN-F SAM CPA programming sequence:

1. For each valid LDID in the system, the **nodeid_ra<ldid>**, **remote_ra<ldid>**, and **cpa_en_ra<ldid>** fields must be programmed in the **por_hnf_rn_phys_id<n>** registers. If the RN-F is a remote requestor, the **remote** bit set to `1'b1`. If CPA is enabled for a remote RN-F, the **cpa_en** bit must be set to `1'b1`. Local RN-F LDIDs must have the **remote** and **cpa_en** bits must be set to 1'b0 and the corresponding CPA Group ID set to 1'b0.
2. CPA hashes address bits [47:6] to distribute the traffic between the CCIX gateways. If certain bits are not to be used in the hashing, the **por_hnf_cml_port_aggr_grp<m>_add_mask** register must be programmed accordingly. Write `1'b0` to the corresponding address bit in the mask.
3. The number of CCIX ports (CCIX gateways) must be programmed in **por_hnf_cml_port_aggr_grp<m>_reg.num_cxg_pag0**. All of the CCIX gateway's CHI node ID belonging to this group must be programmed in the same register's **pag<k>_tgtid** field. This programming is used by all remote RN-Fs that have CPA enabled.
4. When CPA is enabled, the **por_hnf_rn_phys_id<n>.nodeid_ra<ldid>** must be programmed to match the corresponding CPA group's **por_hnf_cml_port_aggr_grp<m>.pag0_tgtid** field.
5. Repeat the above steps for all HN-F SAMs in the chip.

In a two-chip system with CPA enabled, Chip 0's RN SAM CPA mask and Chip 1's HN-F SAM CPA mask must be programmed to match. Similarly, Chip 1's RN SAM CPA mask must match Chip 0's HN-F SAM CPA mask.

2.20 RN and HN-F SAM R2 Support

CMN-600 RN and HNF SAM support additional features when the R2 configuration parameter is enabled.

The features include:

- Secondary memory regions for each *System Cache Group* (SCG).
- Masking of address bits for hashing and range compare
- 64-HNF with CAL support in the RN SAM
- Masking of address bits in the HN-F SAM region compare and hashing

Secondary Memory Regions for System Cache Groups

Each SCG will support two memory regions. If the incoming address matches either of the two programmed, valid regions, the RN SAM will select the corresponding SCG's target ID from the target ID table.

Limitations:

- Secondary memory region sizes must be size aligned, power of two-sized.
- If the primary region for a SCG is set to be in non-hashed mode, the secondary region will also be in non-hashed mode.

Address bit masking

RN SAM will provide support for masking of address bits used for range compare and address hashing. This can be enabled by programming the **rnsam_hash_addr_mask_reg** and **rnsam_region_cmp_addr_mask_reg** registers.

RN SAM uses all address bits [47:26] for hashed and non-hashed memory regions, [47:16] for GIC memory region when comparing the incoming address against the programmed ranges. By programming select bits to 1'b0 in the mask register rnsam_region_cmp_addr_mask_reg, the incoming address and the programmed address ranges can be masked off before comparison. This region mask is applied to hashed, non-hashed and GIC memory regions.

RN SAM hashes all address bits [47:6] to equally distribute the requests across all target devices HN-F and SN-F. By programming select bits in the address mask register rnsam_hash_addr_mask_reg to 1'b0, those address bits can be removed from the hashing logic. This feature is only applicable to hashed memory regions.

Limitations:

- If 3 SN or 6SN mode is enabled, address bits [16:7] and the top_addr_bits are essential in distributing the addresses between memory. It is recommended that these bits are masked carefully to avoid memory aliasing.
- Range compare mask must not mask off bits that represent the size of the region. For example, if any of the region size is 64Mbytes, address bit 26 cannot be masked. Similarly, if a region size is 512MB, address bit 29 cannot be masked.
- The address bits masked in HN-F and RNSAM must be consistent. This ensures that PrefetchTgt requests from an RN-F to SN-F are addresses by the same SN-F as SLC miss from the HN-F to SN-F.

64-HNF with CAL support in the RN SAM

CMN-600 R2 system supports pairing of two HN-F's at a MXP port using CAL. The HN-F NODE ID's that are paired at the CAL are only differentiated using the device ID (NodeID[1:0]) field in the node ID as described in *2.4 Node ID mapping* on page 2-51.
RN SAM depends on this NODE ID scheme to support hashing of addresses over twice the number of HN-F's using the existing hashed target ID programming table.
For example, If a system cache group is programmed to have 4 HN-F's and HN-F CAL mode for this region is enabled, the RNSAM will generate 8 unique target ID's as shown here:
Number of bits in select: 3
select[0] = (6^9^12^15^18^21^24^27^30^33^36^39^42^45)
select[1] = (7^10^13^16^19^22^25^28^31^34^37^40^43^46)
select[2] = (8^11^14^17^20^23^26^29^32^35^38^41^44^47)

Bits select[1:0] are used to pick between the programmed 4 HN-F target IDs. Bit select[2] is used to override the "device ID" field as shown here:

Target NodeID[10:0] = {hash_nodeID_pick[10:1], hash_nodeID_pick[0] ^ select[2]}.

Limitations:

- This feature must only be used when the target HN-F are paired using CAL
- RN SAM will not apply this method to SN-F target IDs. For fully utilizing the benefit of the CHI-B PrefetchTarget operations to SN-F, the paired HN-Fs must always be mapped to same SN-F or group of SN-F's if 3SN/6SN hashing id used.
- Only one HN-F ID from each CAL group must be programmed in the RNSAM hashed target ID registers.

RNSAM register **sys_cache_grp_cal_mode_reg** contains the CAL mode enable bit for each system cache group. For example, to enable the CAL_Mode for System Cache Group 0, write 1'b1 to bit index [0] of this register.

HN-F SAM R2 support

HN-F SAM uses all address bits [47:26] when comparing the incoming address against the programmed ranges. By programming select bits to 1'b0 in the mask register **hnf_sam_region_cmp_addr_mask_reg**, the incoming address and the programmed address ranges can be masked off before comparison. This region mask is only applicable to region based memory partitioning in the HN-F and hence the mask is not applied to the hashing scheme in 3SN and 6SN modes.

Address bit masking

HNF SAM supports masking of address bits used for 3SN or 6SN address hashing. This can be enabled by programming the hn_sam_hash_addr_mask_reg.

Limitations:

- Range compare mask must not mask off bits that represent the size of the region. For example, if any of the region size is 64 MB, address bit 26 cannot be masked. Similarly, if a region size is 512MB, address bit 29 cannot be masked.
- If 3SN or 6SN mode is enabled, address bits [16:7] and the top_addr_bits are essential in distributing the addresses between memory. It is recommended that these bits are masked carefully to avoid memory aliasing.

2.21 RN and HN-F SAM R3 Support

CMN-600 RN and HNF SAM support additional features when the R3 configuration parameter is enabled.

64 hashed targets in RN SAM: R2 revision of the RN-SAM supported a maximum of 32 hashed target ID and 32 SN target IDs. With HN-F CAL mode, it supported hashing of addresses across 64 hashed target IDs. This feature has been extended to support 64 hashed HN-F and SN-F target IDs. This allows to have 64 unique hashed target ID's in the RN-SAM SCG target ID registers as shown in the following table.

Table 2-39 RN-SAM SCG target ID registers

SCG target ID Regs (64 hashed targets)	Number of HN-Fs per SCG				
	64 (CMN600 R3)	32	16	8	4,2,1
CAL MODE?	No	Yes (CMN600 R2)	Yes (CMN600 R2)	Yes (CMN600 R2)	Yes (CMN600 R2)
scg_nodeid_reg0	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs	SCG0_NIDs
scg_nodeid_reg1					-
scg_nodeid_reg2				-	-
scg_nodeid_reg3				-	-
scg_nodeid_reg4			SCG1_NIDs	SCG1_NIDs	SCG1_NIDs
scg_nodeid_reg5					-
scg_nodeid_reg6				-	-
scg_nodeid_reg7				-	-
scg_nodeid_reg8		SCG2_NIDs	SCG2_NIDs	SCG2_NIDs	SCG2_NIDs
scg_nodeid_reg9					-
scg_nodeid_reg10				-	-
scg_nodeid_reg11				-	-
scg_nodeid_reg12			SCG3_NIDs	SCG3_NIDs	SCG3_NIDs
scg_nodeid_reg13					-
scg_nodeid_reg14				-	-
scg_nodeid_reg15				-	-

20 non-hashed regions in RN-SAM: R2 revision of the RN-SAM supported 8 non-hashed regions. This feature has been extended to support 20 unique non-hashed regions.

Note

There will be an additional cycle latency for RN-SAM lookup in the XP on the request flit when 20 non-hashed regions are present.

CPAG programming in RN-SAM

Each of the non-hashed and SCG region can be selectively enabled to use CPAGs.

The fields to enable CPAG are described in the following table.

Table 2-40 RN-SAM CPAG registers

Region Type	Register name	Fieldname	Width	Description
SCG (Hashed)	sys_cache_grp_hn_cpa_en_reg	hash_cpa_en	64 bits	CPA enable: Each bit represents the hashed target ID in CMN600 TRM Table 2-24 Target ID programming table
	sys_cache_grp_hn_cpa_grp_reg	cpa_grp_scgX	2 bits	CPA group: 2 bits per SCG to program the CPAG ID.
Non-hashed	cml_port_aggr_mode_ctrl_reg	regionX_pag_en	1 bit	CPA enable: 1 bit per Non-hashed region to enable CPAG
	cml_port_aggr_mode_ctrl_reg	regionX_pag_grpid	2 bits	CPA group: 2 bits per non-hashed region to program the CPAG ID.

Where ‘X’ in RNSAM CPAG registers represent the region number.

As shown in the table, the CPA enable and CPA group ID must be programmed for each region to enable CPAG. For SCG, the CPA enable is per hashed target ID as the memory region could be hashed across 2 chips. In such a case, only the hashed target ID representing the remote chip will have CPA enable bit set to 1’b1. Hashed target ID representing the local HN, must be 1’b0.

CPAG programming in HN-F SAM

Similar to RN-SAM, HN-F has CPAG registers which must be programmed.

This is required for Snoops from HN-F to use the same CXHA port for a given address as any new incoming request as described in the following table.

Table 2-41 RN-SAM CPAG registers

Register name	Fieldname	Width	Description
Por_hnf_rn_phys_idX	cpa_en_raN	1 bit	CPA enable: Enables the CPA mode for each remote logical device ID
	cpa_grp_raN	2 bits	CPA group: 2 bits per logical device ID

Where ‘X’ in the RN-SAM CPAG registers represents the register number and ‘N’ represents the logical device ID.

2.22 HN-I SAM

HN-I SAM maps the incoming address to a target endpoint that is connected downstream behind HN-I. This process simplifies endpoint mapping and corresponding ordering to downstream endpoint address space.

——— **Note** ———

The endpoint here refers to either a peripheral with memory-mapped I/O space, such as UART or GPIO, or a physical memory, such as SRAM or FLASH.

———————————

HN-I SAM provides the capability to program and configure up to three non-overlapping address regions within its endpoint address space: Address Region 1, Address Region 2 and Address Region 3. The default address region, Default Region or Address Region 0, encompasses all HN-I address space that is not configured using the Address Region {1, 2, 3} configuration registers.

——— **Note** ———

This section uses the terms Default Region and Address Region 0 interchangeably.

———————————

Each address region can be programmed to be either peripheral memory or physical memory. By default, each address region is mapped to peripheral memory unless explicit programmed to be physical memory. Address regions mapped as peripheral memory follows device memory ordering guarantees while those mapped as physical memory follows normal memory ordering guarantees. The attributes of incoming transactions to HN-I do not change these ordering guarantees.

——— **Note** ———

If the address region is mapped to peripheral memory, it can be further divided into smaller address spaces known as order regions. An order region is configured per address region. An order region in HN-I address space is an address granularity within which the peripheral memory ordering is maintained.

———————————

The minimum address granularity for an address region or order region is 4KB. This size is equivalent to the minimum slave address space granularity in AXI/ACE-Lite. Therefore, the base address in the Address Region {1, 2, 3} registers only includes bits [REQ_ADDR_WIDTH-1:12].

To summarize, HN-I SAM provides the capability to program and configure:

- Address regions: one to three.
- Order regions: one configurable size per address region.

In summary:

- Address Regions 1, 2, and 3 cannot overlap.
- All endpoint address space that does not fall under Address Regions 1, 2, or 3 is considered Default Region.
- The order region size within any address region can be configured to `6'b111111` to enforce strict ordering for that specific address region.
- If address region is programmed as physical memory, order region programming function output doesn't matter, as the entire address region follows normal memory ordering guarantees.

Configuration requirements

1. HN-I SAM can only be programmed during boot process.
2. A given HN-I SAM region register must not be enabled if the new requests, that can potentially fall into the newly configured address region and/or order region require ordering with respect to the existing outstanding requests.

Configuration registers

The Address Region 0 register (**por_hni_sam_addrregion0_cfg**) is always valid; no valid bit is defined for this register unlike the Address Region {1, 2, 3} registers. By default, without any prior SAM programming, the entire address space of a given HN-I is mapped to the Default Region and all transactions to this region are kept in order. The default order region size in Address Region 0 is `6'b111111`, which covers the entire HN-I address space. This is the same as configuring the order region size to:

>=`6'b100100` (for REQ_ADDR_WIDTH = 48), or

>=`6'b100000` (for REQ_ADDR_WIDTH = 44)

The following table shows the register bit assignments for **por_hni_sam_addrregion0_cfg**.

Table 2-42 por_hni_sam_addrregion0_cfg bit assignments

Bit field	Width	Default	Field name	Description
5:0	6	`6'b111111`	order_reg_size	<n>; used to calculate Order Region 0 size within Address Region 0 (2^n × 4KB). Example: For n=`0x08`, order region size is 2^8 × 4KB=1MB.
58:58	1	`1'b0`	physical_mem_en	Used to map this address region to physical memory.
59:59	1	`1'b0`	ser_all_wr	Used to serialize all writes within Address Region 0.
60:60	1	`1'b0`	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 0.
61:61	1	`1'b1`	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 0; used to improve ordered read performance.
62:62	1	`1'b1`	pos_early_wr_comp_en	Enables Early Write Acknowledgment in Address Region 0; used to improve write performance.

The following table shows the register bit assignments for the Address Region {1, 2, 3} configuration registers (**por_hni_sam_addrregionX_cfg** where X={1, 2, 3}).

Table 2-43 por_hni_sam_addrregionX_cfg bit assignments

Bit field	Width	Default	Field name	Description
5:0	6	`6'b0`	order_reg_size	<n>; used to calculate Order Region X size within Address Region X (2^n × 4KB). Example: For n=`0x08`, order region size is 2^8 × 4KB=1MB.
15:10	6	`6'b0`	addr_region_size	<n>; used to calculate Address Region X size (2^n × 4KB). CONSTRAINT: Resultant size must be less than or equal to 2^(address width). Example: For n=`0x10`, address region size is 2^{16} × 4KB=256MB.
55:20	36	`36'b0`	base_addr	Address Region X base address [REQ_ADDR_WIDTH-1:12]. CONSTRAINT: Must be aligned to Address Region X size. Example: For an address region size of 256MB, base address can be `0x0`, `0x0000_1000_0000`, `0x0000_2000_0000`, `0x0000_3000_0000`, `0x0000_4000_0000`, etc.
58:58	1	`1'b0`	physical_mem_en	Used to map this address region to physical memory.

Table 2-43 por_hni_sam_addrregionX_cfg bit assignments (continued)

Bit field	Width	Default	Field name	Description
59:59	1	1'b0	ser_all_wr	Used to serialize all writes within Address Region X.
60:60	1	1'b0	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region X.
61:61	1	1'b1	pos_early_rdack_en	Enable sending early read receipts from HN-I in Address Region 0, used to improve ordered read performance.
62:62	1	1'b1	pos_early_wr_comp_en	Enables Early Write Acknowledgment in Address Region X; used to improve write performance.
63:63	1	1'b0	valid	Address Region X fields are programmed and valid.

This section contains the following subsection:

- *2.22.1 Sample system configuration* on page 2-126.

2.22.1 Sample system configuration

This section describes a sample system configuration for HN-I SAM with Address Region 1, Address Region 2, and Address Region 3, as well as order regions within Address Region {0, 1, 2, 3}.

The following figure shows the high-level configuration of the address space and the base addresses of each address region.

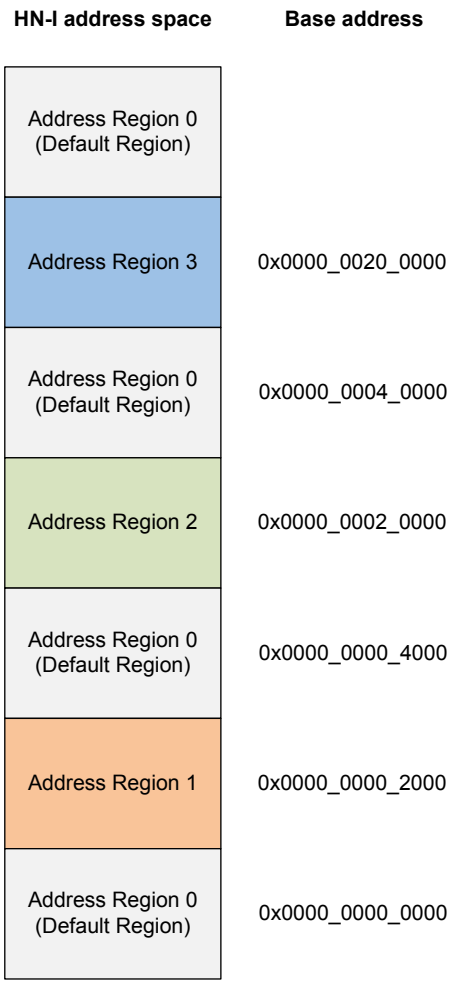


Figure 2-35 HN-I address space example

Configurable parameters

In this example, the following configurable parameters are used:

Address Region 0

The following figure shows the sample configuration for Address Region 0.

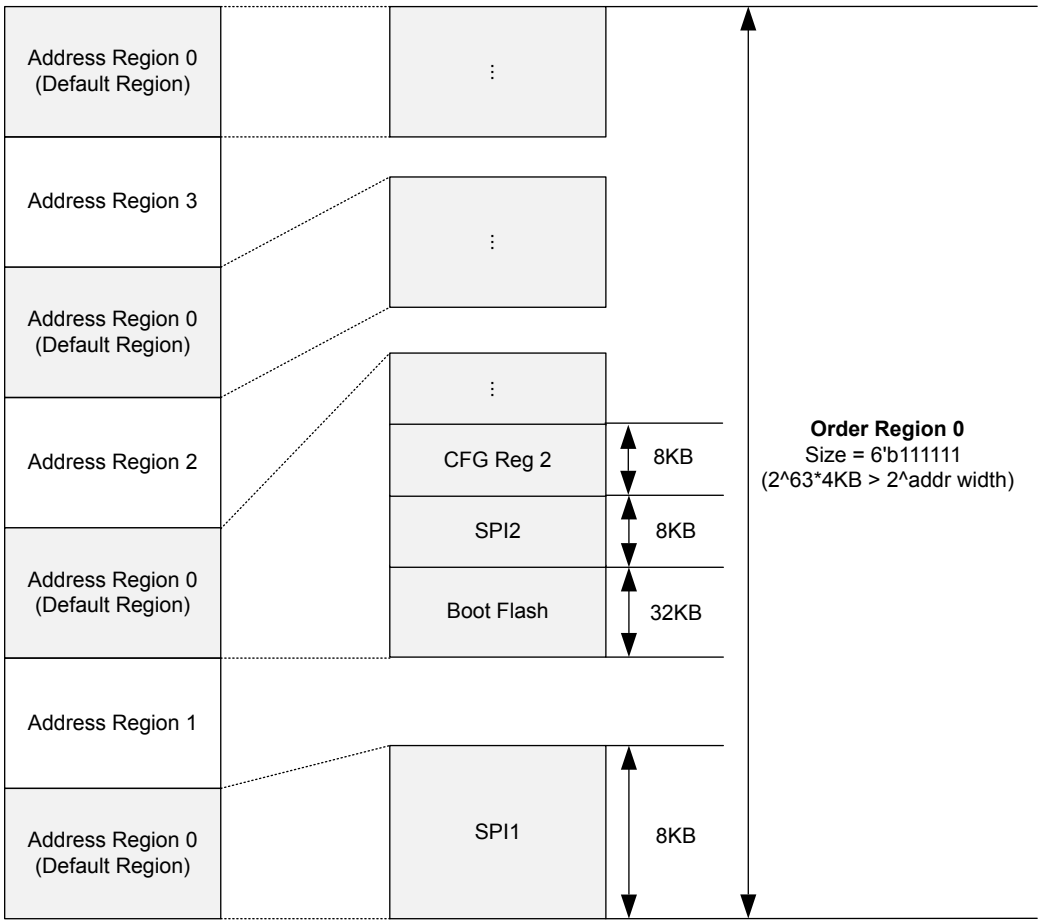


Figure 2-36 Address Region 0 sample configuration

Address Region 0 encompasses any I/O space that does not map to Address Region {1, 2, 3}. The size of the maximum peripheral address space in Address Region 0 is 32KB (Boot Flash). Requests targeting this Boot Flash must be kept in order. By configuring Order Region 0's size to 32KB, requests with addresses that are within the range `0x0000_0000_0000` to `0x0000_0000_8000` are ordered. However, since Boot Flash is not aligned to the 32KB boundary (`0x0000_0000_4000` to `0x0000_0000_C000`), requests may be out of order and create an issue. In order to ensure all requests to Boot Flash are ordered, Order Region 0's size must be configured to at least 64KB. In this configuration, requests to SPI1, SPI2, and CFG Reg 2 are also ordered with respect to requests to Boot Flash, potentially impacting performance. Instead, Address Region 0 can have a SAM with Boot Flash aligned to the 32KB boundary and Order Region 0's size can be configured to 32KB.

Address Region 1

The following figure shows the sample configuration for Address Region 1.

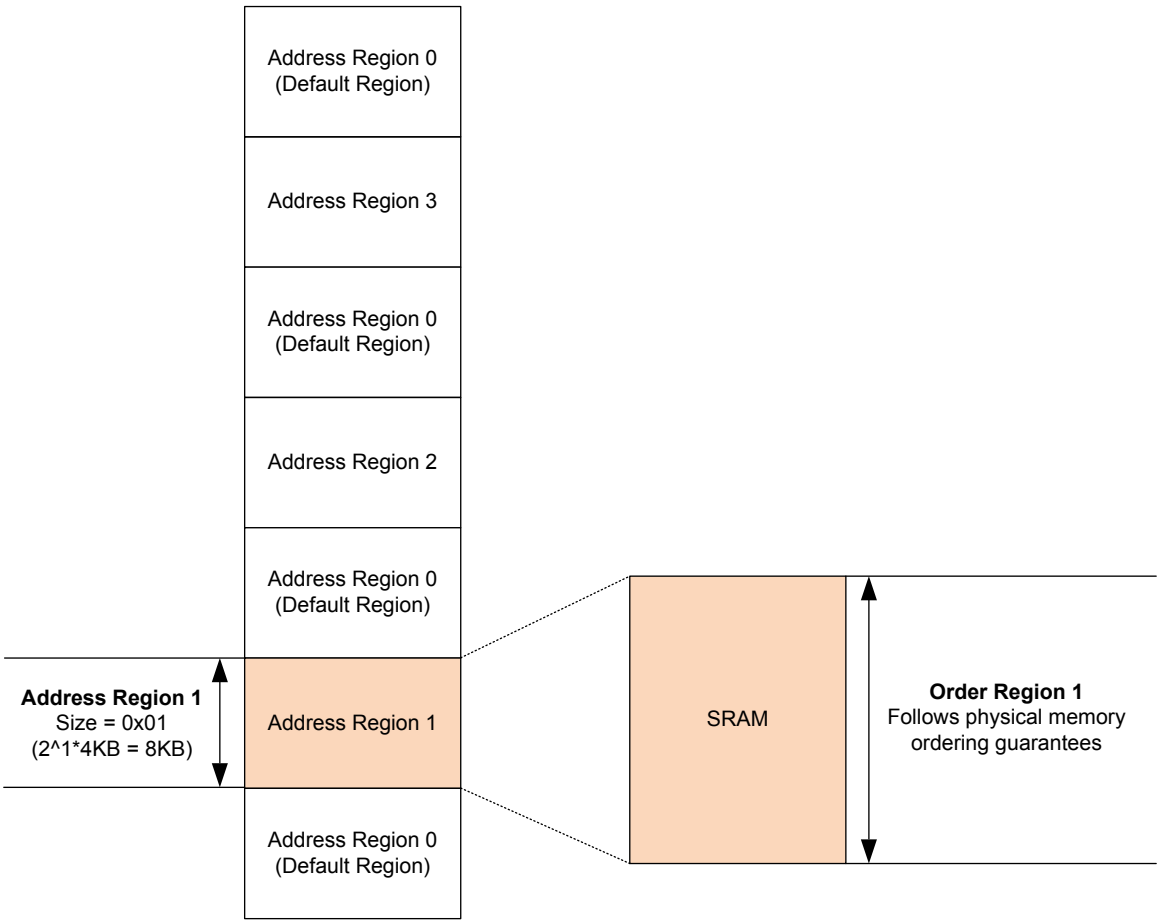


Figure 2-37 Address Region 1 sample configuration

Address Region 1 starts at base address `0x0000_0000_2000` and is 8KB in size. This region is mapped as physical memory as there is SRAM behind this region. The entire Address Region 1 is considered as one order region. Therefore, ordering is maintained between all requests to overlapping cacheline region (64B).

Address Region 2

The following figure shows the sample configuration for Address Region 2.

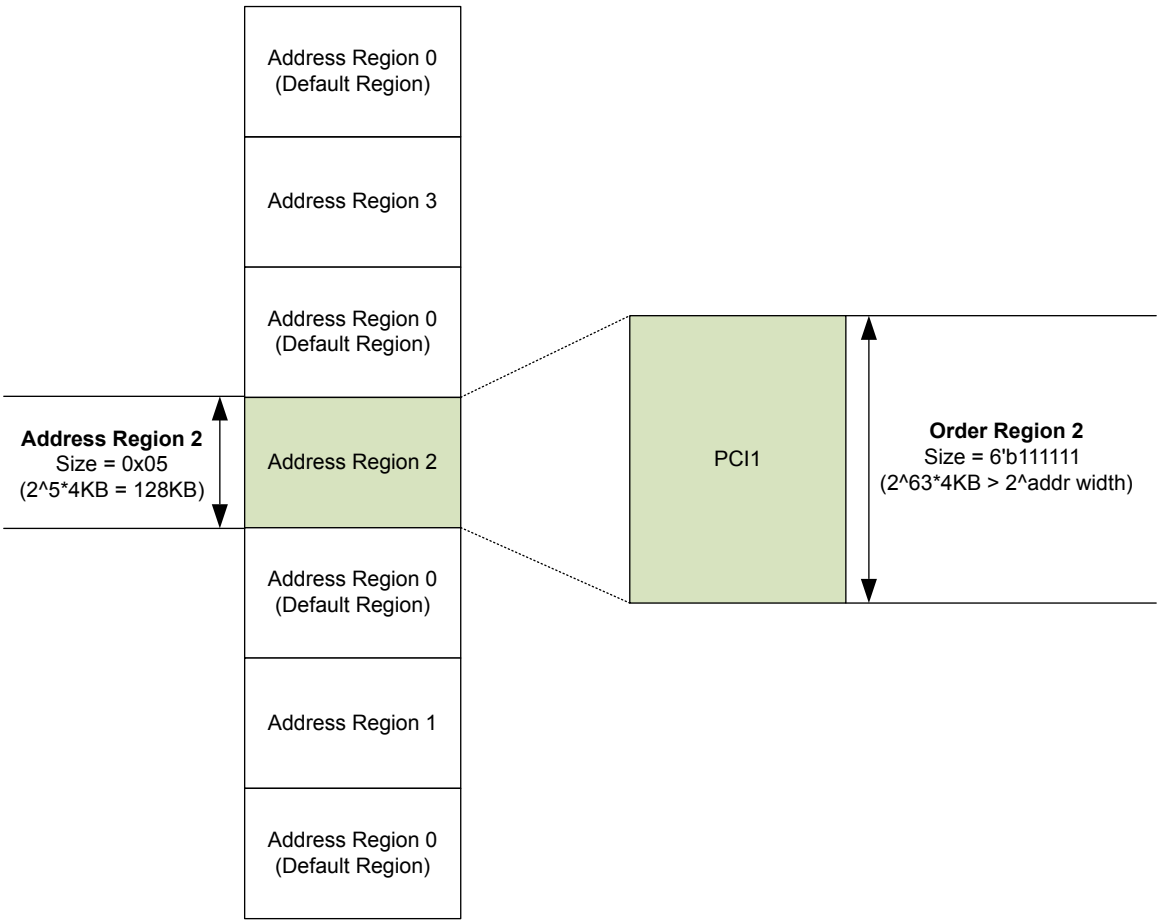


Figure 2-38 Address Region 2 sample configuration

Address Region 2 starts at base address `0x0000_0002_0000` and is 128KB in size. Order Region 2's size (2^{63} × 4KB) is configured to the maximum value (`6'b111111`), so Address Region 2 is considered as one order region. PCI1 occupies the entire order region, so all PCI1 requests are ordered.

Address Region 3

The following figure shows the sample configuration for Address Region 3.

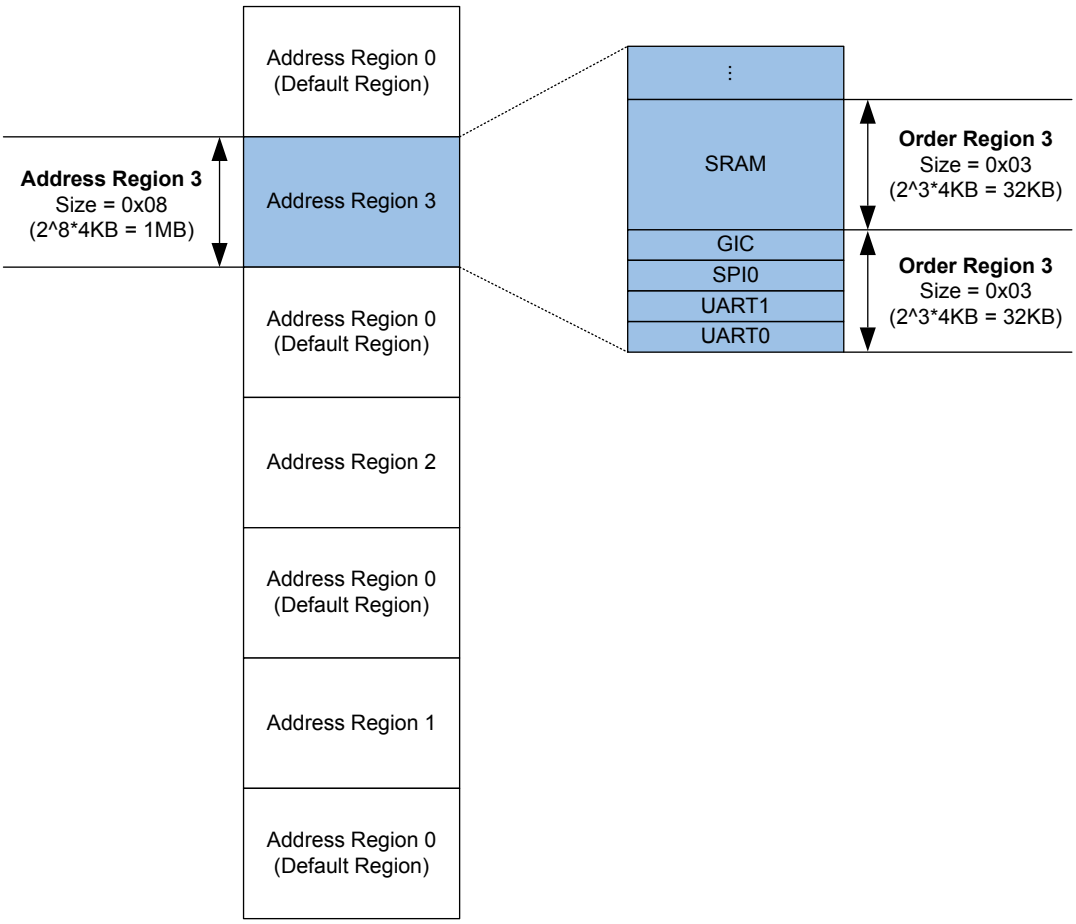


Figure 2-39 Address Region 3 sample configuration

Address Region 3 starts at base address `0x0000_0020_0000` and is 1MB in size. Order Region 3's size (32KB) is less than Address Region 3's size (1MB), resulting in a total of 32 order regions. GIC, SPI0, UART1, and UART0 map to one order region, so all requests to these peripherals are ordered. SRAM also maps to one order region, so all requests to SRAM are ordered. Since SRAM maps to a separate order region from GIC, SPI0, UART1, and UART0, requests to SRAM and requests to GIC, SPI0, UART1, and UART0 are not ordered.

For the above example, HN-I SAM configuration registers (**por_hni_sam_addrregionX_cfg** where X={0, 1, 2, 3}) are programmed as follows:

Table 2-44 Address Region 0 configuration

Bit field	Width	Field name	Configured value
5:0	6	order_reg_size	`6'h4`
58:58	1	physical_mem_en	`1'b0`
59:59	1	ser_all_wr	`1'b0`
60:60	1	ser_devne_wr	`1'b0`
61:61	1	pos_early_rdack_en	`1'b1`
62:62	1	pos_early_wr_comp_en	`1'b1`

Table 2-45 Address Region 1 configuration

Bit field	Width	Field name	Configured value
5:0	6	order_reg_size	6'h1
15:10	6	addr_region_size	6'h1
55:20	36	base_addr	36'h0000_0000_2
58:58	1	physical_mem_en	1'b1
59:59	1	ser_all_wr	1'b0
60:60	1	ser_devne_wr	1'b0
61:61	1	pos_early_rdack_en	1'b1
62:62	1	pos_early_wr_comp_en	1'b1
63:63	1	valid	1'b1

Table 2-46 Address Region 2 configuration

Bit field	Width	Field name	Configured value
5:0	6	order_reg_size	6'b111111
15:10	6	addr_region_size	6'h5
55:20	36	base_addr	36'h0000_0002_0
58:58	1	physical_mem_en	1'b0
59:59	1	ser_all_wr	1'b0
60:60	1	ser_devne_wr	1'b0
61:61	1	pos_early_rdack_en	1'b1
62:62	1	pos_early_wr_comp_en	1'b1
63:63	1	valid	1'b1

Table 2-47 Address Region 3 configuration

Bit field	Width	Field name	Configured value
5:0	6	order_reg_size	6'h3
15:10	6	addr_region_size	6'h8
55:20	36	base_addr	36'h0000_0020_0
58:58	1	physical_mem_en	1'b0
59:59	1	ser_all_wr	1'b0
60:60	1	ser_devne_wr	1'b0
61:61	1	pos_early_rdack_en	1'b1
62:62	1	pos_early_wr_comp_en	1'b1
63:63	1	valid	1'b1

Note

The following attributes are kept as default value:

- **ser_all_wr**
- **ser_devne_wr**
- **pos_early_wr_comp_en**
- **pos_early_rdack_en**

2.23 Cross chip routing and ID mapping

IDs are generated and used to route protocol messages across multiple chips.

Cross chip routing and ID mapping

This section covers ID generation and methods used to route CCIX protocol messages across multiple chips. RA SAM-related acronyms include:

- *CCIX Request Agent ID* (RAID).
- *CCIX Home Agent ID* (HAID).
- *Logical Device ID* (LDID).

LDIDs are uniquely assigned within a device type. For example, RN-Fs in the system could be assigned LDIDs 0-n, while RN-Is could be assigned LDIDs 0-m, and RN-Ds could be assigned LDIDs 0-k.

The following rules apply:

- RAID usage:
  - Is confined to CCIX gateway devices only.
  - All non-CCIX CMN-600 components use and operate on sequentially assigned LDIDs. CXG devices bidirectionally map each CCIX RAID to an LDID.
- RN-F LDID assignment:
  - Local RN-Fs are assigned LDIDs from 0-n, sequentially.
  - Remote RN-Fs must be assigned LDIDs n+1 and above by the discovery software.

A basic block diagram is shown in the following figure.

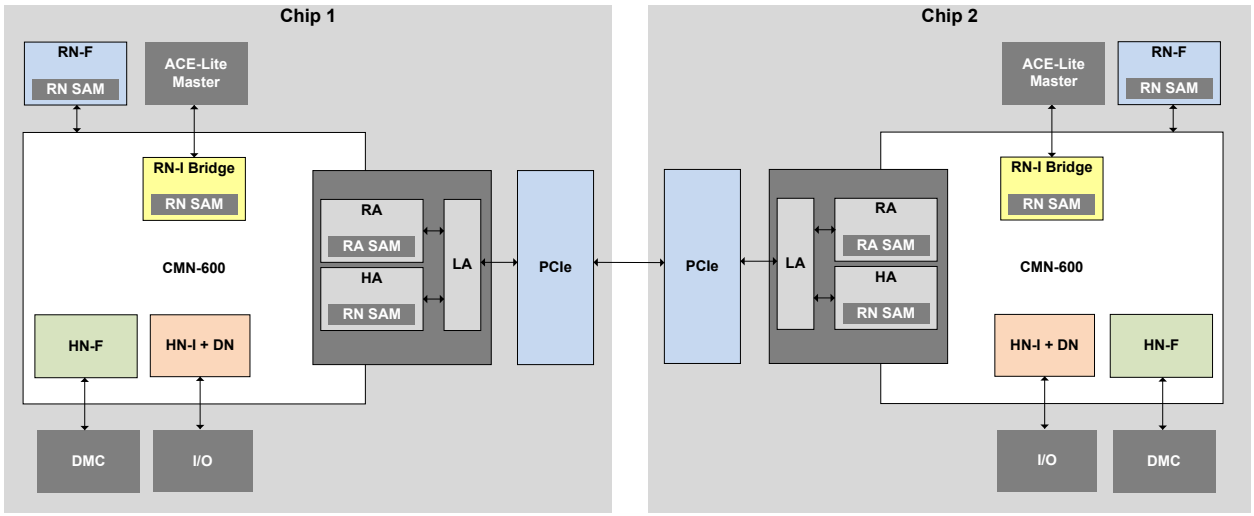


Figure 2-40 RA SAM block diagram

Request from an RN-F to a remote HN-F

The following figure shows all IDs generated and used to route a request from a local RN-F on Chip 1 to a remote HN-F on Chip 2.

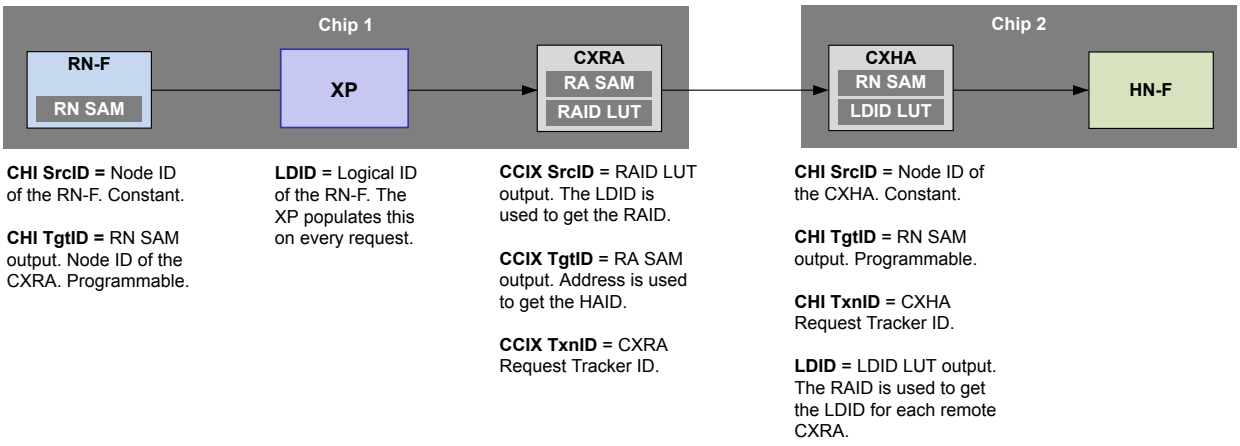


Figure 2-41 RN-F to remote HN-F IDs

The flow for this process is as follows:

- The RN-F looks up the programmable RN SAM to populate the CHI target ID on a request.
- The XP populates the RN-F LDID on this request.
- RN-Is and RN-Ds are internal to CMN-600 and get their logical ID assigned during CMN-600 generation. The RN-I or RN-D sends this LDID on every request.
- The CXRA contains programmable lookup tables, RAID LUTs, for each class of local RN (RN-F, RN-I, and RN-D). CCIX discovery software discovers all local RN-Fs, RN-Ds, and RN-Is, and programs their corresponding RAIDs in these LUTs. The LDID of the incoming request is used to look up these RAID LUTs and determine the CCIX RAID. CXRA also has CCIX RA SAM. This CCIX RA SAM is used to generate the HAID. This HAID is used as the target ID to route the CCIX request message.
- The LDID's for local RN-F's must not be changed. The build-time LDID assignments are discovered by reading any one of the HN-F **por_hnf_rn_physid** registers. A few cycles after reset, these registers are prepopulated with the LDIDs for local RN-Fs within that chip.

The following figure shows the programmable registers during CCIX Discovery.

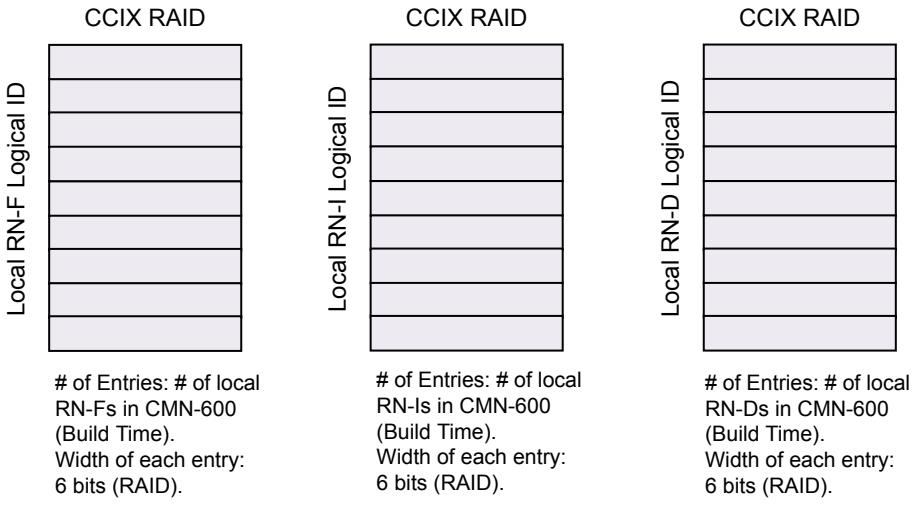


Figure 2-42 Programmable registers during CCIX Discovery

The CXHA contains a programmable register to program the local LDID for each remote CCIX RAID that can communicate with local CHI HNs on a given chip or socket. Each entry in the programmable

register also contains an RN-F bit to identify whether the remote CXRA is a caching agent (RN-F) or not. HN-Fs on the local chip use this LDID to track a line in its SF. Therefore unique LDID assignment is required for each remote requesting caching agent. These should not overlap with LDIDs assigned to local RN-Fs. It is assumed that these IDs are assigned after CCIX Discovery is complete. For example, all the CXRAs are discovered and assigned an RAID.

The following figure shows the programmable register for RAID to LDID during CCIX Discovery.

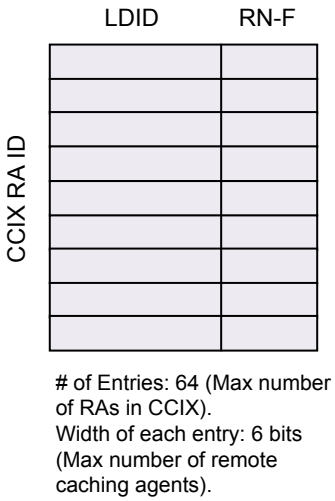


Figure 2-43 RAID to LDID during CCIX Discovery

With the LDID passed to HN-F in all CHI REQ flits, HN-F uses this LDID as the true logical ID for SF tracking purposes. HN-F uses a logical ID vector in the SF, with its size based on the total number of RN-Fs in the entire system (local and remote RN-Fs). The size is assigned when CMN-600 is generated. This value controls the SF efficiency, so it is ideal to set the value based on the total number of caching agents that can be there in the entire system. If the exact number is not known, the value must be set to support the maximum number of caching agents that the entire system can have. CCIX supports a maximum of 64 CXRAs in the entire system.

The following figure shows all IDs that are generated and used to route a response from a remote HN-F on Chip 2 to an RN-F on Chip 1.

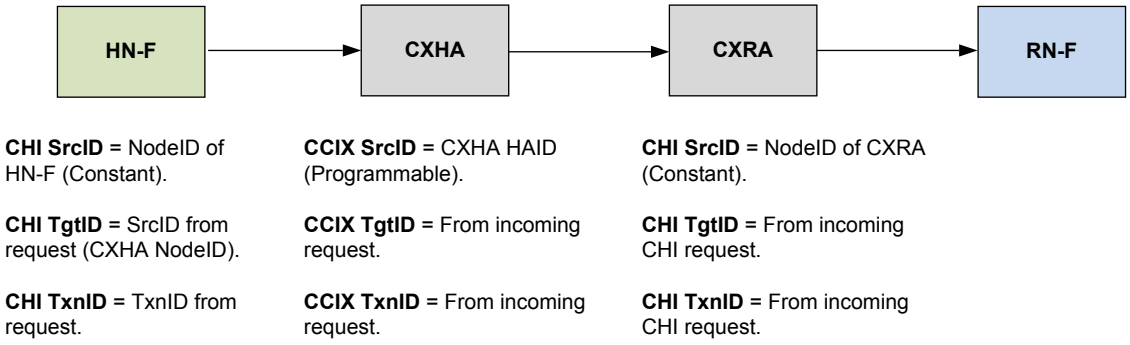


Figure 2-44 Remote HN-F to RN-F IDs

The following figure shows the flow of a snoop from an HN-F to a remote RN-F.

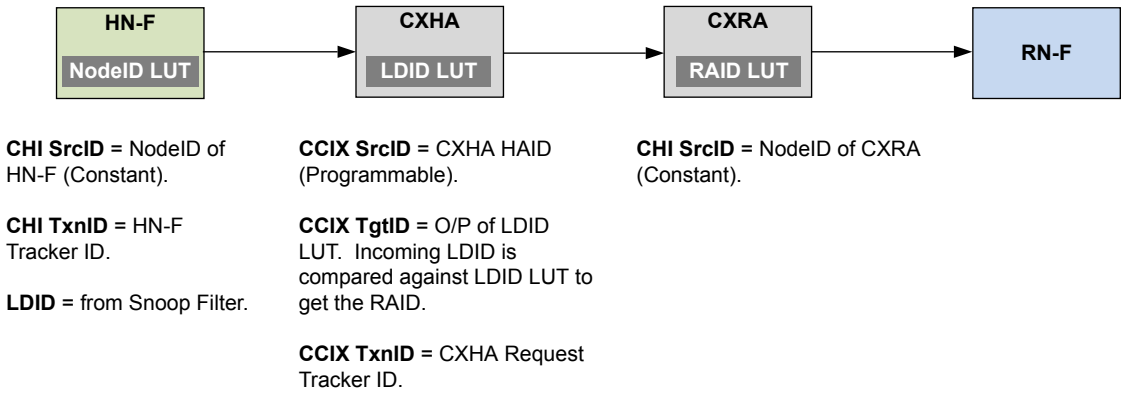


Figure 2-45 Snoop from HN-F to remote RN-F

The HN-F contains the following programmable LUT to program the CXHA node ID of each remote caching agent. HN-F uses the unique LDID from the snoop vector to look up the physical CHI node ID of the CXHA where the snoops need to be sent. The following table shows an example programming where logical IDs 0-7 are assigned to the local RN-Fs and logical IDs 8-15 are assigned to the remote RN-Fs. Software assigns these IDs during the Discovery process.

Table 2-48 Example program

Logical ID as index	HN-F programmable register	
	CHI node ID	ID valid
0	Local RN-F 0	1
1	Local RN-F 1	1
2	Local RN-F 2	1
…	…	…
7	Local RN-F 7	1
8	CXHA	1
9	CXHA	1
…	…	…
15	CXHA	1
16	Not programmed	0
…	Not programmed	0
n	Not programmed	0

The CXHA uses the LDID from incoming CHI snoop to perform a content match against the entries of programmable CCIX RAID to local LDID LUT. This results in the CCIX RAID sending a CCIX snoop, as the following figure shows.

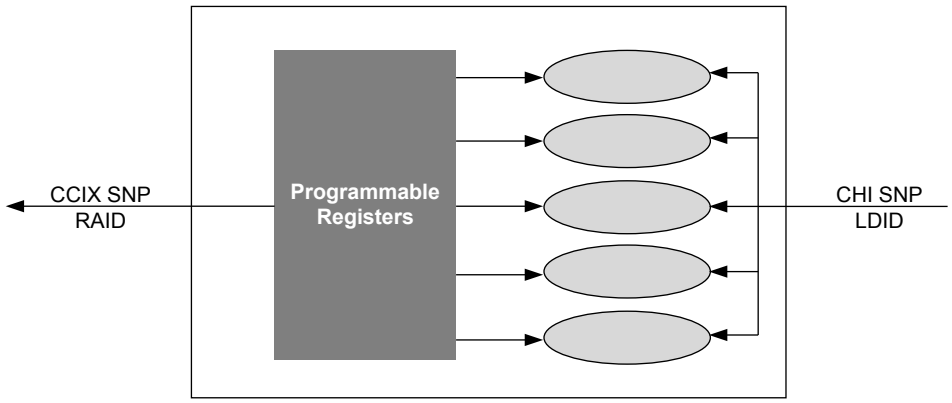


Figure 2-46 CHI SNP LDID to CCIX SNP RAID flow

The following figure shows the number of entries at build time.

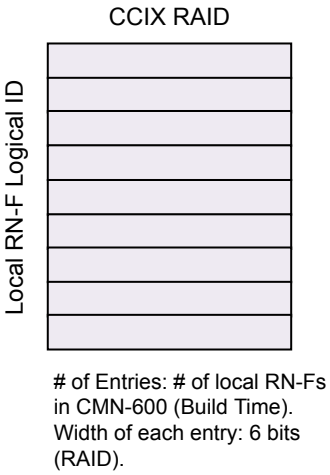


Figure 2-47 Number of entries at build time

The following figure shows the detailed flow of a CHI SNP LDID to CCIX SNP RAID conversion.

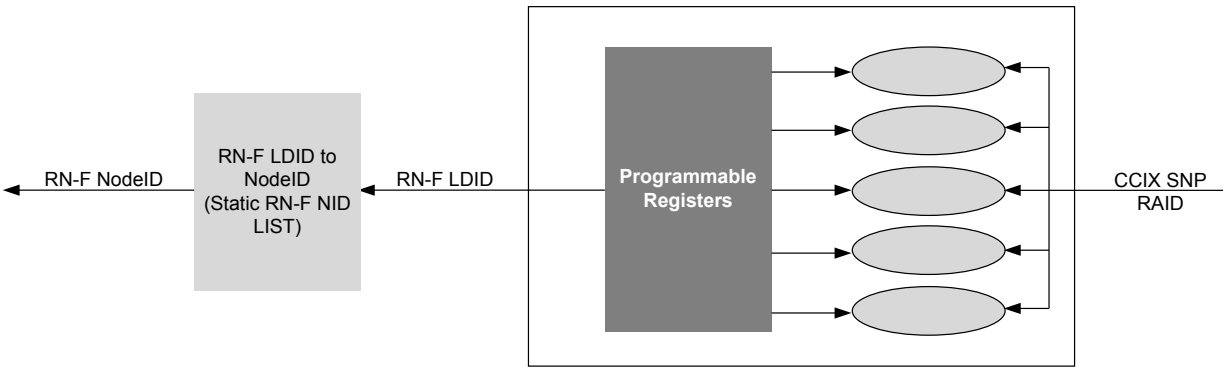


Figure 2-48 CHI SNP LDID to CCIX SNP RAID detailed flow

The following figure shows all IDs that are generated and used to route a snoop response from a remote RN-F on Chip 1 to an HN-F on Chip 2.

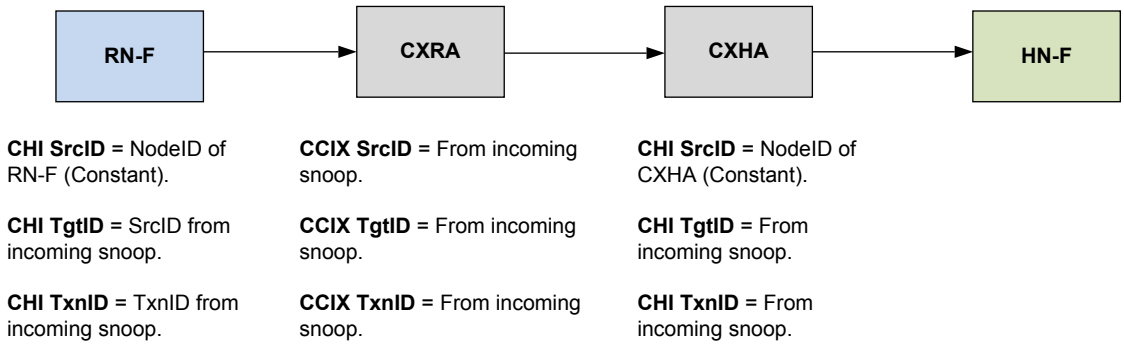


Figure 2-49 Remote RN-F to HN-F with all IDs generated

2.24 CMN-600 R3 128 RN-F support

CMN-600 R3 CML supports asymmetric RN-F count per chip up to a total of 128 RN-F in the system.

For example, 2 CMN with 32 RN-F each and two Accelerator with 16 RN-F each. It also enables Snoop Filter tracking for any combination of RN-Fs in the above topologies. The design extends the R2 CML support for 64 RN-F.

Logical to physical ID conversion LUT are extended to program 128 RNF LDIDs in the HN-F. It will translate the incoming RxREQ LDID to the packed Snoop filter LID vector. New registers are added in HN-F to program the LDID conversion matrix in the following table, namely **por_hnf_ldid_map_table_reg0** to **por_hnf_ldid_map_table_reg3**. The fields in these register are:

- **valid_cxhaX** – To indicate valid CXHA ID and pointer are programmed.
- **srcid_cxhaX** – Contains the CHI Source ID of the CXHA. Each SrcID must be unique in the table.
- **starting_ldid_cxhaX** – The starting LDID of the remote RNFs (behind this CXHA) as seen by HN-F.

Table 2-49 HN-F LDID mapping

Valid	CXHA SRC ID	LDID Pointer
-	-	-
-	-	-
-	-	-
-	-	-
-	-	-

Upon new request from a remote chip, HNF will check if the request is from a remote RNF. If so, then the CHI_SrcID of the CXHA is checked in the LDID Map Table. If the CXHA has been programmed, it will convert the incoming LDID to internal LID as shown here:

- `HNF_Lid = LDID_Ptr + Request_LDID`

Similarly, when a snoop request is to be sent to CXHA, HN-F will lookup the LDID Mapping table to check if the CXHA's CHI_SrcID is programmed. If so, then it will convert the internal LID to interface LDID as shown here:

- `Snp_LID = HNF_Lid - LDID_Ptr`

Example programming for HN-F

Assuming a system as shown in the following figure:

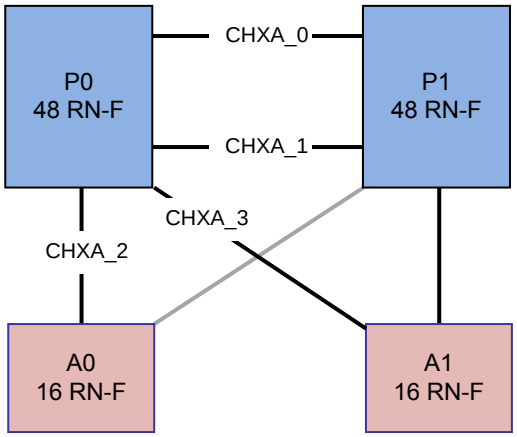


Figure 2-50 HN-F programming example system

The system contains four chips total:

- P0 – CML-based chip with 48 RN-Fs (LDID 0 to 47)
- P1 - CML-based chip with 48 RN-Fs (LDID 0 to 47)
- A0 – Accelerator chip with 16 RN-Fs and one CXHA link (LDID 0 – 15) – CXHA 2
- A1 – Accelerator chip with 16 RN-Fs and one CXHA link (LDID 0 – 15) – CXHA 3

From P0 chip perspective, P1 is connected to it through 2 CCIX links using port aggregation (CXHA_0 and CXHA_1). A0 is connected through CXHA_2 and A1 is connected through CXHA_3.

As there are more than 64 RNF's in the system (while the LDID width in the DEV flit interface is only 6-bits), HNF has to internally remap the flit LDID's to internal logical ID's for SF tracking. The example mapping is shown in the following table.

Table 2-50 HN-F Logical ID in P0 chip

HN-F SF Logical ID	REQ/SNP Flit LDID	Chip which this RN-F belongs
0	0	P0 (Local RN-Fs)
...	...	
47	47	
48	0	A0 (CXHA_2)
...	…	
63	15	
64	0	A1 (CXHA_3)
...	...	
79	15	
80	0	P1 (CXHA_0 and CXHA_1)
...	...	
127	47	

Based on the content in the above table, the LDID mapping table must also be programmed to match the above LID LUT as shown in the following table.

Table 2-51 Programming of LDID Mapping table

Valid	CXHA SRC ID	PDID_Ptr
1	CXHA_0	80
1	CXHA_1	80
1	CXHA_2	48
1	CXHA_3	64
0	0	0

Note

CXHA_0 and CXHA_1 are both programmed with the same LDID_Ptr values as they both connect to P1 Chip. So requests from either CXHA port (or snoops to either CXHA port) will always start at the same pointer in the LDID mapping table.

2.25 CCIX Port Aggregation groups

CMN-600 R3 CML CMN-600's CML configuration supports 2 *CCIX Port Aggregation Groups* (CPAG).

This feature can be used when connecting two or more chips together with multiple ports between the chips. For example, the following figure shows three chips connected and two CPAG are used.

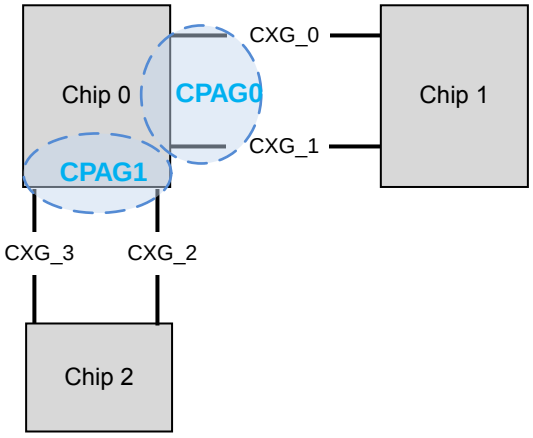


Figure 2-51 CCIX Port Aggregation Groups

CPAG_0: CCIX Port Aggregation group with 2 CCIX ports (CXG_0 and CXG_1) to connect Chip 1 to Chip 0.

CPAG_1: CCIX Port Aggregation group with 2 CCIX ports (CXG_2 and CXG_3) to connect Chip 2 to Chip 0.

In order to enable CPAG, both RNSAM and HNF registers must be programmed accordingly in Chip 0.

2.26 GIC communication over AXI4 Stream ports

CMN-600 supports optional master/slave AXI4 Stream ports on RN-I, RN-D, and SMXP RN-F ports for communication between GIC and CPUs. *General Interrupt Controller* (GIC) information is also transmitted across CCIX links for CML SMP configurations.

More system-level information is available in the *GIC-600 AXI4-Stream Integration* white paper upon request.

A4S routing

The A4S ports are addressed by Logical ID, which are assigned sequentially from 0 to the number of A4S ports. To send a packet from one A4S port to the destination A4S port, the TDEST should be assigned to the Logical ID of the target A4S port, or the Logical ID of the CXRH for GIC traffic targeting the other chip. The CMN-600 Discovery process, see *2.5 Discovery* on page 2-54 for more information, returns the number of A4S ports and Logical ID information for each A4S port by reading corresponding RN-I, RN-D and XP unit information registers.

Other requirements

- The CXRH GICD_DESTID input must be driven the PUB_DESTID associated with GICD A4S port, see the *CMN-600 Release Note* for more information on determining the GICD port PUB_DESTID. GICD drives the CMN-600 **RXA4STRI[7:0]** input (8 MSB bits of GICD ICDRTDEST), indicating the CCIX link of the target chip, in addition to the **RXA4STDEST[7:0]** (8 LSB bits of GICD ICDRTDEST) of CXRH for CML SMP configurations.
- The A4S master needs to assert valid irrespective of ready state to transmit data.

2.27 Clocking

The following sections describe the CMN-600 clocking microarchitecture:

This section contains the following subsections:

2.27.1 Clock domains

CMN-600 operates in a single clock domain as shown in the following figure.

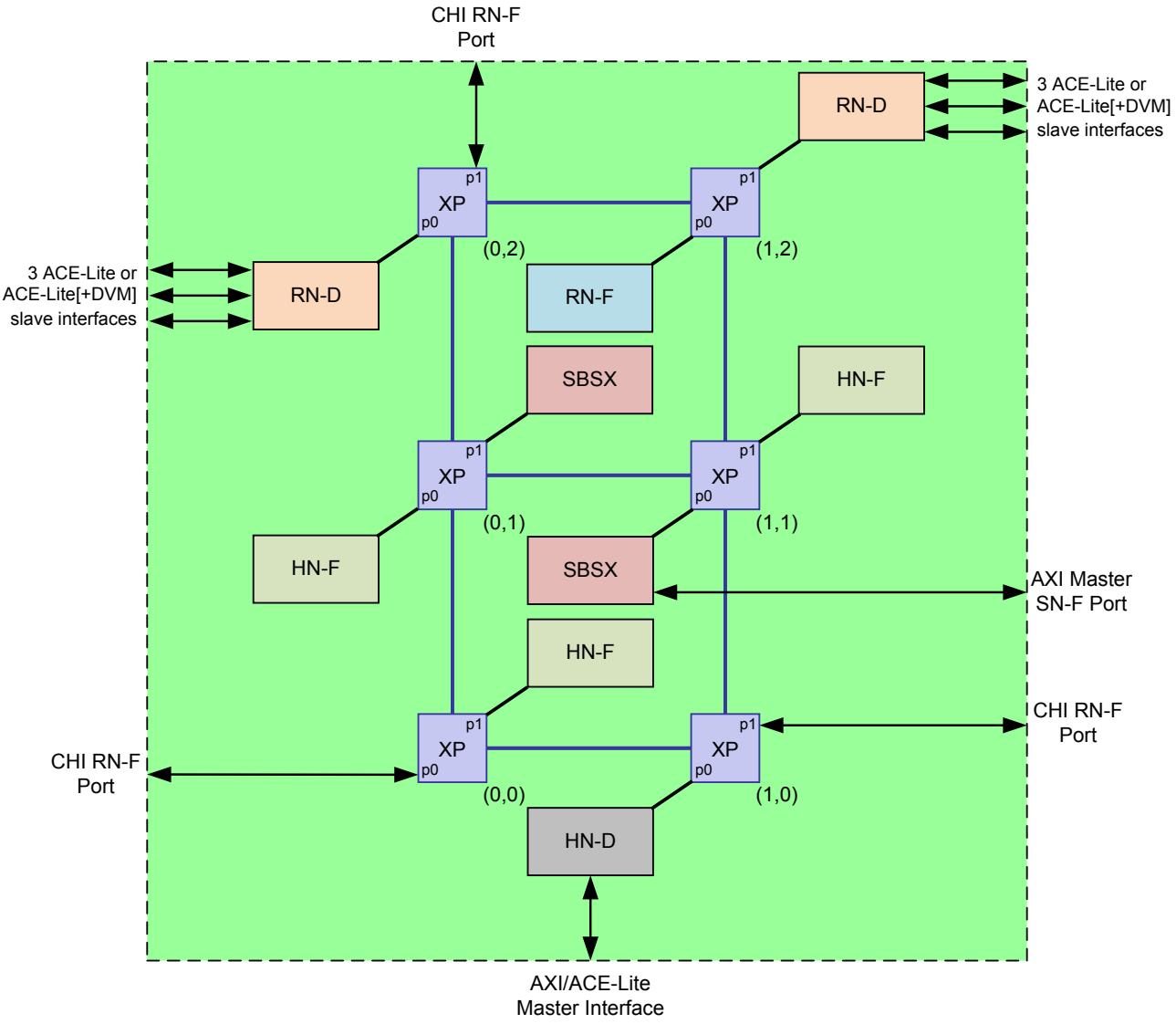


Figure 2-52 CMN-600 clock domain – fully synchronous

2.27.2 CML clock inputs

There are two additional clock inputs for the CML configuration: **CLK_CGL** and **CLK_CXS**.

CLK_CGL is a copy of the CMN clock input **GCLK0**. A separate clock input is provided to allow gating of the CGL clock domain independent of the **GCLK0** domain. **CLK_CXS** clocks the CXS interface logic, and may be synchronous or asynchronous to **GCLK0**. **CLK_CXS** can be driven with **CLK_CGL** for synchronous configurations, as the following figure shows.

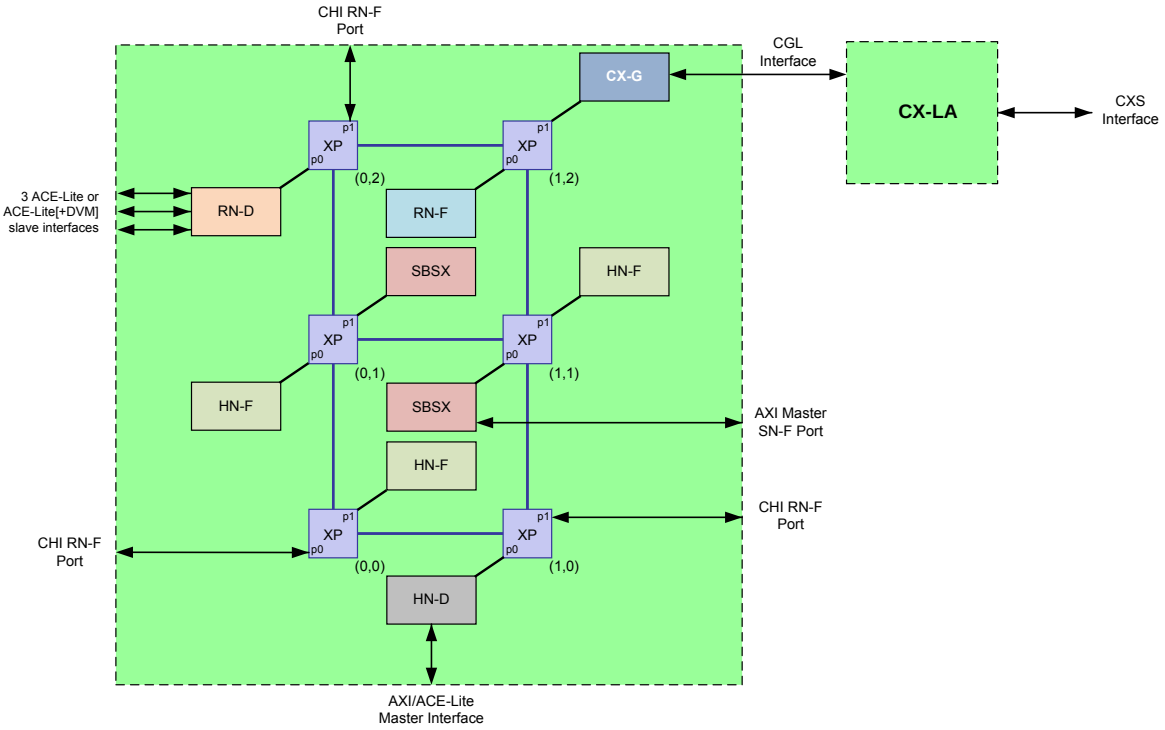


Figure 2-53 CMN-600 clock domains with synchronous CXS domain

The CXLA block contains an asynchronous domain bridge for configurations where the **CLK_CXS** domain is asynchronous to the **CLK_CGL** domain, as the following figure shows.

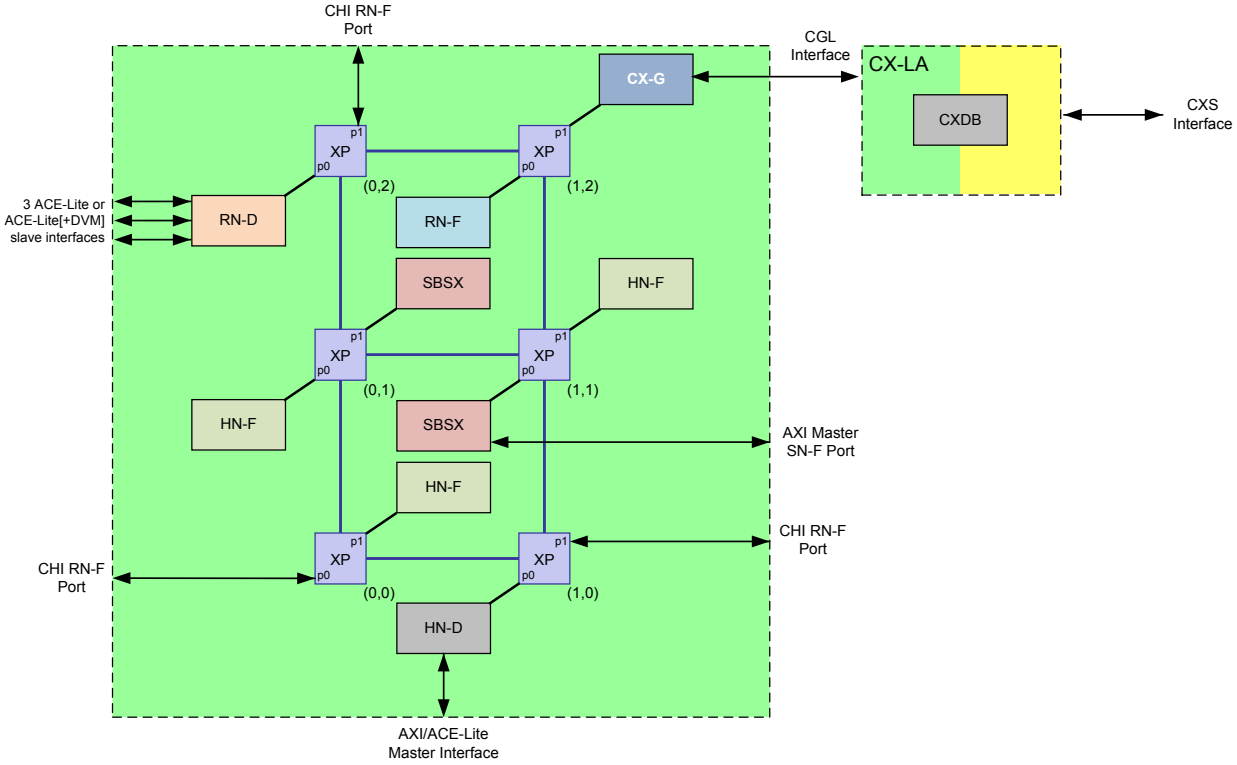


Figure 2-54 CMN-600 clock domains with asynchronous CXS domain

2.27.3 Clock hierarchy

The clocking delivery and clock gating architecture is hierarchical.

Within the clock gating hierarchy, three levels of clocks are defined:

Global clock This is the clock input to the CMN-600 system. The global clock the SoC provides is likely to be controlled by an additional level of clock gating or clock control outside of the system. Although this is not a system requirement, CMN-600 includes support for external clock control.

Regional clocks Regional clocks are created as an output of regional clock gaters that include a coarse enable for coarse-grained clock gating under idle or mostly idle conditions. This enables a higher level of power reduction than is possible using local clock gating, because the clock network between the regional and local gaters can be shut down using the regional gaters. The regional clock gaters are instantiated in and controlled by the CMN-600 RTL. The exact set of regional clocks is internal to CMN-600 and is not described in this book.

Local clocks Local clocks are created as an output of the local clock gaters that are controlled by fine-grained enables that the CMN-600 RTL creates. Local clocks are used to directly clock sequential elements in the CMN-600. The exact set of local clocks is internal to CMN-600 and is not described in this book.

The following figure shows the clocking hierarchy.

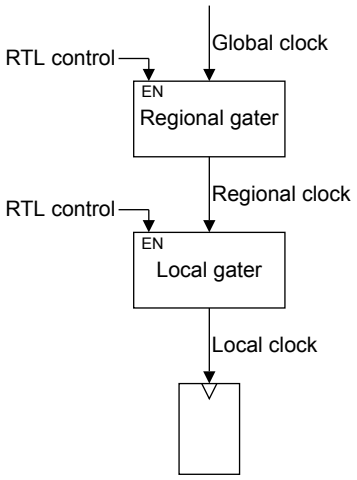


Figure 2-55 Clocking hierarchy

2.27.4 Global clock

The CMN-600 global clock input is indicated in the following table.

Table 2-52 Global clock input

Signal Name	Description
GCLK0	Primary CMN-600 clock input.
CLK_CGL	CML clock input.
CLK_CXS	CML clock input.

2.27.5 Clock enable inputs

CMN-600 includes several clock enable inputs.

The clock enable input signals are:

ACLKEN_S This input is present on each AMBA slave interface.

ACLKEN_M This input is present on each AMBA master interface.

ATCLKEN This input is present on each debug and trace **ATB** interface.

All clock enables, shown here as ***CLKEN***, have identical functionality, enabling the respective interfaces with which they are included to run at integer fractions of **GCLK0**, that is, slower than **GCLK0**, ranging from 1:1 to 4:1. **ATCLKEN** is limited to 2:1 to 4:1 integer fractions. This enables synchronous communication with slower SoC logic.

CLKEN asserts one **GCLK0** cycle before the rising edge of **SoC-CLK**. SoC control logic can change the ratio of **GCLK0** frequency to the SoC clock, **SoC-CLK**, frequency dynamically using ***CLKEN***.

The following figure shows a timing example of ***CLKEN*** that changes the ratio of the frequency at which the relevant interface operates respective to **GCLK0** from 3:1 to 1:1.

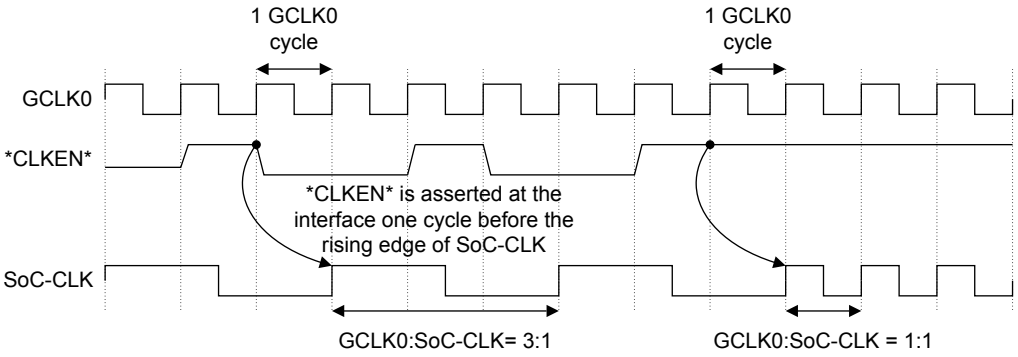


Figure 2-56 *CLKEN* with GCLK0:SoC-CLK ratio changing from 3:1 to 1:1

2.27.6 Timing closure with credited slices

The network provides credited slices to assist during timing closure.

CMN-600 includes the following optional credited slices:

- Device Credited Slice (DCS), at boundaries between a device and CAL/XP.
- Mesh Credited Slice (MCS), at boundaries between XPs.
- CAL Credited Slice (CCS), for CMN-600 R2 at boundaries between a CAL and XP.

The slices are simple repeater-flop structures applied across the entire communication boundary. The supported number of Credited Slices of each type is specified in *1.5.3 Device placement and configuration* on page 1-26. The following figure shows an example CMN-600 configuration with MCS and DCS instances.

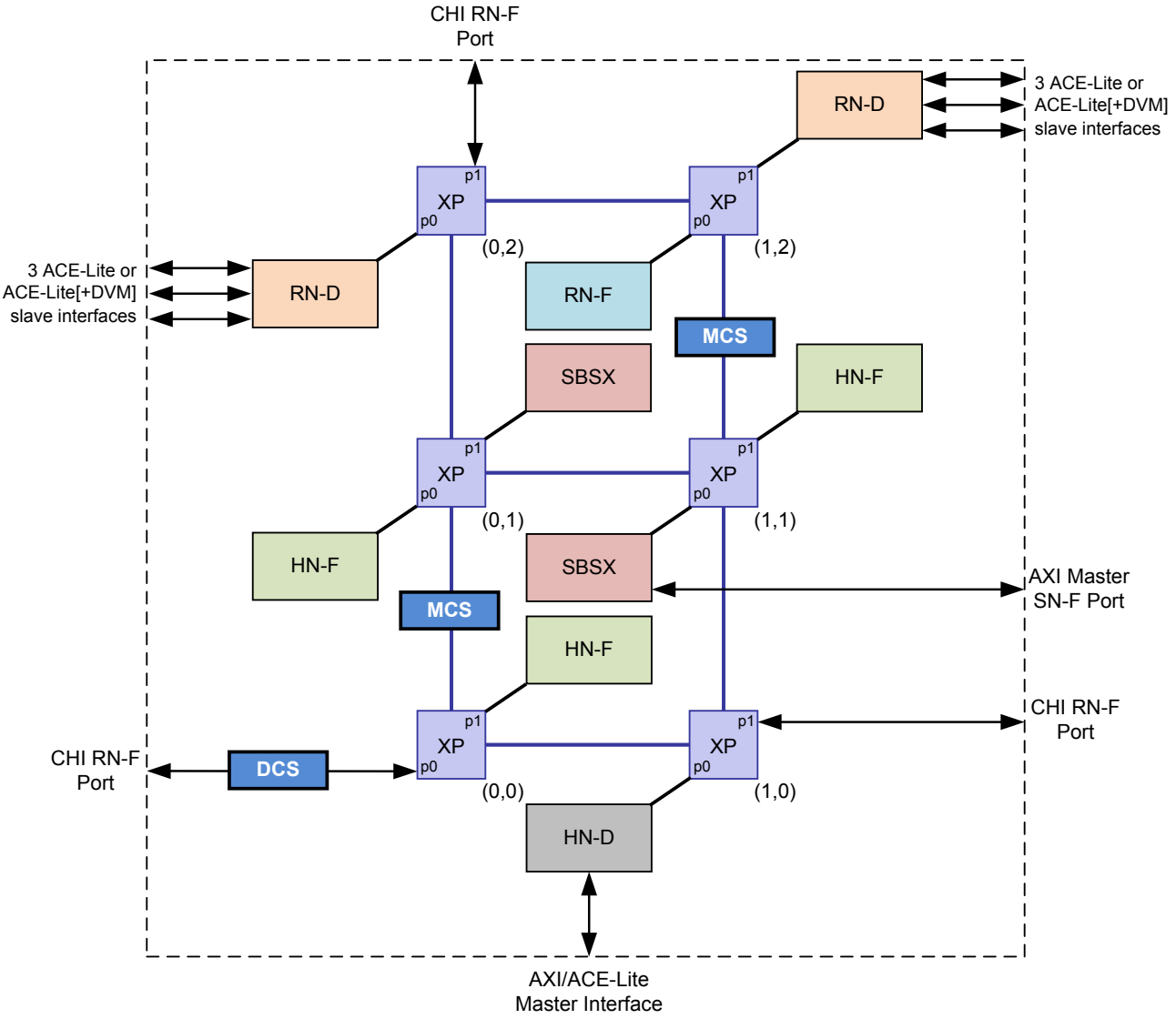


Figure 2-57 CMN-600 system with optional MCS and DCS

2.28 Reset

CMN-600 has a single global reset input signal, **nSRESET**.

nSRESET is an active-LOW signal that can be asynchronously or synchronously asserted and deasserted.

When asserted, **nSRESET** must remain asserted for 72 clock cycles. Likewise, when deasserted, **nSRESET** must remain deasserted for 72 clock cycles. This ensures that all internal CMN-600 components enter and exit their reset states correctly.

All CMN-600 clock inputs must be active during the required 72-cycle, or larger, period of **nSRESET** assertion, and must remain active for at least 72 cycles following deassertion of **nSRESET**.

This section contains the following subsection:

- *2.28.1 CML reset* on page 2-151.

2.28.1 CML reset

There are two additional reset inputs for the CML configuration: **nRESET_CGL** and **nRESET_CXS**.

Both **nRESET_CGL** and **nRESET_CXS** are active-LOW signals that can be asynchronously or synchronously asserted and deasserted.

When asserted, **nRESET_CGL** and **nRESET_CXS** must remain asserted for 20 **CLK_CGL** and **CLK_CXS** clock cycles respectively. Likewise, when deasserted, **nRESET_CGL** and **nRESET_CXS** must remain deasserted for 20 **CLK_CGL** and **CLK_CXS** clock cycles respectively. This ensures that all CML components enter and exit their reset states correctly.

Both **CLK_CGL** and **CLK_CXS** must be active during the required 20-cycle, or larger, period of **nRESET_CGL** and **nRESET_CXS** assertion respectively and must remain active for at least 20 cycles following deassertions.

Refer to *2.27.2 CML clock inputs* on page 2-145 for more relationship information between the CXS and CGL domains.

——— **Note** ———

There is no sequencing requirement between the CMN-600 nSRESET and the CML resets. However, the CML domains must exit reset before CXLA functionality is required.

———————————

2.29 Power and clock management

CMN-600 includes several power management and clock management capabilities, that are either externally controllable or are assisted by the *System-on-Chip* (SoC).

The power management and clock management capabilities are:

- High-level clock gating that indicates inactivity in the system, enabling an external clock controller to disable global clock inputs during periods of inactivity. This significantly reduces dynamic power consumption.
- A number of distinct predefined power states, including states in which all, half, or none of the *SLC* (SLC) tag/data RAMs can be powered up, powered down, or in retention:
  - A state in which only the HN-F SF is active.
  - A state in which neither the SLC RAMs, nor SF RAMs, are active.

  These power states reduce static and dynamic power consumption.
- Support for static retention in HN-F in which the SoC places SLC and SF RAMs in a retention state. This reduces static power consumption.
- Support for in-pipeline low-latency data RAM retention control, in which a programmable idle counter can be used to put the SLC RAMs in retention.

This section contains the following subsections:

2.29.1 High-level clock gating (HCG)

High-level Clock Gating (HCG) is a mechanism supported by the PCCB that notifies the SoC when the CMN-600 is inactive. HCG enables an external SoC clock control unit, the *External Clock Controller* (ExtCC), to stop the CMN-600 **GCLK0** clock inputs.

CMN-600 includes a Q-Channel interface that enables CMN-600 and the SoC to communicate to achieve HCG functionality through the PCCB. See the *AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces* for more information.

External clock controller

This section describes the external clock controller.

The following figure shows an example of how the ExtCC controls the clock gating flow. This example clock gating sequence begins and ends with the Q-Channel in either of the following states:

- Quiescent state (Q_STOPPED), where **QREQn** and **QACCEPTn** are asserted.
- Active state (Q_RUN), where **QREQn** and **QACCEPTn** are deasserted.

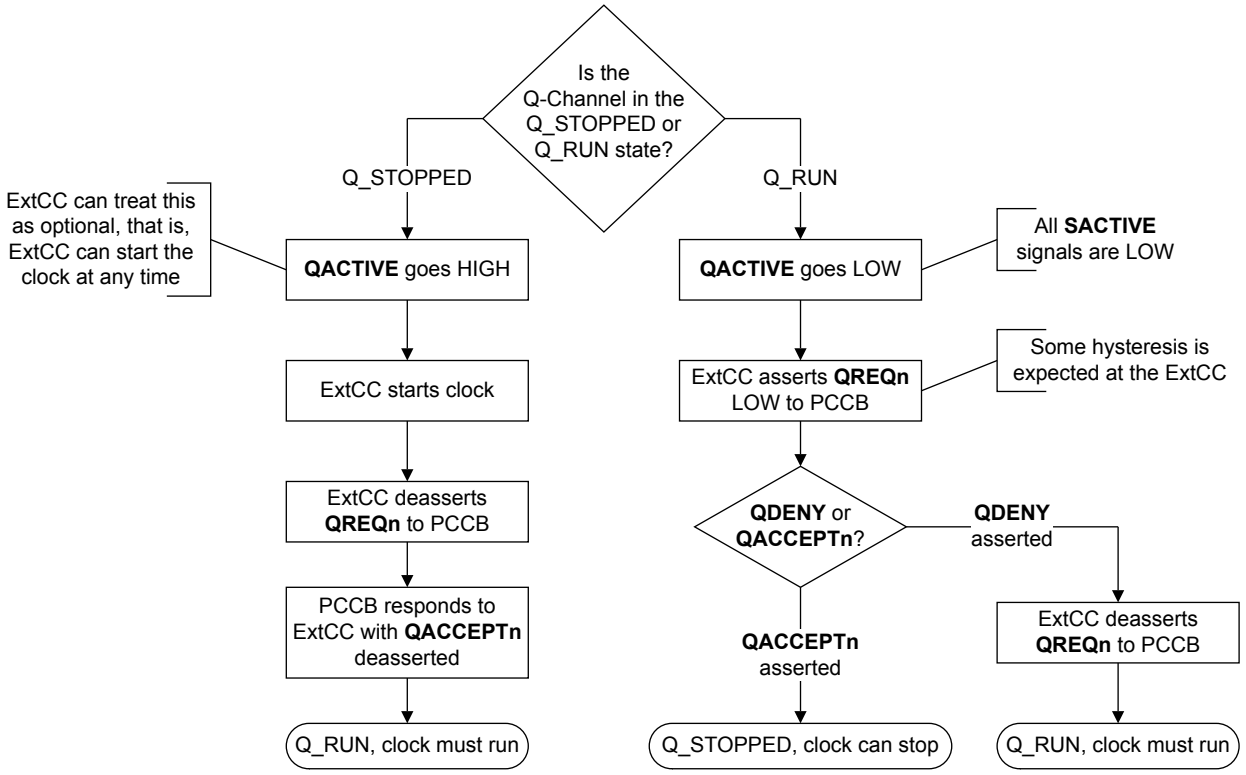


Figure 2-58 Clock gating control using ExtCC

The requirements of the ExtCC are as follows:

- It must supply a clock to CMN-600 when the Q-Channel is in any state other than Q_STOPPED.
- The ExtCC can either choose to gate the clock to CMN-600 when the Q-Channel is in the Q_STOPPED state, or it can choose to run the clock at any time.
- ExtCC is responsible for bringing the Q-Channel to Q_RUN state after reset deassertion.
- Although this manual does not describe the exact behavior of the ExtCC and its usage of **QREQn** in response to **QACTIVE** deassertion, the design of the ExtCC is likely to include a control loop with some hysteresis so that HCG is enabled when the system is inactive for long periods, but is not enabled for very short periods of inactivity. If the clocks are stopped in response to short periods of inactivity, performance of CMN-600 can be negatively affected.
- It is the responsibility of the SoC designer to fully control the clock management Q-Channel. If there is a requirement for a control or configuration bit to completely enable or disable HCG functionality, that register or bit must exist outside of CMN-600. More specifically, CMN-600 has no internal means of disabling HCG.

CML clock management

CMN-600 CML configurations add two additional clock domains and corresponding Q-Channel interfaces for each CXG instance and corresponding CXS interface:

- CLK_CGL Q-Channel: Manages the CGL link and CGL domain logic in the CXG and CXLA devices.
- CLK_CXS Q-Channel: Manages the CXS link interface and CXS clock domain logic in the CXLA.

The following table shows the possible clock states for the CMN-600 and CML device clocks, where N denotes multiple CXS interfaces:

Table 2-53 CMN-600 and CML device clock states

GCLK0	CLK_CGL[N]	CLK_CXS[N]	Description
RUN	RUN	RUN	CMN-600 and CXS[N] interface active
RUN	RUN	STOP	CXS[N] domain gated
RUN	STOP	RUN	CGL[N] inactive, transitory state
RUN	STOP	STOP	CXS[N] interface fully gated
STOP	STOP	RUN	CXS[N] active, others inactive, transitory state
STOP	STOP	STOP	CMN-600 fully gated, all CXS[N] interfaces inactive

2.29.2 Power domains

The power domains in CMN-600 are split between the Logic and RAMs within the HN-F partitions.

The power domains are:

LOGIC power domain
All logic except HN-F SLC tag and data RAMs and HN-F SF RAMs.

HN-F SLC RAM0 power domain
SLC tag/data RAMs way[7:0] within HN-F partitions, the RAMs in each HN-F partition can be independently controlled.

HN-F SLC RAM1 power domain
SLC tag/data RAMs way[15:8] within HN-F partitions, the RAMs in each HN-F partition can be independently controlled. The RAM1 domain for 3MB SLC size configurations includes way[11:8].

HN-F SF power domain
SF RAMs within HN-F partitions, the RAMs in each HN-F partition can be independently controlled.

An example of the power domains is shown in the following figure.

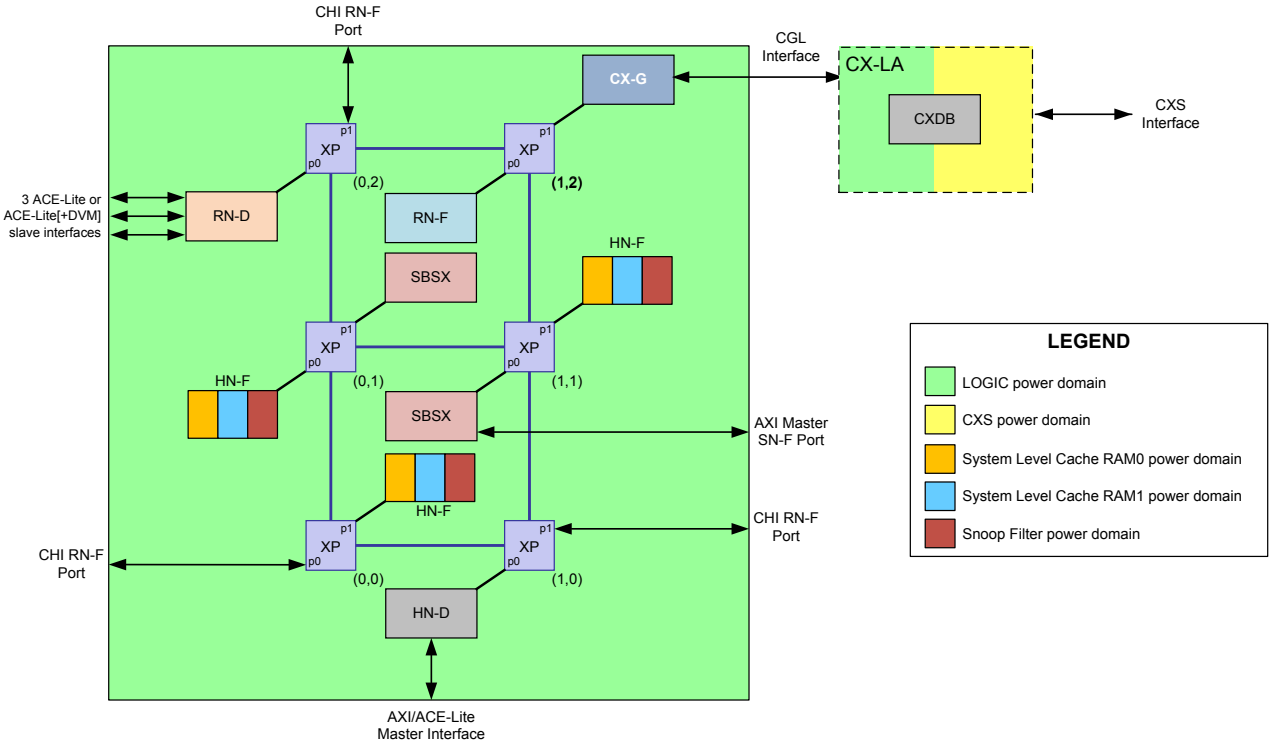


Figure 2-59 CMN-600 power domains

2.29.3 Power domain control

The CMN-600 Logic P-Channel controls all of the non-RAM and non-CXS power domains.

In addition to controlling the Logic domain, it allows synchronization between the HN-F software-controlled power domains and the Logic domain through a CONFIG state as shown in the following figure.

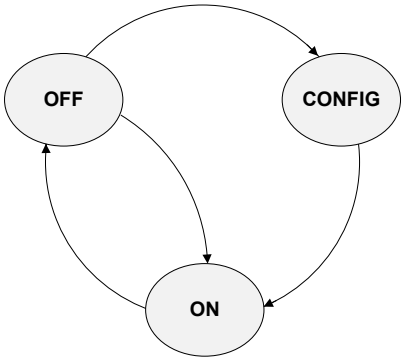


Figure 2-60 Logic domain states

There are two paths for transitioning from the OFF to ON state:

1. Power-on-reset: The Logic PSTATE OFF to ON transition also initiates NOSFSLC->FAM transition for all HN-F partitions.
2. Exit from HN-F Static Retention state: The Logic PSTATE transitions from OFF to CONFIG, indicating that CMN-600 is exiting a Memory Retention state, and does not initiate any HN-F partition power transitions.

The following table contains the power modes of components within the domain and the associated PSTATE values.

Table 2-54 Power mode configurations and PSTATE values

Power mode	PSTATE	CMN-600 Logic	HN-F
Off	00000	Off	Off/Mem_Ret
Config	11000	On	Any
On	01000	On	Any

See *2.29.7 HN-F power domains* on page 2-157 for an introduction to HN-F states.

See *A.4 Power management signals* on page Appx-A-1153 for P-Channel signal list information.

CXS Power Gating

CML systems contain an additional power domain: the CXS power domain. CXS logic is controlled by a combination of the CXS Power Q-Channel, and the CXS Q channel controlling the clocks. Power must be provided unless both the CXS Power Q-Channel and the CXS Q channel are in the OFF State.

2.29.4 P-Channel on device reset

This section shows how to initialize the power state of a power domain.

Certain device power states might power down the control logic. When powering this control logic back on, the power controller must indicate the state that the device must power up. The device detects the required state by sampling **PSTATE** when **nSRESET** deasserts. The **PSTATE** inputs must be asserted before the deassertion of reset and remain after the deassertion of **nSRESET**, to allow reset propagation within CMN-600. The power controller must ensure that the reset sequence is complete before transitioning **PSTATE**, otherwise the device might sample an undetermined value. The following figure shows the state initialization on reset.

Note

PSTATE inputs must be static 100 cycles before deassertion of nSRESET, and also for 100 cycles after.

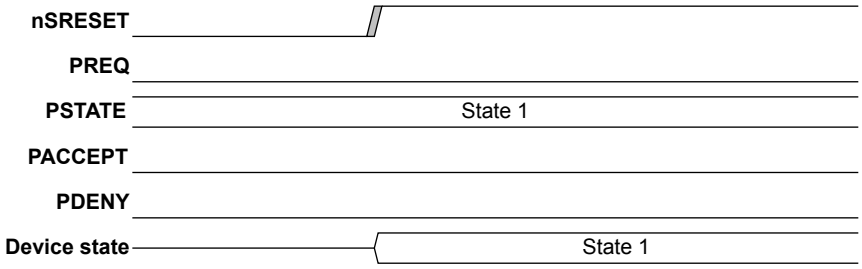


Figure 2-61 Reset state initialization

See *2.29.7 HN-F power domains* on page 2-157 for an introduction to HN-F states.

2.29.5 CXS power domain

The CMN-600 CXS Power Q-Channel controls the CXS power domain.

Note

The CXS power domain can be shut off if the CXS interface is inactive.

The following table shows the possible CMN-600 LOGIC and CXS power states, where N denotes multiple CXS interfaces:

Table 2-55 CMN-600 LOGIC and CXS power states

LOGIC state	CXS[N] state	Description
ON	ON	CMN-600 and CXS[N] interface active.
ON	OFF	CXS[N] interface inactive.
OFF	ON	CXS[N] domain active, transitory state.
OFF	OFF	Shutdown, all CXS[N] interfaces inactive.

2.29.6 HNF memory retention

When isolating the CMN-600 outputs, handshake protocols on certain interfaces must not be violated.

Use these following guidelines to enter the HN-F memory retention.

Process for entering HN-F memory retention:

- Program the HN-Fs to enter the desired power state.
- Quiesce the interconnect, and wait for QACTIVE to drop.
- Place CMN-600 in LOGIC_OFF state through the Logic P-Channel.
- Isolate the CMN-600 outputs. This may be not bee needed if the logic on the other side of the interface is being powered-down and/or reset.
- Turn off power to CMN-600.

Process for leaving HN-F memory retention:

- Apply power to CMN-600.
- Assert reset.
- Enable clocks.
- Disable isolation of the CMN-600 outputs.
- Deassert reset.
- Place CMN-600 in LOGIC_CONFIG state through the logic P-Channel.
- Reprogram the HN-F PWPR to the retention mode the HN-F was in prior to turning off power.
- Reprogram the HN-F PWPR to ON.
- Reprogram the CMN-600 configuration registers, including the RNSAM and any other registers written during cold boot.
- Place CMN-600 in LOGIC_ON state through the P-Channel.
- Resume traffic/normal operation.

2.29.7 HN-F power domains

This section lists the valid power states and shows the power state transition diagram.

The following table shows the valid HN-F power states and their requirements.

——— **Note** ———

Transition to FAM or HAM is not supported if SLC size is 0KB.

———————————

——— **Note** ———

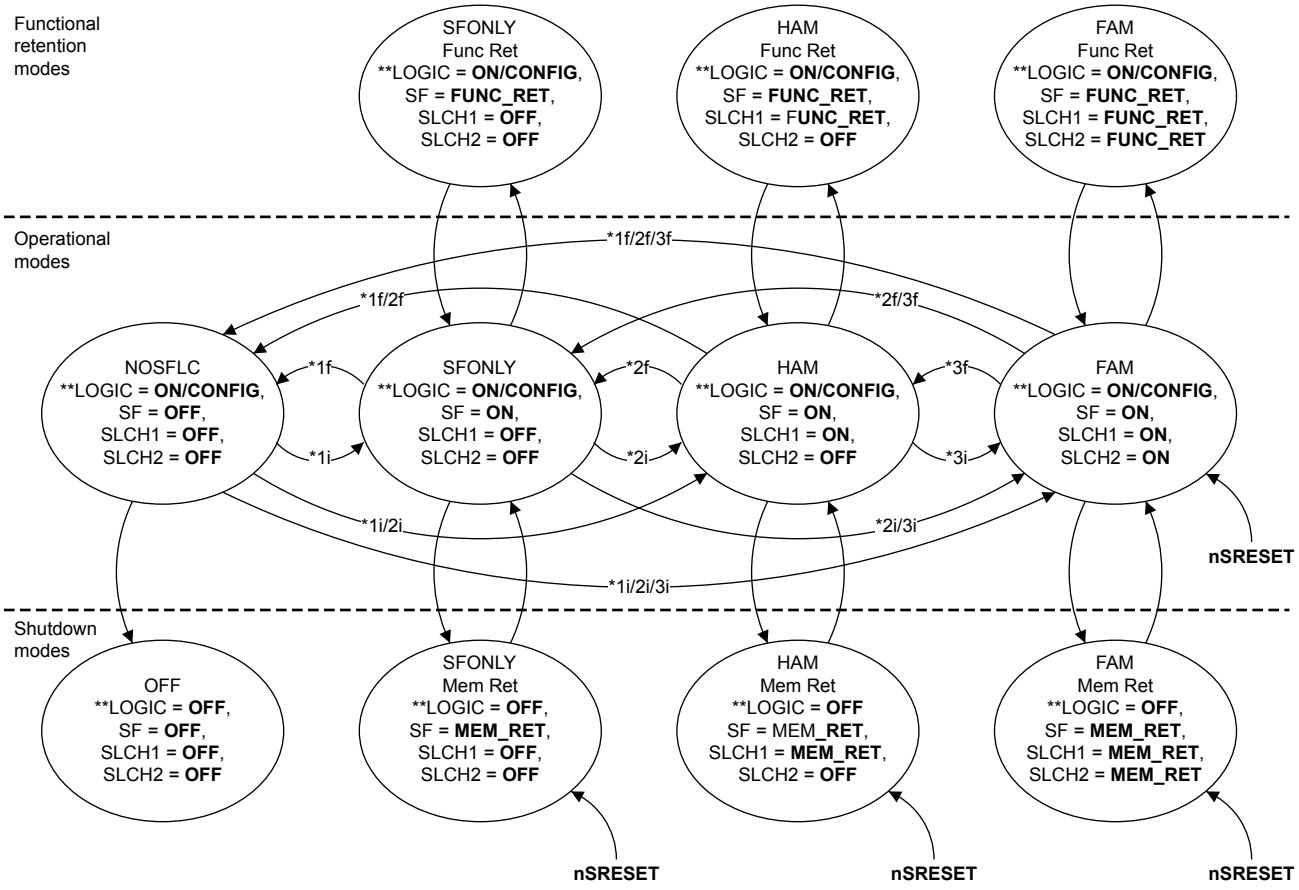
After initialization, power status register will indicate FAM instead of SFONLY for 0KB SLC config.

———————————

Table 2-56 HN-F power states

State	Description	Control logic	SF power state	SLC way[7:0] power state	SLC way[15:8] power state
FAM	Full run mode	On	On	On	On
HAM	Run mode with SLCH2 (SLC upper ways) disabled	On	On	On	Off
SF	Run mode with SLCH1 and SLCH2 disabled	On	On	Off	Off
NOSFSLC	Run mode with SLCH1, SLCH2, and SF disabled	On	Off	Off	Off
FAM Func ret	Run mode with SLCH1, SLCH2, and SF in dynamic retention	On	Retention	Retention	Retention
HAM Func ret	Run mode with SLCH1 and SF in retention, and SLCH2 in power-down	On	Retention	Retention	Off
SF Func ret	Run mode with SF in retention, and SLCH1 and SLCH2 in power-down	On	Retention	Off	Off
FAM Mem ret	Shutdown with SLCH1, SLCH2, and SF in retention	Off	Retention	Retention	Retention
HAM Mem ret	Shutdown with SLCH1 and SF in retention, and SLCH2 in power-down	Off	Retention	Retention	Off
SF Mem ret	Shutdown with SF in retention, and SLCH1 and SLCH2 in power-down	Off	Retention	Off	Off
OFF	Shutdown	Off	Off	Off	Off

The following figure shows the valid power states and transitions for a CMN-600 system.



Note: **BOLD** text shows the required power state.

* Automatic initialization and flushing actions:
1i: Initialize snoop filter RAMs.
2i: Initialize lower ways of tag RAMs.
3i: Initialize upper ways of tag RAMs.
1f: Flush (force back-invalidations as necessary and invalidate) snoop filter RAMs.
2f: Flush (clean/invalidate) lower ways of tag/data RAMs.
3f: Flush (clean/invalidate) upper ways of tag/data RAMs.

** All designations refer to P-state values required to enter the respective state.

Figure 2-62 Power state transitions

The HNF has three classes of power states:

1. Operational states, where logic is on and enabled RAMs are operating as normal.
2. Functional Retention states, where logic is on, and enabled RAMs are in retention.
3. Memory Retention states, where logic is off and enabled RAMs are in retention.

Within these power states, the HN-Fs in an SCG operate in four modes::

FAM Full-Associativity Mode (FAM), where the SF and the entire SLC is enabled.

HAM Half-Associativity Mode (HAM), where the SF is enabled but the upper half of the SLC ways are disabled and powered off.

SFONLY Snoop-Filter-Only Mode (SFONLY), where the SF is enabled but all of the SLC is powered off.

NOSFSLC No-SLC Mode (NOSFSLC), where the SF and SLC are disabled and powered off.

These HN-F power states are transitioned via configuration register writes that must target all HN-Fs in the SCG region. In addition, there is a NOSFSLC->FAM transition that can be initiated by the Logic domain P-Channel interface.

The **por_hnf_ppu_pwpr.policy** and **por_hnf_ppu_pwpr.op_mode** register fields are written to transition the HN-F partitions to a desired power state. The **por_hnf_ppu_pwsr.pow_status** and **por_hnf_ppu_pwsr.op_mode_status** config register fields are updated when the power state transition is complete. This transition can take many thousands of clock cycles if the SLC and/or SF is flushed as part of the transition. In addition, the **INTREQPPU** interrupt output can be used to indicate the completion of the HN-F power state transitions.

From FAM, HAM, or SFONLY, the HN-F can enter a dynamic retention mode via config register writes, where:

- The logic power is on.
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bit-cell retention but insufficient for normal operation.
- The array pipeline is blocked, and a handshake occurs to allow array access when exiting the retention state.

These dynamic power transitions are executed autonomously within each HN-F partition. Each HN-F has a programmable idle cycle counter, and initiates a P-Channel handshake with the corresponding RAMs to enter the dynamic retention state. Then the pipeline blocks transactions that target the HN-F RAMs. A coherent transaction triggers an exit from the dynamic retention state, and initiate another P-Channel handshake and takes the RAMs out of dynamic retention mode.

From these states, the SLC can also enter a memory retention mode, where:

- The logic power is turned off.
- The voltage to the RAMs is on, but is reduced to a level that is sufficient for bit-cell retention but insufficient for normal operation.
- Reset deassertion is essential when exiting retention after logic power off.

The CMN-600 logic domain power state is controlled by a P-Channel interface. This P-Channel interface also interacts with the HN-F power control logic via an internal bus. The HN-F power control logic waits for a command on the deassertion of nSRESET, depending on the overall power state transition that is required. For the power-on-reset HN-F FAM transition case, the PCCB block initiates the HN-F NOSFSLC->FAM command. For exit from static retention cases, the SCP initiates configuration register writes to the HN-F to indicate the HN-F power state.

The difference between the dynamic and static retention modes is that dynamic retention is entered because of a dynamic activity or inactivity indicator from the HN-F to the SoC. This is an output of the HN-F that is used to determine periods of inactivity long enough to warrant entering retention mode, but not long enough or not the type of inactivity to make the SoC place the SLC and SF in static retention. In addition to the static retention modes, the control logic can be powered down from the NOSFSLC state, at which point CMN-600 is fully off.

All activity that is required to enable safe transition between the respective power states is performed automatically by the HN-Fs in response to input P-Channel P-state transitions. No additional activity is required of the SoC logic to enable transitions between power states. For example, the HN-F performs clean and invalidation of half of the ways of the SLC and clean and invalidation of all ways of the SLC, as required by the respective power state transitions.

Note

CMN-600 cannot make any power transitions while the control logic is powered off. For example, for a transition from FAM static retention to OFF, a transition through the FAM and NOSFSLC while the LOGIC power domain in ON must occur to allow the SLC and SF to be flushed.

This table provides the PSTATE encodings for the HN-F and Power Domains including RAM configurations for the different operation modes.

Note

HN-F cannot process any transactions while in static retention (FUNC_RET or MEM_RET). HN-F needs to be in the ON state before sending any transactions to HN-F in this case. If HN-F is in dynamic retention, any activity will autonomously take HN-F out of dynamic retention.

Table 2-57 Power modes, operational modes, and RAM configurations

Operational Mode	Power Mode	PSTATE	Bank 0 RAM	Bank 1 RAM	SF RAM
FAM	ON	11_1000	ON	ON	ON
	FUNC_RET	11_0111	RET	RET	RET
	MEM_RET	11_0010	RET	RET	RET
HAM	ON	10_1000	ON	OFF	ON
	FUNC_RET	10_0111	RET	OFF	RET
	MEM_RET	10_0010	RET	OFF	RET
SFONLY	ON	01_1000	OFF	OFF	ON
	FUNC_RET	01_0111	OFF	OFF	RET
	MEM_RET	01_0010	OFF	OFF	RET
NOSFSLC	MEM_OFF	00_0110	OFF	OFF	OFF
	OFF	00_0000	OFF	OFF	OFF

2.29.8 HN-F RAM PCSM Interface

Each HN-F RAM interface contains a PCSM *(Power Control State Machine)*.

Each PCSM P-Channel interface that can be used to convert power state transitions into technology-specific controls, and the overall HN-F partition power state transition, is dependent on all P-Channel transactions to complete.

The following table lists the valid PSTATEs for this interface. There is no P-Channel PDENY on this interface.

Table 2-58 PSTATE Encodings

PSTATE	Value
On	1000
Func_Ret	0111
Mem_Ret	0010
Off	0000

2.29.9 SLC data RAM retention control

This section describes how to use the **l3_reten_hx** signal when the RAM is in retention mode.

The HN-F SLC data RAM quadwords have an input, **l3_reten_hx**, that can be used for dynamic retention control. This signal asserts four cycles before the data RAMs are accessed, either read or write, and is held for the duration of the access, accounting for RAM latency. This enables the RAMs to be put

in a retention mode, provided the 4-cycle wakeup is sufficient to exit retention mode and allow a read or write.

The following figure shows the **l3_reten_hx** signal behavior for a single SLC data RAM read. It asserts four cycles before the RAM read enable, and is held for the duration of the RAM read, three cycles after the RAM read enable in this case, showing the behavior of 3-cycle data RAMs.

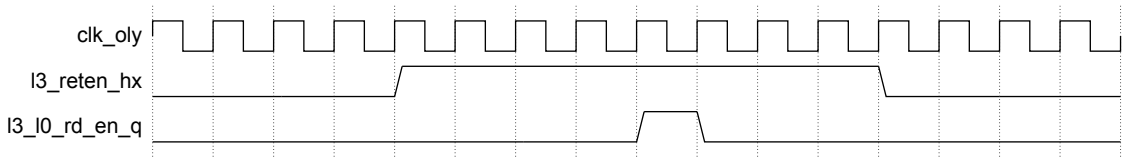


Figure 2-63 l3_reten_hx timing for single SLC data RAM read

2.29.10 HN-F power domain completion interrupt

The PCCB can be configured to generate interrupt **INTREQPPU** on completion of power state transitions for a collection of HN-Fs.

The PCCB contains a global status register **por_ppu_int_status** which indicates HN-F power state transition completion, and a mask register **por_ppu_int_mask** which allows filtering on all or a subset of the HN-Fs in the CMN-600 configuration. The bit positions in the **por_ppu_int_status** and **por_ppu_int_mask** registers correspond to the logical ID of the HN-Fs. **INTREQPPU** asserts when all **por_ppu_int_status** register bits with the corresponding **por_ppu_int_mask** register bit are set by the HN-F power transition completion.

INTREQPPU can be de-asserted by writing **1'b1** to the bits of the **por_ppu_int_status** register corresponding to the masked group of HN-Fs that completed the power transitions.

2.30 RN entry to and exit from Snoop and DVM domains

CMN-600 includes a feature that allows RNs to be included or excluded from the system coherency domain. This is also known as the Snoop domain or DVM domain. This feature ensures correct operations of Snoops and DVMs when:

- An RN is taken out of reset.
- An RN is powered down and then later powered up.

RN-Fs behave as follows:

- If an RN-F is included in the system coherency domain, it must respond to Snoop and DVM requests from CMN-600.
- If an RN-F is excluded from the system coherency domain, it does not receive Snoop or DVM requests from CMN-600.

RN-Ds behave as follows:

- If an RN-D is included in the system coherency domain, it must respond to DVM requests from CMN-600.
- If an RN-D is excluded from the system coherency domain, it does not receive DVM requests from CMN-600.

This section contains the following subsections:

- *2.30.1 Hardware interface* on page 2-163.
- *2.30.2 Software interface* on page 2-164.

2.30.1 Hardware interface

This section describes the hardware interface for RN inclusion into and exclusion from system coherency domain.

CMN-600 provides two signals for RN system coherency entry and exit:

- **SYSCOREQ** input (to CMN-600).
- **SYSCOACK** output (from CMN-600).

These two signals implement a four-phase handshake between the RN and CMN-600 with the four states as specified in the following table.

Table 2-59 RN system coherency states

SYSCOREQ	SYSCOACK	State
0	0	DISABLED
1	0	CONNECT
1	1	ENABLED
0	1	DISCONNECT

Coming out of Reset, the RN is in the DISABLED system coherency state.

CONNECT

To enter system coherency, RN must assert **SYSCOREQ** and transition to CONNECT state. The RN must be ready to receive and respond to Snoop and DVM requests in this state.

ENABLED

Subsequently, CMN-600 asserts **SYSCOACK** and transitions to CONNECT state. The RN is now included in the system coherency domain. The RN can receive and must respond to Snoop and DVM requests in this state.

DISCONNECT

When the RN is ready to exit system coherency, it must deassert **SYSCOREQ** and transition to DISCONNECT state. The RN continues to receive and must respond to Snoop and DVM requests in this state.

DISABLED

When all outstanding Snoop and DVM responses have been received, CMN-600 deasserts **SYSCOACK** and transitions to DISABLED state. In this state, no snoop or DVM transactions are sent to the RN which can now be powered down.

——— **Note** ———

The following rules must be obeyed to adhere to the four-phase handshake protocol.

- When **SYSCOREQ** is asserted, it must remain asserted until **SYSCOACK** is asserted.
- When **SYSCOREQ** is deasserted, it must remain deasserted until **SYSCOACK** is deasserted.

———————————

2.30.2 Software interface

This section describes the software interface for RN inclusion into and exclusion from system coherency domain.

CMN-600 provides two *Configuration Registers* (CRs) for system coherency entry and exit:

- RN-F:
  - **por_mxp_p{1,0}_syscoreq_ctl**
  - **por_mxp_p{1,0}_syscoack_status**
- RN-D:
  - **por_rnd_syscoreq_ctl**
  - **por_rnd_syscoack_status**

Reading and writing to these CRs provides a software alternative to the four-phase hardware handshake.

——— **Note** ———

The CRs may contain multiple bits where each bit corresponds to a different RN. The discussion below pertains to the Read and Write of the CR bit that corresponds to a given RN. When configuring the system coherency entry/exit for a given RN, software must adopt a Read-Modify-Write strategy to ensure that CR bits corresponding to other RNs are not modified when writing into the syscoreq_ctl CR.

———————————

Coming out of Reset, both CRs are cleared, indicating DISABLED state.

CONNECT

To initiate an RN entry into the system coherency domain, software must first poll both CRs and ensure that the CR bits corresponding to that RN are set to zeros. When the RN is ready to receive and respond to Snoop and DVM requests, software must write a 1 into the corresponding bit in the syscoreq_ctl CR in order to transition the RN to CONNECT state.

ENABLED

Subsequently, CMN-600 indicates a transition to CONNECT state by setting the corresponding CR bit in the syscoack_status register to one. The RN is now inside the system coherency domain. Software can poll the syscoack_status register to determine this state transition.

DISCONNECT

To initiate an RN exit from the system coherency domain, software must first poll both CRs. After ensuring that the CR bits corresponding to that RN are set, software must clear the corresponding syscoreq_ctl bit to transition the RN to DISCONNECT state. The RN continues to receive and must respond to Snoop and DVM requests in this state.

DISABLED

When all outstanding Snoop and DVM responses have been received, CMN-600 clears the corresponding **syscoack_status** bit indicating the transition to DISABLED state. In this state, no snoop or DVM transactions are sent to the RN. Software must poll the **syscoack_status** register to ensure that this state transition has occurred before initiating RN power down.

——— **Note** ———

The following rules must be obeyed to adhere to the four-phase handshake protocol.

- The hardware interface is intended as the primary interface. The software interface is provided as an alternative for legacy RN devices and systems that do not support the hardware interface.
- Either hardware or software interface must be used, but not both. Coming out of Reset, the hardware interface is enabled by default. The first write into the **syscoreq_ctl** register disables hardware interface and enables software interface. A Reset is needed to re-enable hardware interface.
- When software interface is employed, **SYSCOREQ** signal must remain deasserted.
- When hardware interface is employed, software must not write to the syscoreq_ctl CR.

———————————

2.31 Link layer

CMN-600 provides link initialization, flow-control, and link deactivation functionality at the RN-F and SN-F device interfaces.

This functionality comprises the following mechanisms:

- A link initialization mechanism by which the receiving device communicates link layer credits, on each CHI channel that is present, to a transmitting device.
- A flow-control mechanism by which the transmitting device uses link layer credits to send CHI flits – one credit per flit. In turn, the receiving device sends these credits back to the transmitting device, one at a time, when it is done processing each flit to allow for subsequent flit transfers.

Note

The latency (in clock cycles) measured from the time a transmitting device uses a link layer credit to send a flit to the receiving device and the earliest time when it can receive that credit back from the receiving device and send a subsequent flit is called credit roundtrip latency.

- A link deactivation mechanism by which the transmitting device sends all unused link layer credits on each CHI channel back to the receiving device by sending corresponding link flits.

On flit upload channels, RN-F or SN-F is the transmitting device and CMN-600 is the receiving device. On flit download channels, CMN-600 is the transmitting device and RN-F or SN-F is the receiving device.

See the *Arm® AMBA® 5 CHI Architecture Specification* for a description of the functional requirements of the CHI link layer.

This section contains the following subsection:

- *2.31.1 Flit buffer sizing requirements* on page 2-166.

2.31.1 Flit buffer sizing requirements

This section describes CMN-600 flit buffer sizing requirements.

Flit buffer sizing at a receiving device is based on the following two factors:

1. To realize full link bandwidth a transmitting device must be able to send flits continuously in a pipelined fashion without stalling due to insufficient link layer credits from the receiving device. The *credit roundtrip latency* between the transmitting device and receiving device is a measure of the minimum number of link layer credits needed to prevent pipeline stalls.
2. At any given time, a receiving device must be capable of accepting and processing as many flits as the number of link layer credits it has outstanding at the transmitting device. Hence the number of link layer credits sent by a receiving device must not exceed its flit buffering and processing capabilities.

Based on the above two factors, flit buffer sizing and corresponding link layer crediting must reflect the *credit roundtrip latency* to achieve optimal flit transfer bandwidth between transmitting and receiving devices.

This section describes the flit buffer sizing and corresponding link layer crediting requirements to achieve optimal transfer bandwidth for flit uploads and downloads at RN-F or SN-F interfaces.

Flit uploads from RN-F or SN-F

For flit uploads, the number of flit buffers in CMN-600 is specified using the RXBUF_NUM_ENTRIES parameter.

Refer to *1.5 Configurable options* on page 1-22 for more information regarding the RXBUF_NUM_ENTRIES parameter.

For optimal flit transfer bandwidth, this parameter must be set equal to the *upload credit roundtrip latency* (UpCrdLat<ch>) which is computed using the following equation:

UpCrdLat<ch> = UpCrdLatInt<ch> + UpCrdLatExt<ch>, where

1. <ch> is the CHI channel and is one of REQ, RSP, SNP or DAT
2. *UpCrdLatInt<ch>* is the upload credit latency *inside* CMN-600. This latency is measured (in clock cycles) from the time RX<ch>FLITV input is asserted by the RN-F/SN-F for a flit uploaded to CMN-600 to the earliest time when RX<ch>LCRDV output is asserted by CMN-600 to the RN-F/SN-F after the flit is processed and the credit sent back. At the RN-F/SN-F interfaces, *UpCrdLatInt<ch>* = 1 on all CHI channels.

UpCrdLatExt<ch> is the upload credit latency *outside* CMN-600. This latency is measured (in clock cycles) from the time RX<ch>LCRDV output is asserted by CMN-600 when the credit is sent back to the RN-F or SN-F to the earliest time when RX<ch>FLITV input is asserted by the RN-F/SN-F when the credit is used to send a subsequent flit.

Flit downloads with RN-F or SN-F

For optimal flit downloads, the RN-F or SN-F must size its input buffers to reflect the *download credit roundtrip latency (DnCrdLat<ch>)*.

The *download credit roundtrip latency (DnCrdLat<ch>)* is computed using the following equation:

DnCrdLat<ch> = DnCrdLatInt<ch> + DnCrdLatExt<ch>, where

1. <ch> is the CHI channel and is one of REQ, RSP, SNP or DAT.
2. *DnCrdLatInt<ch>* is the download credit latency *inside* CMN-600. This latency is measured (in clock cycles) from the time RX<ch>LCRDV input is asserted by the RN-F or SN-F to CMN-600 to the earliest time when RX<ch>FLITV output is asserted by CMN-600 to the RN-F or SN-F for a flit using that credit. At the RN-F or SN-F interfaces, *DnCrdLatInt<ch>* = 2 on all CHI channels.

DnCrdLatExt<ch> is the download credit latency *outside* CMN-600. This latency is measured (in clock cycles) from the time RX<ch>FLITV output is asserted by CMN-600 for a flit downloaded to the RN-F or SN-F to the earliest time when RX<ch>LCRDV input is asserted when the corresponding credit is returned by the RN-F or SN-F to CMN-600.

2.32 CML *Symmetric Multi-Processor* (SMP) Support

SMP allows for a shared, common OS and memory to operate on multiple chips.

CML supports SMP systems if the systems were built using CMN-600-generated CMLs. An SMP mode option will be provided and when set will enable DVM, GIC-D, Exclusives, CPU-Event communication across CCIX links using micro-architected mechanism.

Microarchitecture support for propagating Trace Tag across CCIX links (called Remote Trace Tag) is also enabled in SMP mode only. Propagation of Remote Trace Tag is achieved by the sender CXG only on the outgoing CCIX request, and by the receiving CXG only from the incoming CCIX request. This ensures all subsequent CCIX messages that are part of the same transaction use the same CCIX TxnID. Similarly, propagation of remote Trace Tag is completed by the sender CXG only on the outgoing CCIX Snoop, and the receiving CXG only from the incoming CCIX snoop.

Chapter 3
Programmers Model

This chapter describes the programmers model.

It contains the following sections:

3.1 About the programmers model

A CMN-600 interconnect consists of a number of components, such as XP, RN-I, or DTC, that are accessed through memory mapped registers for configuration, topology, and status information.

The memory mapped registers are organized in a series of 16KB regions. They are accessed via CHI read and write commands.

A full description of a CMN-600 interconnect consists of a list of components, the compile time configuration options for each component, and the connectivity between the components. Software can determine the full configuration of the CMN-600 interconnect through a sequence of accesses to the configuration register space.

This section contains the following subsections:

3.1.1 Node configuration register address mapping

All CMN-600 configuration registers are mapped to an address range starting at PERIPHBASE with a maximum size of 64MB for a system with the maximum X and Y dimensions of 8 or less.

The reset value of PERIPHBASE is controlled by the CFGM_PERIPHBASE input signal.

All configuration, information, and status registers in a CMN-600 interconnect are grouped into 16KB regions each associated with a CMN-600 component instance. The base address of each region can be determined at compile time, or determined at run time through a software discovery mechanism.

Software discovery consists of three steps: (Refer to *2.5.4 Discovery tree structure* on page 2-64 for more information.)

1. Read information in the 16KB region at ROOTNODEBASE to determine the number of XPs in CMN-600 and the offset from PERIPHBASE for each XP's 16KB region.
2. Read information in the 16KB region associated with each XP to determine the components associated with that XP, topology information for those components, and the offset from PERIPHBASE for each component 16KB region.
3. Read information in the 16KB region associated with the component to determine the type of block and the configuration details of the component.

With this sequence, software can build a list of all components in the system and the addresses of their respective 16KB configuration regions.

3.1.2 Global configuration register region

The 16KB block at ROOTNODEBASE contains global information and configuration for CMN-600, as well as the first level of discovery information for components in the system.

Each XP Base Address register above contains the offset from PERIPHBASE for a 16KB region that contains the information about one XP and discovery information for components associated with that XP.

Refer to *3.3.1 Configuration master register descriptions* on page 3-195 for additional register information.

3.1.3 XP configuration register region

Each XP has a 16KB configuration register region with information about that XP and all associated components.

Refer to *3.3.6 XP register descriptions* on page 3-599 for more information.

3.1.4 Component configuration register region

Each non-XP component has a 16KB configuration register region. This region has programmable information, status, and configuration options for that component.

The contents are listed in the following table, including the number of 8-byte registers which fit in the space.

Table 3-1 Configuration register region values

Register sections	Relative offset	Absolute offset	Description
Discovery Register Section			
NODE INFO (node type, node ID)	`0x0`	`0x0`	Up to 16 registers
CHILD INFO (number of children, offset of the first child pointer register = `0x100`)	`0x80`	`0x80`	Up to 16 registers
CHILD POINTER registers	`0x100`	`0x100`	Up to 256 registers
UNIT REGISTER section	`0x900`	Unit-specific registers	
UNIT INFO	`0x0`	`0x900`	Up to 16 registers
UNIT SECURITY	`0x80`	`0x980`	Up to 16 registers
UNIT CTRL	`0x100`	`0xa00`	Up to 16 registers
UNIT QoS	`0x180`	`0xa80`	Up to 32 registers
UNIT DEBUG	`0x280`	`0xb80`	Up to 16 registers
UNIT OTHER	`0x300`	`0xc00`	Up to 128 registers
UNIT POWER	`0x700`	`0x1000`	4KB-aligned space – 512 registers
UNIT PMU	`0x1700`	`0x2000`	4KB-aligned space – 512 registers
UNIT RAS (secure RAS registers)	`0x2700`	`0x3000`	4KB-aligned space – 512 registers
UNIT RAS (non-secure RAS registers)	`0x2800`	`0x3100`	4KB-aligned space – 512 registers

3.1.5 Requirements of configuration register reads and writes

Reads and writes to the CMN-600 configuration registers must meet certain requirements.

If the following requirements are not met then this can result in unpredictable behavior.

- All accesses must be of device type, either:
  - Device, Strongly Ordered.
  - nGnRE, nGnRnE.
- All accesses must have a data size of 32 bits or 64 bits.
- All accesses must be natively aligned, that is:
  - 32-bit accesses must be aligned to a 32-bit boundary.
  - 64-bit accesses must be aligned to a 64-bit boundary.
- For configuration register writes, all bits, 32 or 64, must be written, that is, all byte lanes must be valid:
  - **WRSTB** must indicate that all bytes lanes are valid if the write transaction is from an AMBA AXI/ACE-Lite interface.
  - **BE** must indicate that all byte lanes are valid if the write transaction is sent from an AMBA 5 CHI interface.
- Secure registers can only be accessed by a Secure access, that is, NS = `0b0`. Non-secure registers can be accessed by either a Secure or Non-secure access.

Refer to *2.14 Error handling* on page 2-82 for more information on error signal handling.

3.2 Register summary

This section contains summary tables for all registers in CMN-600.

This section contains the following subsections:

3.2.1 Configuration master register summary

This section lists the configuration master registers used in CMN-600.

CFGM register summary

The following table shows the *CFGM* registers in offset order from the base memory address

Table 3-2 CFGM register summary

Offset	Name	Type	Description
0x0	por_cfgm_node_info	RO	*por_cfgm_node_info* on page 3-195
0x8	por_cfgm_periph_id_0_periph_id_1	RO	*por_cfgm_periph_id_0_periph_id_1* on page 3-196
0x10	por_cfgm_periph_id_2_periph_id_3	RO	*por_cfgm_periph_id_2_periph_id_3* on page 3-196
0x18	por_cfgm_periph_id_4_periph_id_5	RO	*por_cfgm_periph_id_4_periph_id_5* on page 3-198
0x20	por_cfgm_periph_id_6_periph_id_7	RO	*por_cfgm_periph_id_6_periph_id_7* on page 3-199
0x28	por_cfgm_component_id_0_component_id_1	RO	*por_cfgm_component_id_0_component_id_1* on page 3-200
0x30	por_cfgm_component_id_2_component_id_3	RO	*por_cfgm_component_id_2_component_id_3* on page 3-201
0x80	por_cfgm_child_info	RO	*por_cfgm_child_info* on page 3-202
0x980	por_cfgm_secure_access	RW	*por_cfgm_secure_access* on page 3-203
0x3000	por_cfgm_errgsr0	RO	*por_cfgm_errgsr0* on page 3-204
0x3008	por_cfgm_errgsr1	RO	*por_cfgm_errgsr1* on page 3-205
0x3010	por_cfgm_errgsr2	RO	*por_cfgm_errgsr2* on page 3-206
0x3018	por_cfgm_errgsr3	RO	*por_cfgm_errgsr3* on page 3-206
0x3020	por_cfgm_errgsr4	RO	*por_cfgm_errgsr4* on page 3-207
0x3080	por_cfgm_errgsr5	RO	*por_cfgm_errgsr5* on page 3-208
0x3088	por_cfgm_errgsr6	RO	*por_cfgm_errgsr6* on page 3-209
0x3090	por_cfgm_errgsr7	RO	*por_cfgm_errgsr7* on page 3-210
0x3098	por_cfgm_errgsr8	RO	*por_cfgm_errgsr8* on page 3-211

Table 3-2 CFGM register summary (continued)

Offset	Name	Type	Description
0x30A0	por_cfgm_errgsr9	RO	*por_cfgm_errgsr9* on page 3-211
0x3100	por_cfgm_errgsr0_NS	RO	*por_cfgm_errgsr0_NS* on page 3-212
0x3108	por_cfgm_errgsr1_NS	RO	*por_cfgm_errgsr1_NS* on page 3-213
0x3110	por_cfgm_errgsr2_NS	RO	*por_cfgm_errgsr2_NS* on page 3-214
0x3118	por_cfgm_errgsr3_NS	RO	*por_cfgm_errgsr3_NS* on page 3-215
0x3120	por_cfgm_errgsr4_NS	RO	*por_cfgm_errgsr4_NS* on page 3-216
0x3180	por_cfgm_errgsr5_NS	RO	*por_cfgm_errgsr5_NS* on page 3-216
0x3188	por_cfgm_errgsr6_NS	RO	*por_cfgm_errgsr6_NS* on page 3-217
0x3190	por_cfgm_errgsr7_NS	RO	*por_cfgm_errgsr7_NS* on page 3-218
0x3198	por_cfgm_errgsr8_NS	RO	*por_cfgm_errgsr8_NS* on page 3-219
0x31A0	por_cfgm_errgsr9_NS	RO	*por_cfgm_errgsr9_NS* on page 3-220
0x3FA8	por_cfgm_errdevaff	RO	*por_cfgm_errdevaff* on page 3-221
0x3FB8	por_cfgm_errdevarch	RO	*por_cfgm_errdevarch* on page 3-221
0x3FC8	por_cfgm_erridr	RO	*por_cfgm_erridr* on page 3-222
0x3FD0	por_cfgm_errpidr45	RO	*por_cfgm_errpidr45* on page 3-223
0x3FD8	por_cfgm_errpidr67	RO	*por_cfgm_errpidr67* on page 3-224
0x3FE0	por_cfgm_errpidr01	RO	*por_cfgm_errpidr01* on page 3-225
0x3FE8	por_cfgm_errpidr23	RO	*por_cfgm_errpidr23* on page 3-226
0x3FF0	por_cfgm_errcidr01	RO	*por_cfgm_errcidr01* on page 3-227
0x3FF8	por_cfgm_errcidr23	RO	*por_cfgm_errcidr23* on page 3-228
0x900	por_info_global	RO	*por_info_global* on page 3-229
0x1000	por_ppu_int_enable	RW	*por_ppu_int_enable* on page 3-231
0x1008	por_ppu_int_status	W1C	*por_ppu_int_status* on page 3-232
0x1010	por_ppu_qactive_hyst	RW	*por_ppu_qactive_hyst* on page 3-233
0x100	por_cfgm_child_pointer_0	RO	*por_cfgm_child_pointer_0* on page 3-234

3.2.2 DN register summary

This section lists the DN registers used in CMN-600.

DN register summary

The following table shows the *DN* registers in offset order from the base memory address

Table 3-3 DN register summary

Offset	Name	Type	Description
0x0	por_dn_node_info	RO	*por_dn_node_info* on page 3-235
0x80	por_dn_child_info	RO	*por_dn_child_info* on page 3-236

Table 3-3 DN register summary (continued)

Offset	Name	Type	Description
0x900	por_dn_build_info	RO	*por_dn_build_info* on page 3-236
0x980	por_dn_secure_register_groups_override	RW	*por_dn_secure_register_groups_override* on page 3-237
0xA00	por_dn_aux_ctl	RW	*por_dn_aux_ctl* on page 3-238
0xC00	por_dn_vmf0_ctrl	RW	*por_dn_vmf0_ctrl* on page 3-239
0xC08	por_dn_vmf0_rnf0	RW	*por_dn_vmf0_rnf0* on page 3-241
0xC10	por_dn_vmf0_rnd	RW	*por_dn_vmf0_rnd* on page 3-241
0xC18	por_dn_vmf0_cxra	RW	*por_dn_vmf0_cxra* on page 3-242
0xC20	por_dn_vmf1_ctrl	RW	*por_dn_vmf1_ctrl* on page 3-243
0xC28	por_dn_vmf1_rnf0	RW	*por_dn_vmf1_rnf0* on page 3-244
0xC30	por_dn_vmf1_rnd	RW	*por_dn_vmf1_rnd* on page 3-245
0xC38	por_dn_vmf1_cxra	RW	*por_dn_vmf1_cxra* on page 3-246
0xC40	por_dn_vmf2_ctrl	RW	*por_dn_vmf2_ctrl* on page 3-247
0xC48	por_dn_vmf2_rnf0	RW	*por_dn_vmf2_rnf0* on page 3-248
0xC50	por_dn_vmf2_rnd	RW	*por_dn_vmf2_rnd* on page 3-249
0xC58	por_dn_vmf2_cxra	RW	*por_dn_vmf2_cxra* on page 3-250
0xC60	por_dn_vmf3_ctrl	RW	*por_dn_vmf3_ctrl* on page 3-251
0xC68	por_dn_vmf3_rnf0	RW	*por_dn_vmf3_rnf0* on page 3-252
0xC70	por_dn_vmf3_rnd	RW	*por_dn_vmf3_rnd* on page 3-253
0xC78	por_dn_vmf3_cxra	RW	*por_dn_vmf3_cxra* on page 3-254
0xC80	por_dn_vmf4_ctrl	RW	*por_dn_vmf4_ctrl* on page 3-255
0xC88	por_dn_vmf4_rnf0	RW	*por_dn_vmf4_rnf0* on page 3-256
0xC90	por_dn_vmf4_rnd	RW	*por_dn_vmf4_rnd* on page 3-257
0xC98	por_dn_vmf4_cxra	RW	*por_dn_vmf4_cxra* on page 3-258
0xCA0	por_dn_vmf5_ctrl	RW	*por_dn_vmf5_ctrl* on page 3-259
0xCA8	por_dn_vmf5_rnf0	RW	*por_dn_vmf5_rnf0* on page 3-260
0xCB0	por_dn_vmf5_rnd	RW	*por_dn_vmf5_rnd* on page 3-261
0xCB8	por_dn_vmf5_cxra	RW	*por_dn_vmf5_cxra* on page 3-262
0xCC0	por_dn_vmf6_ctrl	RW	*por_dn_vmf6_ctrl* on page 3-263
0xCC8	por_dn_vmf6_rnf0	RW	*por_dn_vmf6_rnf0* on page 3-264
0xCD0	por_dn_vmf6_rnd	RW	*por_dn_vmf6_rnd* on page 3-265
0xCD8	por_dn_vmf6_cxra	RW	*por_dn_vmf6_cxra* on page 3-266
0xCE0	por_dn_vmf7_ctrl	RW	*por_dn_vmf7_ctrl* on page 3-267
0xCE8	por_dn_vmf7_rnf0	RW	*por_dn_vmf7_rnf0* on page 3-268
0xCF0	por_dn_vmf7_rnd	RW	*por_dn_vmf7_rnd* on page 3-269
0xCF8	por_dn_vmf7_cxra	RW	*por_dn_vmf7_cxra* on page 3-270

Table 3-3 DN register summary (continued)

Offset	Name	Type	Description
0xD00	por_dn_vmf8_ctrl	RW	*por_dn_vmf8_ctrl* on page 3-271
0xD08	por_dn_vmf8_rnf0	RW	*por_dn_vmf8_rnf0* on page 3-272
0xD10	por_dn_vmf8_rnd	RW	*por_dn_vmf8_rnd* on page 3-273
0xD18	por_dn_vmf8_cxra	RW	*por_dn_vmf8_cxra* on page 3-274
0xD20	por_dn_vmf9_ctrl	RW	*por_dn_vmf9_ctrl* on page 3-275
0xD28	por_dn_vmf9_rnf0	RW	*por_dn_vmf9_rnf0* on page 3-276
0xD30	por_dn_vmf9_rnd	RW	*por_dn_vmf9_rnd* on page 3-277
0xD38	por_dn_vmf9_cxra	RW	*por_dn_vmf9_cxra* on page 3-278
0xD40	por_dn_vmf10_ctrl	RW	*por_dn_vmf10_ctrl* on page 3-279
0xD48	por_dn_vmf10_rnf0	RW	*por_dn_vmf10_rnf0* on page 3-280
0xD50	por_dn_vmf10_rnd	RW	*por_dn_vmf10_rnd* on page 3-281
0xD58	por_dn_vmf10_cxra	RW	*por_dn_vmf10_cxra* on page 3-282
0xD60	por_dn_vmf11_ctrl	RW	*por_dn_vmf11_ctrl* on page 3-283
0xD68	por_dn_vmf11_rnf0	RW	*por_dn_vmf11_rnf0* on page 3-284
0xD70	por_dn_vmf11_rnd	RW	*por_dn_vmf11_rnd* on page 3-285
0xD78	por_dn_vmf11_cxra	RW	*por_dn_vmf11_cxra* on page 3-286
0xD80	por_dn_vmf12_ctrl	RW	*por_dn_vmf12_ctrl* on page 3-287
0xD88	por_dn_vmf12_rnf0	RW	*por_dn_vmf12_rnf0* on page 3-288
0xD90	por_dn_vmf12_rnd	RW	*por_dn_vmf12_rnd* on page 3-289
0xD98	por_dn_vmf12_cxra	RW	*por_dn_vmf12_cxra* on page 3-290
0xDA0	por_dn_vmf13_ctrl	RW	*por_dn_vmf13_ctrl* on page 3-291
0xDA8	por_dn_vmf13_rnf0	RW	*por_dn_vmf13_rnf0* on page 3-292
0xDB0	por_dn_vmf13_rnd	RW	*por_dn_vmf13_rnd* on page 3-293
0xDB8	por_dn_vmf13_cxra	RW	*por_dn_vmf13_cxra* on page 3-294
0xDC0	por_dn_vmf14_ctrl	RW	*por_dn_vmf14_ctrl* on page 3-295
0xDC8	por_dn_vmf14_rnf0	RW	*por_dn_vmf14_rnf0* on page 3-296
0xDD0	por_dn_vmf14_rnd	RW	*por_dn_vmf14_rnd* on page 3-297
0xDD8	por_dn_vmf14_cxra	RW	*por_dn_vmf14_cxra* on page 3-298
0xDE0	por_dn_vmf15_ctrl	RW	*por_dn_vmf15_ctrl* on page 3-299
0xDE8	por_dn_vmf15_rnf0	RW	*por_dn_vmf15_rnf0* on page 3-300
0xDF0	por_dn_vmf15_rnd	RW	*por_dn_vmf15_rnd* on page 3-301
0xDF8	por_dn_vmf15_cxra	RW	*por_dn_vmf15_cxra* on page 3-302
0x2000	por_dn_pmu_event_sel	RW	*por_dn_pmu_event_sel* on page 3-303

3.2.3 Debug and trace register summary

This section lists the debug and trace registers used in CMN-600.

DT register summary

The following table shows the *DT* registers in offset order from the base memory address

Table 3-4 DT register summary

Offset	Name	Type	Description
0x0	por_dt_node_info	RO	*por_dt_node_info* on page 3-306
0x80	por_dt_child_info	RO	*por_dt_child_info* on page 3-307
0x980	por_dt_secure_access	RW	*por_dt_secure_access* on page 3-307
0xA00	por_dt_dtc_ctl	RW	*por_dt_dtc_ctl* on page 3-309
0xA10	por_dt_trigger_status	RO	*por_dt_trigger_status* on page 3-310
0xA20	por_dt_trigger_status_clr	WO	*por_dt_trigger_status_clr* on page 3-311
0xA30	por_dt_trace_control	RW	*por_dt_trace_control* on page 3-312
0xA48	por_dt_traceid	RW	*por_dt_traceid* on page 3-313
0x2000	por_dt_pmevcntAB	RW	*por_dt_pmevcntAB* on page 3-314
0x2010	por_dt_pmevcntCD	RW	*por_dt_pmevcntCD* on page 3-315
0x2020	por_dt_pmevcntEF	RW	*por_dt_pmevcntEF* on page 3-315
0x2030	por_dt_pmevcntGH	RW	*por_dt_pmevcntGH* on page 3-316
0x2040	por_dt_pmccntr	RW	*por_dt_pmccntr* on page 3-317
0x2050	por_dt_pmevcntsrAB	RW	*por_dt_pmevcntsrAB* on page 3-318
0x2060	por_dt_pmevcntsrCD	RW	*por_dt_pmevcntsrCD* on page 3-319
0x2070	por_dt_pmevcntsrEF	RW	*por_dt_pmevcntsrEF* on page 3-320
0x2080	por_dt_pmevcntsrGH	RW	*por_dt_pmevcntsrGH* on page 3-320
0x2090	por_dt_pmccntrsr	RW	*por_dt_pmccntrsr* on page 3-321
0x2100	por_dt_pmcr	RW	*por_dt_pmcr* on page 3-322
0x2118	por_dt_pmovsr	RO	*por_dt_pmovsr* on page 3-323
0x2120	por_dt_pmovsr_clr	WO	*por_dt_pmovsr_clr* on page 3-324
0x2128	por_dt_pmssr	RO	*por_dt_pmssr* on page 3-325
0x2130	por_dt_pmsrr	WO	*por_dt_pmsrr* on page 3-326
0x2DA0	por_dt_claim	RW	*por_dt_claim* on page 3-327
0x2DA8	por_dt_devaff	RO	*por_dt_devaff* on page 3-328
0x2DB0	por_dt_lsr	RO	*por_dt_lsr* on page 3-329
0x2DB8	por_dt_authstatus_devarch	RO	*por_dt_authstatus_devarch* on page 3-330
0x2DC0	por_dt_devid	RO	*por_dt_devid* on page 3-331
0x2DC8	por_dt_devtype	RO	*por_dt_devtype* on page 3-332
0x2DD0	por_dt_pidr45	RO	*por_dt_pidr45* on page 3-333

Table 3-4 DT register summary (continued)

Offset	Name	Type	Description
0x2DD8	por_dt_pidr67	RO	*por_dt_pidr67* on page 3-334
0x2DE0	por_dt_pidr01	RO	*por_dt_pidr01* on page 3-335
0x2DE8	por_dt_pidr23	RO	*por_dt_pidr23* on page 3-336
0x2DF0	por_dt_cidr01	RO	*por_dt_cidr01* on page 3-337
0x2DF8	por_dt_cidr23	RO	*por_dt_cidr23* on page 3-338

3.2.4 HN-F register summary

This section lists the HN-F registers used in CMN-600.

HNF register summary

The following table shows the *HNF* registers in offset order from the base memory address

Table 3-5 HNF register summary

Offset	Name	Type	Description
0x0	por_hnf_node_info	RO	*por_hnf_node_info* on page 3-340
0x80	por_hnf_child_info	RO	*por_hnf_child_info* on page 3-341
0x980	por_hnf_secure_register_groups_override	RW	*por_hnf_secure_register_groups_override* on page 3-341
0x900	por_hnf_unit_info	RO	*por_hnf_unit_info* on page 3-343
0xA00	por_hnf_cfg_ctl	RW	*por_hnf_cfg_ctl* on page 3-344
0xA08	por_hnf_aux_ctl	RW	*por_hnf_aux_ctl* on page 3-346
0xA10	por_hnf_r2_aux_ctl	RW	*por_hnf_r2_aux_ctl* on page 3-350
0x1000	por_hnf_ppu_pwpr	RW	*por_hnf_ppu_pwpr* on page 3-351
0x1008	por_hnf_ppu_pwsr	RO	*por_hnf_ppu_pwsr* on page 3-352
0x1014	por_hnf_ppu_misr	RO	*por_hnf_ppu_misr* on page 3-353
0x1FB0	por_hnf_ppu_idr0	RO	*por_hnf_ppu_idr0* on page 3-353
0x1FB4	por_hnf_ppu_idr1	RO	*por_hnf_ppu_idr1* on page 3-355
0x1FC8	por_hnf_ppu_iidr	RO	*por_hnf_ppu_iidr* on page 3-356
0x1FCC	por_hnf_ppu_aidr	RO	*por_hnf_ppu_aidr* on page 3-357
0x1100	por_hnf_ppu_dyn_ret_threshold	RW	*por_hnf_ppu_dyn_ret_threshold* on page 3-357
0xA80	por_hnf_qos_band	RO	*por_hnf_qos_band* on page 3-358
0xA88	por_hnf_qos_reservation	RW	*por_hnf_qos_reservation* on page 3-359
0xA90	por_hnf_rn_starvation	RW	*por_hnf_rn_starvation* on page 3-361
0x3000	por_hnf_errfr	RO	*por_hnf_errfr* on page 3-363
0x3008	por_hnf_errctlr	RW	*por_hnf_errctlr* on page 3-364
0x3010	por_hnf_errstatus	W1C	*por_hnf_errstatus* on page 3-365
0x3018	por_hnf_erraddr	RW	*por_hnf_erraddr* on page 3-367

Table 3-5 HNF register summary (continued)

Offset	Name	Type	Description
0x3020	por_hnf_errmisc	RW	*por_hnf_errmisc* on page 3-368
0x3030	por_hnf_err_inj	RW	*por_hnf_err_inj* on page 3-370
0x3038	por_hnf_byte_par_err_inj	WO	*por_hnf_byte_par_err_inj* on page 3-371
0x3100	por_hnf_errfr_NS	RO	*por_hnf_errfr_NS* on page 3-372
0x3108	por_hnf_errctlr_NS	RW	*por_hnf_errctlr_NS* on page 3-374
0x3110	por_hnf_errstatus_NS	W1C	*por_hnf_errstatus_NS* on page 3-375
0x3118	por_hnf_erraddr_NS	RW	*por_hnf_erraddr_NS* on page 3-377
0x3120	por_hnf_errmisc_NS	RW	*por_hnf_errmisc_NS* on page 3-378
0xC00	por_hnf_slc_lock_ways	RW	*por_hnf_slc_lock_ways* on page 3-380
0xC08	por_hnf_slc_lock_base0	RW	*por_hnf_slc_lock_base0* on page 3-381
0xC10	por_hnf_slc_lock_base1	RW	*por_hnf_slc_lock_base1* on page 3-382
0xC18	por_hnf_slc_lock_base2	RW	*por_hnf_slc_lock_base2* on page 3-383
0xC20	por_hnf_slc_lock_base3	RW	*por_hnf_slc_lock_base3* on page 3-384
0xC30	por_hnf_rni_region_vec	RW	*por_hnf_rni_region_vec* on page 3-385
0xC38	por_hnf_rnf_region_vec	RW	*por_hnf_rnf_region_vec* on page 3-386
0xC40	por_hnf_rnd_region_vec	RW	*por_hnf_rnd_region_vec* on page 3-387
0xC48	por_hnf_slcway_partition0_rnf_vec	RW	*por_hnf_slcway_partition0_rnf_vec* on page 3-388
0xC50	por_hnf_slcway_partition1_rnf_vec	RW	*por_hnf_slcway_partition1_rnf_vec* on page 3-389
0xC58	por_hnf_slcway_partition2_rnf_vec	RW	*por_hnf_slcway_partition2_rnf_vec* on page 3-390
0xC60	por_hnf_slcway_partition3_rnf_vec	RW	*por_hnf_slcway_partition3_rnf_vec* on page 3-390
0xC28	por_hnf_rnf_region_vec1	RW	*por_hnf_rnf_region_vec1* on page 3-391
0xCB0	por_hnf_slcway_partition0_rnf_vec1	RW	*por_hnf_slcway_partition0_rnf_vec1* on page 3-392
0xCB8	por_hnf_slcway_partition1_rnf_vec1	RW	*por_hnf_slcway_partition1_rnf_vec1* on page 3-393
0xCC0	por_hnf_slcway_partition2_rnf_vec1	RW	*por_hnf_slcway_partition2_rnf_vec1* on page 3-394
0xCC8	por_hnf_slcway_partition3_rnf_vec1	RW	*por_hnf_slcway_partition3_rnf_vec1* on page 3-395
0xC68	por_hnf_slcway_partition0_rni_vec	RW	*por_hnf_slcway_partition0_rni_vec* on page 3-396
0xC70	por_hnf_slcway_partition1_rni_vec	RW	*por_hnf_slcway_partition1_rni_vec* on page 3-397
0xC78	por_hnf_slcway_partition2_rni_vec	RW	*por_hnf_slcway_partition2_rni_vec* on page 3-397
0xC80	por_hnf_slcway_partition3_rni_vec	RW	*por_hnf_slcway_partition3_rni_vec* on page 3-398
0xC88	por_hnf_slcway_partition0_rnd_vec	RW	*por_hnf_slcway_partition0_rnd_vec* on page 3-399
0xC90	por_hnf_slcway_partition1_rnd_vec	RW	*por_hnf_slcway_partition1_rnd_vec* on page 3-400
0xC98	por_hnf_slcway_partition2_rnd_vec	RW	*por_hnf_slcway_partition2_rnd_vec* on page 3-401
0xCA0	por_hnf_slcway_partition3_rnd_vec	RW	*por_hnf_slcway_partition3_rnd_vec* on page 3-402
0xCA8	por_hnf_rn_region_lock	RW	*por_hnf_rn_region_lock* on page 3-403
0xD00	por_hnf_sam_control	RW	*por_hnf_sam_control* on page 3-404

Table 3-5 HNF register summary (continued)

Offset	Name	Type	Description
0xD08	por_hnf_sam_memregion0	RW	*por_hnf_sam_memregion0* on page 3-406
0xD10	por_hnf_sam_memregion1	RW	*por_hnf_sam_memregion1* on page 3-407
0xD18	por_hnf_sam_sn_properties	RW	*por_hnf_sam_sn_properties* on page 3-408
0xD20	por_hnf_sam_6sn_nodeid	RW	*por_hnf_sam_6sn_nodeid* on page 3-411
0xD28	por_hnf_rn_phys_id0	RW	*por_hnf_rn_phys_id0* on page 3-412
0xD30	por_hnf_rn_phys_id1	RW	*por_hnf_rn_phys_id1* on page 3-415
0xD38	por_hnf_rn_phys_id2	RW	*por_hnf_rn_phys_id2* on page 3-417
0xD40	por_hnf_rn_phys_id3	RW	*por_hnf_rn_phys_id3* on page 3-419
0xD48	por_hnf_rn_phys_id4	RW	*por_hnf_rn_phys_id4* on page 3-421
0xD50	por_hnf_rn_phys_id5	RW	*por_hnf_rn_phys_id5* on page 3-423
0xD58	por_hnf_rn_phys_id6	RW	*por_hnf_rn_phys_id6* on page 3-425
0xD60	por_hnf_rn_phys_id7	RW	*por_hnf_rn_phys_id7* on page 3-427
0xD68	por_hnf_rn_phys_id8	RW	*por_hnf_rn_phys_id8* on page 3-429
0xD70	por_hnf_rn_phys_id9	RW	*por_hnf_rn_phys_id9* on page 3-431
0xD78	por_hnf_rn_phys_id10	RW	*por_hnf_rn_phys_id10* on page 3-433
0xD80	por_hnf_rn_phys_id11	RW	*por_hnf_rn_phys_id11* on page 3-435
0xD88	por_hnf_rn_phys_id12	RW	*por_hnf_rn_phys_id12* on page 3-437
0xD90	por_hnf_rn_phys_id13	RW	*por_hnf_rn_phys_id13* on page 3-439
0xD98	por_hnf_rn_phys_id14	RW	*por_hnf_rn_phys_id14* on page 3-441
0xDA0	por_hnf_rn_phys_id15	RW	*por_hnf_rn_phys_id15* on page 3-443
0xDA8	por_hnf_rn_phys_id16	RW	*por_hnf_rn_phys_id16* on page 3-445
0xDB0	por_hnf_rn_phys_id17	RW	*por_hnf_rn_phys_id17* on page 3-447
0xDB8	por_hnf_rn_phys_id18	RW	*por_hnf_rn_phys_id18* on page 3-449
0xDC0	por_hnf_rn_phys_id19	RW	*por_hnf_rn_phys_id19* on page 3-451
0xDC8	por_hnf_rn_phys_id20	RW	*por_hnf_rn_phys_id20* on page 3-453
0xDD0	por_hnf_rn_phys_id21	RW	*por_hnf_rn_phys_id21* on page 3-455
0xDD8	por_hnf_rn_phys_id22	RW	*por_hnf_rn_phys_id22* on page 3-457
0xDE0	por_hnf_rn_phys_id23	RW	*por_hnf_rn_phys_id23* on page 3-459
0xDE8	por_hnf_rn_phys_id24	RW	*por_hnf_rn_phys_id24* on page 3-461
0xDF0	por_hnf_rn_phys_id25	RW	*por_hnf_rn_phys_id25* on page 3-463
0xDF8	por_hnf_rn_phys_id26	RW	*por_hnf_rn_phys_id26* on page 3-465
0xE00	por_hnf_rn_phys_id27	RW	*por_hnf_rn_phys_id27* on page 3-467
0xE08	por_hnf_rn_phys_id28	RW	*por_hnf_rn_phys_id28* on page 3-469
0xE10	por_hnf_rn_phys_id29	RW	*por_hnf_rn_phys_id29* on page 3-471
0xE18	por_hnf_rn_phys_id30	RW	*por_hnf_rn_phys_id30* on page 3-473

Table 3-5 HNF register summary (continued)

Offset	Name	Type	Description
0xE20	por_hnf_rn_phys_id31	RW	*por_hnf_rn_phys_id31* on page 3-475
0xF00	por_hnf_sf_cxg_blocked_ways	RW	*por_hnf_sf_cxg_blocked_ways* on page 3-477
0xF10	por_hnf_cml_port_aggr_grp0_add_mask	RW	*por_hnf_cml_port_aggr_grp0_add_mask* on page 3-478
0xF18	por_hnf_cml_port_aggr_grp1_add_mask	RW	*por_hnf_cml_port_aggr_grp1_add_mask* on page 3-479
0xF28	por_hnf_cml_port_aggr_grp0_reg	RW	*por_hnf_cml_port_aggr_grp0_reg* on page 3-480
0xF30	por_hnf_cml_port_aggr_grp1_reg	RW	*por_hnf_cml_port_aggr_grp1_reg* on page 3-482
0xF40	hn_sam_hash_addr_mask_reg	RW	*hn_sam_hash_addr_mask_reg* on page 3-483
0xF48	hn_sam_region_cmp_addr_mask_reg	RW	*hn_sam_region_cmp_addr_mask_reg* on page 3-484
0xF50	por_hnf_abf_lo_addr	RW	*por_hnf_abf_lo_addr* on page 3-485
0xF58	por_hnf_abf_hi_addr	RW	*por_hnf_abf_hi_addr* on page 3-486
0xF60	por_hnf_abf_pr	RW	*por_hnf_abf_pr* on page 3-487
0xF68	por_hnf_abf_sr	RO	*por_hnf_abf_sr* on page 3-488
0xE28	por_hnf_rn_phys_id32	RW	*por_hnf_rn_phys_id32* on page 3-489
0xE30	por_hnf_rn_phys_id33	RW	*por_hnf_rn_phys_id33* on page 3-491
0xE38	por_hnf_rn_phys_id34	RW	*por_hnf_rn_phys_id34* on page 3-493
0xE40	por_hnf_rn_phys_id35	RW	*por_hnf_rn_phys_id35* on page 3-495
0xE48	por_hnf_rn_phys_id36	RW	*por_hnf_rn_phys_id36* on page 3-497
0xE50	por_hnf_rn_phys_id37	RW	*por_hnf_rn_phys_id37* on page 3-499
0xE58	por_hnf_rn_phys_id38	RW	*por_hnf_rn_phys_id38* on page 3-501
0xE60	por_hnf_rn_phys_id39	RW	*por_hnf_rn_phys_id39* on page 3-503
0xE68	por_hnf_rn_phys_id40	RW	*por_hnf_rn_phys_id40* on page 3-505
0xE70	por_hnf_rn_phys_id41	RW	*por_hnf_rn_phys_id41* on page 3-507
0xE78	por_hnf_rn_phys_id42	RW	*por_hnf_rn_phys_id42* on page 3-509
0xE80	por_hnf_rn_phys_id43	RW	*por_hnf_rn_phys_id43* on page 3-511
0xE88	por_hnf_rn_phys_id44	RW	*por_hnf_rn_phys_id44* on page 3-513
0xE90	por_hnf_rn_phys_id45	RW	*por_hnf_rn_phys_id45* on page 3-515
0xE98	por_hnf_rn_phys_id46	RW	*por_hnf_rn_phys_id46* on page 3-517
0xEA0	por_hnf_rn_phys_id47	RW	*por_hnf_rn_phys_id47* on page 3-519
0xEA8	por_hnf_rn_phys_id48	RW	*por_hnf_rn_phys_id48* on page 3-521
0xEB0	por_hnf_rn_phys_id49	RW	*por_hnf_rn_phys_id49* on page 3-523
0xEB8	por_hnf_rn_phys_id50	RW	*por_hnf_rn_phys_id50* on page 3-525
0xEC0	por_hnf_rn_phys_id51	RW	*por_hnf_rn_phys_id51* on page 3-527
0xEC8	por_hnf_rn_phys_id52	RW	*por_hnf_rn_phys_id52* on page 3-529
0xED0	por_hnf_rn_phys_id53	RW	*por_hnf_rn_phys_id53* on page 3-531
0xED8	por_hnf_rn_phys_id54	RW	*por_hnf_rn_phys_id54* on page 3-533

Table 3-5 HNF register summary (continued)

Offset	Name	Type	Description
0xEE0	por_hnf_rn_phys_id55	RW	*por_hnf_rn_phys_id55* on page 3-535
0xEE8	por_hnf_rn_phys_id56	RW	*por_hnf_rn_phys_id56* on page 3-537
0xEF0	por_hnf_rn_phys_id57	RW	*por_hnf_rn_phys_id57* on page 3-539
0xEF8	por_hnf_rn_phys_id58	RW	*por_hnf_rn_phys_id58* on page 3-541
0xF70	por_hnf_rn_phys_id59	RW	*por_hnf_rn_phys_id59* on page 3-543
0xF78	por_hnf_rn_phys_id60	RW	*por_hnf_rn_phys_id60* on page 3-545
0xF80	por_hnf_rn_phys_id61	RW	*por_hnf_rn_phys_id61* on page 3-547
0xF88	por_hnf_rn_phys_id62	RW	*por_hnf_rn_phys_id62* on page 3-549
0xF90	por_hnf_rn_phys_id63	RW	*por_hnf_rn_phys_id63* on page 3-551
0xF98	por_hnf_ldid_map_table_reg0	RW	*por_hnf_ldid_map_table_reg0* on page 3-553
0xFA0	por_hnf_ldid_map_table_reg1	RW	*por_hnf_ldid_map_table_reg1* on page 3-555
0xFA8	por_hnf_ldid_map_table_reg2	RW	*por_hnf_ldid_map_table_reg2* on page 3-556
0xFB0	por_hnf_ldid_map_table_reg3	RW	*por_hnf_ldid_map_table_reg3* on page 3-557
0xB80	por_hnf_cfg_slcsf_dbgrd	WO	*por_hnf_cfg_slcsf_dbgrd* on page 3-559
0xB88	por_hnf_slc_cache_access_slc_tag	RO	*por_hnf_slc_cache_access_slc_tag* on page 3-560
0xB90	por_hnf_slc_cache_access_slc_data	RO	*por_hnf_slc_cache_access_slc_data* on page 3-561
0xB98	por_hnf_slc_cache_access_sf_tag	RO	*por_hnf_slc_cache_access_sf_tag* on page 3-562
0xBA0	por_hnf_slc_cache_access_sf_tag1	RO	*por_hnf_slc_cache_access_sf_tag1* on page 3-563
0xBA8	por_hnf_slc_cache_access_sf_tag2	RO	*por_hnf_slc_cache_access_sf_tag2* on page 3-563
0x2000	por_hnf_pmu_event_sel	RW	*por_hnf_pmu_event_sel* on page 3-564

3.2.5 HN-I register summary

This section lists the HN-I registers used in CMN-600.

HNI register summary

The following table shows the *HNI* registers in offset order from the base memory address

Table 3-6 HNI register summary

Offset	Name	Type	Description
0x0	por_hni_node_info	RO	*por_hni_node_info* on page 3-569
0x80	por_hni_child_info	RO	*por_hni_child_info* on page 3-570
0x980	por_hni_secure_register_groups_override	RW	*por_hni_secure_register_groups_override* on page 3-570
0x900	por_hni_unit_info	RO	*por_hni_unit_info* on page 3-571
0xC00	por_hni_sam_addrregion0_cfg	RW	*por_hni_sam_addrregion0_cfg* on page 3-573
0xC08	por_hni_sam_addrregion1_cfg	RW	*por_hni_sam_addrregion1_cfg* on page 3-574
0xC10	por_hni_sam_addrregion2_cfg	RW	*por_hni_sam_addrregion2_cfg* on page 3-576

Table 3-6 HNI register summary (continued)

Offset	Name	Type	Description
0xC18	por_hni_sam_addrregion3_cfg	RW	*por_hni_sam_addrregion3_cfg* on page 3-578
0xA00	por_hni_cfg_ctl	RW	*por_hni_cfg_ctl* on page 3-579
0xA08	por_hni_aux_ctl	RW	*por_hni_aux_ctl* on page 3-580
0x3000	por_hni_errfr	RO	*por_hni_errfr* on page 3-581
0x3008	por_hni_errctlr	RW	*por_hni_errctlr* on page 3-582
0x3010	por_hni_errstatus	W1C	*por_hni_errstatus* on page 3-584
0x3018	por_hni_erraddr	RW	*por_hni_erraddr* on page 3-585
0x3020	por_hni_errmisc	RW	*por_hni_errmisc* on page 3-586
0x3100	por_hni_errfr_NS	RO	*por_hni_errfr_NS* on page 3-588
0x3108	por_hni_errctlr_NS	RW	*por_hni_errctlr_NS* on page 3-590
0x3110	por_hni_errstatus_NS	W1C	*por_hni_errstatus_NS* on page 3-591
0x3118	por_hni_erraddr_NS	RW	*por_hni_erraddr_NS* on page 3-593
0x3120	por_hni_errmisc_NS	RW	*por_hni_errmisc_NS* on page 3-594
0x2000	por_hni_pmu_event_sel	RW	*por_hni_pmu_event_sel* on page 3-596

3.2.6 XP register summary

This section lists the XP registers used in CMN-600.

XP register summary

The following table shows the *MXP* registers in offset order from the base memory address

Table 3-7 MXP register summary

Offset	Name	Type	Description
0x0	por_mxp_node_info	RO	*por_mxp_node_info* on page 3-599
0x8	por_mxp_device_port_connect_info_p0	RO	*por_mxp_device_port_connect_info_p0* on page 3-600
0x10	por_mxp_device_port_connect_info_p1	RO	*por_mxp_device_port_connect_info_p1* on page 3-601
0x18	por_mxp_mesh_port_connect_info_east	RO	*por_mxp_mesh_port_connect_info_east* on page 3-603
0x20	por_mxp_mesh_port_connect_info_north	RO	*por_mxp_mesh_port_connect_info_north* on page 3-604
0x80	por_mxp_child_info	RO	*por_mxp_child_info* on page 3-605
0x100	por_mxp_child_pointer_0	RO	*por_mxp_child_pointer_0* on page 3-606
0x108	por_mxp_child_pointer_1	RO	*por_mxp_child_pointer_1* on page 3-607
0x110	por_mxp_child_pointer_2	RO	*por_mxp_child_pointer_2* on page 3-608
0x118	por_mxp_child_pointer_3	RO	*por_mxp_child_pointer_3* on page 3-609
0x120	por_mxp_child_pointer_4	RO	*por_mxp_child_pointer_4* on page 3-610
0x128	por_mxp_child_pointer_5	RO	*por_mxp_child_pointer_5* on page 3-611
0x130	por_mxp_child_pointer_6	RO	*por_mxp_child_pointer_6* on page 3-612

Table 3-7 MXP register summary (continued)

Offset	Name	Type	Description
0x138	por_mxp_child_pointer_7	RO	*por_mxp_child_pointer_7* on page 3-613
0x140	por_mxp_child_pointer_8	RO	*por_mxp_child_pointer_8* on page 3-614
0x148	por_mxp_child_pointer_9	RO	*por_mxp_child_pointer_9* on page 3-615
0x150	por_mxp_child_pointer_10	RO	*por_mxp_child_pointer_10* on page 3-616
0x158	por_mxp_child_pointer_11	RO	*por_mxp_child_pointer_11* on page 3-617
0x160	por_mxp_child_pointer_12	RO	*por_mxp_child_pointer_12* on page 3-618
0x168	por_mxp_child_pointer_13	RO	*por_mxp_child_pointer_13* on page 3-619
0x170	por_mxp_child_pointer_14	RO	*por_mxp_child_pointer_14* on page 3-620
0x178	por_mxp_child_pointer_15	RO	*por_mxp_child_pointer_15* on page 3-621
0x900	por_mxp_p0_info	RO	*por_mxp_p0_info* on page 3-622
0x908	por_mxp_p1_info	RO	*por_mxp_p1_info* on page 3-623
0x980	por_mxp_secure_register_groups_override	RW	*por_mxp_secure_register_groups_override* on page 3-625
0xA00	por_mxp_aux_ctl	RW	*por_mxp_aux_ctl* on page 3-626
0xA80	por_mxp_p0_qos_control	RW	*por_mxp_p0_qos_control* on page 3-627
0xA88	por_mxp_p0_qos_lat_tgt	RW	*por_mxp_p0_qos_lat_tgt* on page 3-628
0xA90	por_mxp_p0_qos_lat_scale	RW	*por_mxp_p0_qos_lat_scale* on page 3-629
0xA98	por_mxp_p0_qos_lat_range	RW	*por_mxp_p0_qos_lat_range* on page 3-630
0xAA0	por_mxp_p1_qos_control	RW	*por_mxp_p1_qos_control* on page 3-631
0xAA8	por_mxp_p1_qos_lat_tgt	RW	*por_mxp_p1_qos_lat_tgt* on page 3-633
0xAB0	por_mxp_p1_qos_lat_scale	RW	*por_mxp_p1_qos_lat_scale* on page 3-633
0xAB8	por_mxp_p1_qos_lat_range	RW	*por_mxp_p1_qos_lat_range* on page 3-635
0x2000	por_mxp_pmu_event_sel	RW	*por_mxp_pmu_event_sel* on page 3-636
0x3000	por_mxp_errfr	RO	*por_mxp_errfr* on page 3-637
0x3008	por_mxp_errctlr	RW	*por_mxp_errctlr* on page 3-638
0x3010	por_mxp_errstatus	W1C	*por_mxp_errstatus* on page 3-640
0x3028	por_mxp_errmisc	RW	*por_mxp_errmisc* on page 3-641
0x3030	por_mxp_p0_byte_par_err_inj	WO	*por_mxp_p0_byte_par_err_inj* on page 3-643
0x3038	por_mxp_p1_byte_par_err_inj	WO	*por_mxp_p1_byte_par_err_inj* on page 3-644
0x3100	por_mxp_errfr_NS	RO	*por_mxp_errfr_NS* on page 3-645
0x3108	por_mxp_errctlr_NS	RW	*por_mxp_errctlr_NS* on page 3-646
0x3110	por_mxp_errstatus_NS	W1C	*por_mxp_errstatus_NS* on page 3-647
0x3128	por_mxp_errmisc_NS	RW	*por_mxp_errmisc_NS* on page 3-649
0x1000	por_mxp_p0_syscoreq_ctl	RW	*por_mxp_p0_syscoreq_ctl* on page 3-651
0x1008	por_mxp_p1_syscoreq_ctl	RW	*por_mxp_p1_syscoreq_ctl* on page 3-652
0x1010	por_mxp_p0_syscoack_status	RO	*por_mxp_p0_syscoack_status* on page 3-653

Table 3-7 MXP register summary (continued)

Offset	Name	Type	Description
0x1018	por_mxp_p1_syscoack_status	RO	*por_mxp_p1_syscoack_status* on page 3-654
0x2100	por_dtm_control	RW	*por_dtm_control* on page 3-656
0x2118	por_dtm_fifo_entry_ready	W1C	*por_dtm_fifo_entry_ready* on page 3-657
0x2120	por_dtm_fifo_entry0_0	RO	*por_dtm_fifo_entry0_0* on page 3-658
0x2128	por_dtm_fifo_entry0_1	RO	*por_dtm_fifo_entry0_1* on page 3-659
0x2130	por_dtm_fifo_entry0_2	RO	*por_dtm_fifo_entry0_2* on page 3-659
0x2138	por_dtm_fifo_entry1_0	RO	*por_dtm_fifo_entry1_0* on page 3-660
0x2140	por_dtm_fifo_entry1_1	RO	*por_dtm_fifo_entry1_1* on page 3-661
0x2148	por_dtm_fifo_entry1_2	RO	*por_dtm_fifo_entry1_2* on page 3-662
0x2150	por_dtm_fifo_entry2_0	RO	*por_dtm_fifo_entry2_0* on page 3-663
0x2158	por_dtm_fifo_entry2_1	RO	*por_dtm_fifo_entry2_1* on page 3-664
0x2160	por_dtm_fifo_entry2_2	RO	*por_dtm_fifo_entry2_2* on page 3-664
0x2168	por_dtm_fifo_entry3_0	RO	*por_dtm_fifo_entry3_0* on page 3-665
0x2170	por_dtm_fifo_entry3_1	RO	*por_dtm_fifo_entry3_1* on page 3-666
0x2178	por_dtm_fifo_entry3_2	RO	*por_dtm_fifo_entry3_2* on page 3-667
0x21A0	por_dtm_wp0_config	RW	*por_dtm_wp0_config* on page 3-668
0x21A8	por_dtm_wp0_val	RW	*por_dtm_wp0_val* on page 3-670
0x21B0	por_dtm_wp0_mask	RW	*por_dtm_wp0_mask* on page 3-671
0x21B8	por_dtm_wp1_config	RW	*por_dtm_wp1_config* on page 3-672
0x21C0	por_dtm_wp1_val	RW	*por_dtm_wp1_val* on page 3-673
0x21C8	por_dtm_wp1_mask	RW	*por_dtm_wp1_mask* on page 3-674
0x21D0	por_dtm_wp2_config	RW	*por_dtm_wp2_config* on page 3-675
0x21D8	por_dtm_wp2_val	RW	*por_dtm_wp2_val* on page 3-677
0x21E0	por_dtm_wp2_mask	RW	*por_dtm_wp2_mask* on page 3-678
0x21E8	por_dtm_wp3_config	RW	*por_dtm_wp3_config* on page 3-679
0x21F0	por_dtm_wp3_val	RW	*por_dtm_wp3_val* on page 3-681
0x21F8	por_dtm_wp3_mask	RW	*por_dtm_wp3_mask* on page 3-682
0x2200	por_dtm_pmsicr	RW	*por_dtm_pmsicr* on page 3-683
0x2208	por_dtm_pmsirr	RW	*por_dtm_pmsirr* on page 3-683
0x2210	por_dtm_pmu_config	RW	*por_dtm_pmu_config* on page 3-684
0x2220	por_dtm_pmevcnt	RW	*por_dtm_pmevcnt* on page 3-689
0x2240	por_dtm_pmevcntsr	RW	*por_dtm_pmevcntsr* on page 3-690

3.2.7 RN-D register summary

This section lists the RN-D registers used in CMN-600.

RND register summary

The following table shows the *RND* registers in offset order from the base memory address

Table 3-8 RND register summary

Offset	Name	Type	Description
0x0	por_rnd_node_info	RO	*por_rnd_node_info* on page 3-692
0x80	por_rnd_child_info	RO	*por_rnd_child_info* on page 3-693
0x980	por_rnd_secure_register_groups_override	RW	*por_rnd_secure_register_groups_override* on page 3-693
0x900	por_rnd_unit_info	RO	*por_rnd_unit_info* on page 3-694
0xA00	por_rnd_cfg_ctl	RW	*por_rnd_cfg_ctl* on page 3-696
0xA08	por_rnd_aux_ctl	RW	*por_rnd_aux_ctl* on page 3-698
0xA10	por_rnd_s0_port_control	RW	*por_rnd_s0_port_control* on page 3-699
0xA18	por_rnd_s1_port_control	RW	*por_rnd_s1_port_control* on page 3-700
0xA20	por_rnd_s2_port_control	RW	*por_rnd_s2_port_control* on page 3-701
0xA80	por_rnd_s0_qos_control	RW	*por_rnd_s0_qos_control* on page 3-702
0xA88	por_rnd_s0_qos_lat_tgt	RW	*por_rnd_s0_qos_lat_tgt* on page 3-704
0xA90	por_rnd_s0_qos_lat_scale	RW	*por_rnd_s0_qos_lat_scale* on page 3-705
0xA98	por_rnd_s0_qos_lat_range	RW	*por_rnd_s0_qos_lat_range* on page 3-707
0xAA0	por_rnd_s1_qos_control	RW	*por_rnd_s1_qos_control* on page 3-708
0xAA8	por_rnd_s1_qos_lat_tgt	RW	*por_rnd_s1_qos_lat_tgt* on page 3-710
0xAB0	por_rnd_s1_qos_lat_scale	RW	*por_rnd_s1_qos_lat_scale* on page 3-711
0xAB8	por_rnd_s1_qos_lat_range	RW	*por_rnd_s1_qos_lat_range* on page 3-712
0xAC0	por_rnd_s2_qos_control	RW	*por_rnd_s2_qos_control* on page 3-713
0xAC8	por_rnd_s2_qos_lat_tgt	RW	*por_rnd_s2_qos_lat_tgt* on page 3-715
0xAD0	por_rnd_s2_qos_lat_scale	RW	*por_rnd_s2_qos_lat_scale* on page 3-716
0xAD8	por_rnd_s2_qos_lat_range	RW	*por_rnd_s2_qos_lat_range* on page 3-718
0x2000	por_rnd_pmu_event_sel	RW	*por_rnd_pmu_event_sel* on page 3-719
0x1000	por_rnd_syscoreq_ctl	RW	*por_rnd_syscoreq_ctl* on page 3-721
0x1008	por_rnd_syscoack_status	RO	*por_rnd_syscoack_status* on page 3-722

3.2.8 RN-I register summary

This section lists the RN-I registers used in CMN-600.

RNI register summary

The following table shows the *RNI* registers in offset order from the base memory address

Table 3-9 RNI register summary

Offset	Name	Type	Description
0x0	por_rni_node_info	RO	*por_rni_node_info* on page 3-724
0x80	por_rni_child_info	RO	*por_rni_child_info* on page 3-725
0x980	por_rni_secure_register_groups_override	RW	*por_rni_secure_register_groups_override* on page 3-725
0x900	por_rni_unit_info	RO	*por_rni_unit_info* on page 3-726
0xA00	por_rni_cfg_ctl	RW	*por_rni_cfg_ctl* on page 3-728
0xA08	por_rni_aux_ctl	RW	*por_rni_aux_ctl* on page 3-730
0xA10	por_rni_s0_port_control	RW	*por_rni_s0_port_control* on page 3-731
0xA18	por_rni_s1_port_control	RW	*por_rni_s1_port_control* on page 3-732
0xA20	por_rni_s2_port_control	RW	*por_rni_s2_port_control* on page 3-733
0xA80	por_rni_s0_qos_control	RW	*por_rni_s0_qos_control* on page 3-734
0xA88	por_rni_s0_qos_lat_tgt	RW	*por_rni_s0_qos_lat_tgt* on page 3-736
0xA90	por_rni_s0_qos_lat_scale	RW	*por_rni_s0_qos_lat_scale* on page 3-737
0xA98	por_rni_s0_qos_lat_range	RW	*por_rni_s0_qos_lat_range* on page 3-738
0xAA0	por_rni_s1_qos_control	RW	*por_rni_s1_qos_control* on page 3-740
0xAA8	por_rni_s1_qos_lat_tgt	RW	*por_rni_s1_qos_lat_tgt* on page 3-742
0xAB0	por_rni_s1_qos_lat_scale	RW	*por_rni_s1_qos_lat_scale* on page 3-743
0xAB8	por_rni_s1_qos_lat_range	RW	*por_rni_s1_qos_lat_range* on page 3-744
0xAC0	por_rni_s2_qos_control	RW	*por_rni_s2_qos_control* on page 3-745
0xAC8	por_rni_s2_qos_lat_tgt	RW	*por_rni_s2_qos_lat_tgt* on page 3-747
0xAD0	por_rni_s2_qos_lat_scale	RW	*por_rni_s2_qos_lat_scale* on page 3-748
0xAD8	por_rni_s2_qos_lat_range	RW	*por_rni_s2_qos_lat_range* on page 3-750
0x2000	por_rni_pmu_event_sel	RW	*por_rni_pmu_event_sel* on page 3-751

3.2.9 RN SAM register summary

This section lists the RN SAM registers used in CMN-600.

RNSAM register summary

The following table shows the *RNSAM* registers in offset order from the base memory address

Table 3-10 RNSAM register summary

Offset	Name	Type	Description
0x0	por_rnsam_node_info	RO	*por_rnsam_node_info* on page 3-754
0x80	por_rnsam_child_info	RO	*por_rnsam_child_info* on page 3-755
0x980	por_rnsam_secure_register_groups_override	RW	*por_rnsam_secure_register_groups_override* on page 3-755
0x900	por_rnsam_unit_info	RO	*por_rnsam_unit_info* on page 3-756
0xC00	rnsam_status	RW	*rnsam_status* on page 3-757
0xC08	non_hash_mem_region_reg0	RW	*non_hash_mem_region_reg0* on page 3-758

Table 3-10 RNSAM register summary (continued)

Offset	Name	Type	Description
0xC10	non_hash_mem_region_reg1	RW	*non_hash_mem_region_reg1* on page 3-760
0xC18	non_hash_mem_region_reg2	RW	*non_hash_mem_region_reg2* on page 3-762
0xC20	non_hash_mem_region_reg3	RW	*non_hash_mem_region_reg3* on page 3-764
0xC28	non_hash_mem_region_reg4	RW	*non_hash_mem_region_reg4* on page 3-766
0xCA0	non_hash_mem_region_reg5	RW	*non_hash_mem_region_reg5* on page 3-768
0xCA8	non_hash_mem_region_reg6	RW	*non_hash_mem_region_reg6* on page 3-770
0xCB0	non_hash_mem_region_reg7	RW	*non_hash_mem_region_reg7* on page 3-772
0xCB8	non_hash_mem_region_reg8	RW	*non_hash_mem_region_reg8* on page 3-774
0xCC0	non_hash_mem_region_reg9	RW	*non_hash_mem_region_reg9* on page 3-776
0xC30	non_hash_tgt_nodeid0	RW	*non_hash_tgt_nodeid0* on page 3-778
0xC38	non_hash_tgt_nodeid1	RW	*non_hash_tgt_nodeid1* on page 3-780
0xC40	non_hash_tgt_nodeid2	RW	*non_hash_tgt_nodeid2* on page 3-781
0xCE0	non_hash_tgt_nodeid3	RW	*non_hash_tgt_nodeid3* on page 3-782
0xCE8	non_hash_tgt_nodeid4	RW	*non_hash_tgt_nodeid4* on page 3-783
0xC48	sys_cache_grp_region0	RW	*sys_cache_grp_region0* on page 3-784
0xC50	sys_cache_grp_region1	RW	*sys_cache_grp_region1* on page 3-787
0xC58	sys_cache_grp_hn_nodeid_reg0	RW	*sys_cache_grp_hn_nodeid_reg0* on page 3-789
0xC60	sys_cache_grp_hn_nodeid_reg1	RW	*sys_cache_grp_hn_nodeid_reg1* on page 3-790
0xC68	sys_cache_grp_hn_nodeid_reg2	RW	*sys_cache_grp_hn_nodeid_reg2* on page 3-791
0xC70	sys_cache_grp_hn_nodeid_reg3	RW	*sys_cache_grp_hn_nodeid_reg3* on page 3-793
0xC78	sys_cache_grp_hn_nodeid_reg4	RW	*sys_cache_grp_hn_nodeid_reg4* on page 3-794
0xC80	sys_cache_grp_hn_nodeid_reg5	RW	*sys_cache_grp_hn_nodeid_reg5* on page 3-795
0xC88	sys_cache_grp_hn_nodeid_reg6	RW	*sys_cache_grp_hn_nodeid_reg6* on page 3-796
0xC90	sys_cache_grp_hn_nodeid_reg7	RW	*sys_cache_grp_hn_nodeid_reg7* on page 3-798
0xC98	sys_cache_grp_nonhash_nodeid	RW	*sys_cache_grp_nonhash_nodeid* on page 3-799
0xD00	sys_cache_group_hn_count	RW	*sys_cache_group_hn_count* on page 3-800
0xD08	sys_cache_grp_sn_nodeid_reg0	RW	*sys_cache_grp_sn_nodeid_reg0* on page 3-801
0xD10	sys_cache_grp_sn_nodeid_reg1	RW	*sys_cache_grp_sn_nodeid_reg1* on page 3-803
0xD18	sys_cache_grp_sn_nodeid_reg2	RW	*sys_cache_grp_sn_nodeid_reg2* on page 3-804
0xD20	sys_cache_grp_sn_nodeid_reg3	RW	*sys_cache_grp_sn_nodeid_reg3* on page 3-805
0xD28	sys_cache_grp_sn_nodeid_reg4	RW	*sys_cache_grp_sn_nodeid_reg4* on page 3-806
0xD30	sys_cache_grp_sn_nodeid_reg5	RW	*sys_cache_grp_sn_nodeid_reg5* on page 3-808
0xD38	sys_cache_grp_sn_nodeid_reg6	RW	*sys_cache_grp_sn_nodeid_reg6* on page 3-809
0xD40	sys_cache_grp_sn_nodeid_reg7	RW	*sys_cache_grp_sn_nodeid_reg7* on page 3-810
0xD48	sys_cache_grp_sn_sam_cfg0	RW	*sys_cache_grp_sn_sam_cfg0* on page 3-811

Table 3-10 RNSAM register summary (continued)

Offset	Name	Type	Description
0xD50	sys_cache_grp_sn_sam_cfg1	RW	*sys_cache_grp_sn_sam_cfg1* on page 3-813
0xD58	gic_mem_region_reg	RW	*gic_mem_region_reg* on page 3-814
0xD60	sys_cache_grp_sn_attr	RW	*sys_cache_grp_sn_attr* on page 3-816
0xD68	sys_cache_grp_hn_cpa_en_reg	RW	*sys_cache_grp_hn_cpa_en_reg* on page 3-818
0xD70	sys_cache_grp_hn_cpa_grp_reg	RW	*sys_cache_grp_hn_cpa_grp_reg* on page 3-819
0xE00	cml_port_aggr_mode_ctrl_reg	RW	*cml_port_aggr_mode_ctrl_reg* on page 3-821
0xE30	cml_port_aggr_mode_ctrl_reg1	RW	*cml_port_aggr_mode_ctrl_reg1* on page 3-824
0xE08	cml_port_aggr_grp0_add_mask	RW	*cml_port_aggr_grp0_add_mask* on page 3-828
0xE10	cml_port_aggr_grp1_add_mask	RW	*cml_port_aggr_grp1_add_mask* on page 3-829
0xE40	cml_port_aggr_grp0_reg	RW	*cml_port_aggr_grp0_reg* on page 3-830
0xE48	cml_port_aggr_grp1_reg	RW	*cml_port_aggr_grp1_reg* on page 3-832
0xF00	sys_cache_grp_secondary_reg0	RW	*sys_cache_grp_secondary_reg0* on page 3-833
0xF08	sys_cache_grp_secondary_reg1	RW	*sys_cache_grp_secondary_reg1* on page 3-835
0xF10	sys_cache_grp_cal_mode_reg	RW	*sys_cache_grp_cal_mode_reg* on page 3-837
0xF18	rnsam_hash_addr_mask_reg	RW	*rnsam_hash_addr_mask_reg* on page 3-839
0xF20	rnsam_region_cmp_addr_mask_reg	RW	*rnsam_region_cmp_addr_mask_reg* on page 3-839
0xF58	sys_cache_grp_hn_nodeid_reg8	RW	*sys_cache_grp_hn_nodeid_reg8* on page 3-840
0xF60	sys_cache_grp_hn_nodeid_reg9	RW	*sys_cache_grp_hn_nodeid_reg9* on page 3-842
0xF68	sys_cache_grp_hn_nodeid_reg10	RW	*sys_cache_grp_hn_nodeid_reg10* on page 3-843
0xF70	sys_cache_grp_hn_nodeid_reg11	RW	*sys_cache_grp_hn_nodeid_reg11* on page 3-844
0xF78	sys_cache_grp_hn_nodeid_reg12	RW	*sys_cache_grp_hn_nodeid_reg12* on page 3-845
0xF80	sys_cache_grp_hn_nodeid_reg13	RW	*sys_cache_grp_hn_nodeid_reg13* on page 3-847
0xF88	sys_cache_grp_hn_nodeid_reg14	RW	*sys_cache_grp_hn_nodeid_reg14* on page 3-848
0xF90	sys_cache_grp_hn_nodeid_reg15	RW	*sys_cache_grp_hn_nodeid_reg15* on page 3-849
0x1008	sys_cache_grp_sn_nodeid_reg8	RW	*sys_cache_grp_sn_nodeid_reg8* on page 3-850
0x1010	sys_cache_grp_sn_nodeid_reg9	RW	*sys_cache_grp_sn_nodeid_reg9* on page 3-852
0x1018	sys_cache_grp_sn_nodeid_reg10	RW	*sys_cache_grp_sn_nodeid_reg10* on page 3-853
0x1020	sys_cache_grp_sn_nodeid_reg11	RW	*sys_cache_grp_sn_nodeid_reg11* on page 3-854
0x1028	sys_cache_grp_sn_nodeid_reg12	RW	*sys_cache_grp_sn_nodeid_reg12* on page 3-855
0x1030	sys_cache_grp_sn_nodeid_reg13	RW	*sys_cache_grp_sn_nodeid_reg13* on page 3-857
0x1038	sys_cache_grp_sn_nodeid_reg14	RW	*sys_cache_grp_sn_nodeid_reg14* on page 3-858
0x1040	sys_cache_grp_sn_nodeid_reg15	RW	*sys_cache_grp_sn_nodeid_reg15* on page 3-859

3.2.10 SBSX register summary

This section lists the SBSX registers used in CMN-600.

SBSX register summary

The following table shows the *SBSX* registers in offset order from the base memory address

Table 3-11 SBSX register summary

Offset	Name	Type	Description
0x0	por_sbsx_node_info	RO	*por_sbsx_node_info* on page 3-861
0x80	por_sbsx_child_info	RO	*por_sbsx_child_info* on page 3-862
0x900	por_sbsx_unit_info	RO	*por_sbsx_unit_info* on page 3-862
0xA08	por_sbsx_aux_ctl	RW	*por_sbsx_aux_ctl* on page 3-864
0x3000	por_sbsx_errfr	RO	*por_sbsx_errfr* on page 3-865
0x3008	por_sbsx_errctlr	RW	*por_sbsx_errctlr* on page 3-866
0x3010	por_sbsx_errstatus	W1C	*por_sbsx_errstatus* on page 3-867
0x3018	por_sbsx_erraddr	RW	*por_sbsx_erraddr* on page 3-869
0x3020	por_sbsx_errmisc	RW	*por_sbsx_errmisc* on page 3-870
0x3100	por_sbsx_errfr_NS	RO	*por_sbsx_errfr_NS* on page 3-871
0x3108	por_sbsx_errctlr_NS	RW	*por_sbsx_errctlr_NS* on page 3-873
0x3110	por_sbsx_errstatus_NS	W1C	*por_sbsx_errstatus_NS* on page 3-874
0x3118	por_sbsx_erraddr_NS	RW	*por_sbsx_erraddr_NS* on page 3-876
0x3120	por_sbsx_errmisc_NS	RW	*por_sbsx_errmisc_NS* on page 3-877
0x2000	por_sbsx_pmu_event_sel	RW	*por_sbsx_pmu_event_sel* on page 3-878

3.2.11 CXHA register summary

This section lists the CXHA registers used in CMN-600.

CXG_HA register summary

The following table shows the *CXG_HA* registers in offset order from the base memory address

Table 3-12 CXG_HA register summary

Offset	Name	Type	Description
0x0	por_cxg_ha_node_info	RO	*por_cxg_ha_node_info* on page 3-881
0x8	por_cxg_ha_id	RW	*por_cxg_ha_id* on page 3-882
0x80	por_cxg_ha_child_info	RO	*por_cxg_ha_child_info* on page 3-882
0xA08	por_cxg_ha_aux_ctl	RW	*por_cxg_ha_aux_ctl* on page 3-883
0x980	por_cxg_ha_secure_register_groups_override	RW	*por_cxg_ha_secure_register_groups_override* on page 3-885
0x900	por_cxg_ha_unit_info	RO	*por_cxg_ha_unit_info* on page 3-886
0xC00	por_cxg_ha_rnf_raid_to_ldid_reg0	RW	*por_cxg_ha_rnf_raid_to_ldid_reg0* on page 3-887
0xC08	por_cxg_ha_rnf_raid_to_ldid_reg1	RW	*por_cxg_ha_rnf_raid_to_ldid_reg1* on page 3-889
0xC10	por_cxg_ha_rnf_raid_to_ldid_reg2	RW	*por_cxg_ha_rnf_raid_to_ldid_reg2* on page 3-891
0xC18	por_cxg_ha_rnf_raid_to_ldid_reg3	RW	*por_cxg_ha_rnf_raid_to_ldid_reg3* on page 3-893

Table 3-12 CXG_HA register summary (continued)

Offset	Name	Type	Description
0xC20	por_cxg_ha_rnf_raid_to_ldid_reg4	RW	*por_cxg_ha_rnf_raid_to_ldid_reg4* on page 3-895
0xC28	por_cxg_ha_rnf_raid_to_ldid_reg5	RW	*por_cxg_ha_rnf_raid_to_ldid_reg5* on page 3-897
0xC30	por_cxg_ha_rnf_raid_to_ldid_reg6	RW	*por_cxg_ha_rnf_raid_to_ldid_reg6* on page 3-899
0xC38	por_cxg_ha_rnf_raid_to_ldid_reg7	RW	*por_cxg_ha_rnf_raid_to_ldid_reg7* on page 3-901
0xC40	por_cxg_ha_agentid_to_linkid_reg0	RW	*por_cxg_ha_agentid_to_linkid_reg0* on page 3-903
0xC48	por_cxg_ha_agentid_to_linkid_reg1	RW	*por_cxg_ha_agentid_to_linkid_reg1* on page 3-905
0xC50	por_cxg_ha_agentid_to_linkid_reg2	RW	*por_cxg_ha_agentid_to_linkid_reg2* on page 3-907
0xC58	por_cxg_ha_agentid_to_linkid_reg3	RW	*por_cxg_ha_agentid_to_linkid_reg3* on page 3-909
0xC60	por_cxg_ha_agentid_to_linkid_reg4	RW	*por_cxg_ha_agentid_to_linkid_reg4* on page 3-910
0xC68	por_cxg_ha_agentid_to_linkid_reg5	RW	*por_cxg_ha_agentid_to_linkid_reg5* on page 3-912
0xC70	por_cxg_ha_agentid_to_linkid_reg6	RW	*por_cxg_ha_agentid_to_linkid_reg6* on page 3-914
0xC78	por_cxg_ha_agentid_to_linkid_reg7	RW	*por_cxg_ha_agentid_to_linkid_reg7* on page 3-915
0xD00	por_cxg_ha_agentid_to_linkid_val	RW	*por_cxg_ha_agentid_to_linkid_val* on page 3-917
0xD08	por_cxg_ha_rnf_raid_to_ldid_val	RW	*por_cxg_ha_rnf_raid_to_ldid_val* on page 3-918
0x2000	por_cxg_ha_pmu_event_sel	RW	*por_cxg_ha_pmu_event_sel* on page 3-919
0x1000	por_cxg_ha_cxprtcl_link0_ctl	RW	*por_cxg_ha_cxprtcl_link0_ctl* on page 3-920
0x1008	por_cxg_ha_cxprtcl_link0_status	RO	*por_cxg_ha_cxprtcl_link0_status* on page 3-922
0x1010	por_cxg_ha_cxprtcl_link1_ctl	RW	*por_cxg_ha_cxprtcl_link1_ctl* on page 3-924
0x1018	por_cxg_ha_cxprtcl_link1_status	RO	*por_cxg_ha_cxprtcl_link1_status* on page 3-925
0x1020	por_cxg_ha_cxprtcl_link2_ctl	RW	*por_cxg_ha_cxprtcl_link2_ctl* on page 3-927
0x1028	por_cxg_ha_cxprtcl_link2_status	RO	*por_cxg_ha_cxprtcl_link2_status* on page 3-929
0x3000	por_cxg_ha_errfr	RO	*por_cxg_ha_errfr* on page 3-930
0x3008	por_cxg_ha_errctlr	RW	*por_cxg_ha_errctlr* on page 3-932
0x3010	por_cxg_ha_errstatus	W1C	*por_cxg_ha_errstatus* on page 3-933
0x3018	por_cxg_ha_erraddr	RW	*por_cxg_ha_erraddr* on page 3-935
0x3020	por_cxg_ha_errmisc	RW	*por_cxg_ha_errmisc* on page 3-936
0x3100	por_cxg_ha_errfr_NS	RO	*por_cxg_ha_errfr_NS* on page 3-937
0x3108	por_cxg_ha_errctlr_NS	RW	*por_cxg_ha_errctlr_NS* on page 3-939
0x3110	por_cxg_ha_errstatus_NS	W1C	*por_cxg_ha_errstatus_NS* on page 3-940
0x3118	por_cxg_ha_erraddr_NS	RW	*por_cxg_ha_erraddr_NS* on page 3-942
0x3120	por_cxg_ha_errmisc_NS	RW	*por_cxg_ha_errmisc_NS* on page 3-943

3.2.12 CXRA register summary

This section lists the CXRA registers used in CMN-600.

CXG_RA register summary

The following table shows the *CXG_RA* registers in offset order from the base memory address

Table 3-13 CXG_RA register summary

Offset	Name	Type	Description
0x0	por_cxg_ra_node_info	RO	*por_cxg_ra_node_info* on page 3-945
0x80	por_cxg_ra_child_info	RO	*por_cxg_ra_child_info* on page 3-946
0x980	por_cxg_ra_secure_register_groups_override	RW	*por_cxg_ra_secure_register_groups_override* on page 3-946
0x900	por_cxg_ra_unit_info	RO	*por_cxg_ra_unit_info* on page 3-947
0xA00	por_cxg_ra_cfg_ctl	RW	*por_cxg_ra_cfg_ctl* on page 3-949
0xA08	por_cxg_ra_aux_ctl	RW	*por_cxg_ra_aux_ctl* on page 3-950
0xDA8	por_cxg_ra_sam_addr_region_reg0	RW	*por_cxg_ra_sam_addr_region_reg0* on page 3-952
0xDB0	por_cxg_ra_sam_addr_region_reg1	RW	*por_cxg_ra_sam_addr_region_reg1* on page 3-953
0xDB8	por_cxg_ra_sam_addr_region_reg2	RW	*por_cxg_ra_sam_addr_region_reg2* on page 3-954
0xDC0	por_cxg_ra_sam_addr_region_reg3	RW	*por_cxg_ra_sam_addr_region_reg3* on page 3-956
0xDC8	por_cxg_ra_sam_addr_region_reg4	RW	*por_cxg_ra_sam_addr_region_reg4* on page 3-957
0xDD0	por_cxg_ra_sam_addr_region_reg5	RW	*por_cxg_ra_sam_addr_region_reg5* on page 3-958
0xDD8	por_cxg_ra_sam_addr_region_reg6	RW	*por_cxg_ra_sam_addr_region_reg6* on page 3-959
0xDE0	por_cxg_ra_sam_addr_region_reg7	RW	*por_cxg_ra_sam_addr_region_reg7* on page 3-961
0xE00	por_cxg_ra_sam_mem_region0_limit_reg	RW	*por_cxg_ra_sam_mem_region0_limit_reg* on page 3-962
0xE08	por_cxg_ra_sam_mem_region1_limit_reg	RW	*por_cxg_ra_sam_mem_region1_limit_reg* on page 3-963
0xE10	por_cxg_ra_sam_mem_region2_limit_reg	RW	*por_cxg_ra_sam_mem_region2_limit_reg* on page 3-964
0xE18	por_cxg_ra_sam_mem_region3_limit_reg	RW	*por_cxg_ra_sam_mem_region3_limit_reg* on page 3-965
0xE20	por_cxg_ra_sam_mem_region4_limit_reg	RW	*por_cxg_ra_sam_mem_region4_limit_reg* on page 3-966
0xE28	por_cxg_ra_sam_mem_region5_limit_reg	RW	*por_cxg_ra_sam_mem_region5_limit_reg* on page 3-967
0xE30	por_cxg_ra_sam_mem_region6_limit_reg	RW	*por_cxg_ra_sam_mem_region6_limit_reg* on page 3-968
0xE38	por_cxg_ra_sam_mem_region7_limit_reg	RW	*por_cxg_ra_sam_mem_region7_limit_reg* on page 3-969
0xE60	por_cxg_ra_agentid_to_linkid_reg0	RW	*por_cxg_ra_agentid_to_linkid_reg0* on page 3-970
0xE68	por_cxg_ra_agentid_to_linkid_reg1	RW	*por_cxg_ra_agentid_to_linkid_reg1* on page 3-972
0xE70	por_cxg_ra_agentid_to_linkid_reg2	RW	*por_cxg_ra_agentid_to_linkid_reg2* on page 3-973
0xE78	por_cxg_ra_agentid_to_linkid_reg3	RW	*por_cxg_ra_agentid_to_linkid_reg3* on page 3-975
0xE80	por_cxg_ra_agentid_to_linkid_reg4	RW	*por_cxg_ra_agentid_to_linkid_reg4* on page 3-977
0xE88	por_cxg_ra_agentid_to_linkid_reg5	RW	*por_cxg_ra_agentid_to_linkid_reg5* on page 3-978
0xE90	por_cxg_ra_agentid_to_linkid_reg6	RW	*por_cxg_ra_agentid_to_linkid_reg6* on page 3-980
0xE98	por_cxg_ra_agentid_to_linkid_reg7	RW	*por_cxg_ra_agentid_to_linkid_reg7* on page 3-982
0xEA0	por_cxg_ra_rnf_ldid_to_raid_reg0	RW	*por_cxg_ra_rnf_ldid_to_raid_reg0* on page 3-983
0xEA8	por_cxg_ra_rnf_ldid_to_raid_reg1	RW	*por_cxg_ra_rnf_ldid_to_raid_reg1* on page 3-985
0xEB0	por_cxg_ra_rnf_ldid_to_raid_reg2	RW	*por_cxg_ra_rnf_ldid_to_raid_reg2* on page 3-987

Table 3-13 CXG_RA register summary (continued)

Offset	Name	Type	Description
0xEB8	por_cxg_ra_rnf_ldid_to_raid_reg3	RW	*por_cxg_ra_rnf_ldid_to_raid_reg3* on page 3-988
0xEC0	por_cxg_ra_rnf_ldid_to_raid_reg4	RW	*por_cxg_ra_rnf_ldid_to_raid_reg4* on page 3-990
0xEC8	por_cxg_ra_rnf_ldid_to_raid_reg5	RW	*por_cxg_ra_rnf_ldid_to_raid_reg5* on page 3-992
0xED0	por_cxg_ra_rnf_ldid_to_raid_reg6	RW	*por_cxg_ra_rnf_ldid_to_raid_reg6* on page 3-993
0xED8	por_cxg_ra_rnf_ldid_to_raid_reg7	RW	*por_cxg_ra_rnf_ldid_to_raid_reg7* on page 3-995
0xEE0	por_cxg_ra_rni_ldid_to_raid_reg0	RW	*por_cxg_ra_rni_ldid_to_raid_reg0* on page 3-997
0xEE8	por_cxg_ra_rni_ldid_to_raid_reg1	RW	*por_cxg_ra_rni_ldid_to_raid_reg1* on page 3-998
0xEF0	por_cxg_ra_rni_ldid_to_raid_reg2	RW	*por_cxg_ra_rni_ldid_to_raid_reg2* on page 3-1000
0xEF8	por_cxg_ra_rni_ldid_to_raid_reg3	RW	*por_cxg_ra_rni_ldid_to_raid_reg3* on page 3-1002
0xF00	por_cxg_ra_rnd_ldid_to_raid_reg0	RW	*por_cxg_ra_rnd_ldid_to_raid_reg0* on page 3-1003
0xF08	por_cxg_ra_rnd_ldid_to_raid_reg1	RW	*por_cxg_ra_rnd_ldid_to_raid_reg1* on page 3-1005
0xF10	por_cxg_ra_rnd_ldid_to_raid_reg2	RW	*por_cxg_ra_rnd_ldid_to_raid_reg2* on page 3-1007
0xF18	por_cxg_ra_rnd_ldid_to_raid_reg3	RW	*por_cxg_ra_rnd_ldid_to_raid_reg3* on page 3-1008
0xF20	por_cxg_ra_agentid_to_linkid_val	RW	*por_cxg_ra_agentid_to_linkid_val* on page 3-1010
0xF28	por_cxg_ra_rnf_ldid_to_raid_val	RW	*por_cxg_ra_rnf_ldid_to_raid_val* on page 3-1011
0xF30	por_cxg_ra_rni_ldid_to_raid_val	RW	*por_cxg_ra_rni_ldid_to_raid_val* on page 3-1012
0xF38	por_cxg_ra_rnd_ldid_to_raid_val	RW	*por_cxg_ra_rnd_ldid_to_raid_val* on page 3-1013
0x2000	por_cxg_ra_pmu_event_sel	RW	*por_cxg_ra_pmu_event_sel* on page 3-1014
0x1000	por_cxg_ra_cxprtcl_link0_ctl	RW	*por_cxg_ra_cxprtcl_link0_ctl* on page 3-1015
0x1008	por_cxg_ra_cxprtcl_link0_status	RO	*por_cxg_ra_cxprtcl_link0_status* on page 3-1017
0x1010	por_cxg_ra_cxprtcl_link1_ctl	RW	*por_cxg_ra_cxprtcl_link1_ctl* on page 3-1018
0x1018	por_cxg_ra_cxprtcl_link1_status	RO	*por_cxg_ra_cxprtcl_link1_status* on page 3-1020
0x1020	por_cxg_ra_cxprtcl_link2_ctl	RW	*por_cxg_ra_cxprtcl_link2_ctl* on page 3-1022
0x1028	por_cxg_ra_cxprtcl_link2_status	RO	*por_cxg_ra_cxprtcl_link2_status* on page 3-1023

3.2.13 CXLA register summary

This section lists the CXLA registers used in CMN-600.

CXLA register summary

The following table shows the *CXLA* registers in offset order from the base memory address

Table 3-14 CXLA register summary

Offset	Name	Type	Description
0x0	por_cxla_node_info	RO	*por_cxla_node_info* on page 3-1025
0x80	por_cxla_child_info	RO	*por_cxla_child_info* on page 3-1026
0x980	por_cxla_secure_register_groups_override	RW	*por_cxla_secure_register_groups_override* on page 3-1026

Table 3-14 CXLA register summary (continued)

Offset	Name	Type	Description
0x900	por_cxla_unit_info	RO	*por_cxla_unit_info* on page 3-1027
0xA08	por_cxla_aux_ctl	RW	*por_cxla_aux_ctl* on page 3-1029
0xC00	por_cxla_ccix_prop_capabilities	RO	*por_cxla_ccix_prop_capabilities* on page 3-1033
0xC08	por_cxla_ccix_prop_configured	RW	*por_cxla_ccix_prop_configured* on page 3-1034
0xC10	por_cxla_tx_cxs_attr_capabilities	RO	*por_cxla_tx_cxs_attr_capabilities* on page 3-1036
0xC18	por_cxla_rx_cxs_attr_capabilities	RO	*por_cxla_rx_cxs_attr_capabilities* on page 3-1038
0xC30	por_cxla_agentid_to_linkid_reg0	RW	*por_cxla_agentid_to_linkid_reg0* on page 3-1040
0xC38	por_cxla_agentid_to_linkid_reg1	RW	*por_cxla_agentid_to_linkid_reg1* on page 3-1041
0xC40	por_cxla_agentid_to_linkid_reg2	RW	*por_cxla_agentid_to_linkid_reg2* on page 3-1043
0xC48	por_cxla_agentid_to_linkid_reg3	RW	*por_cxla_agentid_to_linkid_reg3* on page 3-1045
0xC50	por_cxla_agentid_to_linkid_reg4	RW	*por_cxla_agentid_to_linkid_reg4* on page 3-1046
0xC58	por_cxla_agentid_to_linkid_reg5	RW	*por_cxla_agentid_to_linkid_reg5* on page 3-1048
0xC60	por_cxla_agentid_to_linkid_reg6	RW	*por_cxla_agentid_to_linkid_reg6* on page 3-1050
0xC68	por_cxla_agentid_to_linkid_reg7	RW	*por_cxla_agentid_to_linkid_reg7* on page 3-1051
0xC70	por_cxla_agentid_to_linkid_val	RW	*por_cxla_agentid_to_linkid_val* on page 3-1053
0xC78	por_cxla_linkid_to_pcie_bus_num	RW	*por_cxla_linkid_to_pcie_bus_num* on page 3-1054
0xD00	por_cxla_permsg_pyld_0_63	RW	*por_cxla_permsg_pyld_0_63* on page 3-1055
0xD08	por_cxla_permsg_pyld_64_127	RW	*por_cxla_permsg_pyld_64_127* on page 3-1056
0xD10	por_cxla_permsg_pyld_128_191	RW	*por_cxla_permsg_pyld_128_191* on page 3-1057
0xD18	por_cxla_permsg_pyld_192_255	RW	*por_cxla_permsg_pyld_192_255* on page 3-1058
0xD20	por_cxla_permsg_ctl	RW	*por_cxla_permsg_ctl* on page 3-1058
0xD28	por_cxla_err_agent_id	RW	*por_cxla_err_agent_id* on page 3-1060
0x2000	por_cxla_pmu_event_sel	RW	*por_cxla_pmu_event_sel* on page 3-1060
0x2210	por_cxla_pmu_config	RW	*por_cxla_pmu_config* on page 3-1062
0x2220	por_cxla_pmevcnt	RW	*por_cxla_pmevcnt* on page 3-1064
0x2240	por_cxla_pmevcntsr	RW	*por_cxla_pmevcntsr* on page 3-1065

3.3 Register descriptions

This section contains register descriptions.

This section contains the following subsections:

3.3.1 Configuration master register descriptions

This section lists the configuration registers.

por_cfgm_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

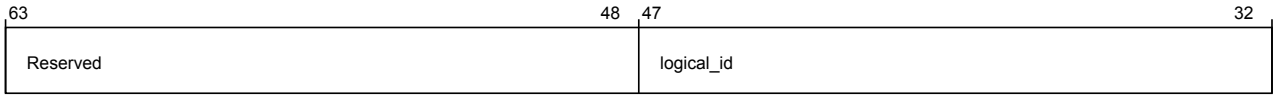


Figure 3-1 por_cfgm_por_cfgm_node_info (high)

The following table shows the por_cfgm_node_info higher register bit assignments.

Table 3-15 por_cfgm_por_cfgm_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

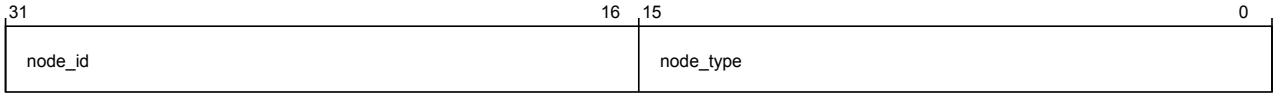


Figure 3-2 por_cfgm_por_cfgm_node_info (low)

The following table shows the por_cfgm_node_info lower register bit assignments.

Table 3-16 por_cfgm_por_cfgm_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0002

por_cfgm_periph_id_0_periph_id_1

Functions as the peripheral ID 0 and peripheral ID 1 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

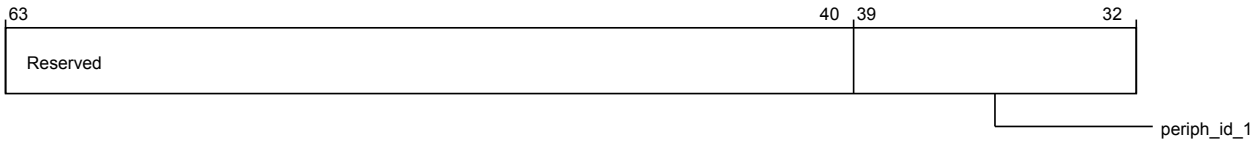


Figure 3-3 por_cfgm_por_cfgm_periph_id_0_periph_id_1 (high)

The following table shows the por_cfgm_periph_id_0_periph_id_1 higher register bit assignments.

Table 3-17 por_cfgm_por_cfgm_periph_id_0_periph_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_1	Peripheral ID 1	RO	8'b10110100

The following image shows the lower register bit assignments.

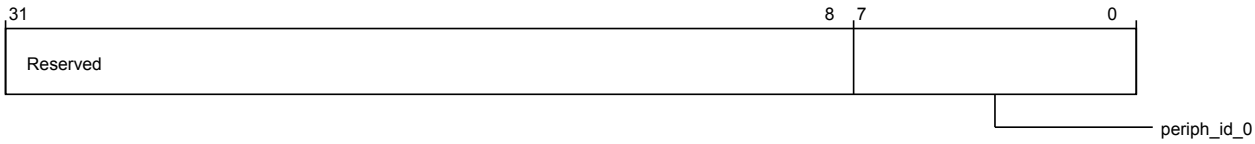


Figure 3-4 por_cfgm_por_cfgm_periph_id_0_periph_id_1 (low)

The following table shows the por_cfgm_periph_id_0_periph_id_1 lower register bit assignments.

Table 3-18 por_cfgm_por_cfgm_periph_id_0_periph_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_0	Peripheral ID 0	RO	Configuration dependent

por_cfgm_periph_id_2_periph_id_3

Functions as the peripheral ID 2 and peripheral ID 3 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h10
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

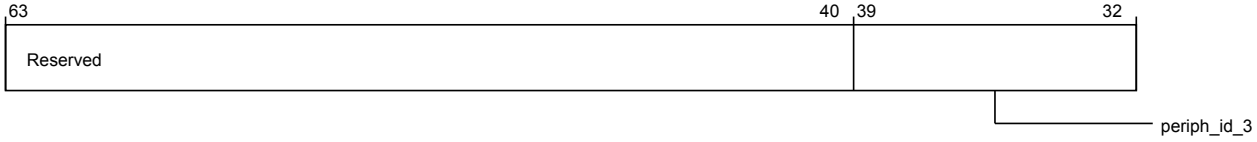


Figure 3-5 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)

The following table shows the por_cfgm_periph_id_2_periph_id_3 higher register bit assignments.

Table 3-19 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

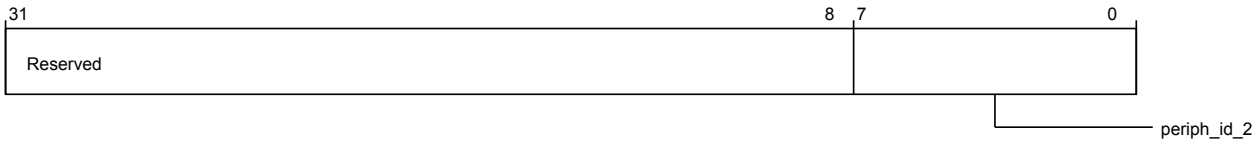


Figure 3-6 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)

The following table shows the por_cfgm_periph_id_2_periph_id_3 lower register bit assignments.

Table 3-20 por_cfgm_por_cfgm_periph_id_2_periph_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_2	Peripheral ID 2 [7:4] indicates revision: 0x0 r1p0 0x1 r1p1 0x2 r1p2 0x3 r1p3 0x4 r2p0 0x5 r3p0 [3] JEDEC JEP106 identity code, 1'b1 [2:0] JEP106 identidy code [6:4], 0'b011	RO	Configuration dependent

por_cfgm_periph_id_4_periph_id_5

Functions as the peripheral ID 4 and peripheral ID 5 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h18
Register reset 64'b011000100
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

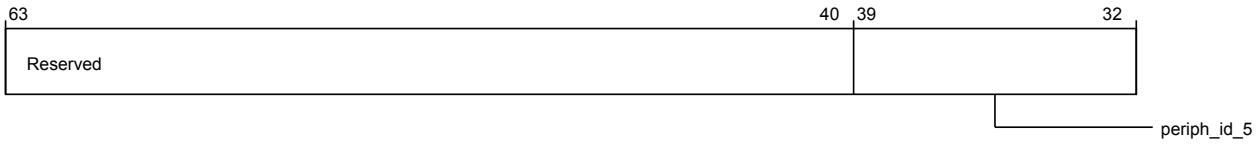


Figure 3-7 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)

The following table shows the por_cfgm_periph_id_4_periph_id_5 higher register bit assignments.

Table 3-21 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

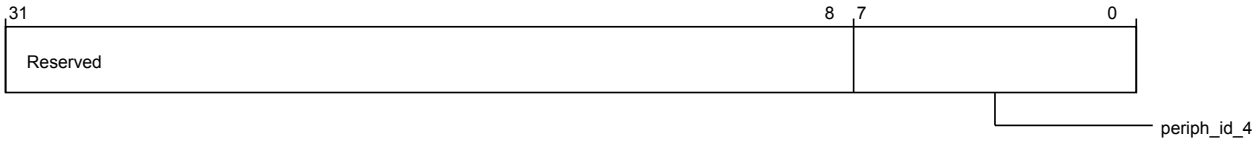


Figure 3-8 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (low)

The following table shows the por_cfgm_periph_id_4_periph_id_5 lower register bit assignments.

Table 3-22 por_cfgm_por_cfgm_periph_id_4_periph_id_5 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_4	Peripheral ID 4	RO	8'b11000100

por_cfgm_periph_id_6_periph_id_7

Functions as the peripheral ID 6 and peripheral ID 7 register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h20
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

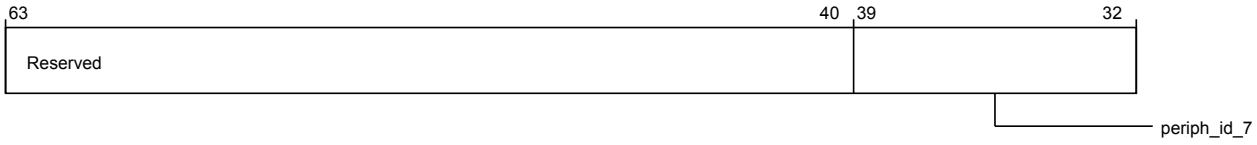


Figure 3-9 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (high)

The following table shows the por_cfgm_periph_id_6_periph_id_7 higher register bit assignments.

Table 3-23 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	periph_id_7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

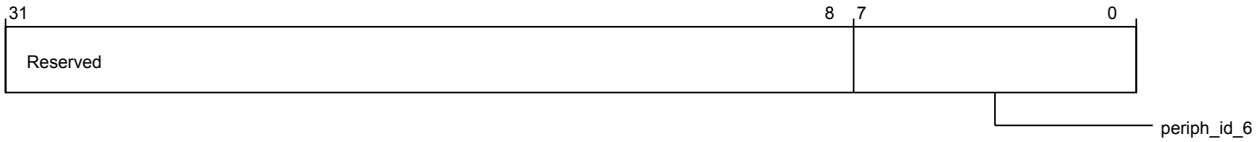


Figure 3-10 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)

The following table shows the por_cfgm_periph_id_6_periph_id_7 lower register bit assignments.

Table 3-24 por_cfgm_por_cfgm_periph_id_6_periph_id_7 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	periph_id_6	Peripheral ID 6	RO	8'b0

por_cfgm_component_id_0_component_id_1

Functions as the component ID 0 and component ID 1 register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h28

Register reset 64'b1111000000001101

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

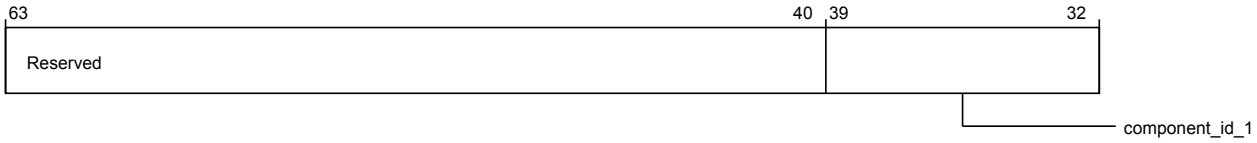


Figure 3-11 por_cfgm_por_cfgm_component_id_0_component_id_1 (high)

The following table shows the por_cfgm_component_id_0_component_id_1 higher register bit assignments.

Table 3-25 por_cfgm_por_cfgm_component_id_0_component_id_1 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_1	Component ID 1	RO	8'b11110000

The following image shows the lower register bit assignments.

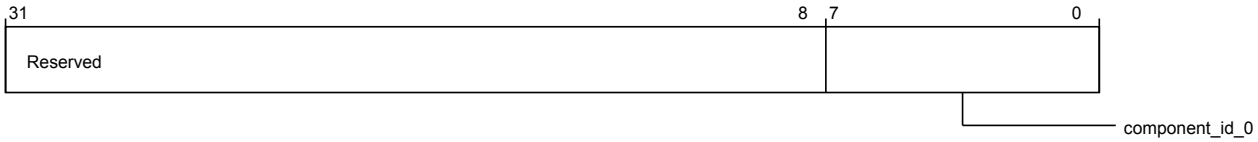


Figure 3-12 por_cfgm_por_cfgm_component_id_0_component_id_1 (low)

The following table shows the por_cfgm_component_id_0_component_id_1 lower register bit assignments.

Table 3-26 por_cfgm_por_cfgm_component_id_0_component_id_1 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_0	Component ID 0	RO	8'b00001101

por_cfgm_component_id_2_component_id_3

Functions as the component ID 2 and component ID 3 register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h30

Register reset 64'b1011000100000101

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

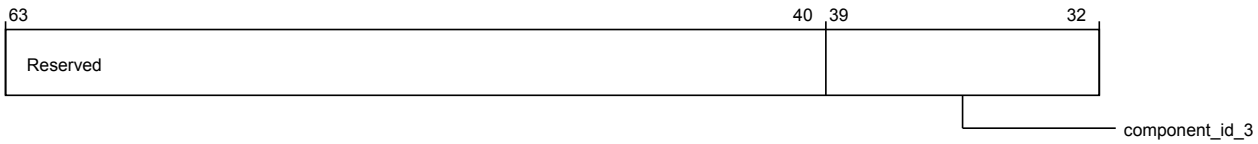


Figure 3-13 por_cfgm_por_cfgm_component_id_2_component_id_3 (high)

The following table shows the por_cfgm_component_id_2_component_id_3 higher register bit assignments.

Table 3-27 por_cfgm_por_cfgm_component_id_2_component_id_3 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	component_id_3	Component ID 3	RO	8'b10110001

The following image shows the lower register bit assignments.

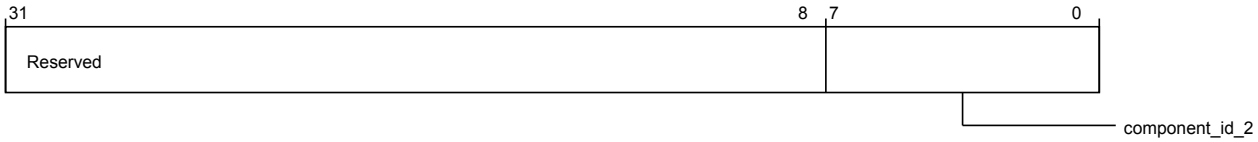


Figure 3-14 por_cfgm_por_cfgm_component_id_2_component_id_3 (low)

The following table shows the por_cfgm_component_id_2_component_id_3 lower register bit assignments.

Table 3-28 por_cfgm_por_cfgm_component_id_2_component_id_3 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	component_id_2	Component ID 2	RO	8'b00000101

por_cfgm_child_info

Provides component child identification information.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h80

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

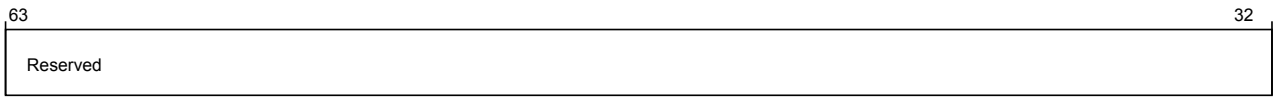


Figure 3-15 por_cfgm_por_cfgm_child_info (high)

The following table shows the por_cfgm_child_info higher register bit assignments.

Table 3-29 por_cfgm_por_cfgm_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

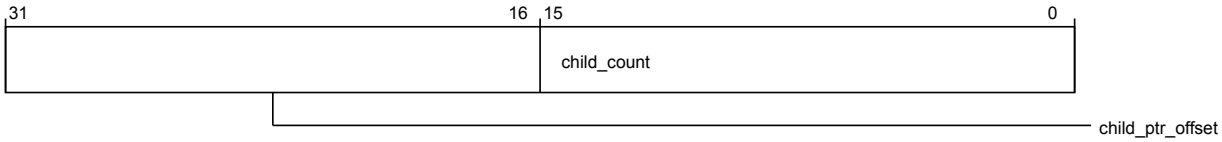


Figure 3-16 por_cfgm_por_cfgm_child_info (low)

The following table shows the por_cfgm_child_info lower register bit assignments.

Table 3-30 por_cfgm_por_cfgm_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

por_cfgm_secure_access

Functions as the secure access control register. This register must be set up at boot time. Before initiating a write to this register, software must ensure that no other configuration accesses are in flight. Once this write is initiated, no other configuration accesses are initiated until complete.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

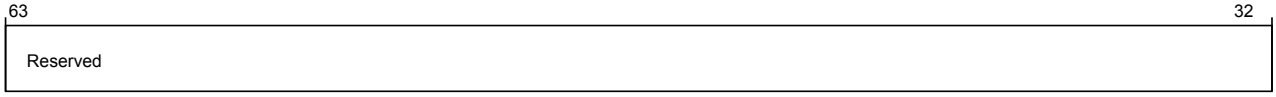


Figure 3-17 por_cfgm_por_cfgm_secure_access (high)

The following table shows the por_cfgm_secure_access higher register bit assignments.

Table 3-31 por_cfgm_por_cfgm_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

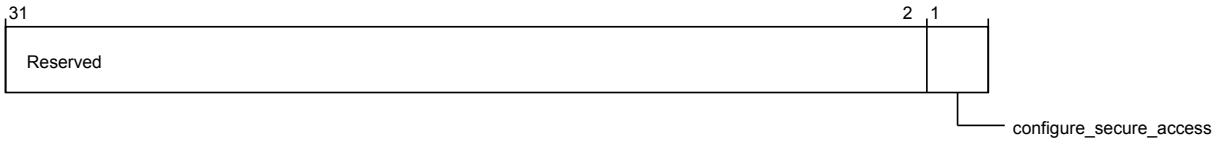


Figure 3-18 por_cfgm_por_cfgm_secure_access (low)

The following table shows the por_cfgm_secure_access lower register bit assignments.

Table 3-32 por_cfgm_por_cfgm_secure_access (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	configure_secure_access	Secure access mode 2'b00: Default operation 2'b01: Allows non-secure access to secure registers 2'b10: Allows secure access only to any configuration register regardless of its security status 2'b11: Undefined behavior	RW	2'b0

por_cfgm_errgsr0

Provides the XP <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

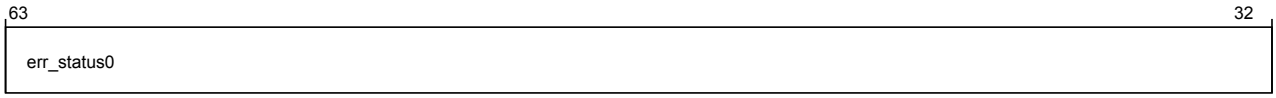


Figure 3-19 por_cfgm_por_cfgm_errgsr0 (high)

The following table shows the por_cfgm_errgsr0 higher register bit assignments.

Table 3-33 por_cfgm_por_cfgm_errgsr0 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status0	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

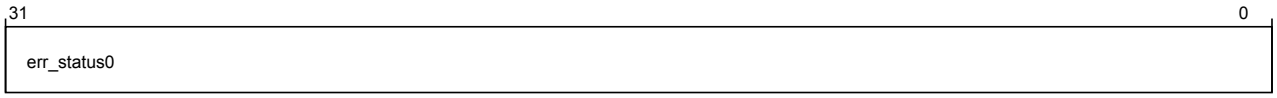


Figure 3-20 por_cfgm_por_cfgm_errgsr0 (low)

The following table shows the por_cfgm_errgsr0 lower register bit assignments.

Table 3-34 por_cfgm_por_cfgm_errgsr0 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr1

Provides the HN-I <n> secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

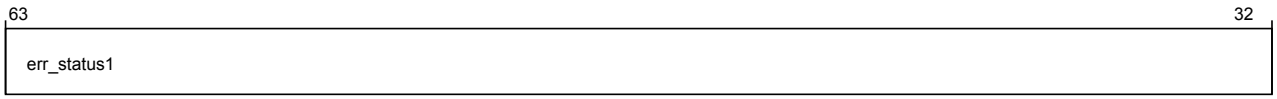


Figure 3-21 por_cfgm_por_cfgm_errgsr1 (high)

The following table shows the por_cfgm_errgsr1 higher register bit assignments.

Table 3-35 por_cfgm_por_cfgm_errgsr1 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

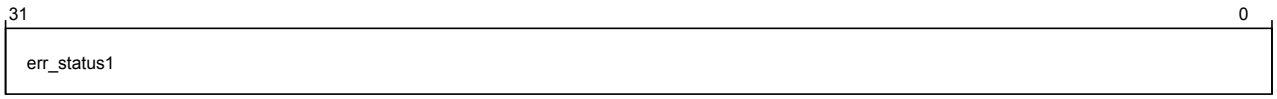


Figure 3-22 por_cfgm_por_cfgm_errgsr1 (low)

The following table shows the por_cfgm_errgsr1 lower register bit assignments.

Table 3-36 por_cfgm_por_cfgm_errgsr1 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr2

Provides the HN-F <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3010
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

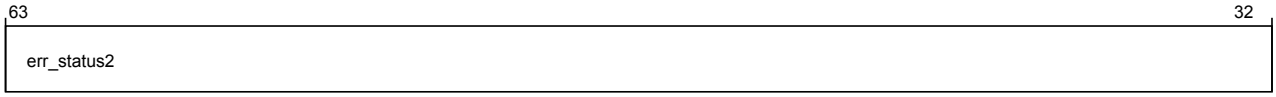


Figure 3-23 por_cfgm_por_cfgm_errgsr2 (high)

The following table shows the por_cfgm_errgsr2 higher register bit assignments.

Table 3-37 por_cfgm_por_cfgm_errgsr2 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

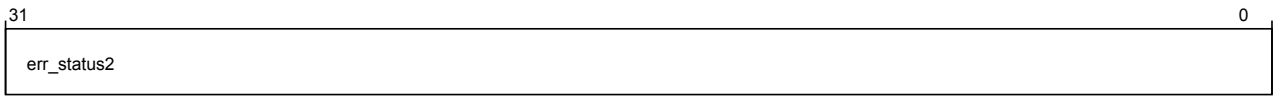


Figure 3-24 por_cfgm_por_cfgm_errgsr2 (low)

The following table shows the por_cfgm_errgsr2 lower register bit assignments.

Table 3-38 por_cfgm_por_cfgm_errgsr2 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr3

Provides the SBSX <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

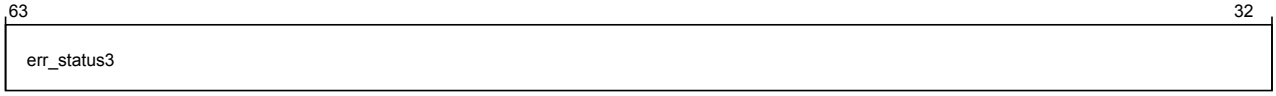


Figure 3-25 por_cfgm_por_cfgm_errgsr3 (high)

The following table shows the por_cfgm_errgsr3 higher register bit assignments.

Table 3-39 por_cfgm_por_cfgm_errgsr3 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

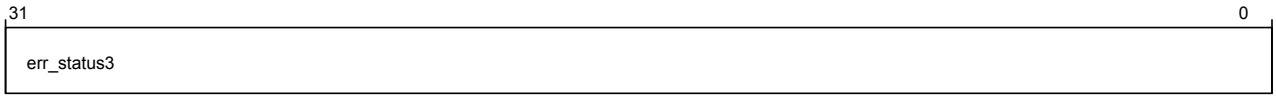


Figure 3-26 por_cfgm_por_cfgm_errgsr3 (low)

The following table shows the por_cfgm_errgsr3 lower register bit assignments.

Table 3-40 por_cfgm_por_cfgm_errgsr3 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr4

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

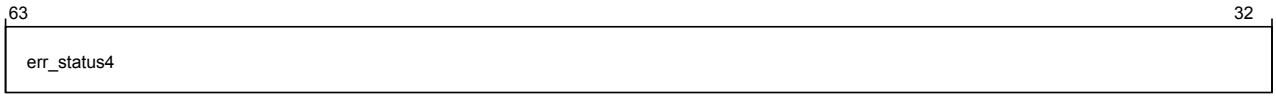


Figure 3-27 por_cfgm_por_cfgm_errgsr4 (high)

The following table shows the por_cfgm_errgsr4 higher register bit assignments.

Table 3-41 por_cfgm_por_cfgm_errgsr4 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

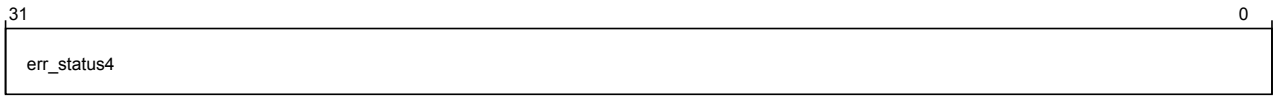


Figure 3-28 por_cfgm_por_cfgm_errgsr4 (low)

The following table shows the por_cfgm_errgsr4 lower register bit assignments.

Table 3-42 por_cfgm_por_cfgm_errgsr4 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr5

Provides the XP <n> secure fault status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3080

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

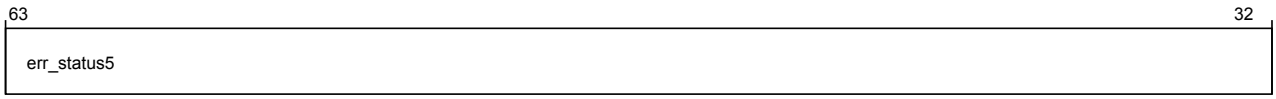


Figure 3-29 por_cfgm_por_cfgm_errgsr5 (high)

The following table shows the por_cfgm_errgsr5 higher register bit assignments.

Table 3-43 por_cfgm_por_cfgm_errgsr5 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

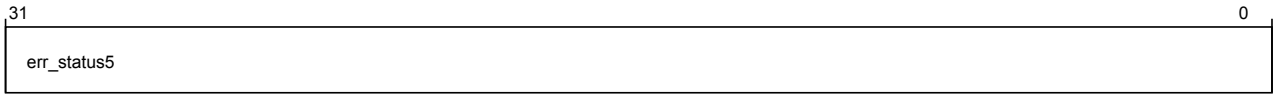


Figure 3-30 por_cfgm_por_cfgm_errgsr5 (low)

The following table shows the por_cfgm_errgsr5 lower register bit assignments.

Table 3-44 por_cfgm_por_cfgm_errgsr5 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr6

Provides the HN-I <n> secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3088
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

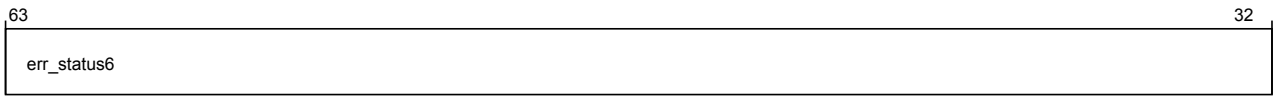


Figure 3-31 por_cfgm_por_cfgm_errgsr6 (high)

The following table shows the por_cfgm_errgsr6 higher register bit assignments.

Table 3-45 por_cfgm_por_cfgm_errgsr6 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

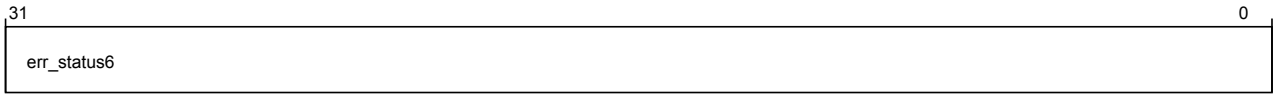


Figure 3-32 por_cfgm_por_cfgm_errgsr6 (low)

The following table shows the por_cfgm_errgsr6 lower register bit assignments.

Table 3-46 por_cfgm_por_cfgm_errgsr6 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr7

Provides the HN-F <n> secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3090
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

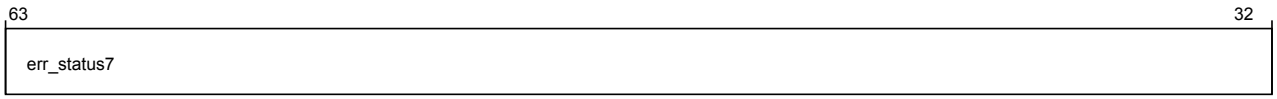


Figure 3-33 por_cfgm_por_cfgm_errgsr7 (high)

The following table shows the por_cfgm_errgsr7 higher register bit assignments.

Table 3-47 por_cfgm_por_cfgm_errgsr7 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status7	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

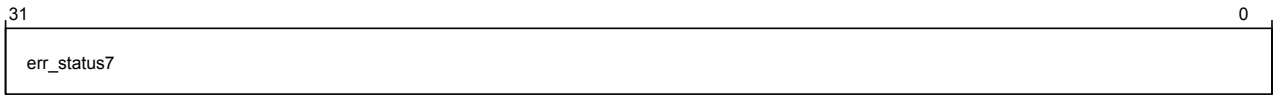


Figure 3-34 por_cfgm_por_cfgm_errgsr7 (low)

The following table shows the por_cfgm_errgsr7 lower register bit assignments.

Table 3-48 por_cfgm_por_cfgm_errgsr7 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status7	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr8

Provides the SBSX <n> secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3098
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

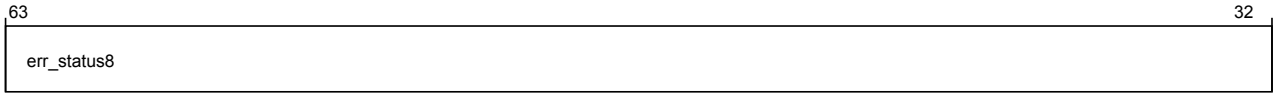


Figure 3-35 por_cfgm_por_cfgm_errgsr8 (high)

The following table shows the por_cfgm_errgsr8 higher register bit assignments.

Table 3-49 por_cfgm_por_cfgm_errgsr8 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status8	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

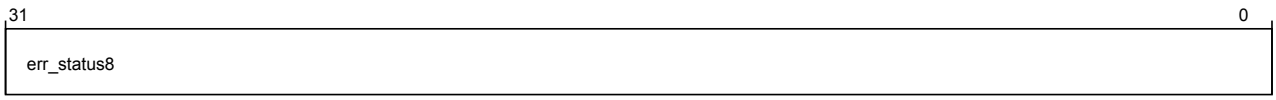


Figure 3-36 por_cfgm_por_cfgm_errgsr8 (low)

The following table shows the por_cfgm_errgsr8 lower register bit assignments.

Table 3-50 por_cfgm_por_cfgm_errgsr8 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr9

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h30A0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

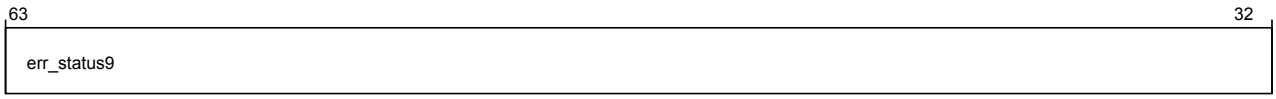


Figure 3-37 por_cfgm_por_cfgm_errgsr9 (high)

The following table shows the por_cfgm_errgsr9 higher register bit assignments.

Table 3-51 por_cfgm_por_cfgm_errgsr9 (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

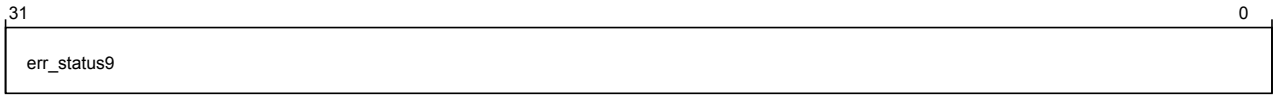


Figure 3-38 por_cfgm_por_cfgm_errgsr9 (low)

The following table shows the por_cfgm_errgsr9 lower register bit assignments.

Table 3-52 por_cfgm_por_cfgm_errgsr9 (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr0_NS

Provides the XP <n> non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

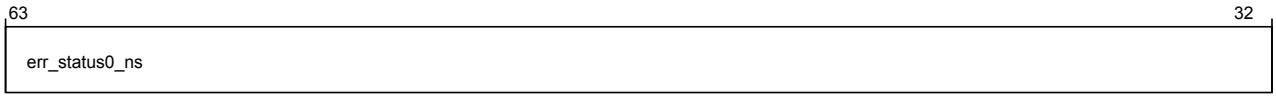


Figure 3-39 por_cfgm_por_cfgm_errgsr0_ns (high)

The following table shows the por_cfgm_errgsr0_NS higher register bit assignments.

Table 3-53 por_cfgm_por_cfgm_errgsr0_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

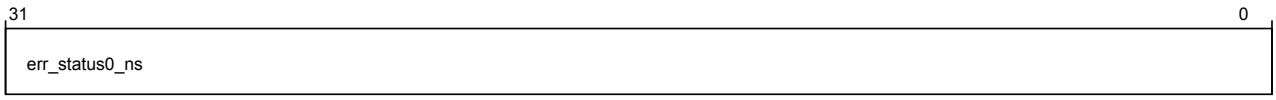


Figure 3-40 por_cfgm_por_cfgm_errgsr0_ns (low)

The following table shows the por_cfgm_errgsr0_NS lower register bit assignments.

Table 3-54 por_cfgm_por_cfgm_errgsr0_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status0_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr1_NS

Provides the HN-I <n> non-secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

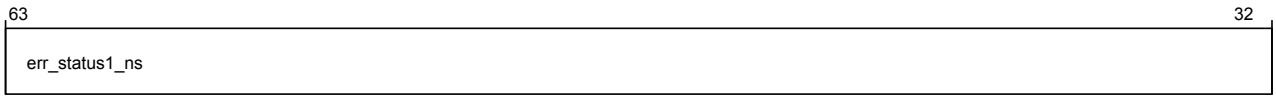


Figure 3-41 por_cfgm_por_cfgm_errgsr1_ns (high)

The following table shows the por_cfgm_errgsr1_NS higher register bit assignments.

Table 3-55 por_cfgm_por_cfgm_errgsr1_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

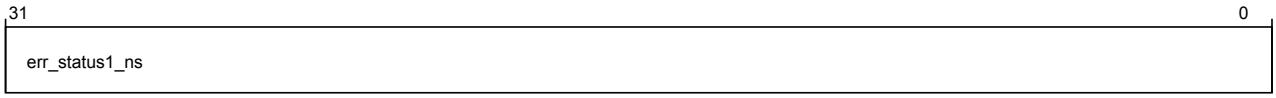


Figure 3-42 por_cfgm_por_cfgm_errgsr1_ns (low)

The following table shows the por_cfgm_errgsr1_NS lower register bit assignments.

Table 3-56 por_cfgm_por_cfgm_errgsr1_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status1_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr2_NS

Provides the HN-F <n> non-secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

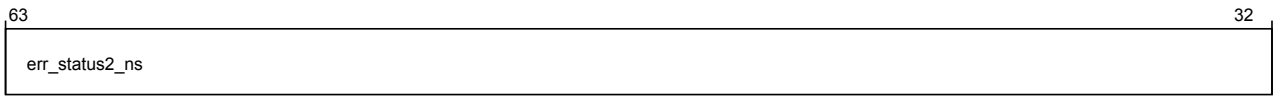


Figure 3-43 por_cfgm_por_cfgm_errgsr2_ns (high)

The following table shows the por_cfgm_errgsr2_NS higher register bit assignments.

Table 3-57 por_cfgm_por_cfgm_errgsr2_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

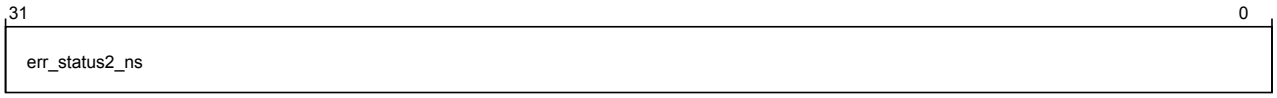


Figure 3-44 por_cfgm_por_cfgm_errgsr2_ns (low)

The following table shows the por_cfgm_errgsr2_NS lower register bit assignments.

Table 3-58 por_cfgm_por_cfgm_errgsr2_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status2_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr3_NS

Provides the SBSX <n> non-secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3118

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

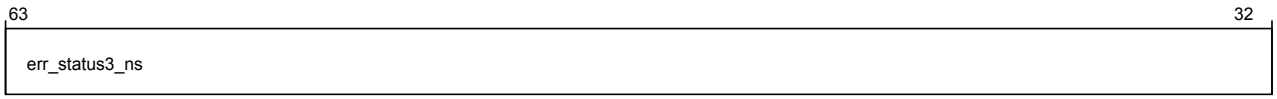


Figure 3-45 por_cfgm_por_cfgm_errgsr3_ns (high)

The following table shows the por_cfgm_errgsr3_NS higher register bit assignments.

Table 3-59 por_cfgm_por_cfgm_errgsr3_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

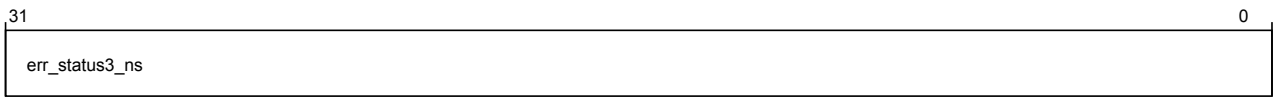


Figure 3-46 por_cfgm_por_cfgm_errgsr3_ns (low)

The following table shows the por_cfgm_errgsr3_NS lower register bit assignments.

Table 3-60 por_cfgm_por_cfgm_errgsr3_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status3_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr4_NS

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3120
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

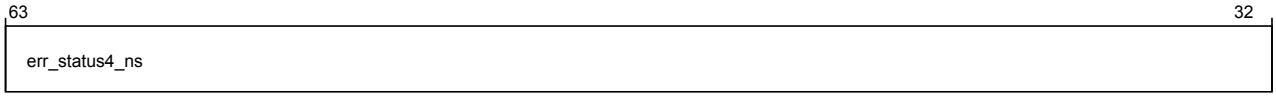


Figure 3-47 por_cfgm_por_cfgm_errgsr4_ns (high)

The following table shows the por_cfgm_errgsr4_NS higher register bit assignments.

Table 3-61 por_cfgm_por_cfgm_errgsr4_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

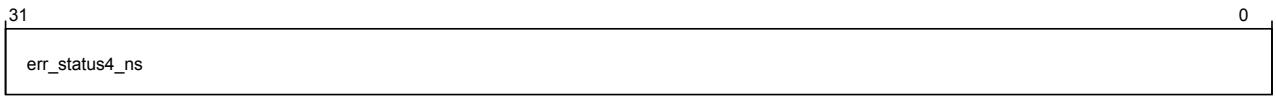


Figure 3-48 por_cfgm_por_cfgm_errgsr4_ns (low)

The following table shows the por_cfgm_errgsr4_NS lower register bit assignments.

Table 3-62 por_cfgm_por_cfgm_errgsr4_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status4_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errgsr5_NS

Provides the XP <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3180
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

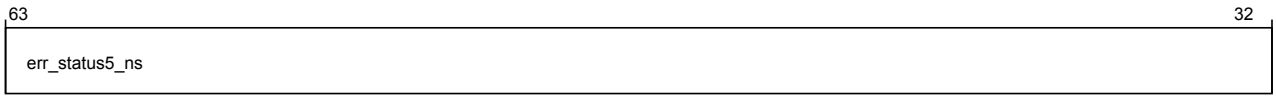


Figure 3-49 por_cfgm_por_cfgm_errgsr5_ns (high)

The following table shows the por_cfgm_errgsr5_NS higher register bit assignments.

Table 3-63 por_cfgm_por_cfgm_errgsr5_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status5_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

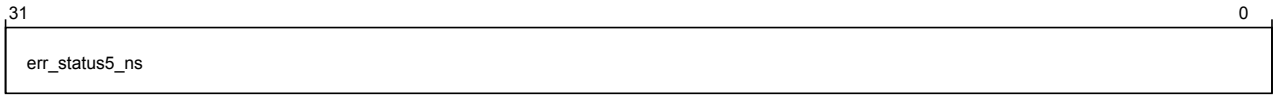


Figure 3-50 por_cfgm_por_cfgm_errgsr5_ns (low)

The following table shows the por_cfgm_errgsr5_NS lower register bit assignments.

Table 3-64 por_cfgm_por_cfgm_errgsr5_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status5_ns	Read-only copy of por_mxp_err<n>status	RO	64'h0

por_cfgm_errgsr6_NS

Provides the HN-I <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3188
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

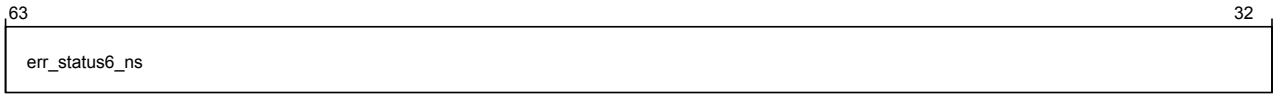


Figure 3-51 por_cfgm_por_cfgm_errgsr6_ns (high)

The following table shows the por_cfgm_errgsr6_NS higher register bit assignments.

Table 3-65 por_cfgm_por_cfgm_errgsr6_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status6_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

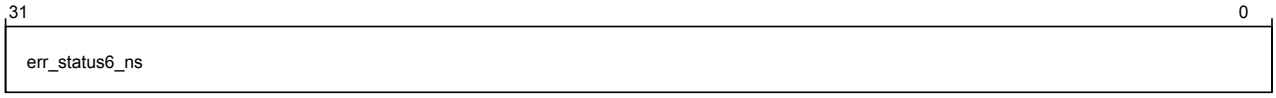


Figure 3-52 por_cfgm_por_cfgm_errgsr6_ns (low)

The following table shows the por_cfgm_errgsr6_NS lower register bit assignments.

Table 3-66 por_cfgm_por_cfgm_errgsr6_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status6_ns	Read-only copy of por_hni_err<n>status	RO	64'h0

por_cfgm_errgsr7_NS

Provides the HN-F <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3190
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

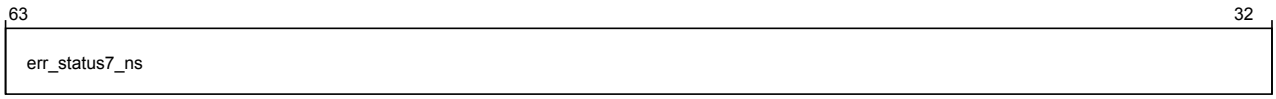


Figure 3-53 por_cfgm_por_cfgm_errgsr7_ns (high)

The following table shows the por_cfgm_errgsr7_NS higher register bit assignments.

Table 3-67 por_cfgm_por_cfgm_errgsr7_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status7_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

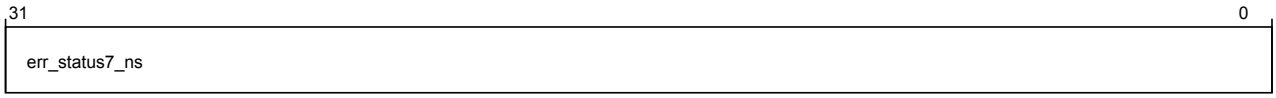


Figure 3-54 por_cfgm_por_cfgm_errgsr7_ns (low)

The following table shows the por_cfgm_errgsr7_NS lower register bit assignments.

Table 3-68 por_cfgm_por_cfgm_errgsr7_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status7_ns	Read-only copy of por_hnf_err<n>status	RO	64'h0

por_cfgm_errgsr8_NS

Provides the SBSX <n> non-secure fault status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3198
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

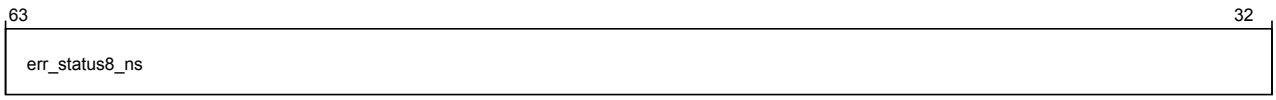


Figure 3-55 por_cfgm_por_cfgm_errgsr8_ns (high)

The following table shows the por_cfgm_errgsr8_NS higher register bit assignments.

Table 3-69 por_cfgm_por_cfgm_errgsr8_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status8_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

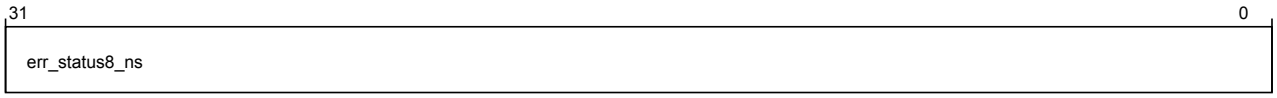


Figure 3-56 por_cfgm_por_cfgm_errgsr8_ns (low)

The following table shows the por_cfgm_errgsr8_NS lower register bit assignments.

Table 3-70 por_cfgm_por_cfgm_errgsr8_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status8_ns	Read-only copy of por_sbsx_err<n>status	RO	64'h0

por_cfgm_errgsr9_NS

Provides the CXG <n> secure error status.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h31A0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

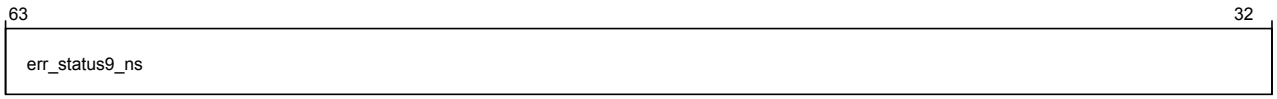


Figure 3-57 por_cfgm_por_cfgm_errgsr9_ns (high)

The following table shows the por_cfgm_errgsr9_NS higher register bit assignments.

Table 3-71 por_cfgm_por_cfgm_errgsr9_ns (high)

Bits	Field name	Description	Type	Reset
63:32	err_status9_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

The following image shows the lower register bit assignments.

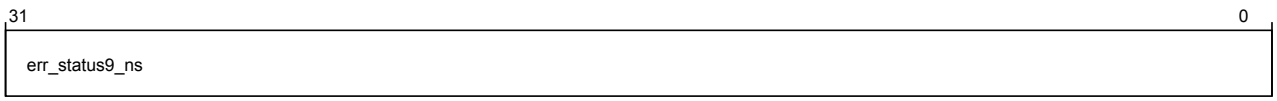


Figure 3-58 por_cfgm_por_cfgm_errgsr9_ns (low)

The following table shows the por_cfgm_errgsr9_NS lower register bit assignments.

Table 3-72 por_cfgm_por_cfgm_errgsr9_ns (low)

Bits	Field name	Description	Type	Reset
31:0	err_status9_ns	Read-only copy of por_cxg_err<n>status	RO	64'h0

por_cfgm_errdevaff

Functions as the device affinity register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3FA8

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

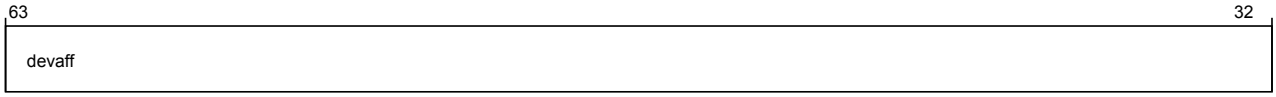


Figure 3-59 por_cfgm_por_cfgm_errdevaff (high)

The following table shows the por_cfgm_errdevaff higher register bit assignments.

Table 3-73 por_cfgm_por_cfgm_errdevaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following image shows the lower register bit assignments.

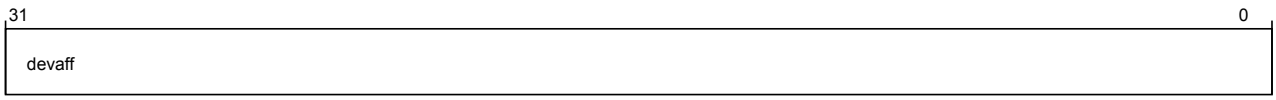


Figure 3-60 por_cfgm_por_cfgm_errdevaff (low)

The following table shows the por_cfgm_errdevaff lower register bit assignments.

Table 3-74 por_cfgm_por_cfgm_errdevaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

por_cfgm_errdevarch

Functions as the device architecture register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3FB8

Register reset 64'b0001011101110000000000101000

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

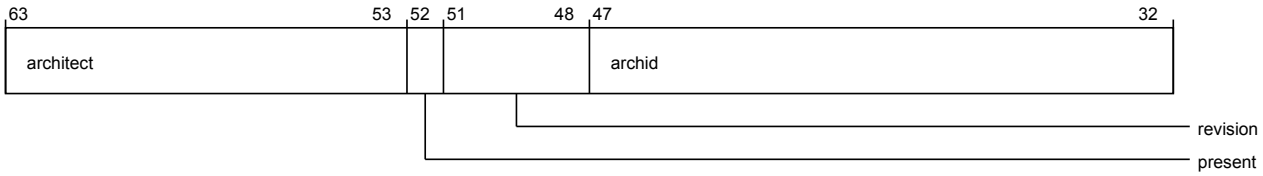


Figure 3-61 por_cfgm_por_cfgm_errdevarch (high)

The following table shows the por_cfgm_errdevarch higher register bit assignments.

Table 3-75 por_cfgm_por_cfgm_errdevarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'h23B
52	present	Present	RO	1'b1
51:48	revision	Architecture revision	RO	4'b0
47:32	archid	Architecture ID	RO	16'h0A00

The following image shows the lower register bit assignments.

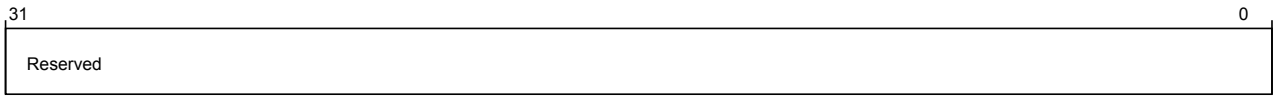


Figure 3-62 por_cfgm_por_cfgm_errdevarch (low)

The following table shows the por_cfgm_errdevarch lower register bit assignments.

Table 3-76 por_cfgm_por_cfgm_errdevarch (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_cfgm_erridr

Contains the number of error records.

Its characteristics are:

Type RO

Register width (Bits) 64
Address offset 14'h3FC8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

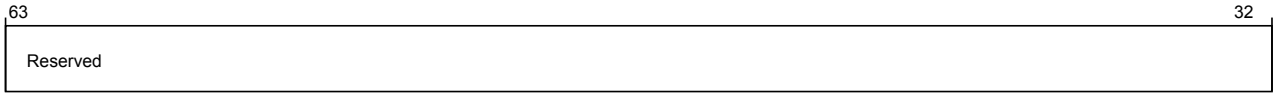


Figure 3-63 por_cfgm_por_cfgm_erridr (high)

The following table shows the por_cfgm_erridr higher register bit assignments.

Table 3-77 por_cfgm_por_cfgm_erridr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

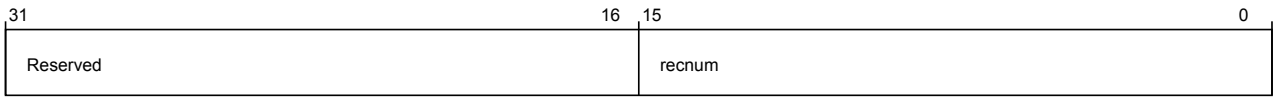


Figure 3-64 por_cfgm_por_cfgm_erridr (low)

The following table shows the por_cfgm_erridr lower register bit assignments.

Table 3-78 por_cfgm_por_cfgm_erridr (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	recnum	Number of error records; equal to 2*(number of logical devices)	RO	Configuration dependent

por_cfgm_errpidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FD0
Register reset 64'b000000100
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

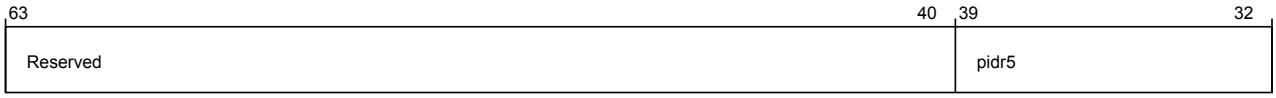


Figure 3-65 por_cfgm_por_cfgm_errpidr45 (high)

The following table shows the por_cfgm_errpidr45 higher register bit assignments.

Table 3-79 por_cfgm_por_cfgm_errpidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

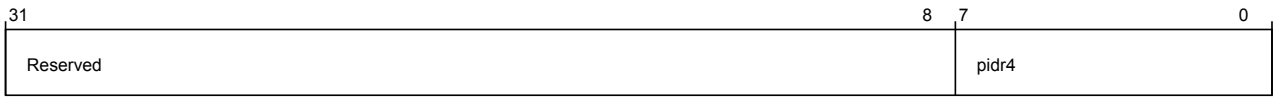


Figure 3-66 por_cfgm_por_cfgm_errpidr45 (low)

The following table shows the por_cfgm_errpidr45 lower register bit assignments.

Table 3-80 por_cfgm_por_cfgm_errpidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

por_cfgm_errpidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FD8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

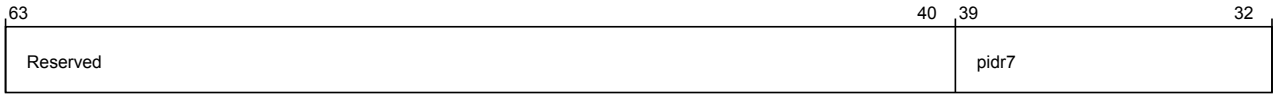


Figure 3-67 por_cfgm_por_cfgm_errpidr67 (high)

The following table shows the por_cfgm_errpidr67 higher register bit assignments.

Table 3-81 por_cfgm_por_cfgm_errpidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

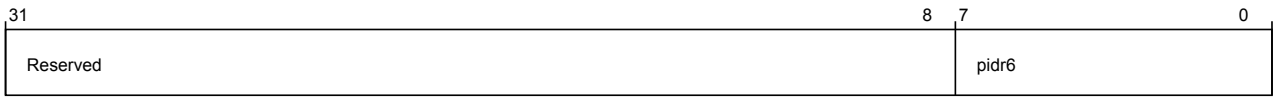


Figure 3-68 por_cfgm_por_cfgm_errpidr67 (low)

The following table shows the por_cfgm_errpidr67 lower register bit assignments.

Table 3-82 por_cfgm_por_cfgm_errpidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

por_cfgm_errpidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FE0
Register reset 64'b0101110000011100
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

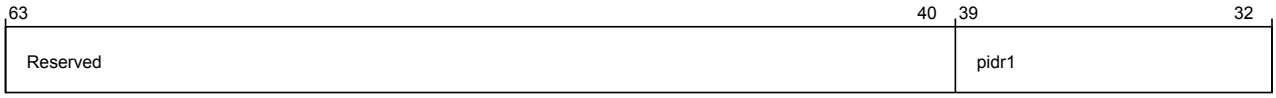


Figure 3-69 por_cfgm_por_cfgm_errpidr01 (high)

The following table shows the por_cfgm_errpidr01 higher register bit assignments.

Table 3-83 por_cfgm_por_cfgm_errpidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

The following image shows the lower register bit assignments.

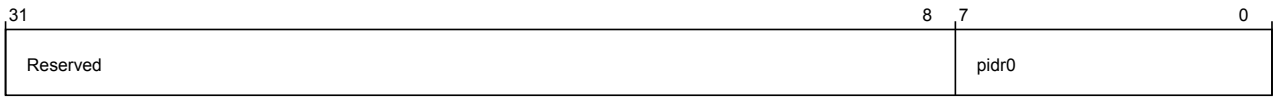


Figure 3-70 por_cfgm_por_cfgm_errpidr01 (low)

The following table shows the por_cfgm_errpidr01 lower register bit assignments.

Table 3-84 por_cfgm_por_cfgm_errpidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

por_cfgm_errpidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FE8
Register reset 64'b000000111
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

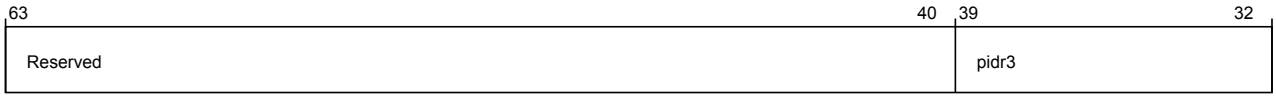


Figure 3-71 por_cfgm_por_cfgm_errpidr23 (high)

The following table shows the por_cfgm_errpidr23 higher register bit assignments.

Table 3-85 por_cfgm_por_cfgm_errpidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

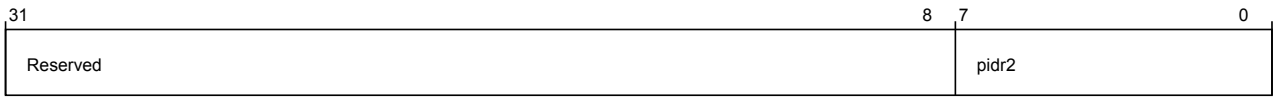


Figure 3-72 por_cfgm_por_cfgm_errpidr23 (low)

The following table shows the por_cfgm_errpidr23 lower register bit assignments.

Table 3-86 por_cfgm_por_cfgm_errpidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

por_cfgm_errcidr01

Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FF0
Register reset 64'b1111111100001101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

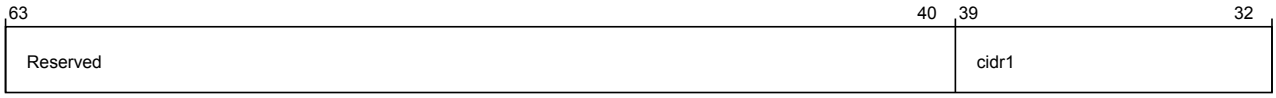


Figure 3-73 por_cfgm_por_cfgm_errcidr01 (high)

The following table shows the por_cfgm_errcidr01 higher register bit assignments.

Table 3-87 por_cfgm_por_cfgm_errcidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr1	Component ID 1	RO	8'hff

The following image shows the lower register bit assignments.

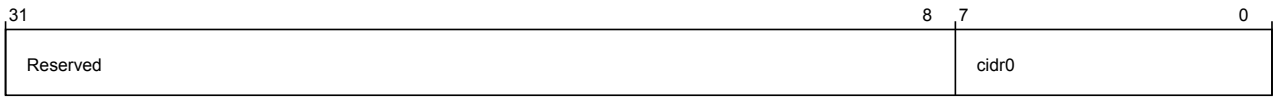


Figure 3-74 por_cfgm_por_cfgm_errcidr01 (low)

The following table shows the por_cfgm_errcidr01 lower register bit assignments.

Table 3-88 por_cfgm_por_cfgm_errcidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr0	Component ID 0	RO	8'hd

por_cfgm_errcidr23

Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3FF8
Register reset 64'b0001011100000101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

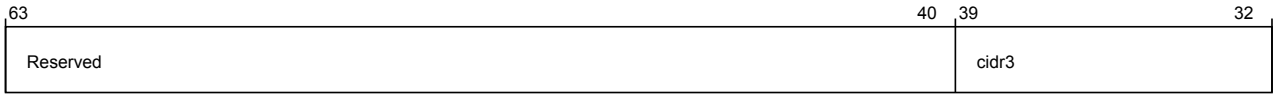


Figure 3-75 por_cfgm_por_cfgm_errcidr23 (high)

The following table shows the por_cfgm_errcidr23 higher register bit assignments.

Table 3-89 por_cfgm_por_cfgm_errcidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr3	Component ID 3	RO	8'hb1

The following image shows the lower register bit assignments.

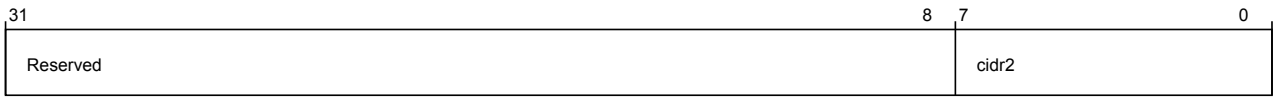


Figure 3-76 por_cfgm_por_cfgm_errcidr23 (low)

The following table shows the por_cfgm_errcidr23 lower register bit assignments.

Table 3-90 por_cfgm_por_cfgm_errcidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

por_info_global

Contains user-specified values of build-time global configuration parameters.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

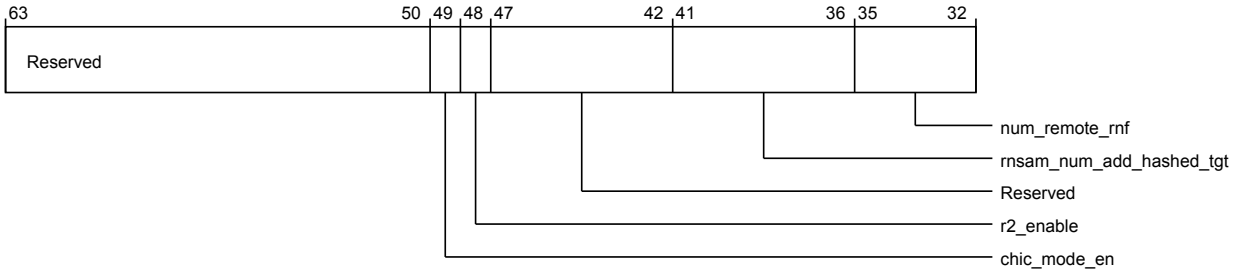


Figure 3-77 por_cfgm_por_info_global (high)

The following table shows the por_info_global higher register bit assignments.

Table 3-91 por_cfgm_por_info_global (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49	chic_mode_en	CHI-C mode enable	RO	Configuration dependent
48	r2_enable	CMN R2 feature enable	RO	Configuration dependent
47:42	Reserved	Reserved	RO	-
41:36	rnsam_num_add_hashed_tgt	Number of additional hashed target ID's supported by the RN SAM, beyond the local HNF count	RO	Configuration dependent
35:32	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent

The following image shows the lower register bit assignments.

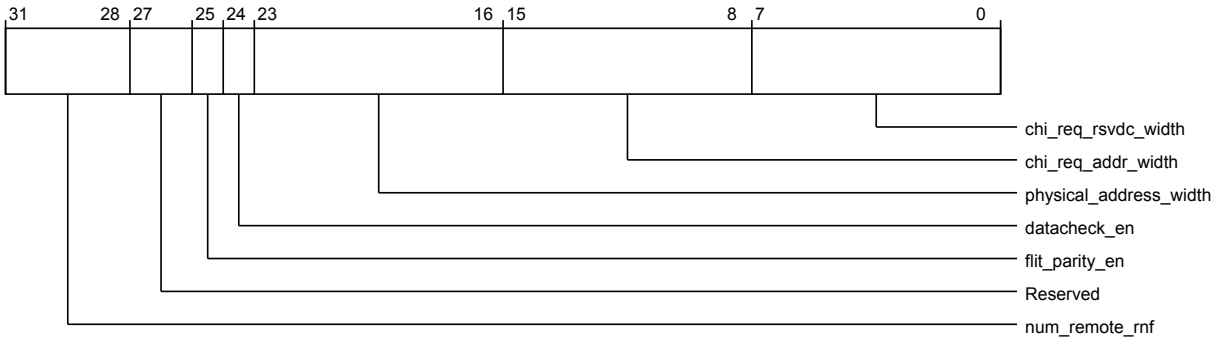


Figure 3-78 por_cfgm_por_info_global (low)

The following table shows the por_info_global lower register bit assignments.

Table 3-92 por_cfgm_por_info_global (low)

Bits	Field name	Description	Type	Reset
31:28	num_remote_rnf	Number of remote RN-F devices in the system when the CML feature is enabled	RO	Configuration dependent
27:26	Reserved	Reserved	RO	-
25	flit_parity_en	Indicates whether parity checking is enabled in the transport layer on all flits sent on the interconnect	RO	Configuration dependent
24	datacheck_en	Indicates whether datacheck feature is enabled for CHI DAT flit	RO	Configuration dependent
23:16	physical_address_width	Physical address width	RO	Configuration dependent
15:8	chi_req_addr_width	REQ address width	RO	Configuration dependent
7:0	chi_req_rsvdc_width	RSVDC field width in CHI REQ flit	RO	Configuration dependent

por_ppu_int_enable

Configures the HN-F PPU event interrupt. Contains the interrupt mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1000
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

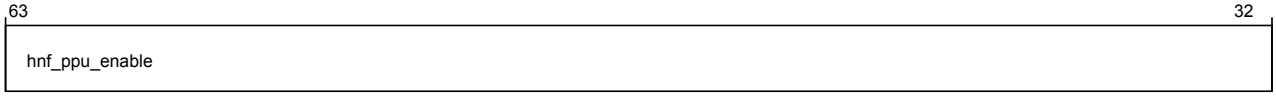


Figure 3-79 por_cfgm_por_ppu_int_enable (high)

The following table shows the por_ppu_int_enable higher register bit assignments.

Table 3-93 por_cfgm_por_ppu_int_enable (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_enable	Interrupt mask	RW	64'b0

The following image shows the lower register bit assignments.

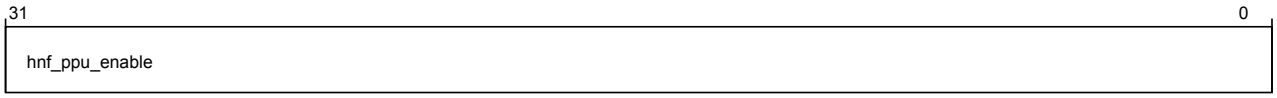


Figure 3-80 por_cfgm_por_ppu_int_enable (low)

The following table shows the por_ppu_int_enable lower register bit assignments.

Table 3-94 por_cfgm_por_ppu_int_enable (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_enable	Interrupt mask	RW	64'b0

por_ppu_int_status

Provides HN-F PPU event interrupt status.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h1008
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

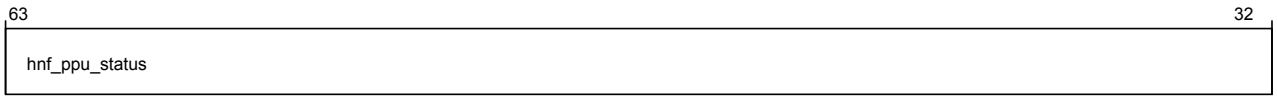


Figure 3-81 por_cfgm_por_ppu_int_status (high)

The following table shows the por_ppu_int_status higher register bit assignments.

Table 3-95 por_cfgm_por_ppu_int_status (high)

Bits	Field name	Description	Type	Reset
63:32	hnf_ppu_status	Interrupt status	W1C	64'b0

The following image shows the lower register bit assignments.

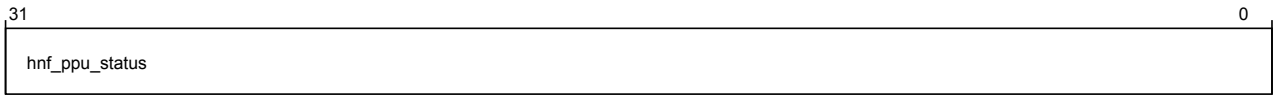


Figure 3-82 por_cfgm_por_ppu_int_status (low)

The following table shows the por_ppu_int_status lower register bit assignments.

Table 3-96 por_cfgm_por_ppu_int_status (low)

Bits	Field name	Description	Type	Reset
31:0	hnf_ppu_status	Interrupt status	W1C	64'b0

por_ppu_qactive_hyst

Number of hysteresis clock cycles to retain QACTIVE assertion

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1010
Register reset 64'b0000000000000010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

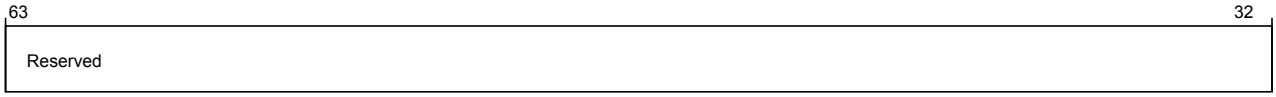


Figure 3-83 por_cfgm_por_ppu_qactive_hyst (high)

The following table shows the por_ppu_qactive_hyst higher register bit assignments.

Table 3-97 por_cfgm_por_ppu_qactive_hyst (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

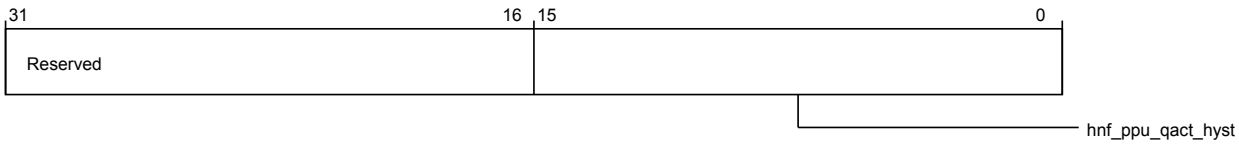


Figure 3-84 por_cfgm_por_ppu_qactive_hyst (low)

The following table shows the por_ppu_qactive_hyst lower register bit assignments.

Table 3-98 por_cfgm_por_ppu_qactive_hyst (low)

Bits	Field name	Description	Type	Reset
31:16	Reserved	Reserved	RO	-
15:0	hnf_ppu_qact_hyst	QACTIVE hysteresis	RW	16'h10

por_cfgm_child_pointer_0

Contains base address of child configuration node. NOTE: There will be as many child pointer registers in the Global Config Unit as the number of XP's on the chip. Each successive child pointer register will be at the next 8 byte address boundary. Each successive child pointer register will be named with the suffix corresponding to the register number. For example por_cfgm_child_pointer_<number>

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h100

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

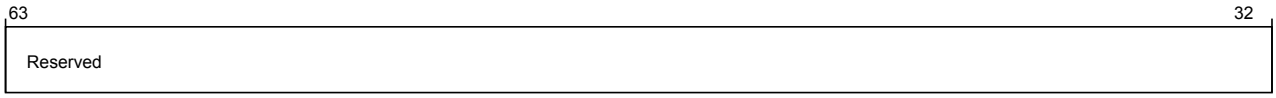


Figure 3-85 por_cfgm_por_cfgm_child_pointer_0 (high)

The following table shows the por_cfgm_child_pointer_0 higher register bit assignments.

Table 3-99 por_cfgm_por_cfgm_child_pointer_0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

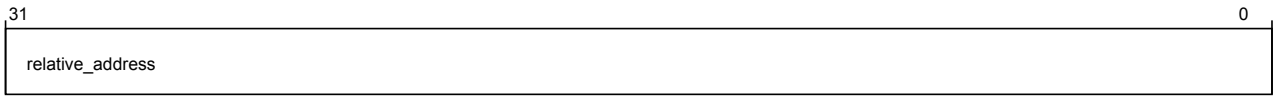


Figure 3-86 por_cfgm_por_cfgm_child_pointer_0 (low)

The following table shows the por_cfgm_child_pointer_0 lower register bit assignments.

Table 3-100 por_cfgm_por_cfgm_child_pointer_0 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address	Bit 31: External or internal child node 1'b1: Indicates child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

3.3.2 DN register descriptions

This section lists the DN registers.

por_dn_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

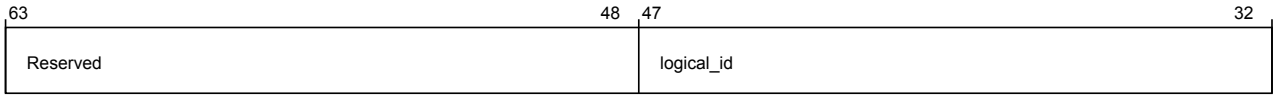


Figure 3-87 por_dn_por_dn_node_info (high)

The following table shows the por_dn_node_info higher register bit assignments.

Table 3-101 por_dn_por_dn_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

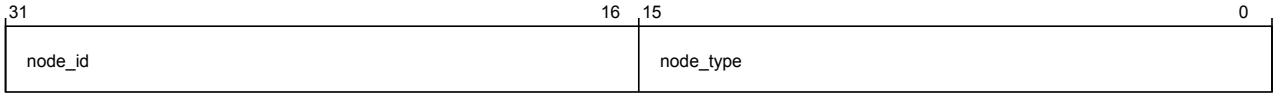


Figure 3-88 por_dn_por_dn_node_info (low)

The following table shows the por_dn_node_info lower register bit assignments.

Table 3-102 por_dn_por_dn_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0001

por_dn_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

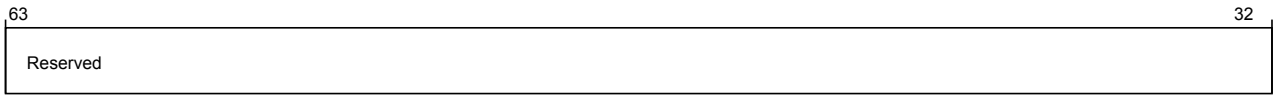


Figure 3-89 por_dn_por_dn_child_info (high)

The following table shows the por_dn_child_info higher register bit assignments.

Table 3-103 por_dn_por_dn_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

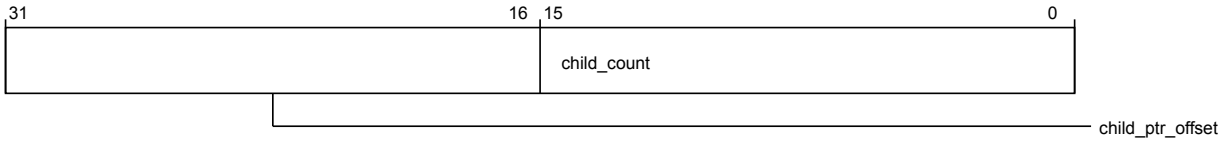


Figure 3-90 por_dn_por_dn_child_info (low)

The following table shows the por_dn_child_info lower register bit assignments.

Table 3-104 por_dn_por_dn_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_dn_build_info

Contains the configuration parameter values. Indicates the specific DN configuration.

Its characteristics are:

Type RO
Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

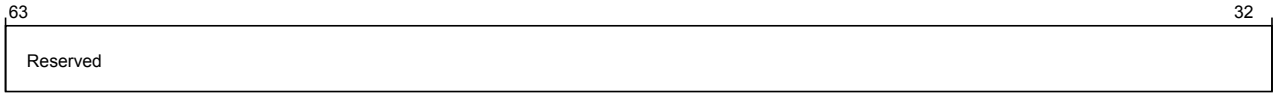


Figure 3-91 por_dn_por_dn_build_info (high)

The following table shows the por_dn_build_info higher register bit assignments.

Table 3-105 por_dn_por_dn_build_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

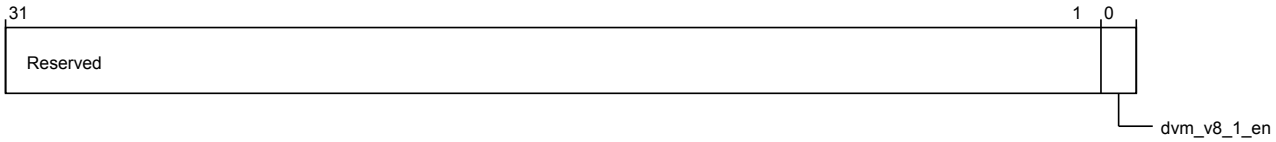


Figure 3-92 por_dn_por_dn_build_info (low)

The following table shows the por_dn_build_info lower register bit assignments.

Table 3-106 por_dn_por_dn_build_info (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	dvm_v8_1_en	Determines whether all nodes receiving DVM snoops support DVM v8.1 operations; must be set to 0 if not supported by all nodes, therefore allowing the node to perform demotion before sending out the DVM snoop	RO	Configuration dependent

por_dn_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

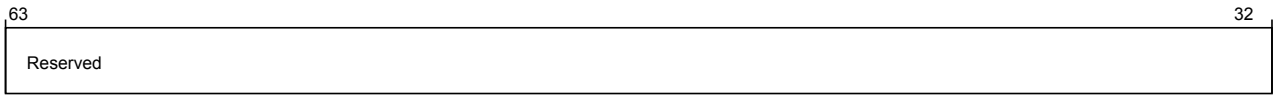


Figure 3-93 por_dn_por_dn_secure_register_groups_override (high)

The following table shows the por_dn_secure_register_groups_override higher register bit assignments.

Table 3-107 por_dn_por_dn_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

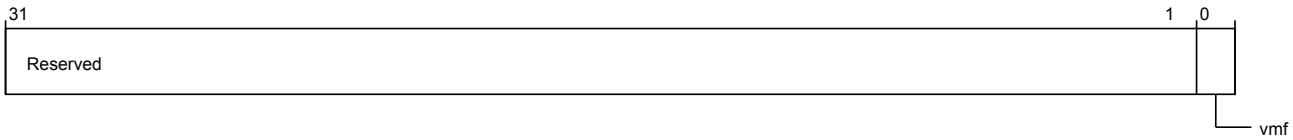


Figure 3-94 por_dn_por_dn_secure_register_groups_override (low)

The following table shows the por_dn_secure_register_groups_override lower register bit assignments.

Table 3-108 por_dn_por_dn_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	vmf	Allows non-secure access to secure VMF registers	RW	1'b0

por_dn_aux_ctl

Functions as the auxiliary control register for DN.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

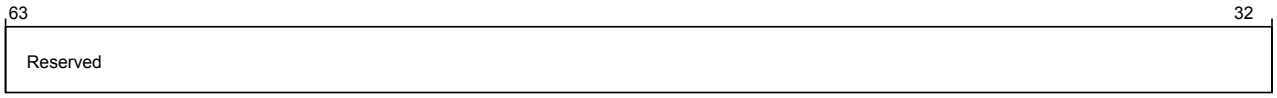


Figure 3-95 por_dn_por_dn_aux_ctl (high)

The following table shows the por_dn_aux_ctl higher register bit assignments.

Table 3-109 por_dn_por_dn_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

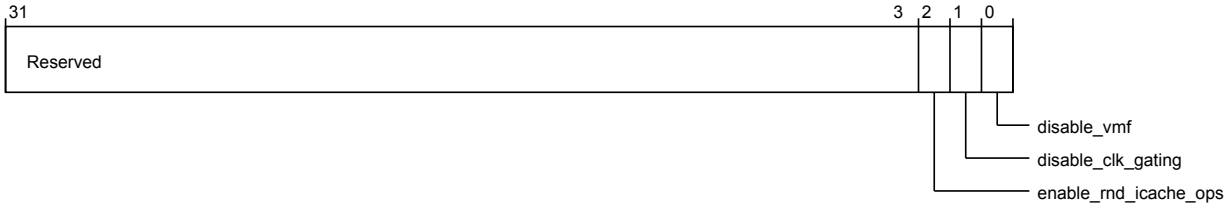


Figure 3-96 por_dn_por_dn_aux_ctl (low)

The following table shows the por_dn_aux_ctl lower register bit assignments.

Table 3-110 por_dn_por_dn_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	enable_rnd_icache_ops	Filters out BPI and VICI/PICI Snps to RNDs when set	RW	Configuration dependent
1	disable_clk_gating	Disables autonomous clock gating when set	RW	1'b0
0	disable_vmf	This bit is currently not supported. Software must not program this bit.	RW	Configuration dependent

por_dn_vmf0_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

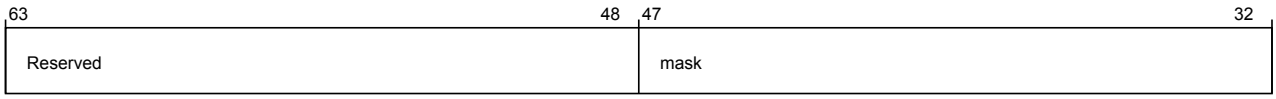


Figure 3-97 por_dn_por_dn_vmf0_ctrl (high)

The following table shows the por_dn_vmf0_ctrl higher register bit assignments.

Table 3-111 por_dn_por_dn_vmf0_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf0_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

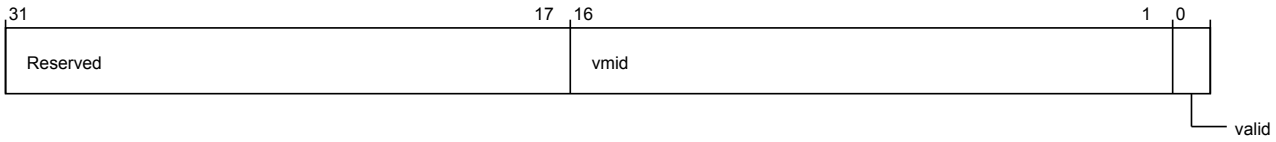


Figure 3-98 por_dn_por_dn_vmf0_ctrl (low)

The following table shows the por_dn_vmf0_ctrl lower register bit assignments.

Table 3-112 por_dn_por_dn_vmf0_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf0_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

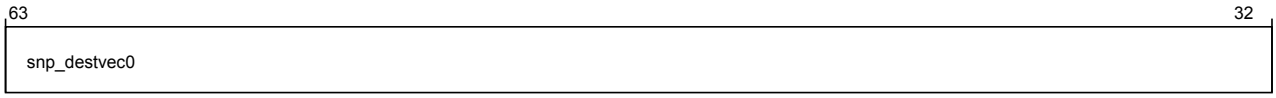


Figure 3-99 por_dn_por_dn_vmf0_rnf0 (high)

The following table shows the por_dn_vmf0_rnf0 higher register bit assignments.

Table 3-113 por_dn_por_dn_vmf0_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

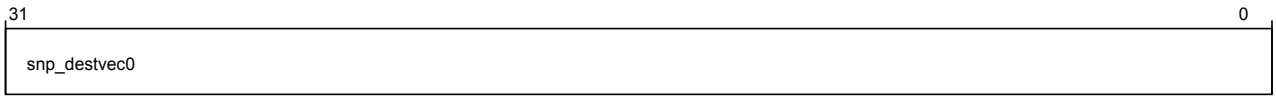


Figure 3-100 por_dn_por_dn_vmf0_rnf0 (low)

The following table shows the por_dn_vmf0_rnf0 lower register bit assignments.

Table 3-114 por_dn_por_dn_vmf0_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

por_dn_vmf0_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

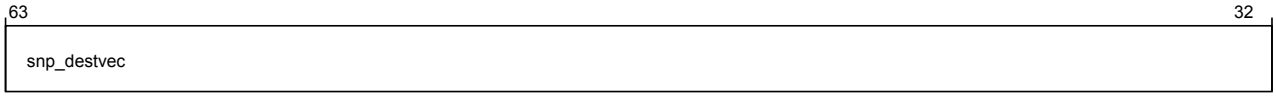


Figure 3-101 por_dn_por_dn_vmf0_rnd (high)

The following table shows the por_dn_vmf0_rnd higher register bit assignments.

Table 3-115 por_dn_por_dn_vmf0_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

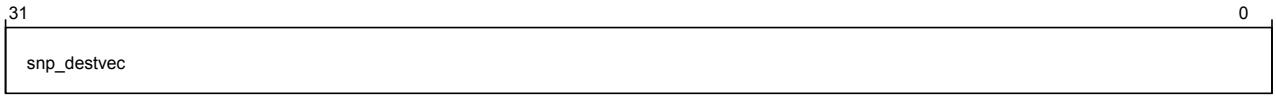


Figure 3-102 por_dn_por_dn_vmf0_rnd (low)

The following table shows the por_dn_vmf0_rnd lower register bit assignments.

Table 3-116 por_dn_por_dn_vmf0_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

por_dn_vmf0_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

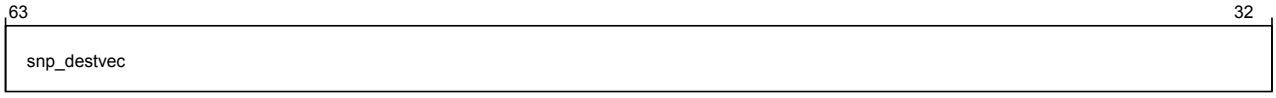


Figure 3-103 por_dn_por_dn_vmf0_cxra (high)

The following table shows the por_dn_vmf0_cxra higher register bit assignments.

Table 3-117 por_dn_por_dn_vmf0_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

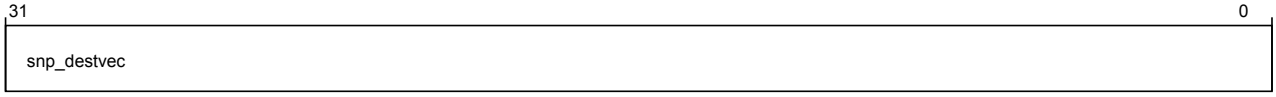


Figure 3-104 por_dn_por_dn_vmf0_cxra (low)

The following table shows the por_dn_vmf0_cxra lower register bit assignments.

Table 3-118 por_dn_por_dn_vmf0_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf0_ctrl.vmid	RW	64'b0

por_dn_vmf1_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC20

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

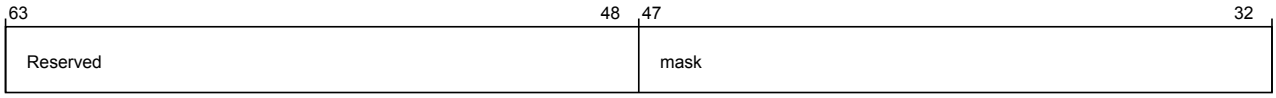


Figure 3-105 por_dn_por_dn_vmf1_ctrl (high)

The following table shows the por_dn_vmf1_ctrl higher register bit assignments.

Table 3-119 por_dn_por_dn_vmf1_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf1_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

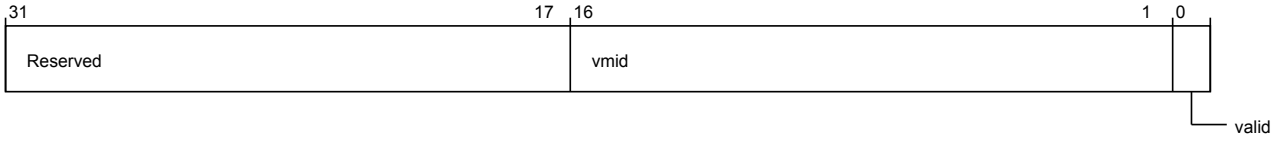


Figure 3-106 por_dn_por_dn_vmf1_ctrl (low)

The following table shows the por_dn_vmf1_ctrl lower register bit assignments.

Table 3-120 por_dn_por_dn_vmf1_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf1_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

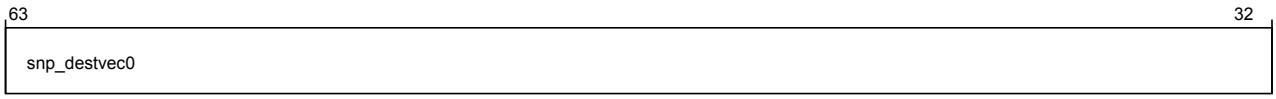


Figure 3-107 por_dn_por_dn_vmf1_rnf0 (high)

The following table shows the por_dn_vmf1_rnf0 higher register bit assignments.

Table 3-121 por_dn_por_dn_vmf1_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

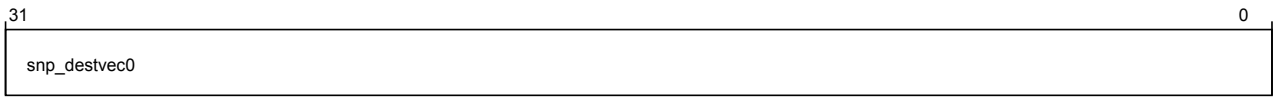


Figure 3-108 por_dn_por_dn_vmf1_rnf0 (low)

The following table shows the por_dn_vmf1_rnf0 lower register bit assignments.

Table 3-122 por_dn_por_dn_vmf1_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf1_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

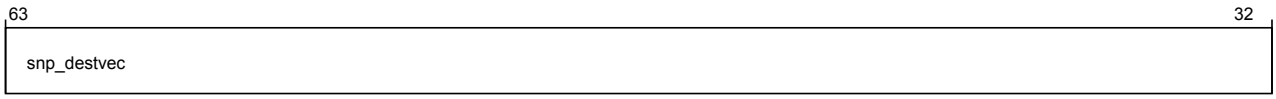


Figure 3-109 por_dn_por_dn_vmf1_rnd (high)

The following table shows the por_dn_vmf1_rnd higher register bit assignments.

Table 3-123 por_dn_por_dn_vmf1_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

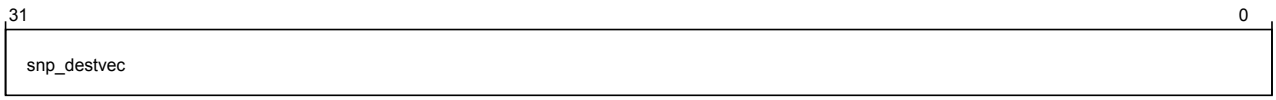


Figure 3-110 por_dn_por_dn_vmf1_rnd (low)

The following table shows the por_dn_vmf1_rnd lower register bit assignments.

Table 3-124 por_dn_por_dn_vmf1_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf1_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

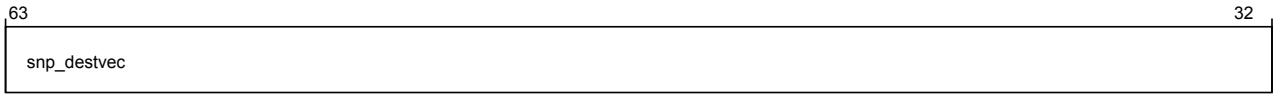


Figure 3-111 por_dn_por_dn_vmf1_cxra (high)

The following table shows the por_dn_vmf1_cxra higher register bit assignments.

Table 3-125 por_dn_por_dn_vmf1_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

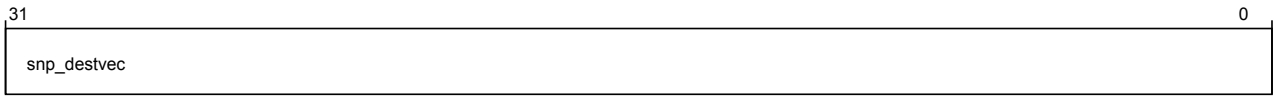


Figure 3-112 por_dn_por_dn_vmf1_cxra (low)

The following table shows the por_dn_vmf1_cxra lower register bit assignments.

Table 3-126 por_dn_por_dn_vmf1_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf1_ctrl.vmid	RW	64'b0

por_dn_vmf2_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC40

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

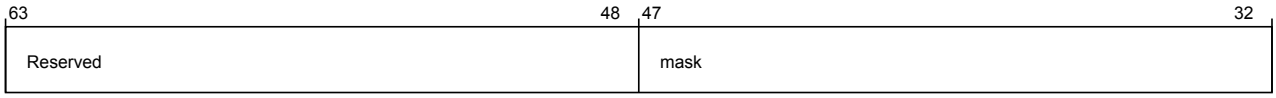


Figure 3-113 por_dn_por_dn_vmf2_ctrl (high)

The following table shows the por_dn_vmf2_ctrl higher register bit assignments.

Table 3-127 por_dn_por_dn_vmf2_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf2_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

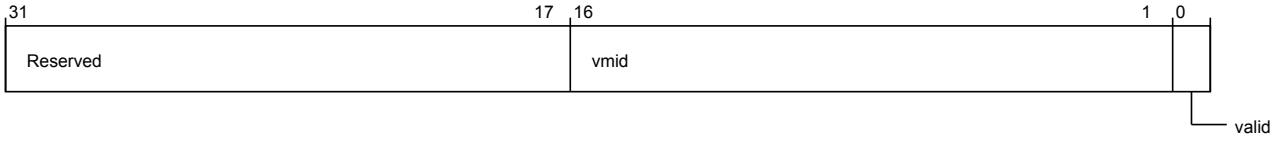


Figure 3-114 por_dn_por_dn_vmf2_ctrl (low)

The following table shows the por_dn_vmf2_ctrl lower register bit assignments.

Table 3-128 por_dn_por_dn_vmf2_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf2_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

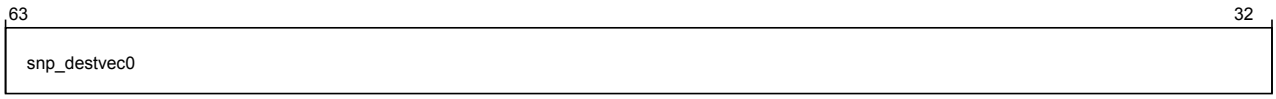


Figure 3-115 por_dn_por_dn_vmf2_rnf0 (high)

The following table shows the por_dn_vmf2_rnf0 higher register bit assignments.

Table 3-129 por_dn_por_dn_vmf2_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

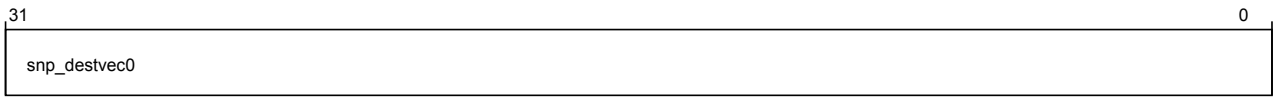


Figure 3-116 por_dn_por_dn_vmf2_rnf0 (low)

The following table shows the por_dn_vmf2_rnf0 lower register bit assignments.

Table 3-130 por_dn_por_dn_vmf2_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf2_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

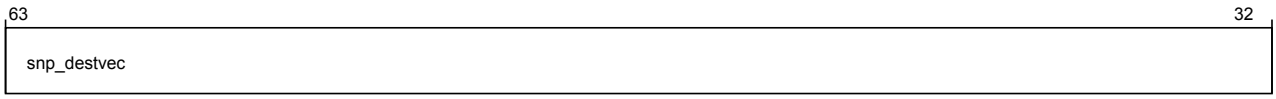


Figure 3-117 por_dn_por_dn_vmf2_rnd (high)

The following table shows the por_dn_vmf2_rnd higher register bit assignments.

Table 3-131 por_dn_por_dn_vmf2_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

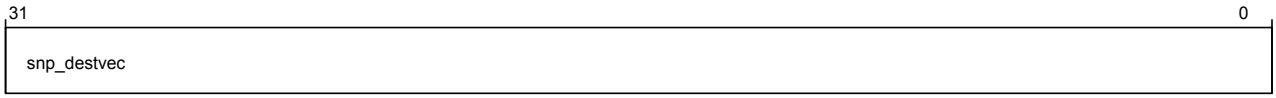


Figure 3-118 por_dn_por_dn_vmf2_rnd (low)

The following table shows the por_dn_vmf2_rnd lower register bit assignments.

Table 3-132 por_dn_por_dn_vmf2_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf2_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

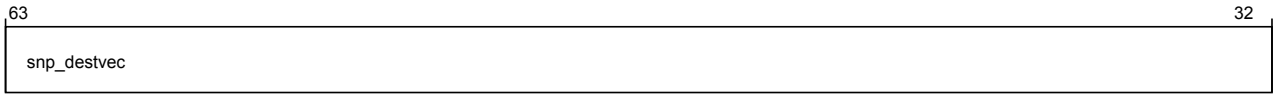


Figure 3-119 por_dn_por_dn_vmf2_cxra (high)

The following table shows the por_dn_vmf2_cxra higher register bit assignments.

Table 3-133 por_dn_por_dn_vmf2_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

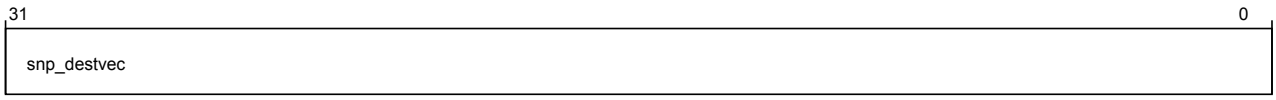


Figure 3-120 por_dn_por_dn_vmf2_cxra (low)

The following table shows the por_dn_vmf2_cxra lower register bit assignments.

Table 3-134 por_dn_por_dn_vmf2_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf2_ctrl.vmid	RW	64'b0

por_dn_vmf3_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

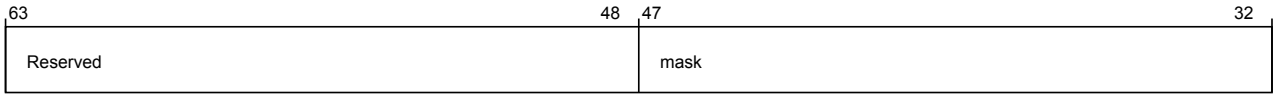


Figure 3-121 por_dn_por_dn_vmf3_ctrl (high)

The following table shows the por_dn_vmf3_ctrl higher register bit assignments.

Table 3-135 por_dn_por_dn_vmf3_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf3_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

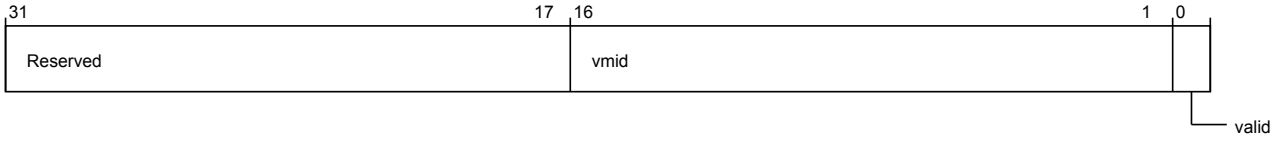


Figure 3-122 por_dn_por_dn_vmf3_ctrl (low)

The following table shows the por_dn_vmf3_ctrl lower register bit assignments.

Table 3-136 por_dn_por_dn_vmf3_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf3_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

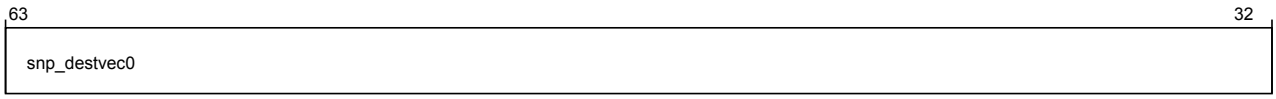


Figure 3-123 por_dn_por_dn_vmf3_rnf0 (high)

The following table shows the por_dn_vmf3_rnf0 higher register bit assignments.

Table 3-137 por_dn_por_dn_vmf3_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

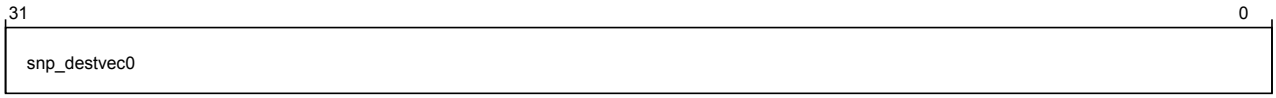


Figure 3-124 por_dn_por_dn_vmf3_rnf0 (low)

The following table shows the por_dn_vmf3_rnf0 lower register bit assignments.

Table 3-138 por_dn_por_dn_vmf3_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf3_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

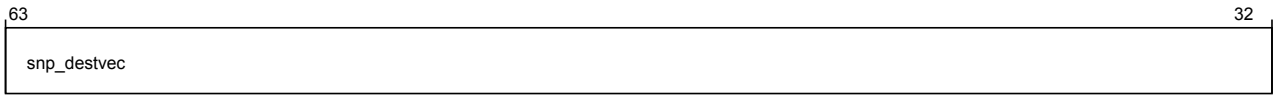


Figure 3-125 por_dn_por_dn_vmf3_rnd (high)

The following table shows the por_dn_vmf3_rnd higher register bit assignments.

Table 3-139 por_dn_por_dn_vmf3_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

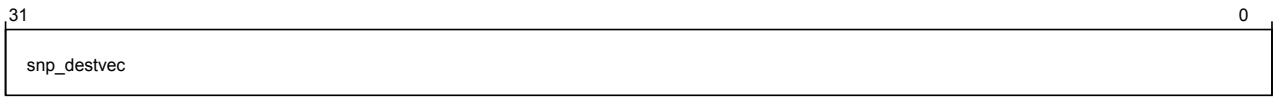


Figure 3-126 por_dn_por_dn_vmf3_rnd (low)

The following table shows the por_dn_vmf3_rnd lower register bit assignments.

Table 3-140 por_dn_por_dn_vmf3_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf3_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

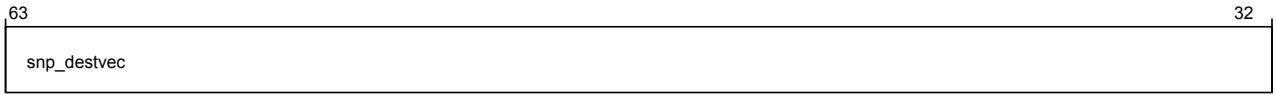


Figure 3-127 por_dn_por_dn_vmf3_cxra (high)

The following table shows the por_dn_vmf3_cxra higher register bit assignments.

Table 3-141 por_dn_por_dn_vmf3_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

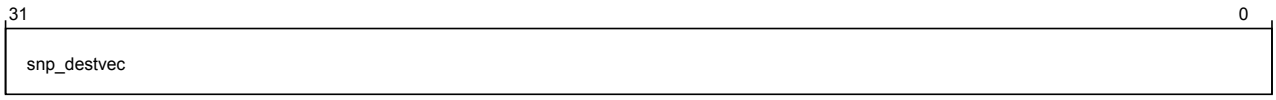


Figure 3-128 por_dn_por_dn_vmf3_cxra (low)

The following table shows the por_dn_vmf3_cxra lower register bit assignments.

Table 3-142 por_dn_por_dn_vmf3_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf3_ctrl.vmid	RW	64'b0

por_dn_vmf4_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC80

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

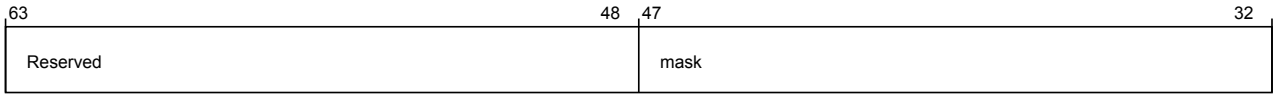


Figure 3-129 por_dn_por_dn_vmf4_ctrl (high)

The following table shows the por_dn_vmf4_ctrl higher register bit assignments.

Table 3-143 por_dn_por_dn_vmf4_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf4_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

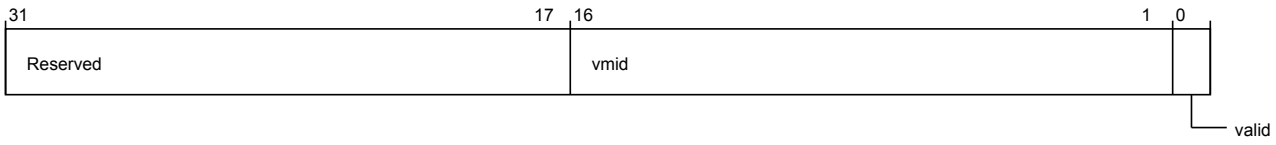


Figure 3-130 por_dn_por_dn_vmf4_ctrl (low)

The following table shows the por_dn_vmf4_ctrl lower register bit assignments.

Table 3-144 por_dn_por_dn_vmf4_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf4_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

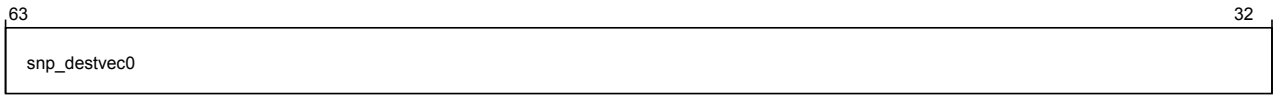


Figure 3-131 por_dn_por_dn_vmf4_rnf0 (high)

The following table shows the por_dn_vmf4_rnf0 higher register bit assignments.

Table 3-145 por_dn_por_dn_vmf4_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

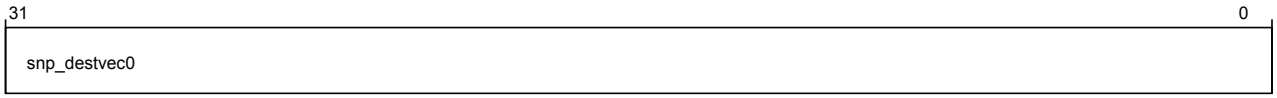


Figure 3-132 por_dn_por_dn_vmf4_rnf0 (low)

The following table shows the por_dn_vmf4_rnf0 lower register bit assignments.

Table 3-146 por_dn_por_dn_vmf4_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf4_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

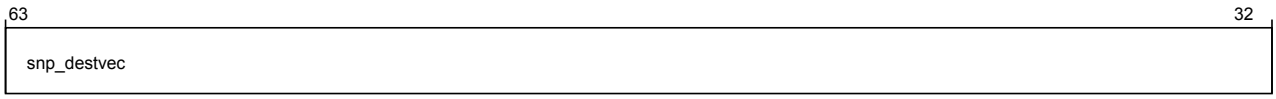


Figure 3-133 por_dn_por_dn_vmf4_rnd (high)

The following table shows the por_dn_vmf4_rnd higher register bit assignments.

Table 3-147 por_dn_por_dn_vmf4_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

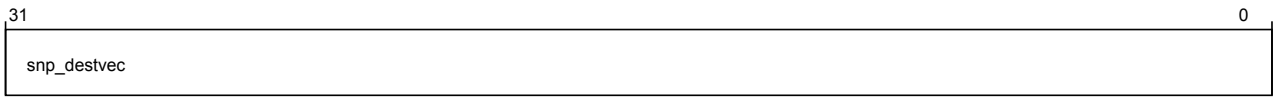


Figure 3-134 por_dn_por_dn_vmf4_rnd (low)

The following table shows the por_dn_vmf4_rnd lower register bit assignments.

Table 3-148 por_dn_por_dn_vmf4_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf4_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

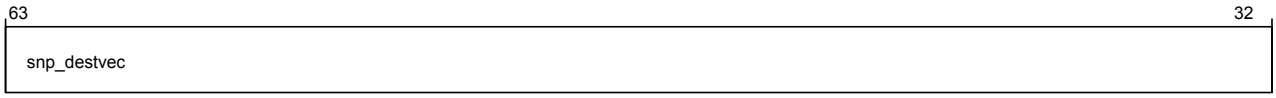


Figure 3-135 por_dn_por_dn_vmf4_cxra (high)

The following table shows the por_dn_vmf4_cxra higher register bit assignments.

Table 3-149 por_dn_por_dn_vmf4_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

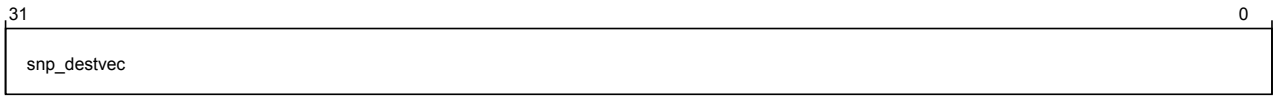


Figure 3-136 por_dn_por_dn_vmf4_cxra (low)

The following table shows the por_dn_vmf4_cxra lower register bit assignments.

Table 3-150 por_dn_por_dn_vmf4_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf4_ctrl.vmid	RW	64'b0

por_dn_vmf5_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCA0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

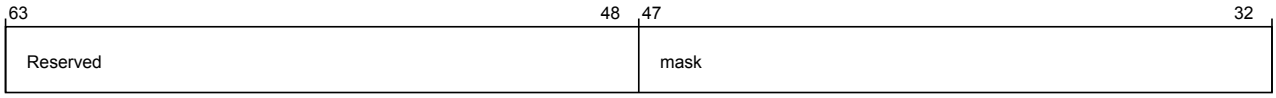


Figure 3-137 por_dn_por_dn_vmf5_ctrl (high)

The following table shows the por_dn_vmf5_ctrl higher register bit assignments.

Table 3-151 por_dn_por_dn_vmf5_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf5_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

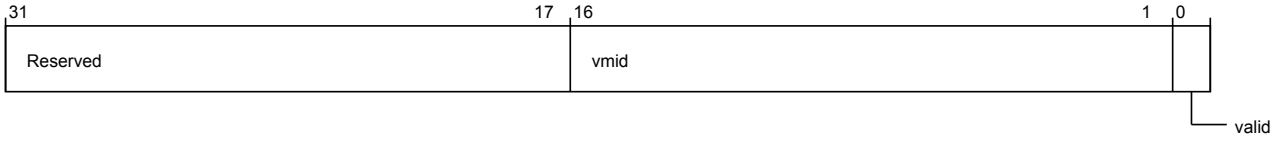


Figure 3-138 por_dn_por_dn_vmf5_ctrl (low)

The following table shows the por_dn_vmf5_ctrl lower register bit assignments.

Table 3-152 por_dn_por_dn_vmf5_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf5_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

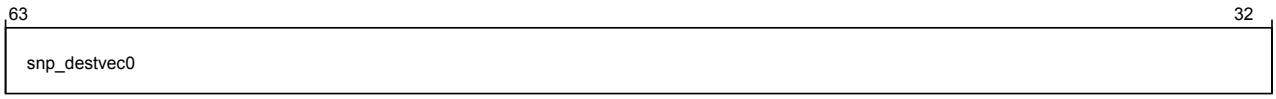


Figure 3-139 por_dn_por_dn_vmf5_rnf0 (high)

The following table shows the por_dn_vmf5_rnf0 higher register bit assignments.

Table 3-153 por_dn_por_dn_vmf5_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

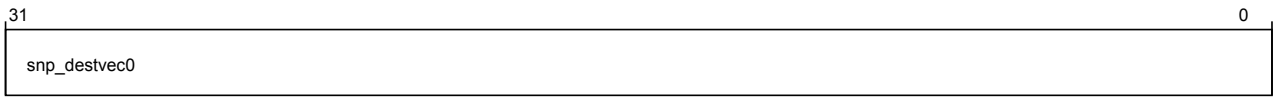


Figure 3-140 por_dn_por_dn_vmf5_rnf0 (low)

The following table shows the por_dn_vmf5_rnf0 lower register bit assignments.

Table 3-154 por_dn_por_dn_vmf5_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf5_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

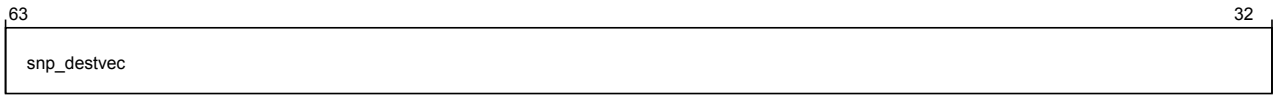


Figure 3-141 por_dn_por_dn_vmf5_rnd (high)

The following table shows the por_dn_vmf5_rnd higher register bit assignments.

Table 3-155 por_dn_por_dn_vmf5_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

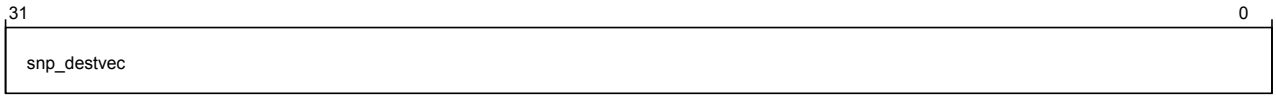


Figure 3-142 por_dn_por_dn_vmf5_rnd (low)

The following table shows the por_dn_vmf5_rnd lower register bit assignments.

Table 3-156 por_dn_por_dn_vmf5_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf5_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

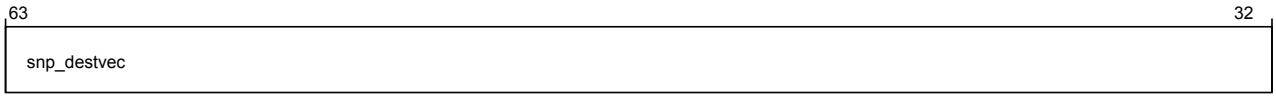


Figure 3-143 por_dn_por_dn_vmf5_cxra (high)

The following table shows the por_dn_vmf5_cxra higher register bit assignments.

Table 3-157 por_dn_por_dn_vmf5_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

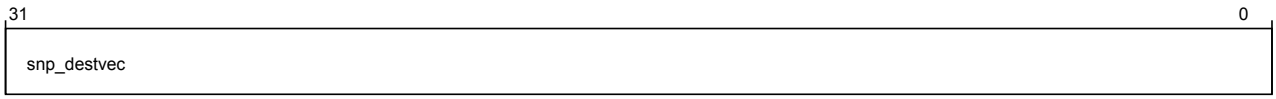


Figure 3-144 por_dn_por_dn_vmf5_cxra (low)

The following table shows the por_dn_vmf5_cxra lower register bit assignments.

Table 3-158 por_dn_por_dn_vmf5_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf5_ctrl.vmid	RW	64'b0

por_dn_vmf6_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCC0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

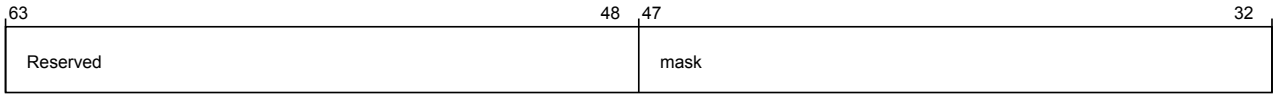


Figure 3-145 por_dn_por_dn_vmf6_ctrl (high)

The following table shows the por_dn_vmf6_ctrl higher register bit assignments.

Table 3-159 por_dn_por_dn_vmf6_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf6_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

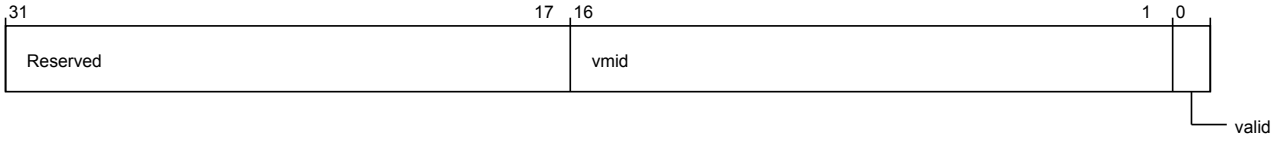


Figure 3-146 por_dn_por_dn_vmf6_ctrl (low)

The following table shows the por_dn_vmf6_ctrl lower register bit assignments.

Table 3-160 por_dn_por_dn_vmf6_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf6_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

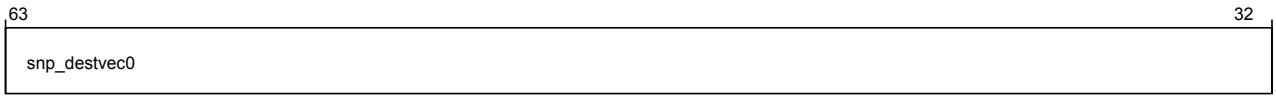


Figure 3-147 por_dn_por_dn_vmf6_rnf0 (high)

The following table shows the por_dn_vmf6_rnf0 higher register bit assignments.

Table 3-161 por_dn_por_dn_vmf6_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

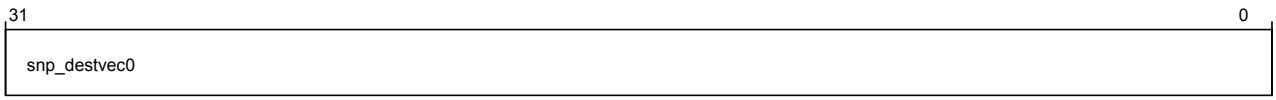


Figure 3-148 por_dn_por_dn_vmf6_rnf0 (low)

The following table shows the por_dn_vmf6_rnf0 lower register bit assignments.

Table 3-162 por_dn_por_dn_vmf6_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf6_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

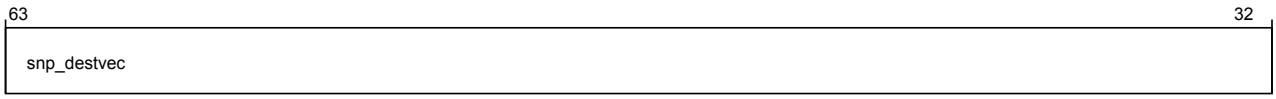


Figure 3-149 por_dn_por_dn_vmf6_rnd (high)

The following table shows the por_dn_vmf6_rnd higher register bit assignments.

Table 3-163 por_dn_por_dn_vmf6_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

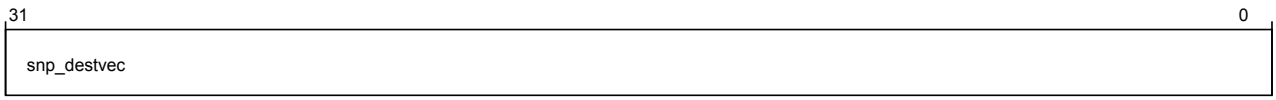


Figure 3-150 por_dn_por_dn_vmf6_rnd (low)

The following table shows the por_dn_vmf6_rnd lower register bit assignments.

Table 3-164 por_dn_por_dn_vmf6_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf6_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

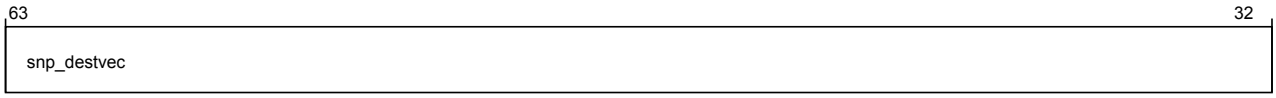


Figure 3-151 por_dn_por_dn_vmf6_cxra (high)

The following table shows the por_dn_vmf6_cxra higher register bit assignments.

Table 3-165 por_dn_por_dn_vmf6_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

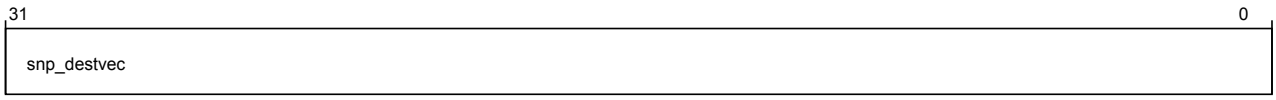


Figure 3-152 por_dn_por_dn_vmf6_cxra (low)

The following table shows the por_dn_vmf6_cxra lower register bit assignments.

Table 3-166 por_dn_por_dn_vmf6_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf6_ctrl.vmid	RW	64'b0

por_dn_vmf7_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCE0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

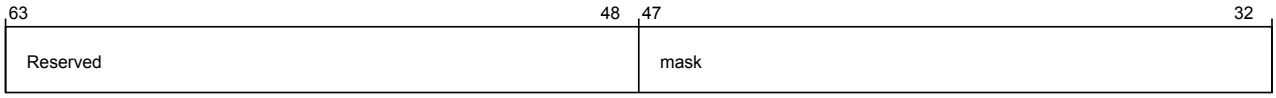


Figure 3-153 por_dn_por_dn_vmf7_ctrl (high)

The following table shows the por_dn_vmf7_ctrl higher register bit assignments.

Table 3-167 por_dn_por_dn_vmf7_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf7_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

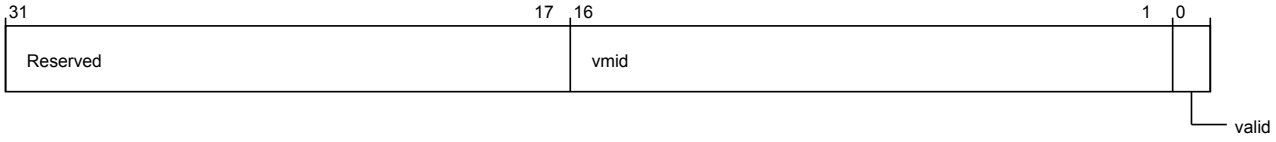


Figure 3-154 por_dn_por_dn_vmf7_ctrl (low)

The following table shows the por_dn_vmf7_ctrl lower register bit assignments.

Table 3-168 por_dn_por_dn_vmf7_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf7_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

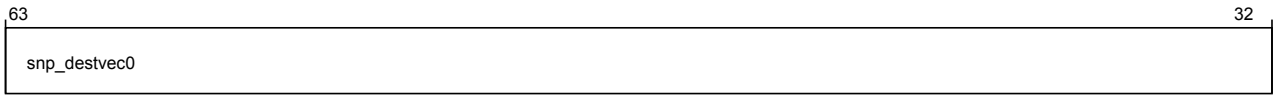


Figure 3-155 por_dn_por_dn_vmf7_rnf0 (high)

The following table shows the por_dn_vmf7_rnf0 higher register bit assignments.

Table 3-169 por_dn_por_dn_vmf7_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

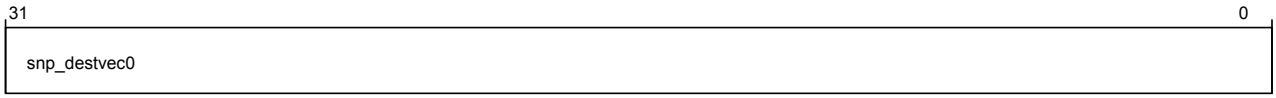


Figure 3-156 por_dn_por_dn_vmf7_rnf0 (low)

The following table shows the por_dn_vmf7_rnf0 lower register bit assignments.

Table 3-170 por_dn_por_dn_vmf7_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf7_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

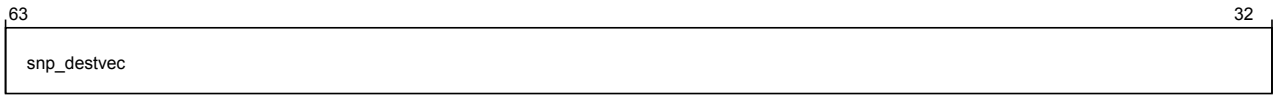


Figure 3-157 por_dn_por_dn_vmf7_rnd (high)

The following table shows the por_dn_vmf7_rnd higher register bit assignments.

Table 3-171 por_dn_por_dn_vmf7_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

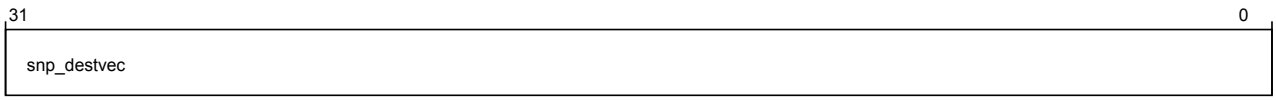


Figure 3-158 por_dn_por_dn_vmf7_rnd (low)

The following table shows the por_dn_vmf7_rnd lower register bit assignments.

Table 3-172 por_dn_por_dn_vmf7_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf7_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

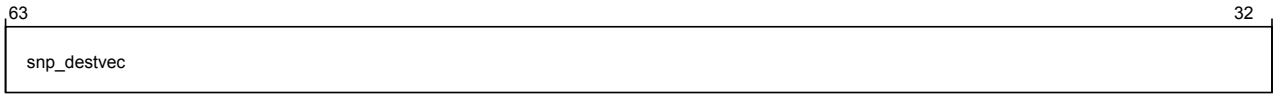


Figure 3-159 por_dn_por_dn_vmf7_cxra (high)

The following table shows the por_dn_vmf7_cxra higher register bit assignments.

Table 3-173 por_dn_por_dn_vmf7_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

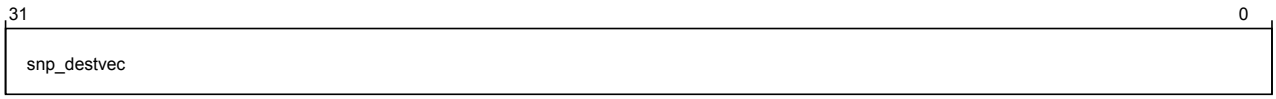


Figure 3-160 por_dn_por_dn_vmf7_cxra (low)

The following table shows the por_dn_vmf7_cxra lower register bit assignments.

Table 3-174 por_dn_por_dn_vmf7_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf7_ctrl.vmid	RW	64'b0

por_dn_vmf8_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD00

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

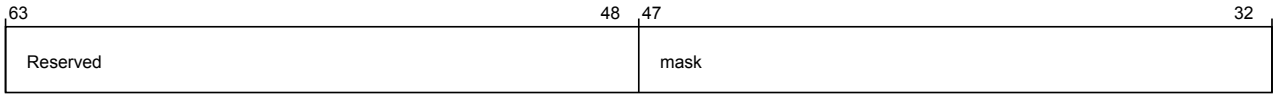


Figure 3-161 por_dn_por_dn_vmf8_ctrl (high)

The following table shows the por_dn_vmf8_ctrl higher register bit assignments.

Table 3-175 por_dn_por_dn_vmf8_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf8_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

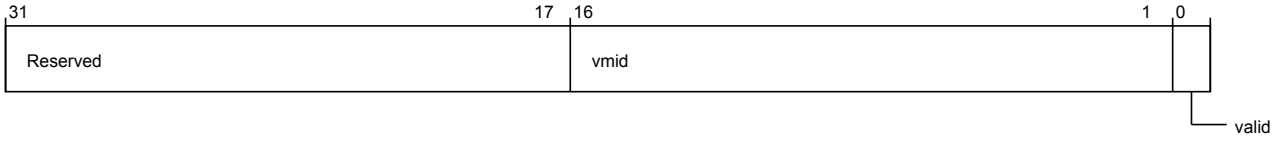


Figure 3-162 por_dn_por_dn_vmf8_ctrl (low)

The following table shows the por_dn_vmf8_ctrl lower register bit assignments.

Table 3-176 por_dn_por_dn_vmf8_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf8_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

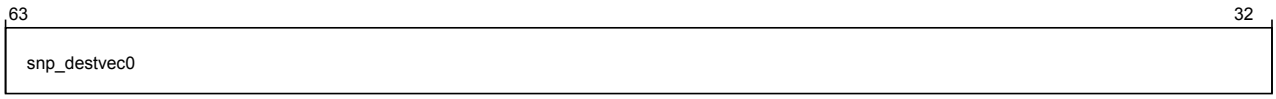


Figure 3-163 por_dn_por_dn_vmf8_rnf0 (high)

The following table shows the por_dn_vmf8_rnf0 higher register bit assignments.

Table 3-177 por_dn_por_dn_vmf8_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

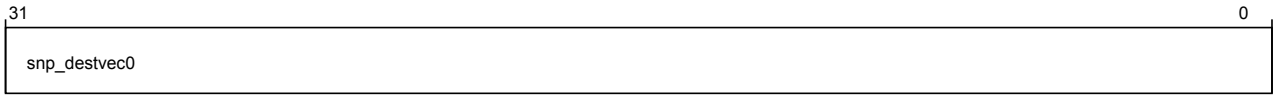


Figure 3-164 por_dn_por_dn_vmf8_rnf0 (low)

The following table shows the por_dn_vmf8_rnf0 lower register bit assignments.

Table 3-178 por_dn_por_dn_vmf8_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf8_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

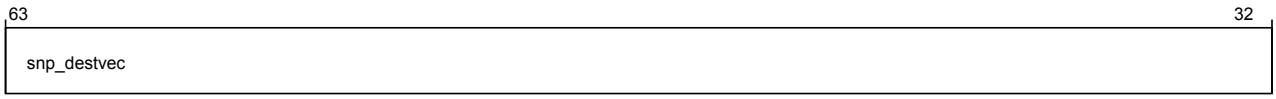


Figure 3-165 por_dn_por_dn_vmf8_rnd (high)

The following table shows the por_dn_vmf8_rnd higher register bit assignments.

Table 3-179 por_dn_por_dn_vmf8_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

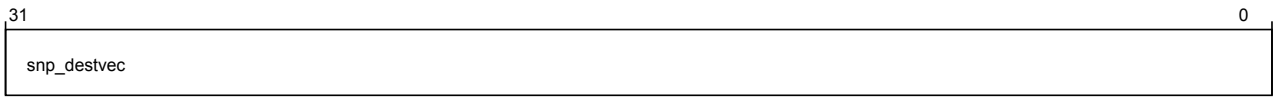


Figure 3-166 por_dn_por_dn_vmf8_rnd (low)

The following table shows the por_dn_vmf8_rnd lower register bit assignments.

Table 3-180 por_dn_por_dn_vmf8_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf8_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

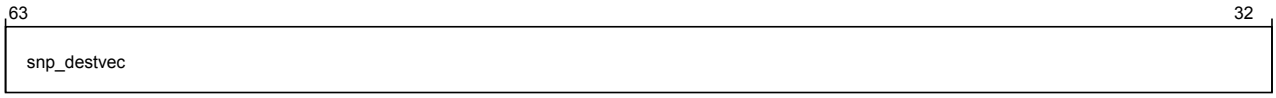


Figure 3-167 por_dn_por_dn_vmf8_cxra (high)

The following table shows the por_dn_vmf8_cxra higher register bit assignments.

Table 3-181 por_dn_por_dn_vmf8_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

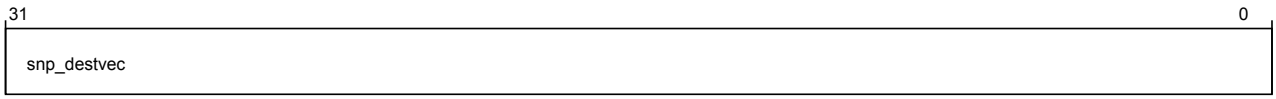


Figure 3-168 por_dn_por_dn_vmf8_cxra (low)

The following table shows the por_dn_vmf8_cxra lower register bit assignments.

Table 3-182 por_dn_por_dn_vmf8_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf8_ctrl.vmid	RW	64'b0

por_dn_vmf9_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD20

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

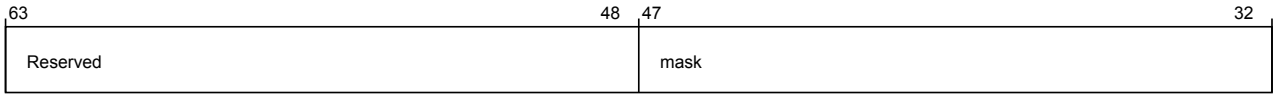


Figure 3-169 por_dn_por_dn_vmf9_ctrl (high)

The following table shows the por_dn_vmf9_ctrl higher register bit assignments.

Table 3-183 por_dn_por_dn_vmf9_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf9_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

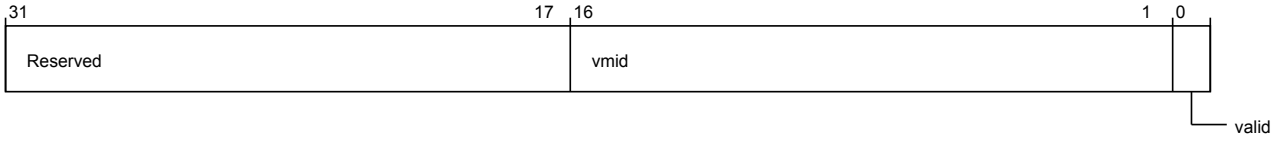


Figure 3-170 por_dn_por_dn_vmf9_ctrl (low)

The following table shows the por_dn_vmf9_ctrl lower register bit assignments.

Table 3-184 por_dn_por_dn_vmf9_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf9_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

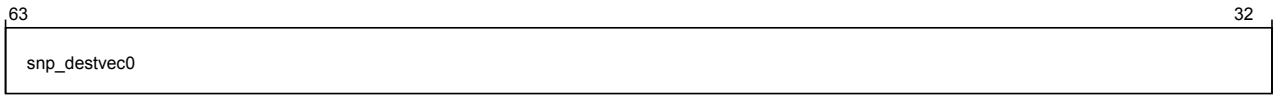


Figure 3-171 por_dn_por_dn_vmf9_rnf0 (high)

The following table shows the por_dn_vmf9_rnf0 higher register bit assignments.

Table 3-185 por_dn_por_dn_vmf9_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

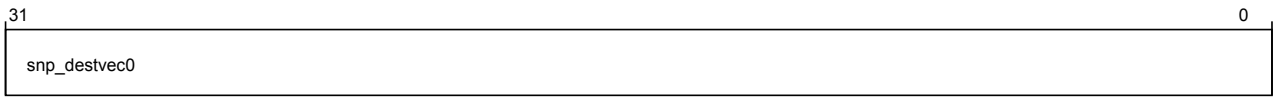


Figure 3-172 por_dn_por_dn_vmf9_rnf0 (low)

The following table shows the por_dn_vmf9_rnf0 lower register bit assignments.

Table 3-186 por_dn_por_dn_vmf9_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf9_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

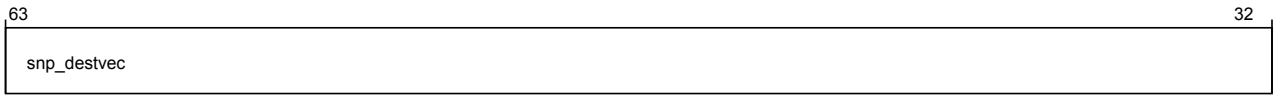


Figure 3-173 por_dn_por_dn_vmf9_rnd (high)

The following table shows the por_dn_vmf9_rnd higher register bit assignments.

Table 3-187 por_dn_por_dn_vmf9_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

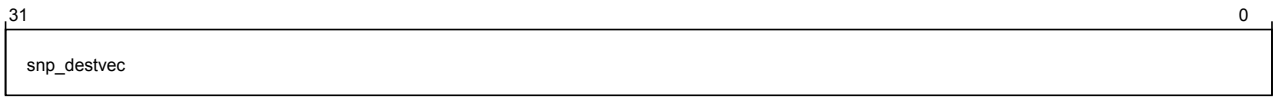


Figure 3-174 por_dn_por_dn_vmf9_rnd (low)

The following table shows the por_dn_vmf9_rnd lower register bit assignments.

Table 3-188 por_dn_por_dn_vmf9_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf9_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

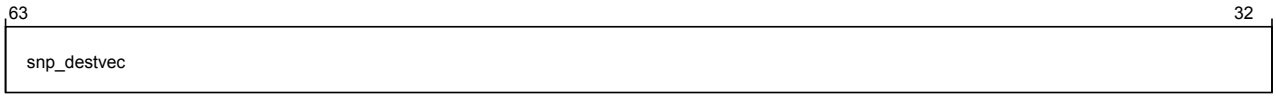


Figure 3-175 por_dn_por_dn_vmf9_cxra (high)

The following table shows the por_dn_vmf9_cxra higher register bit assignments.

Table 3-189 por_dn_por_dn_vmf9_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

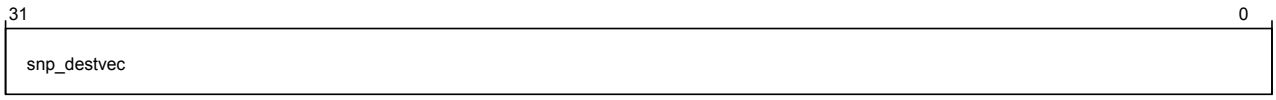


Figure 3-176 por_dn_por_dn_vmf9_cxra (low)

The following table shows the por_dn_vmf9_cxra lower register bit assignments.

Table 3-190 por_dn_por_dn_vmf9_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf9_ctrl.vmid	RW	64'b0

por_dn_vmf10_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD40

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

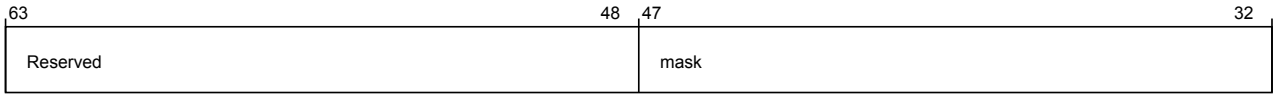


Figure 3-177 por_dn_por_dn_vmf10_ctrl (high)

The following table shows the por_dn_vmf10_ctrl higher register bit assignments.

Table 3-191 por_dn_por_dn_vmf10_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf10_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

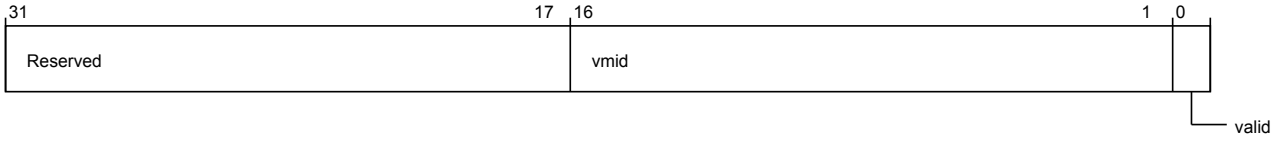


Figure 3-178 por_dn_por_dn_vmf10_ctrl (low)

The following table shows the por_dn_vmf10_ctrl lower register bit assignments.

Table 3-192 por_dn_por_dn_vmf10_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf10_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

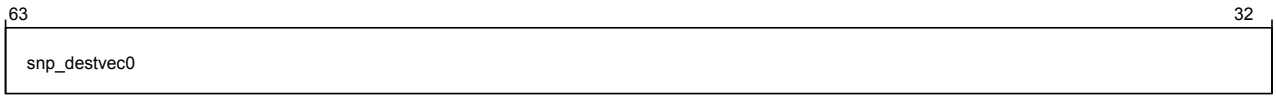


Figure 3-179 por_dn_por_dn_vmf10_rnf0 (high)

The following table shows the por_dn_vmf10_rnf0 higher register bit assignments.

Table 3-193 por_dn_por_dn_vmf10_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

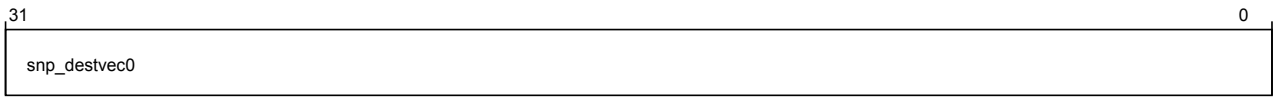


Figure 3-180 por_dn_por_dn_vmf10_rnf0 (low)

The following table shows the por_dn_vmf10_rnf0 lower register bit assignments.

Table 3-194 por_dn_por_dn_vmf10_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf10_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

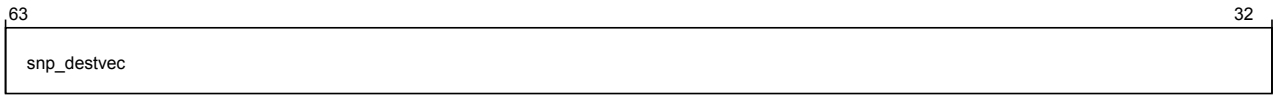


Figure 3-181 por_dn_por_dn_vmf10_rnd (high)

The following table shows the por_dn_vmf10_rnd higher register bit assignments.

Table 3-195 por_dn_por_dn_vmf10_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

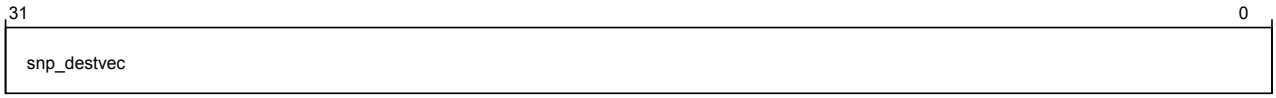


Figure 3-182 por_dn_por_dn_vmf10_rnd (low)

The following table shows the por_dn_vmf10_rnd lower register bit assignments.

Table 3-196 por_dn_por_dn_vmf10_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf10_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

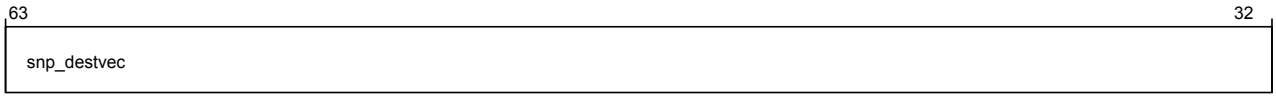


Figure 3-183 por_dn_por_dn_vmf10_cxra (high)

The following table shows the por_dn_vmf10_cxra higher register bit assignments.

Table 3-197 por_dn_por_dn_vmf10_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

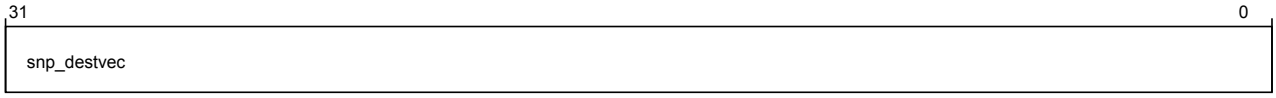


Figure 3-184 por_dn_por_dn_vmf10_cxra (low)

The following table shows the por_dn_vmf10_cxra lower register bit assignments.

Table 3-198 por_dn_por_dn_vmf10_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf10_ctrl.vmid	RW	64'b0

por_dn_vmf11_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD60

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

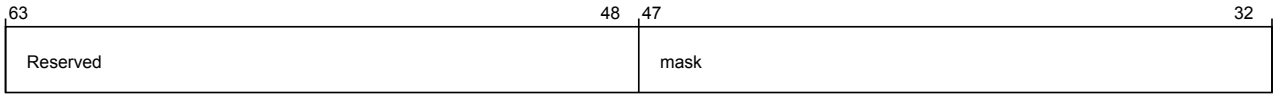


Figure 3-185 por_dn_por_dn_vmf11_ctrl (high)

The following table shows the por_dn_vmf11_ctrl higher register bit assignments.

Table 3-199 por_dn_por_dn_vmf11_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf11_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

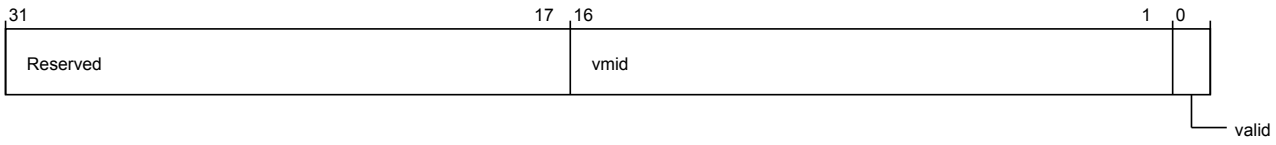


Figure 3-186 por_dn_por_dn_vmf11_ctrl (low)

The following table shows the por_dn_vmf11_ctrl lower register bit assignments.

Table 3-200 por_dn_por_dn_vmf11_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf11_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

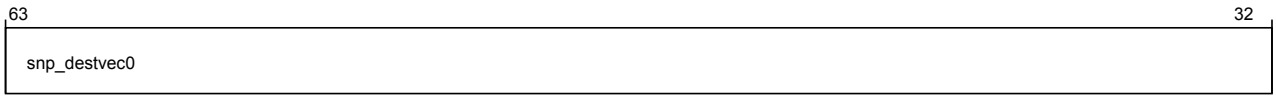


Figure 3-187 por_dn_por_dn_vmf11_rnf0 (high)

The following table shows the por_dn_vmf11_rnf0 higher register bit assignments.

Table 3-201 por_dn_por_dn_vmf11_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

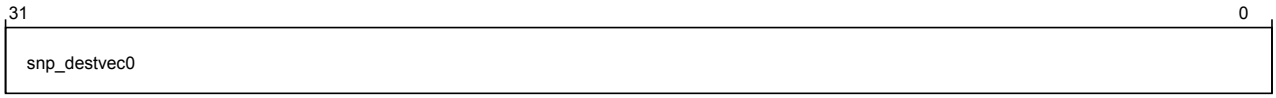


Figure 3-188 por_dn_por_dn_vmf11_rnf0 (low)

The following table shows the por_dn_vmf11_rnf0 lower register bit assignments.

Table 3-202 por_dn_por_dn_vmf11_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

por_dn_vmf11_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

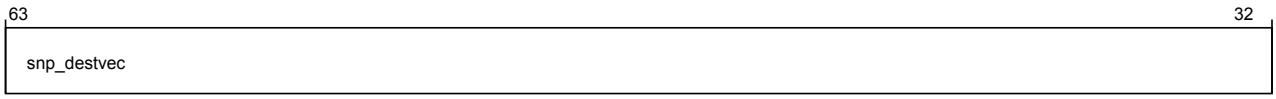


Figure 3-189 por_dn_por_dn_vmf11_rnd (high)

The following table shows the por_dn_vmf11_rnd higher register bit assignments.

Table 3-203 por_dn_por_dn_vmf11_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

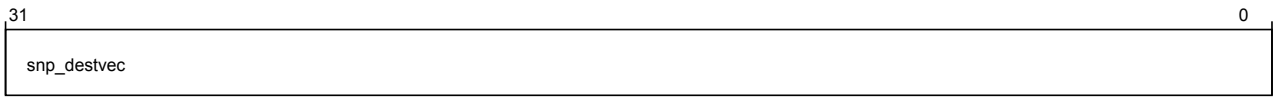


Figure 3-190 por_dn_por_dn_vmf11_rnd (low)

The following table shows the por_dn_vmf11_rnd lower register bit assignments.

Table 3-204 por_dn_por_dn_vmf11_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

por_dn_vmf11_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

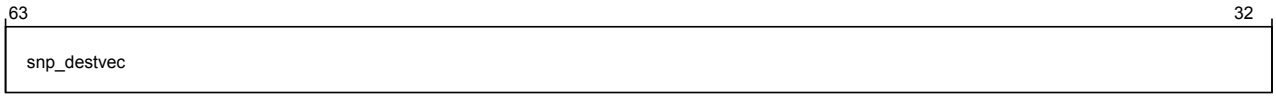


Figure 3-191 por_dn_por_dn_vmf11_cxra (high)

The following table shows the por_dn_vmf11_cxra higher register bit assignments.

Table 3-205 por_dn_por_dn_vmf11_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

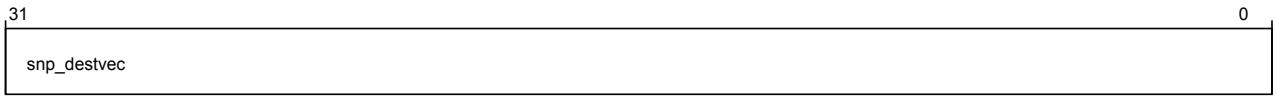


Figure 3-192 por_dn_por_dn_vmf11_cxra (low)

The following table shows the por_dn_vmf11_cxra lower register bit assignments.

Table 3-206 por_dn_por_dn_vmf11_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf11_ctrl.vmid	RW	64'b0

por_dn_vmf12_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD80

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

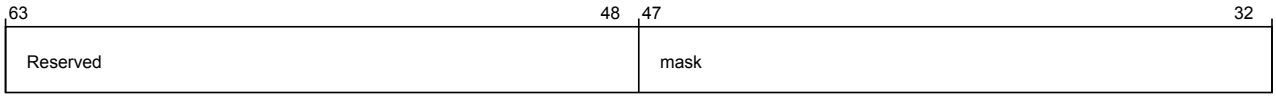


Figure 3-193 por_dn_por_dn_vmf12_ctrl (high)

The following table shows the por_dn_vmf12_ctrl higher register bit assignments.

Table 3-207 por_dn_por_dn_vmf12_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf12_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

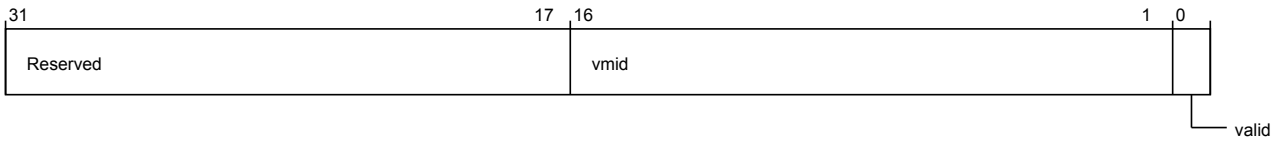


Figure 3-194 por_dn_por_dn_vmf12_ctrl (low)

The following table shows the por_dn_vmf12_ctrl lower register bit assignments.

Table 3-208 por_dn_por_dn_vmf12_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf12_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

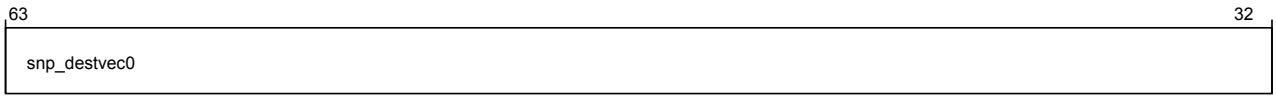


Figure 3-195 por_dn_por_dn_vmf12_rnf0 (high)

The following table shows the por_dn_vmf12_rnf0 higher register bit assignments.

Table 3-209 por_dn_por_dn_vmf12_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

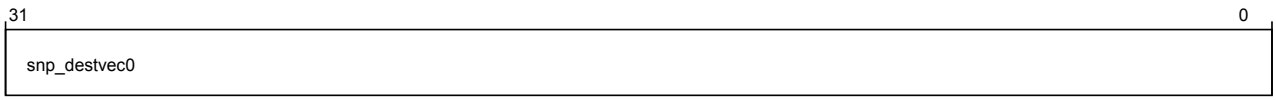


Figure 3-196 por_dn_por_dn_vmf12_rnf0 (low)

The following table shows the por_dn_vmf12_rnf0 lower register bit assignments.

Table 3-210 por_dn_por_dn_vmf12_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

por_dn_vmf12_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

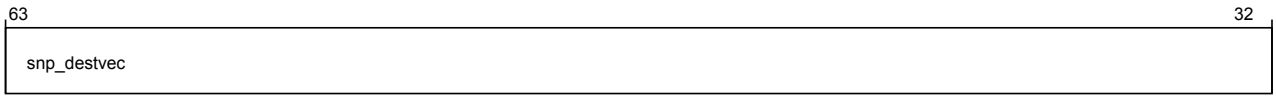


Figure 3-197 por_dn_por_dn_vmf12_rnd (high)

The following table shows the por_dn_vmf12_rnd higher register bit assignments.

Table 3-211 por_dn_por_dn_vmf12_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

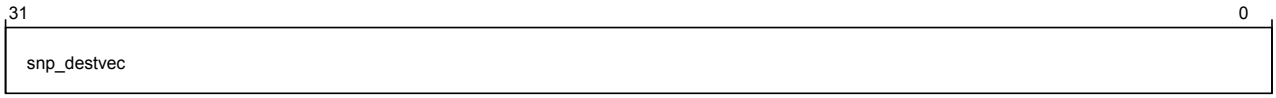


Figure 3-198 por_dn_por_dn_vmf12_rnd (low)

The following table shows the por_dn_vmf12_rnd lower register bit assignments.

Table 3-212 por_dn_por_dn_vmf12_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

por_dn_vmf12_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

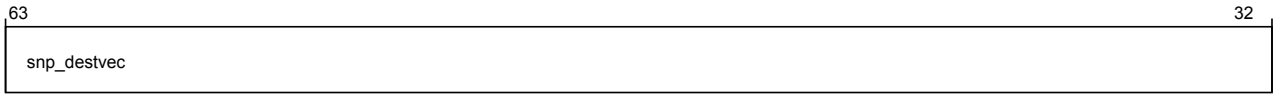


Figure 3-199 por_dn_por_dn_vmf12_cxra (high)

The following table shows the por_dn_vmf12_cxra higher register bit assignments.

Table 3-213 por_dn_por_dn_vmf12_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

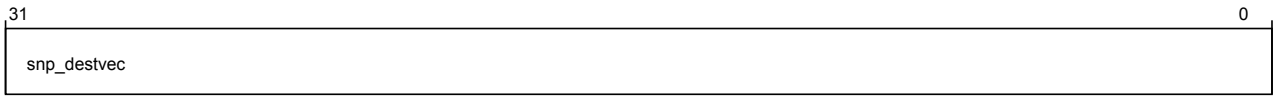


Figure 3-200 por_dn_por_dn_vmf12_cxra (low)

The following table shows the por_dn_vmf12_cxra lower register bit assignments.

Table 3-214 por_dn_por_dn_vmf12_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf12_ctrl.vmid	RW	64'b0

por_dn_vmf13_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDA0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

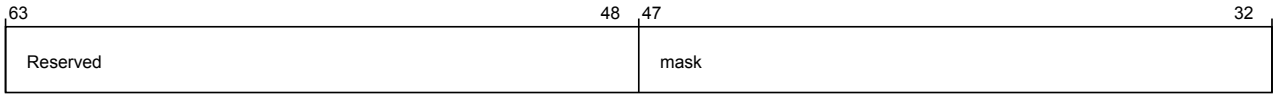


Figure 3-201 por_dn_por_dn_vmf13_ctrl (high)

The following table shows the por_dn_vmf13_ctrl higher register bit assignments.

Table 3-215 por_dn_por_dn_vmf13_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf13_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

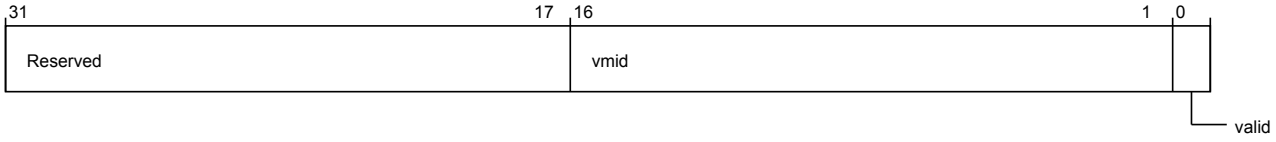


Figure 3-202 por_dn_por_dn_vmf13_ctrl (low)

The following table shows the por_dn_vmf13_ctrl lower register bit assignments.

Table 3-216 por_dn_por_dn_vmf13_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf13_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

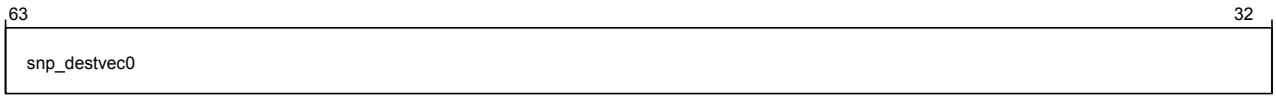


Figure 3-203 por_dn_por_dn_vmf13_rnf0 (high)

The following table shows the por_dn_vmf13_rnf0 higher register bit assignments.

Table 3-217 por_dn_por_dn_vmf13_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

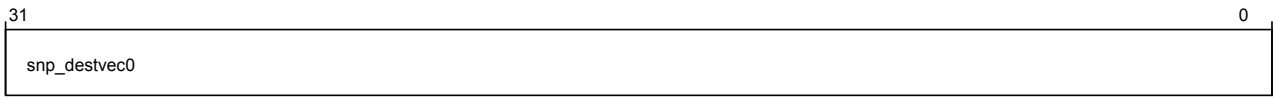


Figure 3-204 por_dn_por_dn_vmf13_rnf0 (low)

The following table shows the por_dn_vmf13_rnf0 lower register bit assignments.

Table 3-218 por_dn_por_dn_vmf13_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

por_dn_vmf13_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

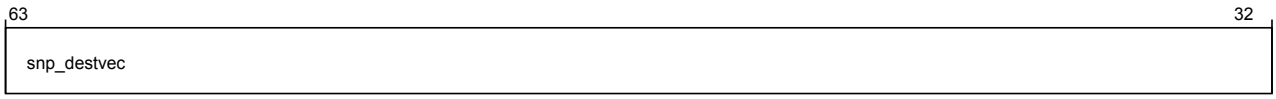


Figure 3-205 por_dn_por_dn_vmf13_rnd (high)

The following table shows the por_dn_vmf13_rnd higher register bit assignments.

Table 3-219 por_dn_por_dn_vmf13_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

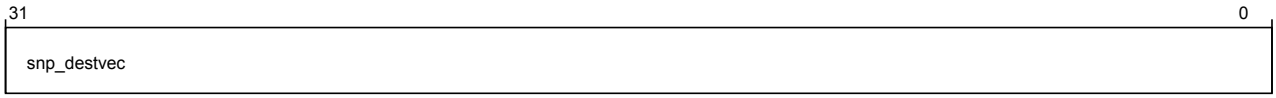


Figure 3-206 por_dn_por_dn_vmf13_rnd (low)

The following table shows the por_dn_vmf13_rnd lower register bit assignments.

Table 3-220 por_dn_por_dn_vmf13_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

por_dn_vmf13_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

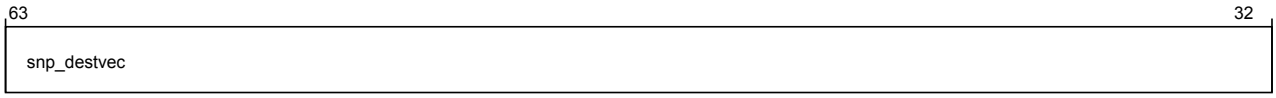


Figure 3-207 por_dn_por_dn_vmf13_cxra (high)

The following table shows the por_dn_vmf13_cxra higher register bit assignments.

Table 3-221 por_dn_por_dn_vmf13_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

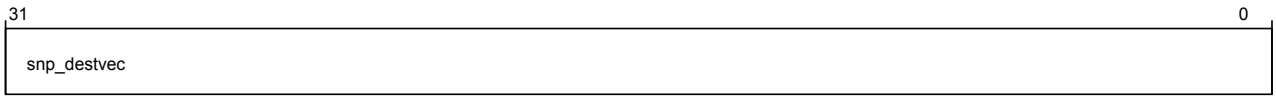


Figure 3-208 por_dn_por_dn_vmf13_cxra (low)

The following table shows the por_dn_vmf13_cxra lower register bit assignments.

Table 3-222 por_dn_por_dn_vmf13_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf13_ctrl.vmid	RW	64'b0

por_dn_vmf14_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDC0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

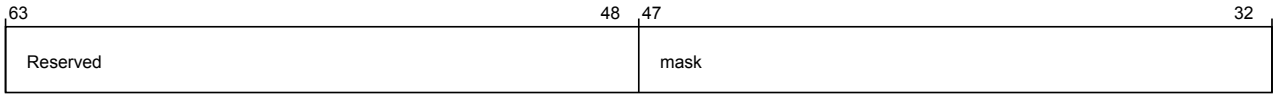


Figure 3-209 por_dn_por_dn_vmf14_ctrl (high)

The following table shows the por_dn_vmf14_ctrl higher register bit assignments.

Table 3-223 por_dn_por_dn_vmf14_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf14_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

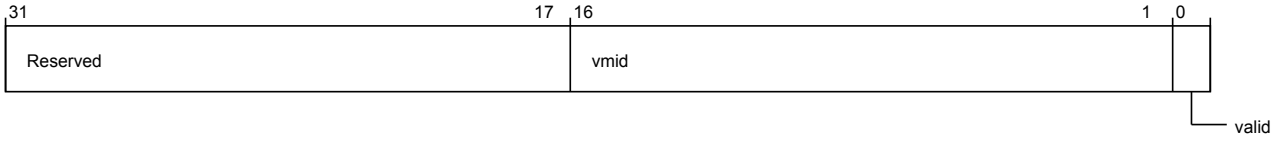


Figure 3-210 por_dn_por_dn_vmf14_ctrl (low)

The following table shows the por_dn_vmf14_ctrl lower register bit assignments.

Table 3-224 por_dn_por_dn_vmf14_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf14_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

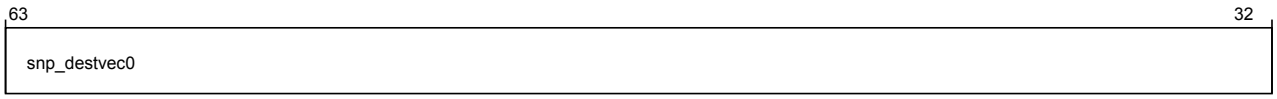


Figure 3-211 por_dn_por_dn_vmf14_rnf0 (high)

The following table shows the por_dn_vmf14_rnf0 higher register bit assignments.

Table 3-225 por_dn_por_dn_vmf14_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

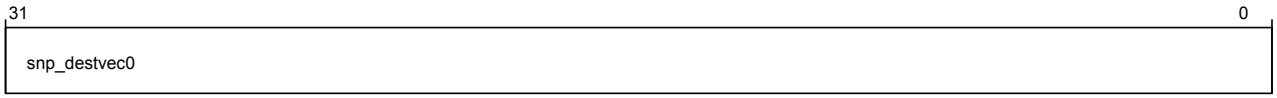


Figure 3-212 por_dn_por_dn_vmf14_rnf0 (low)

The following table shows the por_dn_vmf14_rnf0 lower register bit assignments.

Table 3-226 por_dn_por_dn_vmf14_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf14_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

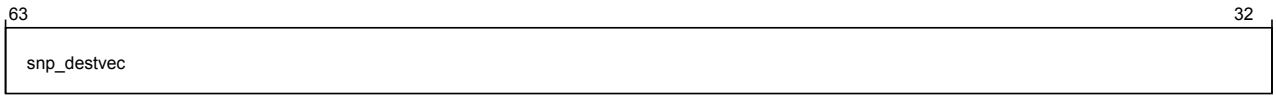


Figure 3-213 por_dn_por_dn_vmf14_rnd (high)

The following table shows the por_dn_vmf14_rnd higher register bit assignments.

Table 3-227 por_dn_por_dn_vmf14_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

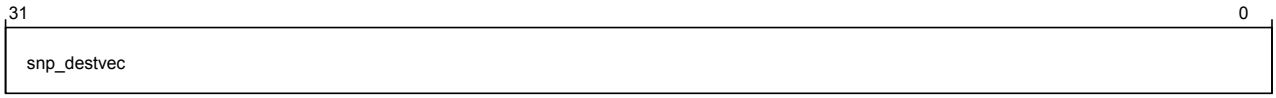


Figure 3-214 por_dn_por_dn_vmf14_rnd (low)

The following table shows the por_dn_vmf14_rnd lower register bit assignments.

Table 3-228 por_dn_por_dn_vmf14_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf14_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

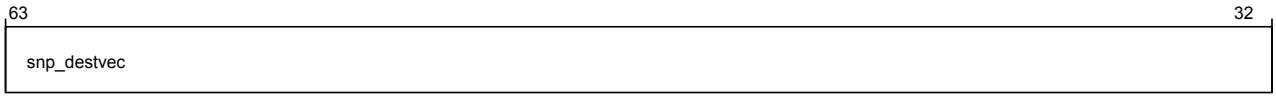


Figure 3-215 por_dn_por_dn_vmf14_cxra (high)

The following table shows the por_dn_vmf14_cxra higher register bit assignments.

Table 3-229 por_dn_por_dn_vmf14_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

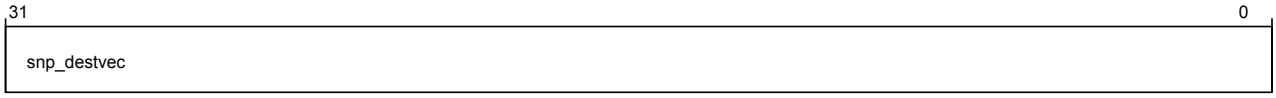


Figure 3-216 por_dn_por_dn_vmf14_cxra (low)

The following table shows the por_dn_vmf14_cxra lower register bit assignments.

Table 3-230 por_dn_por_dn_vmf14_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf14_ctrl.vmid	RW	64'b0

por_dn_vmf15_ctrl

Functions as the control register for VMID-based DVM snoop filtering. NOTE: This register has no effect when por_dn_aux_ctl.disable_vmf is set to 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDE0

Register reset 64'b1111111111111111000000000000000000

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

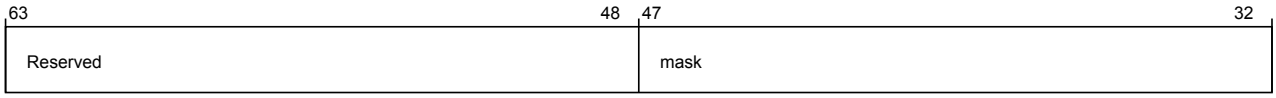


Figure 3-217 por_dn_por_dn_vmf15_ctrl (high)

The following table shows the por_dn_vmf15_ctrl higher register bit assignments.

Table 3-231 por_dn_por_dn_vmf15_ctrl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	mask	VMID mask; enables mapping of multiple VMID values to a single register NOTE: Logically, the AND operator is performed on the mask and por_dn_vmf15_ctrl.vmid. Then, the AND operator is performed on the mask and the incoming request's VMID. The two results are then compared, and filtering is applied to the incoming request if the masked VMIDs match.	RW	16'hffff

The following image shows the lower register bit assignments.

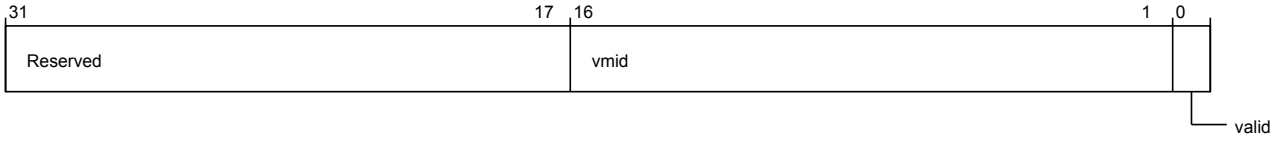


Figure 3-218 por_dn_por_dn_vmf15_ctrl (low)

The following table shows the por_dn_vmf15_ctrl lower register bit assignments.

Table 3-232 por_dn_por_dn_vmf15_ctrl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16:1	vmid	VMID value NOTE: The incoming request's VMID is only compared with this VMID value if the request's VMID valid bit is set. If the request's VMID is valid and the two VMIDs match, filtering is applied to the incoming request.	RW	16'h0000
0	valid	Register valid 1'b1: Register is enabled 1'b0: Register is not enabled	RW	1'b0

por_dn_vmf15_rnf0

Contains the logical RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

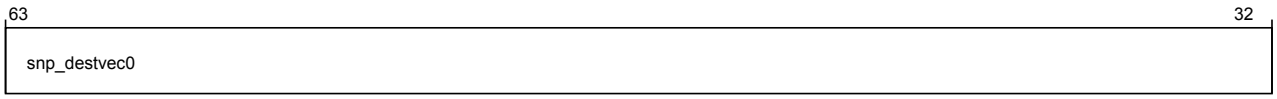


Figure 3-219 por_dn_por_dn_vmf15_rnf0 (high)

The following table shows the por_dn_vmf15_rnf0 higher register bit assignments.

Table 3-233 por_dn_por_dn_vmf15_rnf0 (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

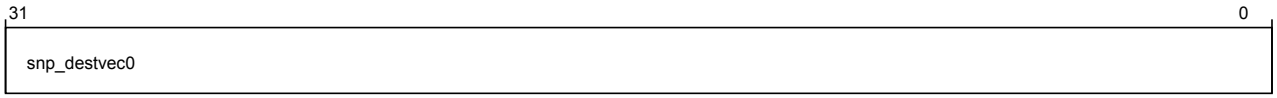


Figure 3-220 por_dn_por_dn_vmf15_rnf0 (low)

The following table shows the por_dn_vmf15_rnf0 lower register bit assignments.

Table 3-234 por_dn_por_dn_vmf15_rnf0 (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec0	RN-F bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

por_dn_vmf15_rnd

Contains the logical RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

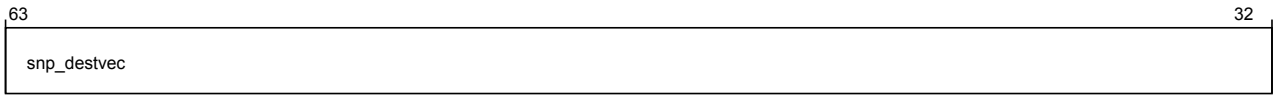


Figure 3-221 por_dn_por_dn_vmf15_rnd (high)

The following table shows the por_dn_vmf15_rnd higher register bit assignments.

Table 3-235 por_dn_por_dn_vmf15_rnd (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

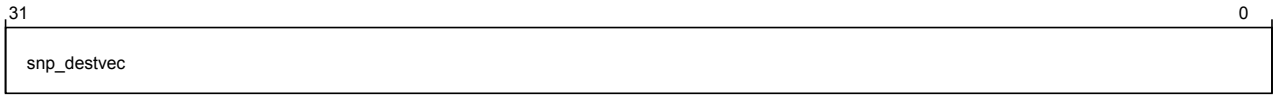


Figure 3-222 por_dn_por_dn_vmf15_rnd (low)

The following table shows the por_dn_vmf15_rnd lower register bit assignments.

Table 3-236 por_dn_por_dn_vmf15_rnd (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	RN-D bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

por_dn_vmf15_cxra

Contains the logical CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid. Used for VMID-based DVM snoop filtering. NOTE: Not applicable in a single-chip CMN-600 system. Does not have any effect.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_dn_secure_register_groups_override.vmf

The following image shows the higher register bit assignments.

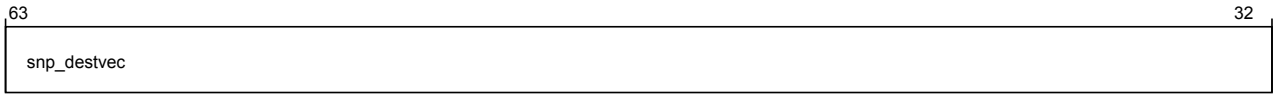


Figure 3-223 por_dn_por_dn_vmf15_cxra (high)

The following table shows the por_dn_vmf15_cxra higher register bit assignments.

Table 3-237 por_dn_por_dn_vmf15_cxra (high)

Bits	Field name	Description	Type	Reset
63:32	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

The following image shows the lower register bit assignments.

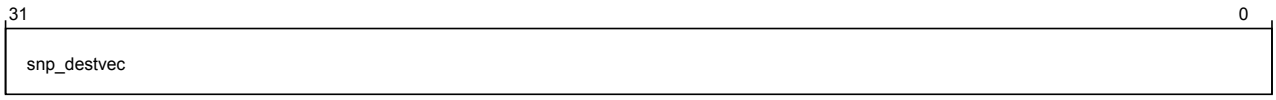


Figure 3-224 por_dn_por_dn_vmf15_cxra (low)

The following table shows the por_dn_vmf15_cxra lower register bit assignments.

Table 3-238 por_dn_por_dn_vmf15_cxra (low)

Bits	Field name	Description	Type	Reset
31:0	snp_destvec	CXRA bit vector 63:0 corresponding to por_dn_vmf15_ctrl.vmid	RW	64'b0

por_dn_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

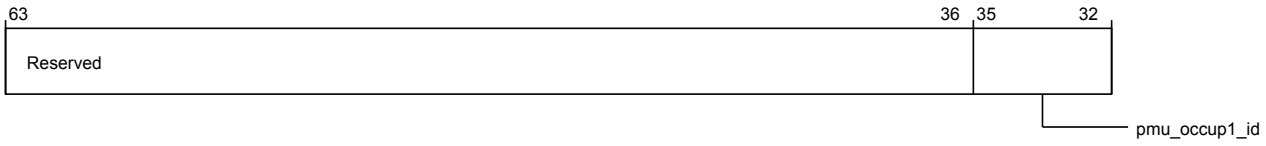


Figure 3-225 por_dn_por_dn_pmu_event_sel (high)

The following table shows the por_dn_pmu_event_sel higher register bit assignments.

Table 3-239 por_dn_por_dn_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	PMU occupancy event selector ID 4'b0000: All 4'b0001: DVM ops 4'b0010: DVM syncs	RW	4'b0

The following image shows the lower register bit assignments.

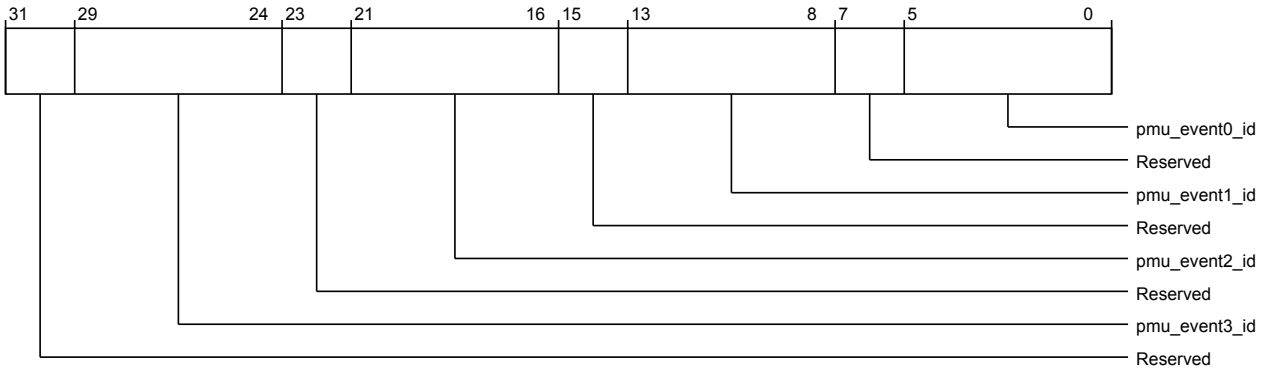


Figure 3-226 por_dn_por_dn_pmu_event_sel (low)

The following table shows the por_dn_pmu_event_sel lower register bit assignments.

Table 3-240 por_dn_por_dn_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 3-240 por_dn_por_dn_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	PMU Event 0 ID 6'h00: No event 6'h01: Number of TLBI DVM op requests 6'h02: Number of BPI DVM op requests 6'h03: Number of PICI DVM op requests 6'h04: Number of VICI DVM op requests 6'h05: Number of DVM sync requests 6'h06: Number of DVM op requests that were filtered using VMID filtering 6'h07: Number of DVM op requests to RNDs, BPI or PICI/VICI, that were filtered 6'h08: Number of retried REQ 6'h09: Number of SNPs sent to RNs 6'h0a: Number of SNPs stalled to RNs due to lack of Crds 6'h0b: DVM tracker full counter 6'h0c: DVM tracker occupancy counter	RW	5'b0

3.3.3 Debug and trace register descriptions

This section lists the debug and trace registers.

por_dt_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

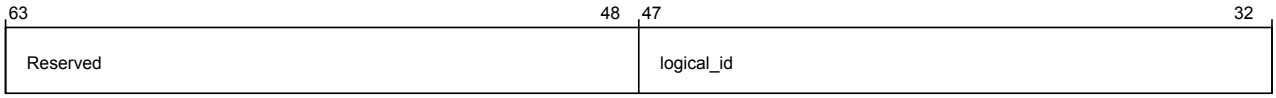


Figure 3-227 por_dt_por_dt_node_info (high)

The following table shows the por_dt_node_info higher register bit assignments.

Table 3-241 por_dt_por_dt_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

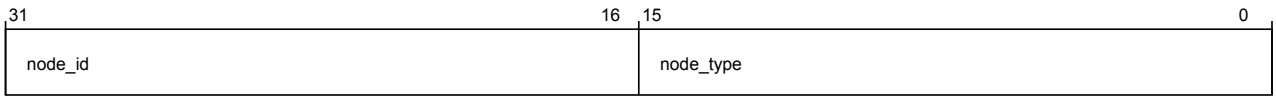


Figure 3-228 por_dt_por_dt_node_info (low)

The following table shows the por_dt_node_info lower register bit assignments.

Table 3-242 por_dt_por_dt_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h3

por_dt_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

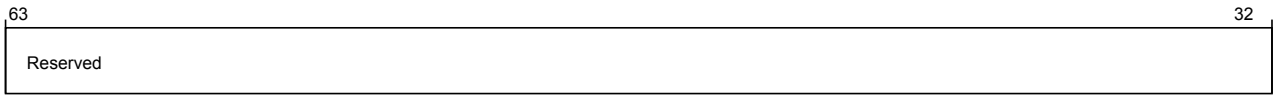


Figure 3-229 por_dt_por_dt_child_info (high)

The following table shows the por_dt_child_info higher register bit assignments.

Table 3-243 por_dt_por_dt_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

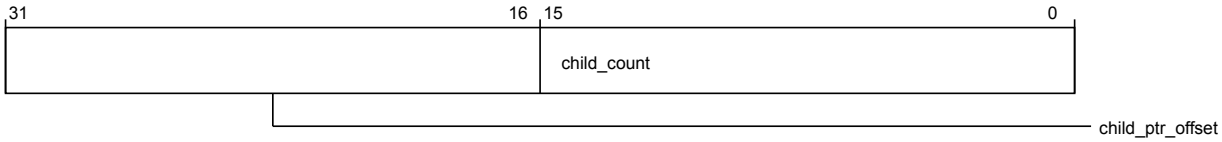


Figure 3-230 por_dt_por_dt_child_info (low)

The following table shows the por_dt_child_info lower register bit assignments.

Table 3-244 por_dt_por_dt_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0000
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_dt_secure_access

Functions as the secure access control register.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

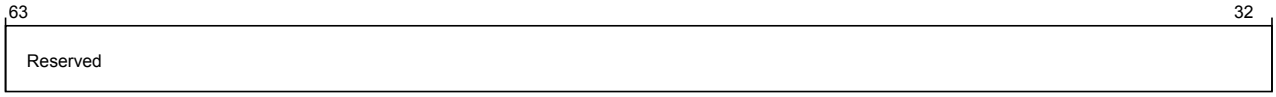


Figure 3-231 por_dt_por_dt_secure_access (high)

The following table shows the por_dt_secure_access higher register bit assignments.

Table 3-245 por_dt_por_dt_secure_access (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

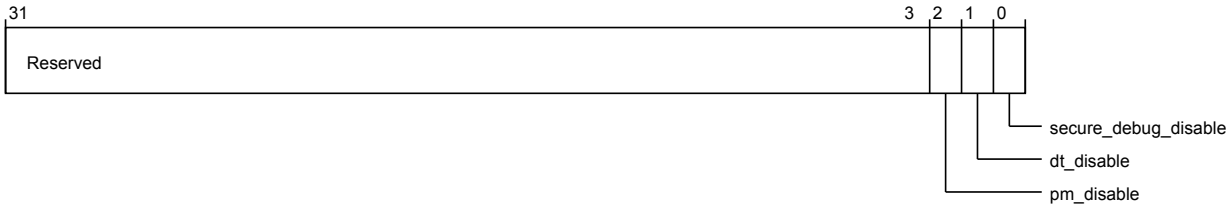


Figure 3-232 por_dt_por_dt_secure_access (low)

The following table shows the por_dt_secure_access lower register bit assignments.

Table 3-246 por_dt_por_dt_secure_access (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	pm_disable	PMU disable 1'b0: PMU function is not affected 1'b1: PMU function is disabled.	RW	1'b0
1	dt_disable	Debug disable 1'b0: DT function is not affected 1'b1: DT function is disabled.	RW	1'b0
0	secure_debug_disable	Secure debug disable 1'b0: Secure events are monitored by the PMU 1'b1: Secure events are only monitored by the PMU if SPNIDEN is set to 1	RW	1'b0

por_dt_dtc_ctl

Functions as the debug trace control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA00
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

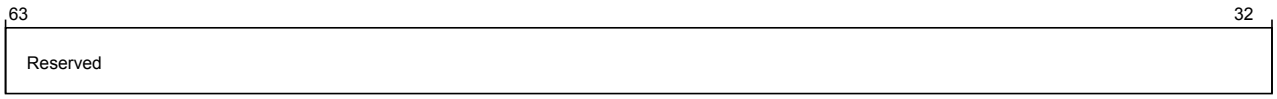


Figure 3-233 por_dt_por_dt_dtc_ctl (high)

The following table shows the por_dt_dtc_ctl higher register bit assignments.

Table 3-247 por_dt_por_dt_dtc_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

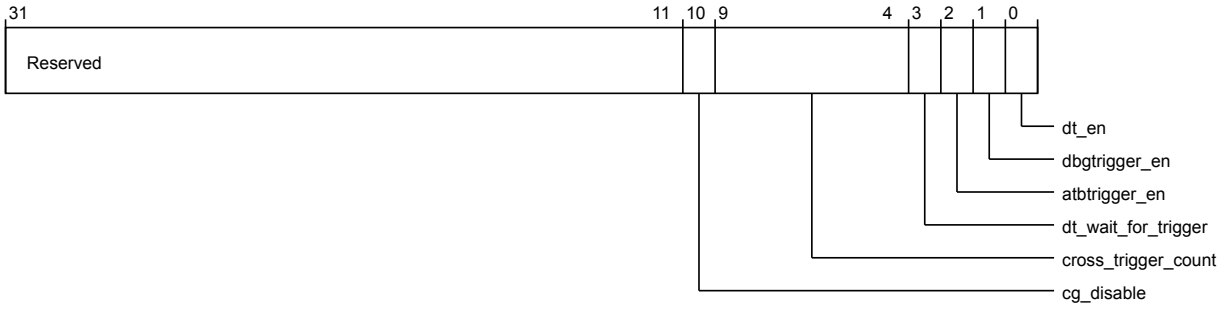


Figure 3-234 por_dt_por_dt_dtc_ctl (low)

The following table shows the por_dt_dtc_ctl lower register bit assignments.

Table 3-248 por_dt_por_dt_dtc_ctl (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	cg_disable	Disables DT architectural clock gates	RW	1'b0
9:4	cross_trigger_count	Number of cross triggers received before trace enable NOTE: Only applicable if dt_wait_for_trigger is set to 1.	RW	6'b0

Table 3-248 por_dt_por_dt_dtc_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
3	dt_wait_for_trigger	Enables waiting for cross trigger before trace enable	RW	1'b0
2	atbtrigger_en	ATB trigger enable	RW	1'b0
1	dbgtrigger_en	DBGWATCHTRIG enable	RW	1'b0
0	dt_en	Enables debug, trace, and PMU features	RW	1'b0

por_dt_trigger_status

Provides the trigger status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'hA10
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

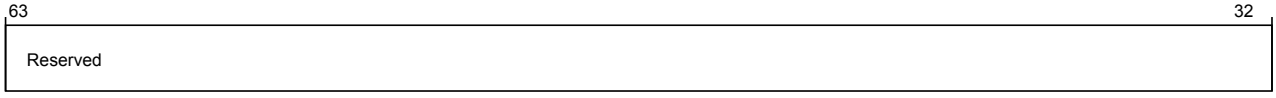


Figure 3-235 por_dt_por_dt_trigger_status (high)

The following table shows the por_dt_trigger_status higher register bit assignments.

Table 3-249 por_dt_por_dt_trigger_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

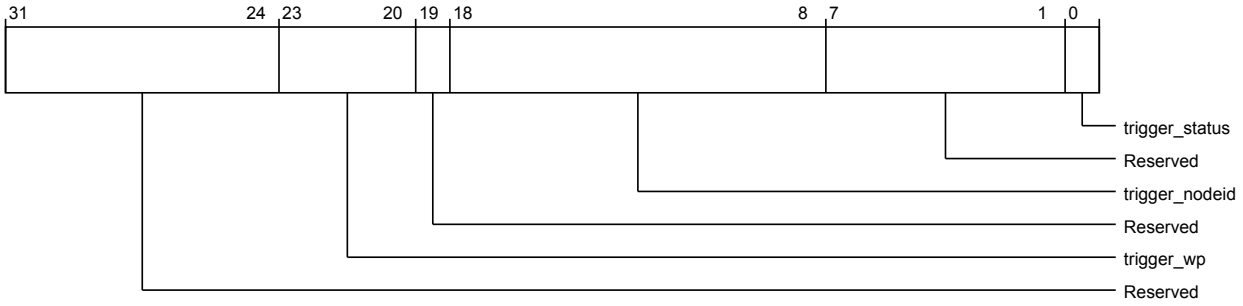


Figure 3-236 por_dt_por_dt_trigger_status (low)

The following table shows the por_dt_trigger_status lower register bit assignments.

Table 3-250 por_dt_por_dt_trigger_status (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	trigger_wp	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by watchpoint	RO	1'h0
19	Reserved	Reserved	RO	-
18:8	trigger_nodeid	DBGWATCHTRIGREQ assertion and/or ATB trigger are caused by node ID	RO	11'h0
7:1	Reserved	Reserved	RO	-
0	trigger_status	Indicates DBGWATCHTRIGREQ assertion and/or ATB trigger	RO	1'h0

por_dt_trigger_status_clr

Clears the trigger status.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'hA20
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

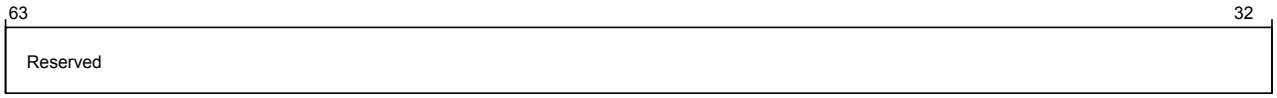


Figure 3-237 por_dt_por_dt_trigger_status_clr (high)

The following table shows the por_dt_trigger_status_clr higher register bit assignments.

Table 3-251 por_dt_por_dt_trigger_status_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

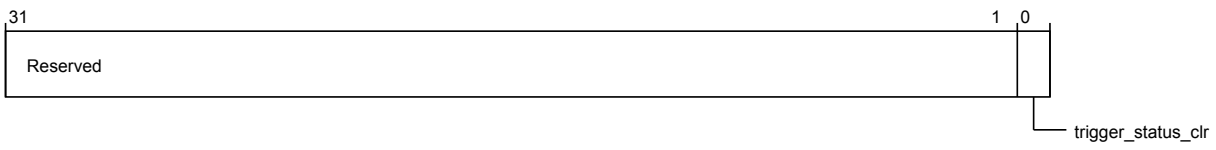


Figure 3-238 por_dt_por_dt_trigger_status_clr (low)

The following table shows the por_dt_trigger_status_clr lower register bit assignments.

Table 3-252 por_dt_por_dt_trigger_status_clr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	trigger_status_clr	Write a 1 to clear por_dt_trigger_status.trigger_status	WO	1'b0

por_dt_trace_control

Functions as the trace control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA30
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

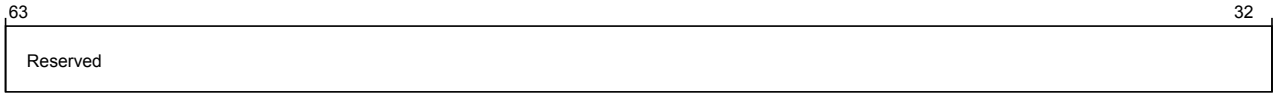


Figure 3-239 por_dt_por_dt_trace_control (high)

The following table shows the por_dt_trace_control higher register bit assignments.

Table 3-253 por_dt_por_dt_trace_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

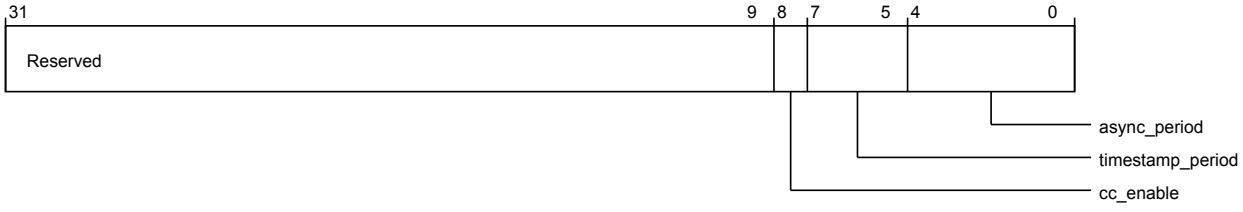


Figure 3-240 por_dt_por_dt_trace_control (low)

The following table shows the por_dt_trace_control lower register bit assignments.

Table 3-254 por_dt_por_dt_trace_control (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	cc_enable	Cycle count enable	RW	1'b0
7:5	timestamp_period	Time stamp packet insertion period 3'b000: Time stamp disabled 3'b011: Time stamp every 8K clock cycles 3'b100: Time stamp every 16K clock cycles 3'b101: Time stamp every 32K clock cycles 3'b110: Time stamp every 64K clock cycles	RW	3'b0
4:0	async_period	Alignment sync packet insertion period 5'h00: Alignment sync disabled 5'h08: Alignment sync inserted after 256B of trace 5'h09: Alignment sync inserted after 512B of trace 5'h14: Alignment sync inserted after 1048576B of trace NOTE: All other values are reserved.	RW	5'b0

por_dt_traceid

Contains the ATB ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA48
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

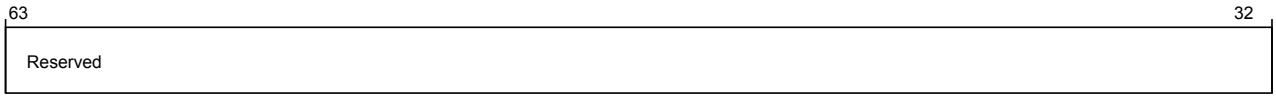


Figure 3-241 por_dt_por_dt_traceid (high)

The following table shows the por_dt_traceid higher register bit assignments.

Table 3-255 por_dt_por_dt_traceid (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

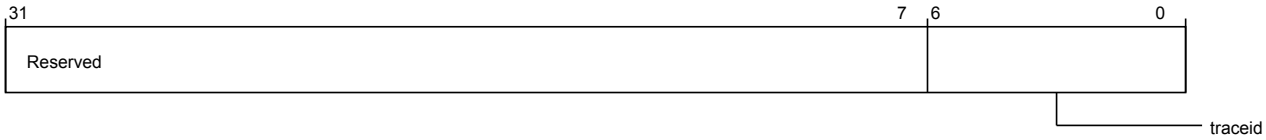


Figure 3-242 por_dt_por_dt_traceid (low)

The following table shows the por_dt_traceid lower register bit assignments.

Table 3-256 por_dt_por_dt_traceid (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6:0	traceid	ATB ID	RW	7'h0

por_dt_pmevcntAB

Contains the PMU event counters A and B.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

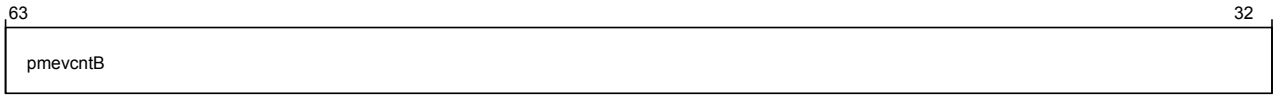


Figure 3-243 por_dt_por_dt_pmevcntab (high)

The following table shows the por_dt_pmevcntAB higher register bit assignments.

Table 3-257 por_dt_por_dt_pmevcntab (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntB	PMU counter B	RW	32'h0000

The following image shows the lower register bit assignments.

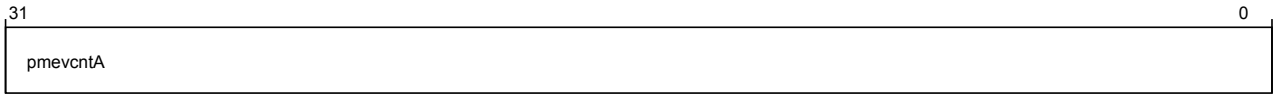


Figure 3-244 por_dt_por_dt_pmevcntab (low)

The following table shows the por_dt_pmevcntAB lower register bit assignments.

Table 3-258 por_dt_por_dt_pmevcntab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntA	PMU counter A	RW	32'h0000

por_dt_pmevcntCD

Contains the PMU event counters C and D.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2010
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

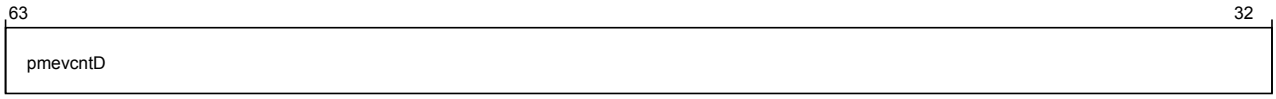


Figure 3-245 por_dt_por_dt_pmevcntcd (high)

The following table shows the por_dt_pmevcntCD higher register bit assignments.

Table 3-259 por_dt_por_dt_pmevcntcd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntD	PMU counter D	RW	32'h0000

The following image shows the lower register bit assignments.

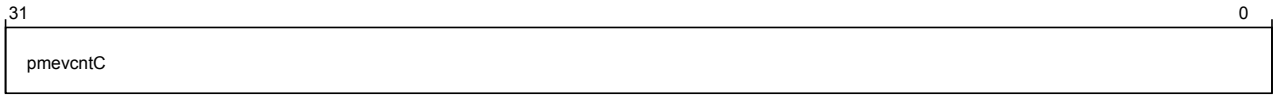


Figure 3-246 por_dt_por_dt_pmevcntcd (low)

The following table shows the por_dt_pmevcntCD lower register bit assignments.

Table 3-260 por_dt_por_dt_pmevcntcd (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntC	PMU counter C	RW	32'h0000

por_dt_pmevcntEF

Contains the PMU event counters E and F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2020
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

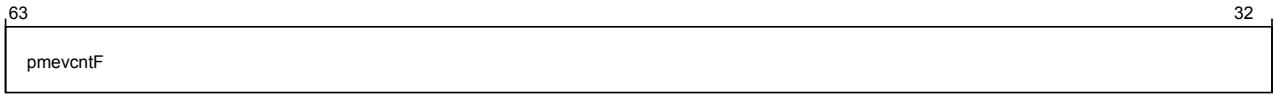


Figure 3-247 por_dt_por_dt_pmevcntef (high)

The following table shows the por_dt_pmevcntEF higher register bit assignments.

Table 3-261 por_dt_por_dt_pmevcntef (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntF	PMU counter F	RW	32'h0000

The following image shows the lower register bit assignments.

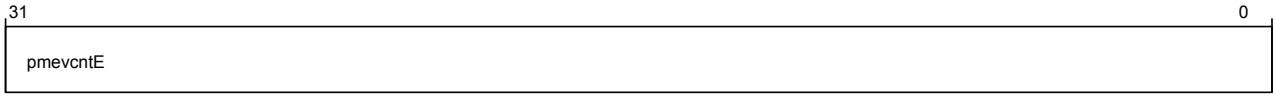


Figure 3-248 por_dt_por_dt_pmevcntef (low)

The following table shows the por_dt_pmevcntEF lower register bit assignments.

Table 3-262 por_dt_por_dt_pmevcntef (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntE	PMU counter E	RW	32'h0000

por_dt_pmevcntGH

Contains the PMU event counters G and H.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2030
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

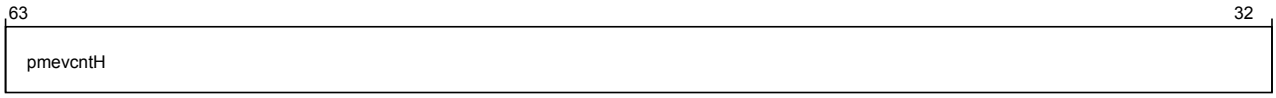


Figure 3-249 por_dt_por_dt_pmevcntgh (high)

The following table shows the por_dt_pmevcntGH higher register bit assignments.

Table 3-263 por_dt_por_dt_pmevcntgh (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntH	PMU counter H	RW	32'h0000

The following image shows the lower register bit assignments.

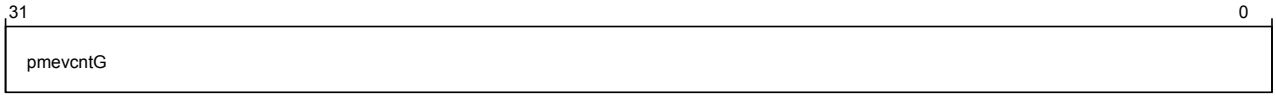


Figure 3-250 por_dt_por_dt_pmevcntgh (low)

The following table shows the por_dt_pmevcntGH lower register bit assignments.

Table 3-264 por_dt_por_dt_pmevcntgh (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntG	PMU counter G	RW	32'h0000

por_dt_pmccntr

Contains the PMU cycle counter.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2040

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

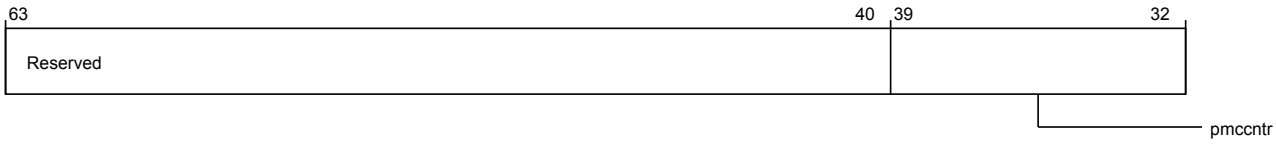


Figure 3-251 por_dt_por_dt_pmccntr (high)

The following table shows the por_dt_pmccntr higher register bit assignments.

Table 3-265 por_dt_por_dt_pmccntr (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pmccntr	PMU cycle counter	RW	40'h0

The following image shows the lower register bit assignments.

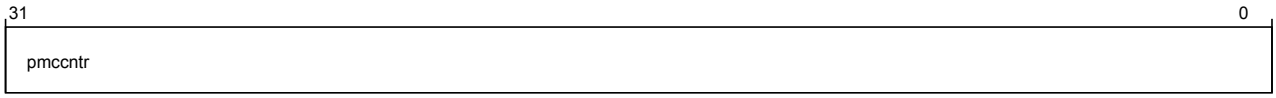


Figure 3-252 por_dt_por_dt_pmccntr (low)

The following table shows the por_dt_pmccntr lower register bit assignments.

Table 3-266 por_dt_por_dt_pmccntr (low)

Bits	Field name	Description	Type	Reset
31:0	pmccntr	PMU cycle counter	RW	40'h0

por_dt_pmevcntsrAB

Contains the PMU event counter shadow registers A and B.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2050
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

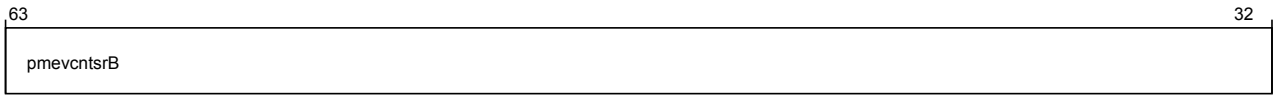


Figure 3-253 por_dt_por_dt_pmevcntsrab (high)

The following table shows the por_dt_pmevcntsrAB higher register bit assignments.

Table 3-267 por_dt_por_dt_pmevcntsrab (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrB	PMU counter B shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

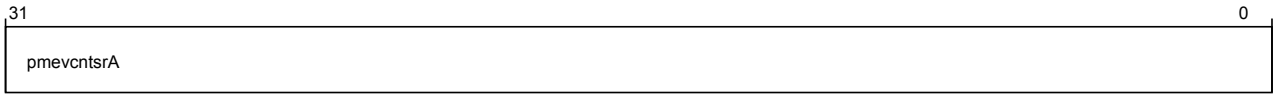


Figure 3-254 por_dt_por_dt_pmevcntsrab (low)

The following table shows the por_dt_pmevcntsrAB lower register bit assignments.

Table 3-268 por_dt_por_dt_pmevcntsrab (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrA	PMU counter A shadow register	RW	32'h0000

por_dt_pmevcntsrCD

Contains the PMU event counter shadow registers C and D.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2060

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

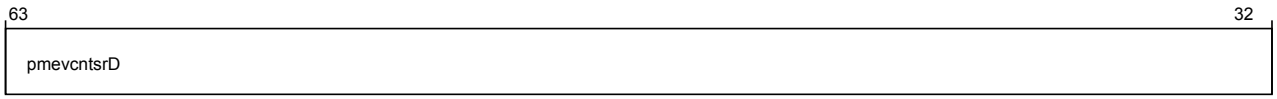


Figure 3-255 por_dt_por_dt_pmevcntsrcd (high)

The following table shows the por_dt_pmevcntsrCD higher register bit assignments.

Table 3-269 por_dt_por_dt_pmevcntsrcd (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrD	PMU counter D shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

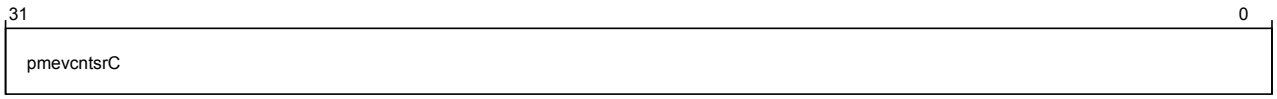


Figure 3-256 por_dt_por_dt_pmevcntsrcd (low)

The following table shows the por_dt_pmevcntsrCD lower register bit assignments.

Table 3-270 por_dt_por_dt_pmevcntsrcd (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrC	PMU counter C shadow register	RW	32'h0000

por_dt_pmevcntsrEF

Contains the PMU event counter shadow registers E and F.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2070
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

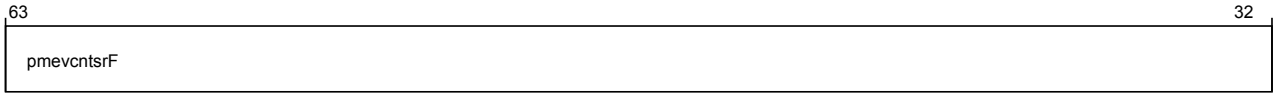


Figure 3-257 por_dt_por_dt_pmevcntsref (high)

The following table shows the por_dt_pmevcntsrEF higher register bit assignments.

Table 3-271 por_dt_por_dt_pmevcntsref (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrF	PMU counter F shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

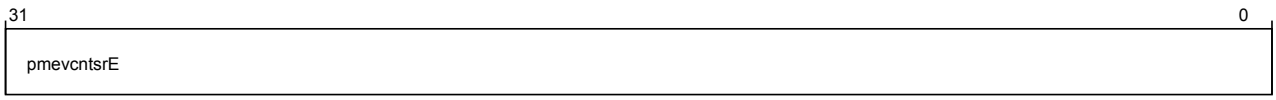


Figure 3-258 por_dt_por_dt_pmevcntsref (low)

The following table shows the por_dt_pmevcntsrEF lower register bit assignments.

Table 3-272 por_dt_por_dt_pmevcntsref (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrE	PMU counter E shadow register	RW	32'h0000

por_dt_pmevcntsrGH

Contains the PMU event counter shadow registers G and H.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2080
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

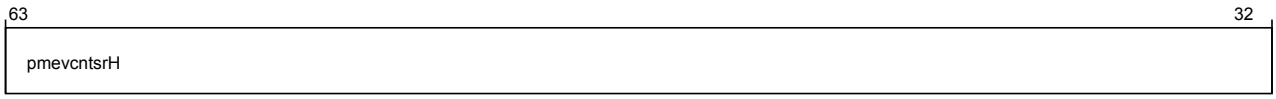


Figure 3-259 por_dt_por_dt_pmevcntsrgh (high)

The following table shows the por_dt_pmevcntsrGH higher register bit assignments.

Table 3-273 por_dt_por_dt_pmevcntsrgh (high)

Bits	Field name	Description	Type	Reset
63:32	pmevcntsrH	PMU counter H shadow register	RW	32'h0000

The following image shows the lower register bit assignments.

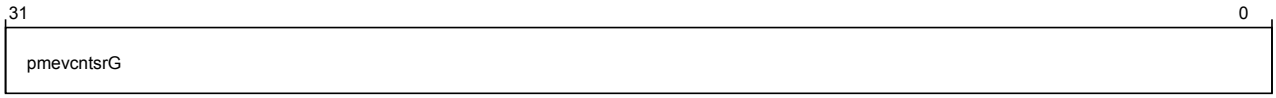


Figure 3-260 por_dt_por_dt_pmevcntsrgh (low)

The following table shows the por_dt_pmevcntsrGH lower register bit assignments.

Table 3-274 por_dt_por_dt_pmevcntsrgh (low)

Bits	Field name	Description	Type	Reset
31:0	pmevcntsrG	PMU counter G shadow register	RW	32'h0000

por_dt_pmccntrsr

Contains the PMU cycle counter shadow register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2090
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

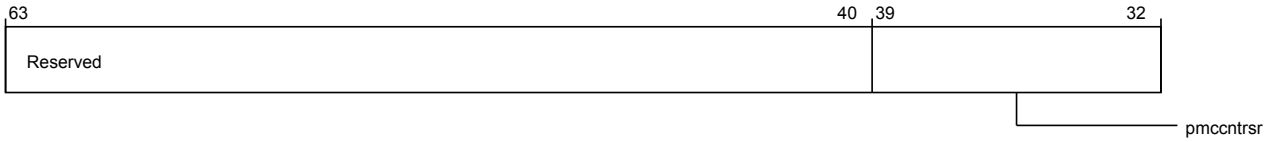


Figure 3-261 por_dt_por_dt_pmccntrsr (high)

The following table shows the por_dt_pmccntrsr higher register bit assignments.

Table 3-275 por_dt_por_dt_pmccntrsr (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

The following image shows the lower register bit assignments.

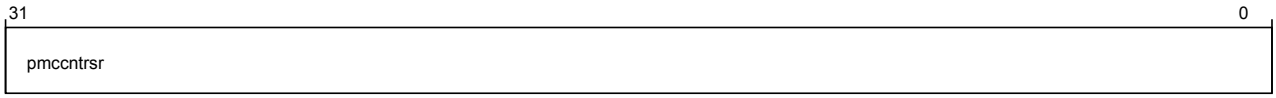


Figure 3-262 por_dt_por_dt_pmccntrsr (low)

The following table shows the por_dt_pmccntrsr lower register bit assignments.

Table 3-276 por_dt_por_dt_pmccntrsr (low)

Bits	Field name	Description	Type	Reset
31:0	pmccntrsr	PMU cycle counter shadow register	RW	40'h0

por_dt_pmcr

Functions as the PMU control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

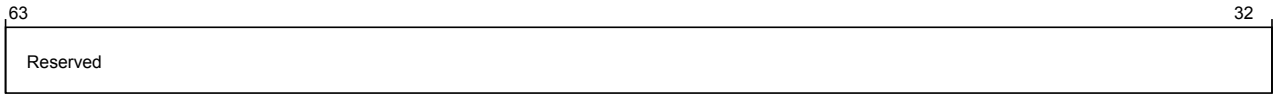


Figure 3-263 por_dt_por_dt_pmcr (high)

The following table shows the por_dt_pmcr higher register bit assignments.

Table 3-277 por_dt_por_dt_pmcr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

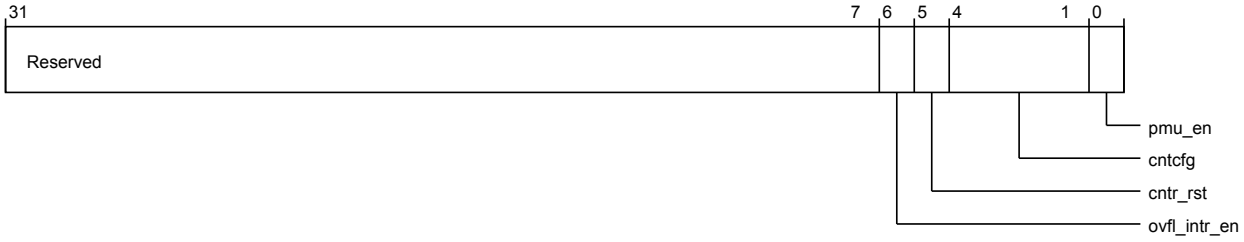


Figure 3-264 por_dt_por_dt_pmcr (low)

The following table shows the por_dt_pmcr lower register bit assignments.

Table 3-278 por_dt_por_dt_pmcr (low)

Bits	Field name	Description	Type	Reset
31:7	Reserved	Reserved	RO	-
6	ovfl_intr_en	Enables INTREQPMU assertion on PMU counter overflow	RW	1'h0
5	cntr_rst	Enables clearing of live counters upon assertion of por_dt_pmsrr.ss_req or PMUSNAPSHOTREQ	RW	1'h0
4:1	cntcfg	Groups adjacent 32-bit registers into a 64-bit register	RW	4'h0
0	pmu_en	Enables PMU features	RW	1'b0

por_dt_pmovsr

Provides the PMU overflow status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

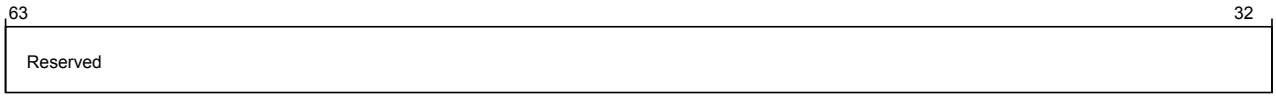


Figure 3-265 por_dt_por_dt_pmovsr (high)

The following table shows the por_dt_pmovsr higher register bit assignments.

Table 3-279 por_dt_por_dt_pmovsr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

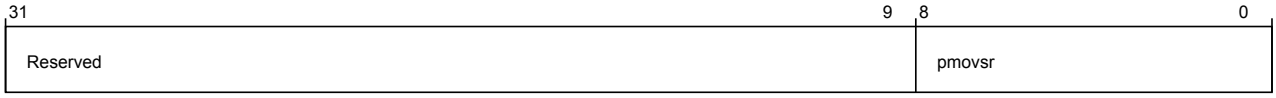


Figure 3-266 por_dt_por_dt_pmovsr (low)

The following table shows the por_dt_pmovsr lower register bit assignments.

Table 3-280 por_dt_por_dt_pmovsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr	PMU overflow status Bit 8: Indicates overflow from cycle counter Bits [7:0]: Indicates overflow from counters 7 to 0	RO	9'h0

por_dt_pmovsr_clr

Clears the PMU overflow status.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h2120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

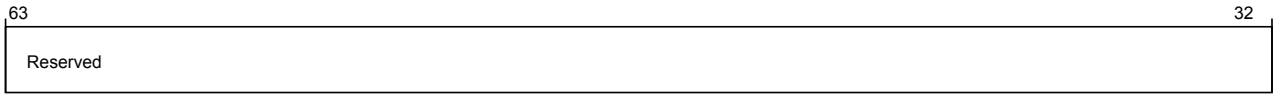


Figure 3-267 por_dt_por_dt_pmovsr_clr (high)

The following table shows the por_dt_pmovsr_clr higher register bit assignments.

Table 3-281 por_dt_por_dt_pmovsr_clr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

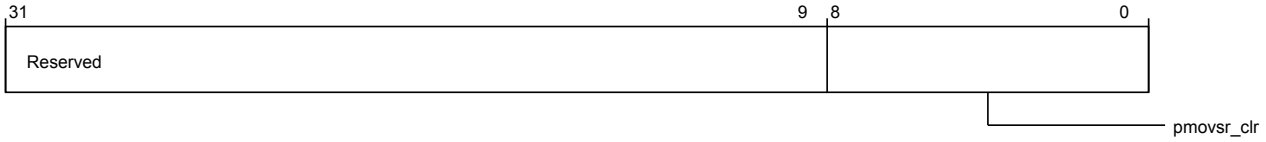


Figure 3-268 por_dt_por_dt_pmovsr_clr (low)

The following table shows the por_dt_pmovsr_clr lower register bit assignments.

Table 3-282 por_dt_por_dt_pmovsr_clr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8:0	pmovsr_clr	Write a 1 to clear the corresponding bit in por_dt_pmovsr.pmovsr	WO	9'b0

por_dt_pmssr

Provides the PMU snapshot status.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

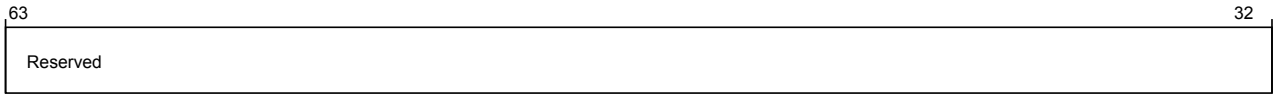


Figure 3-269 por_dt_por_dt_pmssr (high)

The following table shows the por_dt_pmssr higher register bit assignments.

Table 3-283 por_dt_por_dt_pmssr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

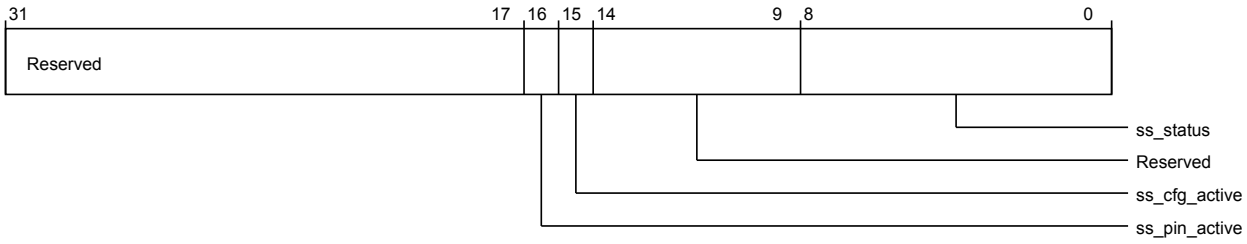


Figure 3-270 por_dt_por_dt_pmssr (low)

The following table shows the por_dt_pmssr lower register bit assignments.

Table 3-284 por_dt_por_dt_pmssr (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	ss_pin_active	Activates PMU snapshot from PMUSNAPSHOTREQ	RO	1'b0
15	ss_cfg_active	PMU snapshot activated from configuration write	RO	1'b0
14:9	Reserved	Reserved	RO	-
8:0	ss_status	PMU snapshot status Bit 8: Indicates snapshot status for cycle counter Bits [7:0]: Indicates snapshot status for counters 7 to 0	RO	9'b0

por_dt_pmsrr

Sends PMU snapshot requests.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h2130
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

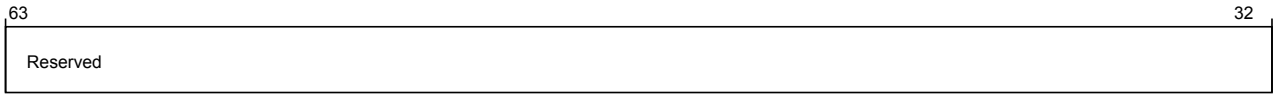


Figure 3-271 por_dt_por_dt_pmsrr (high)

The following table shows the por_dt_pmsrr higher register bit assignments.

Table 3-285 por_dt_por_dt_pmsrr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

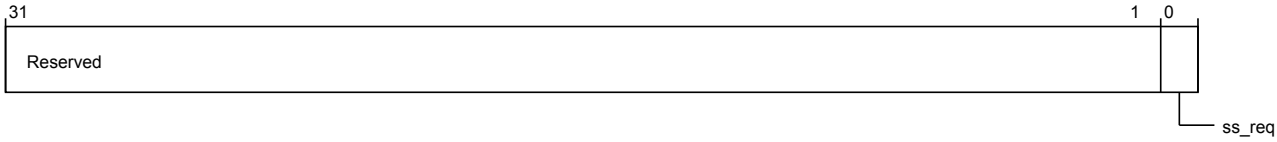


Figure 3-272 por_dt_por_dt_pmsrr (low)

The following table shows the por_dt_pmsrr lower register bit assignments.

Table 3-286 por_dt_por_dt_pmsrr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	ss_req	Write a 1 to request PMU snapshot	WO	1'b0

por_dt_claim

Functions as the claim tag set register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2DA0
Register reset 64'b0111111111111111111111111111111111
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

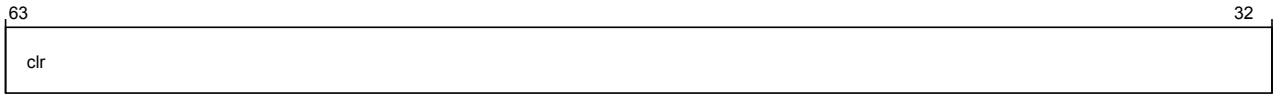


Figure 3-273 por_dt_por_dt_claim (high)

The following table shows the por_dt_claim higher register bit assignments.

Table 3-287 por_dt_por_dt_claim (high)

Bits	Field name	Description	Type	Reset
63:32	clr	Upper half of the claim tag value; enables individual bits to be cleared (write) and returns the current claim tag value (read)	RW	32'b0

The following image shows the lower register bit assignments.

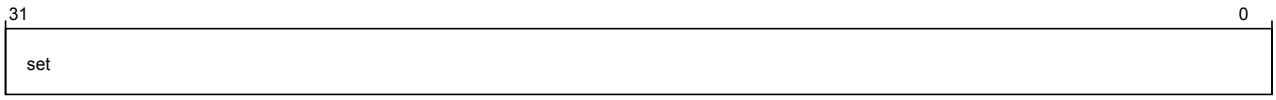


Figure 3-274 por_dt_por_dt_claim (low)

The following table shows the por_dt_claim lower register bit assignments.

Table 3-288 por_dt_por_dt_claim (low)

Bits	Field name	Description	Type	Reset
31:0	set	Lower half of the claim tag value; allows individual bits to be set (write) and returns the number of bits that can be set (read)	RW	32'hffffffff

por_dt_devaff

Functions as the device affinity register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2DA8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

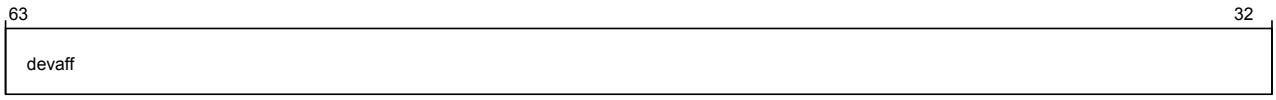


Figure 3-275 por_dt_por_dt_devaff (high)

The following table shows the por_dt_devaff higher register bit assignments.

Table 3-289 por_dt_por_dt_devaff (high)

Bits	Field name	Description	Type	Reset
63:32	devaff	Device affinity register	RO	64'b0

The following image shows the lower register bit assignments.

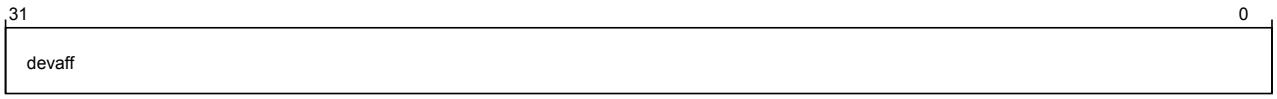


Figure 3-276 por_dt_por_dt_devaff (low)

The following table shows the por_dt_devaff lower register bit assignments.

Table 3-290 por_dt_por_dt_devaff (low)

Bits	Field name	Description	Type	Reset
31:0	devaff	Device affinity register	RO	64'b0

por_dt_lsr

Functions as the lock status register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DB0

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

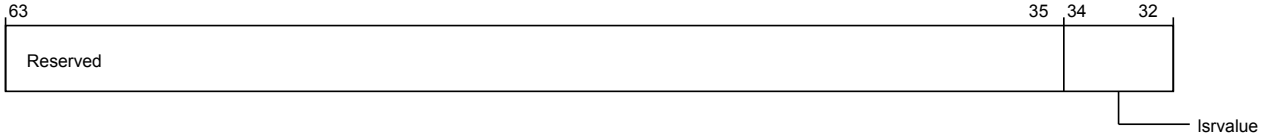


Figure 3-277 por_dt_por_dt_lsr (high)

The following table shows the por_dt_lsr higher register bit assignments.

Table 3-291 por_dt_por_dt_lsr (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	lsrvalue	Lock status value	RO	3'b0

The following image shows the lower register bit assignments.

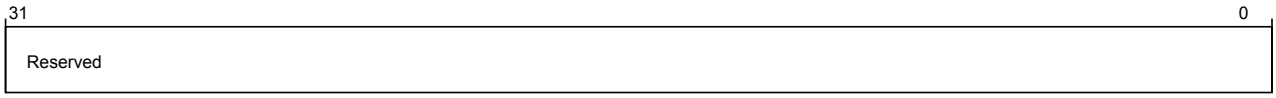


Figure 3-278 por_dt_por_dt_lsr (low)

The following table shows the por_dt_lsr lower register bit assignments.

Table 3-292 por_dt_por_dt_lsr (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_dt_authstatus_devarch

Functions as the authentication status register and the device architecture register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DB8

Register reset 64'b01001010

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

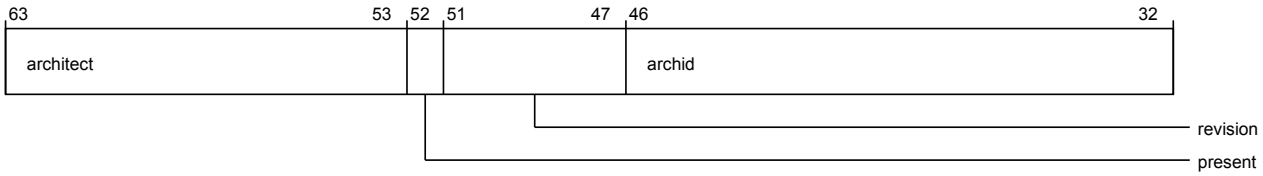


Figure 3-279 por_dt_por_dt_authstatus_devarch (high)

The following table shows the por_dt_authstatus_devarch higher register bit assignments.

Table 3-293 por_dt_por_dt_authstatus_devarch (high)

Bits	Field name	Description	Type	Reset
63:53	architect	Architect	RO	11'b0
52	present	Present	RO	1'b1
51:47	revision	Architecture revision	RO	6'b0
46:32	archid	Architecture ID	RO	16'b0

The following image shows the lower register bit assignments.

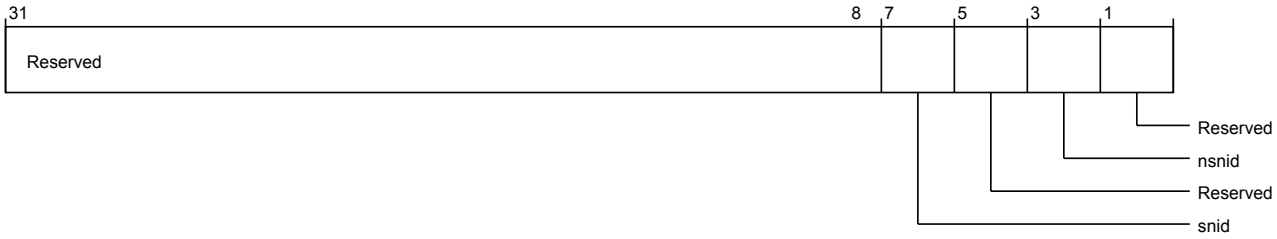


Figure 3-280 por_dt_por_dt_authstatus_devarch (low)

The following table shows the por_dt_authstatus_devarch lower register bit assignments.

Table 3-294 por_dt_por_dt_authstatus_devarch (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:6	snid	Secure non-invasive debug	RO	2'b10
5:4	Reserved	Reserved	RO	-
3:2	nsnid	Non-secure non-invasive debug	RO	2'b10
1:0	Reserved	Reserved	RO	-

por_dt_devid

Functions as the device configuration register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2DC0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

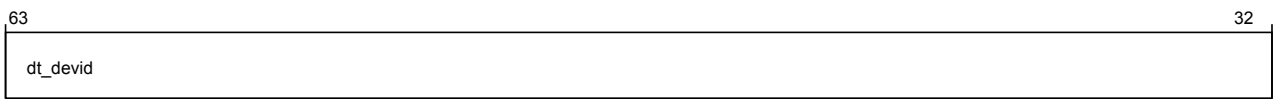


Figure 3-281 por_dt_por_dt_devid (high)

The following table shows the por_dt_devid higher register bit assignments.

Table 3-295 por_dt_por_dt_devid (high)

Bits	Field name	Description	Type	Reset
63:32	dt_devid	Device ID	RO	64'b0

The following image shows the lower register bit assignments.

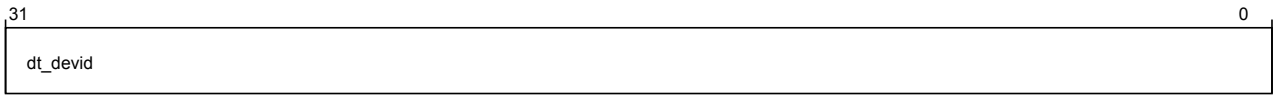


Figure 3-282 por_dt_por_dt_devid (low)

The following table shows the por_dt_devid lower register bit assignments.

Table 3-296 por_dt_por_dt_devid (low)

Bits	Field name	Description	Type	Reset
31:0	dt_devid	Device ID	RO	64'b0

por_dt_devtype

Functions as the device type identifier register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DC8

Register reset 64'b01000011

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

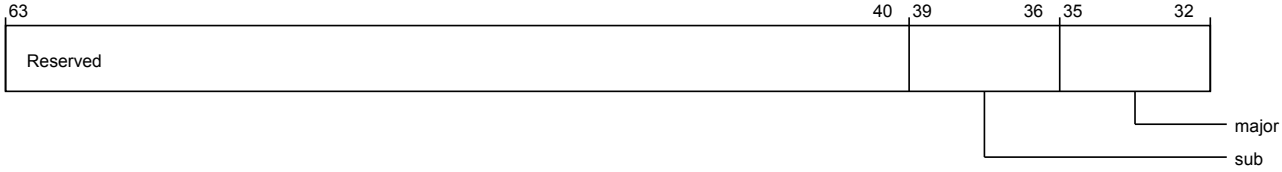


Figure 3-283 por_dt_por_dt_devtype (high)

The following table shows the por_dt_devtype higher register bit assignments.

Table 3-297 por_dt_por_dt_devtype (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:36	sub	Sub type	RO	4'h4
35:32	major	Major type	RO	4'h3

The following image shows the lower register bit assignments.

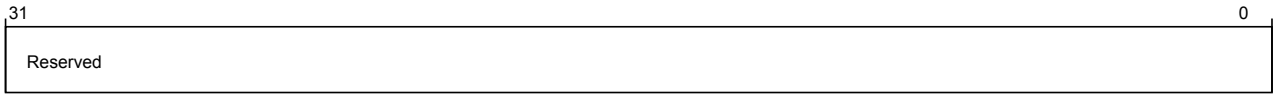


Figure 3-284 por_dt_por_dt_devtype (low)

The following table shows the por_dt_devtype lower register bit assignments.

Table 3-298 por_dt_por_dt_devtype (low)

Bits	Field name	Description	Type	Reset
31:0	Reserved	Reserved	RO	-

por_dt_pidr45

Functions as the identification register for peripheral ID 4 and peripheral ID 5.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DD0

Register reset 64'b000000100

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

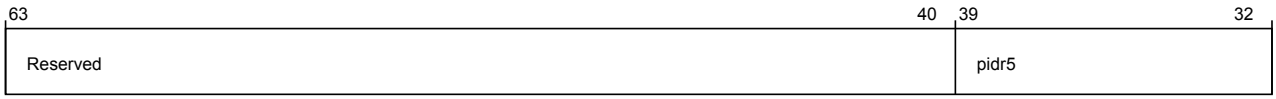


Figure 3-285 por_dt_por_dt_pidr45 (high)

The following table shows the por_dt_pidr45 higher register bit assignments.

Table 3-299 por_dt_por_dt_pidr45 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr5	Peripheral ID 5	RO	8'b0

The following image shows the lower register bit assignments.

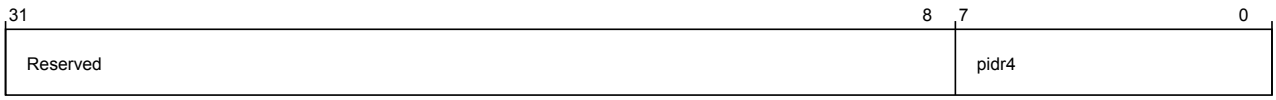


Figure 3-286 por_dt_por_dt_pidr45 (low)

The following table shows the por_dt_pidr45 lower register bit assignments.

Table 3-300 por_dt_por_dt_pidr45 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr4	Peripheral ID 4	RO	8'h4

por_dt_pidr67

Functions as the identification register for peripheral ID 6 and peripheral ID 7.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2DD8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

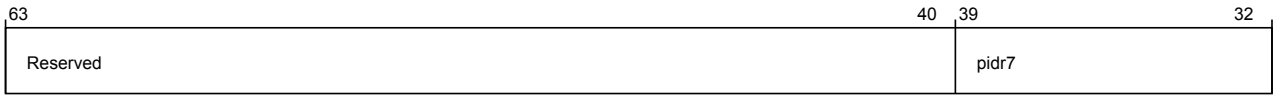


Figure 3-287 por_dt_por_dt_pidr67 (high)

The following table shows the por_dt_pidr67 higher register bit assignments.

Table 3-301 por_dt_por_dt_pidr67 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr7	Peripheral ID 7	RO	8'b0

The following image shows the lower register bit assignments.

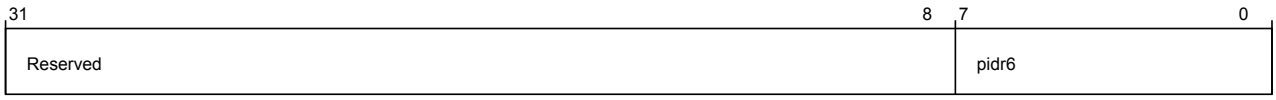


Figure 3-288 por_dt_por_dt_pidr67 (low)

The following table shows the por_dt_pidr67 lower register bit assignments.

Table 3-302 por_dt_por_dt_pidr67 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr6	Peripheral ID 6	RO	8'b0

por_dt_pidr01

Functions as the identification register for peripheral ID 0 and peripheral ID 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2DE0
Register reset 64'b0101110000011100
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

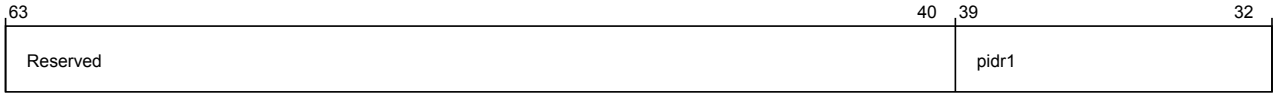


Figure 3-289 por_dt_por_dt_pidr01 (high)

The following table shows the por_dt_pidr01 higher register bit assignments.

Table 3-303 por_dt_por_dt_pidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr1	Peripheral ID 1	RO	8'hb4

The following image shows the lower register bit assignments.

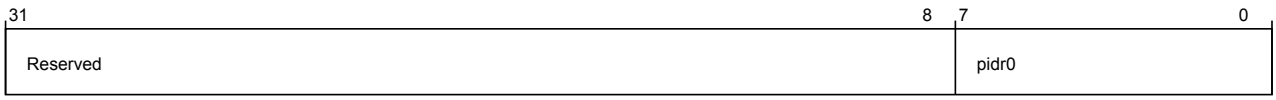


Figure 3-290 por_dt_por_dt_pidr01 (low)

The following table shows the por_dt_pidr01 lower register bit assignments.

Table 3-304 por_dt_por_dt_pidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr0	Peripheral ID 0	RO	8'h34

por_dt_pidr23

Functions as the identification register for peripheral ID 2 and peripheral ID 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2DE8
Register reset 64'b000000111
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

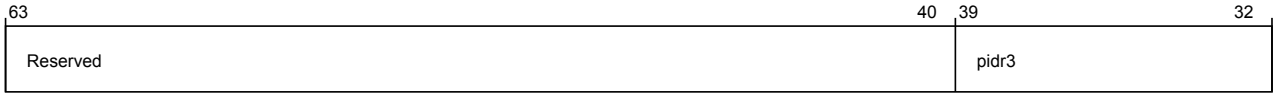


Figure 3-291 por_dt_por_dt_pidr23 (high)

The following table shows the por_dt_pidr23 higher register bit assignments.

Table 3-305 por_dt_por_dt_pidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	pidr3	Peripheral ID 3	RO	8'b0

The following image shows the lower register bit assignments.

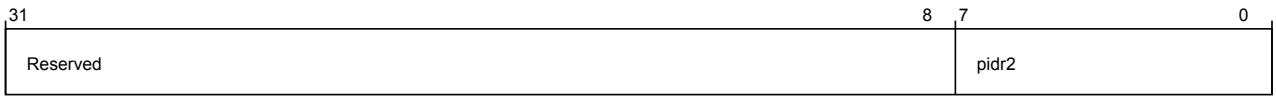


Figure 3-292 por_dt_por_dt_pidr23 (low)

The following table shows the por_dt_pidr23 lower register bit assignments.

Table 3-306 por_dt_por_dt_pidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	pidr2	Peripheral ID 2	RO	8'h7

por_dt_cidr01

Functions as the identification register for component ID 0 and component ID 1.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DF0

Register reset 64'b1001111100001101

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

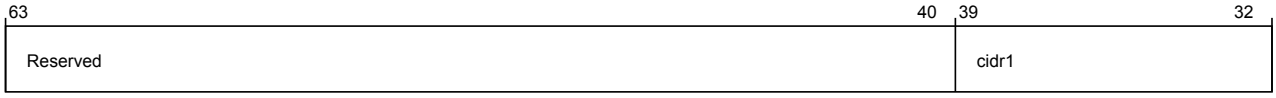


Figure 3-293 por_dt_por_dt_cidr01 (high)

The following table shows the por_dt_cidr01 higher register bit assignments.

Table 3-307 por_dt_por_dt_cidr01 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr1	Component ID 1	RO	8'h9f

The following image shows the lower register bit assignments.

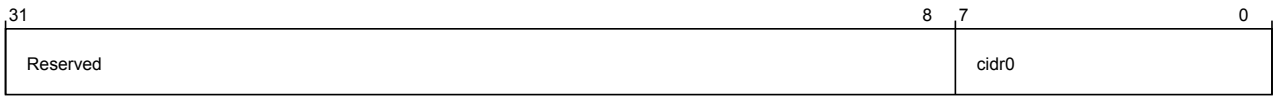


Figure 3-294 por_dt_por_dt_cidr01 (low)

The following table shows the por_dt_cidr01 lower register bit assignments.

Table 3-308 por_dt_por_dt_cidr01 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr0	Component ID 0	RO	8'hd

por_dt_cidr23

Functions as the identification register for component ID 2 and component ID 3.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2DF8

Register reset 64'b0001011100000101

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

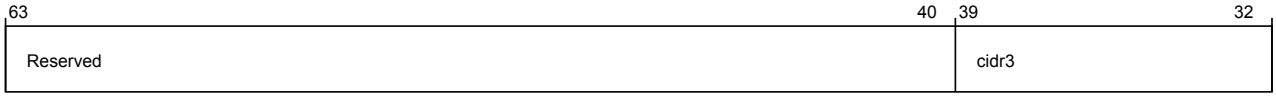


Figure 3-295 por_dt_por_dt_cidr23 (high)

The following table shows the por_dt_cidr23 higher register bit assignments.

Table 3-309 por_dt_por_dt_cidr23 (high)

Bits	Field name	Description	Type	Reset
63:40	Reserved	Reserved	RO	-
39:32	cidr3	Component ID 3	RO	8'hb1

The following image shows the lower register bit assignments.

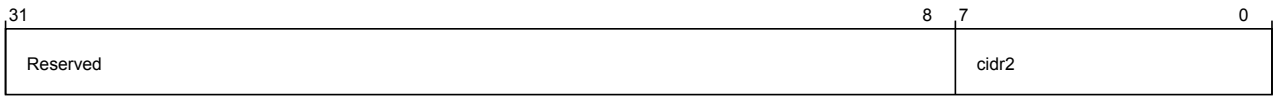


Figure 3-296 por_dt_por_dt_cidr23 (low)

The following table shows the por_dt_cidr23 lower register bit assignments.

Table 3-310 por_dt_por_dt_cidr23 (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:0	cidr2	Component ID 2	RO	8'h5

3.3.4 HN-F register descriptions

Lists the HN-F registers.

por_hnf_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

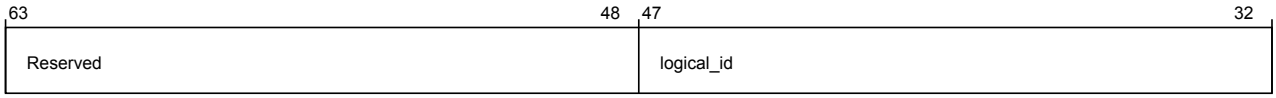


Figure 3-297 por_hnf_por_hnf_node_info (high)

The following table shows the por_hnf_node_info higher register bit assignments.

Table 3-311 por_hnf_por_hnf_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

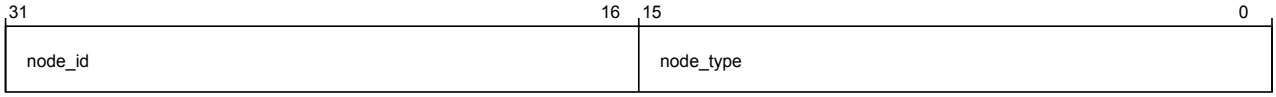


Figure 3-298 por_hnf_por_hnf_node_info (low)

The following table shows the por_hnf_node_info lower register bit assignments.

Table 3-312 por_hnf_por_hnf_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0005

por_hnf_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

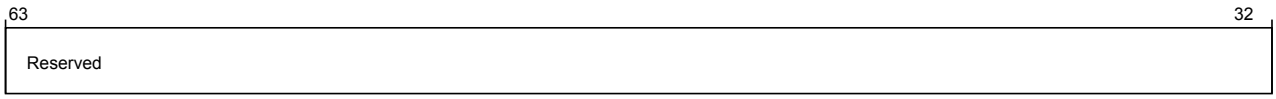


Figure 3-299 por_hnf_por_hnf_child_info (high)

The following table shows the por_hnf_child_info higher register bit assignments.

Table 3-313 por_hnf_por_hnf_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

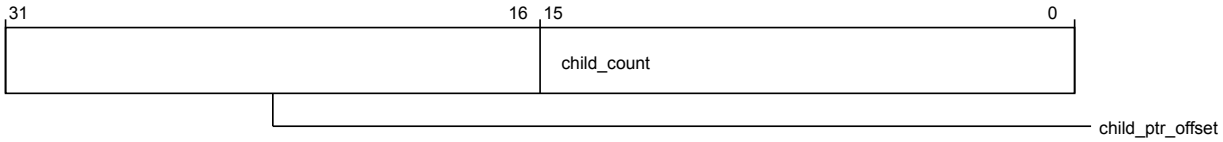


Figure 3-300 por_hnf_por_hnf_child_info (low)

The following table shows the por_hnf_child_info lower register bit assignments.

Table 3-314 por_hnf_por_hnf_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_hnf_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

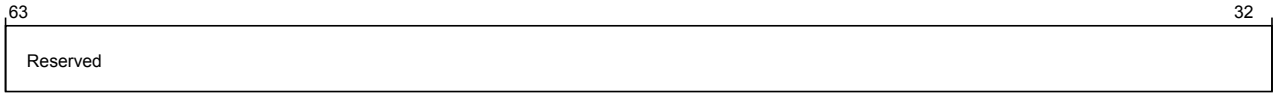


Figure 3-301 por_hnf_por_hnf_secure_register_groups_override (high)

The following table shows the por_hnf_secure_register_groups_override higher register bit assignments.

Table 3-315 por_hnf_por_hnf_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

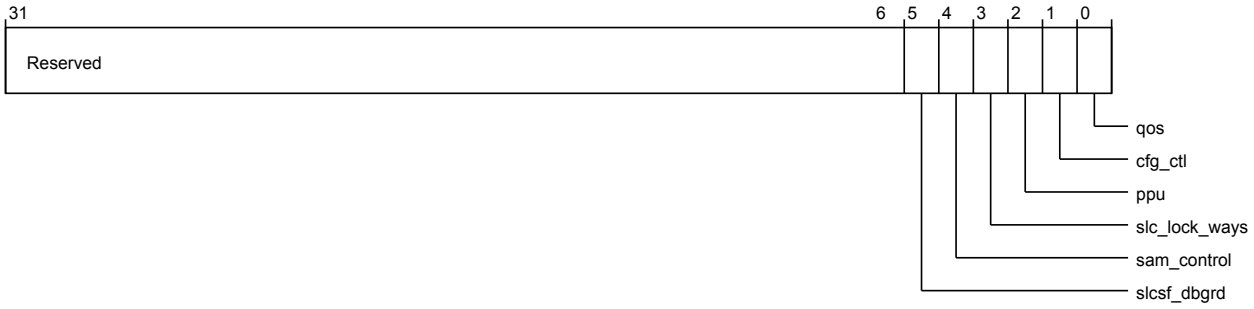


Figure 3-302 por_hnf_por_hnf_secure_register_groups_override (low)

The following table shows the por_hnf_secure_register_groups_override lower register bit assignments.

Table 3-316 por_hnf_por_hnf_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	slcsf_dbgrd	Allows non-secure access to secure SLC/SF debug read registers	RW	1'b0
4	sam_control	Allows non-secure access to secure HN-F SAM control registers	RW	1'b0
3	slc_lock_ways	Allows non-secure access to secure cache way locking registers	RW	1'b0
2	ppu	Allows non-secure access to secure power policy registers	RW	1'b0
1	cfg_ctl	Allows non-secure access to secure configuration control register (por_hnf_cfg_ctl)	RW	1'b0
0	qos	Allows non-secure access to secure QoS registers	RW	1'b0

por_hnf_unit_info

Provides component identification information for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

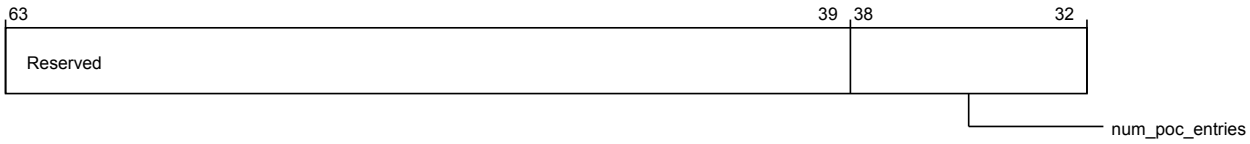


Figure 3-303 por_hnf_por_hnf_unit_info (high)

The following table shows the por_hnf_unit_info higher register bit assignments.

Table 3-317 por_hnf_por_hnf_unit_info (high)

Bits	Field name	Description	Type	Reset
63:39	Reserved	Reserved	RO	-
38:32	num_poc_entries	Number of POCQ entries	RO	Configuration dependent

The following image shows the lower register bit assignments.

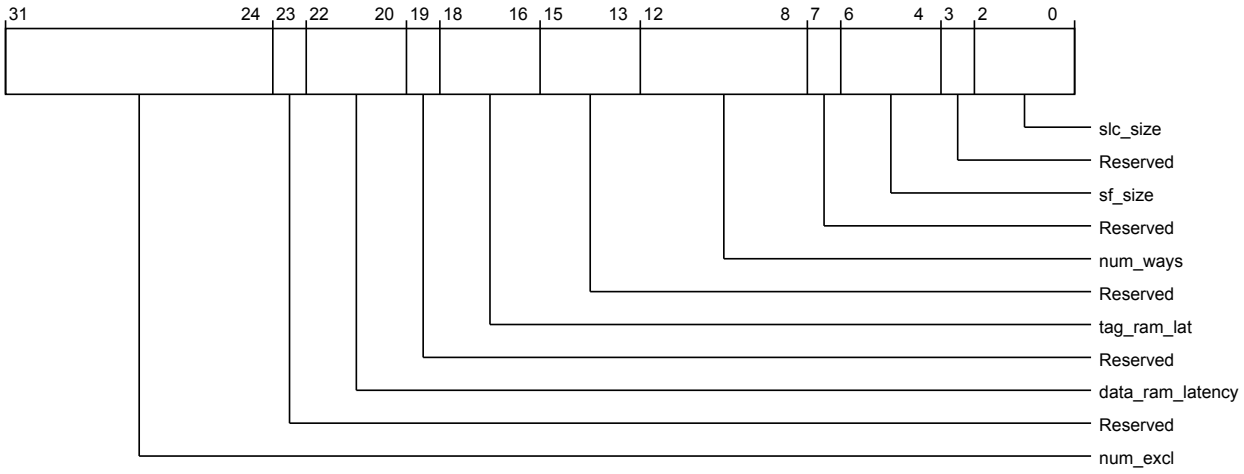


Figure 3-304 por_hnf_por_hnf_unit_info (low)

The following table shows the por_hnf_unit_info lower register bit assignments.

Table 3-318 por_hnf_por_hnf_unit_info (low)

Bits	Field name	Description	Type	Reset
31:24	num_excl	Number of exclusive monitors	RO	-
23	Reserved	Reserved	RO	-
22:20	data_ram_latency	SLC data RAM latency (in cycles)	RO	-
19	Reserved	Reserved	RO	-
18:16	tag_ram_lat	SLC tag RAM latency (in cycles)	RO	-
15:13	Reserved	Reserved	RO	-
12:8	num_ways	Number of cache ways in the SLC	RO	-
7	Reserved	Reserved	RO	-
6:4	sf_size	SF size 3'b000: 512KB 3'b001: 1MB 3'b010: 2MB 3'b011: 4MB 3'b100: 8MB	RO	-
3	Reserved	Reserved	RO	-
2:0	slc_size	SLC size 3'b000: No SLC 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1MB 3'b101: 2MB 3'b110: 3MB 3'b111: 4MB	RO	-

por_hnf_cfg_ctl

Functions as the configuration control register for HN-F.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

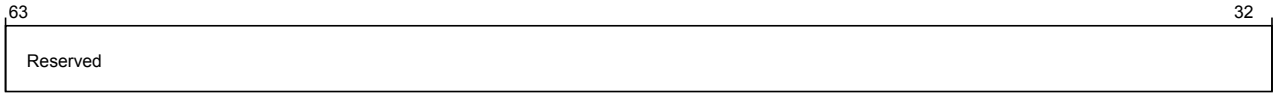


Figure 3-305 por_hnf_por_hnf_cfg_ctl (high)

The following table shows the por_hnf_cfg_ctl higher register bit assignments.

Table 3-319 por_hnf_por_hnf_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

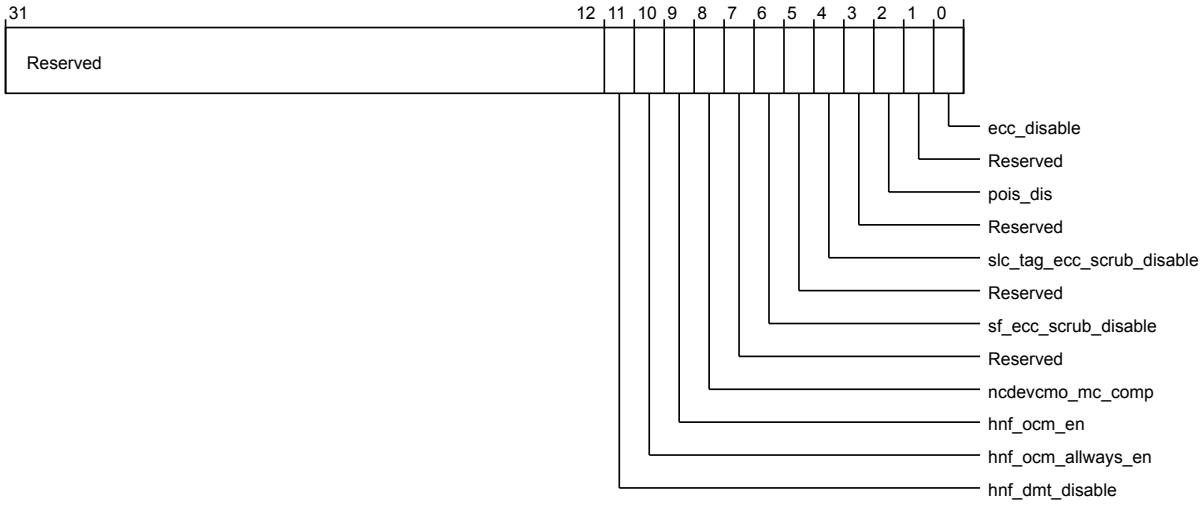


Figure 3-306 por_hnf_por_hnf_cfg_ctl (low)

The following table shows the por_hnf_cfg_ctl lower register bit assignments.

Table 3-320 por_hnf_por_hnf_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11	hnf_dmt_disable	Disables DMT when set	RW	1'b0
10	hnf_ocm_allways_en	Enables all SLC ways with OCM	RW	1'b0
9	hnf_ocm_en	Enables region locking with OCM support	RW	1'b0

Table 3-320 por_hnf_por_hnf_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
8	ncdevcmo_mc_comp	Disables HN-F completion when set NOTE: When set, HN-F sends completion for the following transactions received after completion from SN: 1. Non-cacheable WriteNoSnp 2. Device WriteNoSnp 3. CMO (cache maintenance operations) CONSTRAINT: When this bit is set, por_rni_cfg_ctl.dis_ncwr_stream and por_rnd_cfg_ctl.dis_ncwr_stream must also be set.	RW	1'b0
7	Reserved	Reserved	RO	-
6	sf_ecc_scrub_disable	Disables SF tag single-bit ECC error scrubbing when set	RW	1'b0
5	Reserved	Reserved	RO	-
4	slc_tag_ecc_scrub_disable	Disables SLC tag single-bit ECC error scrubbing when set	RW	1'b0
3	Reserved	Reserved	RO	-
2	pois_dis	Disables parity error data poison when set	RW	1'b0
1	Reserved	Reserved	RO	-
0	ecc_disable	Disables SLC and SF ECC generation/detection when set	RW	1'b0

por_hnf_aux_ctl

Functions as the auxiliary control register for HN-F.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

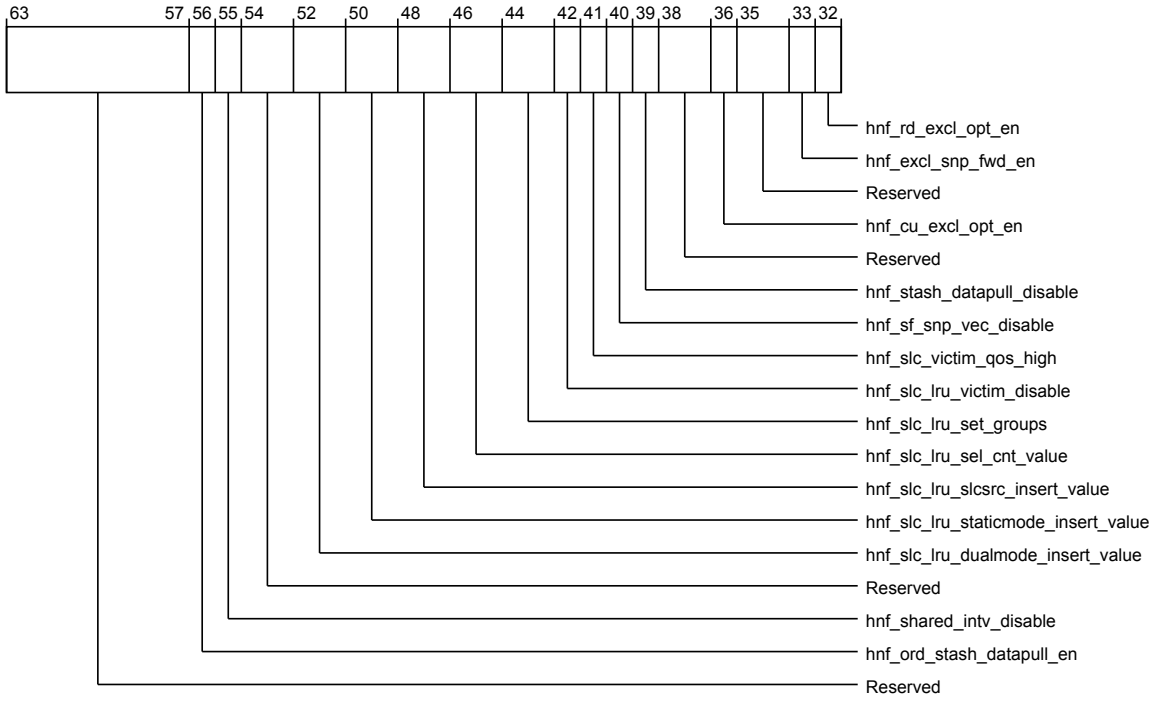


Figure 3-307 por_hnf_por_hnf_aux_ctl (high)

The following table shows the por_hnf_aux_ctl higher register bit assignments.

Table 3-321 por_hnf_por_hnf_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56	hnf_ord_stash_datapull_en	Enables stash datapull for ordered write stash requests	RW	Configuration dependent
55	hnf_shared_intv_disable	Disables snoop requests to CHIB RN-F with shared copy	RW	Configuration dependent
54:53	Reserved	Reserved	RO	-
52:51	hnf_slc_lru_dualmode_insert_value	Insertion value for Dual mode eLRU NOTE: Default is 2'b11.	RW	2'b11
50:49	hnf_slc_lru_staticmode_insert_value	Insertion value for Static mode eLRU NOTE: Default is 2'b10.	RW	2'b10
48:47	hnf_slc_lru_slcsrc_insert_value	Insertion value if SLC source bit is set NOTE: Default is 2'b00.	RW	2'b00

Table 3-321 por_hnf_por_hnf_aux_ctl (high) (continued)

Bits	Field name	Description	Type	Reset
46:45	hnf_slc_lru_sel_cnt_value	Selection counter value for eLRU to determine which group policy is more effective 2'b00: Sel counter is like an 8-bit range; upper limit is 255; middle point is 128 2'b01: Sel counter is like a 9-bit range; upper limit is 511; middle point is 256 2'b10: Sel counter is like a 10-bit range; upper limit is 1023; middle point is 512 2'b11: Sel counter is like an 11-bit range; upper limit is 2047; middle point is 1024 NOTE: Default is 10-bit with counter reset to a value of 512.	RW	2'b10
44:43	hnf_slc_lru_set_groups	Number of sets in monitor group for enhance LRU 2'b00: 16 2'b01: 32 2'b10: 64 2'b11: 128 NOTE: Default is 32 sets per monitor group. If cache size is small (128KB or less), there would be only one set per group.	RW	2'b01
42	hnf_slc_lru_victim_disable	Disable enhanced LRU based victim selection for SLC 1'b0: SLC victim selection is based on eLRU. 1'b1: SLC victim selection is based on LFSR. NOTE: Victim selection for SF is always LFSR-based.	RW	1'b1
41	hnf_slc_victim_qos_high	SLC victim QoS behavior for SN write request 1'b0: Each victim inherits the QoS value of the request which caused it 1'b1: All victims use high QoS class (14)	RW	1'b0
40	hnf_sf_snp_vec_disable	Disables SF snoop vector when set	RW	1'b0
39	hnf_stash_datapull_disable	Disables HN-F stash data pull support when set	RW	1'b0
38:37	Reserved	Reserved	RO	-
36	hnf_cu_excl_opt_en	CleanUnique exclusive optimization enable	RW	Configuration dependent
35:34	Reserved	Reserved	RO	-
33	hnf_excl_snp_fwd_en	Snoop forwarding with exclusives enable	RW	1'b0
32	hnf_rd_excl_opt_en	ReadNotSharedDirty exclusive optimization enable	RW	1'b0

The following image shows the lower register bit assignments.

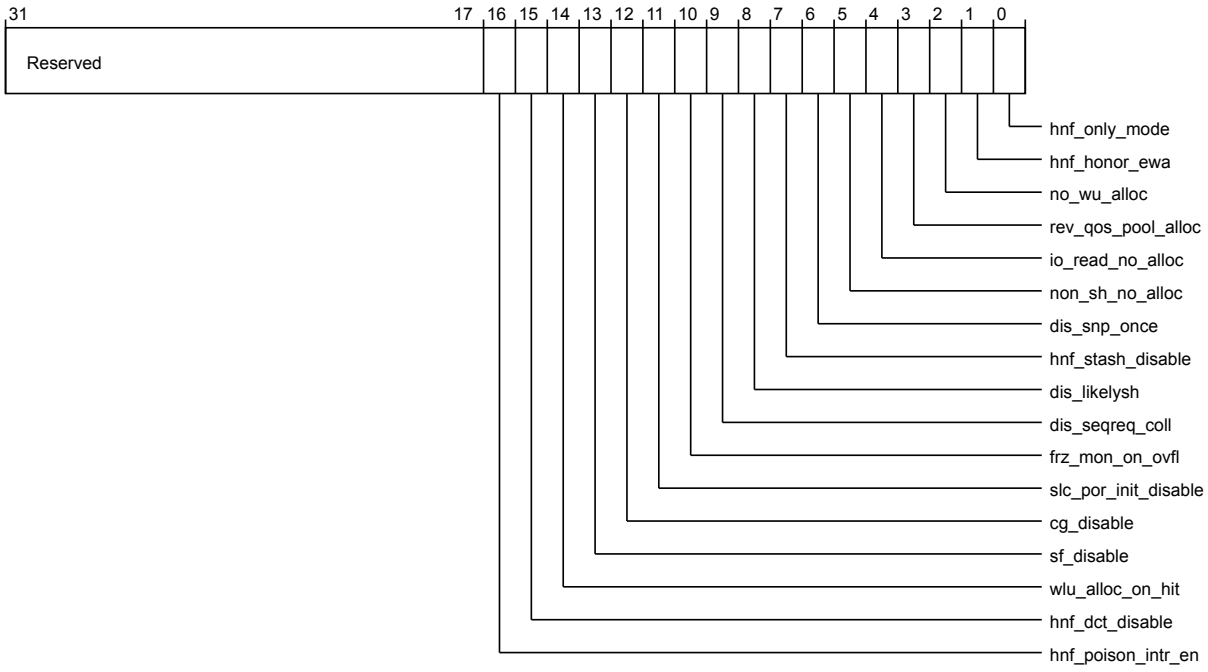


Figure 3-308 por_hnf_por_hnf_aux_ctl (low)

The following table shows the por_hnf_aux_ctl lower register bit assignments.

Table 3-322 por_hnf_por_hnf_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	hnf_poison_intr_en	Enables reporting an interrupt by HN-F when poison is detected at SLC	RW	Configuration dependent
15	hnf_dct_disable	Disables DCT when set	RW	Configuration dependent
14	wlu_alloc_on_hit	Forces WLU requests to allocate if the line hit in SLC	RW	1'b0
13	sf_disable	Disables SF	RW	1'b0
12	cg_disable	Disables HN-F architectural clock gates	RW	1'b0
11	slc_por_init_disable	Disables SLC and SF initialization on Reset	RW	1'b0
10	frz_mon_on_ovfl	Freezes the exclusive monitors	RW	1'b0
9	dis_seqreq_coll		RW	1'b0
8	dis_likelysh	Disables Likely Shared based allocations	RW	1'b0
7	hnf_stash_disable	Disables HN-F stash support	RW	Configuration dependent
6	dis_snp_once	When set, disables SnpOnce and converts to SnpShared	RW	Configuration dependent

Table 3-322 por_hnf_por_hnf_aux_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
5	non_sh_no_alloc	Disables SLC allocation for non-shareable cacheable transactions when set	RW	1'b0
4	io_read_no_alloc	When set, disables ReadOnce and ReadNoSnp allocation in SLC from RN-Is	RW	1'b0
3	rev_qos_pool_alloc	Reverses QoS pool allocation algorithm	RW	1'b0
2	no_wu_alloc	Disables WriteUnique/WriteLineUnique allocations in SLC when set	RW	1'b0
1	hnf_honor_ewa	When set, postpones completion for writes where EWA=0 in the request until HN-F receives completion from MC or SBSX	RW	1'b1
0	hnf_only_mode	Enables HN-F only mode; disables SLC and SF when set	RW	1'b0

por_hnf_r2_aux_ctl

Functions as the auxiliary control register for HN-F for CMN-600 R2 features.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

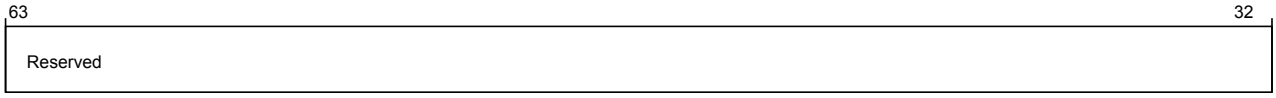


Figure 3-309 por_hnf_por_hnf_r2_aux_ctl (high)

The following table shows the por_hnf_r2_aux_ctl higher register bit assignments.

Table 3-323 por_hnf_por_hnf_r2_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

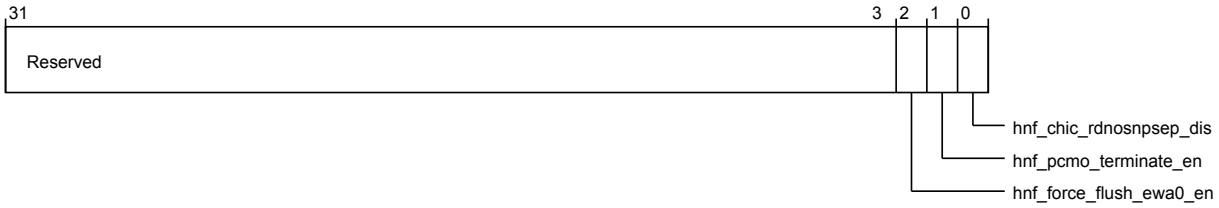


Figure 3-310 por_hnf_por_hnf_r2_aux_ctl (low)

The following table shows the por_hnf_r2_aux_ctl lower register bit assignments.

Table 3-324 por_hnf_por_hnf_r2_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	hnf_force_flush_ewa0_en	Force SLC and SF flush to use EWA 0 for SN writes	RW	1'b0
1	hnf_pcmo_terminate_en	Terminate PCMO in HNF when this bit is set to 1'b1	RW	1'b0
0	hnf_chic_rdnosnpsep_dis	Disables separation of Data and Comp in CHIC mode	RW	1'b0

por_hnf_ppu_pwpr

Functions as the power policy register for HN-F.

Its characteristics are:

Type RW

Register width (Bits) 32

Address offset 14'h1000

Register reset 32'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the lower register bit assignments.

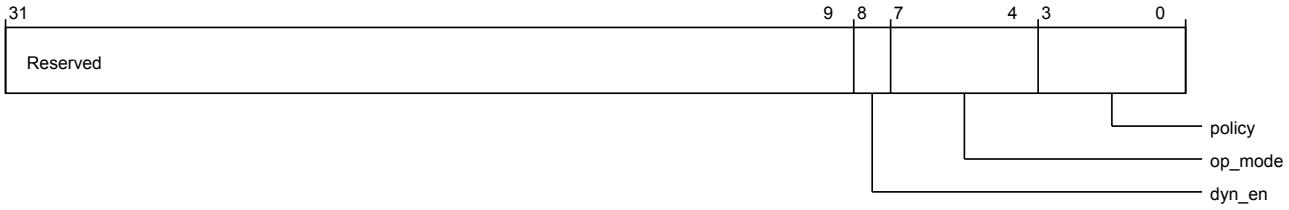


Figure 3-311 por_hnf_por_hnf_ppu_pwpr

The following table shows the por_hnf_ppu_pwpr register bit assignments.

Table 3-325 por_hnf_por_hnf_ppu_pwpr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	dyn_en	Dynamic transition enable	RW	1'b0
7:4	op_mode	HN-F operational power mode 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RW	4'b0
3:0	policy	HN-F power mode policy 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RW	4'b0

por_hnf_ppu_pwsr

Provides power status information for HN-F.

Its characteristics are:

Type RO

Register width (Bits) 32

Address offset 14'h1008

Register reset 32'b0

Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

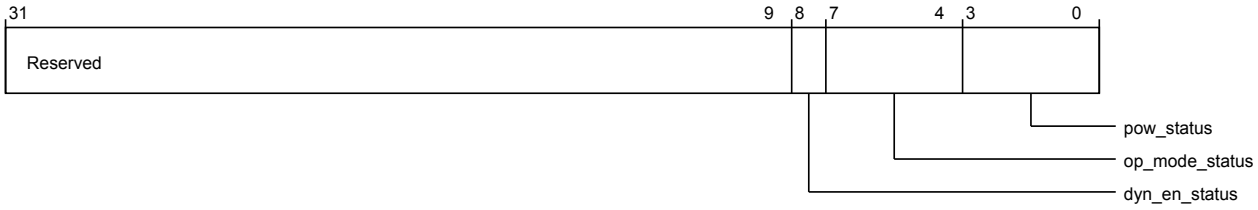


Figure 3-312 por_hnf_por_hnf_ppu_pwsr

The following table shows the por_hnf_ppu_pwsr register bit assignments.

Table 3-326 por_hnf_por_hnf_ppu_pwsr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	dyn_en_status	Dynamic transition status	RO	1'b0

Table 3-326 por_hnf_por_hnf_ppu_pwsr (low) (continued)

Bits	Field name	Description	Type	Reset
7:4	op_mode_status	HN-F operational mode status 4'b0011: FAM 4'b0010: HAM 4'b0001: SFONLY 4'b0000: NOSFSLC	RO	4'b0
3:0	pow_status	HN-F power mode status 4'b1000: ON 4'b0111: FUNC_RET 4'b0010: MEM_RET 4'b0000: OFF	RO	4'b0

por_hnf_ppu_misr

Functions as the power miscellaneous input current status register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 14'h1014
Register reset 32'b0
Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

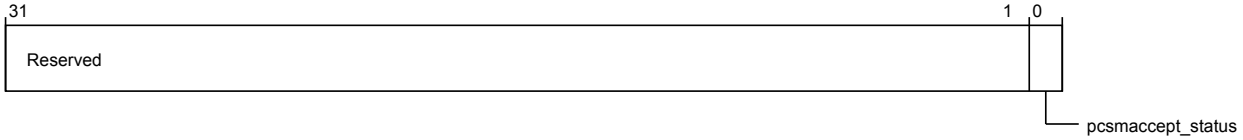


Figure 3-313 por_hnf_por_hnf_ppu_misr

The following table shows the por_hnf_ppu_misr register bit assignments.

Table 3-327 por_hnf_por_hnf_ppu_misr (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	pcsmaccept_status	HN-F RAM PCSMACCEPT status	RO	1'b0

por_hnf_ppu_idr0

Provides identification information for the HN-F PPU.

Its characteristics are:

Type RO

Register width (Bits) 32

Address offset 14'h1FB0

Register reset 32'b00100000000011010010101000

Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

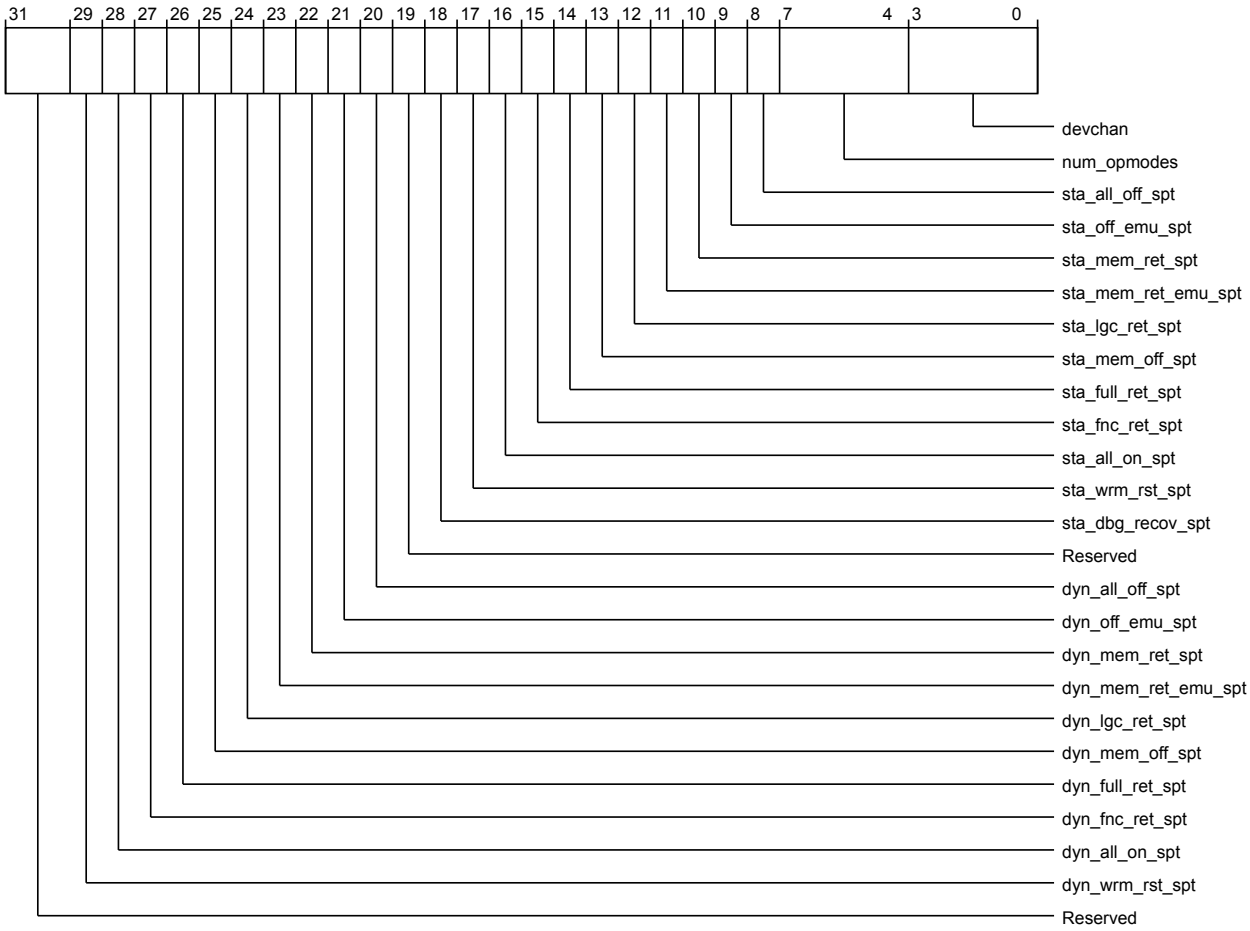


Figure 3-314 por_hnf_por_hnf_ppu_idr0

The following table shows the por_hnf_ppu_idr0 register bit assignments.

Table 3-328 por_hnf_por_hnf_ppu_idr0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29	dyn_wrm_rst_spt	Dynamic warm_rst support	RO	1'b0
28	dyn_all_on_spt	Dynamic on support	RO	1'b0
27	dyn_fnc_ret_spt	Dynamic func_ret support	RO	1'b1
26	dyn_full_ret_spt	Dynamic full_ret support	RO	1'b0

Table 3-328 por_hnf_por_hnf_ppu_idr0 (low) (continued)

Bits	Field name	Description	Type	Reset
25	dyn_mem_off_spt	Dynamic mem_off support	RO	1'b0
24	dyn_lgc_ret_spt	Dynamic logic_ret support	RO	1'b0
23	dyn_mem_ret_emu_spt	Dynamic mem_ret_emu support	RO	1'b0
22	dyn_mem_ret_spt	Dynamic mem_ret support	RO	1'b0
21	dyn_off_emu_spt	Dynamic off_emu support	RO	1'b0
20	dyn_all_off_spt	Dynamic off support	RO	1'b0
19	Reserved	Reserved	RO	-
18	sta_dbg_recov_spt	Static dbg_recov support	RO	1'b0
17	sta_wrm_rst_spt	Static warm_rst support	RO	1'b0
16	sta_all_on_spt	Static on support	RO	1'b1
15	sta_fnc_ret_spt	Static func_ret support	RO	1'b1
14	sta_full_ret_spt	Static full_ret support	RO	1'b0
13	sta_mem_off_spt	Static mem_off support	RO	1'b1
12	sta_lgc_ret_spt	Static logic_ret support	RO	1'b0
11	sta_mem_ret_emu_spt	Static mem_ret_emu support	RO	1'b0
10	sta_mem_ret_spt	Static mem_ret support	RO	1'b1
9	sta_off_emu_spt	Static off_emu support	RO	1'b0
8	sta_all_off_spt	Static off support	RO	1'b1
7:4	num_opmodes	Number of operational modes	RO	4'b0100
3:0	devchan	Number of device interface channels	RO	1'b0

por_hnf_ppu_idr1

Provides identification information for the HN-F PPU.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 14'h1FB4
Register reset 32'b0
Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

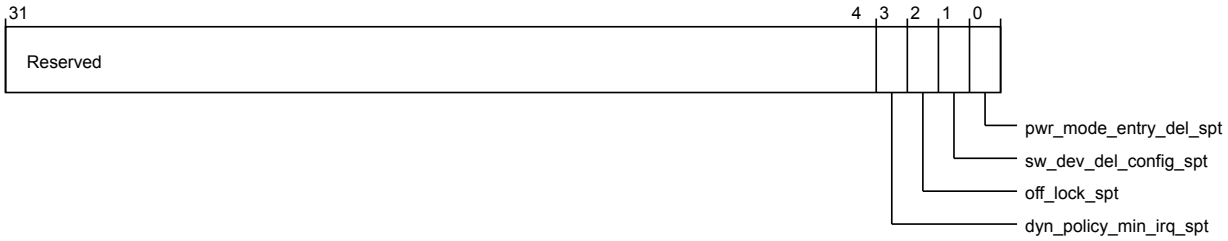


Figure 3-315 por_hnf_por_hnf_ppu_idr1

The following table shows the por_hnf_ppu_idr1 register bit assignments.

Table 3-329 por_hnf_por_hnf_ppu_idr1 (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	dyn_policy_min_irq_spt	Dynamic minimum policy interrupt support	RO	1'b0
2	off_lock_spt	Off and mem_ret lock support	RO	1'b0
1	sw_dev_del_config_spt	Software device delay control configuration support	RO	1'b0
0	pwr_mode_entry_del_spt	Power mode entry delay support	RO	1'b0

por_hnf_ppu_iidr

Functions as the power implementation identification register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 14'h1FC8
Register reset 32'b00001001110000000000000100111011
Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

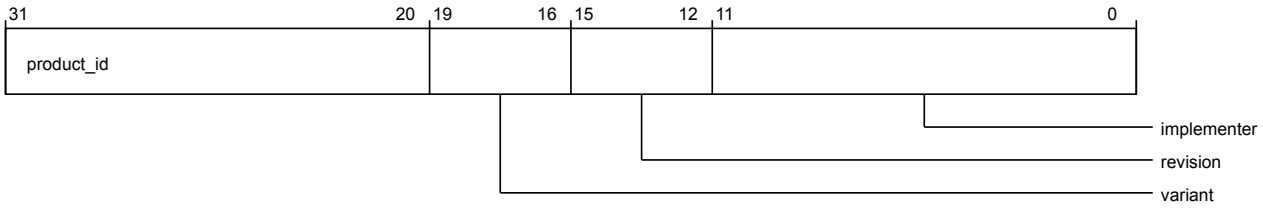


Figure 3-316 por_hnf_por_hnf_ppu_iidr

The following table shows the por_hnf_ppu_iidr register bit assignments.

Table 3-330 por_hnf_por_hnf_ppu_iidr (low)

Bits	Field name	Description	Type	Reset
31:20	product_id	Implementation identifier	RO	12'h434
19:16	variant	Implementation variant	RO	4'h0
15:12	revision	Implementation revision	RO	4'h0
11:0	implementer	Arm implementation	RO	12'h43B

por_hnf_ppu_aidr

Functions as the power architecture identification register for HN-F.

Its characteristics are:

Type RO
Register width (Bits) 32
Address offset 14'h1FCC
Register reset 32'b00010001
Usage constraints There are no usage constraints.

The following image shows the lower register bit assignments.

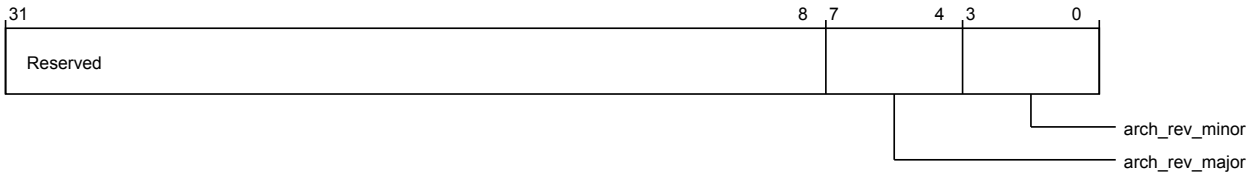


Figure 3-317 por_hnf_por_hnf_ppu_aidr

The following table shows the por_hnf_ppu_aidr register bit assignments.

Table 3-331 por_hnf_por_hnf_ppu_aidr (low)

Bits	Field name	Description	Type	Reset
31:8	Reserved	Reserved	RO	-
7:4	arch_rev_major	PPU architecture major revision	RO	4'h1
3:0	arch_rev_minor	PPU architecture minor revision	RO	4'h1

por_hnf_ppu_dyn_ret_threshold

Configures the dynamic retention threshold for SLC and SF RAM.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1100
Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.

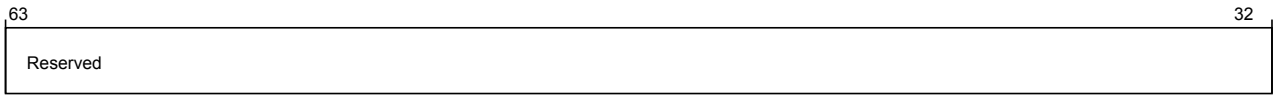


Figure 3-318 por_hnf_por_hnf_ppu_dyn_ret_threshold (high)

The following table shows the por_hnf_ppu_dyn_ret_threshold higher register bit assignments.

Table 3-332 por_hnf_por_hnf_ppu_dyn_ret_threshold (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

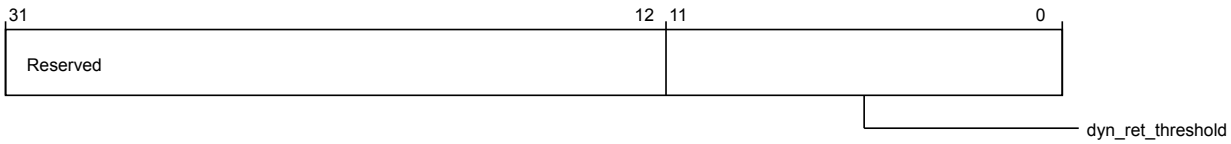


Figure 3-319 por_hnf_por_hnf_ppu_dyn_ret_threshold (low)

The following table shows the por_hnf_ppu_dyn_ret_threshold lower register bit assignments.

Table 3-333 por_hnf_por_hnf_ppu_dyn_ret_threshold (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	dyn_ret_threshold	HN-F RAM idle cycle count threshold	RW	32'b0

por_hnf_qos_band

Provides QoS classifications based on the QoS value ranges.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hA80

Register reset 64'b1111111111101100101110000111000 0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

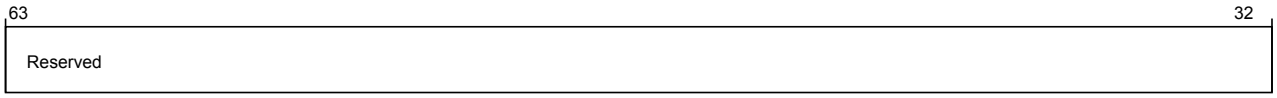


Figure 3-320 por_hnf_por_hnf_qos_band (high)

The following table shows the por_hnf_qos_band higher register bit assignments.

Table 3-334 por_hnf_por_hnf_qos_band (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

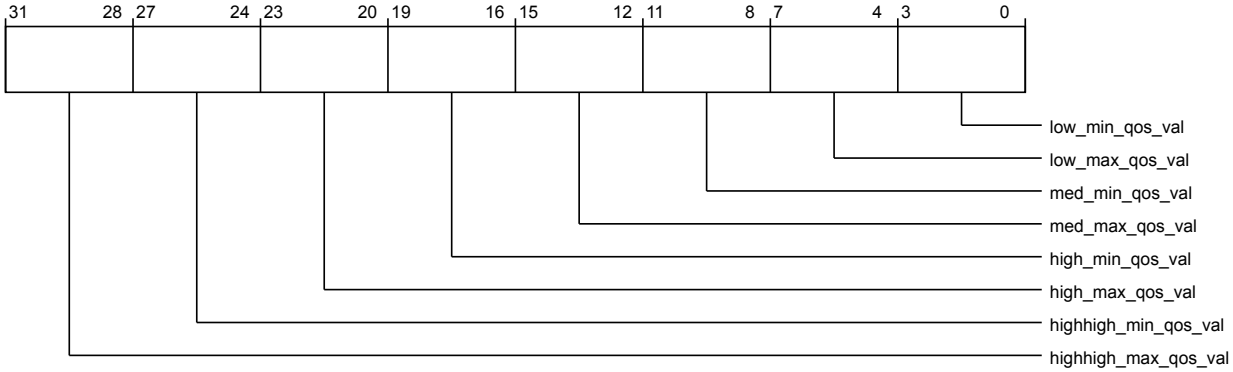


Figure 3-321 por_hnf_por_hnf_qos_band (low)

The following table shows the por_hnf_qos_band lower register bit assignments.

Table 3-335 por_hnf_por_hnf_qos_band (low)

Bits	Field name	Description	Type	Reset
31:28	highhigh_max_qos_val	Maximum value for HighHigh QoS class	RO	4'hF
27:24	highhigh_min_qos_val	Minimum value for HighHigh QoS class	RO	4'hF
23:20	high_max_qos_val	Maximum value for High QoS class	RO	4'hE
19:16	high_min_qos_val	Minimum value for High QoS class	RO	4'hC
15:12	med_max_qos_val	Maximum value for Medium QoS class	RO	4'hB
11:8	med_min_qos_val	Minimum value for Medium QoS class	RO	4'h8
7:4	low_max_qos_val	Maximum value for Low QoS class	RO	4'h7
3:0	low_min_qos_val	Minimum value for Low QoS class	RO	4'h0

por_hnf_qos_reservation

Controls POCQ maximum occupancy counts for each QoS class (HighHigh, High, Medium, and Low).

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA88
Register reset	Configuration dependent
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hnf_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

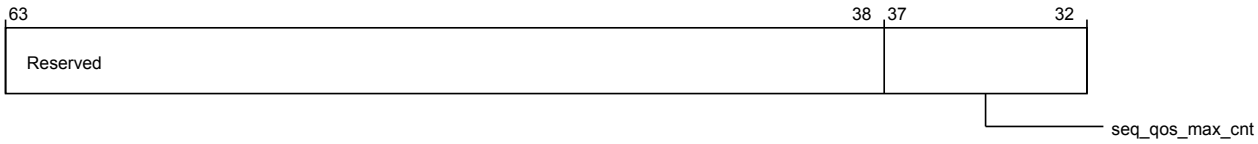


Figure 3-322 por_hnf_por_hnf_qos_reservation (high)

The following table shows the por_hnf_qos_reservation higher register bit assignments.

Table 3-336 por_hnf_por_hnf_qos_reservation (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	seq_qos_max_cnt	Number of entries reserved for SF evictions in POCQ CONSTRAINT: Maximum number is 2 entries.	RW	6'h1

The following image shows the lower register bit assignments.

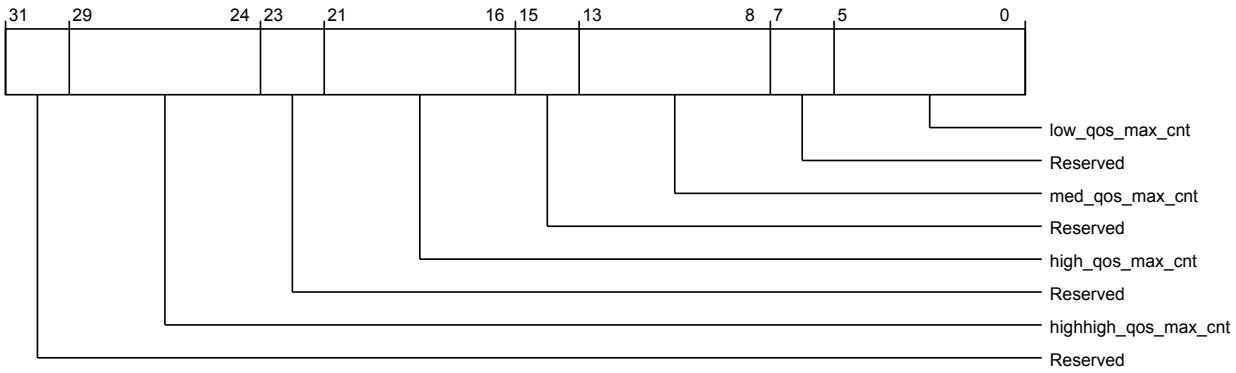


Figure 3-323 por_hnf_por_hnf_qos_reservation (low)

The following table shows the por_hnf_qos_reservation lower register bit assignments.

Table 3-337 por_hnf_por_hnf_qos_reservation (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	highhigh_qos_max_cnt	Maximum number of HighHigh QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
23:22	Reserved	Reserved	RO	-
21:16	high_qos_max_cnt	Maximum number of High QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:8	med_qos_max_cnt	Maximum number of Medium QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent
7:6	Reserved	Reserved	RO	-
5:0	low_qos_max_cnt	Maximum number of Low QoS class occupancy. CONSTRAINT: Minimum is 2 entries	RW	Configuration dependent

por_hnf_rn_starvation

Controls starvation counts for each QoS class. Determines static credit grantee selection.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b1111111111111111011111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.qos

The following image shows the higher register bit assignments.

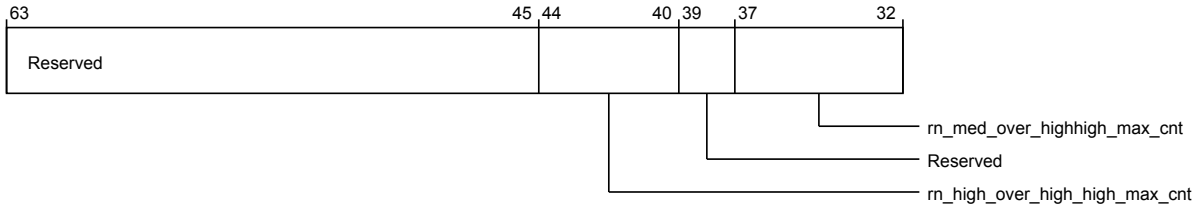


Figure 3-324 por_hnf_por_hnf_rn_starvation (high)

The following table shows the por_hnf_rn_starvation higher register bit assignments.

Table 3-338 por_hnf_por_hnf_rn_starvation (high)

Bits	Field name	Description	Type	Reset
63:45	Reserved	Reserved	RO	-
44:40	rn_high_over_high_high_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over High QoS class	RW	5'h1F
39:38	Reserved	Reserved	RO	-
37:32	rn_med_over_highhigh_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over Medium QoS class	RW	6'h3F

The following image shows the lower register bit assignments.

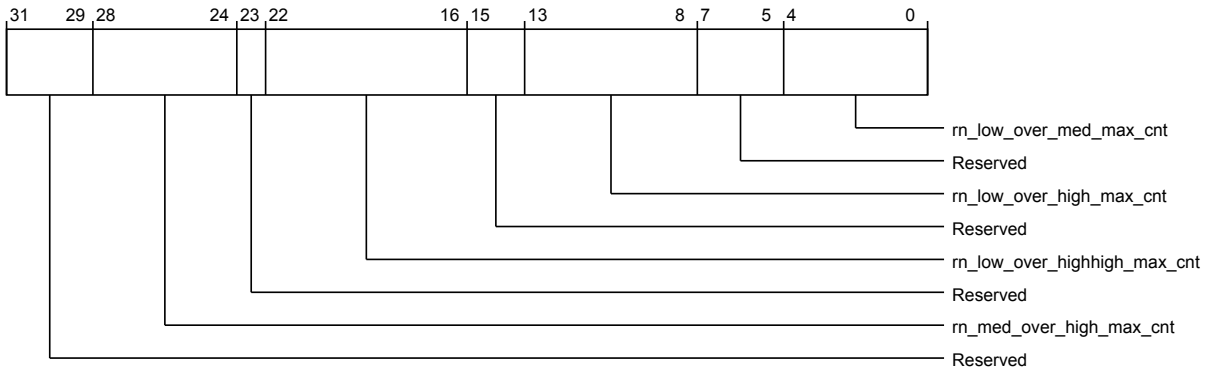


Figure 3-325 por_hnf_por_hnf_rn_starvation (low)

The following table shows the por_hnf_rn_starvation lower register bit assignments.

Table 3-339 por_hnf_por_hnf_rn_starvation (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	rn_med_over_high_max_cnt	Maximum number of consecutive instances where High QoS class wins priority over Medium QoS class	RW	5'h1F
23	Reserved	Reserved	RO	-
22:16	rn_low_over_highhigh_max_cnt	Maximum number of consecutive instances where HighHigh QoS class wins priority over Low QoS class	RW	7'h3F
15:14	Reserved	Reserved	RO	-
13:8	rn_low_over_high_max_cnt	Maximum number of consecutive instances where High QoS class wins priority over Low QoS class	RW	6'h3F
7:5	Reserved	Reserved	RO	-
4:0	rn_low_over_med_max_cnt	Maximum number of consecutive instances where Medium QoS class wins priority over Low QoS class	RW	5'h1F

por_hnf_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b1001010100101
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

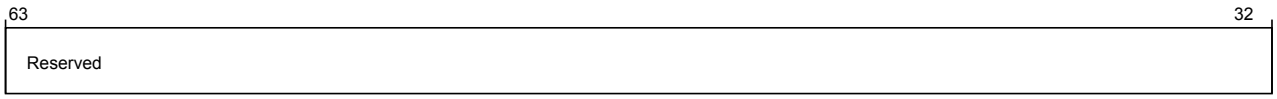


Figure 3-326 por_hnf_por_hnf_errfr (high)

The following table shows the por_hnf_errfr higher register bit assignments.

Table 3-340 por_hnf_por_hnf_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

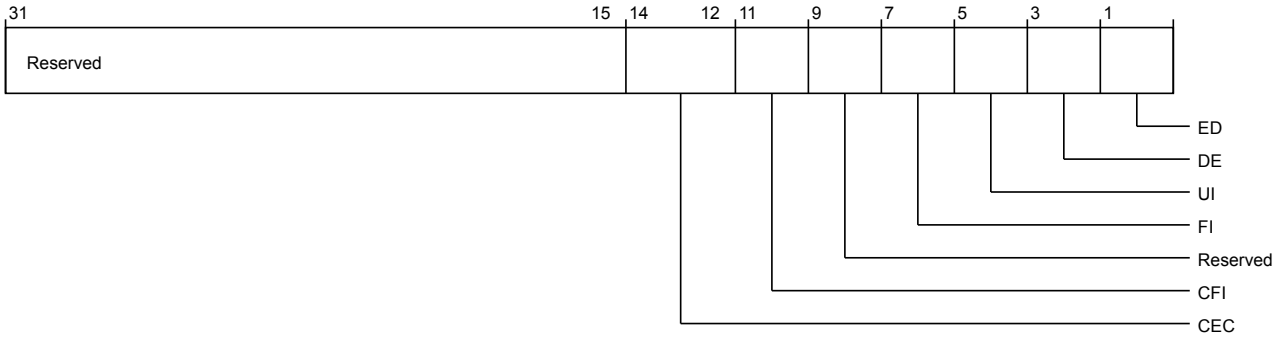


Figure 3-327 por_hnf_por_hnf_errfr (low)

The following table shows the por_hnf_errfr lower register bit assignments.

Table 3-341 por_hnf_por_hnf_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_hnf_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_hnf_errmisc[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hnf_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3008
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

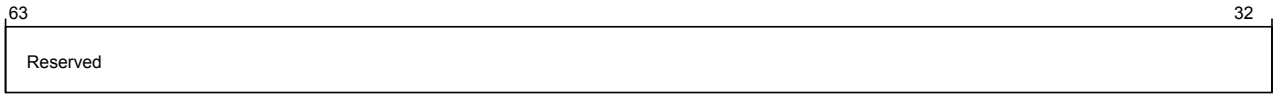


Figure 3-328 por_hnf_por_hnf_errctlr (high)

The following table shows the por_hnf_errctlr higher register bit assignments.

Table 3-342 por_hnf_por_hnf_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

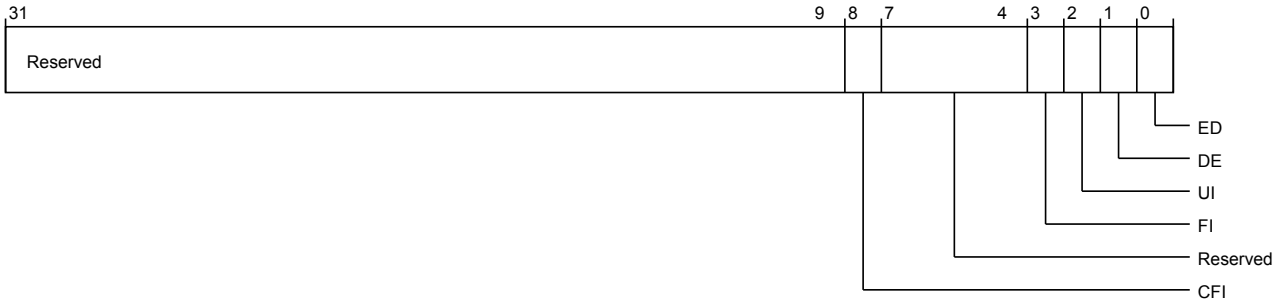


Figure 3-329 por_hnf_por_hnf_errctlr (low)

The following table shows the por_hnf_errctlr lower register bit assignments.

Table 3-343 por_hnf_por_hnf_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hnf_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hnf_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hnf_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hnf_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hnf_errfr.ED	RW	1'b0

por_hnf_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3010
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

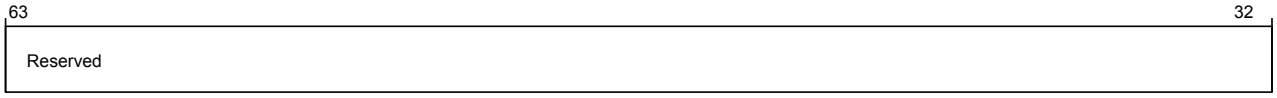


Figure 3-330 por_hnf_por_hnf_errstatus (high)

The following table shows the por_hnf_errstatus higher register bit assignments.

Table 3-344 por_hnf_por_hnf_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-331 por_hnf_por_hnf_errstatus (low)

The following table shows the por_hnf_errstatus lower register bit assignments.

Table 3-345 por_hnf_por_hnf_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hnf_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Table 3-345 por_hnf_por_hnf_errstatus (low) (continued)

Bits	Field name	Description	Type	Reset
26	MV	por_hnf_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_hnf_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

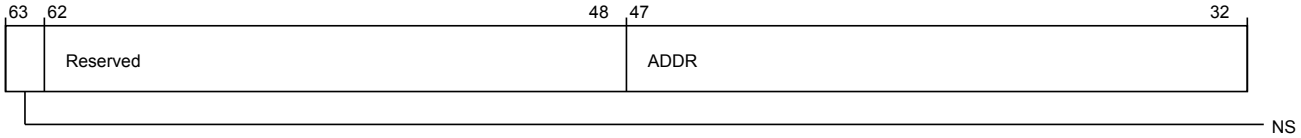


Figure 3-332 por_hnf_por_hnf_erraddr (high)

The following table shows the por_hnf_erraddr higher register bit assignments.

Table 3-346 por_hnf_por_hnf_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hnf_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

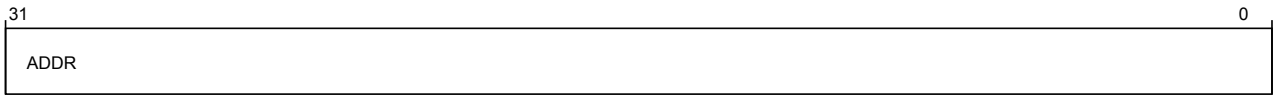


Figure 3-333 por_hnf_por_hnf_erraddr (low)

The following table shows the por_hnf_erraddr lower register bit assignments.

Table 3-347 por_hnf_por_hnf_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hnf_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/ uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

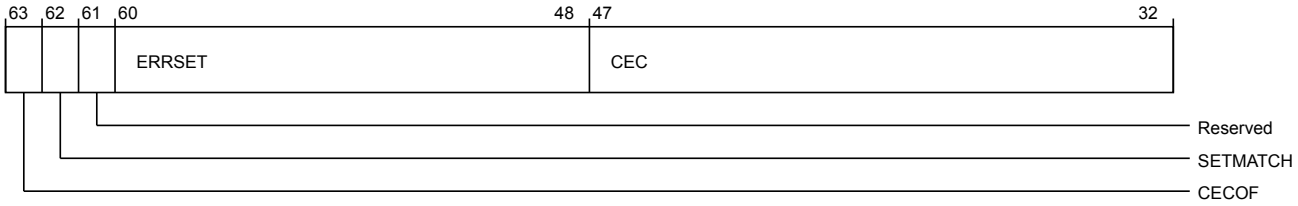


Figure 3-334 por_hnf_por_hnf_errmisc (high)

The following table shows the por_hnf_errmisc higher register bit assignments.

Table 3-348 por_hnf_por_hnf_errmisc (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following image shows the lower register bit assignments.

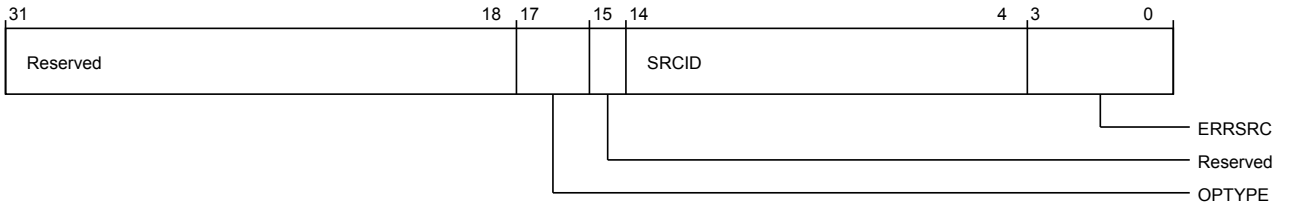


Figure 3-335 por_hnf_por_hnf_errmisc (low)

The following table shows the por_hnf_errmisc lower register bit assignments.

Table 3-349 por_hnf_por_hnf_errmisc (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00

Table 3-349 por_hnf_por_hnf_errmisc (low) (continued)

Bits	Field name	Description	Type	Reset
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

por_hnf_err_inj

Enables error injection and setup. When enabled for a given source ID and logic processor ID, HN-F returns a slave error and reports an error interrupt. This error interrupt emulates a SLC double-bit data ECC error. This feature enables software to test the error handler. The slave error is reported for cacheable read access for which SLC hit is the data source. No slave error or error interrupt is reported for cacheable read access in which SLC miss is the data source.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3030

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

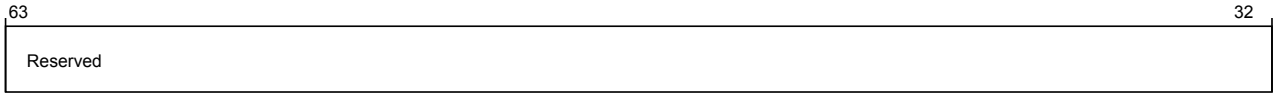


Figure 3-336 por_hnf_por_hnf_err_inj (high)

The following table shows the por_hnf_err_inj higher register bit assignments.

Table 3-350 por_hnf_por_hnf_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

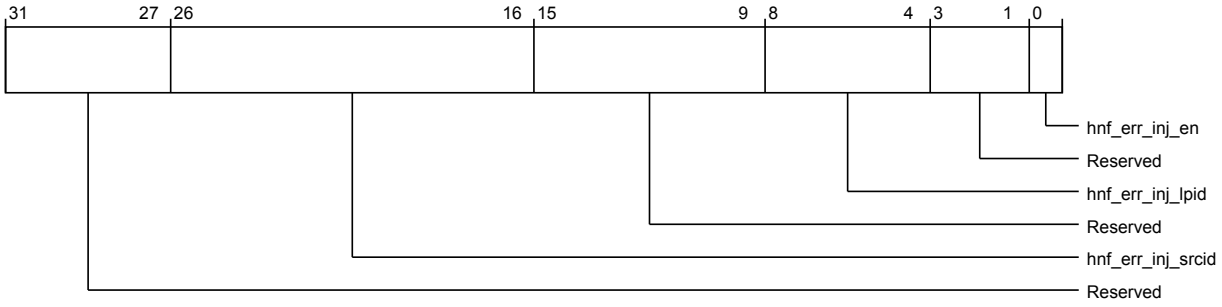


Figure 3-337 por_hnf_por_hnf_err_inj (low)

The following table shows the por_hnf_err_inj lower register bit assignments.

Table 3-351 por_hnf_por_hnf_err_inj (low)

Bits	Field name	Description	Type	Reset
31:27	Reserved	Reserved	RO	-
26:16	hnf_err_inj_srcid	RN source ID for read access which results in a SLC miss; does not report slave error or error to match error injection	RW	11'h0
15:9	Reserved	Reserved	RO	-
8:4	hnf_err_inj_lpid	LPID used to match for error injection	RW	5'h0
3:1	Reserved	Reserved	RO	-
0	hnf_err_inj_en	Enables error injection and report	RW	1'b0

por_hnf_byte_par_err_inj

Functions as the byte parity error injection register for HN-F.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h3038
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

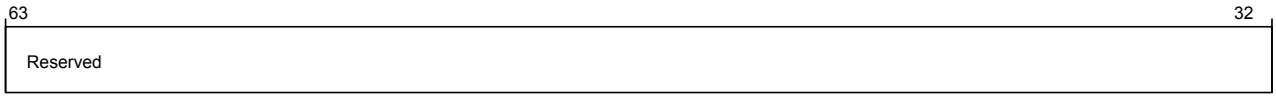


Figure 3-338 por_hnf_por_hnf_byte_par_err_inj (high)

The following table shows the por_hnf_byte_par_err_inj higher register bit assignments.

Table 3-352 por_hnf_por_hnf_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

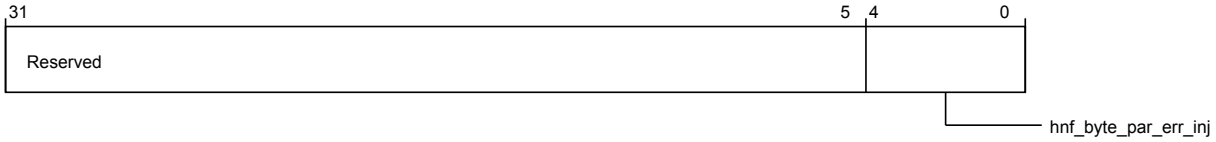


Figure 3-339 por_hnf_por_hnf_byte_par_err_inj (low)

The following table shows the por_hnf_byte_par_err_inj lower register bit assignments.

Table 3-353 por_hnf_por_hnf_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	hnf_byte_par_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next SLC hit; the error will be injected in all data flits on specified byte (0 to 31)	WO	5'h0

por_hnf_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b1001010100101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

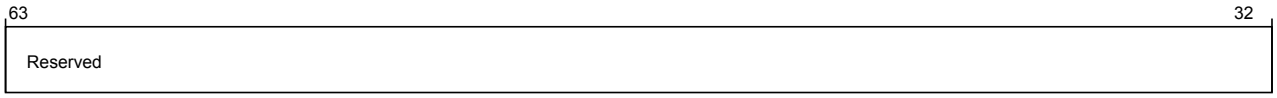


Figure 3-340 por_hnf_por_hnf_errfr_ns (high)

The following table shows the por_hnf_errfr_NS higher register bit assignments.

Table 3-354 por_hnf_por_hnf_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

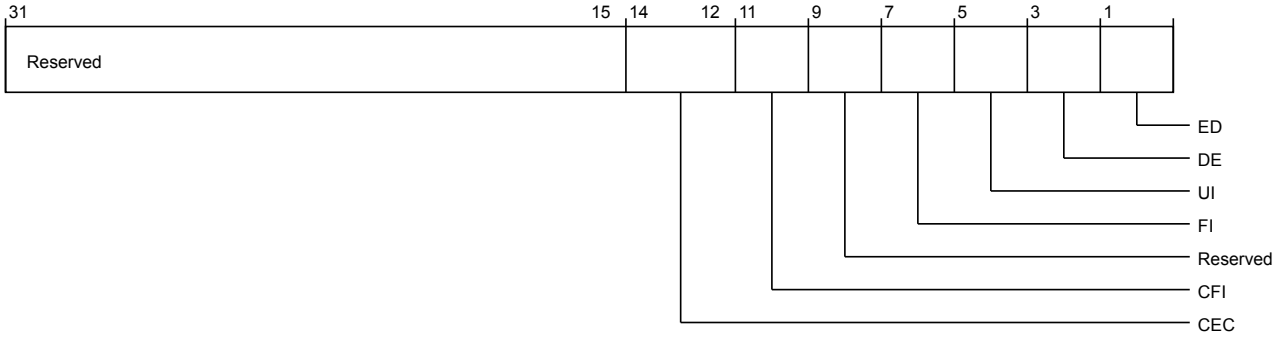


Figure 3-341 por_hnf_por_hnf_errfr_ns (low)

The following table shows the por_hnf_errfr_NS lower register bit assignments.

Table 3-355 por_hnf_por_hnf_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_hnf_errmisc_NS[39:32] 3'b100: Implements 16-bit error counter in por_hnf_errmisc_NS[47:32]	RO	3'b100
11:10	CFI	Corrected error interrupt	RO	2'b10
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hnf_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

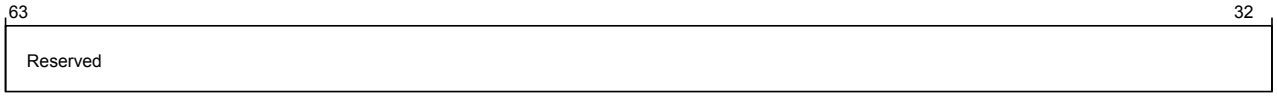


Figure 3-342 por_hnf_por_hnf_errctlr_ns (high)

The following table shows the por_hnf_errctlr_NS higher register bit assignments.

Table 3-356 por_hnf_por_hnf_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

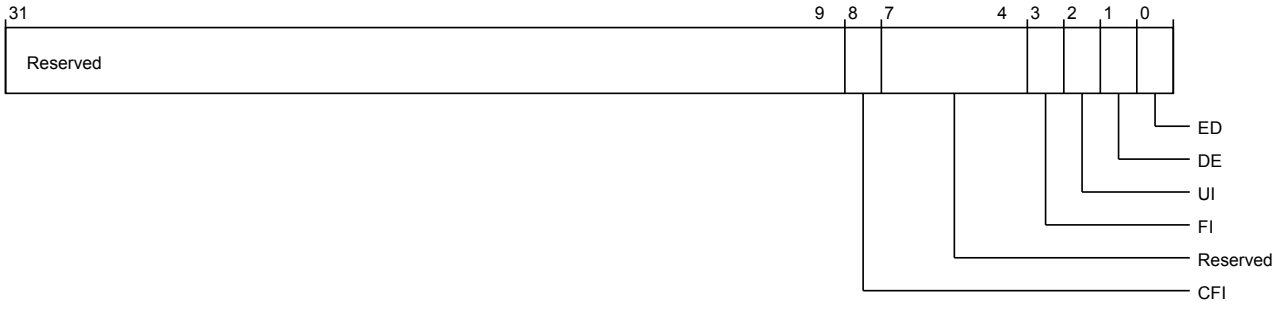


Figure 3-343 por_hnf_por_hnf_errctlr_ns (low)

The following table shows the por_hnf_errctlr_NS lower register bit assignments.

Table 3-357 por_hnf_por_hnf_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hnf_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 3-357 por_hnf_por_hnf_errctlr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hnf_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hnf_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hnf_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hnf_errfr_NS.ED	RW	1'b0

por_hnf_errstatus_NS

Functions as the non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3110

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

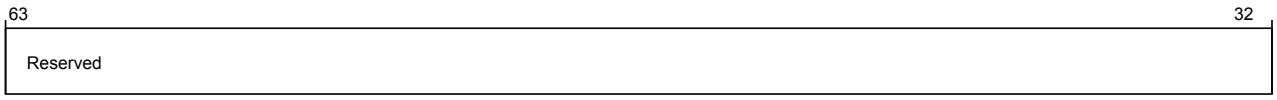


Figure 3-344 por_hnf_por_hnf_errstatus_ns (high)

The following table shows the por_hnf_errstatus_NS higher register bit assignments.

Table 3-358 por_hnf_por_hnf_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-345 por_hnf_por_hnf_errstatus_ns (low)

The following table shows the por_hnf_errstatus_NS lower register bit assignments.

Table 3-359 por_hnf_por_hnf_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hnf_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hnf_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 3-359 por_hnf_por_hnf_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_hnf_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

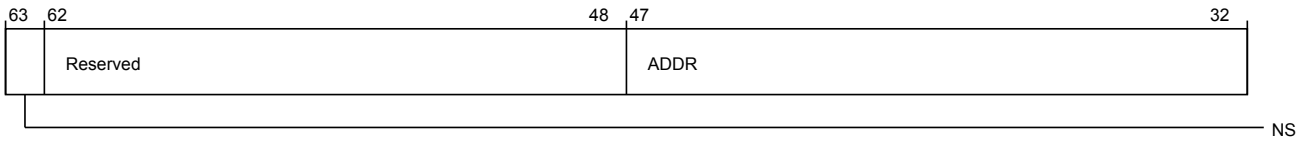


Figure 3-346 por_hnf_por_hnf_erraddr_ns (high)

The following table shows the por_hnf_erraddr_NS higher register bit assignments.

Table 3-360 por_hnf_por_hnf_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hnf_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

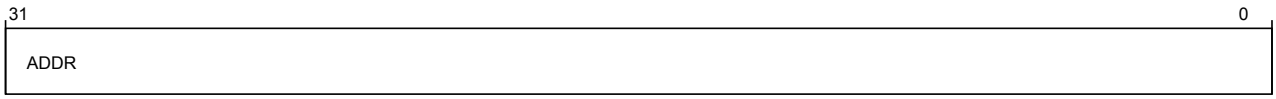


Figure 3-347 por_hnf_por_hnf_erraddr_ns (low)

The following table shows the por_hnf_erraddr_NS lower register bit assignments.

Table 3-361 por_hnf_por_hnf_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hnf_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

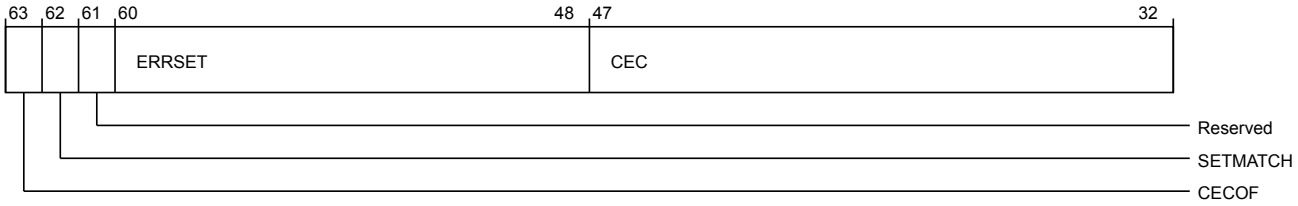


Figure 3-348 por_hnf_por_hnf_errmisc_ns (high)

The following table shows the por_hnf_errmisc_NS higher register bit assignments.

Table 3-362 por_hnf_por_hnf_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63	CECOF	Corrected error counter overflow	RW	1'b0
62	SETMATCH	Set address match	RW	1'b0
61	Reserved	Reserved	RO	-
60:48	ERRSET	SLC/SF set address for ECC error	RW	13'b0
47:32	CEC	Corrected ECC error count	RW	16'b0

The following image shows the lower register bit assignments.

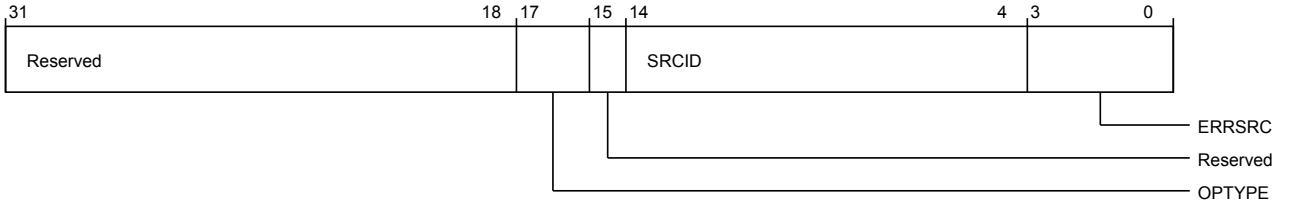


Figure 3-349 por_hnf_por_hnf_errmisc_ns (low)

The following table shows the por_hnf_errmisc_NS lower register bit assignments.

Table 3-363 por_hnf_por_hnf_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	OPTYPE	Error op type 2'b00: Writes, CleanShared, Atomics and stash requests with invalid targets 2'b01: WriteBack, Evict, and Stash requests with valid target 2'b10: CMO 2'b11: Other op types	RW	2'b00

Table 3-363 por_hnf_por_hnf_errmisc_ns (low) (continued)

Bits	Field name	Description	Type	Reset
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0001: Data single-bit ECC 4'b0010: Data double-bit ECC 4'b0011: Single-bit ECC overflow 4'b0100: Tag single-bit ECC 4'b0101: Tag double-bit ECC 4'b0111: SF tag single-bit ECC 4'b1000: SF tag double-bit ECC 4'b1010: Data parity error 4'b1011: Data parity and poison 4'b1100: NDE	RW	4'b0000

por_hnf_slc_lock_ways

Controls SLC way lock settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

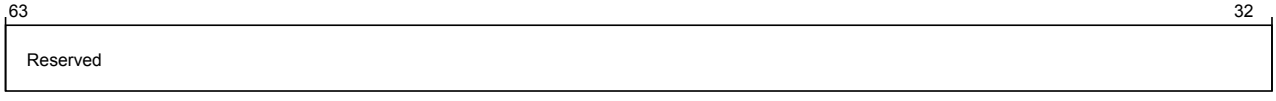


Figure 3-350 por_hnf_por_hnf_slc_lock_ways (high)

The following table shows the por_hnf_slc_lock_ways higher register bit assignments.

Table 3-364 por_hnf_por_hnf_slc_lock_ways (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

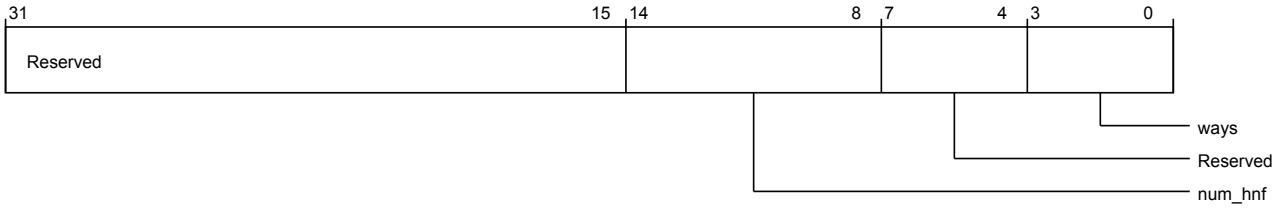


Figure 3-351 por_hnf_por_hnf_slc_lock_ways (low)

The following table shows the por_hnf_slc_lock_ways lower register bit assignments.

Table 3-365 por_hnf_por_hnf_slc_lock_ways (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:8	num_hnf	Number of HN-Fs in NUMA (non-uniform memory access) region	RW	Configuration dependent
7:4	Reserved	Reserved	RO	-
3:0	ways	Number of SLC ways locked (1, 2, 4, 8, 12)	RW	4'b0

por_hnf_slc_lock_base0

Functions as the base register for lock region 0 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

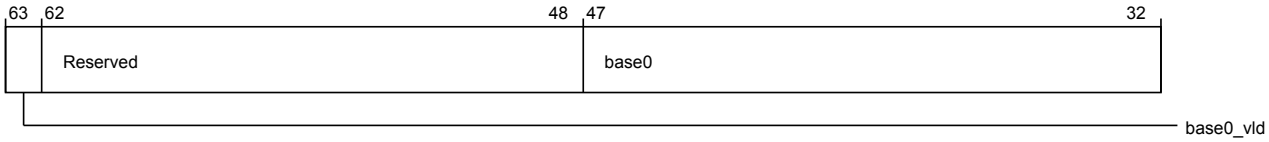


Figure 3-352 por_hnf_por_hnf_slc_lock_base0 (high)

The following table shows the por_hnf_slc_lock_base0 higher register bit assignments.

Table 3-366 por_hnf_por_hnf_slc_lock_base0 (high)

Bits	Field name	Description	Type	Reset
63	base0_vld	Lock region 0 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base0	Lock region 0 base address	RW	48'b0

The following image shows the lower register bit assignments.

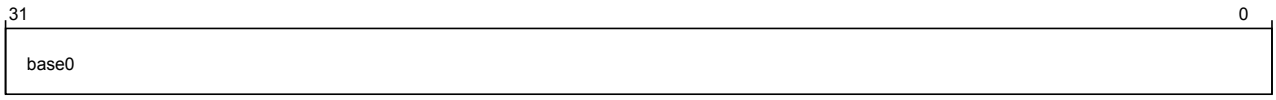


Figure 3-353 por_hnf_por_hnf_slc_lock_base0 (low)

The following table shows the por_hnf_slc_lock_base0 lower register bit assignments.

Table 3-367 por_hnf_por_hnf_slc_lock_base0 (low)

Bits	Field name	Description	Type	Reset
31:0	base0	Lock region 0 base address	RW	48'b0

por_hnf_slc_lock_base1

Functions as the base register for lock region 1 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

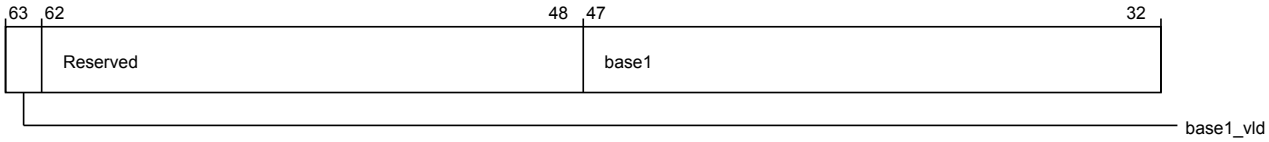


Figure 3-354 por_hnf_por_hnf_slc_lock_base1 (high)

The following table shows the por_hnf_slc_lock_base1 higher register bit assignments.

Table 3-368 por_hnf_por_hnf_slc_lock_base1 (high)

Bits	Field name	Description	Type	Reset
63	base1_vld	Lock region 1 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base1	Lock region 1 base address	RW	48'b0

The following image shows the lower register bit assignments.

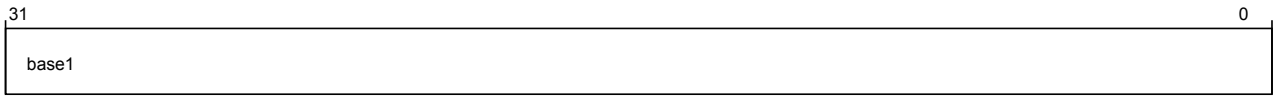


Figure 3-355 por_hnf_por_hnf_slc_lock_base1 (low)

The following table shows the por_hnf_slc_lock_base1 lower register bit assignments.

Table 3-369 por_hnf_por_hnf_slc_lock_base1 (low)

Bits	Field name	Description	Type	Reset
31:0	base1	Lock region 1 base address	RW	48'b0

por_hnf_slc_lock_base2

Functions as the base register for lock region 2 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

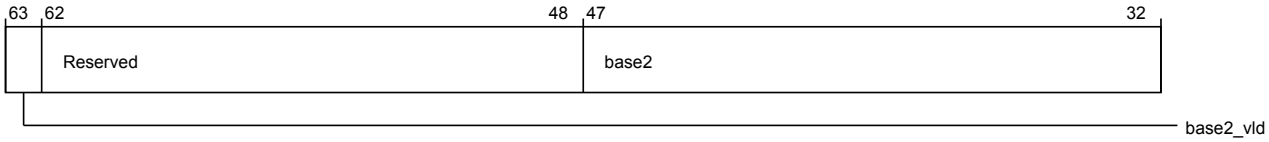


Figure 3-356 por_hnf_por_hnf_slc_lock_base2 (high)

The following table shows the por_hnf_slc_lock_base2 higher register bit assignments.

Table 3-370 por_hnf_por_hnf_slc_lock_base2 (high)

Bits	Field name	Description	Type	Reset
63	base2_vld	Lock region 2 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base2	Lock region 2 base address	RW	48'b0

The following image shows the lower register bit assignments.

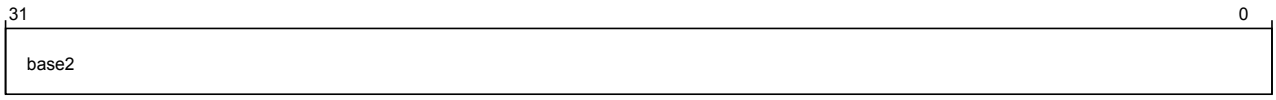


Figure 3-357 por_hnf_por_hnf_slc_lock_base2 (low)

The following table shows the por_hnf_slc_lock_base2 lower register bit assignments.

Table 3-371 por_hnf_por_hnf_slc_lock_base2 (low)

Bits	Field name	Description	Type	Reset
31:0	base2	Lock region 2 base address	RW	48'b0

por_hnf_slc_lock_base3

Functions as the base register for lock region 3 [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. The SLC must be flushed before writing to this register. Non-configuration accesses to this HN-F cannot occur before this configuration write and after the SLC flush.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

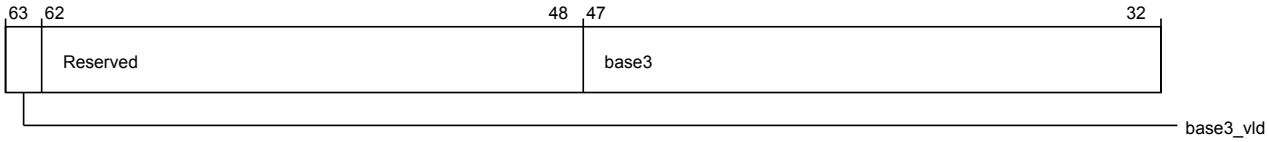


Figure 3-358 por_hnf_por_hnf_slc_lock_base3 (high)

The following table shows the por_hnf_slc_lock_base3 higher register bit assignments.

Table 3-372 por_hnf_por_hnf_slc_lock_base3 (high)

Bits	Field name	Description	Type	Reset
63	base3_vld	Lock region 3 base valid	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	base3	Lock region 3 base address	RW	48'b0

The following image shows the lower register bit assignments.

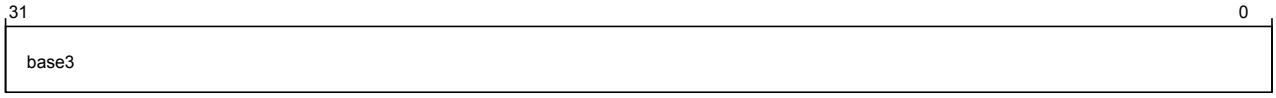


Figure 3-359 por_hnf_por_hnf_slc_lock_base3 (low)

The following table shows the por_hnf_slc_lock_base3 lower register bit assignments.

Table 3-373 por_hnf_por_hnf_slc_lock_base3 (low)

Bits	Field name	Description	Type	Reset
31:0	base3	Lock region 3 base address	RW	48'b0

por_hnf_rni_region_vec

Functions as the control register for RN-I source SLC way allocation.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

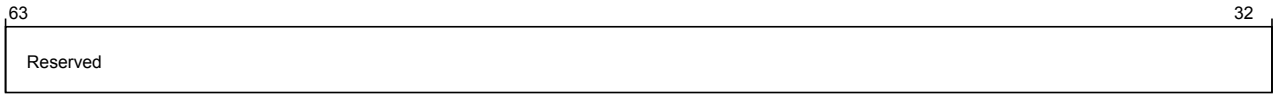


Figure 3-360 por_hnf_por_hnf_rni_region_vec (high)

The following table shows the por_hnf_rni_region_vec higher register bit assignments.

Table 3-374 por_hnf_por_hnf_rni_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

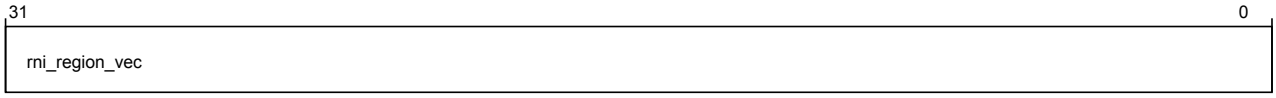


Figure 3-361 por_hnf_por_hnf_rni_region_vec (low)

The following table shows the por_hnf_rni_region_vec lower register bit assignments.

Table 3-375 por_hnf_por_hnf_rni_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_region_vec	Bit vector mask; identifies which logical IDs of the RN-Is to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

por_hnf_rnf_region_vec

Functions as the control register for RN-F source SLC way allocation.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC38
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

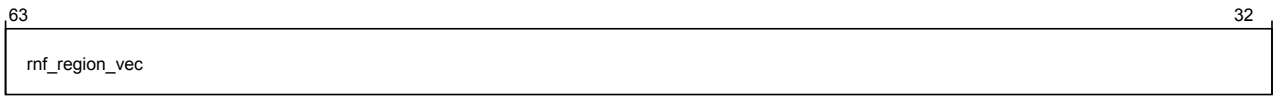


Figure 3-362 por_hnf_por_hnf_rnf_region_vec (high)

The following table shows the por_hnf_rnf_region_vec higher register bit assignments.

Table 3-376 por_hnf_por_hnf_rnf_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following image shows the lower register bit assignments.

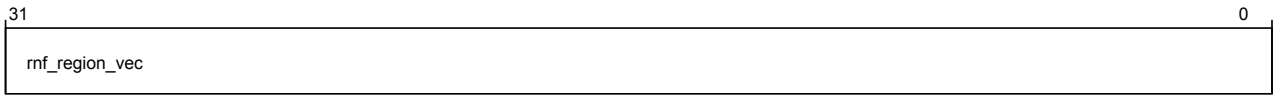


Figure 3-363 por_hnf_por_hnf_rnf_region_vec (low)

The following table shows the por_hnf_rnf_region_vec lower register bit assignments.

Table 3-377 por_hnf_por_hnf_rnf_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_region_vec	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

por_hnf_rnd_region_vec

Functions as the control register for RN-D source SLC way allocation.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

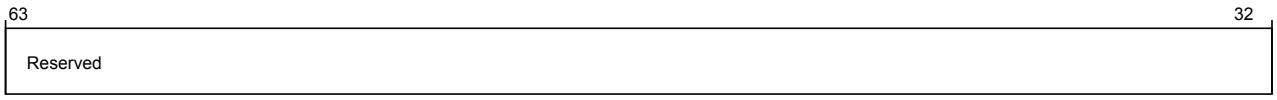


Figure 3-364 por_hnf_por_hnf_rnd_region_vec (high)

The following table shows the por_hnf_rnd_region_vec higher register bit assignments.

Table 3-378 por_hnf_por_hnf_rnd_region_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

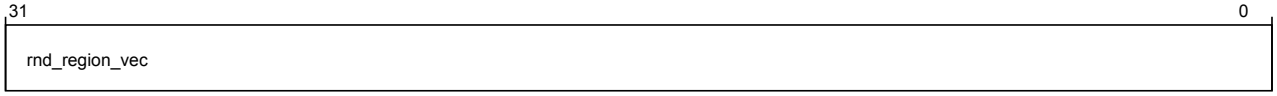


Figure 3-365 por_hnf_por_hnf_rnd_region_vec (low)

The following table shows the por_hnf_rnd_region_vec lower register bit assignments.

Table 3-379 por_hnf_por_hnf_rnd_region_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_region_vec	Bit vector mask; identifies which logical IDs of the RN-Ds to allocate to the locked region NOTE: Must be set to 32'b0 if range-based region locking or OCM is enabled.	RW	32'b0

por_hnf_slcway_partition0_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

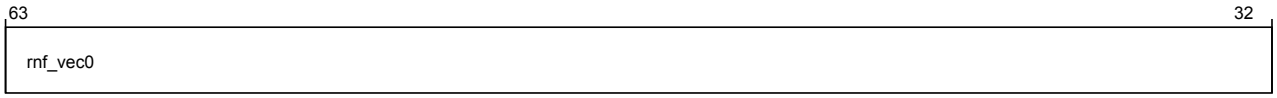


Figure 3-366 por_hnf_por_hnf_slcway_partition0_rnf_vec (high)

The following table shows the por_hnf_slcway_partition0_rnf_vec higher register bit assignments.

Table 3-380 por_hnf_por_hnf_slcway_partition0_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

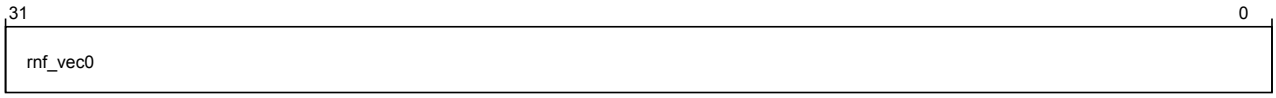


Figure 3-367 por_hnf_por_hnf_slcway_partition0_rnf_vec (low)

The following table shows the por_hnf_slcway_partition0_rnf_vec lower register bit assignments.

Table 3-381 por_hnf_por_hnf_slcway_partition0_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec0	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition1_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

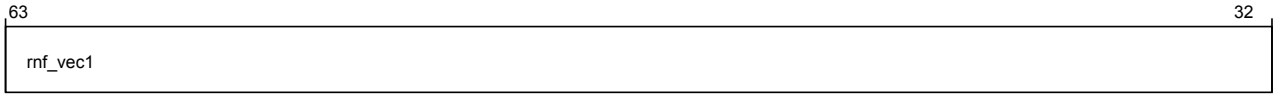


Figure 3-368 por_hnf_por_hnf_slcway_partition1_rnf_vec (high)

The following table shows the por_hnf_slcway_partition1_rnf_vec higher register bit assignments.

Table 3-382 por_hnf_por_hnf_slcway_partition1_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

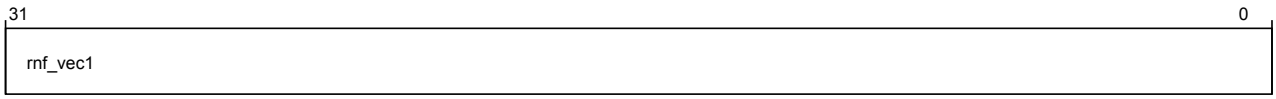


Figure 3-369 por_hnf_por_hnf_slcway_partition1_rnf_vec (low)

The following table shows the por_hnf_slcway_partition1_rnf_vec lower register bit assignments.

Table 3-383 por_hnf_por_hnf_slcway_partition1_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec1	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition2_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

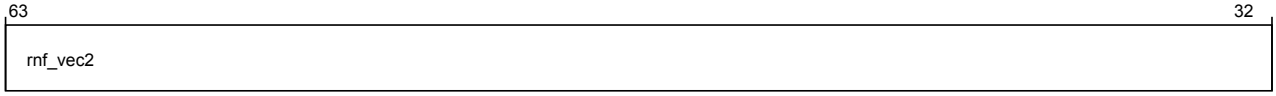


Figure 3-370 por_hnf_por_hnf_slcway_partition2_rnf_vec (high)

The following table shows the por_hnf_slcway_partition2_rnf_vec higher register bit assignments.

Table 3-384 por_hnf_por_hnf_slcway_partition2_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

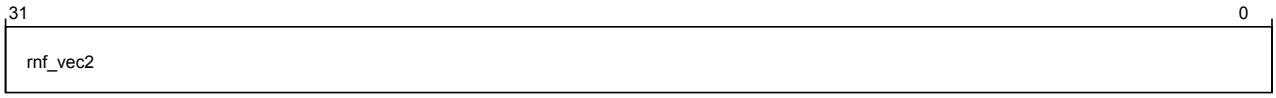


Figure 3-371 por_hnf_por_hnf_slcway_partition2_rnf_vec (low)

The following table shows the por_hnf_slcway_partition2_rnf_vec lower register bit assignments.

Table 3-385 por_hnf_por_hnf_slcway_partition2_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec2	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition3_rnf_vec

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

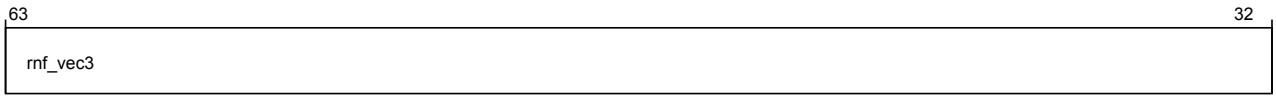


Figure 3-372 por_hnf_por_hnf_slcway_partition3_rnf_vec (high)

The following table shows the por_hnf_slcway_partition3_rnf_vec higher register bit assignments.

Table 3-386 por_hnf_por_hnf_slcway_partition3_rnf_vec (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

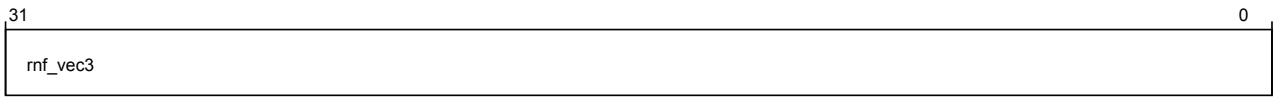


Figure 3-373 por_hnf_por_hnf_slcway_partition3_rnf_vec (low)

The following table shows the por_hnf_slcway_partition3_rnf_vec lower register bit assignments.

Table 3-387 por_hnf_por_hnf_slcway_partition3_rnf_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec3	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_rnf_region_vec1

Functions as the control register for RN-sF source SLC way allocation for logical ID's 64 through 127s.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

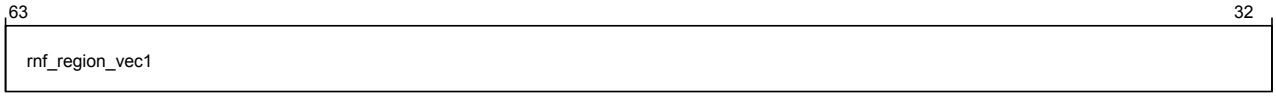


Figure 3-374 por_hnf_por_hnf_rnf_region_vec1 (high)

The following table shows the por_hnf_rnf_region_vec1 higher register bit assignments.

Table 3-388 por_hnf_por_hnf_rnf_region_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

The following image shows the lower register bit assignments.

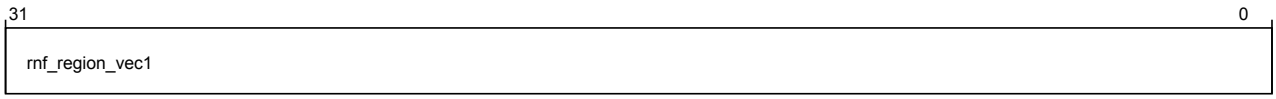


Figure 3-375 por_hnf_por_hnf_rnf_region_vec1 (low)

The following table shows the por_hnf_rnf_region_vec1 lower register bit assignments.

Table 3-389 por_hnf_por_hnf_rnf_region_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_region_vec1	Bit vector mask; identifies which logical IDs of the RN-Fs to allocate to the locked region NOTE: Must be 64'b0 if range-based region locking or OCM is enabled.	RW	64'b0

por_hnf_slcway_partition0_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB0

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

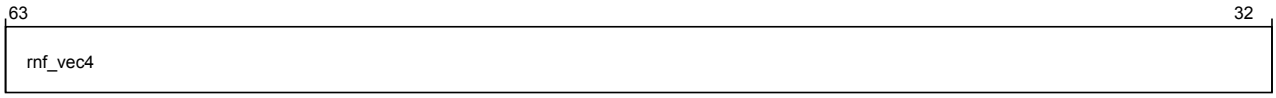


Figure 3-376 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)

The following table shows the por_hnf_slcway_partition0_rnf_vec1 higher register bit assignments.

Table 3-390 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

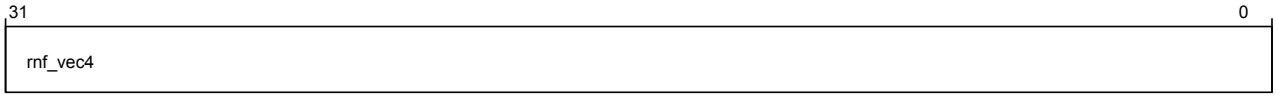


Figure 3-377 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (low)

The following table shows the por_hnf_slcway_partition0_rnf_vec1 lower register bit assignments.

Table 3-391 por_hnf_por_hnf_slcway_partition0_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec4	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition1_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 1 (ways 4, 5, 6, and 7) for Logical RNF ID's 64 to 127.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCB8

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

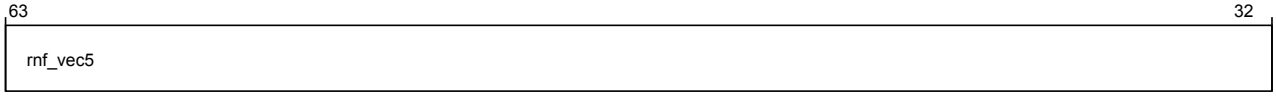


Figure 3-378 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)

The following table shows the por_hnf_slcway_partition1_rnf_vec1 higher register bit assignments.

Table 3-392 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

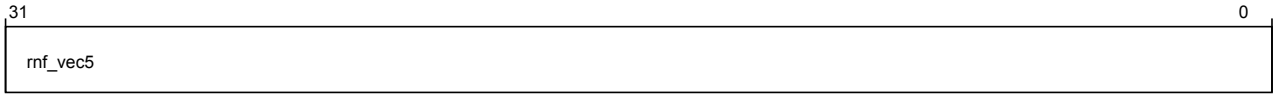


Figure 3-379 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (low)

The following table shows the por_hnf_slcway_partition1_rnf_vec1 lower register bit assignments.

Table 3-393 por_hnf_por_hnf_slcway_partition1_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec5	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition2_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 2 (ways 8, 9, 10, and 11) for Logical RNF ID's 64 to 127.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCC0

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

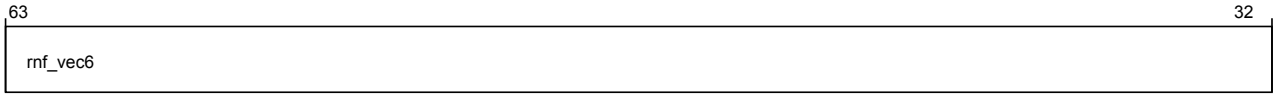


Figure 3-380 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (high)

The following table shows the por_hnf_slcway_partition2_rnf_vec1 higher register bit assignments.

Table 3-394 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

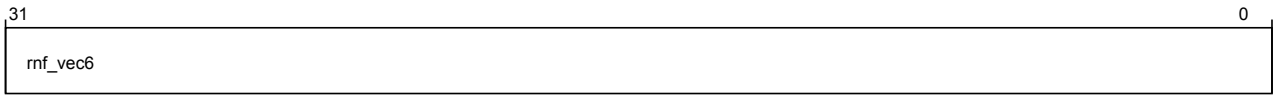


Figure 3-381 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)

The following table shows the por_hnf_slcway_partition2_rnf_vec1 lower register bit assignments.

Table 3-395 por_hnf_por_hnf_slcway_partition2_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec6	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition3_rnf_vec1

Functions as the control register for RN-Fs that can allocate to partition 3 (ways 12, 13, 14, and 15) for Logical RNF ID's 64 to 127.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCC8

Register reset 64'b1111111111111111111111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

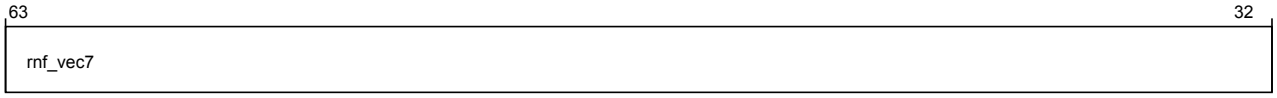


Figure 3-382 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (high)

The following table shows the por_hnf_slcway_partition3_rnf_vec1 higher register bit assignments.

Table 3-396 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (high)

Bits	Field name	Description	Type	Reset
63:32	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

The following image shows the lower register bit assignments.

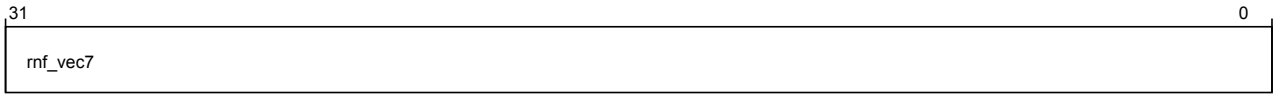


Figure 3-383 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)

The following table shows the por_hnf_slcway_partition3_rnf_vec1 lower register bit assignments.

Table 3-397 por_hnf_por_hnf_slcway_partition3_rnf_vec1 (low)

Bits	Field name	Description	Type	Reset
31:0	rnf_vec7	Bit vector mask; identifies which logical IDs of the RN-F can allocate	RW	64'hFFFFFFFFFFFFFFFF

por_hnf_slcway_partition0_rni_vec

Functions as the control register for RN-Is that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC68

Register reset 64'b11111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

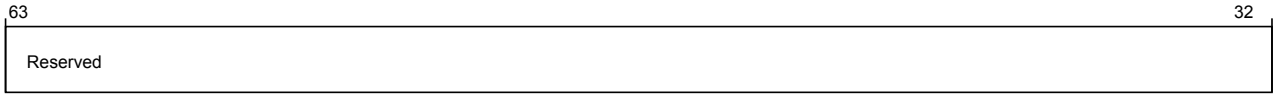


Figure 3-384 por_hnf_por_hnf_slcway_partition0_rni_vec (high)

The following table shows the por_hnf_slcway_partition0_rni_vec higher register bit assignments.

Table 3-398 por_hnf_por_hnf_slcway_partition0_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

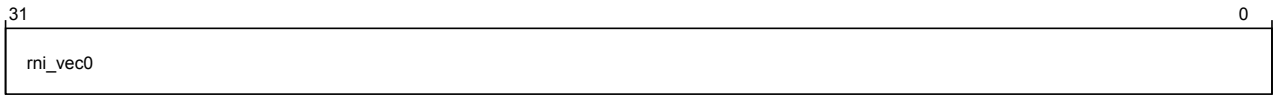


Figure 3-385 por_hnf_por_hnf_slcway_partition0_rni_vec (low)

The following table shows the por_hnf_slcway_partition0_rni_vec lower register bit assignments.

Table 3-399 por_hnf_por_hnf_slcway_partition0_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition1_rni_vec

Functions as the control register for RN-Is that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

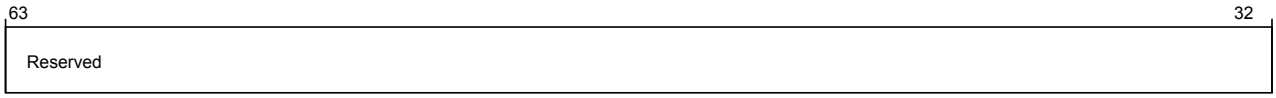


Figure 3-386 por_hnf_por_hnf_slcway_partition1_rni_vec (high)

The following table shows the por_hnf_slcway_partition1_rni_vec higher register bit assignments.

Table 3-400 por_hnf_por_hnf_slcway_partition1_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

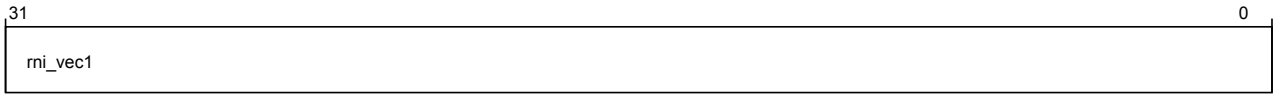


Figure 3-387 por_hnf_por_hnf_slcway_partition1_rni_vec (low)

The following table shows the por_hnf_slcway_partition1_rni_vec lower register bit assignments.

Table 3-401 por_hnf_por_hnf_slcway_partition1_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition2_rni_vec

Functions as the control register for RN-Is that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

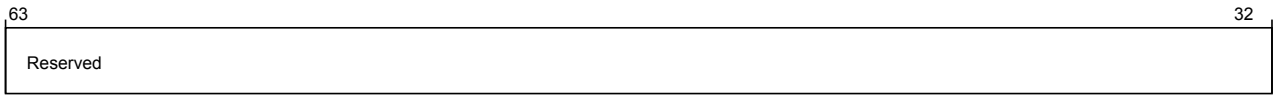


Figure 3-388 por_hnf_por_hnf_slcway_partition2_rni_vec (high)

The following table shows the por_hnf_slcway_partition2_rni_vec higher register bit assignments.

Table 3-402 por_hnf_por_hnf_slcway_partition2_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

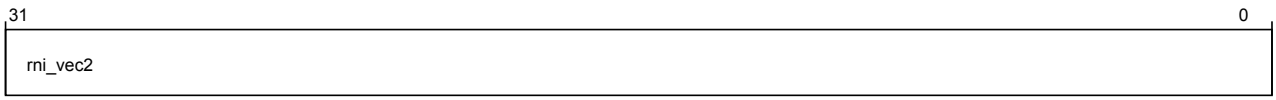


Figure 3-389 por_hnf_por_hnf_slcway_partition2_rni_vec (low)

The following table shows the por_hnf_slcway_partition2_rni_vec lower register bit assignments.

Table 3-403 por_hnf_por_hnf_slcway_partition2_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition3_rni_vec

Functions as the control register for RN-Is that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC80

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

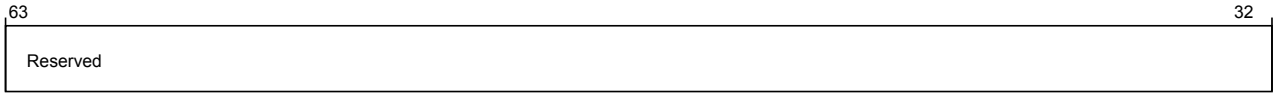


Figure 3-390 por_hnf_por_hnf_slcway_partition3_rni_vec (high)

The following table shows the por_hnf_slcway_partition3_rni_vec higher register bit assignments.

Table 3-404 por_hnf_por_hnf_slcway_partition3_rni_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

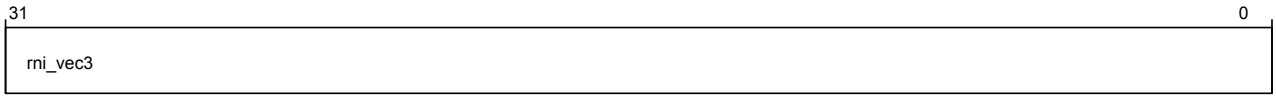


Figure 3-391 por_hnf_por_hnf_slcway_partition3_rni_vec (low)

The following table shows the por_hnf_slcway_partition3_rni_vec lower register bit assignments.

Table 3-405 por_hnf_por_hnf_slcway_partition3_rni_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rni_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition0_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 0 (ways 0, 1, 2, and 3).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC88

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

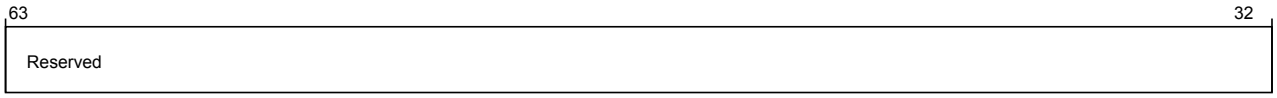


Figure 3-392 por_hnf_por_hnf_slcway_partition0_rnd_vec (high)

The following table shows the por_hnf_slcway_partition0_rnd_vec higher register bit assignments.

Table 3-406 por_hnf_por_hnf_slcway_partition0_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

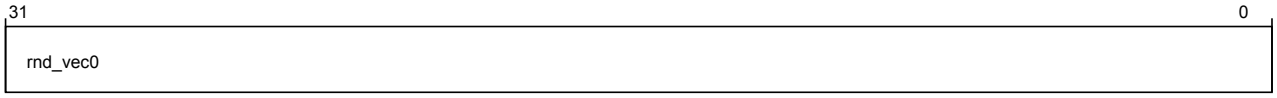


Figure 3-393 por_hnf_por_hnf_slcway_partition0_rnd_vec (low)

The following table shows the por_hnf_slcway_partition0_rnd_vec lower register bit assignments.

Table 3-407 por_hnf_por_hnf_slcway_partition0_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec0	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition1_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 1 (ways 4, 5, 6, and 7).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC90

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

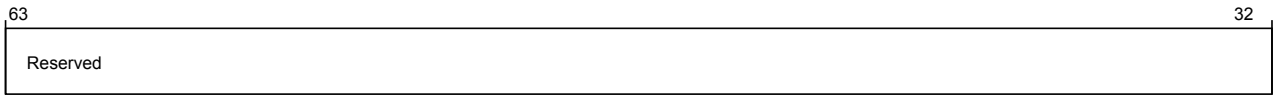


Figure 3-394 por_hnf_por_hnf_slcway_partition1_rnd_vec (high)

The following table shows the por_hnf_slcway_partition1_rnd_vec higher register bit assignments.

Table 3-408 por_hnf_por_hnf_slcway_partition1_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

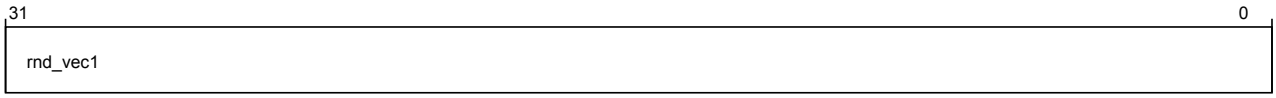


Figure 3-395 por_hnf_por_hnf_slcway_partition1_rnd_vec (low)

The following table shows the por_hnf_slcway_partition1_rnd_vec lower register bit assignments.

Table 3-409 por_hnf_por_hnf_slcway_partition1_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec1	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition2_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 2 (ways 8, 9, 10, and 11).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC98

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

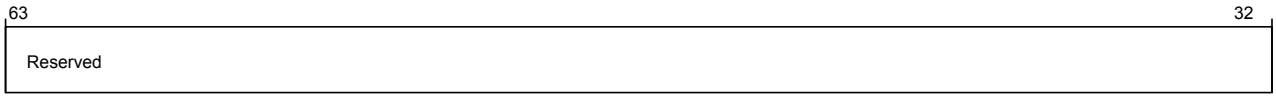


Figure 3-396 por_hnf_por_hnf_slcway_partition2_rnd_vec (high)

The following table shows the por_hnf_slcway_partition2_rnd_vec higher register bit assignments.

Table 3-410 por_hnf_por_hnf_slcway_partition2_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

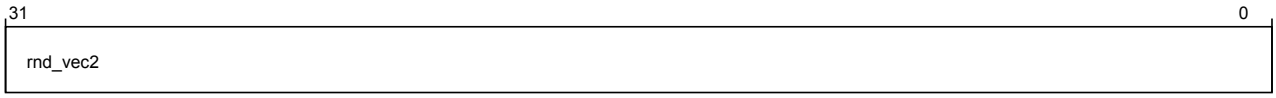


Figure 3-397 por_hnf_por_hnf_slcway_partition2_rnd_vec (low)

The following table shows the por_hnf_slcway_partition2_rnd_vec lower register bit assignments.

Table 3-411 por_hnf_por_hnf_slcway_partition2_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec2	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_slcway_partition3_rnd_vec

Functions as the control register for RN-Ds that can allocate to partition 3 (ways 12, 13, 14, and 15).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCA0

Register reset 64'b1111111111111111111111111111111

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

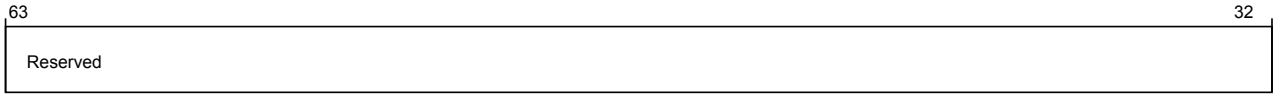


Figure 3-398 por_hnf_por_hnf_slcway_partition3_rnd_vec (high)

The following table shows the por_hnf_slcway_partition3_rnd_vec higher register bit assignments.

Table 3-412 por_hnf_por_hnf_slcway_partition3_rnd_vec (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

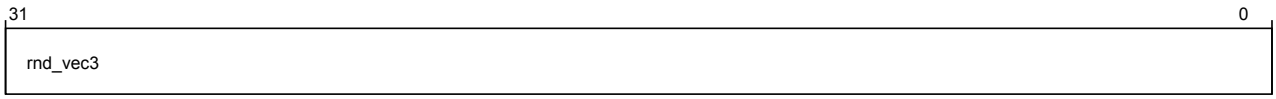


Figure 3-399 por_hnf_por_hnf_slcway_partition3_rnd_vec (low)

The following table shows the por_hnf_slcway_partition3_rnd_vec lower register bit assignments.

Table 3-413 por_hnf_por_hnf_slcway_partition3_rnd_vec (low)

Bits	Field name	Description	Type	Reset
31:0	rnd_vec3	Bit vector mask; identifies which logical IDs of the RN-I/RN-D can allocate	RW	32'hFFFFFFFF

por_hnf_rn_region_lock

Functions as the enable register for source-based SLC way allocation.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slc_lock_ways

The following image shows the higher register bit assignments.

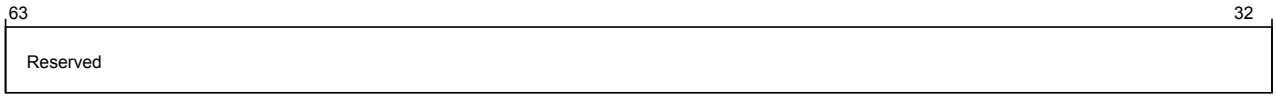


Figure 3-400 por_hnf_por_hnf_rn_region_lock (high)

The following table shows the por_hnf_rn_region_lock higher register bit assignments.

Table 3-414 por_hnf_por_hnf_rn_region_lock (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

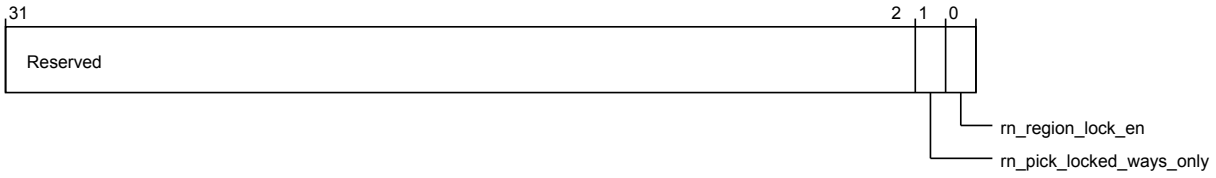


Figure 3-401 por_hnf_por_hnf_rn_region_lock (low)

The following table shows the por_hnf_rn_region_lock lower register bit assignments.

Table 3-415 por_hnf_por_hnf_rn_region_lock (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	rn_pick_locked_ways_only	Specifies which ways the programmed RNs can allocate new cache lines to 1'b0: Programmed RN will choose all ways including locked 1'b1: Programmed RN will only allocate in locked ways	RW	1'b0
0	rn_region_lock_en	Enables SRC-based region locking 1'b0: SRC based way locking is disabled 1'b1: SRC based way locking is enabled	RW	1'b0

por_hnf_sam_control

Configures HN-F SAM. All top_address_bit fields must be between bits 47 and 28 of the address. top_address_bit2 > top_address_bit1 > top_address_bit0. Must be configured to match corresponding por_rnsam_sys_cache_grp_sn_sam_cfgN register in the RN SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

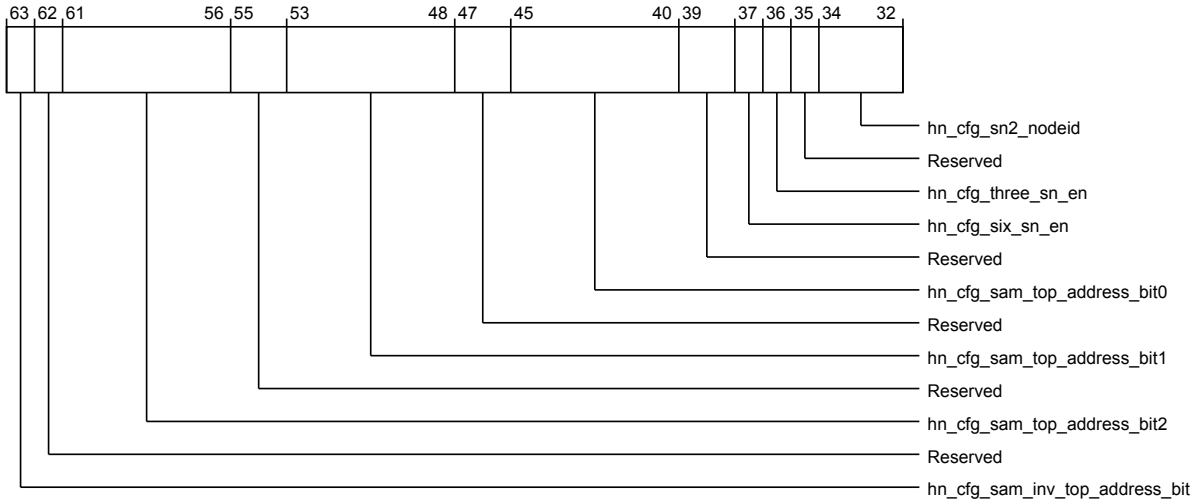


Figure 3-402 por_hnf_por_hnf_sam_control (high)

The following table shows the por_hnf_sam_control higher register bit assignments.

Table 3-416 por_hnf_por_hnf_sam_control (high)

Bits	Field name	Description	Type	Reset
63	hn_cfg_sam_inv_top_address_bit	Inverts the top address bit (hn_cfg_sam_top_address_bit1 if 3-SN, hn_cfg_sam_top_address_bit2 if 6-SN) NOTE: Can only be used when the address map does not have unique address bit combinations.	RW	1'h0
62	Reserved	Reserved	RO	-
61:56	hn_cfg_sam_top_address_bit2	Bit position of top_address_bit2; used for address hashing in 6-SN configuration	RW	6'h00
55:54	Reserved	Reserved	RO	-
53:48	hn_cfg_sam_top_address_bit1	Bit position of top_address_bit1; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
47:46	Reserved	Reserved	RO	-
45:40	hn_cfg_sam_top_address_bit0	Bit position of top_address_bit0; used for address hashing in 3-SN/6-SN configuration	RW	6'h00
39:38	Reserved	Reserved	RO	-
37	hn_cfg_six_sn_en	Enables 6-SN configuration	RW	1'b0
36	hn_cfg_three_sn_en	Enables 3-SN configuration	RW	1'b0
35	Reserved	Reserved	RO	-
34:32	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0

The following image shows the lower register bit assignments.

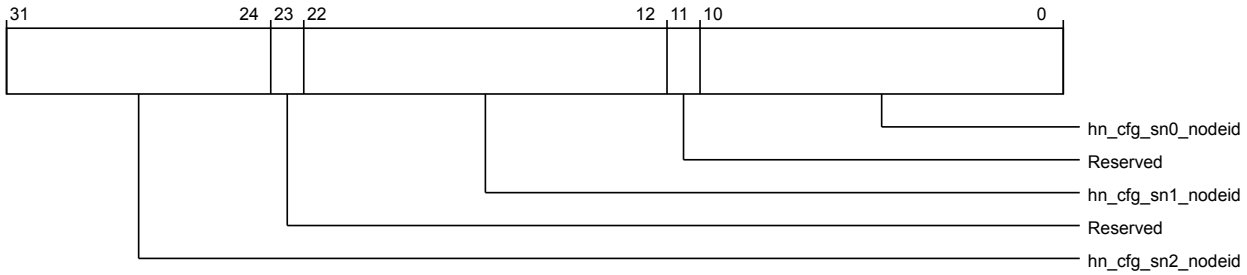


Figure 3-403 por_hnf_por_hnf_sam_control (low)

The following table shows the por_hnf_sam_control lower register bit assignments.

Table 3-417 por_hnf_por_hnf_sam_control (low)

Bits	Field name	Description	Type	Reset
31:24	hn_cfg_sn2_nodeid	SN 2 node ID	RW	11'h0
23	Reserved	Reserved	RO	-

Table 3-417 por_hnf_por_hnf_sam_control (low) (continued)

Bits	Field name	Description	Type	Reset
22:12	hn_cfg_sn1_nodeid	SN 1 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	hn_cfg_sn0_nodeid	SN 0 node ID	RW	11'h0

por_hnf_sam_memregion0

Configures range-based memory region 0 in HN-F SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

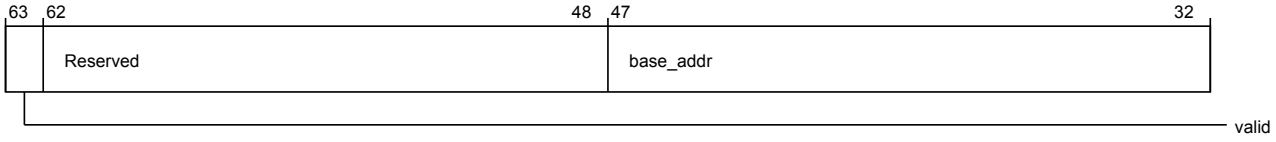


Figure 3-404 por_hnf_por_hnf_sam_memregion0 (high)

The following table shows the por_hnf_sam_memregion0 higher register bit assignments.

Table 3-418 por_hnf_por_hnf_sam_memregion0 (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:48	Reserved	Reserved	RO	-
47:32	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0

The following image shows the lower register bit assignments.

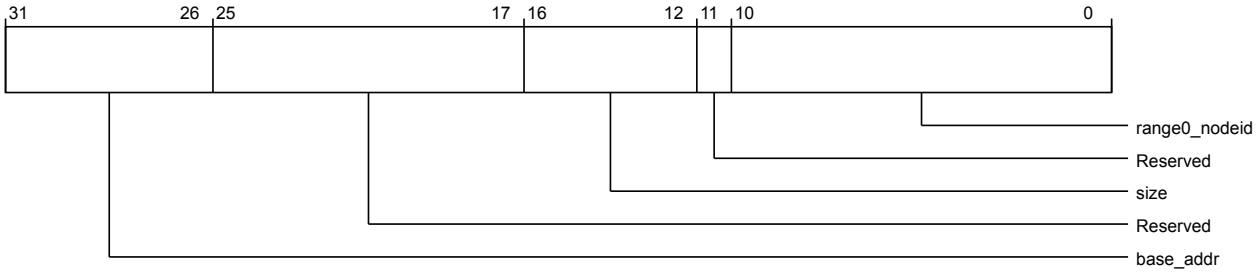


Figure 3-405 por_hnf_por_hnf_sam_memregion0 (low)

The following table shows the por_hnf_sam_memregion0 lower register bit assignments.

Table 3-419 por_hnf_por_hnf_sam_memregion0 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 0 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'h0
11	Reserved	Reserved	RO	-
10:0	range0_nodeid	Memory region 0 target node ID	RW	11'h0

por_hnf_sam_memregion1

Configures range-based memory region 1 in HN-F SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

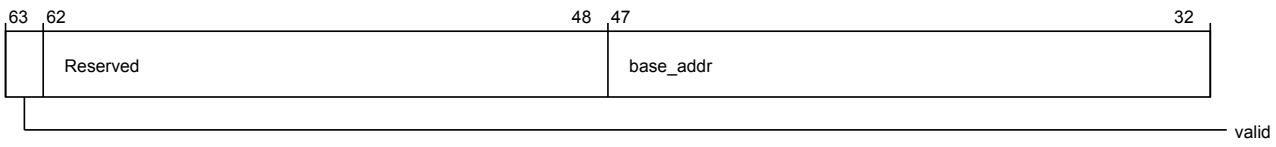


Figure 3-406 por_hnf_por_hnf_sam_memregion1 (high)

The following table shows the por_hnf_sam_memregion1 higher register bit assignments.

Table 3-420 por_hnf_por_hnf_sam_memregion1 (high)

Bits	Field name	Description	Type	Reset
63	valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'h0
62:48	Reserved	Reserved	RO	-
47:32	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0

The following image shows the lower register bit assignments.

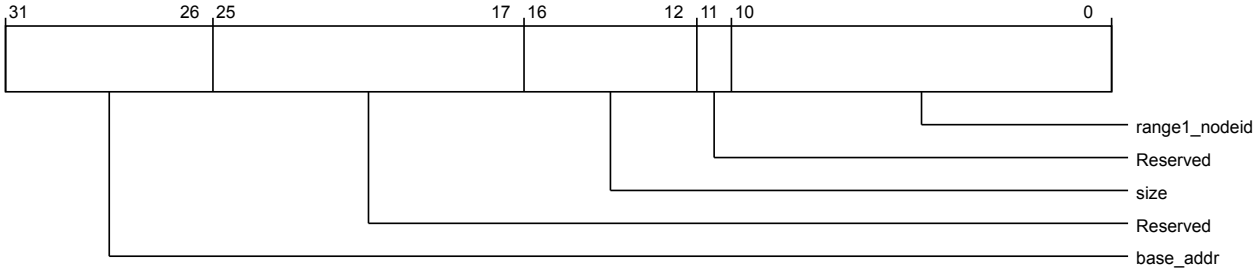


Figure 3-407 por_hnf_por_hnf_sam_memregion1 (low)

The following table shows the por_hnf_sam_memregion1 lower register bit assignments.

Table 3-421 por_hnf_por_hnf_sam_memregion1 (low)

Bits	Field name	Description	Type	Reset
31:26	base_addr	Base address of memory region 1 CONSTRAINT: Must be an integer multiple of region size.	RW	22'h0
25:17	Reserved	Reserved	RO	-
16:12	size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'h0
11	Reserved	Reserved	RO	-
10:0	range1_nodeid	Memory region 1 target node ID	RW	11'h0

por_hnf_sam_sn_properties

Configures properties for all six SN targets and two range-based SN targets.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'hD18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

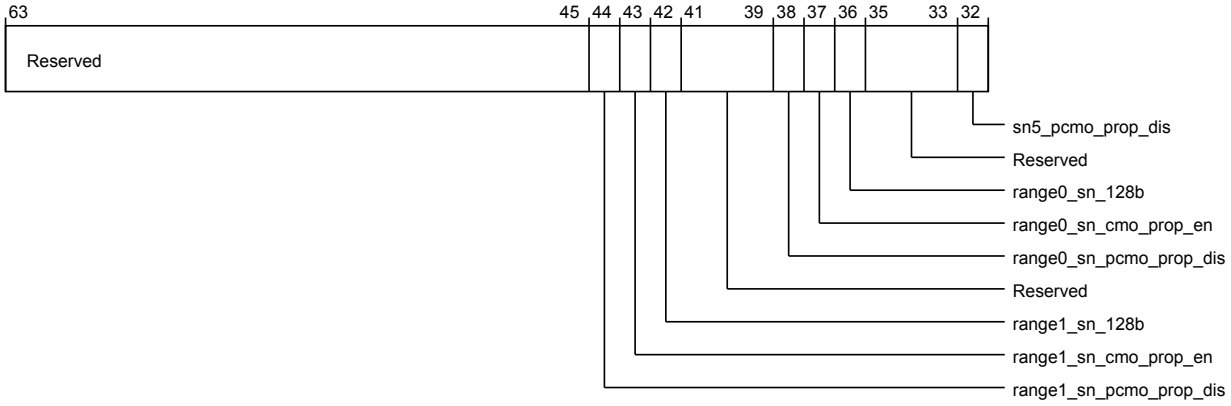


Figure 3-408 por_hnf_por_hnf_sam_sn_properties (high)

The following table shows the por_hnf_sam_sn_properties higher register bit assignments.

Table 3-422 por_hnf_por_hnf_sam_sn_properties (high)

Bits	Field name	Description	Type	Reset
63:45	Reserved	Reserved	RO	-
44	range1_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 1 SN when set	RW	1'b0
43	range1_sn_cmo_prop_en	Enables CMO propagation for range 1 SN	RW	1'b0
42	range1_sn_128b	Data width of range 1 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
41:39	Reserved	Reserved	RO	-
38	range0_sn_pcmo_prop_dis	Disables PCMO (persistent CMO) propagation for range 0 SN when set	RW	1'b0
37	range0_sn_cmo_prop_en	Enables CMO propagation for range 0 SN	RW	1'b0
36	range0_sn_128b	Data width of range 0 SN 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
35:33	Reserved	Reserved	RO	-
32	sn5_pcmo_prop_dis	Disables PCMO propagation for SN 5 when set	RW	1'b0

The following image shows the lower register bit assignments.

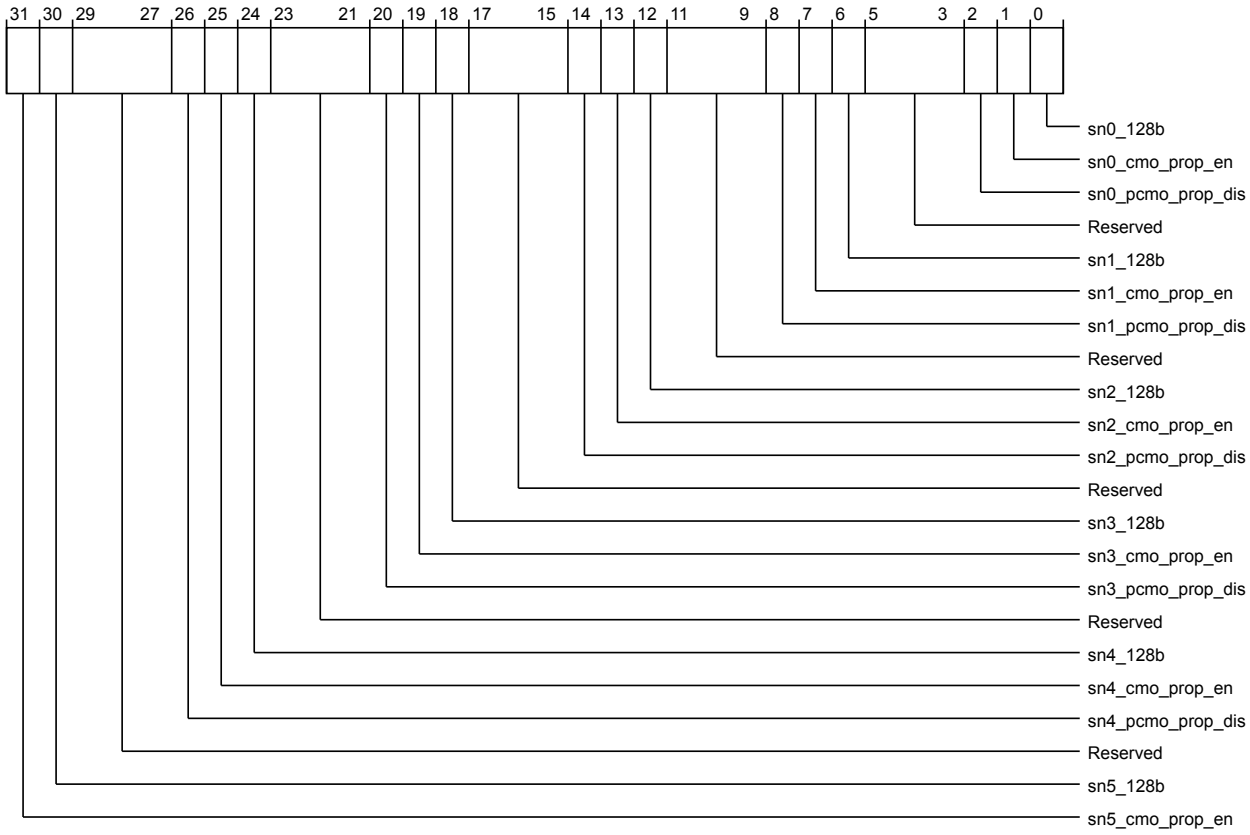


Figure 3-409 por_hnf_por_hnf_sam_sn_properties (low)

The following table shows the por_hnf_sam_sn_properties lower register bit assignments.

Table 3-423 por_hnf_por_hnf_sam_sn_properties (low)

Bits	Field name	Description	Type	Reset
31	sn5_cmo_prop_en	Enables CMO propagation for SN 5 when set	RW	1'b0
30	sn5_128b	Data width of SN 5 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
29:27	Reserved	Reserved	RO	-
26	sn4_pcmo_prop_dis	Disables PCMO propagation for SN 4 when set	RW	1'b0
25	sn4_cmo_prop_en	Enables CMO propagation for SN 4 when set	RW	1'b0
24	sn4_128b	Data width of SN 4 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
23:21	Reserved	Reserved	RO	-

Table 3-423 por_hnf_por_hnf_sam_sn_properties (low) (continued)

Bits	Field name	Description	Type	Reset
20	sn3_pcmo_prop_dis	Disables PCMO propagation for SN 3 when set	RW	1'b0
19	sn3_cmo_prop_en	Enables CMO propagation for SN 3 when set	RW	1'b0
18	sn3_128b	Data width of SN 3 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
17:15	Reserved	Reserved	RO	-
14	sn2_pcmo_prop_dis	Disables PCMO propagation for SN 2 when set	RW	1'b0
13	sn2_cmo_prop_en	Enables CMO propagation for SN 2 when set	RW	1'b0
12	sn2_128b	Data width of SN 2 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
11:9	Reserved	Reserved	RO	-
8	sn1_pcmo_prop_dis	Disables PCMO propagation for SN 1 when set	RW	1'b0
7	sn1_cmo_prop_en	Enables CMO propagation for SN 1 when set	RW	1'b0
6	sn1_128b	Data width of SN 1 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0
5:3	Reserved	Reserved	RO	-
2	sn0_pcmo_prop_dis	Disables PCMO propagation for SN 0 when set	RW	1'b0
1	sn0_cmo_prop_en	Enables CMO propagation for SN 0 when set	RW	1'b0
0	sn0_128b	Data width of SN 0 1'b1: 128 bits 1'b0: 256 bits	RW	1'b0

por_hnf_sam_6sn_nodeid

Configures node IDs for slave nodes 3 to 5 in 6-SN configuration mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD20
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

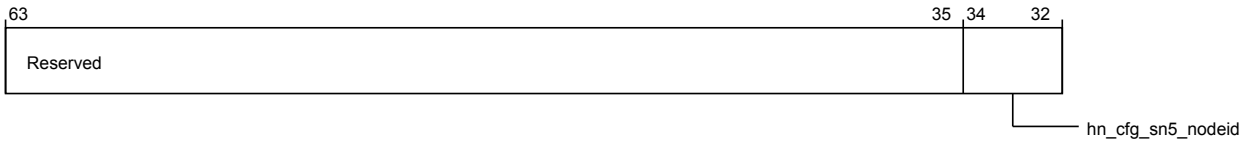


Figure 3-410 por_hnf_por_hnf_sam_6sn_nodeid (high)

The following table shows the por_hnf_sam_6sn_nodeid higher register bit assignments.

Table 3-424 por_hnf_por_hnf_sam_6sn_nodeid (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	hn_cfg_sn5_nodeid	SN 5 node ID	RW	11'h0

The following image shows the lower register bit assignments.

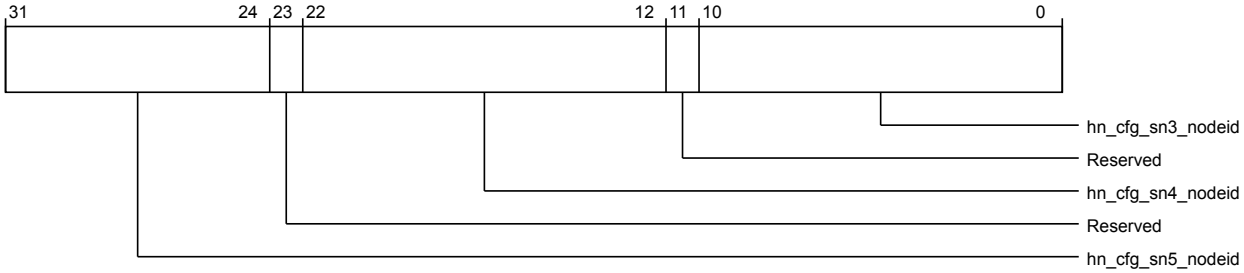


Figure 3-411 por_hnf_por_hnf_sam_6sn_nodeid (low)

The following table shows the por_hnf_sam_6sn_nodeid lower register bit assignments.

Table 3-425 por_hnf_por_hnf_sam_6sn_nodeid (low)

Bits	Field name	Description	Type	Reset
31:24	hn_cfg_sn5_nodeid	SN 5 node ID	RW	11'h0
23	Reserved	Reserved	RO	-
22:12	hn_cfg_sn4_nodeid	SN 4 node ID	RW	11'h0
11	Reserved	Reserved	RO	-
10:0	hn_cfg_sn3_nodeid	SN 3 node ID	RW	11'h0

por_hnf_rn_phys_id0

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hD28
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.
Secure group override	por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

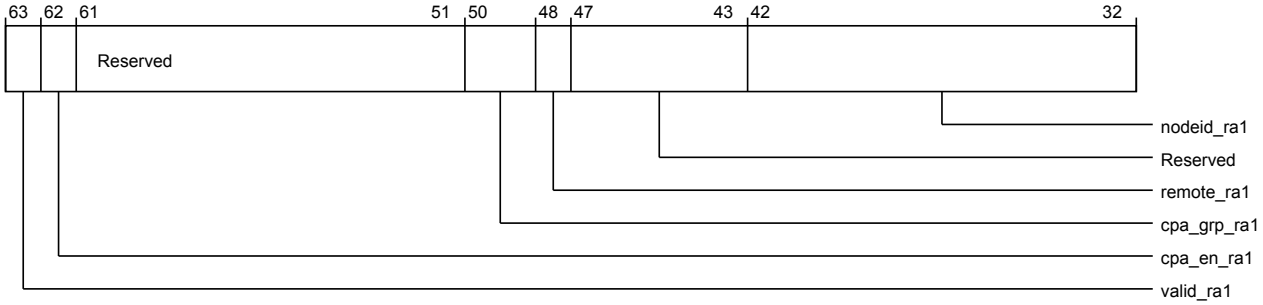


Figure 3-412 por_hnf_por_hnf_rn_phys_id0 (high)

The following table shows the por_hnf_rn_phys_id0 higher register bit assignments.

Table 3-426 por_hnf_por_hnf_rn_phys_id0 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra1	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra1	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra1	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra1	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0

Table 3-426 por_hnf_por_hnf_rn_phys_id0 (high) (continued)

Bits	Field name	Description	Type	Reset
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra1	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

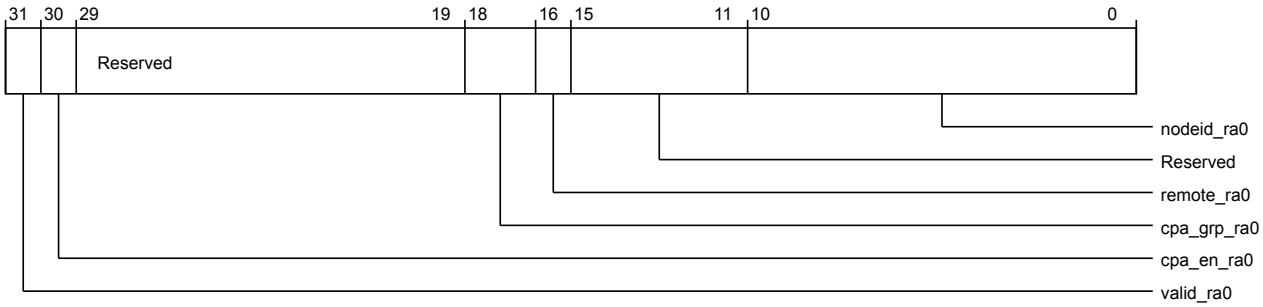


Figure 3-413 por_hnf_por_hnf_rn_phys_id0 (low)

The following table shows the por_hnf_rn_phys_id0 lower register bit assignments.

Table 3-427 por_hnf_por_hnf_rn_phys_id0 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra0	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra0	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra0	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra0	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra0	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id1

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

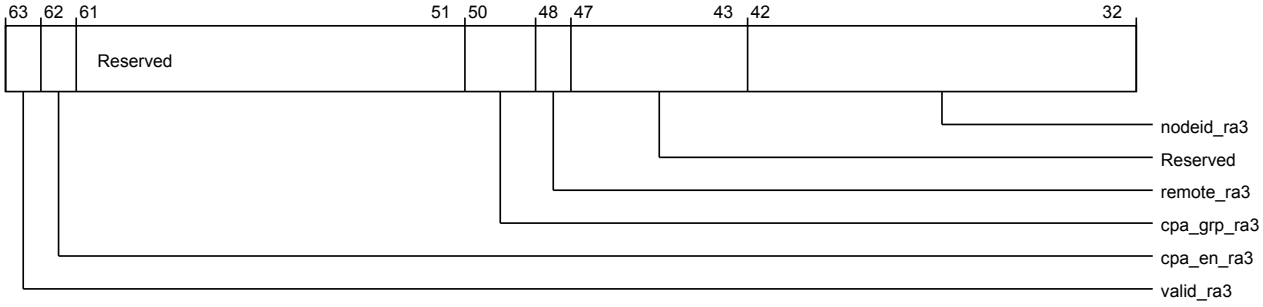


Figure 3-414 por_hnf_por_hnf_rn_phys_id1 (high)

The following table shows the por_hnf_rn_phys_id1 higher register bit assignments.

Table 3-428 por_hnf_por_hnf_rn_phys_id1 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra3	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra3	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra3	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0

Table 3-428 por_hnf_por_hnf_rn_phys_id1 (high) (continued)

Bits	Field name	Description	Type	Reset
48	remote_ra3	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra3	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

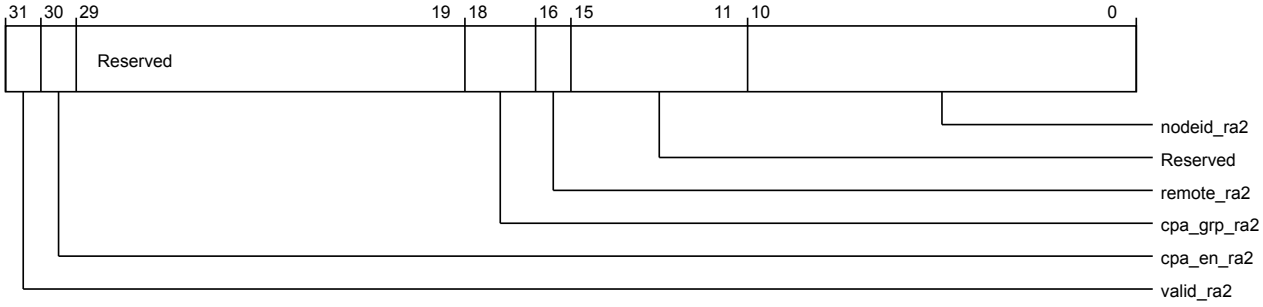


Figure 3-415 por_hnf_por_hnf_rn_phys_id1 (low)

The following table shows the por_hnf_rn_phys_id1 lower register bit assignments.

Table 3-429 por_hnf_por_hnf_rn_phys_id1 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra2	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra2	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra2	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0

Table 3-429 por_hnf_por_hnf_rn_phys_id1 (low) (continued)

Bits	Field name	Description	Type	Reset
16	remote_ra2	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra2	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id2

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

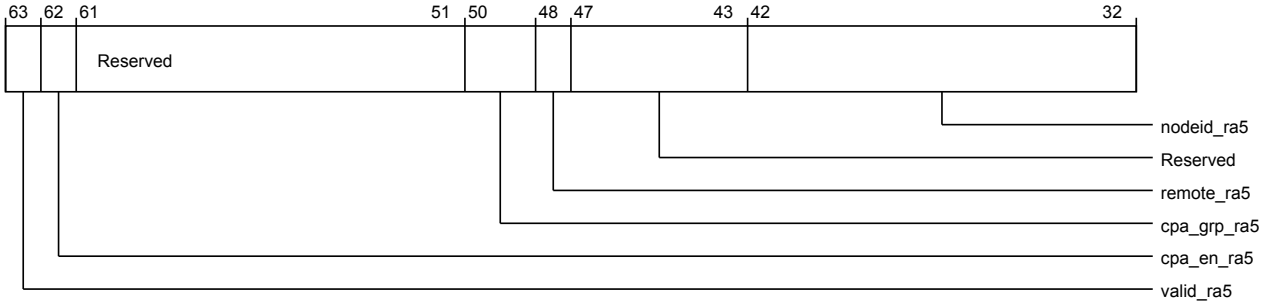


Figure 3-416 por_hnf_por_hnf_rn_phys_id2 (high)

The following table shows the por_hnf_rn_phys_id2 higher register bit assignments.

Table 3-430 por_hnf_por_hnf_rn_phys_id2 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra5	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra5	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra5	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra5	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra5	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

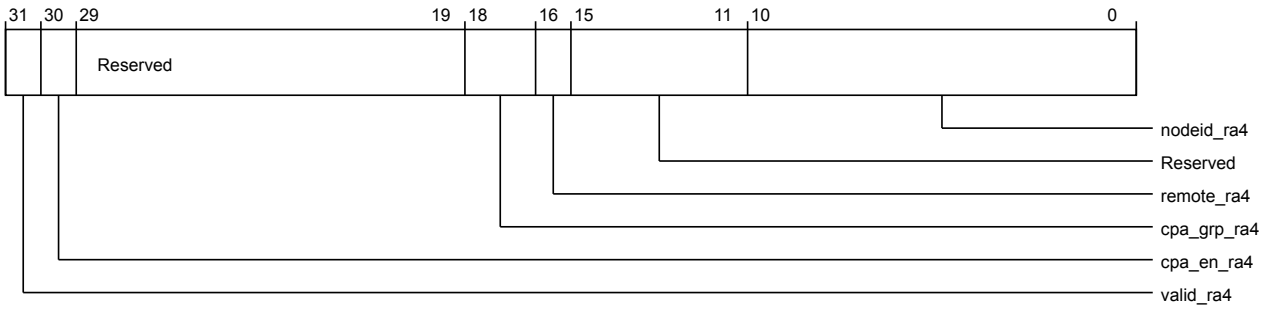


Figure 3-417 por_hnf_por_hnf_rn_phys_id2 (low)

The following table shows the por_hnf_rn_phys_id2 lower register bit assignments.

Table 3-431 por_hnf_por_hnf_rn_phys_id2 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra4	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra4	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra4	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra4	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra4	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id3

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD40
Register reset 64'b0
Usage constraints Only accessible by secure accesses.
Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

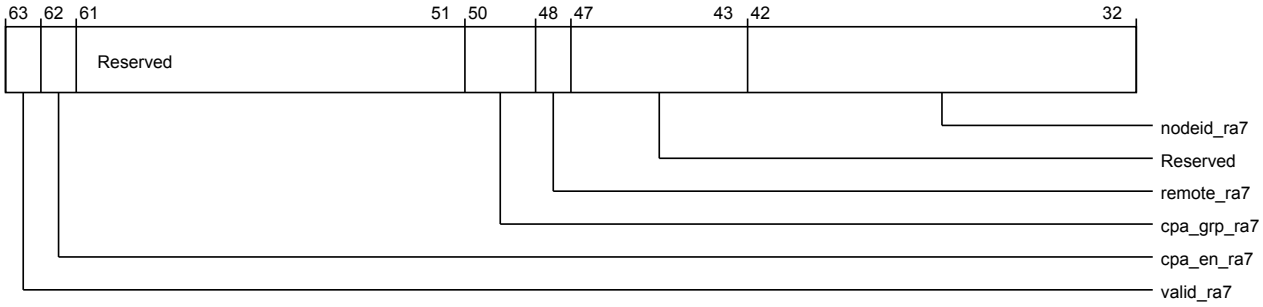


Figure 3-418 por_hnf_por_hnf_rn_phys_id3 (high)

The following table shows the por_hnf_rn_phys_id3 higher register bit assignments.

Table 3-432 por_hnf_por_hnf_rn_phys_id3 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra7	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra7	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra7	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra7	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra7	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

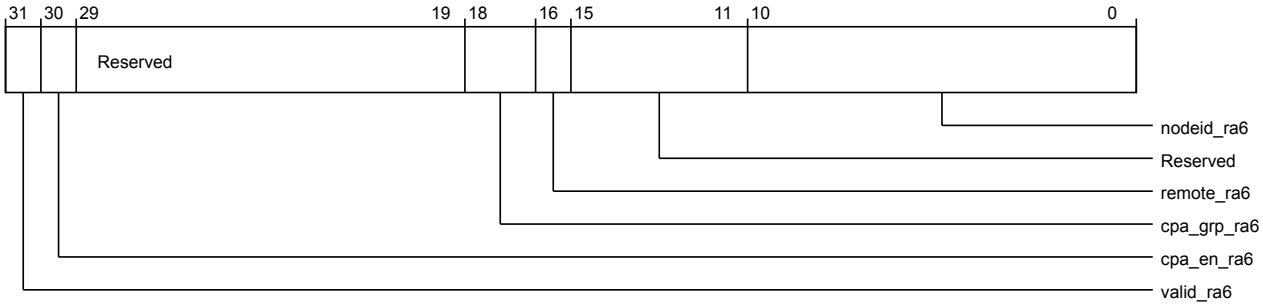


Figure 3-419 por_hnf_por_hnf_rn_phys_id3 (low)

The following table shows the por_hnf_rn_phys_id3 lower register bit assignments.

Table 3-433 por_hnf_por_hnf_rn_phys_id3 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra6	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra6	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra6	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra6	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra6	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id4

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

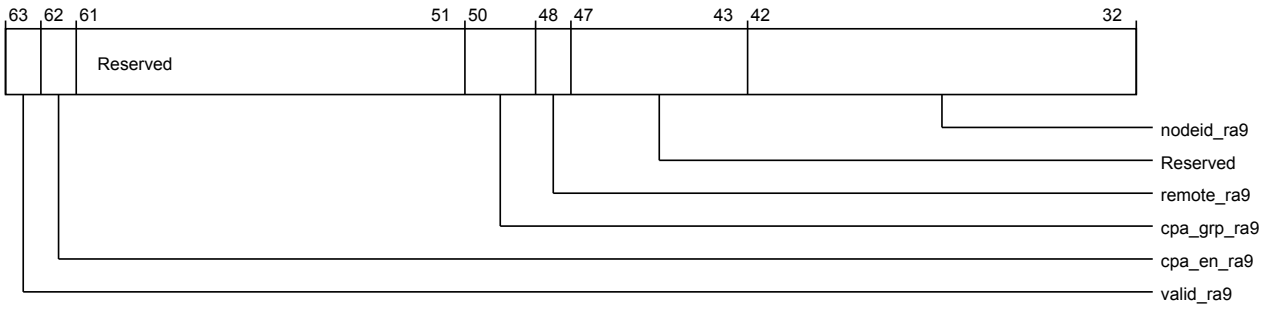


Figure 3-420 por_hnf_por_hnf_rn_phys_id4 (high)

The following table shows the por_hnf_rn_phys_id4 higher register bit assignments.

Table 3-434 por_hnf_por_hnf_rn_phys_id4 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra9	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra9	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra9	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra9	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra9	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

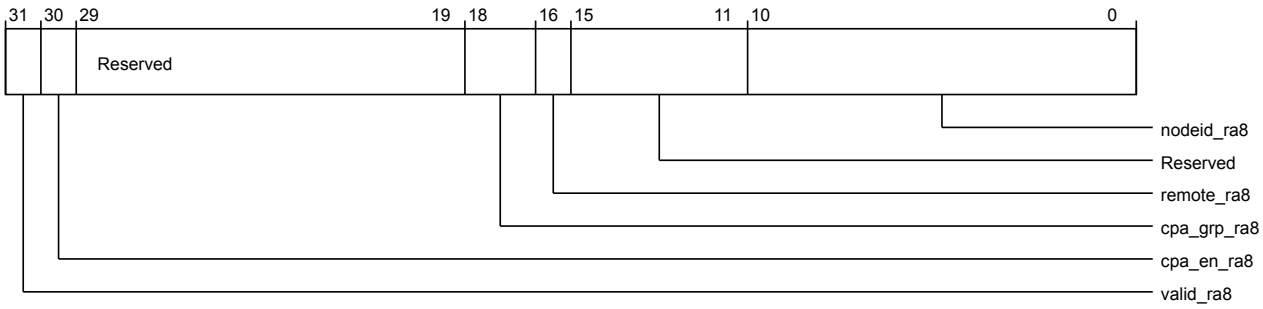


Figure 3-421 por_hnf_por_hnf_rn_phys_id4 (low)

The following table shows the por_hnf_rn_phys_id4 lower register bit assignments.

Table 3-435 por_hnf_por_hnf_rn_phys_id4 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra8	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra8	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra8	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra8	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra8	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id5

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

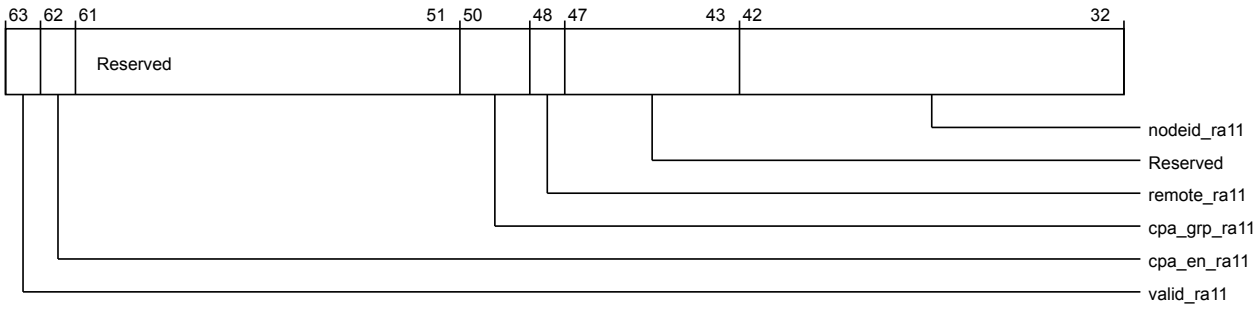


Figure 3-422 por_hnf_por_hnf_rn_phys_id5 (high)

The following table shows the por_hnf_rn_phys_id5 higher register bit assignments.

Table 3-436 por_hnf_por_hnf_rn_phys_id5 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra11	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra11	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra11	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra11	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra11	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

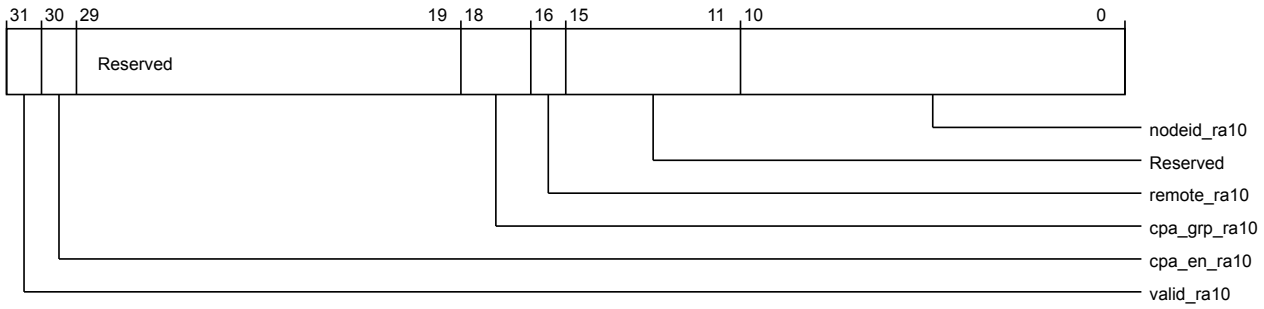


Figure 3-423 por_hnf_por_hnf_rn_phys_id5 (low)

The following table shows the por_hnf_rn_phys_id5 lower register bit assignments.

Table 3-437 por_hnf_por_hnf_rn_phys_id5 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra10	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra10	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra10	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra10	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra10	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id6

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

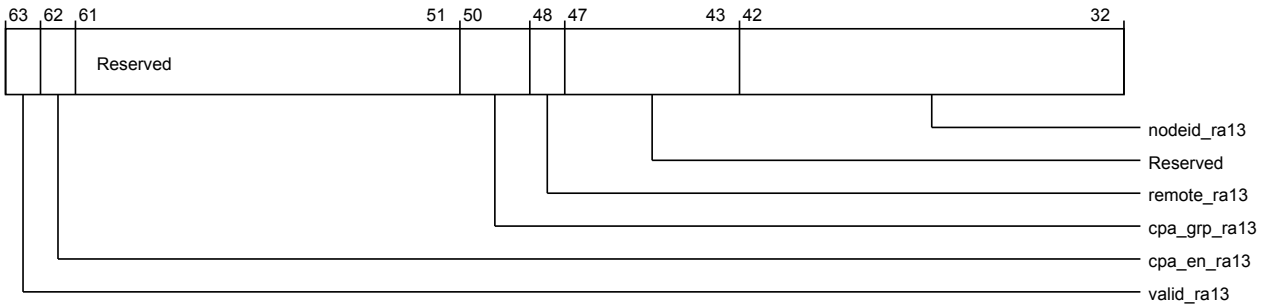


Figure 3-424 por_hnf_por_hnf_rn_phys_id6 (high)

The following table shows the por_hnf_rn_phys_id6 higher register bit assignments.

Table 3-438 por_hnf_por_hnf_rn_phys_id6 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra13	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra13	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra13	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra13	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra13	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

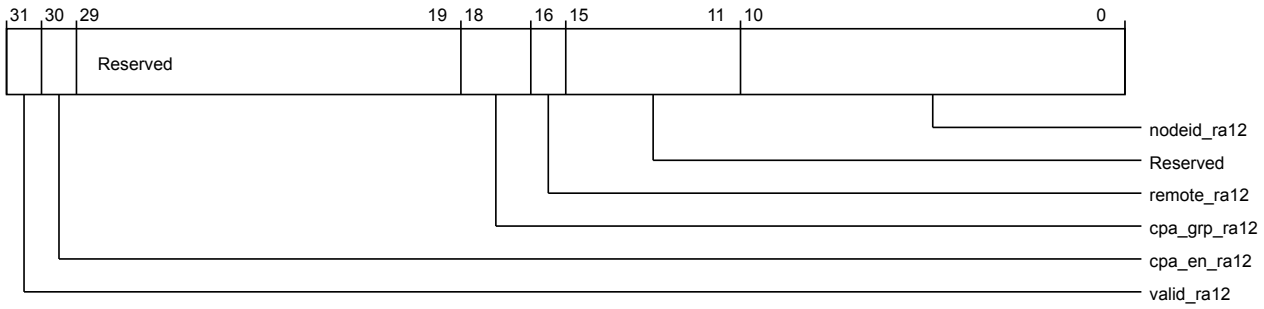


Figure 3-425 por_hnf_por_hnf_rn_phys_id6 (low)

The following table shows the por_hnf_rn_phys_id6 lower register bit assignments.

Table 3-439 por_hnf_por_hnf_rn_phys_id6 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra12	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra12	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra12	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra12	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra12	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id7

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

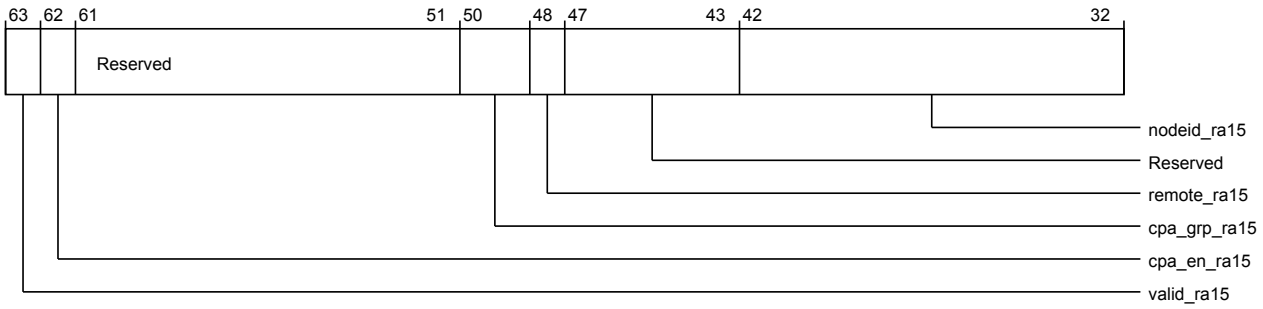


Figure 3-426 por_hnf_por_hnf_rn_phys_id7 (high)

The following table shows the por_hnf_rn_phys_id7 higher register bit assignments.

Table 3-440 por_hnf_por_hnf_rn_phys_id7 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra15	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra15	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra15	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra15	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra15	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

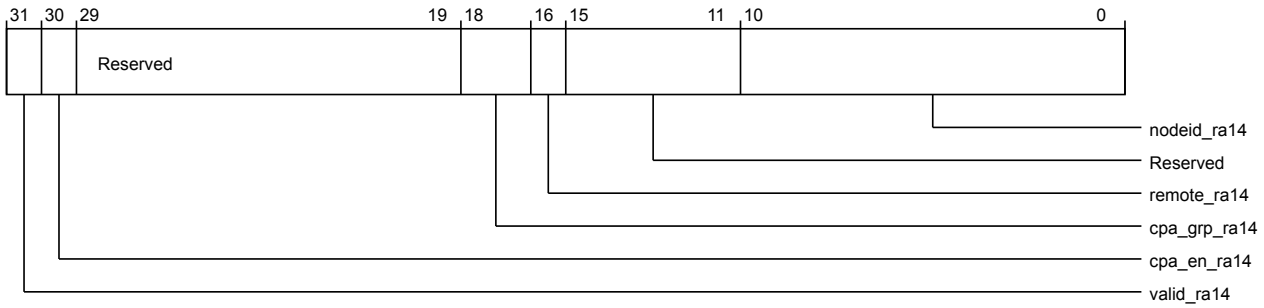


Figure 3-427 por_hnf_por_hnf_rn_phys_id7 (low)

The following table shows the por_hnf_rn_phys_id7 lower register bit assignments.

Table 3-441 por_hnf_por_hnf_rn_phys_id7 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra14	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra14	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra14	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra14	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra14	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id8

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

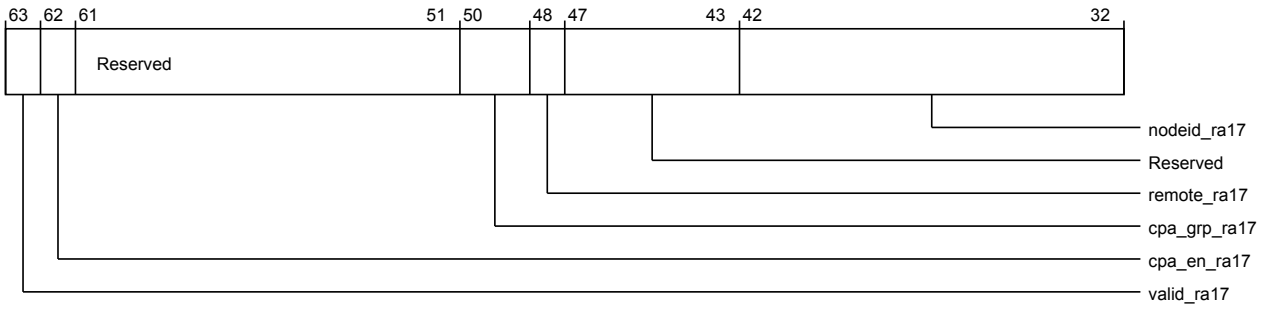


Figure 3-428 por_hnf_por_hnf_rn_phys_id8 (high)

The following table shows the por_hnf_rn_phys_id8 higher register bit assignments.

Table 3-442 por_hnf_por_hnf_rn_phys_id8 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra17	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra17	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra17	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra17	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra17	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

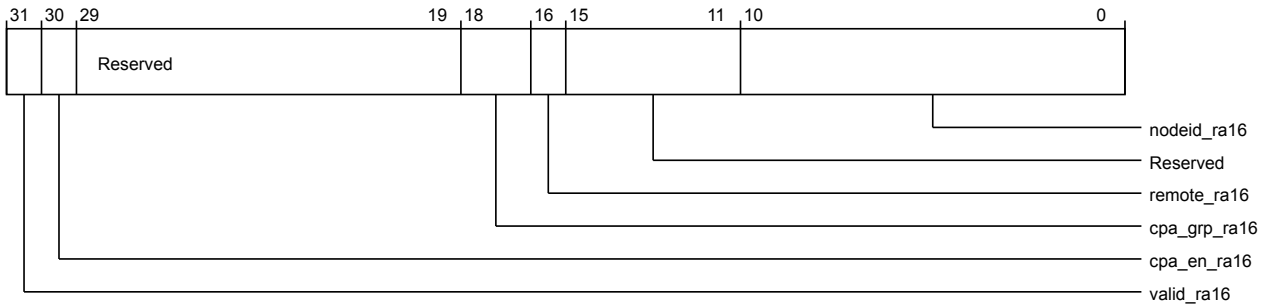


Figure 3-429 por_hnf_por_hnf_rn_phys_id8 (low)

The following table shows the por_hnf_rn_phys_id8 lower register bit assignments.

Table 3-443 por_hnf_por_hnf_rn_phys_id8 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra16	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra16	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra16	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra16	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra16	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id9

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

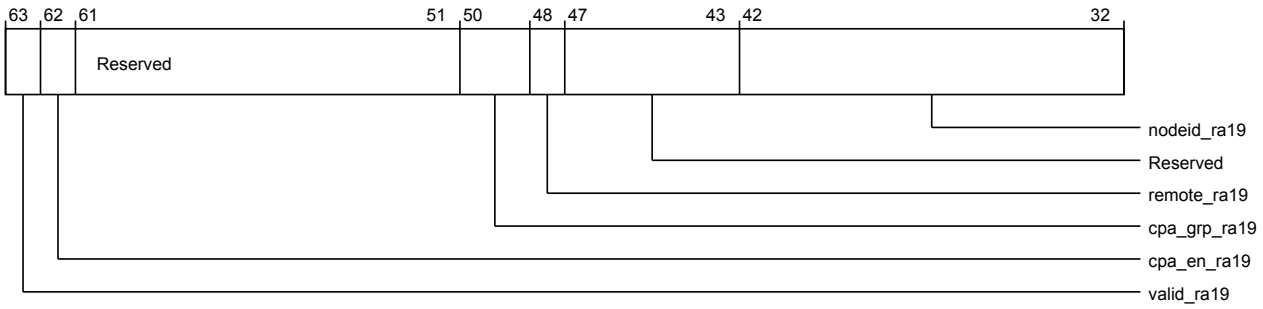


Figure 3-430 por_hnf_por_hnf_rn_phys_id9 (high)

The following table shows the por_hnf_rn_phys_id9 higher register bit assignments.

Table 3-444 por_hnf_por_hnf_rn_phys_id9 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra19	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra19	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra19	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra19	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra19	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

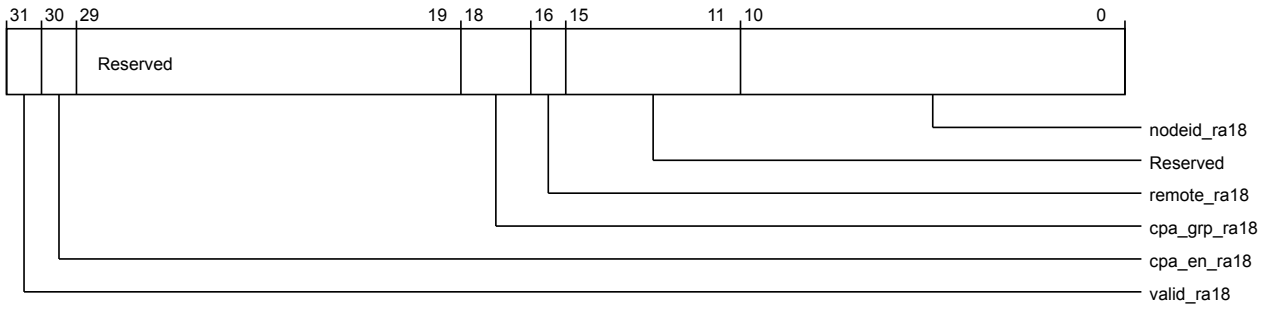


Figure 3-431 por_hnf_por_hnf_rn_phys_id9 (low)

The following table shows the por_hnf_rn_phys_id9 lower register bit assignments.

Table 3-445 por_hnf_por_hnf_rn_phys_id9 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra18	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra18	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra18	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra18	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra18	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id10

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

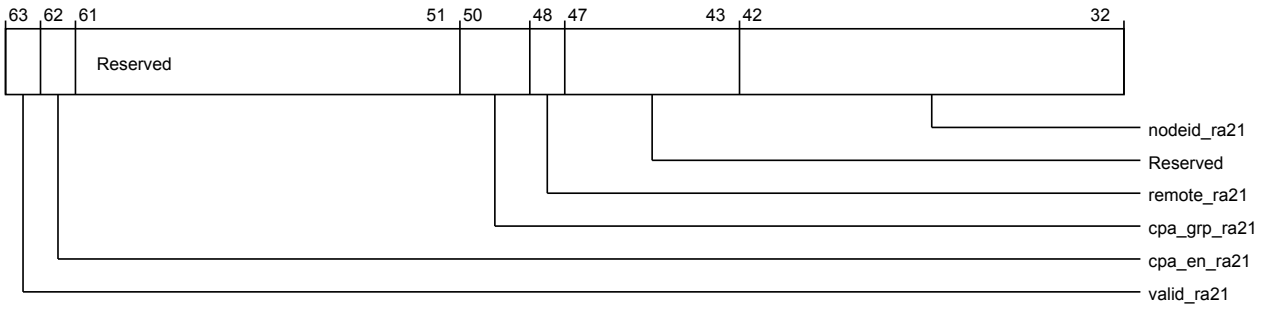


Figure 3-432 por_hnf_por_hnf_rn_phys_id10 (high)

The following table shows the por_hnf_rn_phys_id10 higher register bit assignments.

Table 3-446 por_hnf_por_hnf_rn_phys_id10 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra21	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra21	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra21	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra21	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra21	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

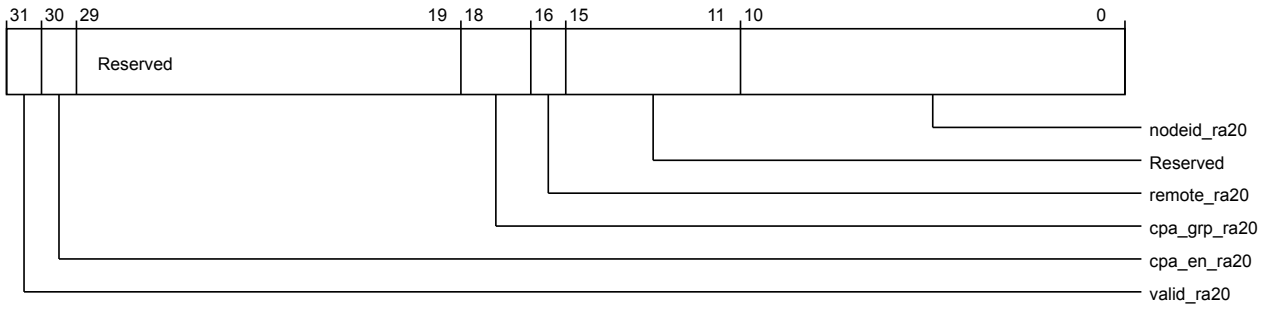


Figure 3-433 por_hnf_por_hnf_rn_phys_id10 (low)

The following table shows the por_hnf_rn_phys_id10 lower register bit assignments.

Table 3-447 por_hnf_por_hnf_rn_phys_id10 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra20	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra20	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra20	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra20	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra20	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id11

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

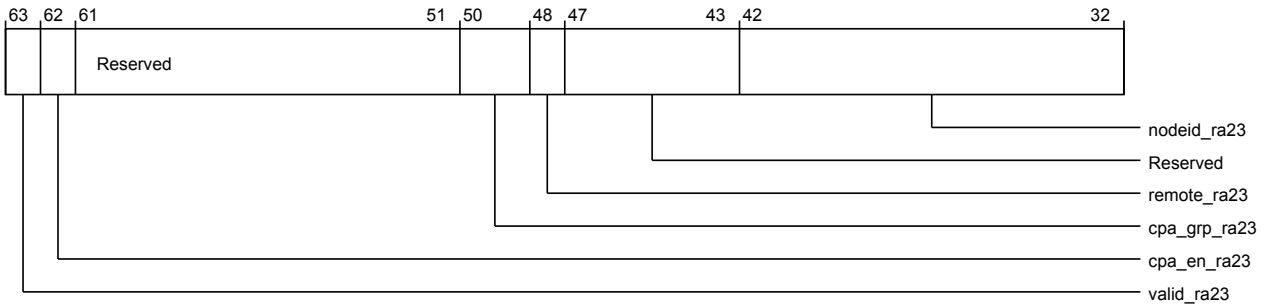


Figure 3-434 por_hnf_por_hnf_rn_phys_id11 (high)

The following table shows the por_hnf_rn_phys_id11 higher register bit assignments.

Table 3-448 por_hnf_por_hnf_rn_phys_id11 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra23	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra23	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra23	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra23	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra23	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

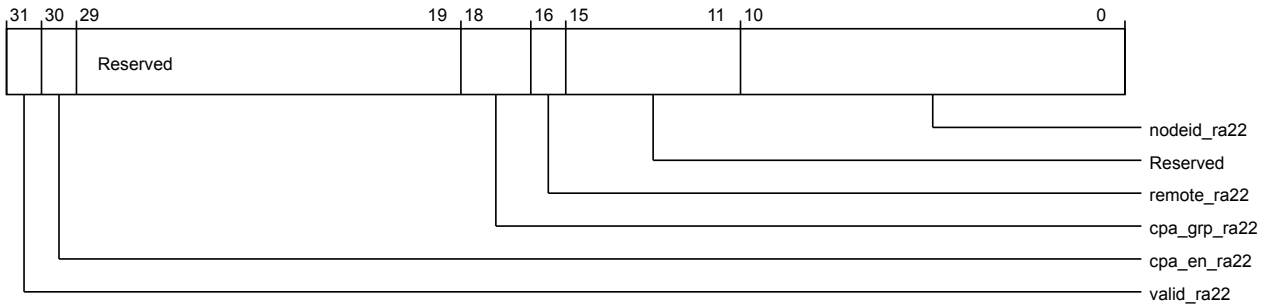


Figure 3-435 por_hnf_por_hnf_rn_phys_id11 (low)

The following table shows the por_hnf_rn_phys_id11 lower register bit assignments.

Table 3-449 por_hnf_por_hnf_rn_phys_id11 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra22	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra22	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra22	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra22	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra22	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id12

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

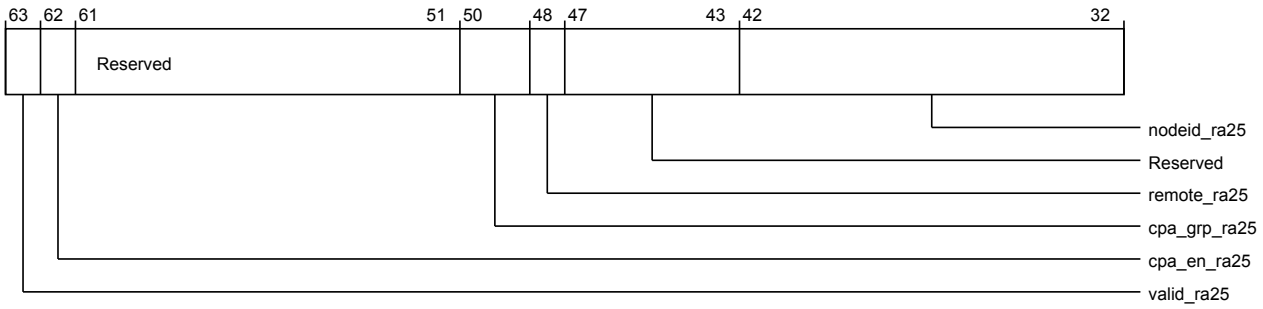


Figure 3-436 por_hnf_por_hnf_rn_phys_id12 (high)

The following table shows the por_hnf_rn_phys_id12 higher register bit assignments.

Table 3-450 por_hnf_por_hnf_rn_phys_id12 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra25	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra25	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra25	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra25	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra25	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

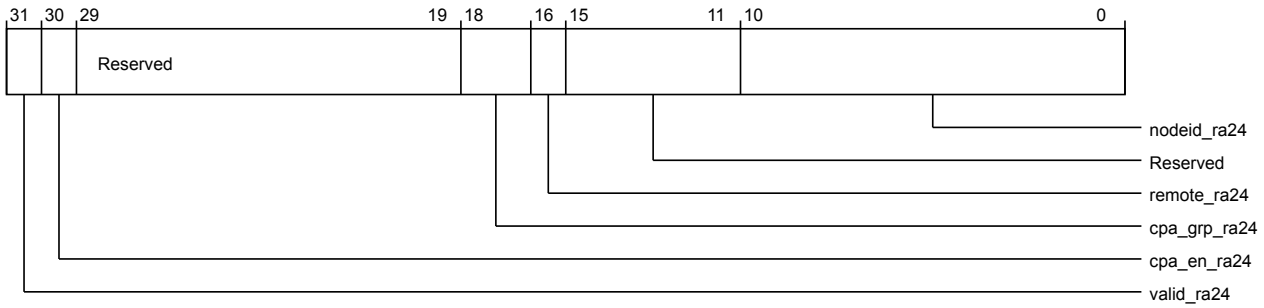


Figure 3-437 por_hnf_por_hnf_rn_phys_id12 (low)

The following table shows the por_hnf_rn_phys_id12 lower register bit assignments.

Table 3-451 por_hnf_por_hnf_rn_phys_id12 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra24	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra24	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra24	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra24	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra24	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id13

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

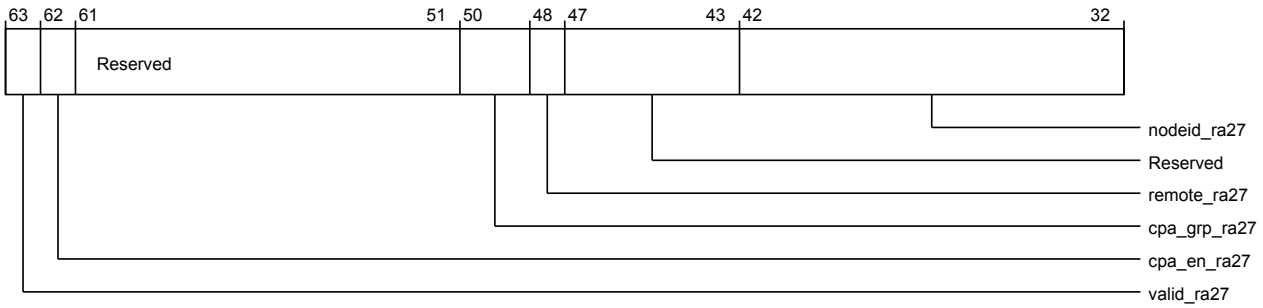


Figure 3-438 por_hnf_por_hnf_rn_phys_id13 (high)

The following table shows the por_hnf_rn_phys_id13 higher register bit assignments.

Table 3-452 por_hnf_por_hnf_rn_phys_id13 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra27	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra27	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra27	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra27	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra27	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

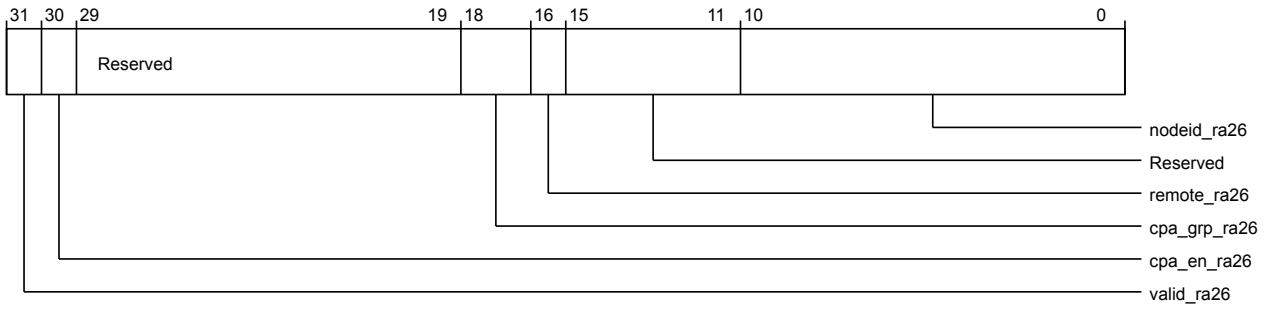


Figure 3-439 por_hnf_por_hnf_rn_phys_id13 (low)

The following table shows the por_hnf_rn_phys_id13 lower register bit assignments.

Table 3-453 por_hnf_por_hnf_rn_phys_id13 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra26	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra26	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra26	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra26	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra26	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id14

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

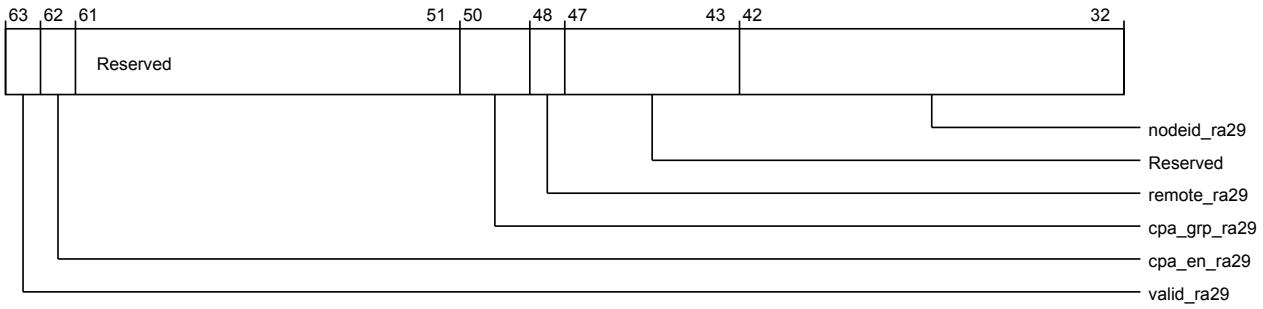


Figure 3-440 por_hnf_por_hnf_rn_phys_id14 (high)

The following table shows the por_hnf_rn_phys_id14 higher register bit assignments.

Table 3-454 por_hnf_por_hnf_rn_phys_id14 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra29	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra29	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra29	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra29	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra29	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

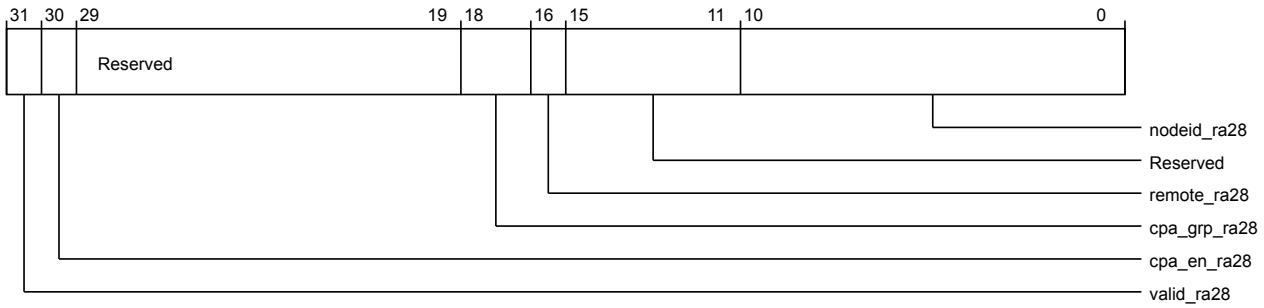


Figure 3-441 por_hnf_por_hnf_rn_phys_id14 (low)

The following table shows the por_hnf_rn_phys_id14 lower register bit assignments.

Table 3-455 por_hnf_por_hnf_rn_phys_id14 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra28	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra28	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra28	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra28	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra28	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id15

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

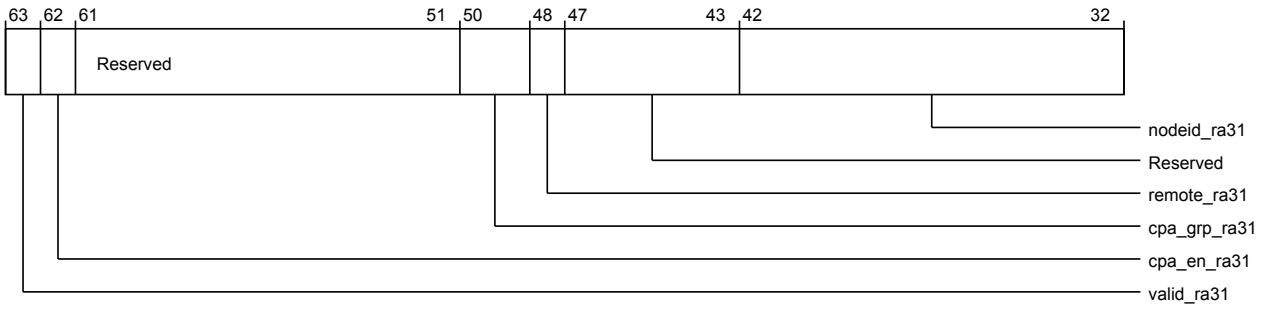


Figure 3-442 por_hnf_por_hnf_rn_phys_id15 (high)

The following table shows the por_hnf_rn_phys_id15 higher register bit assignments.

Table 3-456 por_hnf_por_hnf_rn_phys_id15 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra31	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra31	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra31	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra31	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra31	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

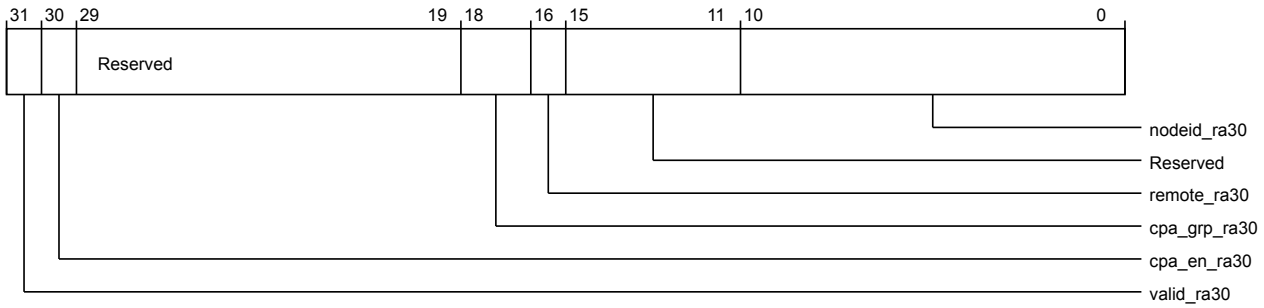


Figure 3-443 por_hnf_por_hnf_rn_phys_id15 (low)

The following table shows the por_hnf_rn_phys_id15 lower register bit assignments.

Table 3-457 por_hnf_por_hnf_rn_phys_id15 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra30	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra30	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra30	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra30	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra30	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id16

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

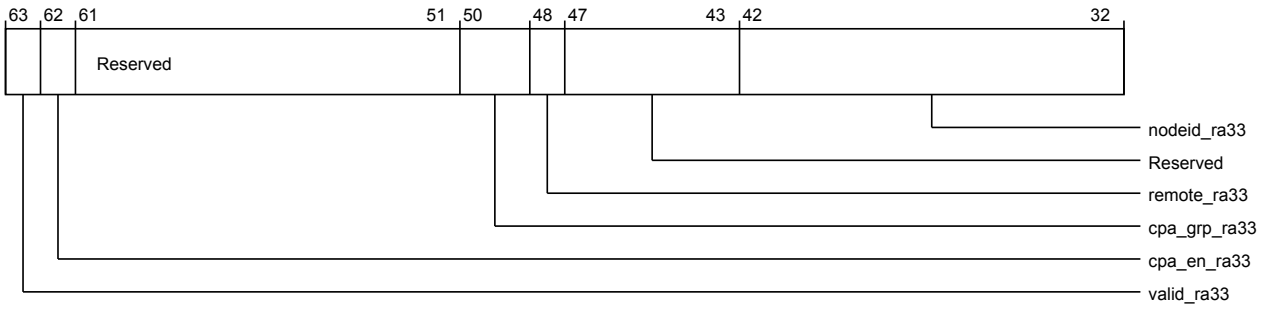


Figure 3-444 por_hnf_por_hnf_rn_phys_id16 (high)

The following table shows the por_hnf_rn_phys_id16 higher register bit assignments.

Table 3-458 por_hnf_por_hnf_rn_phys_id16 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra33	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra33	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra33	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra33	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra33	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

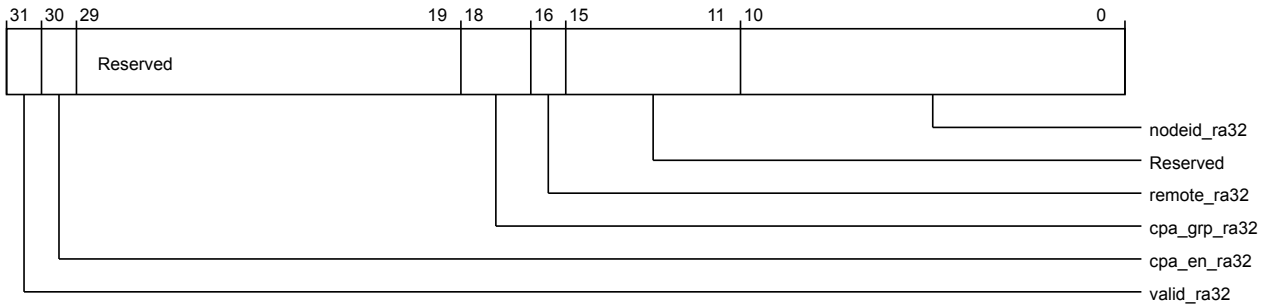


Figure 3-445 por_hnf_por_hnf_rn_phys_id16 (low)

The following table shows the por_hnf_rn_phys_id16 lower register bit assignments.

Table 3-459 por_hnf_por_hnf_rn_phys_id16 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra32	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra32	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra32	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra32	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra32	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id17

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

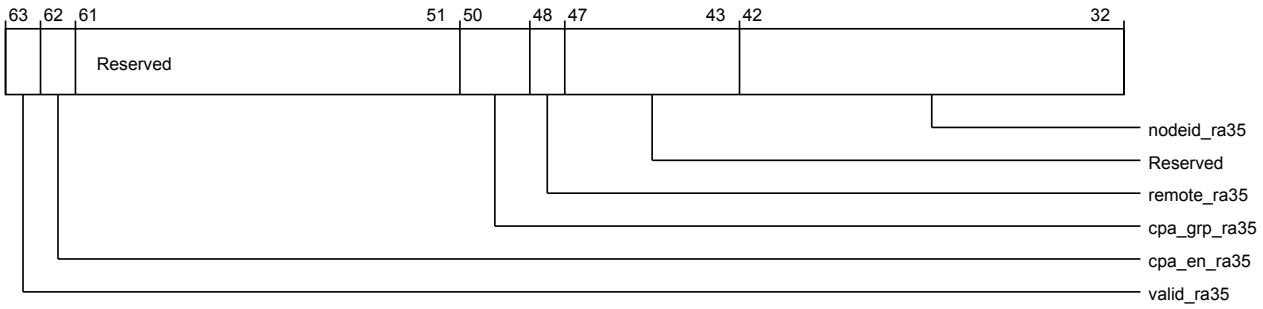


Figure 3-446 por_hnf_por_hnf_rn_phys_id17 (high)

The following table shows the por_hnf_rn_phys_id17 higher register bit assignments.

Table 3-460 por_hnf_por_hnf_rn_phys_id17 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra35	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra35	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra35	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra35	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra35	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

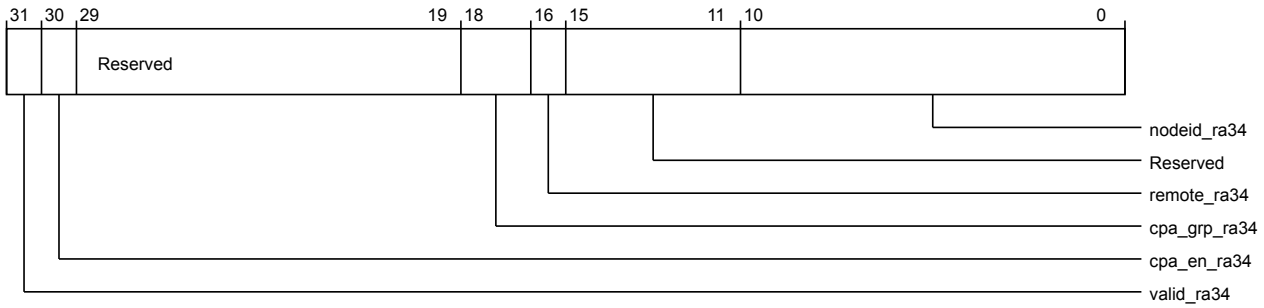


Figure 3-447 por_hnf_por_hnf_rn_phys_id17 (low)

The following table shows the por_hnf_rn_phys_id17 lower register bit assignments.

Table 3-461 por_hnf_por_hnf_rn_phys_id17 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra34	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra34	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra34	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra34	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra34	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id18

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

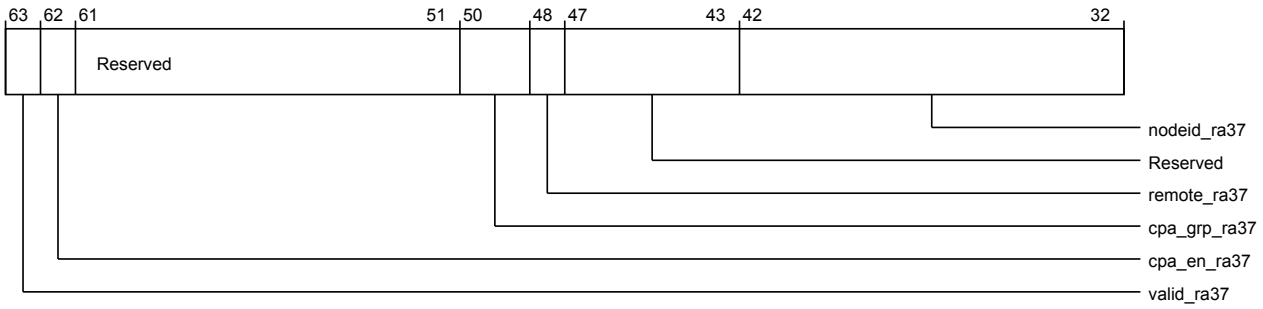


Figure 3-448 por_hnf_por_hnf_rn_phys_id18 (high)

The following table shows the por_hnf_rn_phys_id18 higher register bit assignments.

Table 3-462 por_hnf_por_hnf_rn_phys_id18 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra37	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra37	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra37	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra37	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra37	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

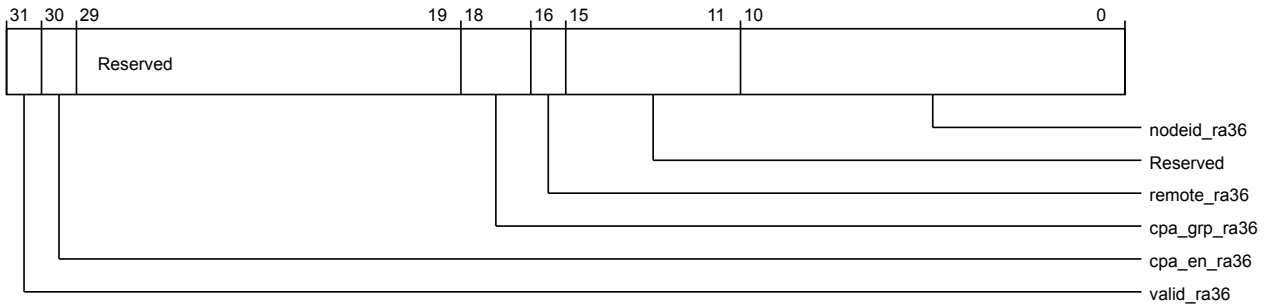


Figure 3-449 por_hnf_por_hnf_rn_phys_id18 (low)

The following table shows the por_hnf_rn_phys_id18 lower register bit assignments.

Table 3-463 por_hnf_por_hnf_rn_phys_id18 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra36	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra36	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra36	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra36	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra36	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id19

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

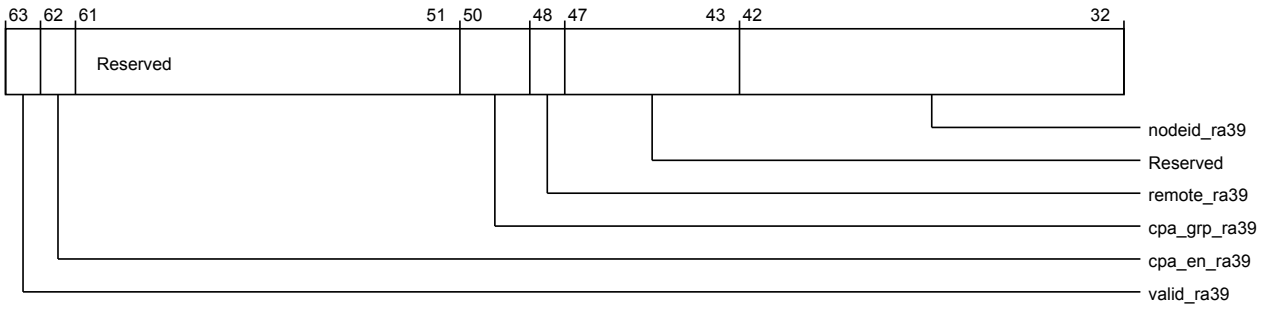


Figure 3-450 por_hnf_por_hnf_rn_phys_id19 (high)

The following table shows the por_hnf_rn_phys_id19 higher register bit assignments.

Table 3-464 por_hnf_por_hnf_rn_phys_id19 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra39	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra39	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra39	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra39	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra39	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

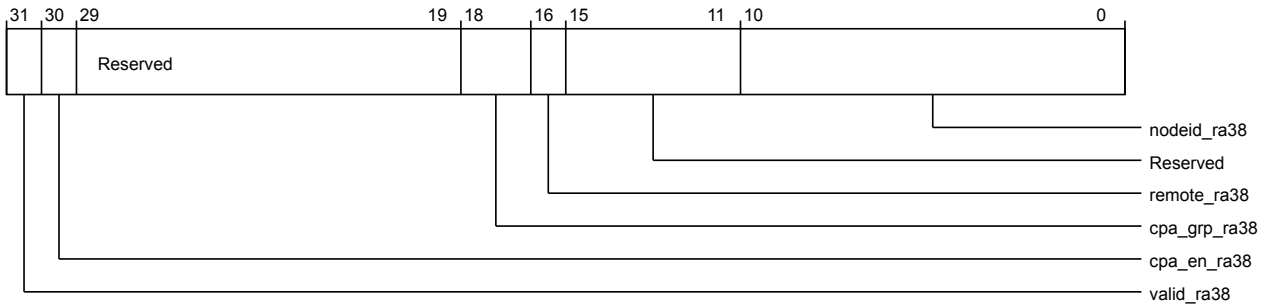


Figure 3-451 por_hnf_por_hnf_rn_phys_id19 (low)

The following table shows the por_hnf_rn_phys_id19 lower register bit assignments.

Table 3-465 por_hnf_por_hnf_rn_phys_id19 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra38	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra38	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra38	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra38	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra38	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id20

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

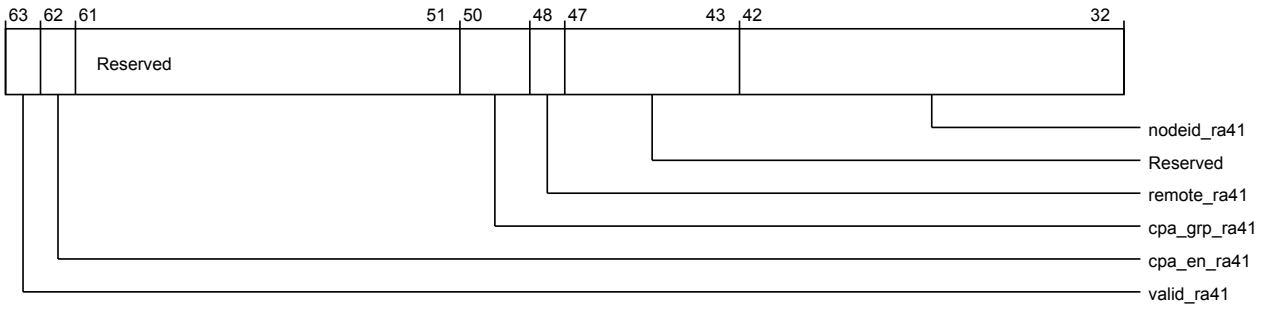


Figure 3-452 por_hnf_por_hnf_rn_phys_id20 (high)

The following table shows the por_hnf_rn_phys_id20 higher register bit assignments.

Table 3-466 por_hnf_por_hnf_rn_phys_id20 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra41	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra41	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra41	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra41	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra41	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

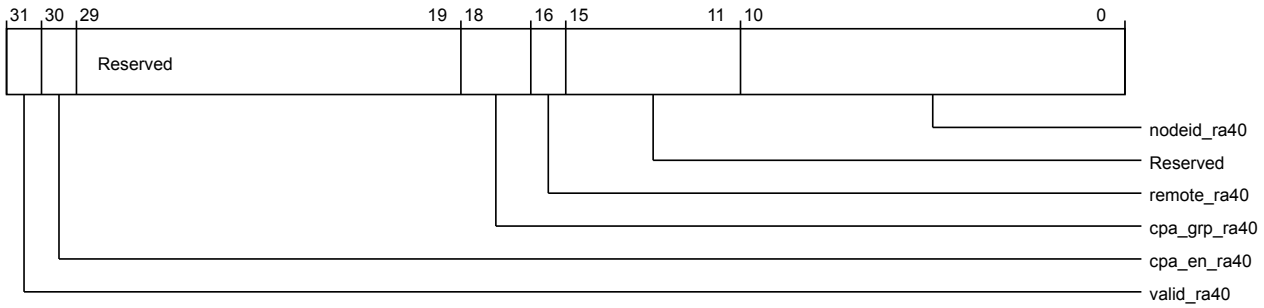


Figure 3-453 por_hnf_por_hnf_rn_phys_id20 (low)

The following table shows the por_hnf_rn_phys_id20 lower register bit assignments.

Table 3-467 por_hnf_por_hnf_rn_phys_id20 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra40	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra40	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra40	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra40	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra40	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id21

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

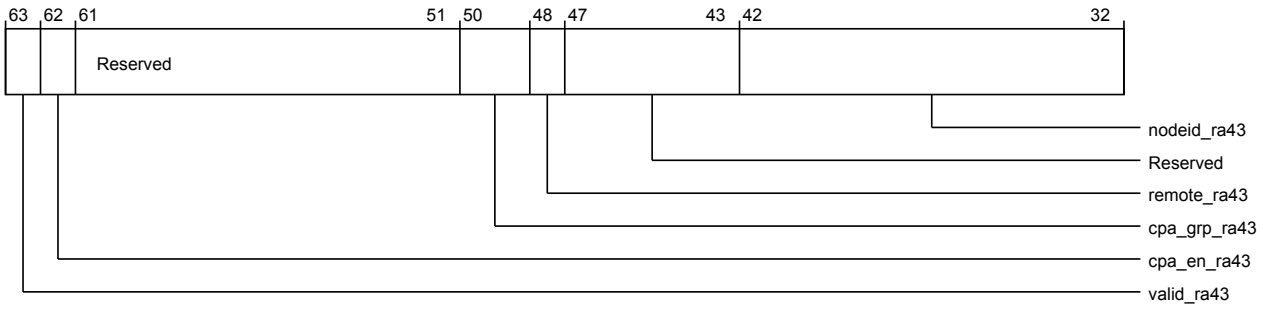


Figure 3-454 por_hnf_por_hnf_rn_phys_id21 (high)

The following table shows the por_hnf_rn_phys_id21 higher register bit assignments.

Table 3-468 por_hnf_por_hnf_rn_phys_id21 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra43	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra43	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra43	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra43	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra43	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

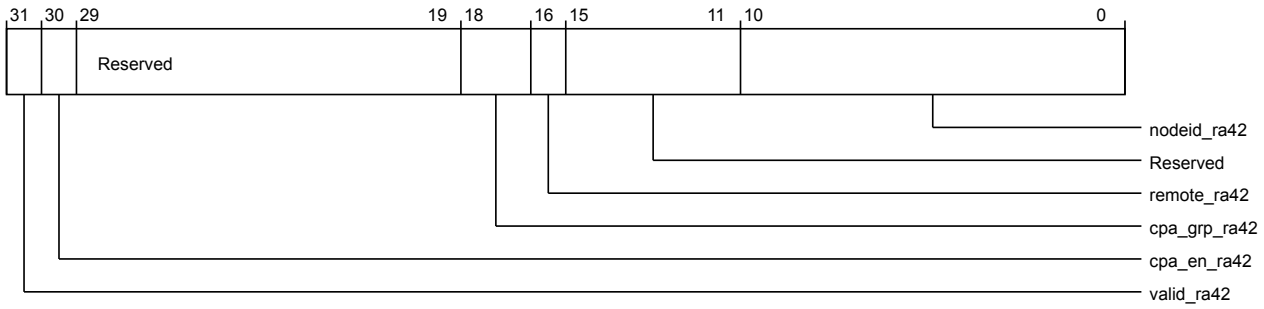


Figure 3-455 por_hnf_por_hnf_rn_phys_id21 (low)

The following table shows the por_hnf_rn_phys_id21 lower register bit assignments.

Table 3-469 por_hnf_por_hnf_rn_phys_id21 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra42	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra42	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra42	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra42	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra42	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id22

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

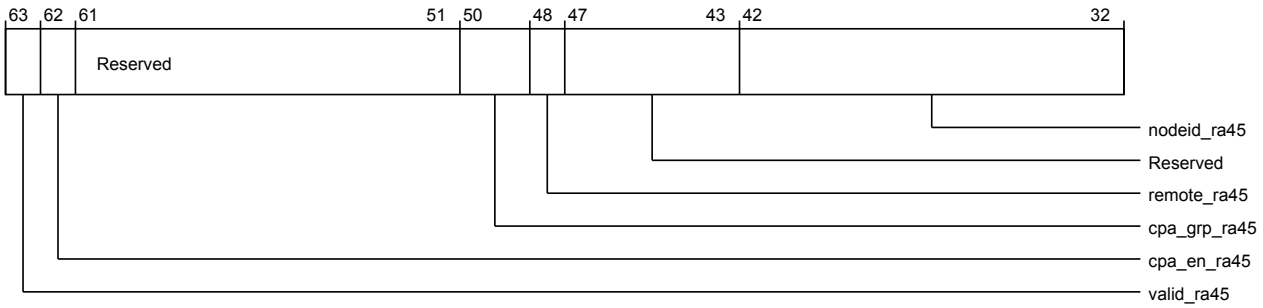


Figure 3-456 por_hnf_por_hnf_rn_phys_id22 (high)

The following table shows the por_hnf_rn_phys_id22 higher register bit assignments.

Table 3-470 por_hnf_por_hnf_rn_phys_id22 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra45	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra45	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra45	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra45	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra45	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

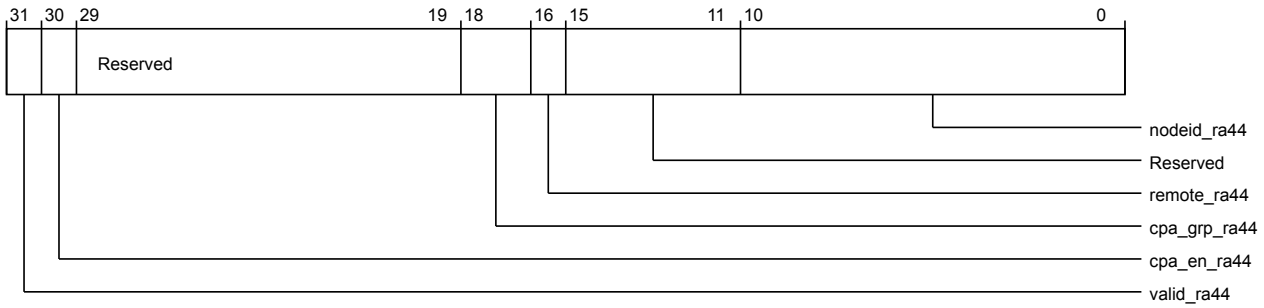


Figure 3-457 por_hnf_por_hnf_rn_phys_id22 (low)

The following table shows the por_hnf_rn_phys_id22 lower register bit assignments.

Table 3-471 por_hnf_por_hnf_rn_phys_id22 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra44	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra44	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra44	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra44	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra44	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id23

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

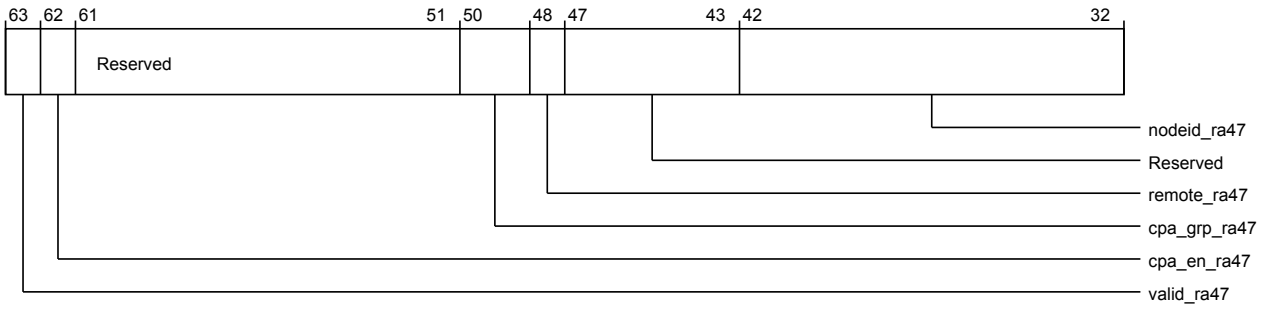


Figure 3-458 por_hnf_por_hnf_rn_phys_id23 (high)

The following table shows the por_hnf_rn_phys_id23 higher register bit assignments.

Table 3-472 por_hnf_por_hnf_rn_phys_id23 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra47	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra47	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra47	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra47	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra47	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

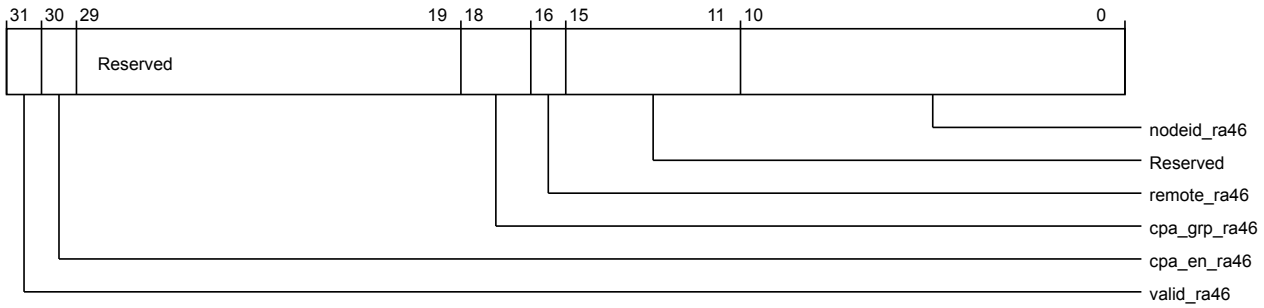


Figure 3-459 por_hnf_por_hnf_rn_phys_id23 (low)

The following table shows the por_hnf_rn_phys_id23 lower register bit assignments.

Table 3-473 por_hnf_por_hnf_rn_phys_id23 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra46	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra46	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra46	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra46	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra46	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id24

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

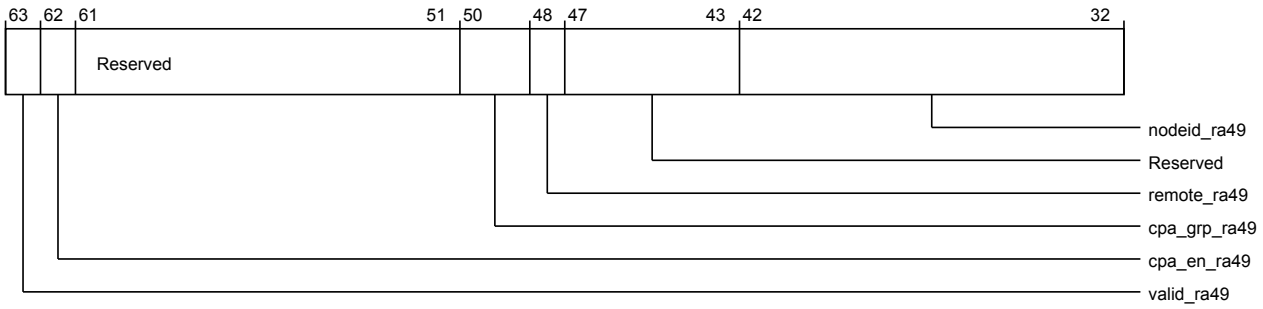


Figure 3-460 por_hnf_por_hnf_rn_phys_id24 (high)

The following table shows the por_hnf_rn_phys_id24 higher register bit assignments.

Table 3-474 por_hnf_por_hnf_rn_phys_id24 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra49	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra49	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra49	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra49	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra49	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

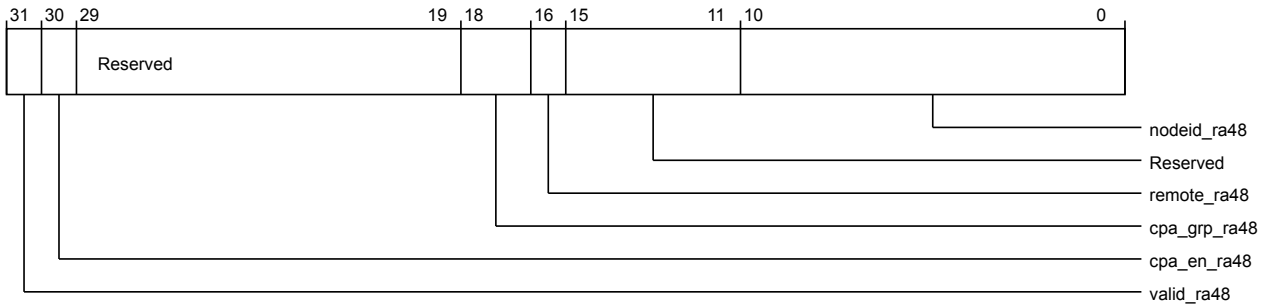


Figure 3-461 por_hnf_por_hnf_rn_phys_id24 (low)

The following table shows the por_hnf_rn_phys_id24 lower register bit assignments.

Table 3-475 por_hnf_por_hnf_rn_phys_id24 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra48	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra48	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra48	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra48	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra48	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id25

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

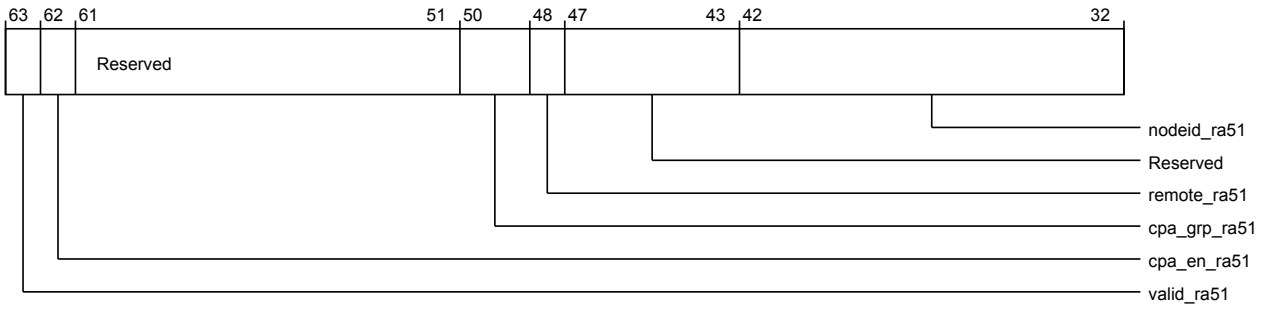


Figure 3-462 por_hnf_por_hnf_rn_phys_id25 (high)

The following table shows the por_hnf_rn_phys_id25 higher register bit assignments.

Table 3-476 por_hnf_por_hnf_rn_phys_id25 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra51	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra51	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra51	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra51	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra51	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

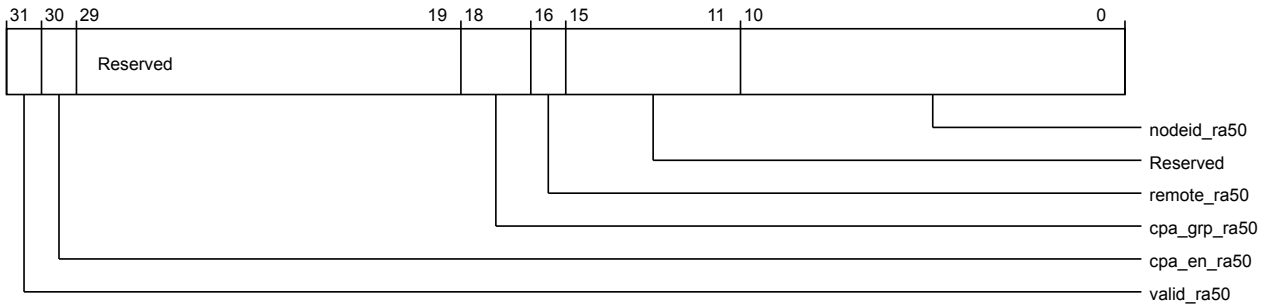


Figure 3-463 por_hnf_por_hnf_rn_phys_id25 (low)

The following table shows the por_hnf_rn_phys_id25 lower register bit assignments.

Table 3-477 por_hnf_por_hnf_rn_phys_id25 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra50	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra50	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra50	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra50	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra50	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id26

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hDF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

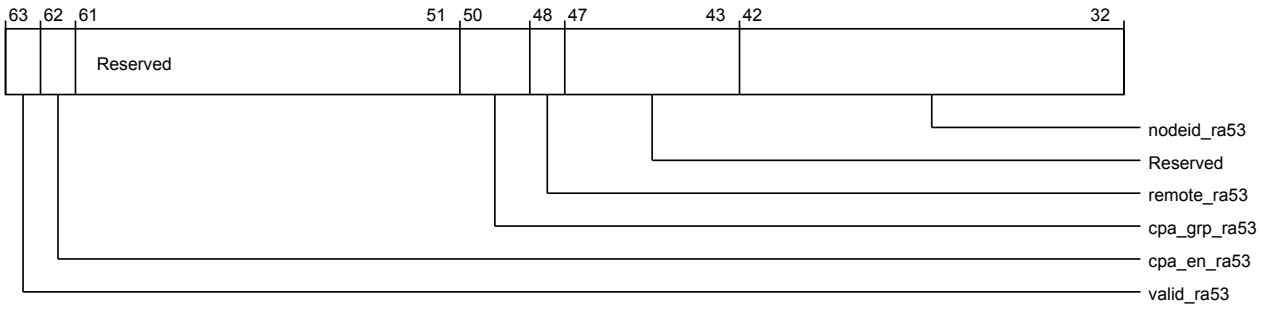


Figure 3-464 por_hnf_por_hnf_rn_phys_id26 (high)

The following table shows the por_hnf_rn_phys_id26 higher register bit assignments.

Table 3-478 por_hnf_por_hnf_rn_phys_id26 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra53	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra53	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra53	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra53	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra53	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

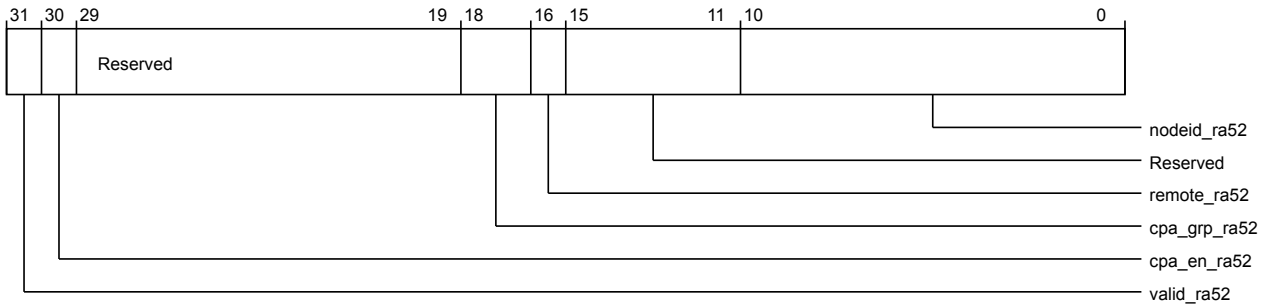


Figure 3-465 por_hnf_por_hnf_rn_phys_id26 (low)

The following table shows the por_hnf_rn_phys_id26 lower register bit assignments.

Table 3-479 por_hnf_por_hnf_rn_phys_id26 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra52	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra52	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra52	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra52	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra52	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id27

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

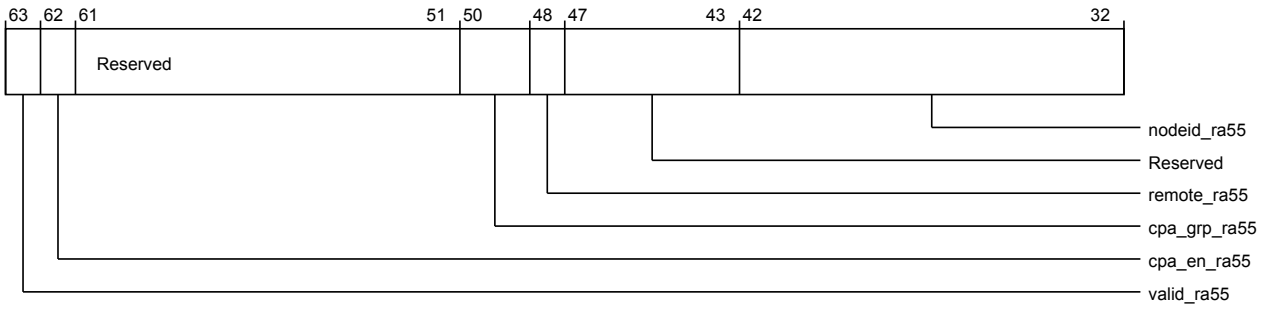


Figure 3-466 por_hnf_por_hnf_rn_phys_id27 (high)

The following table shows the por_hnf_rn_phys_id27 higher register bit assignments.

Table 3-480 por_hnf_por_hnf_rn_phys_id27 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra55	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra55	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra55	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra55	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra55	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

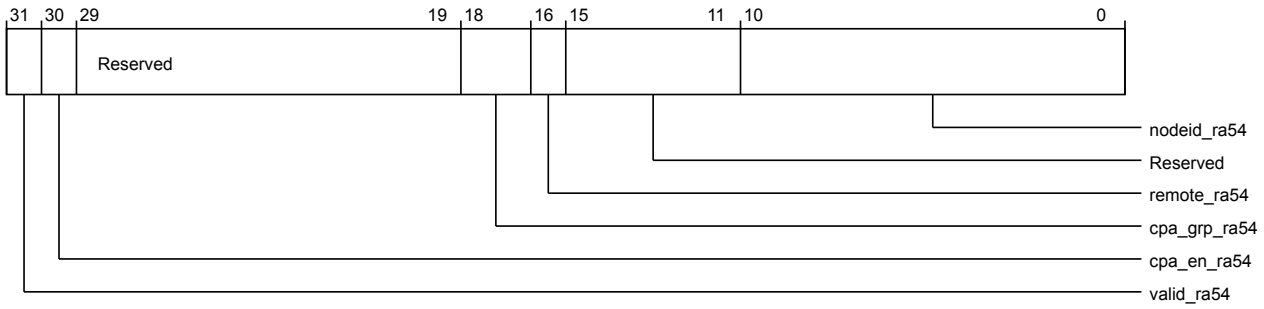


Figure 3-467 por_hnf_por_hnf_rn_phys_id27 (low)

The following table shows the por_hnf_rn_phys_id27 lower register bit assignments.

Table 3-481 por_hnf_por_hnf_rn_phys_id27 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra54	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra54	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra54	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra54	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra54	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id28

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

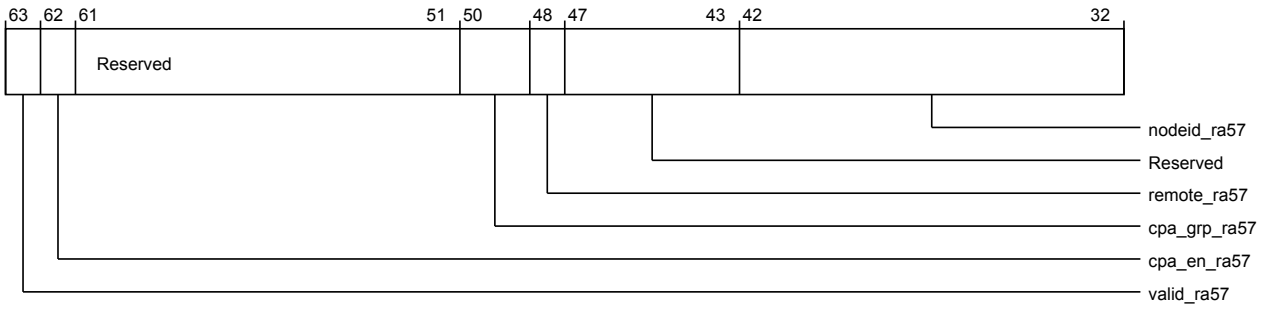


Figure 3-468 por_hnf_por_hnf_rn_phys_id28 (high)

The following table shows the por_hnf_rn_phys_id28 higher register bit assignments.

Table 3-482 por_hnf_por_hnf_rn_phys_id28 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra57	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra57	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra57	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra57	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra57	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

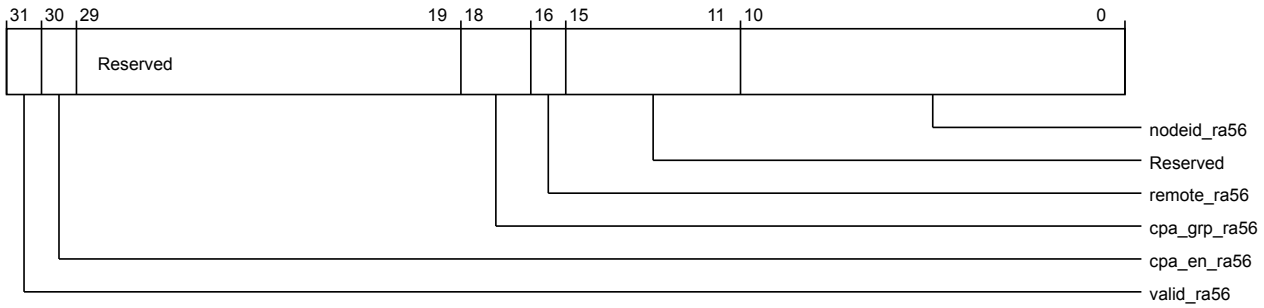


Figure 3-469 por_hnf_por_hnf_rn_phys_id28 (low)

The following table shows the por_hnf_rn_phys_id28 lower register bit assignments.

Table 3-483 por_hnf_por_hnf_rn_phys_id28 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra56	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra56	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra56	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra56	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra56	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id29

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

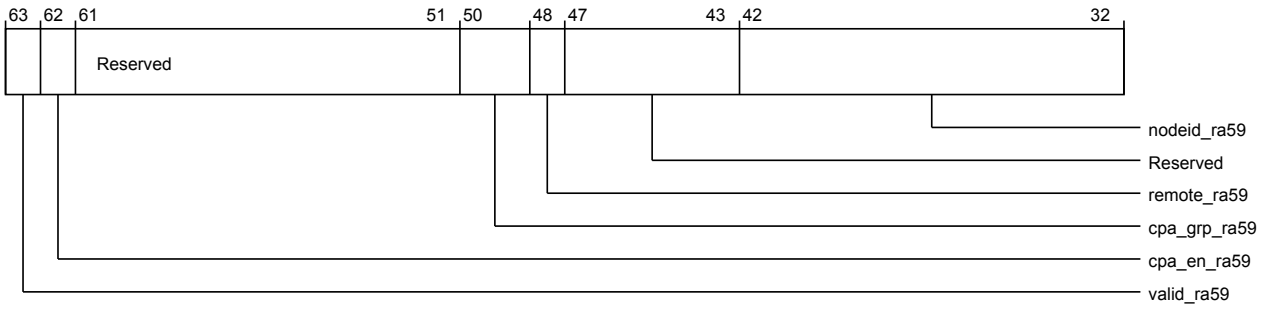


Figure 3-470 por_hnf_por_hnf_rn_phys_id29 (high)

The following table shows the por_hnf_rn_phys_id29 higher register bit assignments.

Table 3-484 por_hnf_por_hnf_rn_phys_id29 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra59	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra59	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra59	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra59	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra59	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

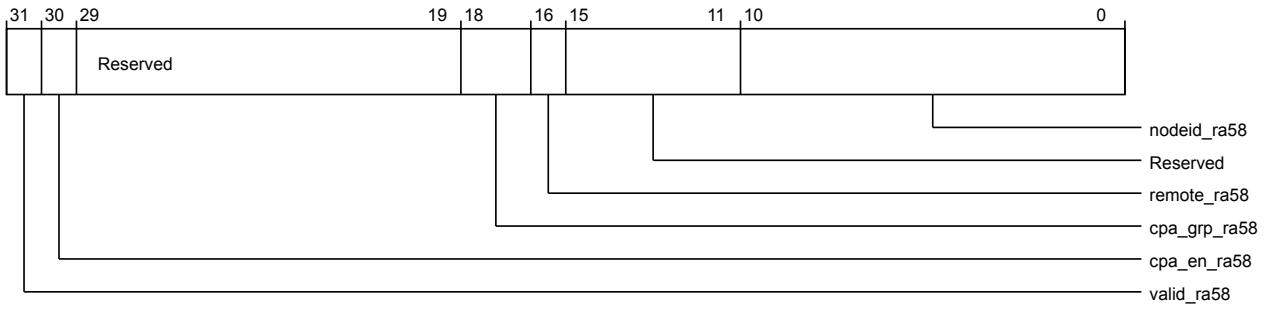


Figure 3-471 por_hnf_por_hnf_rn_phys_id29 (low)

The following table shows the por_hnf_rn_phys_id29 lower register bit assignments.

Table 3-485 por_hnf_por_hnf_rn_phys_id29 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra58	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra58	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra58	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra58	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra58	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id30

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

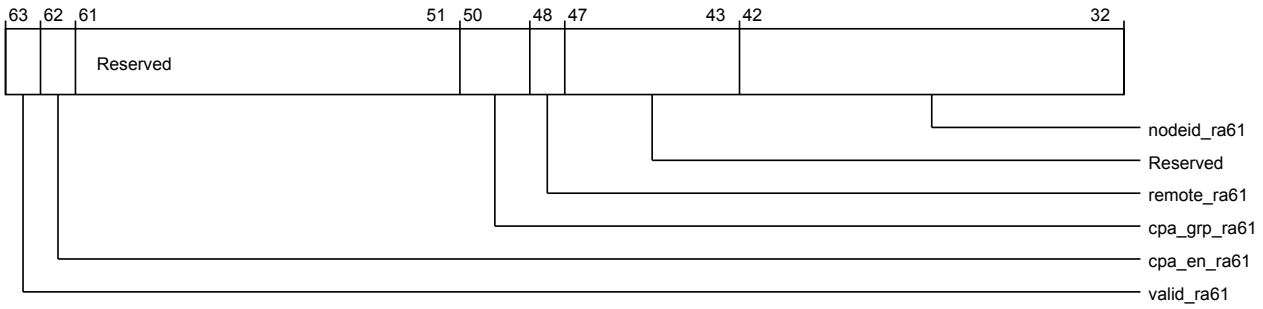


Figure 3-472 por_hnf_por_hnf_rn_phys_id30 (high)

The following table shows the por_hnf_rn_phys_id30 higher register bit assignments.

Table 3-486 por_hnf_por_hnf_rn_phys_id30 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra61	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra61	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra61	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra61	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra61	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

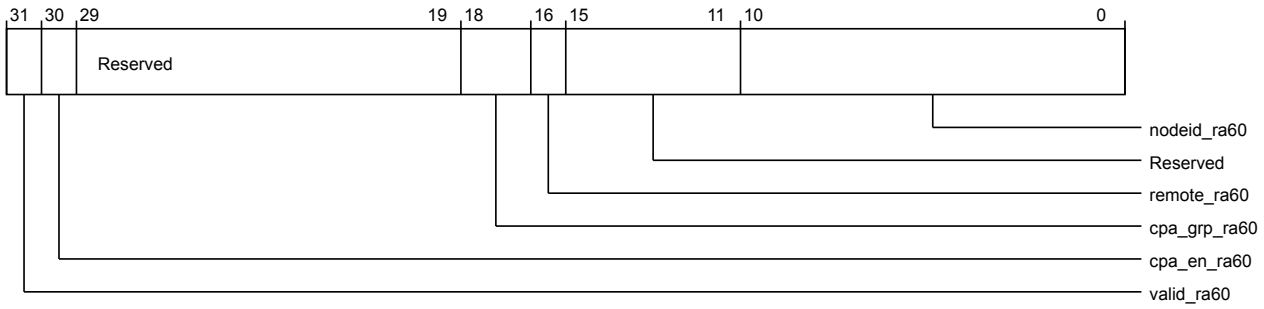


Figure 3-473 por_hnf_por_hnf_rn_phys_id30 (low)

The following table shows the por_hnf_rn_phys_id30 lower register bit assignments.

Table 3-487 por_hnf_por_hnf_rn_phys_id30 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra60	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra60	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra60	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra60	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra60	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id31

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hE20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

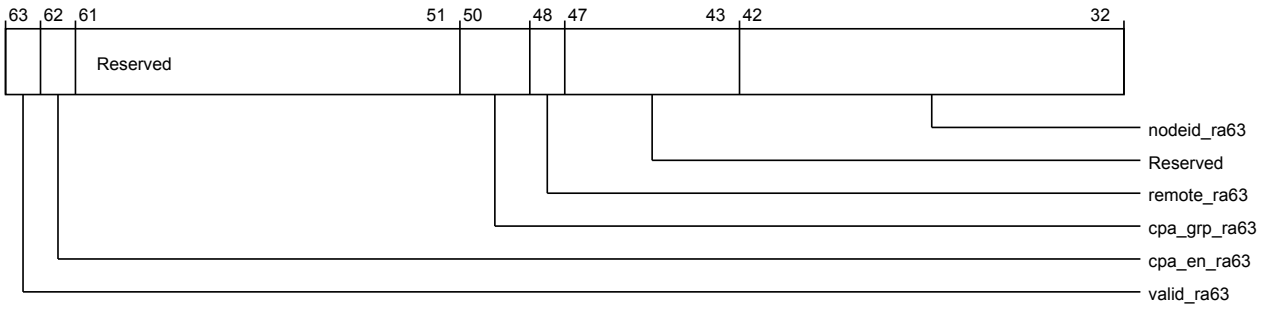


Figure 3-474 por_hnf_por_hnf_rn_phys_id31 (high)

The following table shows the por_hnf_rn_phys_id31 higher register bit assignments.

Table 3-488 por_hnf_por_hnf_rn_phys_id31 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra63	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra63	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra63	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra63	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra63	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

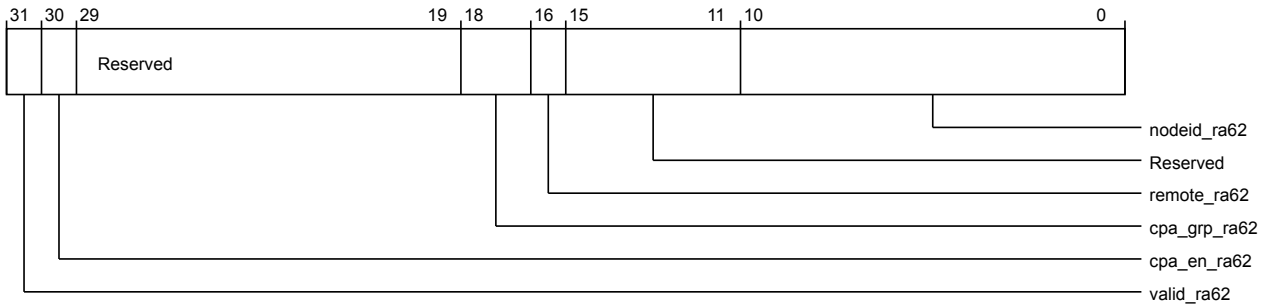


Figure 3-475 por_hnf_por_hnf_rn_phys_id31 (low)

The following table shows the por_hnf_rn_phys_id31 lower register bit assignments.

Table 3-489 por_hnf_por_hnf_rn_phys_id31 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra62	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra62	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra62	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra62	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra62	Specifies the node ID	RW	11'h0

por_hnf_sf_cxg_blocked_ways

Specifies the SF ways that are blocked for remote chip to use in CML mode.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hF00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

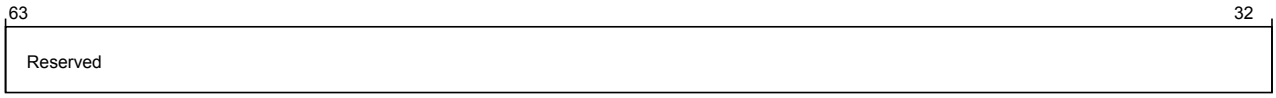


Figure 3-476 por_hnf_por_hnf_sf_cxg_blocked_ways (high)

The following table shows the por_hnf_sf_cxg_blocked_ways higher register bit assignments.

Table 3-490 por_hnf_por_hnf_sf_cxg_blocked_ways (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

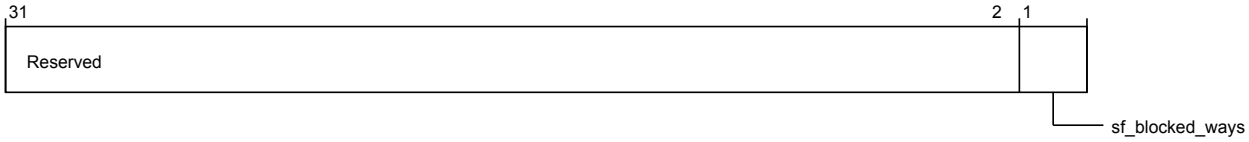


Figure 3-477 por_hnf_por_hnf_sf_cxg_blocked_ways (low)

The following table shows the por_hnf_sf_cxg_blocked_ways lower register bit assignments.

Table 3-491 por_hnf_por_hnf_sf_cxg_blocked_ways (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1:0	sf_blocked_ways	Number of SF ways blocked for remote chips to use in CML mode (0, 4, 8, or 12) 2'b00: No ways are blocked; all 16 SF ways could be used by local or remote RN-Fs 2'b01: Lower 4 ways are blocked from remote RN-Fs; ways 3:0 for local RN-Fs only; ways 15:4 for local and remote RN-Fs 2'b10: Lower 8 ways are blocked from remote RN-Fs; ways 7:0 for local RN-Fs only; ways 15:8 for local and remote RN-Fs 2'b11: Lower 12 ways are blocked from remote RN-Fs; ways 11:0 for local RN-Fs only; ways 15:12 for local and remote RN-Fs	RW	2'b00

por_hnf_cml_port_aggr_grp0_add_mask

Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF10

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

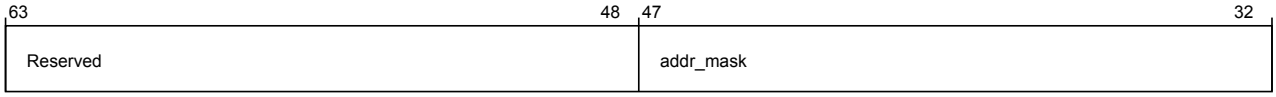


Figure 3-478 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)

The following table shows the por_hnf_cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 3-492 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

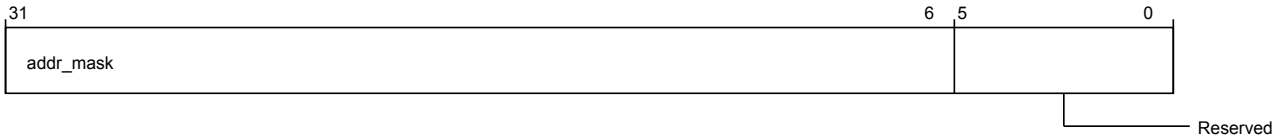


Figure 3-479 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)

The following table shows the por_hnf_cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 3-493 por_hnf_por_hnf_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

por_hnf_cml_port_aggr_grp1_add_mask

Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF18

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

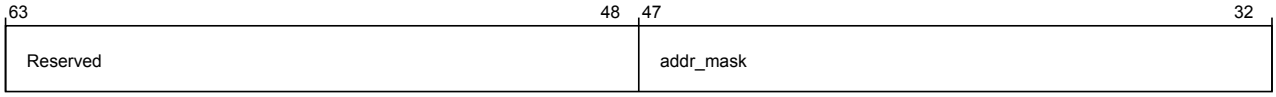


Figure 3-480 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)

The following table shows the por_hnf_cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 3-494 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

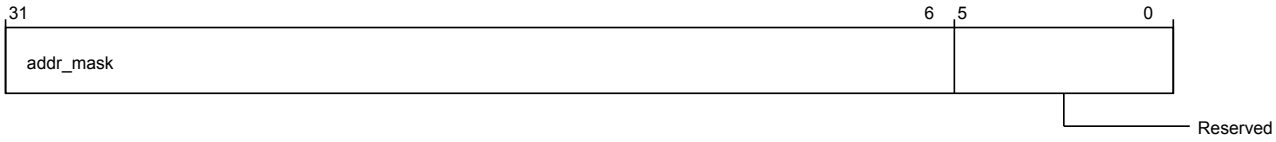


Figure 3-481 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)

The following table shows the por_hnf_cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 3-495 por_hnf_por_hnf_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

por_hnf_cml_port_aggr_grp0_reg

Configures the CCIX port aggregation port IDs for group 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

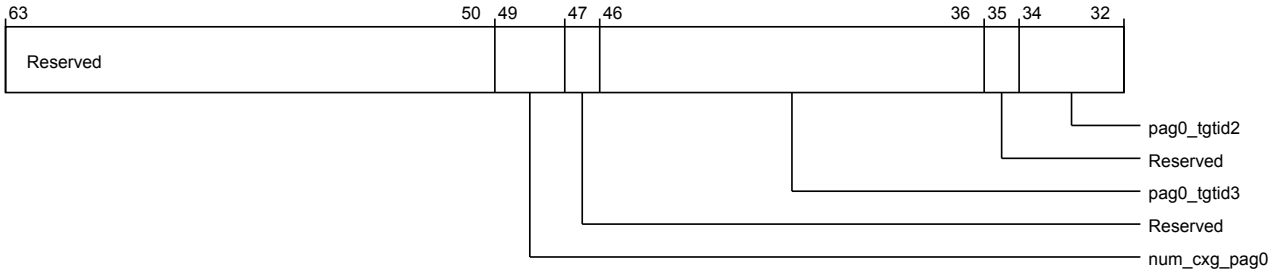


Figure 3-482 por_hnf_por_hnf_cml_port_aggr_grp0_reg (high)

The following table shows the por_hnf_cml_port_aggr_grp0_reg higher register bit assignments.

Table 3-496 por_hnf_por_hnf_cml_port_aggr_grp0_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag0	Specifies the number of CXRAs in CPAG 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag0_tgtid3	Specifies the target ID for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag0_tgtid2	Specifies the target ID for CPAG	RW	11'b0

The following image shows the lower register bit assignments.

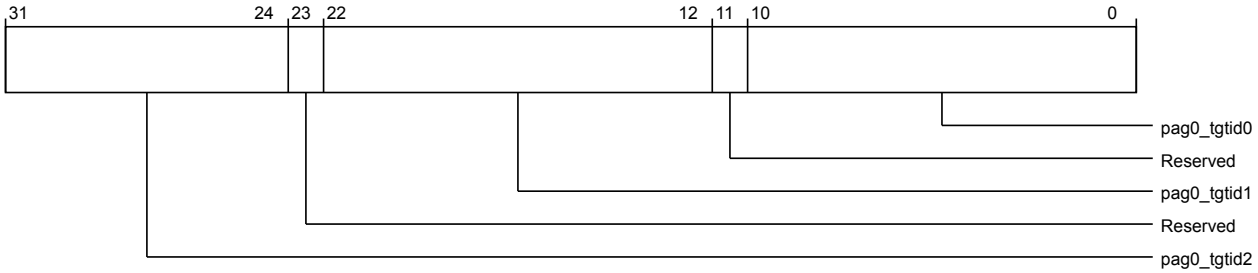


Figure 3-483 por_hnf_por_hnf_cml_port_aggr_grp0_reg (low)

The following table shows the por_hnf_cml_port_aggr_grp0_reg lower register bit assignments.

Table 3-497 por_hnf_por_hnf_cml_port_aggr_grp0_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag0_tgtid2	Specifies the target ID for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag0_tgtid1	Specifies the target ID for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag0_tgtid0	Specifies the target ID for CPAG	RW	11'b0

por_hnf_cml_port_aggr_grp1_reg

Configures the CCIX port aggregation port IDs for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

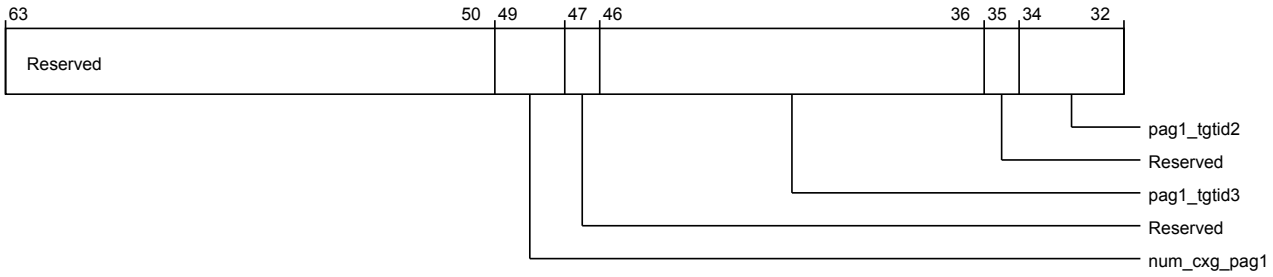


Figure 3-484 por_hnf_por_hnf_cml_port_aggr_grp1_reg (high)

The following table shows the por_hnf_cml_port_aggr_grp1_reg higher register bit assignments.

Table 3-498 por_hnf_por_hnf_cml_port_aggr_grp1_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag1	Specifies the number of CXRAs in CPAG	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag1_tgtid3	Specifies the target ID for CPAG	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag1_tgtid2	Specifies the target ID for CPAG	RW	11'b0

The following image shows the lower register bit assignments.

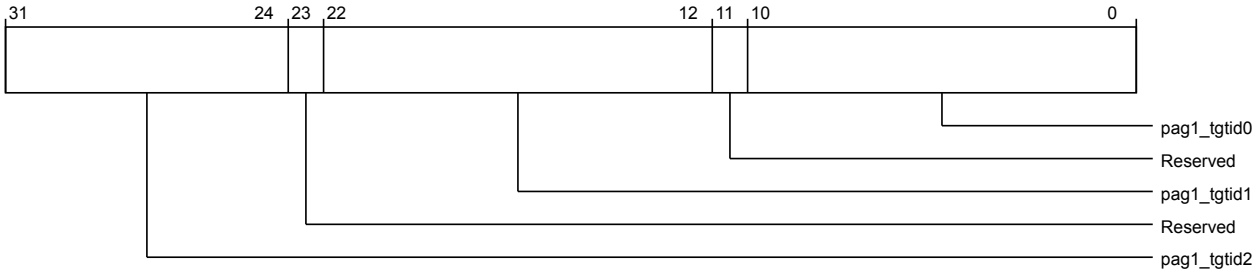


Figure 3-485 por_hnf_por_hnf_cml_port_aggr_grp1_reg (low)

The following table shows the por_hnf_cml_port_aggr_grp1_reg lower register bit assignments.

Table 3-499 por_hnf_por_hnf_cml_port_aggr_grp1_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag1_tgtid2	Specifies the target ID for CPAG	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag1_tgtid1	Specifies the target ID for CPAG	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag1_tgtid0	Specifies the target ID for CPAG	RW	11'b0

hn_sam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hF40
Register reset 64'b1111111111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

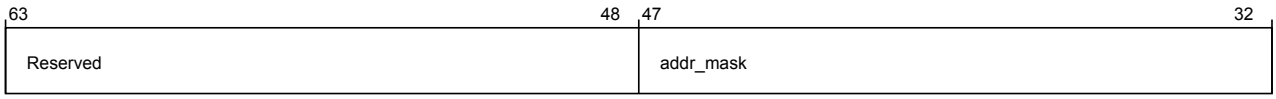


Figure 3-486 por_hnf_hn_sam_hash_addr_mask_reg (high)

The following table shows the hn_sam_hash_addr_mask_reg higher register bit assignments.

Table 3-500 por_hnf_hn_sam_hash_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF

The following image shows the lower register bit assignments.

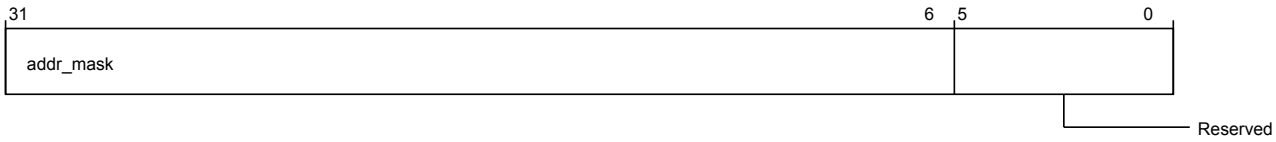


Figure 3-487 por_hnf_hn_sam_hash_addr_mask_reg (low)

The following table shows the hn_sam_hash_addr_mask_reg lower register bit assignments.

Table 3-501 por_hnf_hn_sam_hash_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF
5:0	Reserved	Reserved	RO	-

hn_sam_region_cmp_addr_mask_reg

Configures the address mask that is applied before memory region compare.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF48

Register reset 64'b11111111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

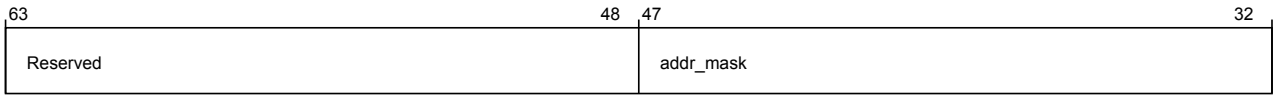


Figure 3-488 por_hnf_hn_sam_region_cmp_addr_mask_reg (high)

The following table shows the hn_sam_region_cmp_addr_mask_reg higher register bit assignments.

Table 3-502 por_hnf_hn_sam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before memory region compare	RW	22'h3FFFFF

The following image shows the lower register bit assignments.

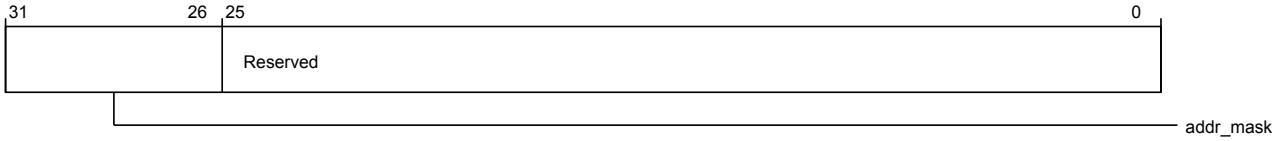


Figure 3-489 por_hnf_hn_sam_region_cmp_addr_mask_reg (low)

The following table shows the hn_sam_region_cmp_addr_mask_reg lower register bit assignments.

Table 3-503 por_hnf_hn_sam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:26	addr_mask	Address mask applied before memory region compare	RW	22'h3FFFFF
25:0	Reserved	Reserved	RO	-

por_hnf_abf_lo_addr

Lower address range for Address Based Flush (ABF) [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.

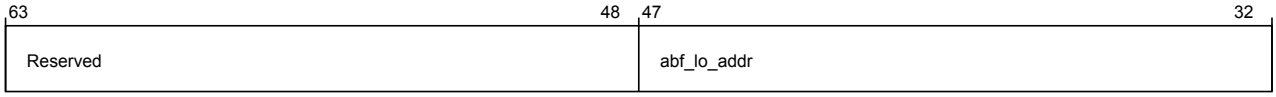


Figure 3-490 por_hnf_por_hnf_abf_lo_addr (high)

The following table shows the por_hnf_abf_lo_addr higher register bit assignments.

Table 3-504 por_hnf_por_hnf_abf_lo_addr (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	abf_lo_addr	Lower address range for ABF	RW	48'b0

The following image shows the lower register bit assignments.

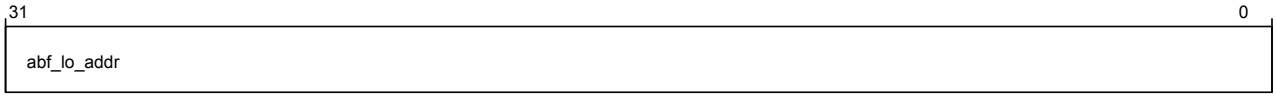


Figure 3-491 por_hnf_por_hnf_abf_lo_addr (low)

The following table shows the por_hnf_abf_lo_addr lower register bit assignments.

Table 3-505 por_hnf_por_hnf_abf_lo_addr (low)

Bits	Field name	Description	Type	Reset
31:0	abf_lo_addr	Lower address range for ABF	RW	48'b0

por_hnf_abf_hi_addr

Upper address range for Address Based Flush (ABF) [47:0].

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.

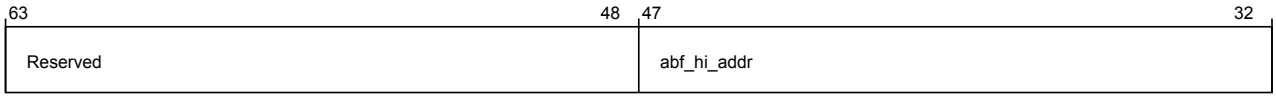


Figure 3-492 por_hnf_por_hnf_abf_hi_addr (high)

The following table shows the por_hnf_abf_hi_addr higher register bit assignments.

Table 3-506 por_hnf_por_hnf_abf_hi_addr (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	abf_hi_addr	Upper address range for ABF	RW	48'b0

The following image shows the lower register bit assignments.

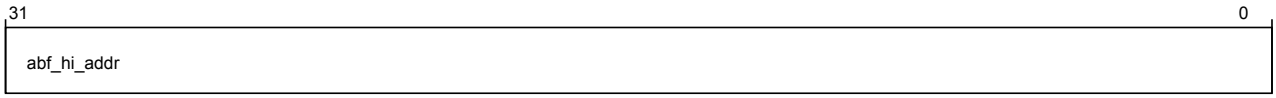


Figure 3-493 por_hnf_por_hnf_abf_hi_addr (low)

The following table shows the por_hnf_abf_hi_addr lower register bit assignments.

Table 3-507 por_hnf_por_hnf_abf_hi_addr (low)

Bits	Field name	Description	Type	Reset
31:0	abf_hi_addr	Upper address range for ABF	RW	48'b0

por_hnf_abf_pr

Functions as the Address Based Flush (ABF) policy register.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hnf_secure_register_groups_override.ppu

The following image shows the higher register bit assignments.

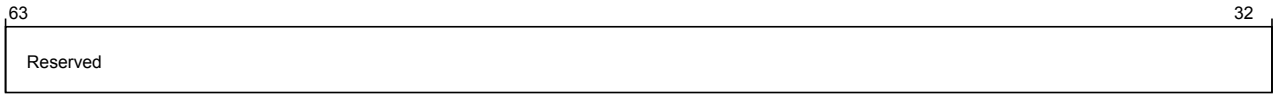


Figure 3-494 por_hnf_por_hnf_abf_pr (high)

The following table shows the por_hnf_abf_pr higher register bit assignments.

Table 3-508 por_hnf_por_hnf_abf_pr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

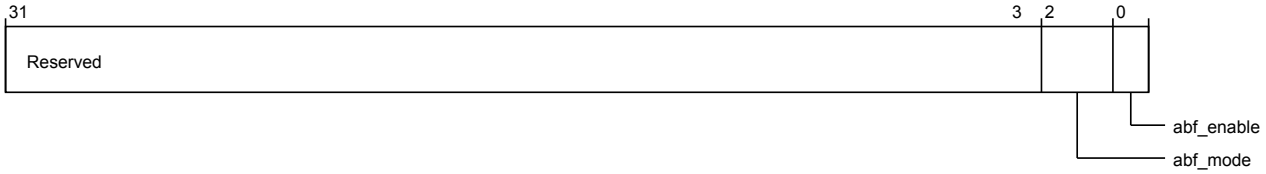


Figure 3-495 por_hnf_por_hnf_abf_pr (low)

The following table shows the por_hnf_abf_pr lower register bit assignments.

Table 3-509 por_hnf_por_hnf_abf_pr (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:1	abf_mode	ABF mode 2'b00: Clean Invalidate; WB dirty data and invalidate local copy 2'b01: Make Invalidate; invalidate without writing back dirty data 2'b10: Clean Shared; WB dirty data and can keep clean copy 2'b11: Reserved	RW	2'b00
0	abf_enable	Start Address Based Flushing based on high and low address ranges	RW	1'b0

por_hnf_abf_sr

Functions as the Address Based Flush (ABF) status register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hF68

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

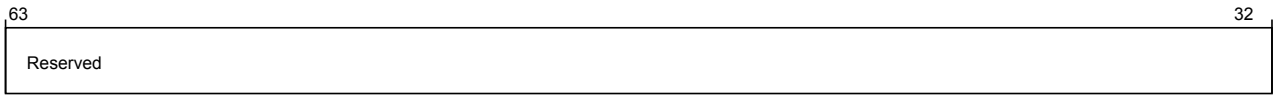


Figure 3-496 por_hnf_por_hnf_abf_sr (high)

The following table shows the por_hnf_abf_sr higher register bit assignments.

Table 3-510 por_hnf_por_hnf_abf_sr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

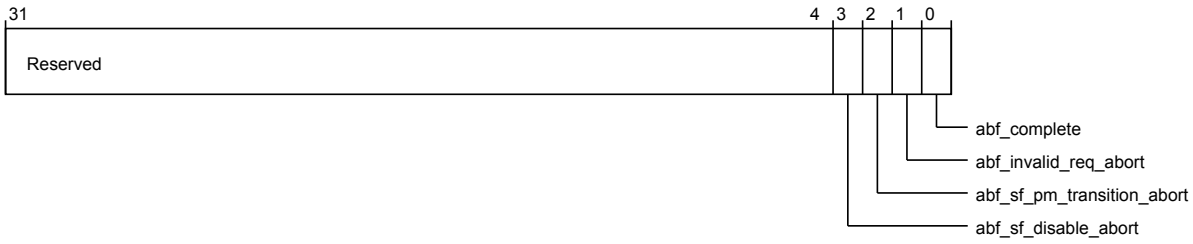


Figure 3-497 por_hnf_por_hnf_abf_sr (low)

The following table shows the por_hnf_abf_sr lower register bit assignments.

Table 3-511 por_hnf_por_hnf_abf_sr (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	abf_sf_disable_abort	ABF aborted due to SF not being enabled, either by configuration or double-bit ECC error	RO	1'b0
2	abf_sf_pm_transition_abort	ABF aborted due to PM transition while ABF in progress, or both PM and ABF requested at the same time	RO	1'b0
1	abf_invalid_req_abort	ABF request made while PM is not in FAM/HAM/SF_ONLY mode; request aborted in this case	RO	1'b0
0	abf_complete	ABF completed	RO	1'b0

por_hnf_rn_phys_id32

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'hE28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

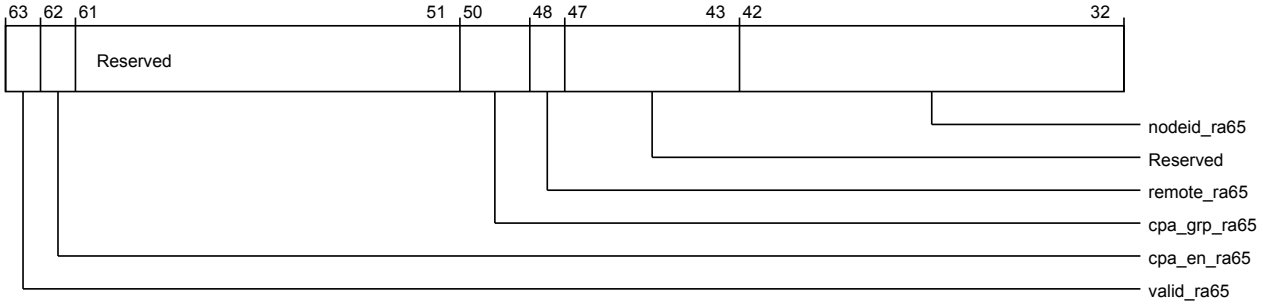


Figure 3-498 por_hnf_por_hnf_rn_phys_id32 (high)

The following table shows the por_hnf_rn_phys_id32 higher register bit assignments.

Table 3-512 por_hnf_por_hnf_rn_phys_id32 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra65	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra65	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra65	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra65	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra65	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

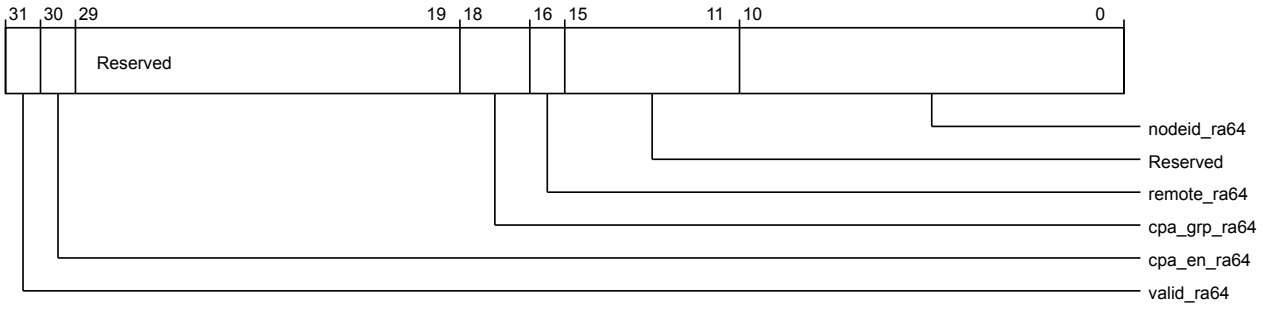


Figure 3-499 por_hnf_por_hnf_rn_phys_id32 (low)

The following table shows the por_hnf_rn_phys_id32 lower register bit assignments.

Table 3-513 por_hnf_por_hnf_rn_phys_id32 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra64	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra64	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra64	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra64	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra64	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id33

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

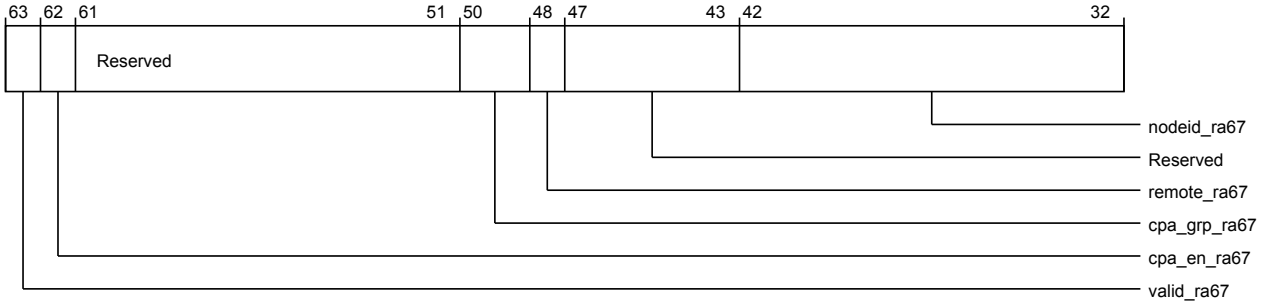


Figure 3-500 por_hnf_por_hnf_rn_phys_id33 (high)

The following table shows the por_hnf_rn_phys_id33 higher register bit assignments.

Table 3-514 por_hnf_por_hnf_rn_phys_id33 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra67	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra67	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra67	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra67	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra67	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

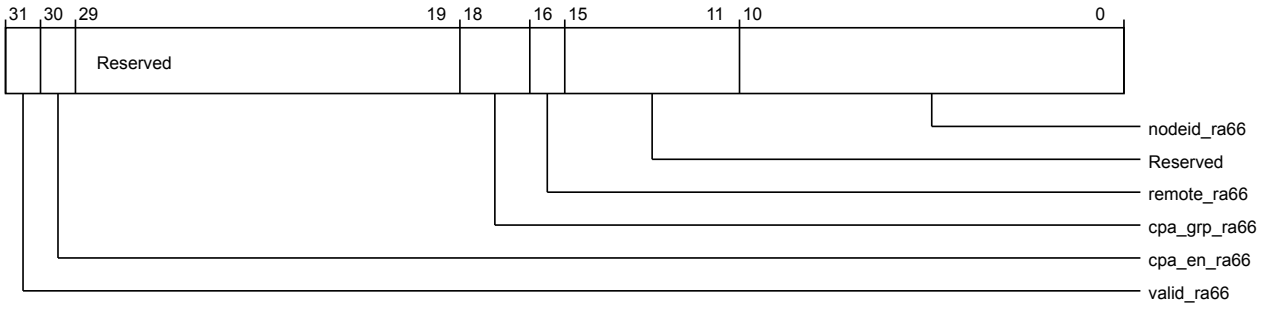


Figure 3-501 por_hnf_por_hnf_rn_phys_id33 (low)

The following table shows the por_hnf_rn_phys_id33 lower register bit assignments.

Table 3-515 por_hnf_por_hnf_rn_phys_id33 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra66	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra66	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra66	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra66	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra66	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id34

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

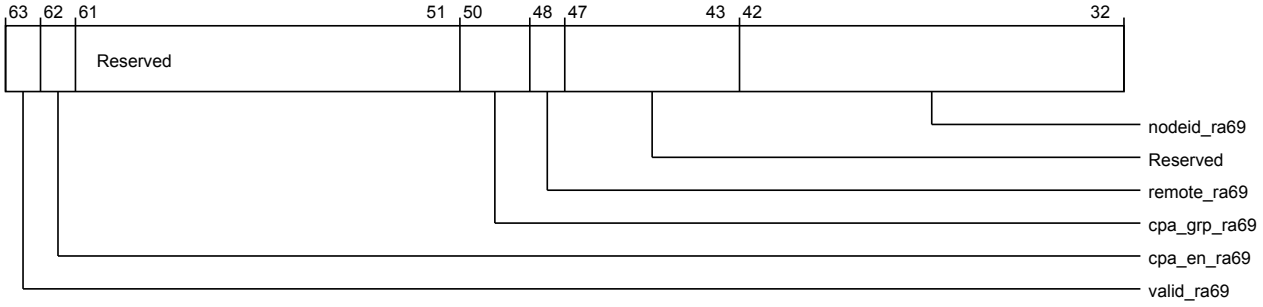


Figure 3-502 por_hnf_por_hnf_rn_phys_id34 (high)

The following table shows the por_hnf_rn_phys_id34 higher register bit assignments.

Table 3-516 por_hnf_por_hnf_rn_phys_id34 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra69	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra69	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra69	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra69	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra69	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

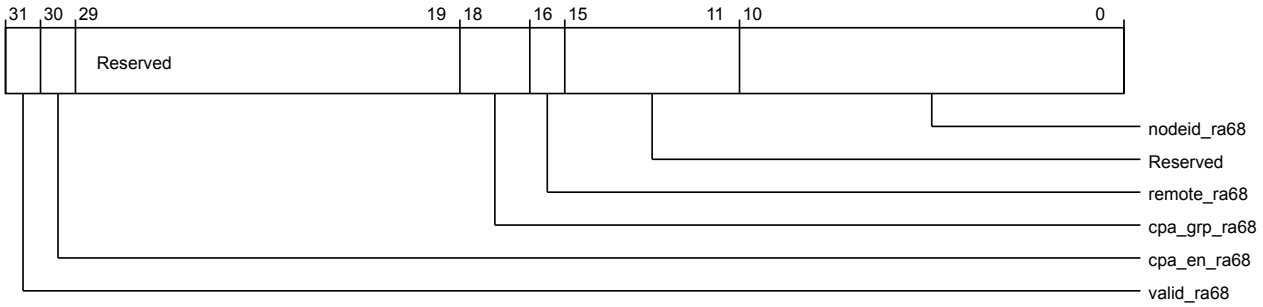


Figure 3-503 por_hnf_por_hnf_rn_phys_id34 (low)

The following table shows the por_hnf_rn_phys_id34 lower register bit assignments.

Table 3-517 por_hnf_por_hnf_rn_phys_id34 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra68	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra68	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra68	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra68	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra68	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id35

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE40

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

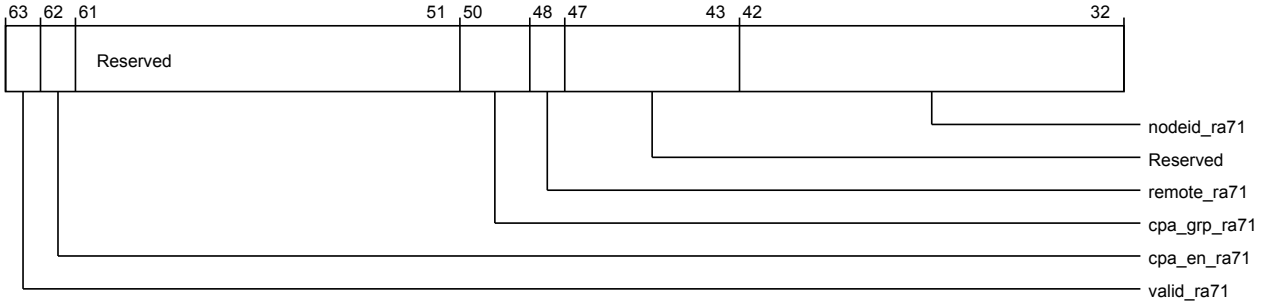


Figure 3-504 por_hnf_por_hnf_rn_phys_id35 (high)

The following table shows the por_hnf_rn_phys_id35 higher register bit assignments.

Table 3-518 por_hnf_por_hnf_rn_phys_id35 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra71	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra71	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra71	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra71	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra71	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

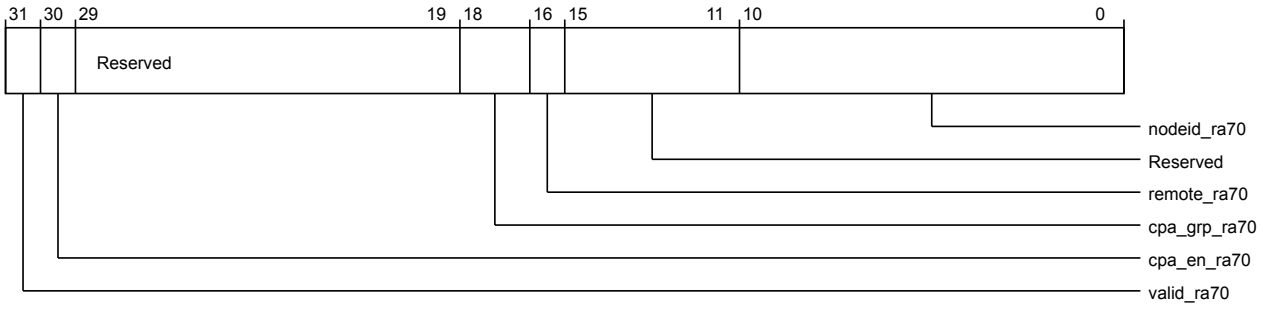


Figure 3-505 por_hnf_por_hnf_rn_phys_id35 (low)

The following table shows the por_hnf_rn_phys_id35 lower register bit assignments.

Table 3-519 por_hnf_por_hnf_rn_phys_id35 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra70	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra70	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra70	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra70	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra70	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id36

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

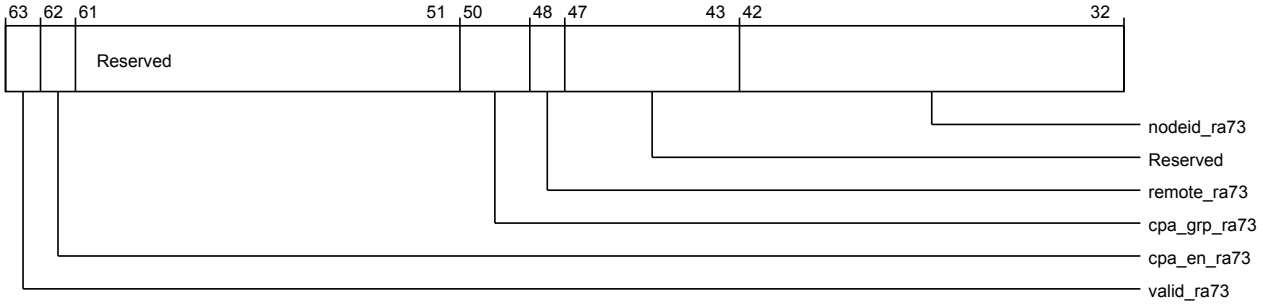


Figure 3-506 por_hnf_por_hnf_rn_phys_id36 (high)

The following table shows the por_hnf_rn_phys_id36 higher register bit assignments.

Table 3-520 por_hnf_por_hnf_rn_phys_id36 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra73	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra73	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra73	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra73	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra73	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

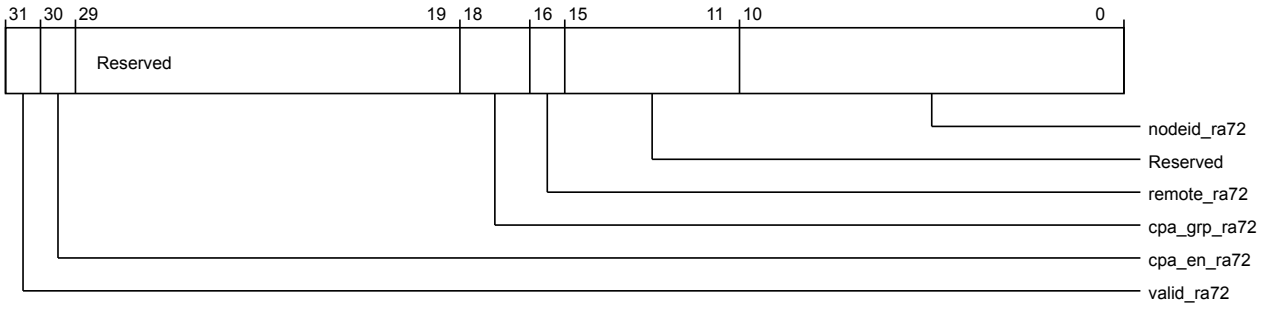


Figure 3-507 por_hnf_por_hnf_rn_phys_id36 (low)

The following table shows the por_hnf_rn_phys_id36 lower register bit assignments.

Table 3-521 por_hnf_por_hnf_rn_phys_id36 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra72	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra72	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra72	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra72	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra72	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id37

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

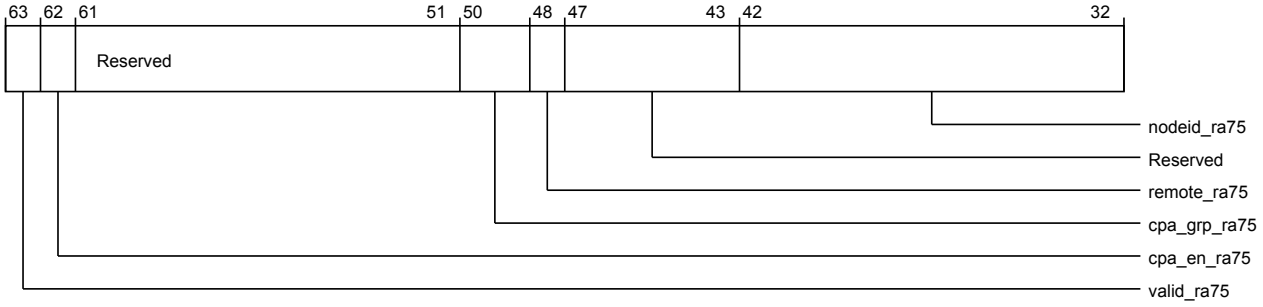


Figure 3-508 por_hnf_por_hnf_rn_phys_id37 (high)

The following table shows the por_hnf_rn_phys_id37 higher register bit assignments.

Table 3-522 por_hnf_por_hnf_rn_phys_id37 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra75	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra75	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra75	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra75	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra75	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

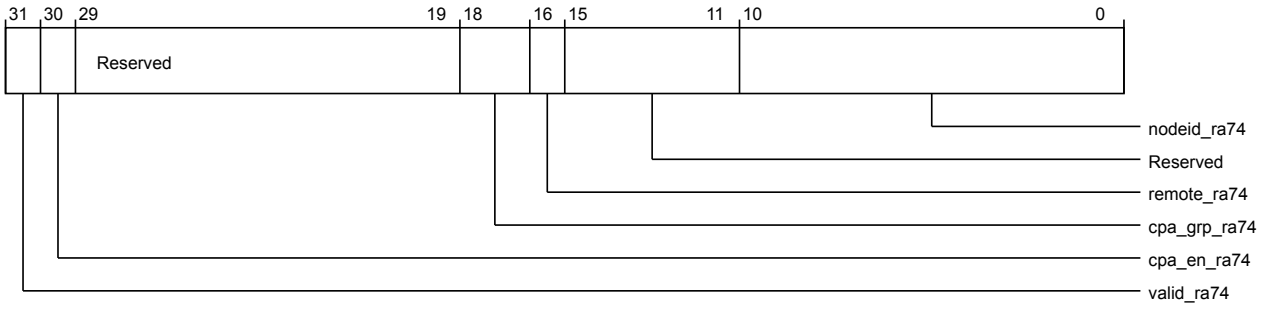


Figure 3-509 por_hnf_por_hnf_rn_phys_id37 (low)

The following table shows the por_hnf_rn_phys_id37 lower register bit assignments.

Table 3-523 por_hnf_por_hnf_rn_phys_id37 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra74	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra74	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra74	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra74	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra74	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id38

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

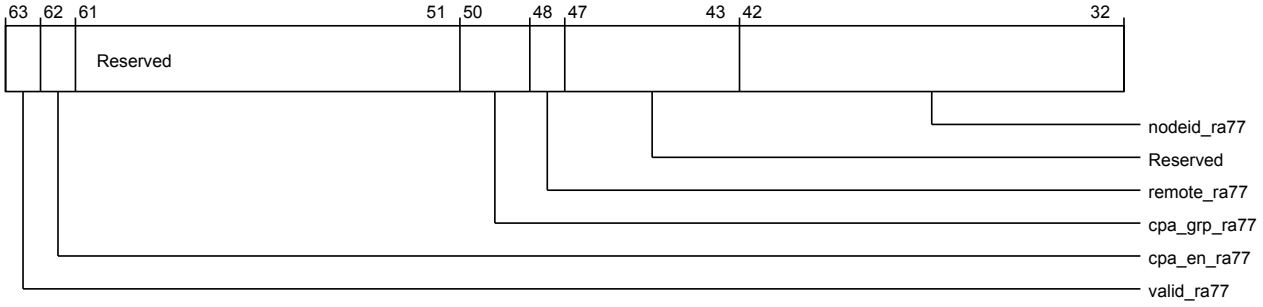


Figure 3-510 por_hnf_por_hnf_rn_phys_id38 (high)

The following table shows the por_hnf_rn_phys_id38 higher register bit assignments.

Table 3-524 por_hnf_por_hnf_rn_phys_id38 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra77	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra77	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra77	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra77	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra77	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

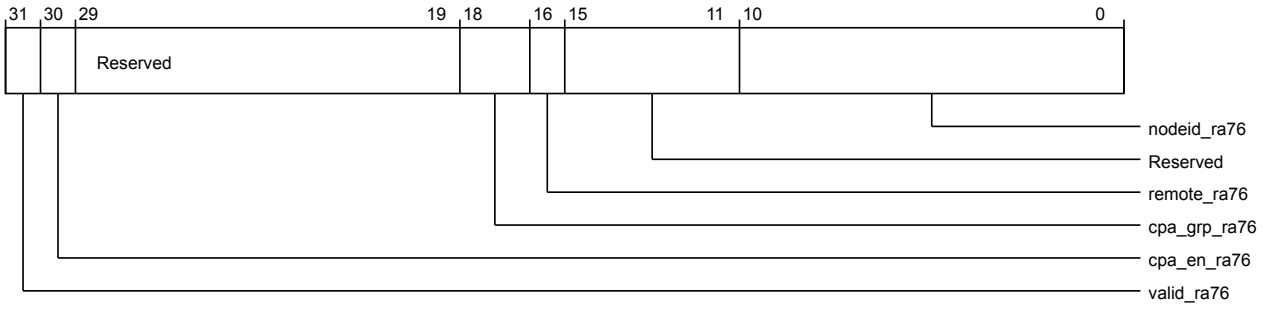


Figure 3-511 por_hnf_por_hnf_rn_phys_id38 (low)

The following table shows the por_hnf_rn_phys_id38 lower register bit assignments.

Table 3-525 por_hnf_por_hnf_rn_phys_id38 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra76	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra76	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra76	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra76	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra76	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id39

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

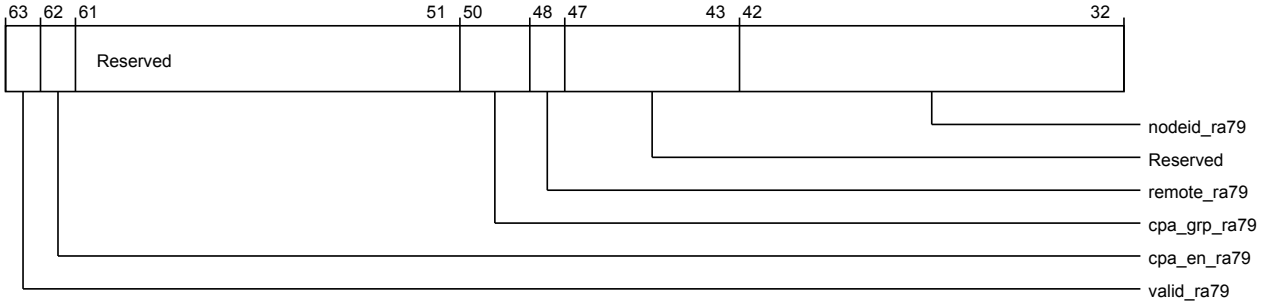


Figure 3-512 por_hnf_por_hnf_rn_phys_id39 (high)

The following table shows the por_hnf_rn_phys_id39 higher register bit assignments.

Table 3-526 por_hnf_por_hnf_rn_phys_id39 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra79	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra79	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra79	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra79	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra79	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

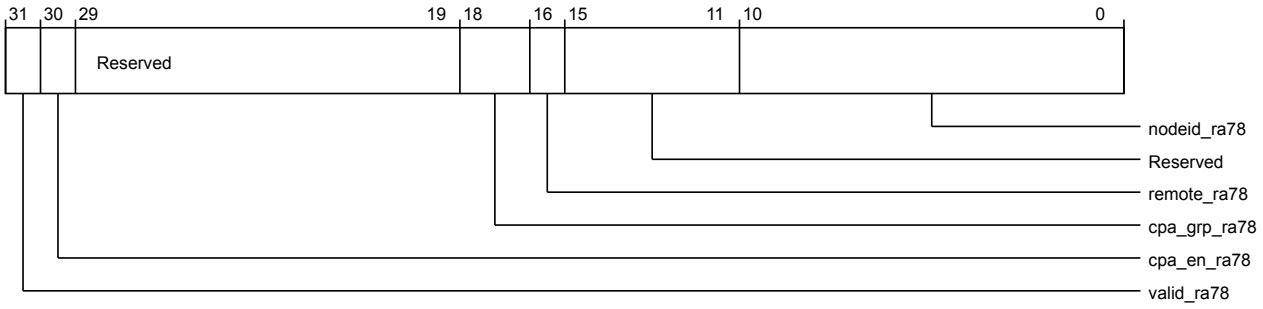


Figure 3-513 por_hnf_por_hnf_rn_phys_id39 (low)

The following table shows the por_hnf_rn_phys_id39 lower register bit assignments.

Table 3-527 por_hnf_por_hnf_rn_phys_id39 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra78	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra78	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra78	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra78	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra78	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id40

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

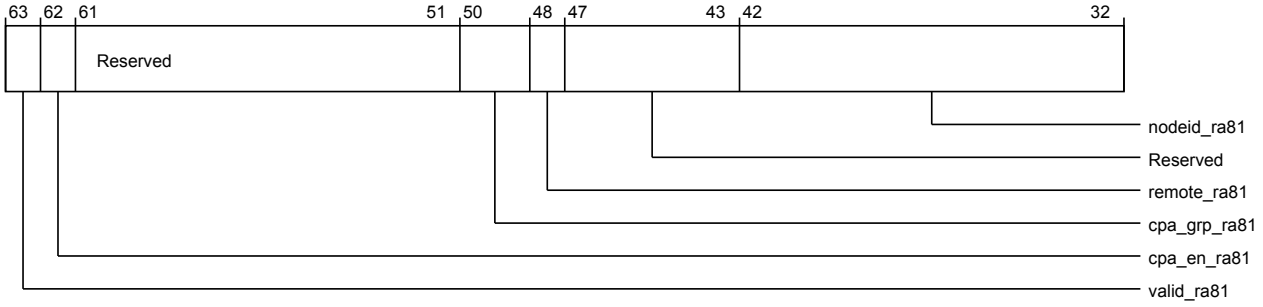


Figure 3-514 por_hnf_por_hnf_rn_phys_id40 (high)

The following table shows the por_hnf_rn_phys_id40 higher register bit assignments.

Table 3-528 por_hnf_por_hnf_rn_phys_id40 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra81	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra81	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra81	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra81	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra81	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

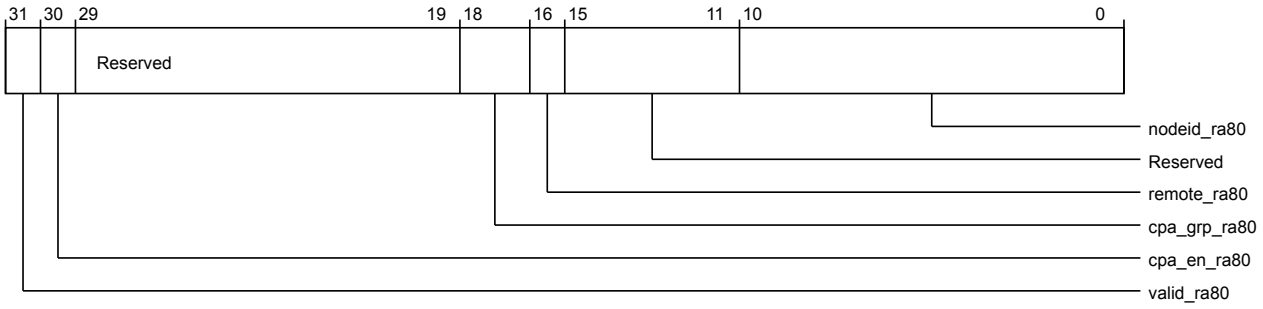


Figure 3-515 por_hnf_por_hnf_rn_phys_id40 (low)

The following table shows the por_hnf_rn_phys_id40 lower register bit assignments.

Table 3-529 por_hnf_por_hnf_rn_phys_id40 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra80	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra80	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra80	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra80	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra80	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id41

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

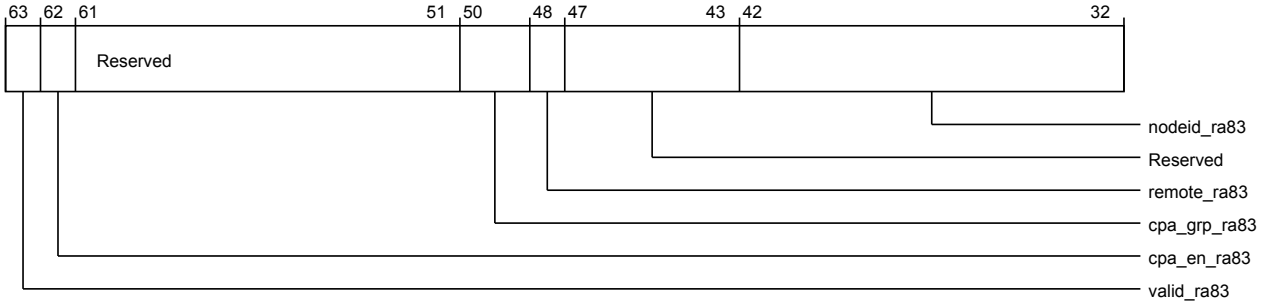


Figure 3-516 por_hnf_por_hnf_rn_phys_id41 (high)

The following table shows the por_hnf_rn_phys_id41 higher register bit assignments.

Table 3-530 por_hnf_por_hnf_rn_phys_id41 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra83	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra83	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra83	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra83	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra83	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

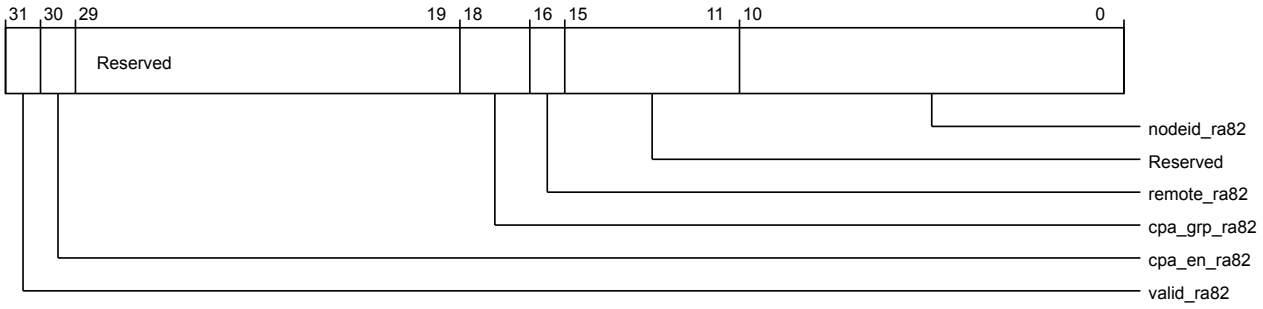


Figure 3-517 por_hnf_por_hnf_rn_phys_id41 (low)

The following table shows the por_hnf_rn_phys_id41 lower register bit assignments.

Table 3-531 por_hnf_por_hnf_rn_phys_id41 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra82	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra82	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra82	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra82	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra82	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id42

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

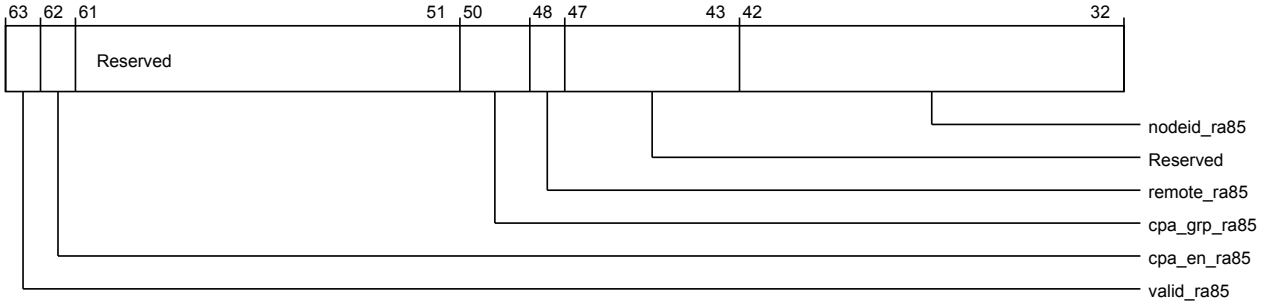


Figure 3-518 por_hnf_por_hnf_rn_phys_id42 (high)

The following table shows the por_hnf_rn_phys_id42 higher register bit assignments.

Table 3-532 por_hnf_por_hnf_rn_phys_id42 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra85	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra85	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra85	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra85	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra85	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

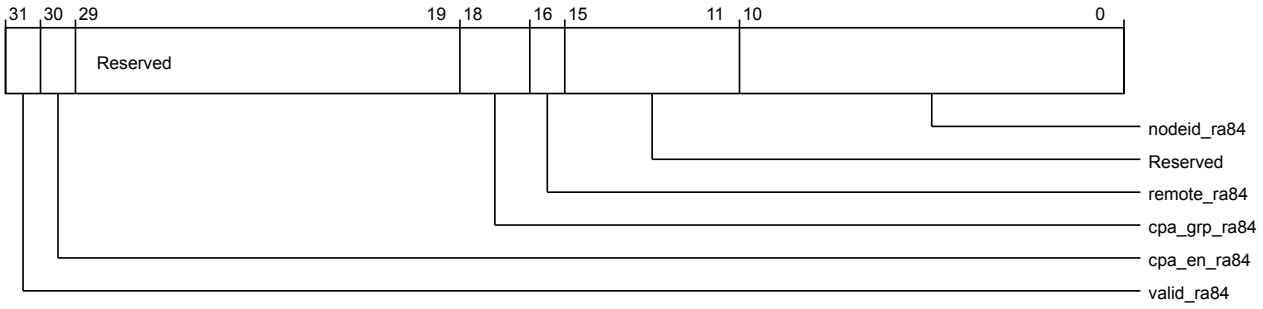


Figure 3-519 por_hnf_por_hnf_rn_phys_id42 (low)

The following table shows the por_hnf_rn_phys_id42 lower register bit assignments.

Table 3-533 por_hnf_por_hnf_rn_phys_id42 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra84	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra84	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra84	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra84	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra84	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id43

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

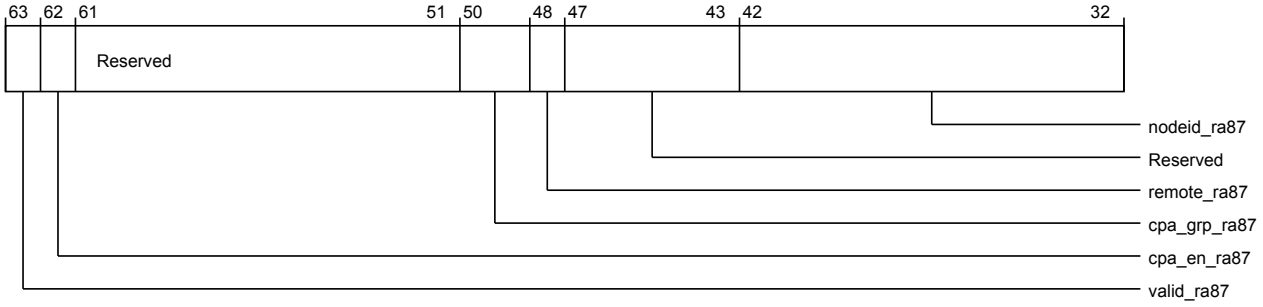


Figure 3-520 por_hnf_por_hnf_rn_phys_id43 (high)

The following table shows the por_hnf_rn_phys_id43 higher register bit assignments.

Table 3-534 por_hnf_por_hnf_rn_phys_id43 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra87	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra87	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra87	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra87	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra87	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

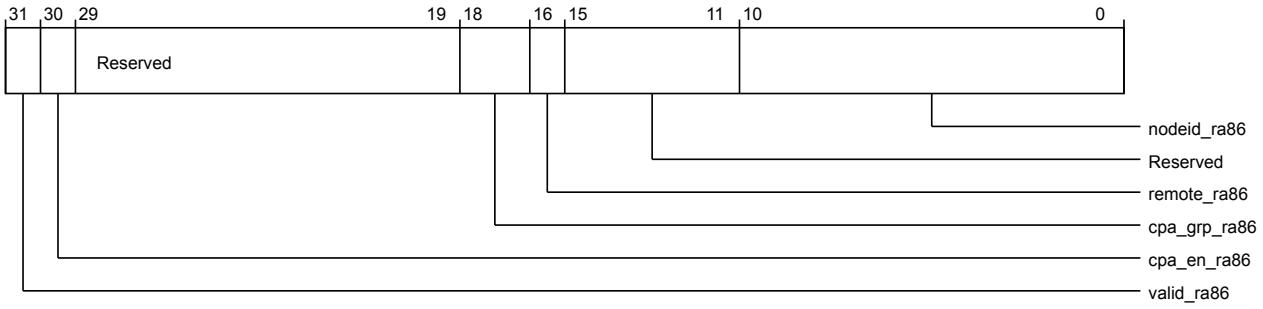


Figure 3-521 por_hnf_por_hnf_rn_phys_id43 (low)

The following table shows the por_hnf_rn_phys_id43 lower register bit assignments.

Table 3-535 por_hnf_por_hnf_rn_phys_id43 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra86	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra86	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra86	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra86	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra86	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id44

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

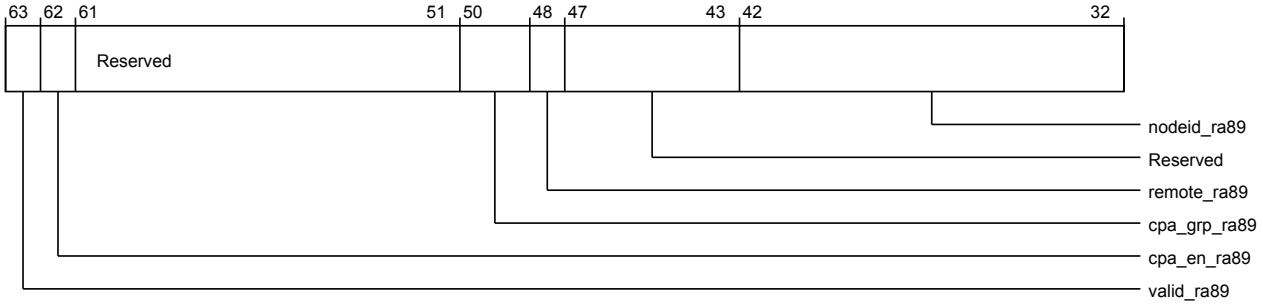


Figure 3-522 por_hnf_por_hnf_rn_phys_id44 (high)

The following table shows the por_hnf_rn_phys_id44 higher register bit assignments.

Table 3-536 por_hnf_por_hnf_rn_phys_id44 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra89	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra89	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra89	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra89	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra89	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

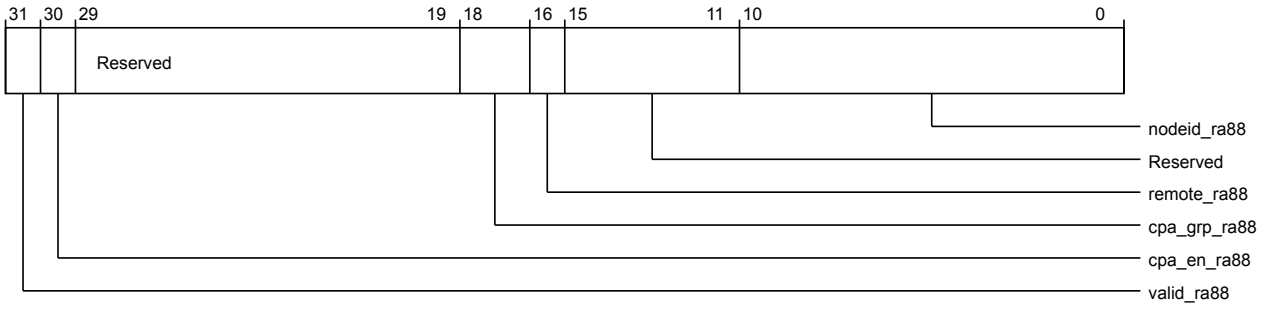


Figure 3-523 por_hnf_por_hnf_rn_phys_id44 (low)

The following table shows the por_hnf_rn_phys_id44 lower register bit assignments.

Table 3-537 por_hnf_por_hnf_rn_phys_id44 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra88	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra88	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra88	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra88	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra88	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id45

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

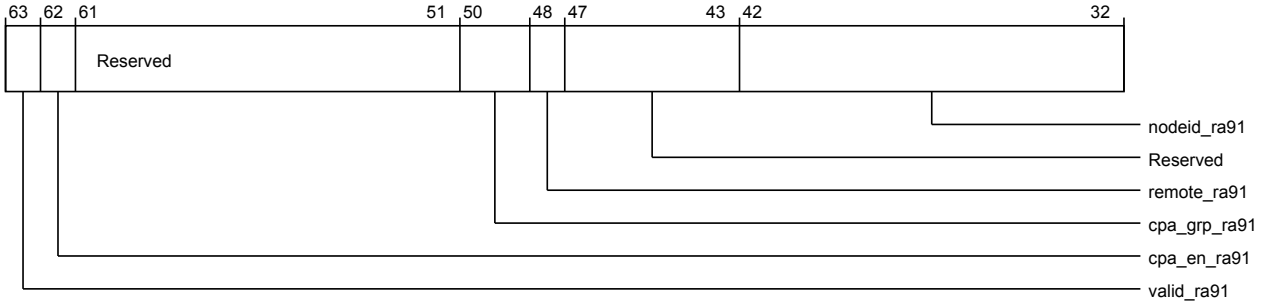


Figure 3-524 por_hnf_por_hnf_rn_phys_id45 (high)

The following table shows the por_hnf_rn_phys_id45 higher register bit assignments.

Table 3-538 por_hnf_por_hnf_rn_phys_id45 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra91	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra91	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra91	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra91	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra91	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

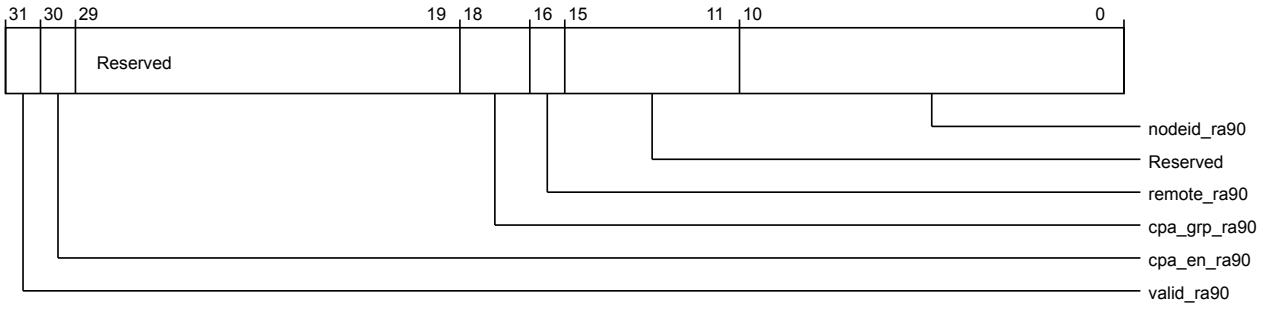


Figure 3-525 por_hnf_por_hnf_rn_phys_id45 (low)

The following table shows the por_hnf_rn_phys_id45 lower register bit assignments.

Table 3-539 por_hnf_por_hnf_rn_phys_id45 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra90	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra90	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra90	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra90	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra90	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id46

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

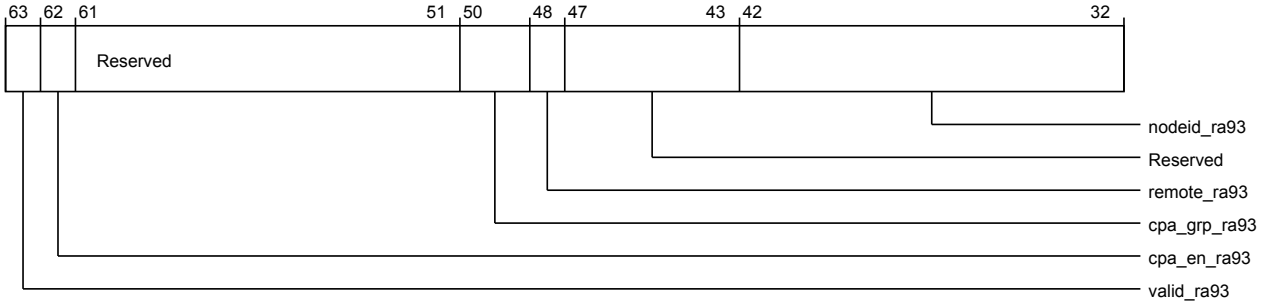


Figure 3-526 por_hnf_por_hnf_rn_phys_id46 (high)

The following table shows the por_hnf_rn_phys_id46 higher register bit assignments.

Table 3-540 por_hnf_por_hnf_rn_phys_id46 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra93	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra93	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra93	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra93	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra93	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

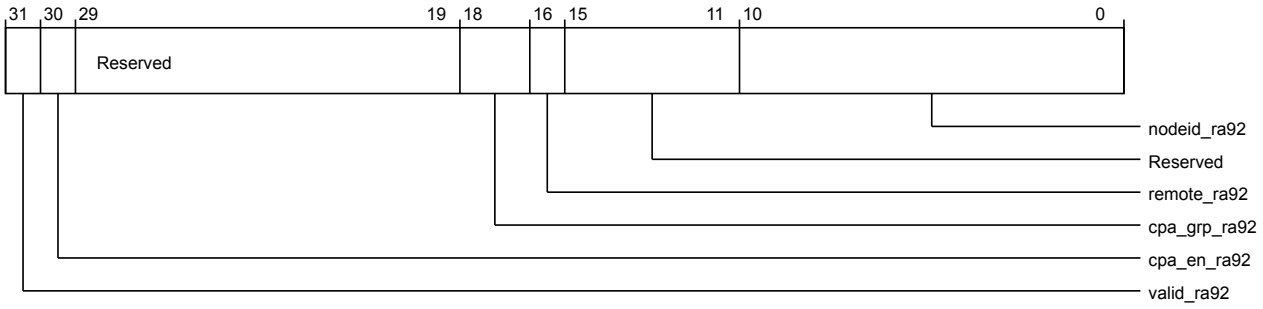


Figure 3-527 por_hnf_por_hnf_rn_phys_id46 (low)

The following table shows the por_hnf_rn_phys_id46 lower register bit assignments.

Table 3-541 por_hnf_por_hnf_rn_phys_id46 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra92	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra92	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra92	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra92	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra92	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id47

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

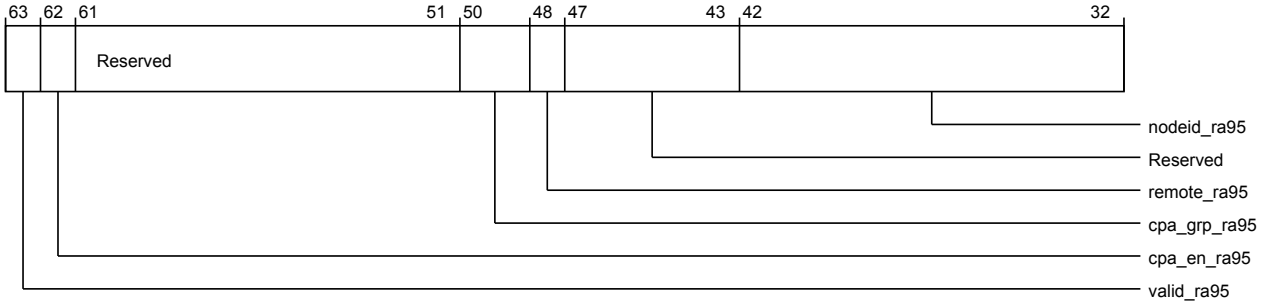


Figure 3-528 por_hnf_por_hnf_rn_phys_id47 (high)

The following table shows the por_hnf_rn_phys_id47 higher register bit assignments.

Table 3-542 por_hnf_por_hnf_rn_phys_id47 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra95	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra95	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra95	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra95	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra95	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

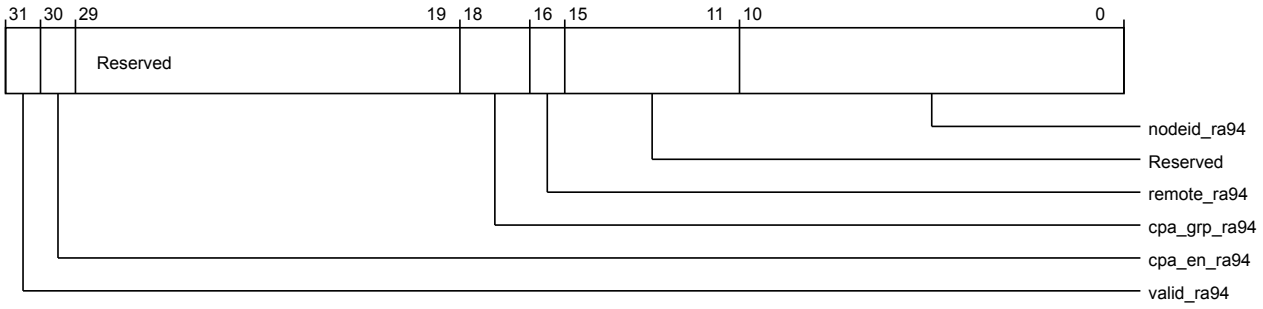


Figure 3-529 por_hnf_por_hnf_rn_phys_id47 (low)

The following table shows the por_hnf_rn_phys_id47 lower register bit assignments.

Table 3-543 por_hnf_por_hnf_rn_phys_id47 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra94	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra94	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra94	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra94	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra94	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id48

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

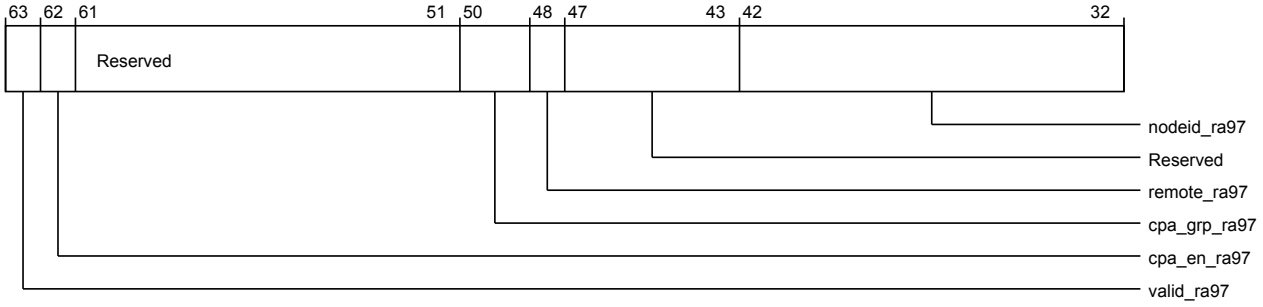


Figure 3-530 por_hnf_por_hnf_rn_phys_id48 (high)

The following table shows the por_hnf_rn_phys_id48 higher register bit assignments.

Table 3-544 por_hnf_por_hnf_rn_phys_id48 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra97	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra97	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra97	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra97	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra97	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

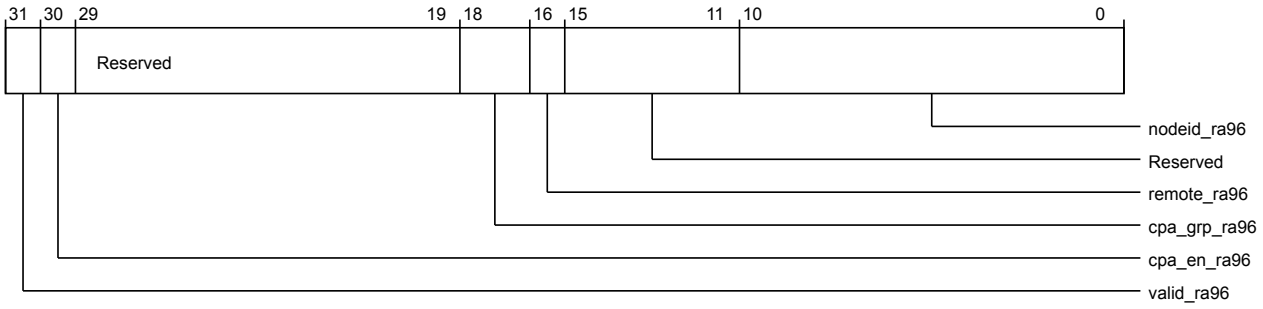


Figure 3-531 por_hnf_por_hnf_rn_phys_id48 (low)

The following table shows the por_hnf_rn_phys_id48 lower register bit assignments.

Table 3-545 por_hnf_por_hnf_rn_phys_id48 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra96	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra96	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra96	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra96	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra96	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id49

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

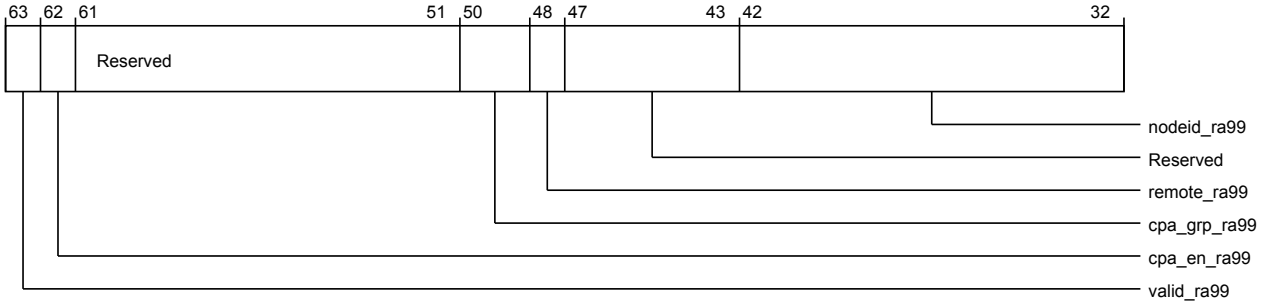


Figure 3-532 por_hnf_por_hnf_rn_phys_id49 (high)

The following table shows the por_hnf_rn_phys_id49 higher register bit assignments.

Table 3-546 por_hnf_por_hnf_rn_phys_id49 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra99	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra99	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra99	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra99	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra99	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

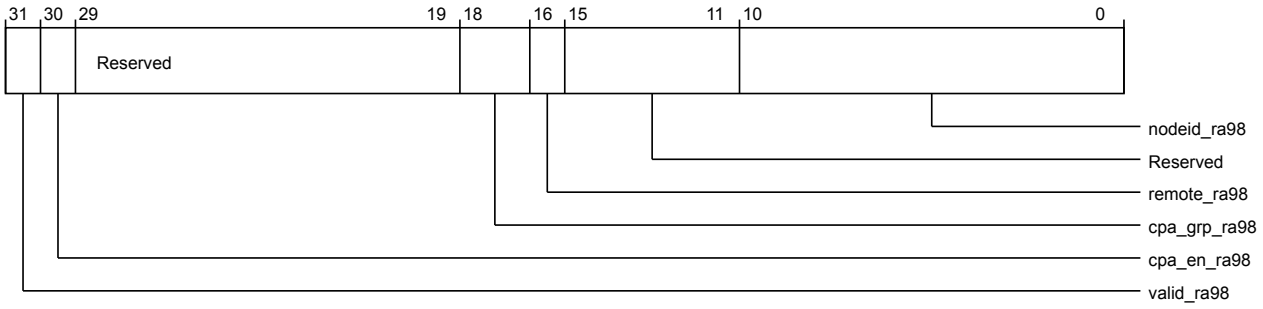


Figure 3-533 por_hnf_por_hnf_rn_phys_id49 (low)

The following table shows the por_hnf_rn_phys_id49 lower register bit assignments.

Table 3-547 por_hnf_por_hnf_rn_phys_id49 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra98	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra98	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra98	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra98	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra98	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id50

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

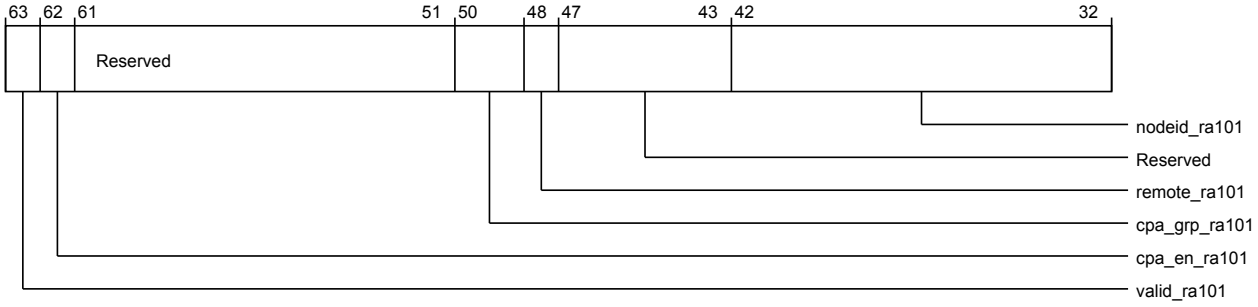


Figure 3-534 por_hnf_por_hnf_rn_phys_id50 (high)

The following table shows the por_hnf_rn_phys_id50 higher register bit assignments.

Table 3-548 por_hnf_por_hnf_rn_phys_id50 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra101	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra101	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra101	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra101	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra101	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

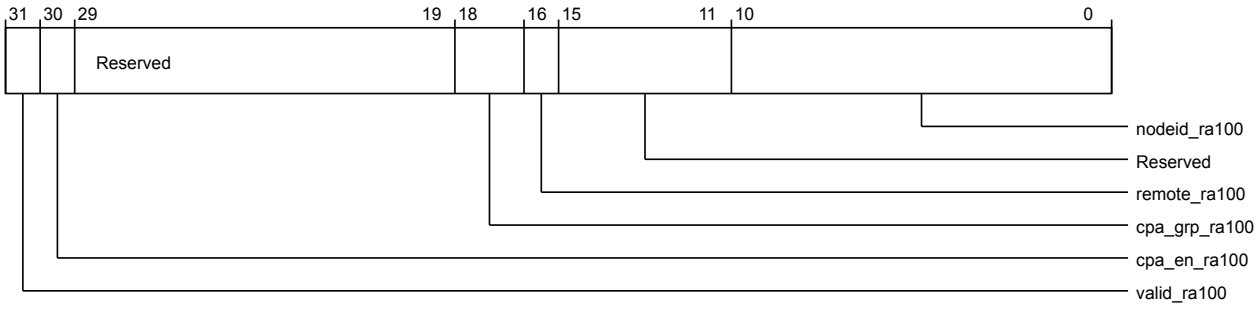


Figure 3-535 por_hnf_por_hnf_rn_phys_id50 (low)

The following table shows the por_hnf_rn_phys_id50 lower register bit assignments.

Table 3-549 por_hnf_por_hnf_rn_phys_id50 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra100	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra100	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra100	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra100	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra100	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id51

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

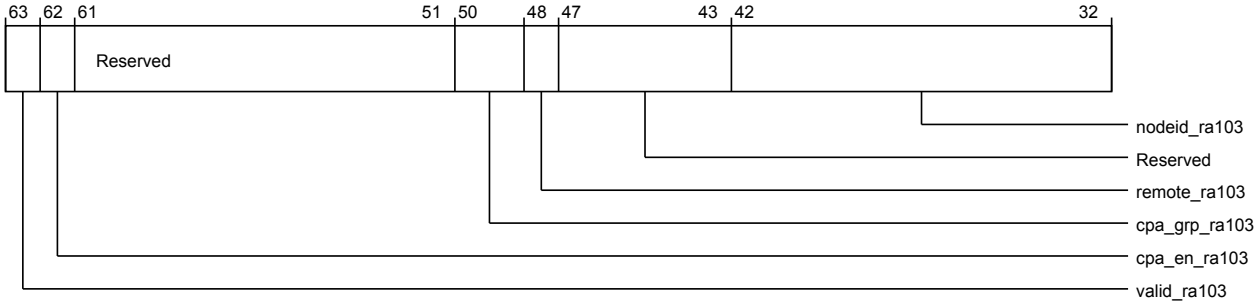


Figure 3-536 por_hnf_por_hnf_rn_phys_id51 (high)

The following table shows the por_hnf_rn_phys_id51 higher register bit assignments.

Table 3-550 por_hnf_por_hnf_rn_phys_id51 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra103	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra103	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra103	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra103	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra103	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

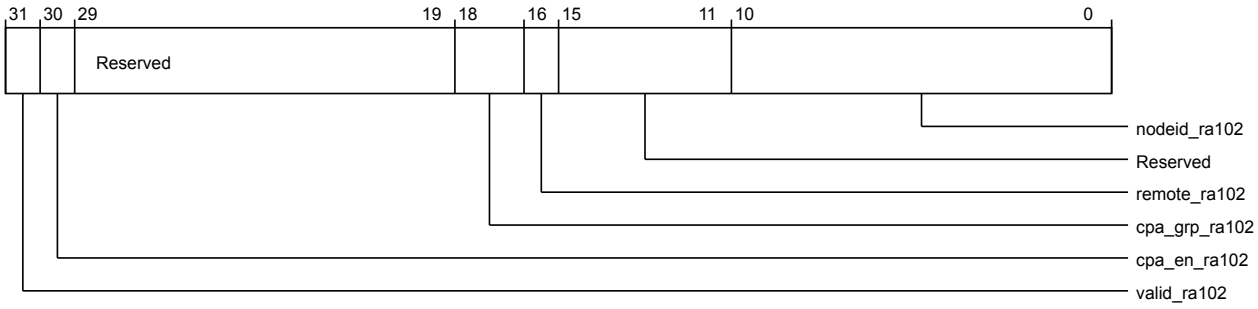


Figure 3-537 por_hnf_por_hnf_rn_phys_id51 (low)

The following table shows the por_hnf_rn_phys_id51 lower register bit assignments.

Table 3-551 por_hnf_por_hnf_rn_phys_id51 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra102	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra102	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra102	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra102	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra102	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id52

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

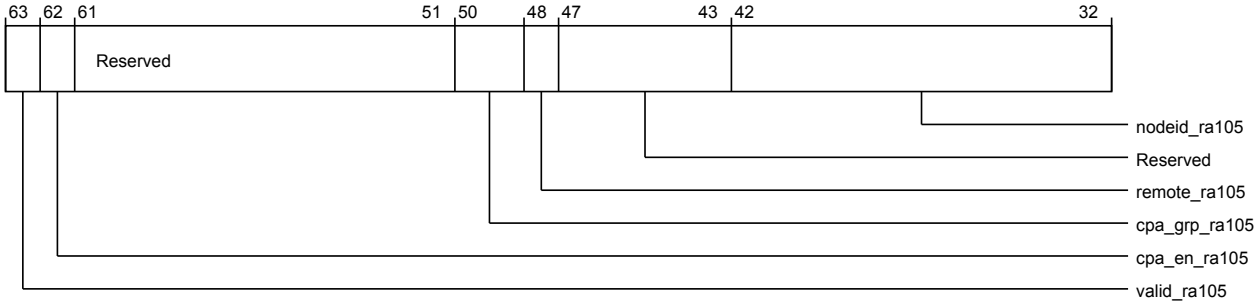


Figure 3-538 por_hnf_por_hnf_rn_phys_id52 (high)

The following table shows the por_hnf_rn_phys_id52 higher register bit assignments.

Table 3-552 por_hnf_por_hnf_rn_phys_id52 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra105	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra105	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra105	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra105	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra105	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

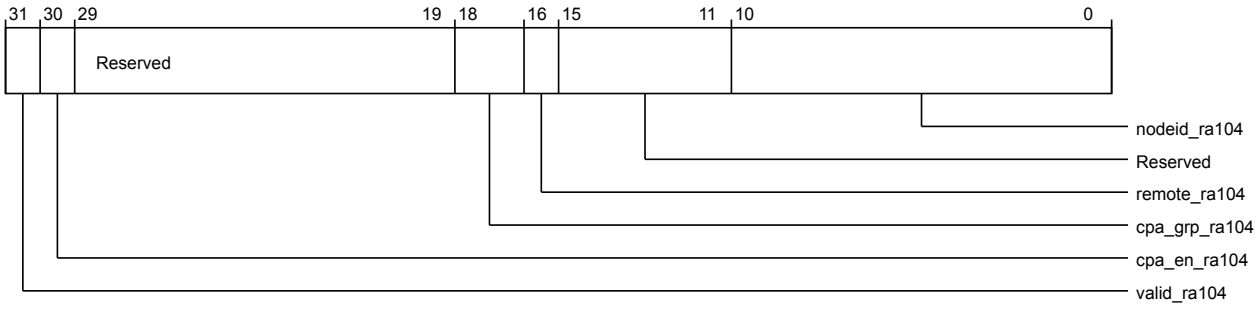


Figure 3-539 por_hnf_por_hnf_rn_phys_id52 (low)

The following table shows the por_hnf_rn_phys_id52 lower register bit assignments.

Table 3-553 por_hnf_por_hnf_rn_phys_id52 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra104	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra104	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra104	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra104	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra104	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id53

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

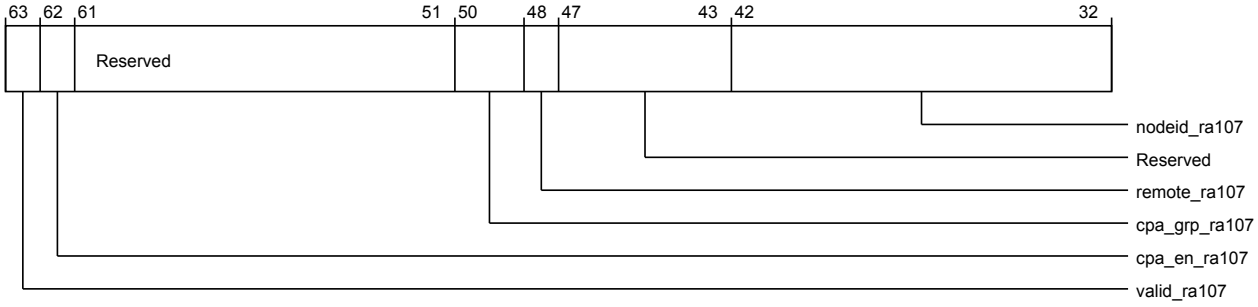


Figure 3-540 por_hnf_por_hnf_rn_phys_id53 (high)

The following table shows the por_hnf_rn_phys_id53 higher register bit assignments.

Table 3-554 por_hnf_por_hnf_rn_phys_id53 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra107	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra107	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra107	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra107	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra107	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

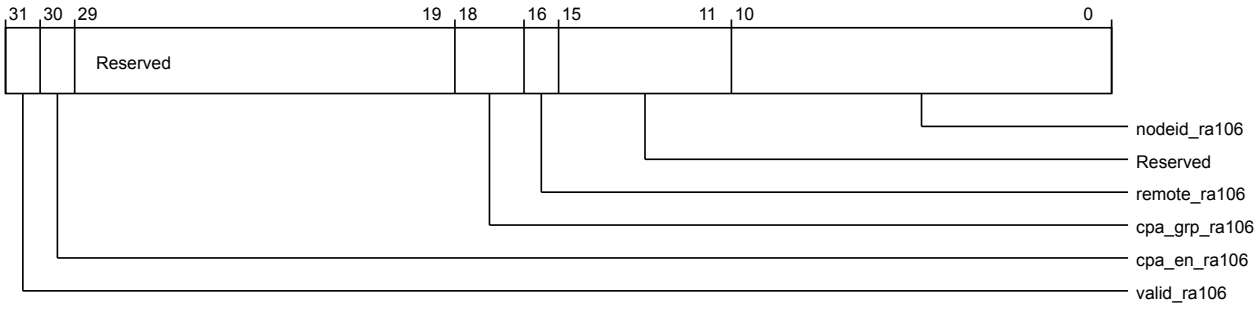


Figure 3-541 por_hnf_por_hnf_rn_phys_id53 (low)

The following table shows the por_hnf_rn_phys_id53 lower register bit assignments.

Table 3-555 por_hnf_por_hnf_rn_phys_id53 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra106	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra106	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra106	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra106	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra106	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id54

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

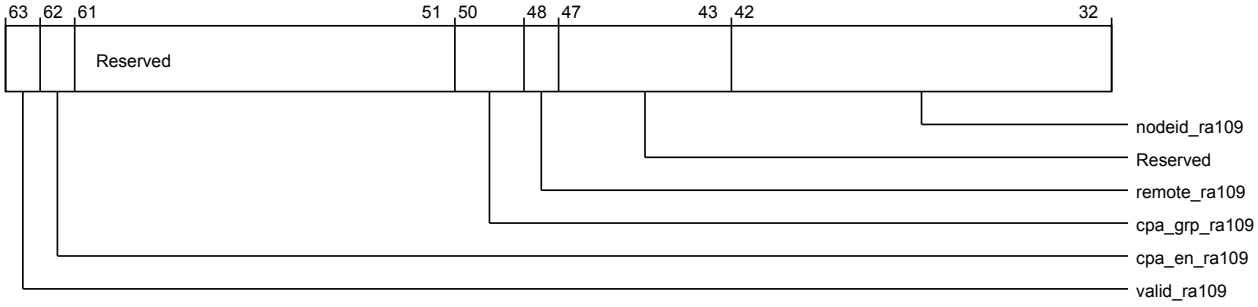


Figure 3-542 por_hnf_por_hnf_rn_phys_id54 (high)

The following table shows the por_hnf_rn_phys_id54 higher register bit assignments.

Table 3-556 por_hnf_por_hnf_rn_phys_id54 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra109	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra109	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra109	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra109	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra109	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

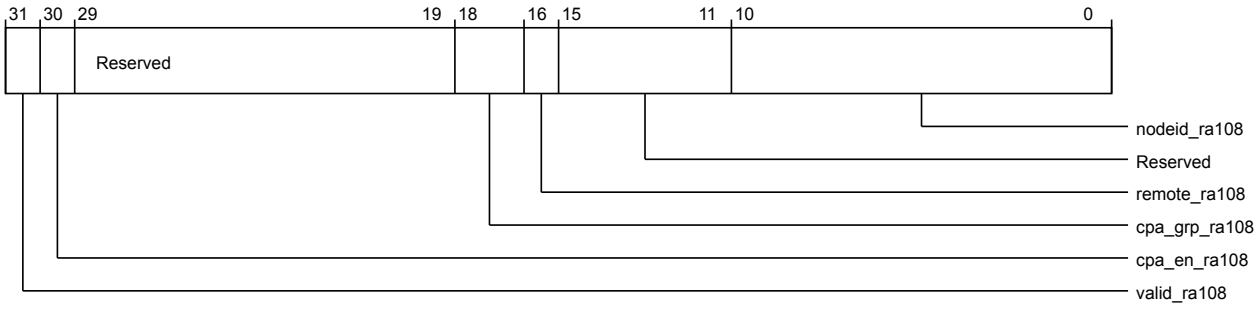


Figure 3-543 por_hnf_por_hnf_rn_phys_id54 (low)

The following table shows the por_hnf_rn_phys_id54 lower register bit assignments.

Table 3-557 por_hnf_por_hnf_rn_phys_id54 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra108	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra108	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra108	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra108	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra108	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id55

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

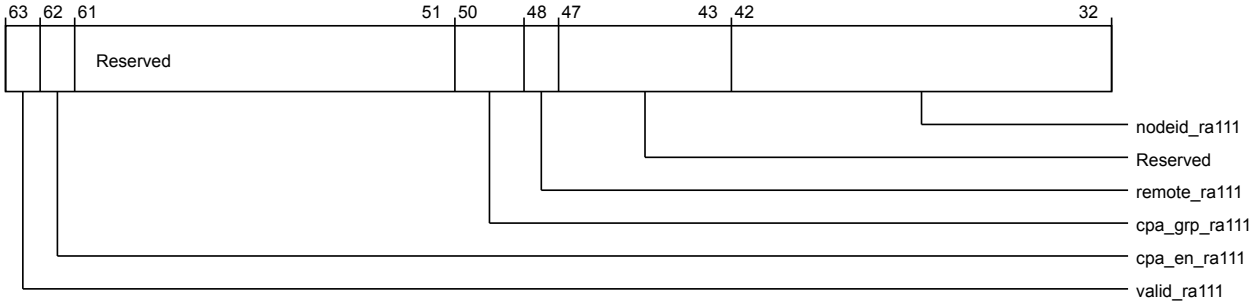


Figure 3-544 por_hnf_por_hnf_rn_phys_id55 (high)

The following table shows the por_hnf_rn_phys_id55 higher register bit assignments.

Table 3-558 por_hnf_por_hnf_rn_phys_id55 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra111	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra111	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra111	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra111	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra111	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

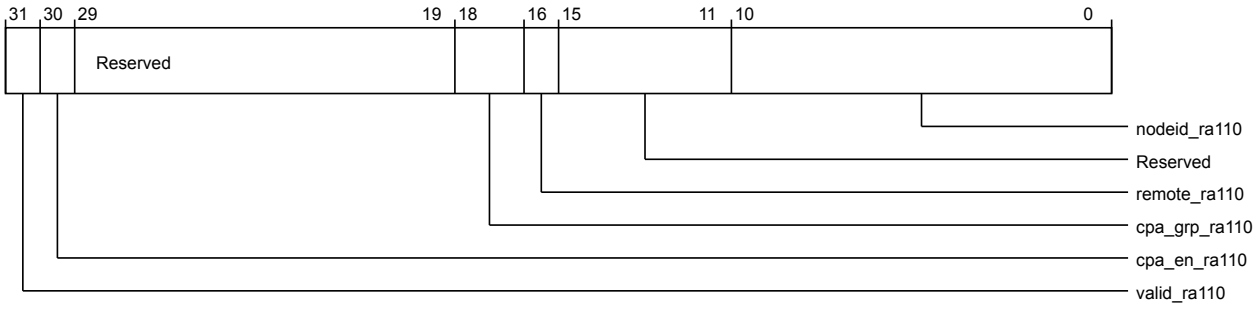


Figure 3-545 por_hnf_por_hnf_rn_phys_id55 (low)

The following table shows the por_hnf_rn_phys_id55 lower register bit assignments.

Table 3-559 por_hnf_por_hnf_rn_phys_id55 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra110	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra110	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra110	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra110	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra110	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id56

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

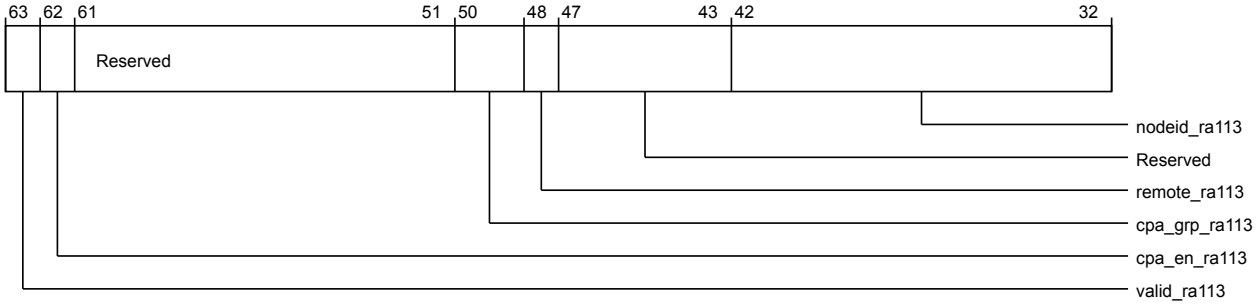


Figure 3-546 por_hnf_por_hnf_rn_phys_id56 (high)

The following table shows the por_hnf_rn_phys_id56 higher register bit assignments.

Table 3-560 por_hnf_por_hnf_rn_phys_id56 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra113	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra113	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra113	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra113	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra113	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

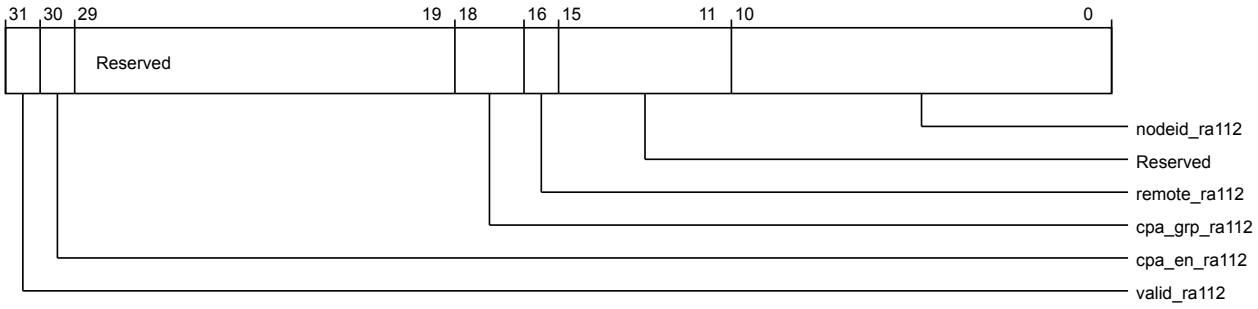


Figure 3-547 por_hnf_por_hnf_rn_phys_id56 (low)

The following table shows the por_hnf_rn_phys_id56 lower register bit assignments.

Table 3-561 por_hnf_por_hnf_rn_phys_id56 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra112	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra112	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra112	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra112	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra112	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id57

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

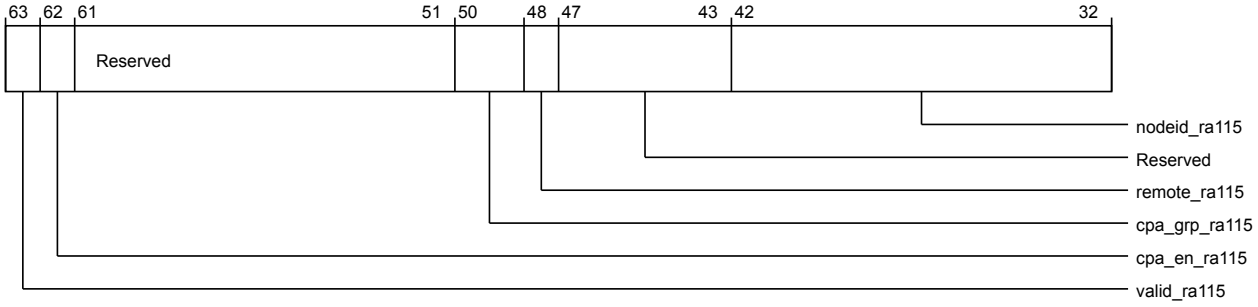


Figure 3-548 por_hnf_por_hnf_rn_phys_id57 (high)

The following table shows the por_hnf_rn_phys_id57 higher register bit assignments.

Table 3-562 por_hnf_por_hnf_rn_phys_id57 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra115	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra115	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra115	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra115	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra115	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

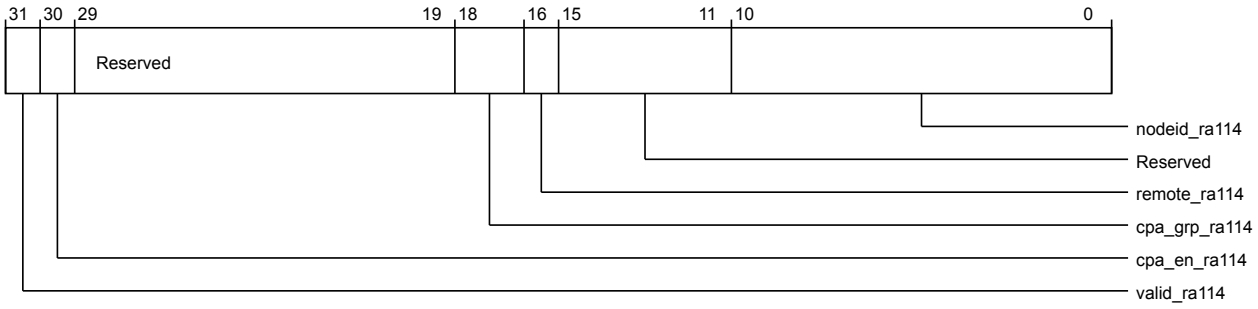


Figure 3-549 por_hnf_por_hnf_rn_phys_id57 (low)

The following table shows the por_hnf_rn_phys_id57 lower register bit assignments.

Table 3-563 por_hnf_por_hnf_rn_phys_id57 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra114	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra114	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra114	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra114	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra114	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id58

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

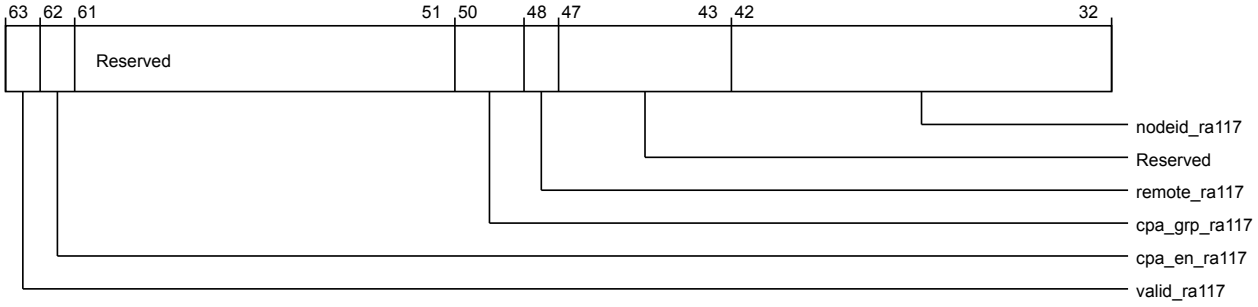


Figure 3-550 por_hnf_por_hnf_rn_phys_id58 (high)

The following table shows the por_hnf_rn_phys_id58 higher register bit assignments.

Table 3-564 por_hnf_por_hnf_rn_phys_id58 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra117	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra117	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra117	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra117	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra117	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

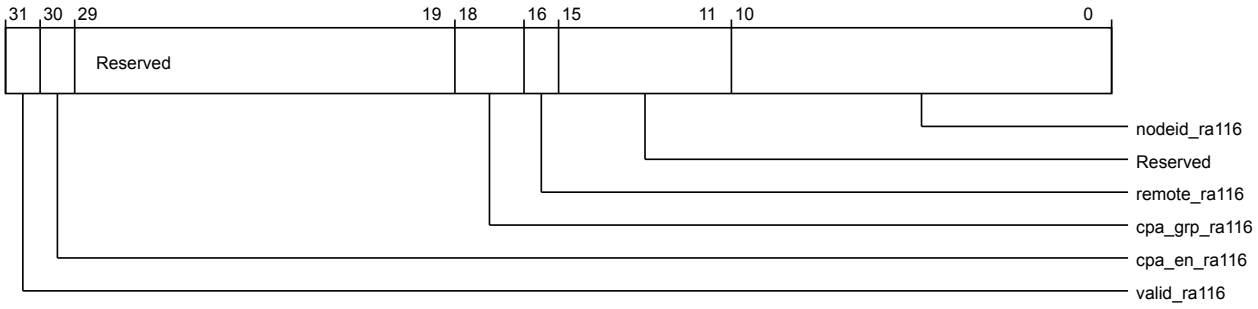


Figure 3-551 por_hnf_por_hnf_rn_phys_id58 (low)

The following table shows the por_hnf_rn_phys_id58 lower register bit assignments.

Table 3-565 por_hnf_por_hnf_rn_phys_id58 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra116	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra116	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra116	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra116	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra116	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id59

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

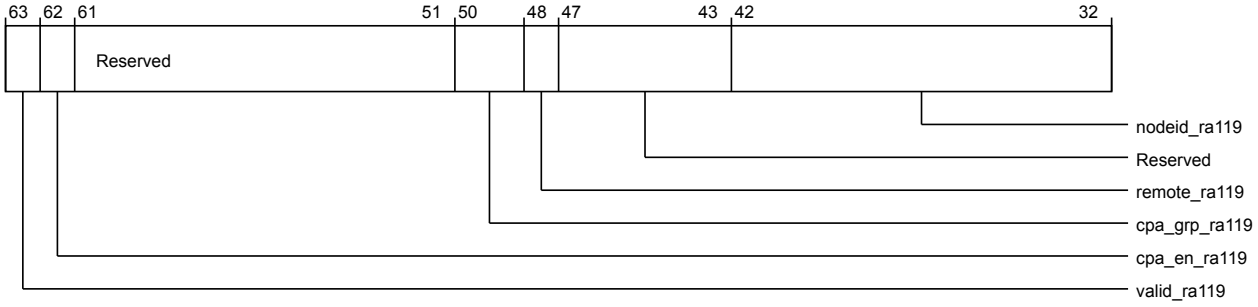


Figure 3-552 por_hnf_por_hnf_rn_phys_id59 (high)

The following table shows the por_hnf_rn_phys_id59 higher register bit assignments.

Table 3-566 por_hnf_por_hnf_rn_phys_id59 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra119	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra119	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra119	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra119	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra119	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

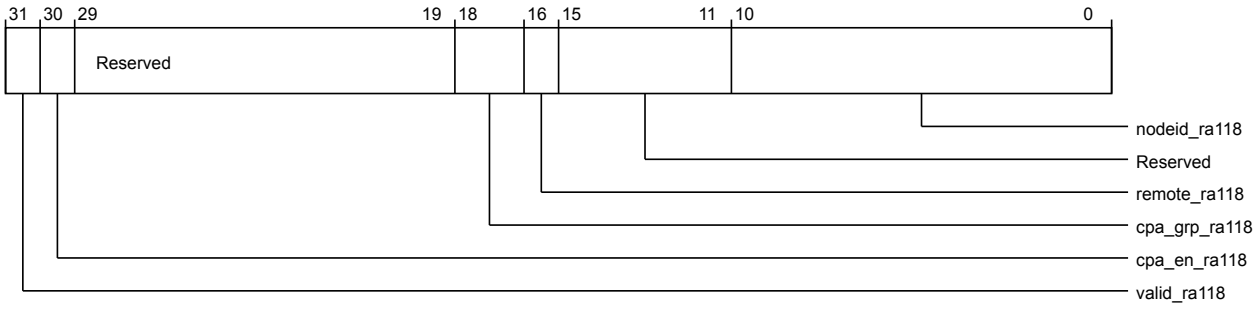


Figure 3-553 por_hnf_por_hnf_rn_phys_id59 (low)

The following table shows the por_hnf_rn_phys_id59 lower register bit assignments.

Table 3-567 por_hnf_por_hnf_rn_phys_id59 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra118	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra118	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra118	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra118	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra118	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id60

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

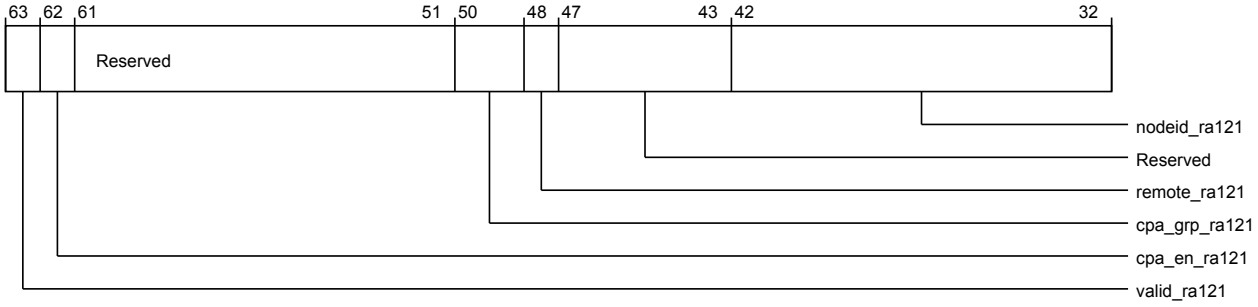


Figure 3-554 por_hnf_por_hnf_rn_phys_id60 (high)

The following table shows the por_hnf_rn_phys_id60 higher register bit assignments.

Table 3-568 por_hnf_por_hnf_rn_phys_id60 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra121	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra121	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra121	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra121	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra121	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

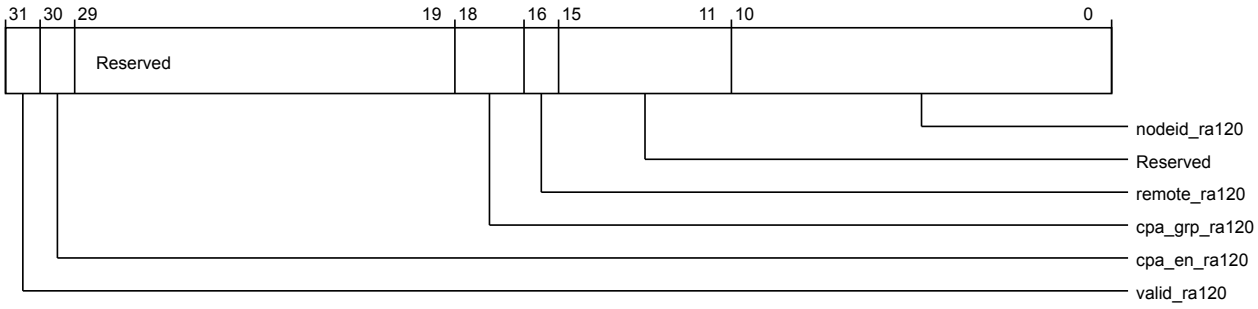


Figure 3-555 por_hnf_por_hnf_rn_phys_id60 (low)

The following table shows the por_hnf_rn_phys_id60 lower register bit assignments.

Table 3-569 por_hnf_por_hnf_rn_phys_id60 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra120	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra120	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra120	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra120	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra120	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id61

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

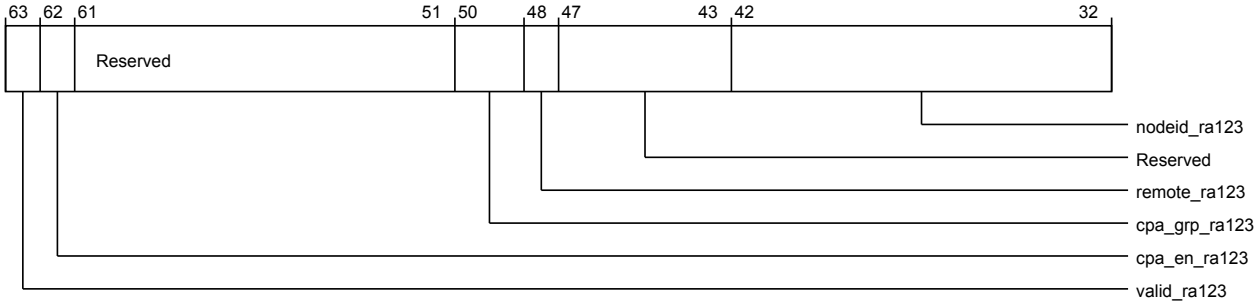


Figure 3-556 por_hnf_por_hnf_rn_phys_id61 (high)

The following table shows the por_hnf_rn_phys_id61 higher register bit assignments.

Table 3-570 por_hnf_por_hnf_rn_phys_id61 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra123	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra123	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra123	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra123	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra123	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

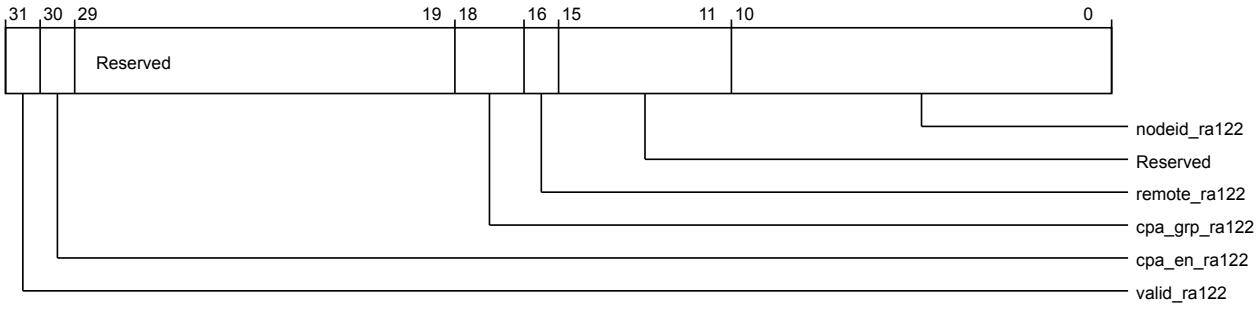


Figure 3-557 por_hnf_por_hnf_rn_phys_id61 (low)

The following table shows the por_hnf_rn_phys_id61 lower register bit assignments.

Table 3-571 por_hnf_por_hnf_rn_phys_id61 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra122	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra122	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra122	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra122	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra122	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id62

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

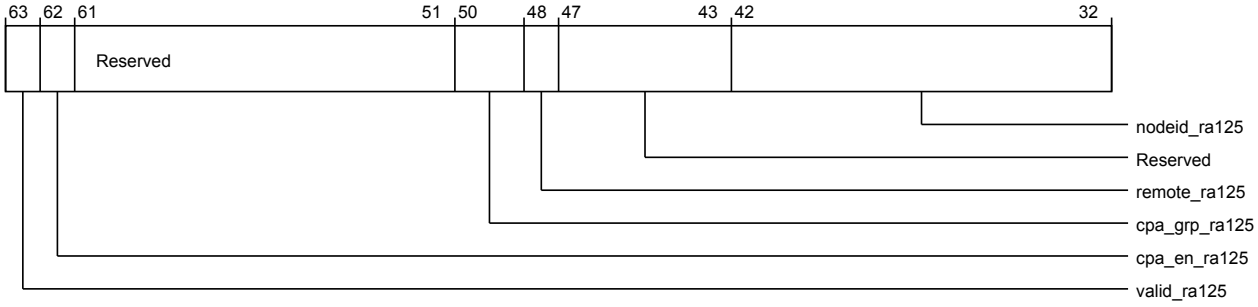


Figure 3-558 por_hnf_por_hnf_rn_phys_id62 (high)

The following table shows the por_hnf_rn_phys_id62 higher register bit assignments.

Table 3-572 por_hnf_por_hnf_rn_phys_id62 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra125	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra125	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra125	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra125	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra125	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

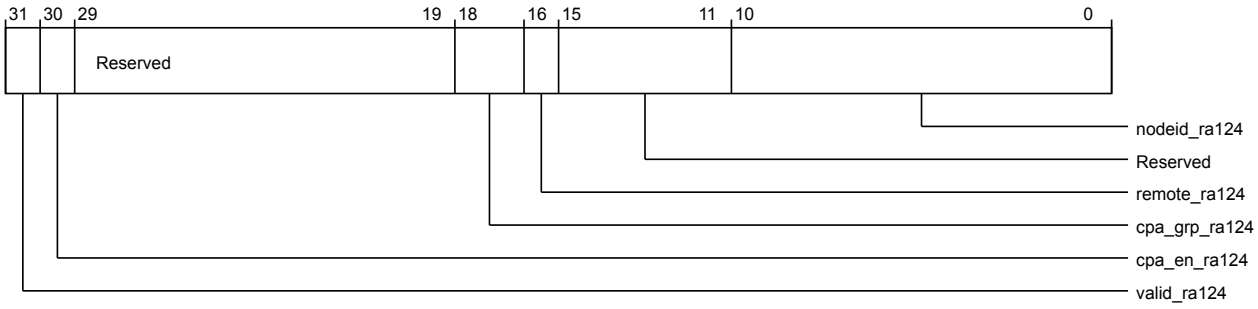


Figure 3-559 por_hnf_por_hnf_rn_phys_id62 (low)

The following table shows the por_hnf_rn_phys_id62 lower register bit assignments.

Table 3-573 por_hnf_por_hnf_rn_phys_id62 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra124	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra124	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra124	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra124	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra124	Specifies the node ID	RW	11'h0

por_hnf_rn_phys_id63

Configures node IDs for RNs in the system corresponding to each RN ID.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

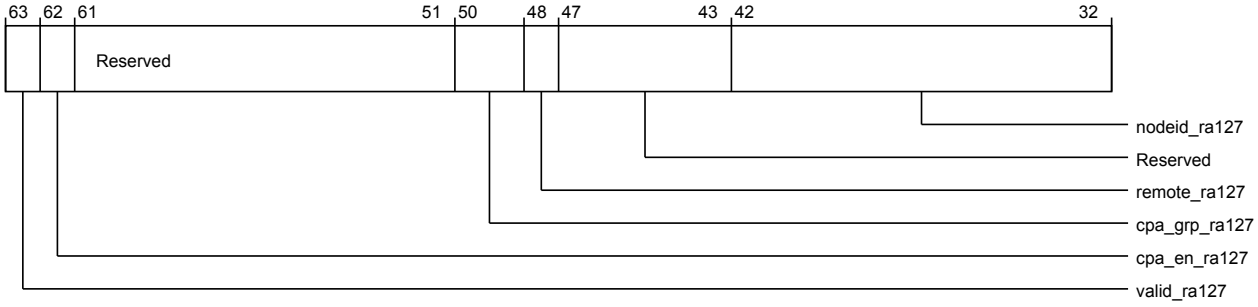


Figure 3-560 por_hnf_por_hnf_rn_phys_id63 (high)

The following table shows the por_hnf_rn_phys_id63 higher register bit assignments.

Table 3-574 por_hnf_por_hnf_rn_phys_id63 (high)

Bits	Field name	Description	Type	Reset
63	valid_ra127	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
62	cpa_en_ra127	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
61:51	Reserved	Reserved	RO	-
50:49	cpa_grp_ra127	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
48	remote_ra127	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
47:43	Reserved	Reserved	RO	-
42:32	nodeid_ra127	Specifies the node ID	RW	11'h0

The following image shows the lower register bit assignments.

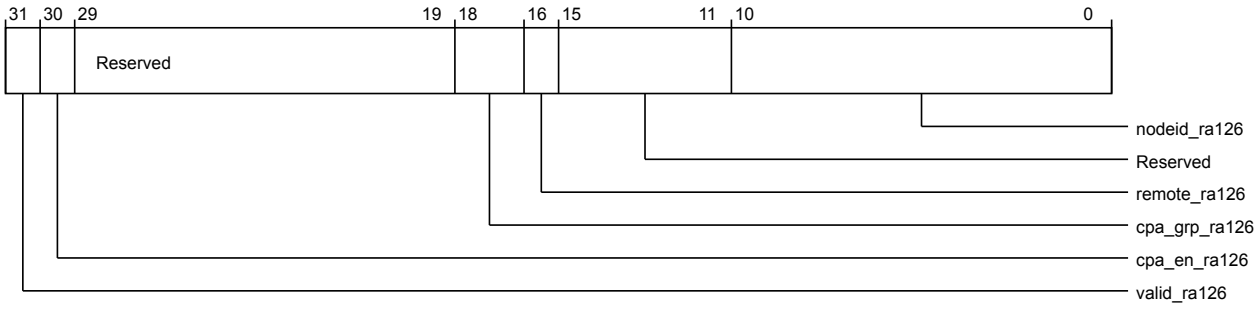


Figure 3-561 por_hnf_por_hnf_rn_phys_id63 (low)

The following table shows the por_hnf_rn_phys_id63 lower register bit assignments.

Table 3-575 por_hnf_por_hnf_rn_phys_id63 (low)

Bits	Field name	Description	Type	Reset
31	valid_ra126	Specifies whether the RN is valid 1'b0: RN ID is not valid 1'b1: RN ID is pointing to a valid CHI device	RW	1'h0
30	cpa_en_ra126	Specifies whether the CCIX port aggregation is enabled 1'b0: CPA not enabled 1'b1: CPA enabled	RW	1'h0
29:19	Reserved	Reserved	RO	-
18:17	cpa_grp_ra126	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'h0
16	remote_ra126	Specifies whether the RN is remote or local 1'b0: Local RN 1'b1: Remote RN	RW	1'h0
15:11	Reserved	Reserved	RO	-
10:0	nodeid_ra126	Specifies the node ID	RW	11'h0

por_hnf_ldid_map_table_reg0

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

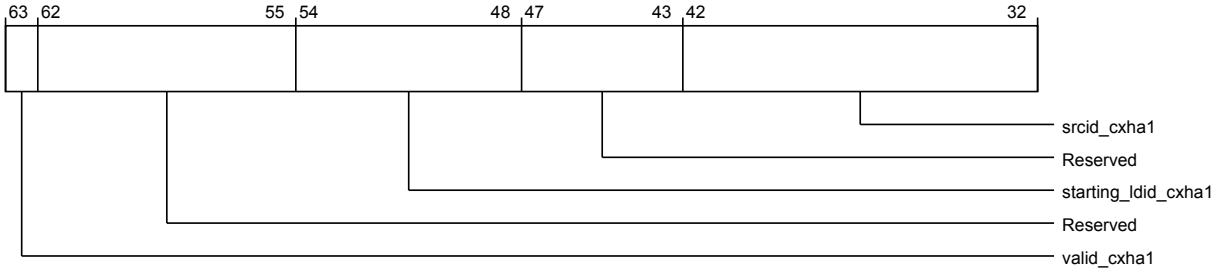


Figure 3-562 por_hnf_por_hnf_ldid_map_table_reg0 (high)

The following table shows the por_hnf_ldid_map_table_reg0 higher register bit assignments.

Table 3-576 por_hnf_por_hnf_ldid_map_table_reg0 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha1	Specifies CXHA 1 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha1	Specifies the starting LDID for RN-F's behind CXHA 1	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha1	Specifies the node ID for CXHA 1	RW	11'h0

The following image shows the lower register bit assignments.

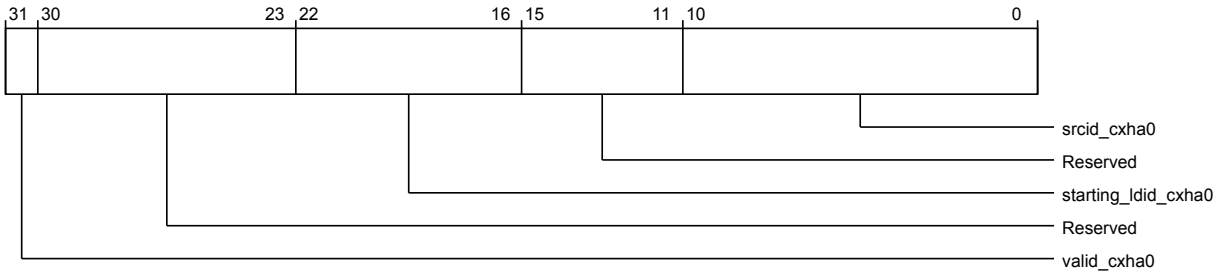


Figure 3-563 por_hnf_por_hnf_ldid_map_table_reg0 (low)

The following table shows the por_hnf_ldid_map_table_reg0 lower register bit assignments.

Table 3-577 por_hnf_por_hnf_ldid_map_table_reg0 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha0	Specifies CXHA 0 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha0	Specifies the starting LDID for RN-F's behind CXHA 0	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha0	Specifies the node ID for CXHA 0	RW	11'h0

por_hnf_ldid_map_table_reg1

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hFA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

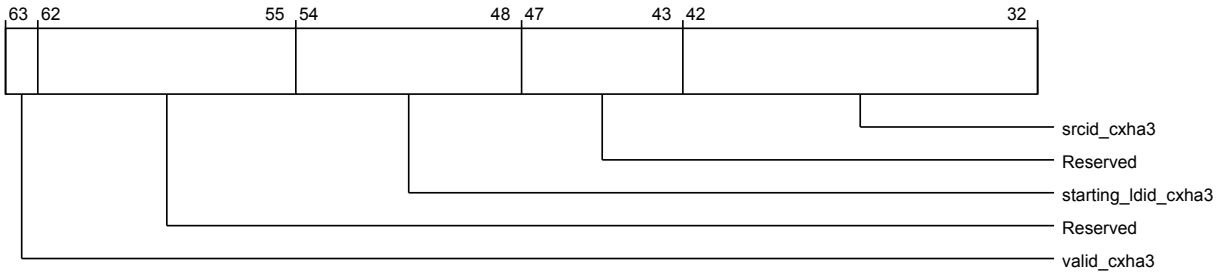


Figure 3-564 por_hnf_por_hnf_ldid_map_table_reg1 (high)

The following table shows the por_hnf_ldid_map_table_reg1 higher register bit assignments.

Table 3-578 por_hnf_por_hnf_ldid_map_table_reg1 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha3	Specifies CXHA 3 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha3	Specifies the starting LDID for RN-F's behind CXHA 3	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha3	Specifies the node ID for CXHA 3	RW	11'h0

The following image shows the lower register bit assignments.

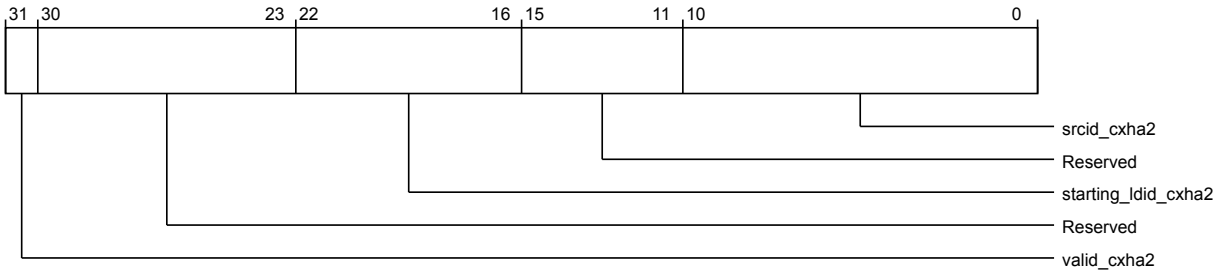


Figure 3-565 por_hnf_por_hnf_ldid_map_table_reg1 (low)

The following table shows the por_hnf_ldid_map_table_reg1 lower register bit assignments.

Table 3-579 por_hnf_por_hnf_ldid_map_table_reg1 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha2	Specifies CXHA 2 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha2	Specifies the starting LDID for RN-F's behind CXHA 2	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha2	Specifies the node ID for CXHA 2	RW	11'h0

por_hnf_ldid_map_table_reg2

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hFA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

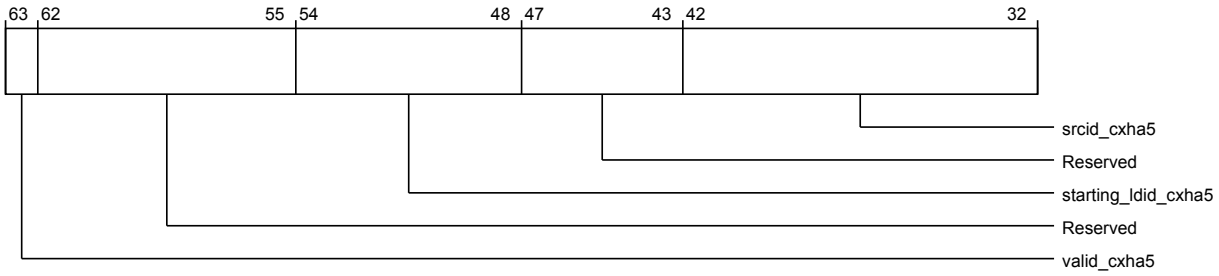


Figure 3-566 por_hnf_por_hnf_ldid_map_table_reg2 (high)

The following table shows the por_hnf_ldid_map_table_reg2 higher register bit assignments.

Table 3-580 por_hnf_por_hnf_ldid_map_table_reg2 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha5	Specifies CXHA 5 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha5	Specifies the starting LDID for RN-F's behind CXHA 5	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha5	Specifies the node ID for CXHA 5	RW	11'h0

The following image shows the lower register bit assignments.

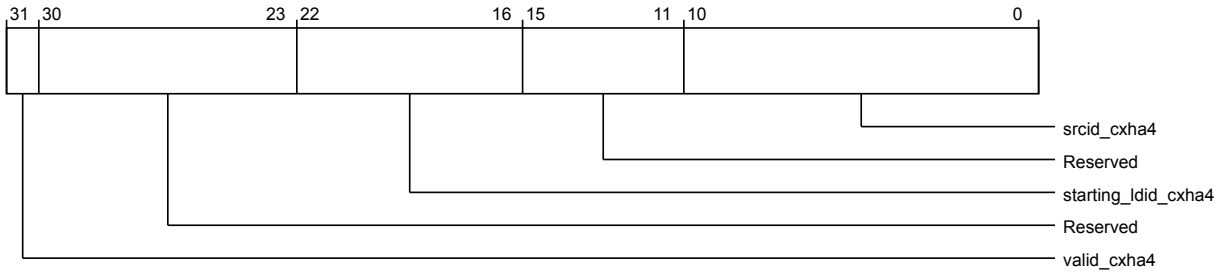


Figure 3-567 por_hnf_por_hnf_ldid_map_table_reg2 (low)

The following table shows the por_hnf_ldid_map_table_reg2 lower register bit assignments.

Table 3-581 por_hnf_por_hnf_ldid_map_table_reg2 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha4	Specifies CXHA 4 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha4	Specifies the starting LDID for RN-F's behind CXHA 4	RW	7'h0
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha4	Specifies the node ID for CXHA 4	RW	11'h0

por_hnf_ldid_map_table_reg3

Configures LDID start pointer for remote RN-F's behind each CXG

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hFB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.sam_control

The following image shows the higher register bit assignments.

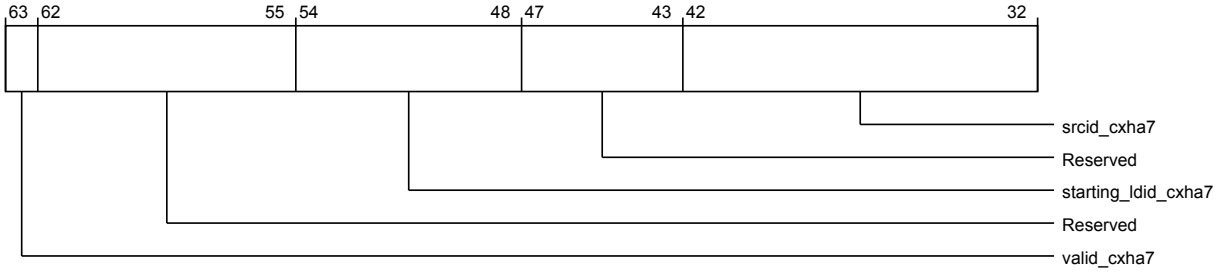


Figure 3-568 por_hnf_por_hnf_ldid_map_table_reg3 (high)

The following table shows the por_hnf_ldid_map_table_reg3 higher register bit assignments.

Table 3-582 por_hnf_por_hnf_ldid_map_table_reg3 (high)

Bits	Field name	Description	Type	Reset
63	valid_cxha7	Specifies CXHA 7 programming is valid	RW	1'h0
62:55	Reserved	Reserved	RO	-
54:48	starting_ldid_cxha7	Specifies the starting LDID for RN-F's behind CXHA 7	RW	7'h0
47:43	Reserved	Reserved	RO	-
42:32	srcid_cxha7	Specifies the node ID for CXHA 7	RW	11'h0

The following image shows the lower register bit assignments.

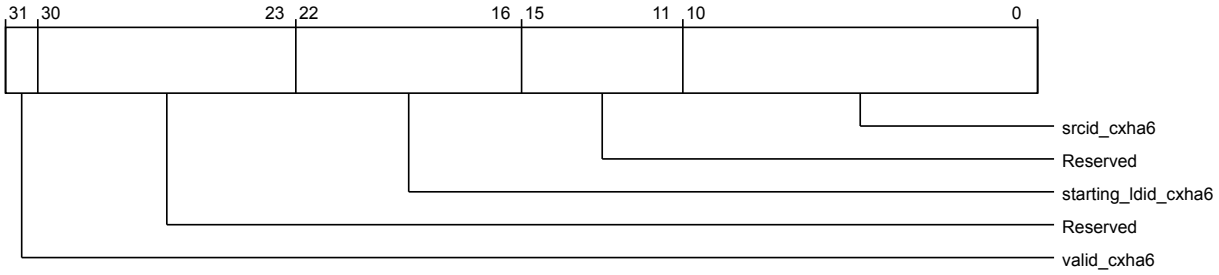


Figure 3-569 por_hnf_por_hnf_ldid_map_table_reg3 (low)

The following table shows the por_hnf_ldid_map_table_reg3 lower register bit assignments.

Table 3-583 por_hnf_por_hnf_ldid_map_table_reg3 (low)

Bits	Field name	Description	Type	Reset
31	valid_cxha6	Specifies CXHA 6 programming is valid	RW	1'h0
30:23	Reserved	Reserved	RO	-
22:16	starting_ldid_cxha6	Specifies the starting LDID for RN-F's behind CXHA 6	RW	7'h0

Table 3-583 por_hnf_por_hnf_ldid_map_table_reg3 (low) (continued)

Bits	Field name	Description	Type	Reset
15:11	Reserved	Reserved	RO	-
10:0	srcid_cxha6	Specifies the node ID for CXHA 6	RW	11'h0

por_hnf_cfg_slcsf_dbgrd

Controls access modes for SLC tasg, SLC data, and SF tag debug read.

Its characteristics are:

Type WO

Register width (Bits) 64

Address offset 14'hB80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

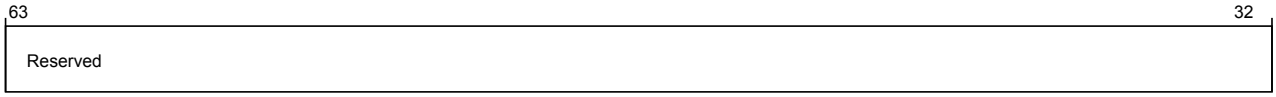


Figure 3-570 por_hnf_por_hnf_cfg_slcsf_dbgrd (high)

The following table shows the por_hnf_cfg_slcsf_dbgrd higher register bit assignments.

Table 3-584 por_hnf_por_hnf_cfg_slcsf_dbgrd (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

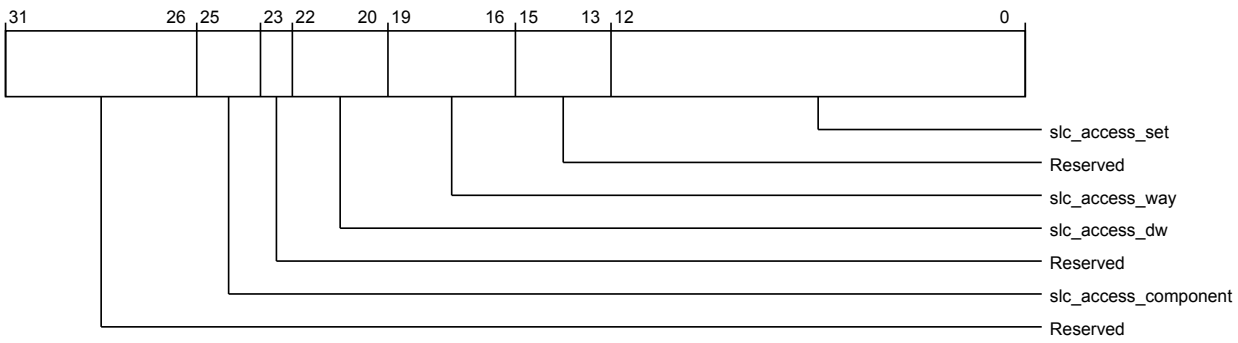


Figure 3-571 por_hnf_por_hnf_cfg_slcsf_dbgrd (low)

The following table shows the por_hnf_cfg_slcsf_dbgrd lower register bit assignments.

Table 3-585 por_hnf_por_hnf_cfg_slcsf_dbgrd (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	slc_access_component	Specifies SLC/SF array debug read 2'b01: SLC data read 2'b10: SLC tag read 2'b11: SF tag read	WO	2'b00
23	Reserved	Reserved	RO	-
22:20	slc_access_dw	64-bit chunk address for SLC data debug read access	WO	3'h0
19:16	slc_access_way	Way address for SLC/SF debug read access	WO	4'h0
15:13	Reserved	Reserved	RO	-
12:0	slc_access_set	Set address for SLC/SF debug read access	WO	13'h0

por_hnf_slc_cache_access_slc_tag

Contains SLC tag debug read data.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hB88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

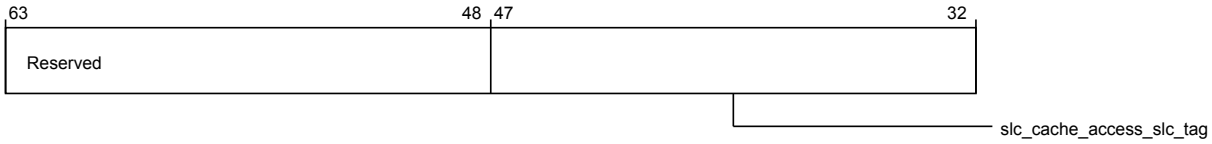


Figure 3-572 por_hnf_por_hnf_slc_cache_access_slc_tag (high)

The following table shows the por_hnf_slc_cache_access_slc_tag higher register bit assignments.

Table 3-586 por_hnf_por_hnf_slc_cache_access_slc_tag (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	slc_cache_access_slc_tag	SLC tag debug read data	RO	48'h0

The following image shows the lower register bit assignments.

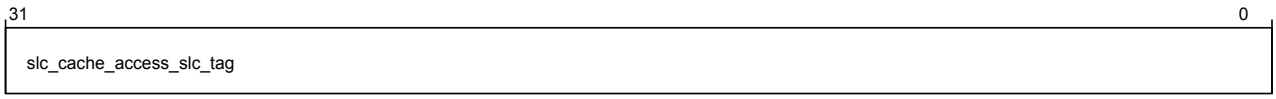


Figure 3-573 por_hnf_por_hnf_slc_cache_access_slc_tag (low)

The following table shows the por_hnf_slc_cache_access_slc_tag lower register bit assignments.

Table 3-587 por_hnf_por_hnf_slc_cache_access_slc_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_tag	SLC tag debug read data	RO	48'h0

por_hnf_slc_cache_access_slc_data

Contains SLC data RAM debug read data.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hB90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

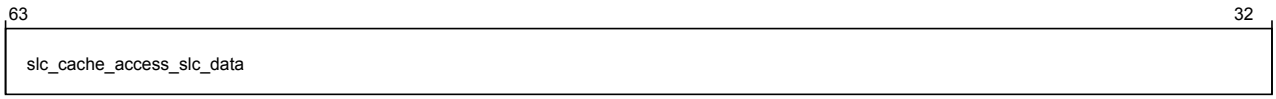


Figure 3-574 por_hnf_por_hnf_slc_cache_access_slc_data (high)

The following table shows the por_hnf_slc_cache_access_slc_data higher register bit assignments.

Table 3-588 por_hnf_por_hnf_slc_cache_access_slc_data (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

The following image shows the lower register bit assignments.

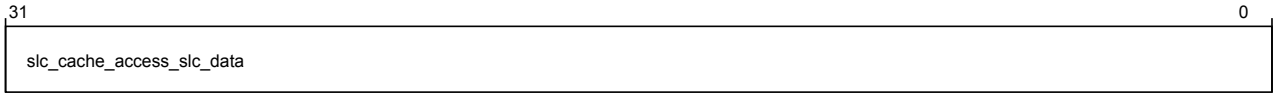


Figure 3-575 por_hnf_por_hnf_slc_cache_access_slc_data (low)

The following table shows the por_hnf_slc_cache_access_slc_data lower register bit assignments.

Table 3-589 por_hnf_por_hnf_slc_cache_access_slc_data (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_slc_data	SLC data RAM debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag

Contains SF tag debug read data. Bits[63:0]

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hB98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

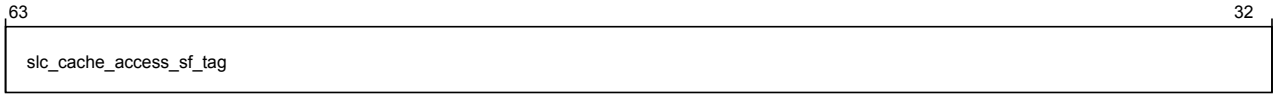


Figure 3-576 por_hnf_por_hnf_slc_cache_access_sf_tag (high)

The following table shows the por_hnf_slc_cache_access_sf_tag higher register bit assignments.

Table 3-590 por_hnf_por_hnf_slc_cache_access_sf_tag (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

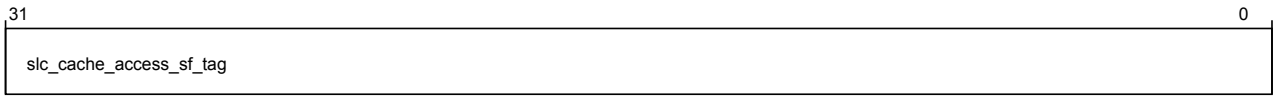


Figure 3-577 por_hnf_por_hnf_slc_cache_access_sf_tag (low)

The following table shows the por_hnf_slc_cache_access_sf_tag lower register bit assignments.

Table 3-591 por_hnf_por_hnf_slc_cache_access_sf_tag (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag	SF tag debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag1

Contains SF tag debug read data bits [127:64], when present in SF Tag

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hBA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

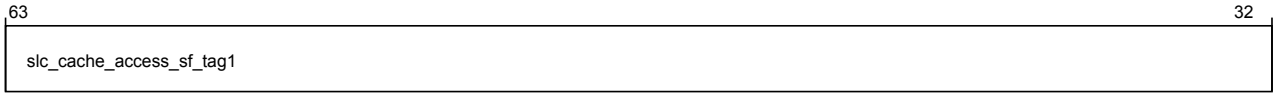


Figure 3-578 por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)

The following table shows the por_hnf_slc_cache_access_sf_tag1 higher register bit assignments.

Table 3-592 por_hnf_por_hnf_slc_cache_access_sf_tag1 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

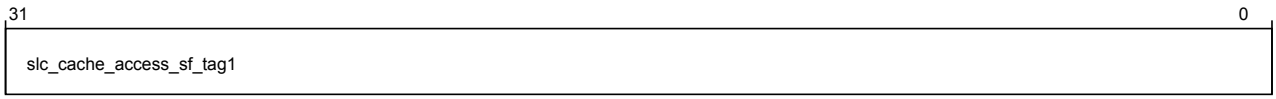


Figure 3-579 por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)

The following table shows the por_hnf_slc_cache_access_sf_tag1 lower register bit assignments.

Table 3-593 por_hnf_por_hnf_slc_cache_access_sf_tag1 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag1	SF tag debug read data	RO	64'h0

por_hnf_slc_cache_access_sf_tag2

Contains SF tag debug read data bits [128:191], when present in SF Tag

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'hBA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_hnf_secure_register_groups_override.slcsf_dbgrd

The following image shows the higher register bit assignments.

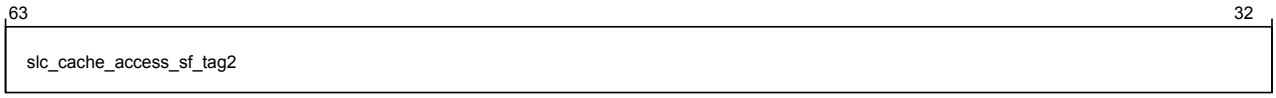


Figure 3-580 por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)

The following table shows the por_hnf_slc_cache_access_sf_tag2 higher register bit assignments.

Table 3-594 por_hnf_por_hnf_slc_cache_access_sf_tag2 (high)

Bits	Field name	Description	Type	Reset
63:32	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

The following image shows the lower register bit assignments.

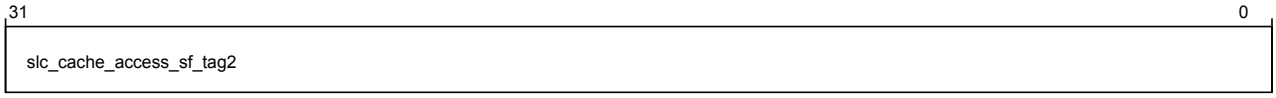


Figure 3-581 por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)

The following table shows the por_hnf_slc_cache_access_sf_tag2 lower register bit assignments.

Table 3-595 por_hnf_por_hnf_slc_cache_access_sf_tag2 (low)

Bits	Field name	Description	Type	Reset
31:0	slc_cache_access_sf_tag2	SF tag debug read data	RO	64'h0

por_hnf_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

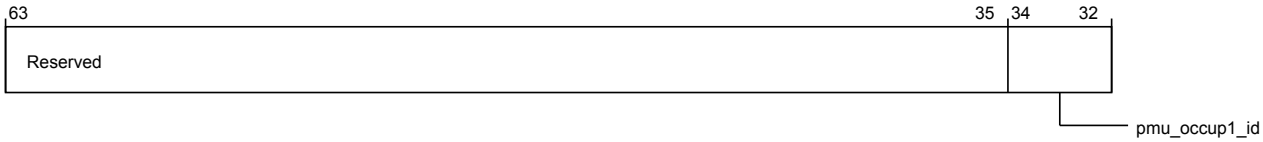


Figure 3-582 por_hnf_por_hnf_pmu_event_sel (high)

The following table shows the por_hnf_pmu_event_sel higher register bit assignments.

Table 3-596 por_hnf_por_hnf_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	pmu_occup1_id	HN-F PMU occupancy 1 select 3'b000: All occupancy selected 3'b001: Read requests 3'b010: Write requests 3'b011: Atomic operation requests 3'b100: Stash requests	RW	3'h0

The following image shows the lower register bit assignments.

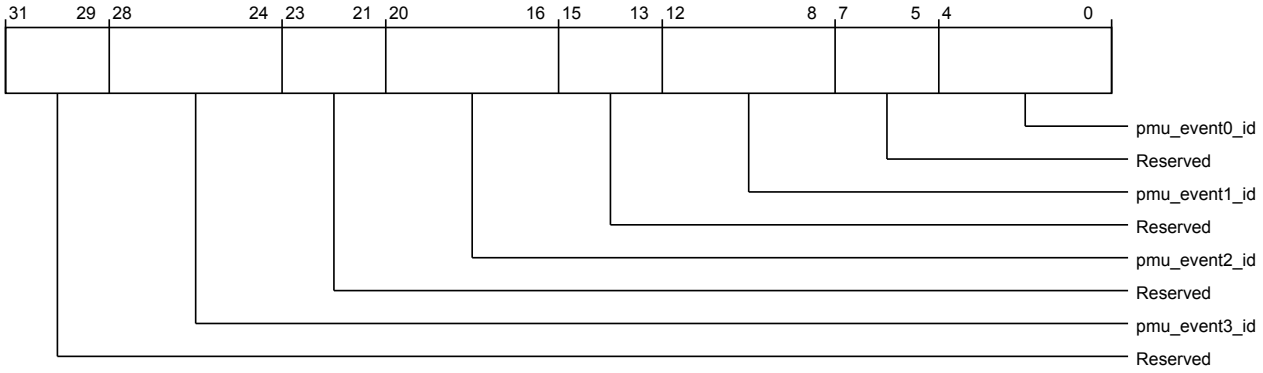


Figure 3-583 por_hnf_por_hnf_pmu_event_sel (low)

The following table shows the por_hnf_pmu_event_sel lower register bit assignments.

Table 3-597 por_hnf_por_hnf_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	HN-F PMU Event 3 select; see pmu_event0_id for encodings	RW	5'h00
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	HN-F PMU Event 2 select; see pmu_event0_id for encodings	RW	5'h00
15:13	Reserved	Reserved	RO	-

Table 3-597 por_hnf_por_hnf_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
12:8	pmu_event1_id	HN-F PMU Event 1 select; see pmu_event0_id for encodings	RW	5'h00

Table 3-597 por_hnf_por_hnf_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-

Table 3-597 por_hnf_por_hnf_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
4:0	pmu_event0_id	HN-F PMU Event 0 select 5'h00: No event 5'h01: PMU_HN_CACHE_MISS_EVENT; counts total cache misses in first lookup result (high priority) 5'h02: PMU_HN_SLCSF_CACHE_ACCESS_EVENT; counts number of cache accesses in first access (high priority) 5'h03: PMU_HN_CACHE_FILL_EVENT; counts total allocations in HN SLC (all cache line allocations to SLC) 5'h04: PMU_HN_POCQ_RETRY_EVENT; counts number of retried requests 5'h05: PMU_HN_POCQ_REQS_RECVD_EVENT; counts number of requests received by HN 5'h06: PMU_HN_SF_HIT_EVENT; counts number of SF hits 5'h07: PMU_HN_SF_EVICTIONS_EVENT; counts number of SF eviction cache invalidations initiated 5'h08: PMU_HN_DIR_SNOOPS_SENT_EVENT; counts number of directed snoops sent (not including SF back invalidation) 5'h09: PMU_HN_DIR_SNOOPS_SENTEVENT; counts number of multicast snoops send (not including SF back invalidation) 5'h0A: PMU_HN_SLC_EVICTION_EVENT; counts number of SLC evictions (dirty only) 5'h0B: PMU_HN_SLC_FILL_INVALID_WAY_EVENT; counts number of SLC fills to an invalid way 5'h0C: PMU_HN_MC_RETRIES_EVENT; counts number of retried transactions by the MC 5'h0D: PMU_HN_MC_REQS_EVENT; counts number of requests sent to MC 5'h0E: PMU_HN_QOS_HH_RETRY_EVENT; counts number of times a HighHigh priority request is protocol retried at the HN-F 5'h0F: PMU_HN_POCQ_OCCUPANCY_EVENT; counts the POCQ occupancy in HN-F; occupancy filtering is programmed in pmu_occup1_id 5'h10: PMU_HN_POCQ_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation 5'h11: PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT; counts number of POCQ address hazards upon allocation for atomic operations 5'h12: PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT; counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations 5'h13: PMU_HN_CMP_ADQ_FULL_EVENT; counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations 5'h14: PMU_HN_TXDAT_STALL_EVENT; counts number of times HN-F has a pending TXDAT flit but no credits to upload 5'h15: PMU_HN_TXRSP_STALL_EVENT; counts number of times HN-F has a pending TXRSP flit but no credits to upload 5'h16: PMU_HN_SEQ_FULL_EVENT; counts number of times requests are replayed in SLC pipe due to SEQ being full 5'h17: PMU_HN_SEQ_HIT_EVENT; counts number of times a request in SLC hit a pending SF eviction in SEQ 5'h18: PM ling directed/ 5'h19: PMU_HN_SFBI_DIR_SNP_SENT_EVENT; counts number of times directed snoops	RW	5'h00

3.3.5 HN-I register descriptions

This section lists the HN-I registers.

por_hni_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

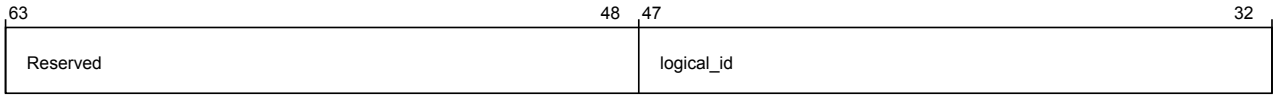


Figure 3-584 por_hni_por_hni_node_info (high)

The following table shows the por_hni_node_info higher register bit assignments.

Table 3-598 por_hni_por_hni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

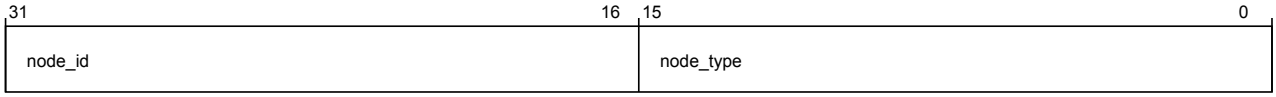


Figure 3-585 por_hni_por_hni_node_info (low)

The following table shows the por_hni_node_info lower register bit assignments.

Table 3-599 por_hni_por_hni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0004

por_hni_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

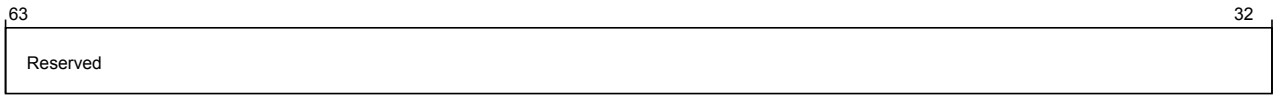


Figure 3-586 por_hni_por_hni_child_info (high)

The following table shows the por_hni_child_info higher register bit assignments.

Table 3-600 por_hni_por_hni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

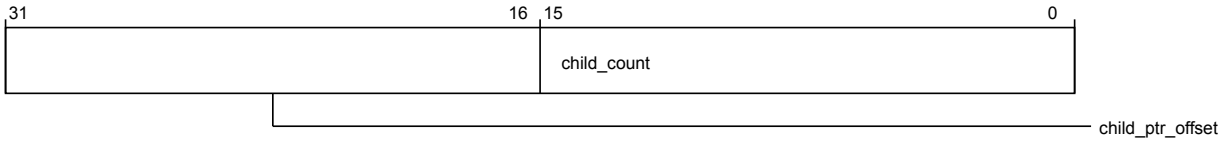


Figure 3-587 por_hni_por_hni_child_info (low)

The following table shows the por_hni_child_info lower register bit assignments.

Table 3-601 por_hni_por_hni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_hni_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

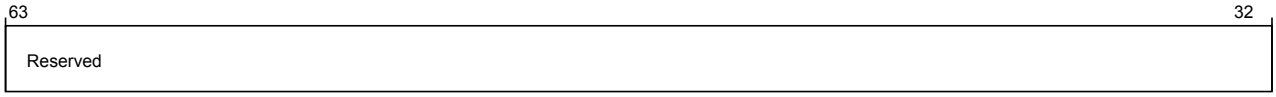


Figure 3-588 por_hni_por_hni_secure_register_groups_override (high)

The following table shows the por_hni_secure_register_groups_override higher register bit assignments.

Table 3-602 por_hni_por_hni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

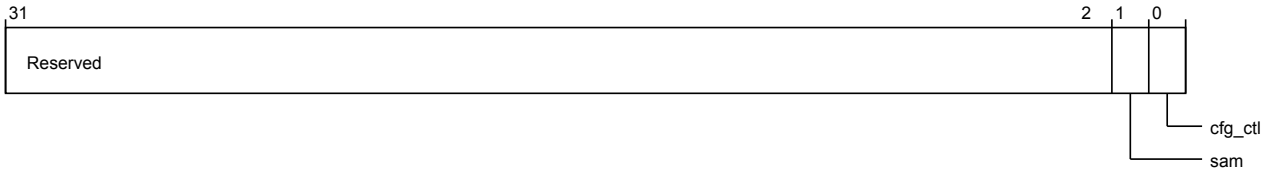


Figure 3-589 por_hni_por_hni_secure_register_groups_override (low)

The following table shows the por_hni_secure_register_groups_override lower register bit assignments.

Table 3-603 por_hni_por_hni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	sam	Allows non-secure access to secure SAM registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_hni_unit_info

Provides component identification information for HN-I.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

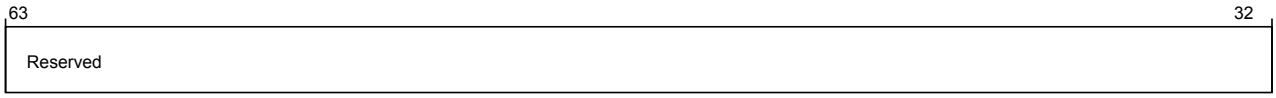


Figure 3-590 por_hni_por_hni_unit_info (high)

The following table shows the por_hni_unit_info higher register bit assignments.

Table 3-604 por_hni_por_hni_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

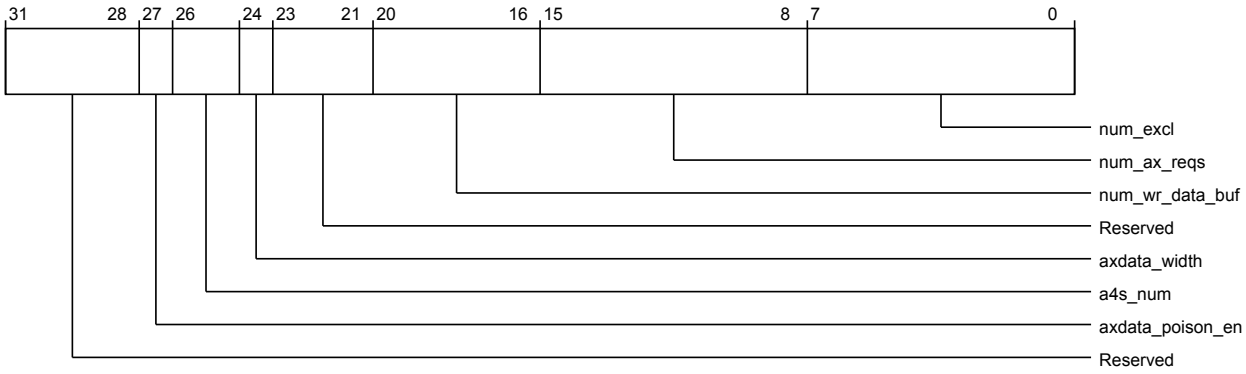


Figure 3-591 por_hni_por_hni_unit_info (low)

The following table shows the por_hni_unit_info lower register bit assignments.

Table 3-605 por_hni_por_hni_unit_info (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent
26:25	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
24	axdata_width	Data width on ACE-Lite/AXI4 interface 1'b0: 128 bits 1'b1: 256 bits	RO	Configuration dependent
23:21	Reserved	Reserved	RO	-

Table 3-605 por_hni_por_hni_unit_info (low) (continued)

Bits	Field name	Description	Type	Reset
20:16	num_wr_data_buf	Number of write data buffers in HN-I	RO	Configuration dependent
15:8	num_ax_reqs	Maximum number of outstanding ACE-Lite/AXI4 requests	RO	Configuration dependent
7:0	num_excl	Number of exclusive monitors in HN-I	RO	Configuration dependent

por_hni_sam_addrregion0_cfg

Configures Address Region 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset 64'b11000111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

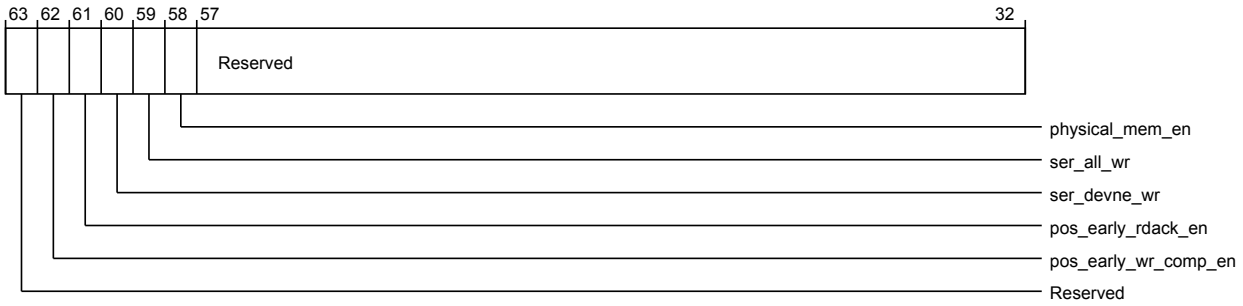


Figure 3-592 por_hni_por_hni_sam_addrregion0_cfg (high)

The following table shows the por_hni_sam_addrregion0_cfg higher register bit assignments.

Table 3-606 por_hni_por_hni_sam_addrregion0_cfg (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 0; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 0; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 0	RW	1'b0

Table 3-606 por_hni_por_hni_sam_addrregion0_cfg (high) (continued)

Bits	Field name	Description	Type	Reset
59	ser_all_wr	Used to serialize all writes within Address Region 0	RW	1'b0
58	physical_mem_en	Address Region 0 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

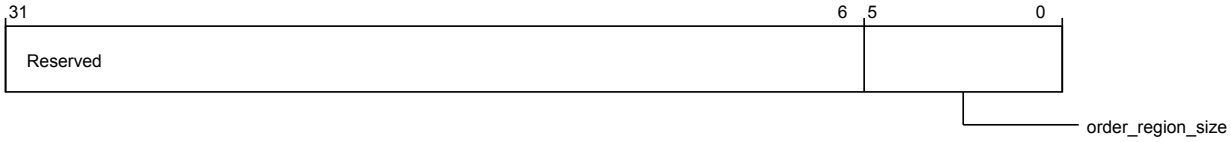


Figure 3-593 por_hni_por_hni_sam_addrregion0_cfg (low)

The following table shows the por_hni_sam_addrregion0_cfg lower register bit assignments.

Table 3-607 por_hni_por_hni_sam_addrregion0_cfg (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 0 size within Address Region 0 (2^n*4KB)	RW	6'b111111

por_hni_sam_addrregion1_cfg

Configures Address Region 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

Register reset 64'b0110000000000000000000000000000000000000000000000000000000000000

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

Figure 3-594 por_hni_por_hni_sam_addrregion1_cfg (high)

The following table shows the por_hni_sam_addrregion1_cfg higher register bit assignments.

Table 3-608 por_hni_por_hni_sam_addrregion1_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Address Region 1 fields are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 1; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 1; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 1	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 1	RW	1'b0
58	physical_mem_en	Address Region 1 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	36'h0

The following image shows the lower register bit assignments.

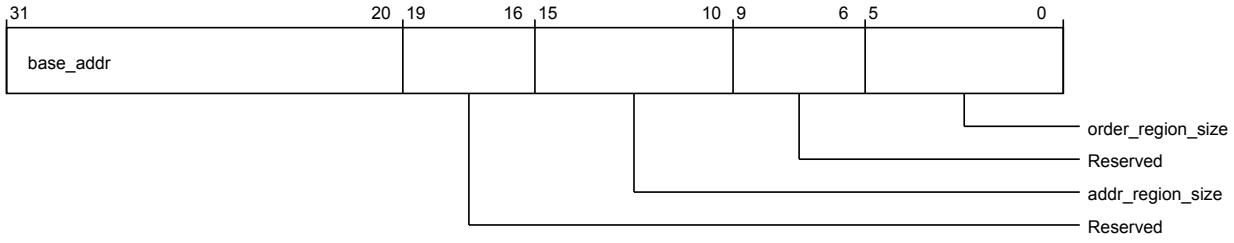


Figure 3-595 por_hni_por_hni_sam_addrregion1_cfg (low)

The following table shows the por_hni_sam_addrregion1_cfg lower register bit assignments.

Table 3-609 por_hni_por_hni_sam_addrregion1_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 1 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 1 size.	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 1 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 1 size is less than or equal to 2^(address width).	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 1 size within Address Region 1 (2^n*4KB)	RW	6'h0

por_hni_sam_addrregion2_cfg

Configures Address Region 2.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC10

Register reset 64'b0110000000000000000000000000000000000000000000000000000000000000

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

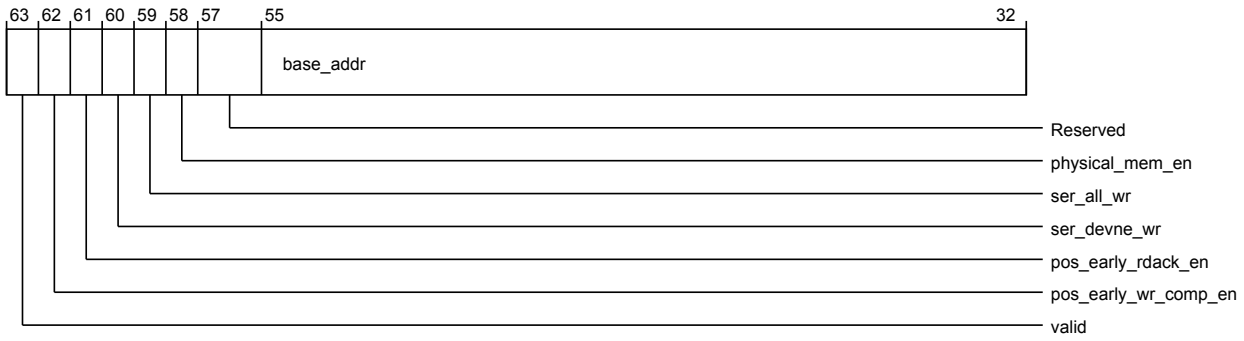


Figure 3-596 por_hni_por_hni_sam_addrregion2_cfg (high)

The following table shows the por_hni_sam_addrregion2_cfg higher register bit assignments.

Table 3-610 por_hni_por_hni_sam_addrregion2_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Address Region 2 fields are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 2; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 2; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 2	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 2	RW	1'b0
58	physical_mem_en	Address Region 2 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	36'h0

The following image shows the lower register bit assignments.

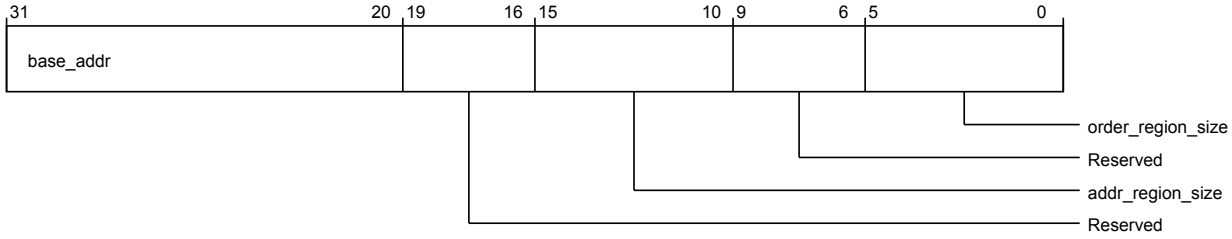


Figure 3-597 por_hni_por_hni_sam_addrregion2_cfg (low)

The following table shows the por_hni_sam_addrregion2_cfg lower register bit assignments.

Table 3-611 por_hni_por_hni_sam_addrregion2_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 2 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 2 size	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 2 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 2 size is less than or equal to 2^(address width).	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 2 size within Address Region 2 (2^n*4KB)	RW	6'h0

por_hni_sam_addrregion3_cfg

Configures Address Region 3.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hC18
Register reset	64'b0110000000000000000000000000000000000000000000000000000000000000
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_hni_secure_register_groups_override.sam

The following image shows the higher register bit assignments.

Figure 3-598 por_hni_por_hni_sam_addrregion3_cfg (high)

The following table shows the por_hni_sam_addrregion3_cfg higher register bit assignments.

Table 3-612 por_hni_por_hni_sam_addrregion3_cfg (high)

Bits	Field name	Description	Type	Reset
63	valid	Fields of Address Region 3 are programmed and valid	RW	1'h0
62	pos_early_wr_comp_en	Enables early write acknowledgment in Address Region 3; used to improve write performance	RW	1'b1
61	pos_early_rdack_en	Enables sending early read receipts from HN-I in Address Region 3; used to improve ordered read performance	RW	1'b1
60	ser_devne_wr	Used to serialize Device-nGnRnE writes within Address Region 3	RW	1'b0
59	ser_all_wr	Used to serialize all writes within Address Region 3	RW	1'b0
58	physical_mem_en	Address Region 3 follows Arm Architecture Reference Manual physical memory ordering guarantees	RW	1'b0
57:56	Reserved	Reserved	RO	-
55:32	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	36'h0

The following image shows the lower register bit assignments.

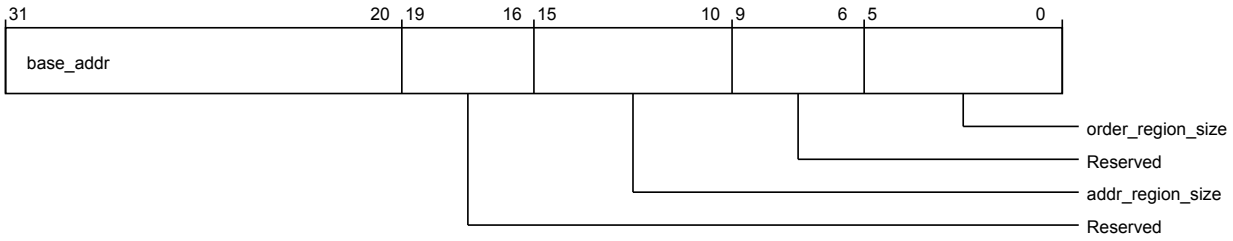


Figure 3-599 por_hni_por_hni_sam_addrregion3_cfg (low)

The following table shows the por_hni_sam_addrregion3_cfg lower register bit assignments.

Table 3-613 por_hni_por_hni_sam_addrregion3_cfg (low)

Bits	Field name	Description	Type	Reset
31:20	base_addr	Address Region 3 base address; [address width-1:12] CONSTRAINT: Must be an integer multiple of the Address Region 3 size	RW	36'h0
19:16	Reserved	Reserved	RO	-
15:10	addr_region_size	<n>; used to calculate Address Region 3 size (2^n*4KB) CONSTRAINT: <n> must be configured so that the Address Region 3 size is less than or equal to 2^(address width).	RW	6'h0
9:6	Reserved	Reserved	RO	-
5:0	order_region_size	<n>; used to calculate Order Region 3 size within Address Region 3 (2^n*4KB)	RW	6'h0

por_hni_cfg_ctl

Functions as the configuration control register for HN-I.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_hni_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

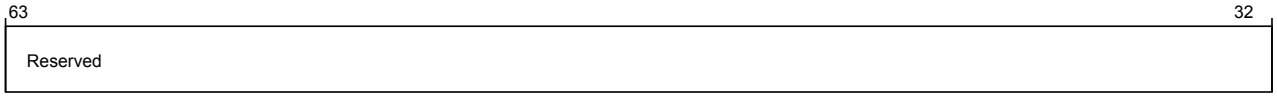


Figure 3-600 por_hni_por_hni_cfg_ctl (high)

The following table shows the por_hni_cfg_ctl higher register bit assignments.

Table 3-614 por_hni_por_hni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

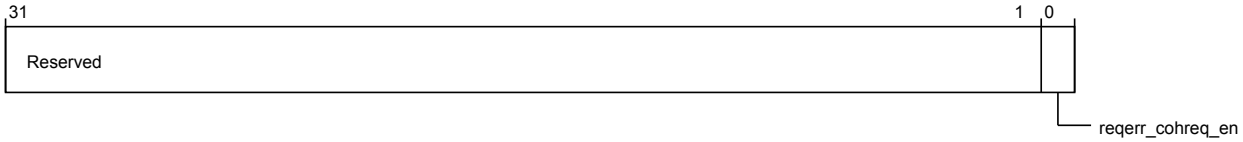


Figure 3-601 por_hni_por_hni_cfg_ctl (low)

The following table shows the por_hni_cfg_ctl lower register bit assignments.

Table 3-615 por_hni_por_hni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	reqerr_cohreq_en	Enables sending of NDE response error to RN and logging of error information for the following requests: 1. Coherent Read 2. CleanUnique/MakeUnique 3. Coherent/CopyBack Write	RW	1'b1

por_hni_aux_ctl

Functions as the auxiliary control register for HN-I.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

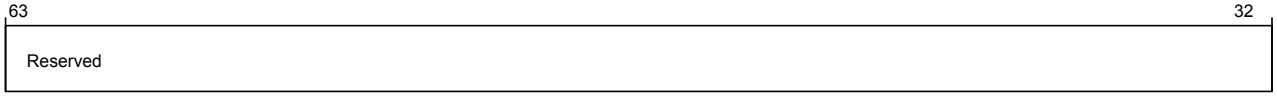


Figure 3-602 por_hni_por_hni_aux_ctl (high)

The following table shows the por_hni_aux_ctl higher register bit assignments.

Table 3-616 por_hni_por_hni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

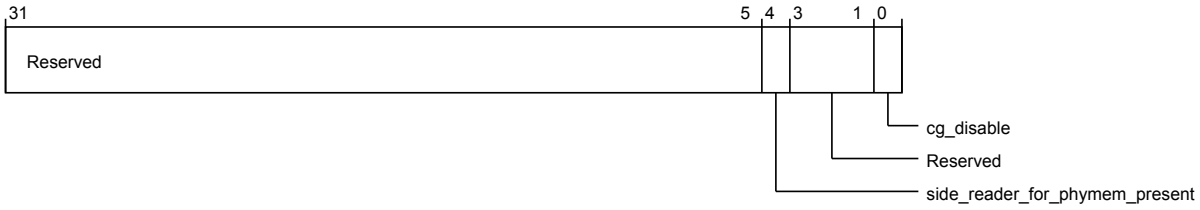


Figure 3-603 por_hni_por_hni_aux_ctl (low)

The following table shows the por_hni_aux_ctl lower register bit assignments.

Table 3-617 por_hni_por_hni_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4	side_reader_for_phymem_present	Enables side reader in physical memory range	RW	1'b0
3:1	Reserved	Reserved	RO	-
0	cg_disable	Disables HN-I architectural clock gates	RW	1'b0

por_hni_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b0000010100101
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

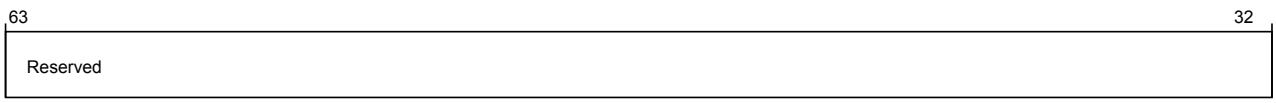


Figure 3-604 por_hni_por_hni_errfr (high)

The following table shows the por_hni_errfr higher register bit assignments.

Table 3-618 por_hni_por_hni_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

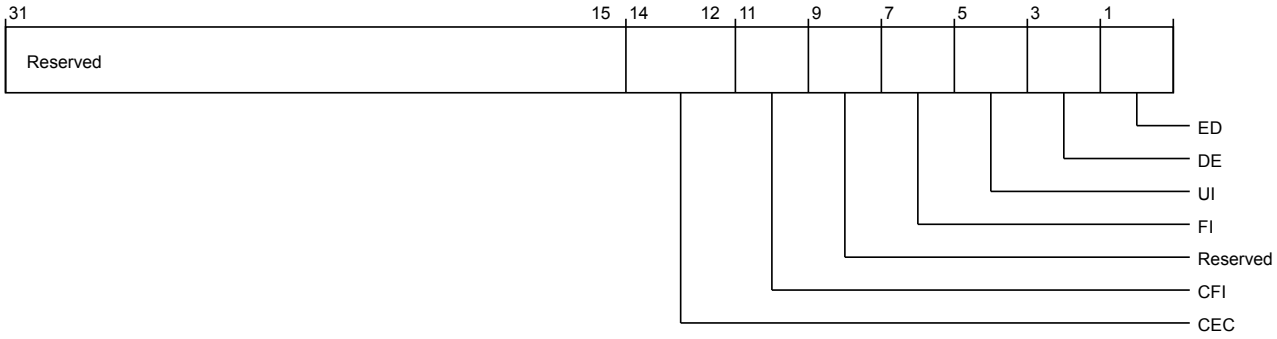


Figure 3-605 por_hni_por_hni_errfr (low)

The following table shows the por_hni_errfr lower register bit assignments.

Table 3-619 por_hni_por_hni_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hni_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

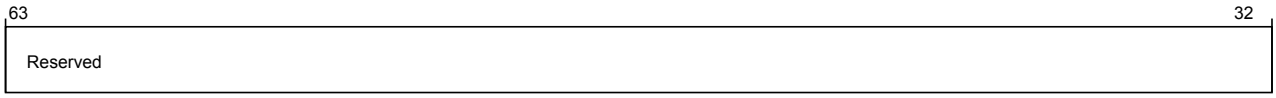


Figure 3-606 por_hni_por_hni_errctlr (high)

The following table shows the por_hni_errctlr higher register bit assignments.

Table 3-620 por_hni_por_hni_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

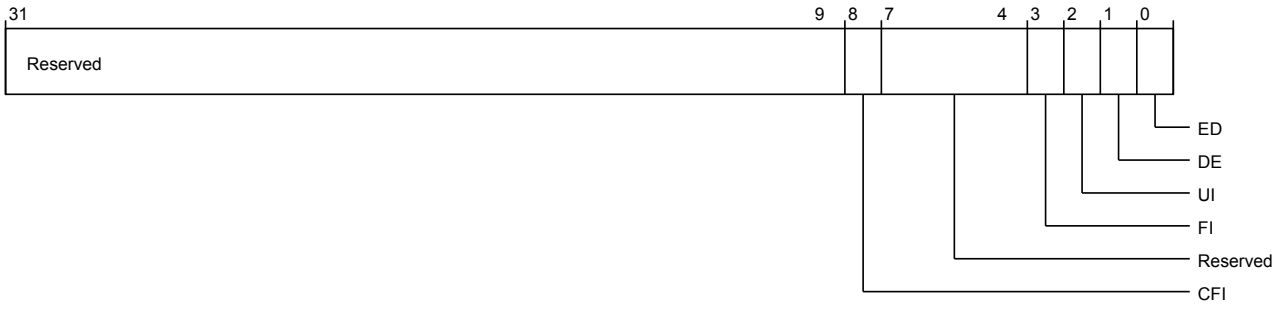


Figure 3-607 por_hni_por_hni_errctlr (low)

The following table shows the por_hni_errctlr lower register bit assignments.

Table 3-621 por_hni_por_hni_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr.ED	RW	1'b0

por_hni_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

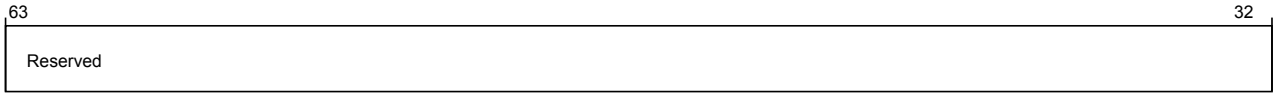


Figure 3-608 por_hni_por_hni_errstatus (high)

The following table shows the por_hni_errstatus higher register bit assignments.

Table 3-622 por_hni_por_hni_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-609 por_hni_por_hni_errstatus (low)

The following table shows the por_hni_errstatus lower register bit assignments.

Table 3-623 por_hni_por_hni_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hni_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hni_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_hni_erraddr

Contains the error record address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3018

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

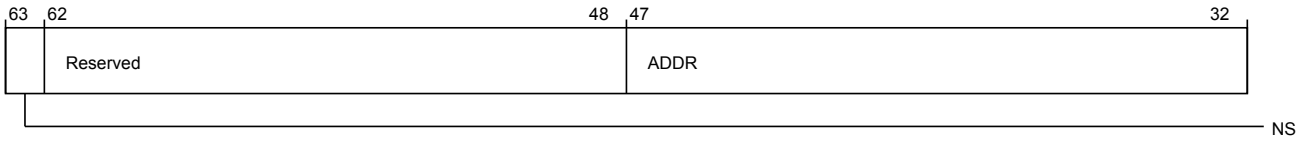


Figure 3-610 por_hni_por_hni_erraddr (high)

The following table shows the por_hni_erraddr higher register bit assignments.

Table 3-624 por_hni_por_hni_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

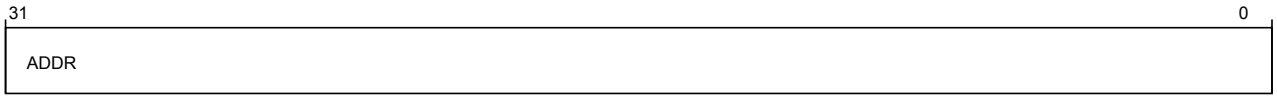


Figure 3-611 por_hni_por_hni_erraddr (low)

The following table shows the por_hni_erraddr lower register bit assignments.

Table 3-625 por_hni_por_hni_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hni_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/ uncorrected errors.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'h3020
Register reset	64'b0
Usage constraints	Only accessible by secure accesses.

The following image shows the higher register bit assignments.

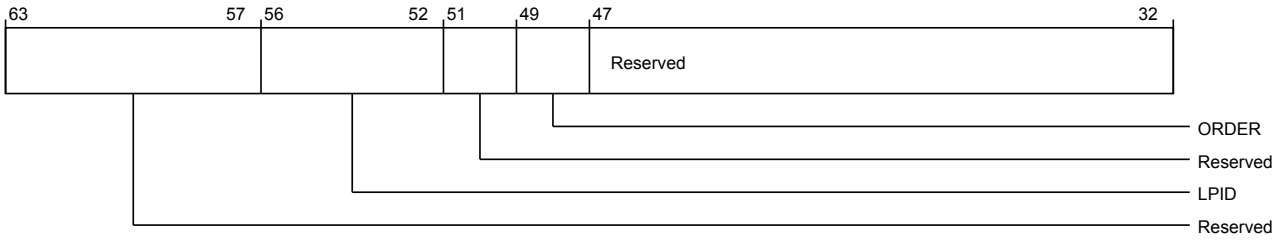


Figure 3-612 por_hni_por_hni_errmisc (high)

The following table shows the por_hni_errmisc higher register bit assignments.

Table 3-626 por_hni_por_hni_errmisc (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

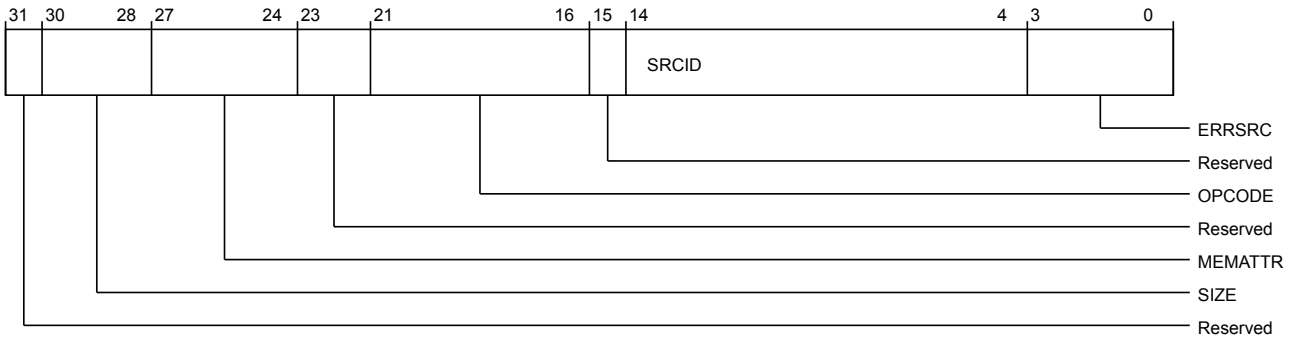


Figure 3-613 por_hni_por_hni_errmisc (low)

The following table shows the por_hni_errmisc lower register bit assignments.

Table 3-627 por_hni_por_hni_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0000: Coherent read 4'b0001: Coherent write 4'b0010: CleanUnique/MakeUnique 4'b0011: Atomic 4'b0100: Illegal configuration read 4'b0101: Illegal configuration write 4'b0110: Configuration write data partial byte enable error 4'b0111: Configuration write data parity error or poison error 4'b1000: BRESP error 4'b1001: Poison error 4'b1010: BRESP error and poison error NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc.SRCID is the only valid field. For other error types, all fields are valid.	RW	4'b0

por_hni_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b0000010100101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

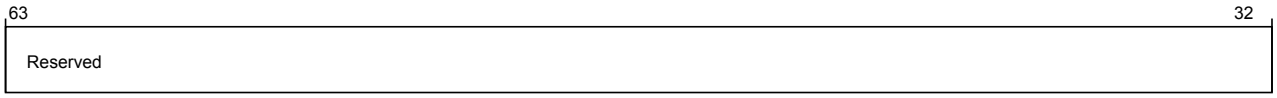


Figure 3-614 por_hni_por_hni_errfr_ns (high)

The following table shows the por_hni_errfr_NS higher register bit assignments.

Table 3-628 por_hni_por_hni_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

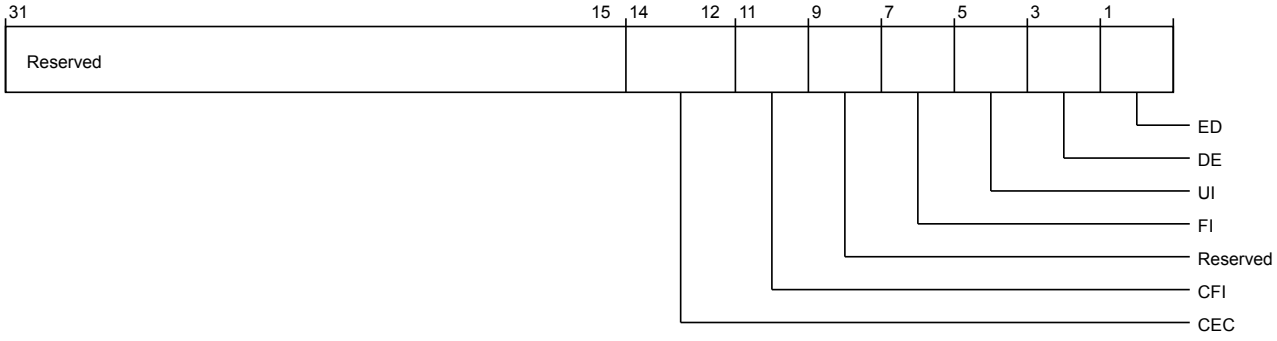


Figure 3-615 por_hni_por_hni_errfr_ns (low)

The following table shows the por_hni_errfr_NS lower register bit assignments.

Table 3-629 por_hni_por_hni_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_hni_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

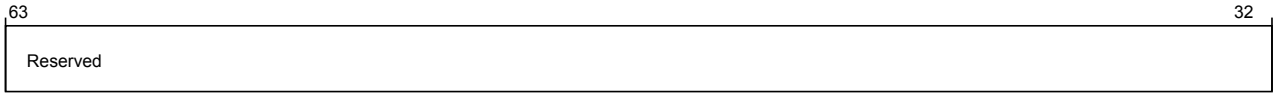


Figure 3-616 por_hni_por_hni_errctlr_ns (high)

The following table shows the por_hni_errctlr_NS higher register bit assignments.

Table 3-630 por_hni_por_hni_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

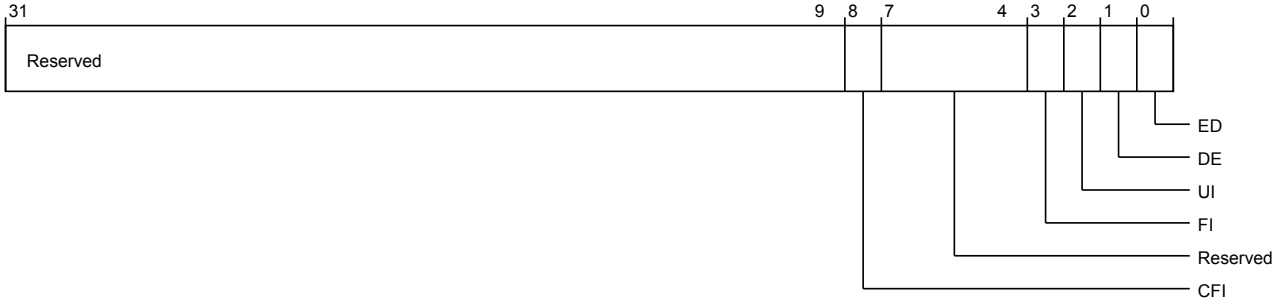


Figure 3-617 por_hni_por_hni_errctlr_ns (low)

The following table shows the por_hni_errctlr_NS lower register bit assignments.

Table 3-631 por_hni_por_hni_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_hni_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 3-631 por_hni_por_hni_errctlr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_hni_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_hni_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_hni_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_hni_errfr_NS.ED	RW	1'b0

por_hni_errstatus_NS

Functions as the non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

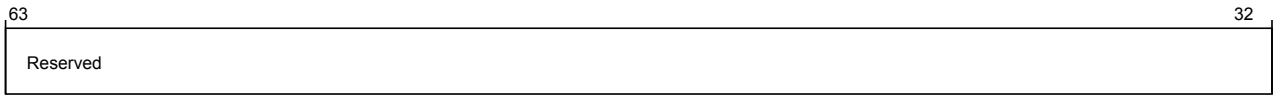


Figure 3-618 por_hni_por_hni_errstatus_ns (high)

The following table shows the por_hni_errstatus_NS higher register bit assignments.

Table 3-632 por_hni_por_hni_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-619 por_hni_por_hni_errstatus_ns (low)

The following table shows the por_hni_errstatus_NS lower register bit assignments.

Table 3-633 por_hni_por_hni_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_hni_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_hni_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 3-633 por_hni_por_hni_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_hni_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

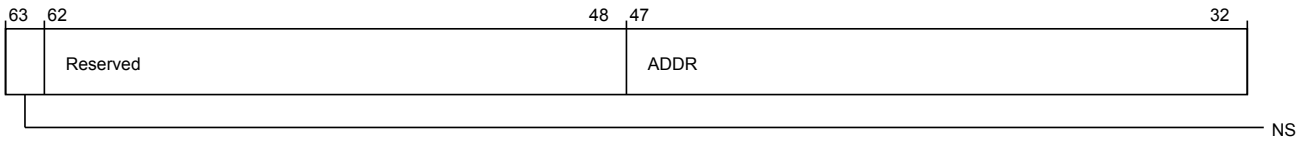


Figure 3-620 por_hni_por_hni_erraddr_ns (high)

The following table shows the por_hni_erraddr_NS higher register bit assignments.

Table 3-634 por_hni_por_hni_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_hni_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

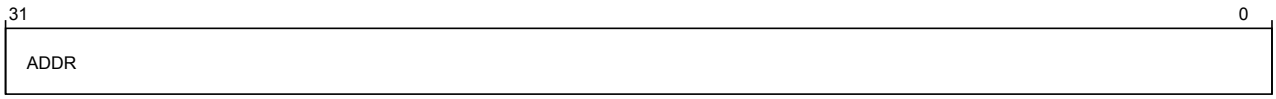


Figure 3-621 por_hni_por_hni_erraddr_ns (low)

The following table shows the por_hni_erraddr_NS lower register bit assignments.

Table 3-635 por_hni_por_hni_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_hni_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3120

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

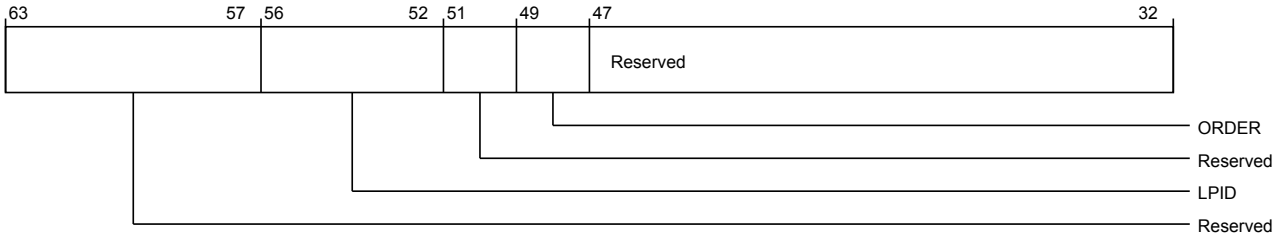


Figure 3-622 por_hni_por_hni_errmisc_ns (high)

The following table shows the por_hni_errmisc_NS higher register bit assignments.

Table 3-636 por_hni_por_hni_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:57	Reserved	Reserved	RO	-
56:52	LPID	Error logic processor ID	RW	5'b0
51:50	Reserved	Reserved	RO	-
49:48	ORDER	Error order	RW	4'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

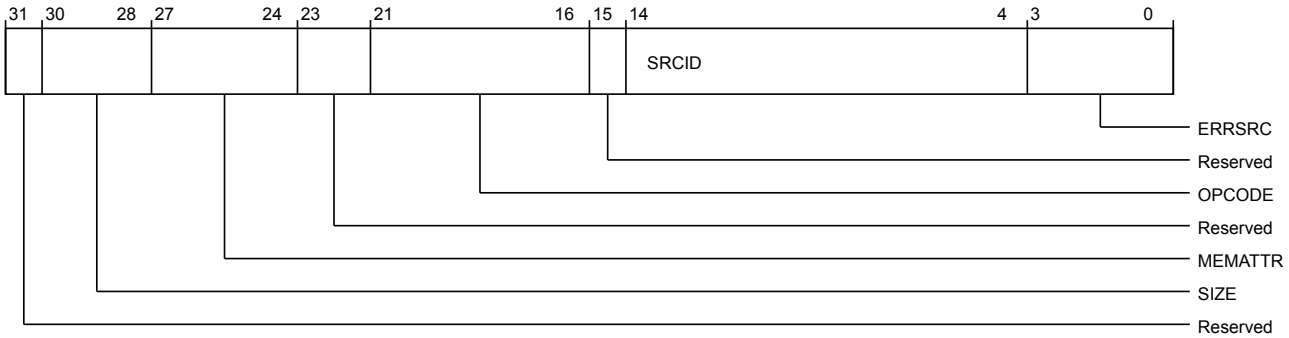


Figure 3-623 por_hni_por_hni_errmisc_ns (low)

The following table shows the por_hni_errmisc_NS lower register bit assignments.

Table 3-637 por_hni_por_hni_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:22	Reserved	Reserved	RO	-

Table 3-637 por_hni_por_hni_errmisc_ns (low) (continued)

Bits	Field name	Description	Type	Reset
21:16	OPCODE	Error opcode	RW	6'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	ERRSRC	Error source 4'b0000: Coherent read 4'b0001: Coherent write 4'b0010: CleanUnique/MakeUnique 4'b0011: Atomic 4'b0100: Illegal configuration read 4'b0101: Illegal configuration write 4'b0110: Configuration write data partial byte enable error 4'b0111: Configuration write data parity error or poison error 4'b1000: BRESP error 4'b1001: Poison error 4'b1010: BRESP error and poison error NOTE: For configuration write data, BRESP, and poison errors, por_hni_errmisc_NS.SRCID is the only valid field. For other error types, all fields are valid.	RW	4'b0

por_hni_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

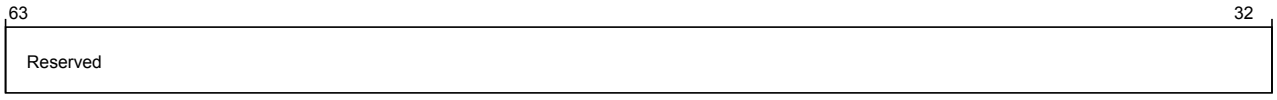


Figure 3-624 por_hni_por_hni_pmu_event_sel (high)

The following table shows the por_hni_pmu_event_sel higher register bit assignments.

Table 3-638 por_hni_por_hni_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

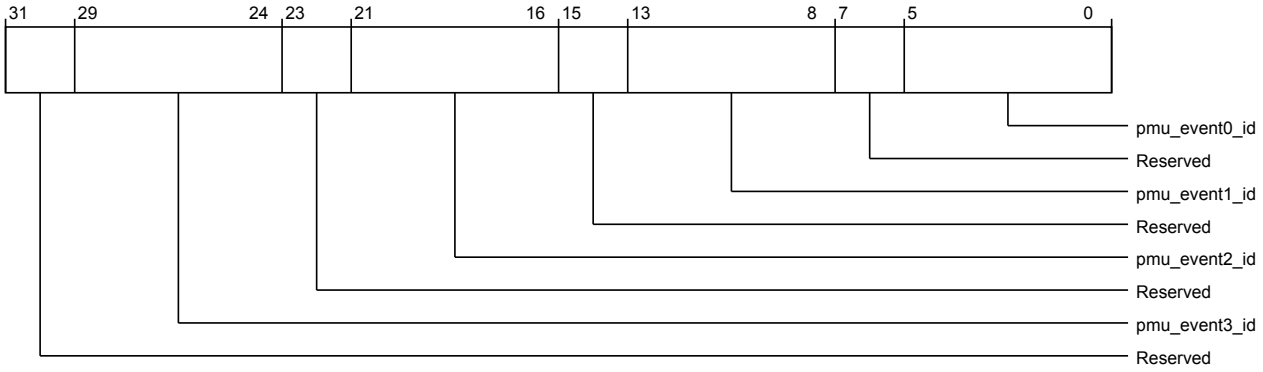


Figure 3-625 por_hni_por_hni_pmu_event_sel (low)

The following table shows the por_hni_pmu_event_sel lower register bit assignments.

Table 3-639 por_hni_por_hni_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	HN-I PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	HN-I PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	HN-I PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0

Table 3-639 por_hni_por_hni_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	HN-I PMU Event 0 select 6'h00: No event 6'h20: RRT read occupancy count overflow 6'h21: RRT write occupancy count overflow 6'h22: RDT read occupancy count overflow 6'h23: RDT write occupancy count overflow 6'h24: WDB occupancy count overflow 6'h25: RRT read allocation 6'h26: RRT write allocation 6'h27: RDT read allocation 6'h28: RDT write allocation 6'h29: WDB allocation 6'h2A: RETRYACK TXRSP flit sent 6'h2B: ARVALID set without ARREADY event 6'h2C: ARREADY set without ARVALID event 6'h2D: AWVALID set without AWREADY event 6'h2E: AWREADY set without AWVALID event 6'h2F: WVALID set without WREADY event 6'h30: TXDAT stall (TXDAT valid but no link credit available) 6'h31: Non-PCIe serialization event 6'h32: PCIe serialization event NOTE: All other encodings are reserved.	RW	6'b0

3.3.6 XP register descriptions

Lists the XP registers.

por_mxp_node_info

Provides component identification information.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h0

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

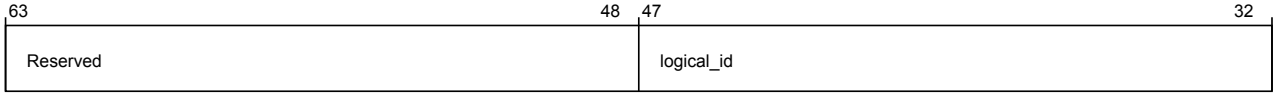


Figure 3-626 por_mxp_por_mxp_node_info (high)

The following table shows the por_mxp_node_info higher register bit assignments.

Table 3-640 por_mxp_por_mxp_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

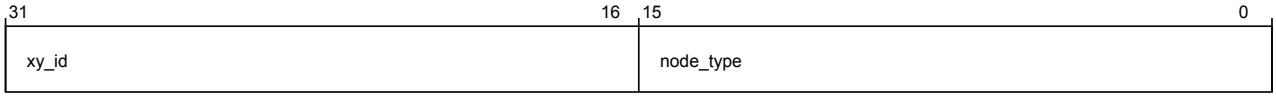


Figure 3-627 por_mxp_por_mxp_node_info (low)

The following table shows the por_mxp_node_info lower register bit assignments.

Table 3-641 por_mxp_por_mxp_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	xy_id	Identifies (X,Y) location of XP within the mesh NOTE: The (X,Y) location is specified following the node ID format as defined in Node ID mapping section, with the bottom 3 bits, corresponding to port ID and device ID, set to 0. Bits 31:11 must always be set to 0. The range of bits representing the (X,Y) location varies for different node ID formats.	RO	16'h0000
15:0	node_type	CMN-600 node type identifier	RO	16'h0006

por_mxp_device_port_connect_info_p0

Contains device port connection information for port 0.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h8
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

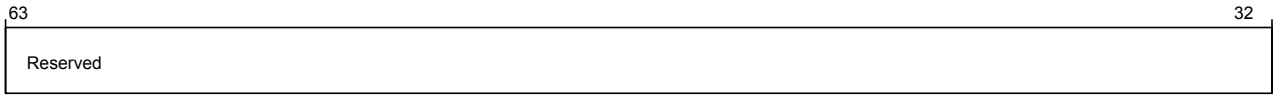


Figure 3-628 por_mxp_por_mxp_device_port_connect_info_p0 (high)

The following table shows the por_mxp_device_port_connect_info_p0 higher register bit assignments.

Table 3-642 por_mxp_por_mxp_device_port_connect_info_p0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

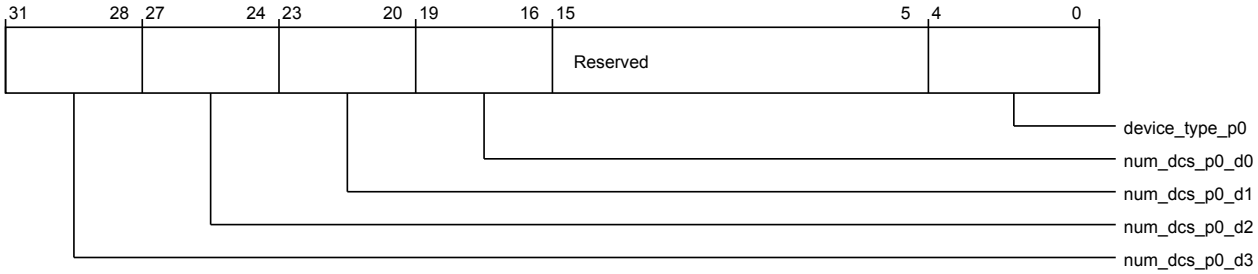


Figure 3-629 por_mxp_por_mxp_device_port_connect_info_p0 (low)

The following table shows the por_mxp_device_port_connect_info_p0 lower register bit assignments.

Table 3-643 por_mxp_por_mxp_device_port_connect_info_p0 (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p0_d3	Number of device credited slices connected to port 0 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p0_d2	Number of device credited slices connected to port 0 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p0_d1	Number of device credited slices connected to port 0 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p0_d0	Number of device credited slices connected to port 0 device 0 (Allowed values: 0-4)	RO	Configuration dependent
15:5	Reserved	Reserved	RO	-
4:0	device_type_p0	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F_CHIB 5'b00101: RN-F_CHIB_ESAM 5'b00110: RN-F_CHIA 5'b00111: RN-F_CHIA_ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F 5'b01101: SBSX 5'b01110: HN-F 5'b01111: Reserved 5'b10000: Reserved 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100-5'b11111: Reserved	RO	Configuration dependent

por_mxp_device_port_connect_info_p1

Contains device port connection information for port 1.

Its characteristics are:

Type RO

Register width (Bits) 64
Address offset 14'h10
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

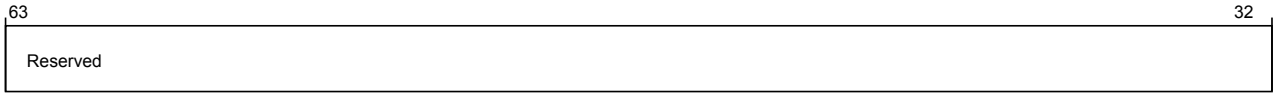


Figure 3-630 por_mxp_por_mxp_device_port_connect_info_p1 (high)

The following table shows the por_mxp_device_port_connect_info_p1 higher register bit assignments.

Table 3-644 por_mxp_por_mxp_device_port_connect_info_p1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

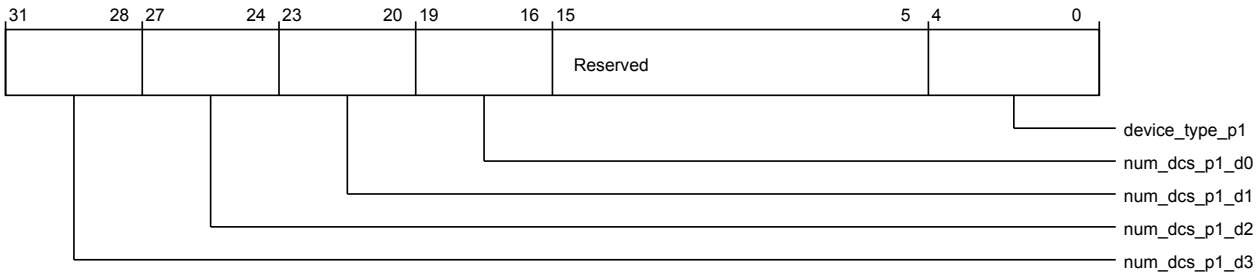


Figure 3-631 por_mxp_por_mxp_device_port_connect_info_p1 (low)

The following table shows the por_mxp_device_port_connect_info_p1 lower register bit assignments.

Table 3-645 por_mxp_por_mxp_device_port_connect_info_p1 (low)

Bits	Field name	Description	Type	Reset
31:28	num_dcs_p1_d3	Number of device credited slices connected to port 1 device 3 (Allowed values: 0-4)	RO	Configuration dependent
27:24	num_dcs_p1_d2	Number of device credited slices connected to port 1 device 2 (Allowed values: 0-4)	RO	Configuration dependent
23:20	num_dcs_p1_d1	Number of device credited slices connected to port 1 device 1 (Allowed values: 0-4)	RO	Configuration dependent
19:16	num_dcs_p1_d0	Number of device credited slices connected to port 1 device 0 (Allowed values: 0-4)	RO	Configuration dependent

Table 3-645 por_mxp_por_mxp_device_port_connect_info_p1 (low) (continued)

Bits	Field name	Description	Type	Reset
15:5	Reserved	Reserved	RO	-
4:0	device_type_p1	Connected device type 5'b00000: Reserved 5'b00001: RN-I 5'b00010: RN-D 5'b00011: Reserved 5'b00100: RN-F CHIB 5'b00101: RN-F CHIB ESAM 5'b00110: RN-F CHIA 5'b00111: RN-F CHIA ESAM 5'b01000: HN-T 5'b01001: HN-I 5'b01010: HN-D 5'b01011: Reserved 5'b01100: SN-F 5'b01101: SBSX 5'b01110: HN-F 5'b01111: Reserved 5'b10000: Reserved 5'b10001: CXHA 5'b10010: CXRA 5'b10011: CXRH 5'b10100-5'b11111: Reserved	RO	Configuration dependent

por_mxp_mesh_port_connect_info_east

Contains port connection information for East port.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h18
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

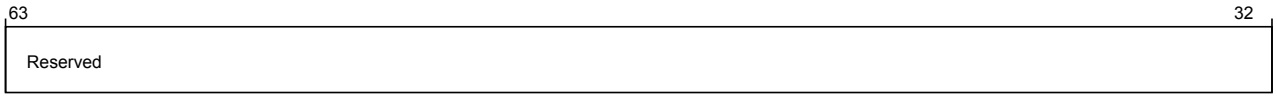


Figure 3-632 por_mxp_por_mxp_mesh_port_connect_info_east (high)

The following table shows the por_mxp_mesh_port_connect_info_east higher register bit assignments.

Table 3-646 por_mxp_por_mxp_mesh_port_connect_info_east (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

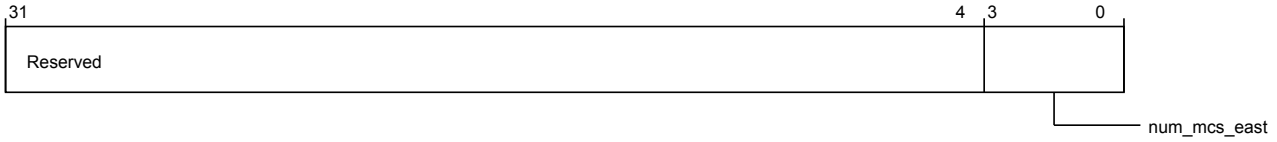


Figure 3-633 por_mxp_por_mxp_mesh_port_connect_info_east (low)

The following table shows the por_mxp_mesh_port_connect_info_east lower register bit assignments.

Table 3-647 por_mxp_por_mxp_mesh_port_connect_info_east (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_east	Number of mesh credited slices connected to East port (Allowed values: 0-4)	RO	Configuration dependent

por_mxp_mesh_port_connect_info_north

Contains port connection information for North port.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h20
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

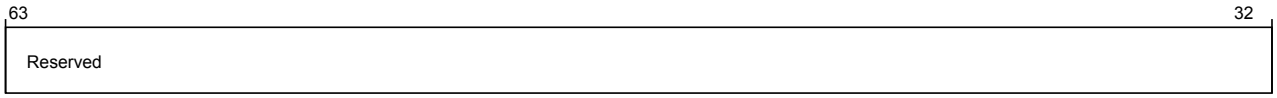


Figure 3-634 por_mxp_por_mxp_mesh_port_connect_info_north (high)

The following table shows the por_mxp_mesh_port_connect_info_north higher register bit assignments.

Table 3-648 por_mxp_por_mxp_mesh_port_connect_info_north (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

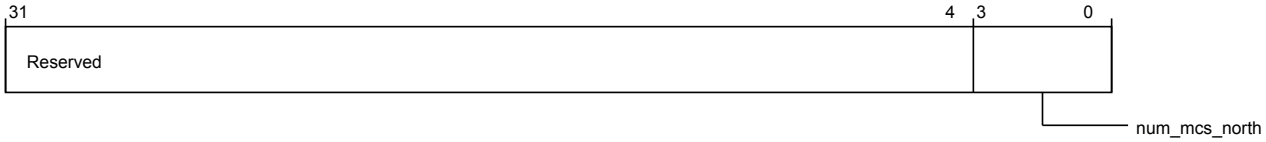


Figure 3-635 por_mxp_por_mxp_mesh_port_connect_info_north (low)

The following table shows the por_mxp_mesh_port_connect_info_north lower register bit assignments.

Table 3-649 por_mxp_por_mxp_mesh_port_connect_info_north (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	num_mcs_north	Number of mesh credited slices connected to North port (Allowed values: 0-4)	RO	Configuration dependent

por_mxp_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

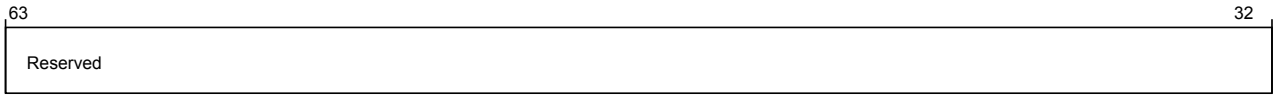


Figure 3-636 por_mxp_por_mxp_child_info (high)

The following table shows the por_mxp_child_info higher register bit assignments.

Table 3-650 por_mxp_por_mxp_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

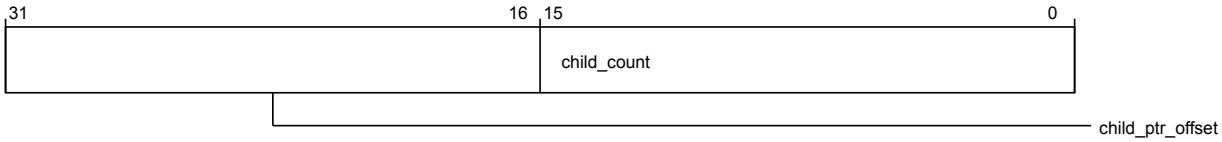


Figure 3-637 por_mxp_por_mxp_child_info (low)

The following table shows the por_mxp_child_info lower register bit assignments.

Table 3-651 por_mxp_por_mxp_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h100
15:0	child_count	Number of child nodes; used in discovery process	RO	Configuration dependent

por_mxp_child_pointer_0

Contains base address of the configuration slave for child 0.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

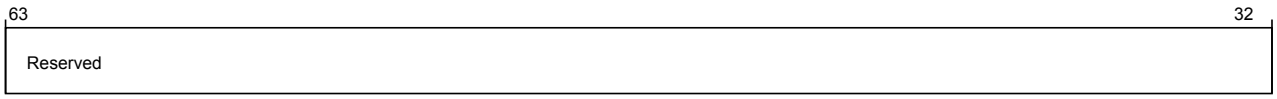


Figure 3-638 por_mxp_por_mxp_child_pointer_0 (high)

The following table shows the por_mxp_child_pointer_0 higher register bit assignments.

Table 3-652 por_mxp_por_mxp_child_pointer_0 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

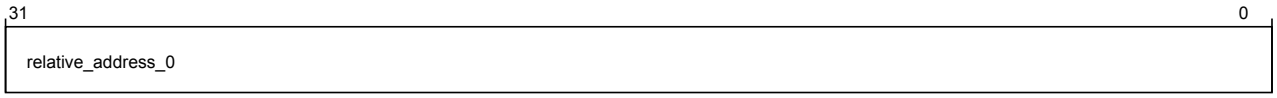


Figure 3-639 por_mxp_por_mxp_child_pointer_0 (low)

The following table shows the por_mxp_child_pointer_0 lower register bit assignments.

Table 3-653 por_mxp_por_mxp_child_pointer_0 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_0	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_1

Contains base address of the configuration slave for child 1.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h108
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

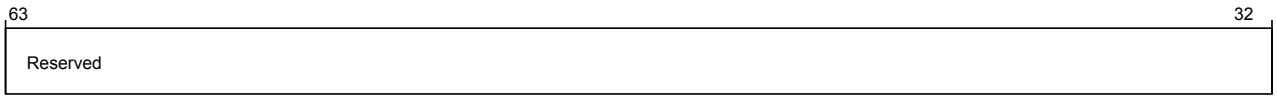


Figure 3-640 por_mxp_por_mxp_child_pointer_1 (high)

The following table shows the por_mxp_child_pointer_1 higher register bit assignments.

Table 3-654 por_mxp_por_mxp_child_pointer_1 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

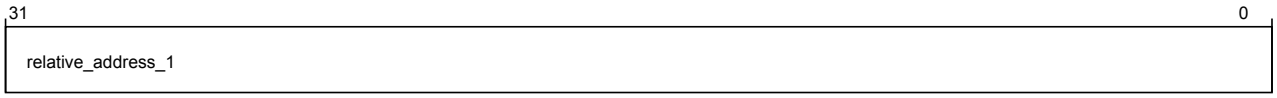


Figure 3-641 por_mxp_por_mxp_child_pointer_1 (low)

The following table shows the por_mxp_child_pointer_1 lower register bit assignments.

Table 3-655 por_mxp_por_mxp_child_pointer_1 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_1	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_2

Contains base address of the configuration slave for child 2.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

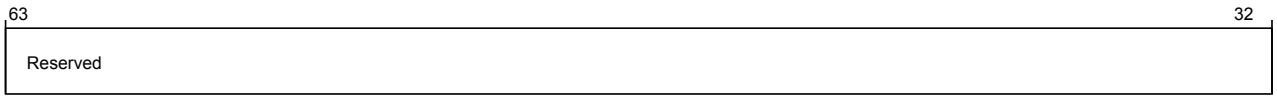


Figure 3-642 por_mxp_por_mxp_child_pointer_2 (high)

The following table shows the por_mxp_child_pointer_2 higher register bit assignments.

Table 3-656 por_mxp_por_mxp_child_pointer_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

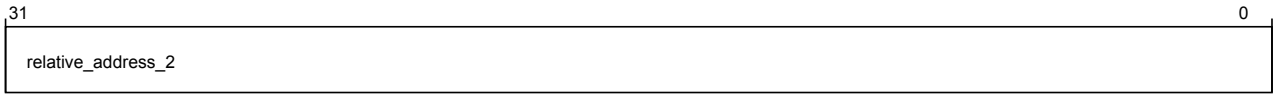


Figure 3-643 por_mxp_por_mxp_child_pointer_2 (low)

The following table shows the por_mxp_child_pointer_2 lower register bit assignments.

Table 3-657 por_mxp_por_mxp_child_pointer_2 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_2	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_3

Contains base address of the configuration slave for child 3.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

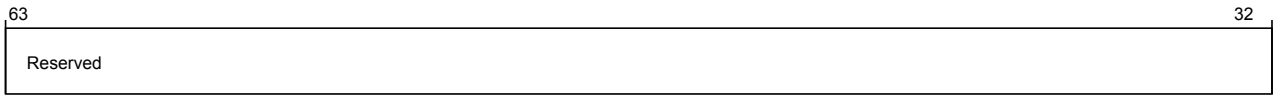


Figure 3-644 por_mxp_por_mxp_child_pointer_3 (high)

The following table shows the por_mxp_child_pointer_3 higher register bit assignments.

Table 3-658 por_mxp_por_mxp_child_pointer_3 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

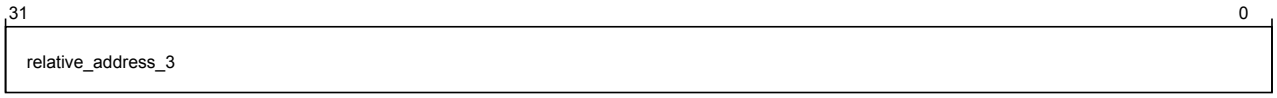


Figure 3-645 por_mxp_por_mxp_child_pointer_3 (low)

The following table shows the por_mxp_child_pointer_3 lower register bit assignments.

Table 3-659 por_mxp_por_mxp_child_pointer_3 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_3	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_4

Contains base address of the configuration slave for child 4.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

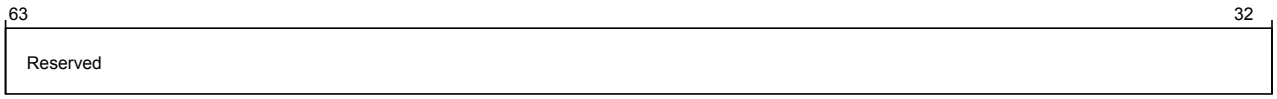


Figure 3-646 por_mxp_por_mxp_child_pointer_4 (high)

The following table shows the por_mxp_child_pointer_4 higher register bit assignments.

Table 3-660 por_mxp_por_mxp_child_pointer_4 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

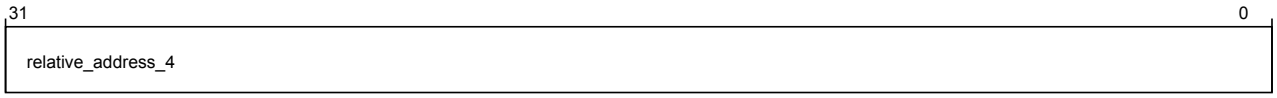


Figure 3-647 por_mxp_por_mxp_child_pointer_4 (low)

The following table shows the por_mxp_child_pointer_4 lower register bit assignments.

Table 3-661 por_mxp_por_mxp_child_pointer_4 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_4	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_5

Contains base address of the configuration slave for child 5.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

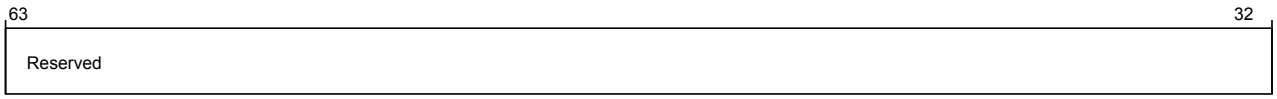


Figure 3-648 por_mxp_por_mxp_child_pointer_5 (high)

The following table shows the por_mxp_child_pointer_5 higher register bit assignments.

Table 3-662 por_mxp_por_mxp_child_pointer_5 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

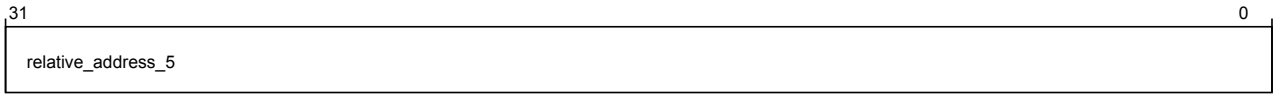


Figure 3-649 por_mxp_por_mxp_child_pointer_5 (low)

The following table shows the por_mxp_child_pointer_5 lower register bit assignments.

Table 3-663 por_mxp_por_mxp_child_pointer_5 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_5	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_6

Contains base address of the configuration slave for child 6.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h130
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

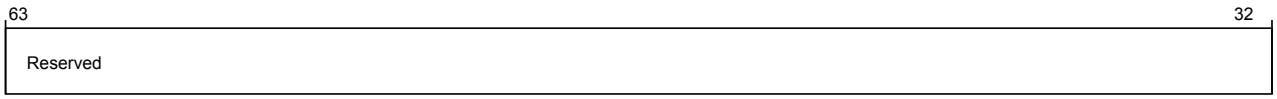


Figure 3-650 por_mxp_por_mxp_child_pointer_6 (high)

The following table shows the por_mxp_child_pointer_6 higher register bit assignments.

Table 3-664 por_mxp_por_mxp_child_pointer_6 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

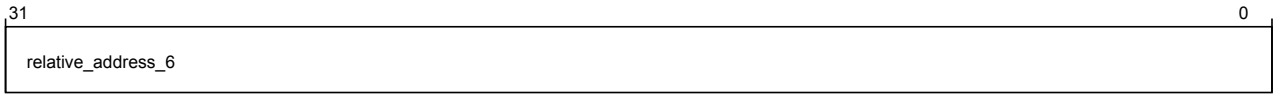


Figure 3-651 por_mxp_por_mxp_child_pointer_6 (low)

The following table shows the por_mxp_child_pointer_6 lower register bit assignments.

Table 3-665 por_mxp_por_mxp_child_pointer_6 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_6	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_7

Contains base address of the configuration slave for child 7.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h138
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

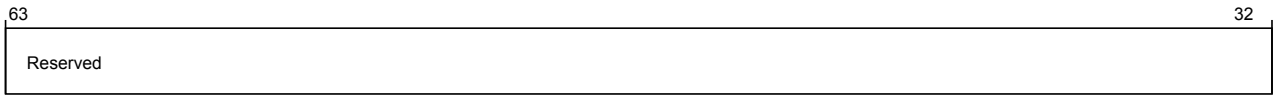


Figure 3-652 por_mxp_por_mxp_child_pointer_7 (high)

The following table shows the por_mxp_child_pointer_7 higher register bit assignments.

Table 3-666 por_mxp_por_mxp_child_pointer_7 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

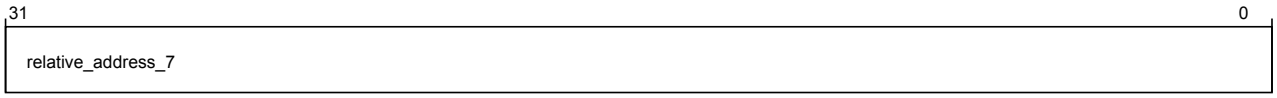


Figure 3-653 por_mxp_por_mxp_child_pointer_7 (low)

The following table shows the por_mxp_child_pointer_7 lower register bit assignments.

Table 3-667 por_mxp_por_mxp_child_pointer_7 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_7	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_8

Contains base address of the configuration slave for child 8.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h140
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

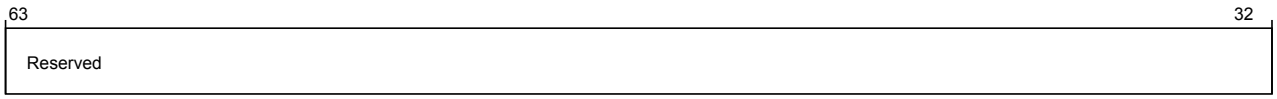


Figure 3-654 por_mxp_por_mxp_child_pointer_8 (high)

The following table shows the por_mxp_child_pointer_8 higher register bit assignments.

Table 3-668 por_mxp_por_mxp_child_pointer_8 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

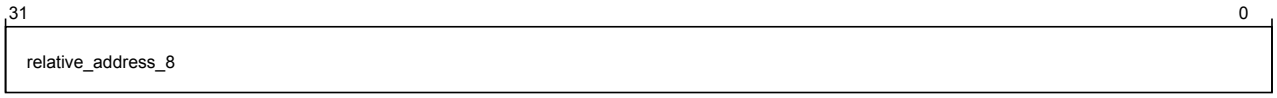


Figure 3-655 por_mxp_por_mxp_child_pointer_8 (low)

The following table shows the por_mxp_child_pointer_8 lower register bit assignments.

Table 3-669 por_mxp_por_mxp_child_pointer_8 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_8	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_9

Contains base address of the configuration slave for child 9.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h148
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

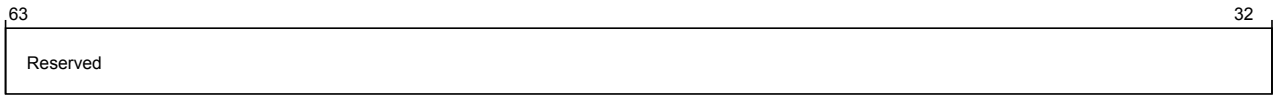


Figure 3-656 por_mxp_por_mxp_child_pointer_9 (high)

The following table shows the por_mxp_child_pointer_9 higher register bit assignments.

Table 3-670 por_mxp_por_mxp_child_pointer_9 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

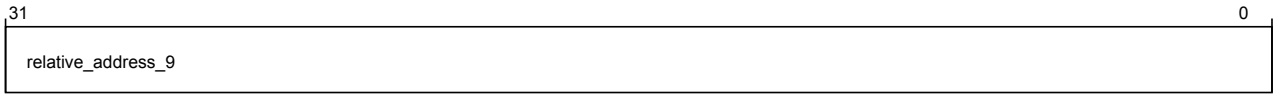


Figure 3-657 por_mxp_por_mxp_child_pointer_9 (low)

The following table shows the por_mxp_child_pointer_9 lower register bit assignments.

Table 3-671 por_mxp_por_mxp_child_pointer_9 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_9	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_10

Contains base address of the configuration slave for child 10.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h150
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

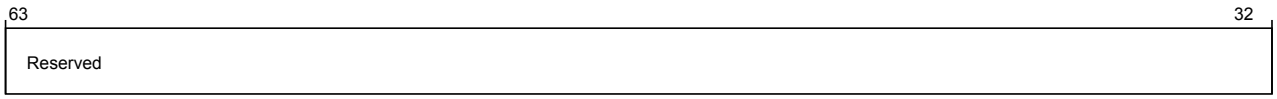


Figure 3-658 por_mxp_por_mxp_child_pointer_10 (high)

The following table shows the por_mxp_child_pointer_10 higher register bit assignments.

Table 3-672 por_mxp_por_mxp_child_pointer_10 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

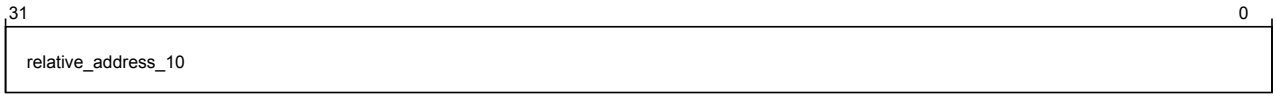


Figure 3-659 por_mxp_por_mxp_child_pointer_10 (low)

The following table shows the por_mxp_child_pointer_10 lower register bit assignments.

Table 3-673 por_mxp_por_mxp_child_pointer_10 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_10	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_11

Contains base address of the configuration slave for child 11.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h158
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

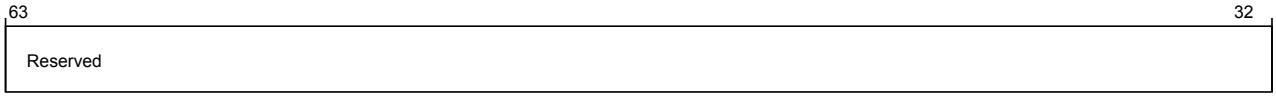


Figure 3-660 por_mxp_por_mxp_child_pointer_11 (high)

The following table shows the por_mxp_child_pointer_11 higher register bit assignments.

Table 3-674 por_mxp_por_mxp_child_pointer_11 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

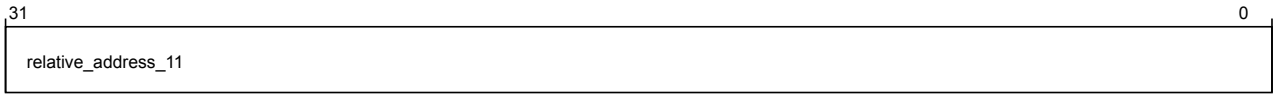


Figure 3-661 por_mxp_por_mxp_child_pointer_11 (low)

The following table shows the por_mxp_child_pointer_11 lower register bit assignments.

Table 3-675 por_mxp_por_mxp_child_pointer_11 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_11	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_12

Contains base address of the configuration slave for child 12.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h160
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

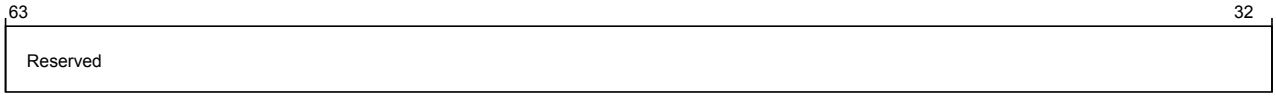


Figure 3-662 por_mxp_por_mxp_child_pointer_12 (high)

The following table shows the por_mxp_child_pointer_12 higher register bit assignments.

Table 3-676 por_mxp_por_mxp_child_pointer_12 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

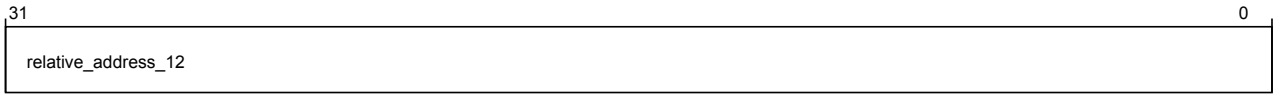


Figure 3-663 por_mxp_por_mxp_child_pointer_12 (low)

The following table shows the por_mxp_child_pointer_12 lower register bit assignments.

Table 3-677 por_mxp_por_mxp_child_pointer_12 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_12	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_13

Contains base address of the configuration slave for child 13.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h168
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

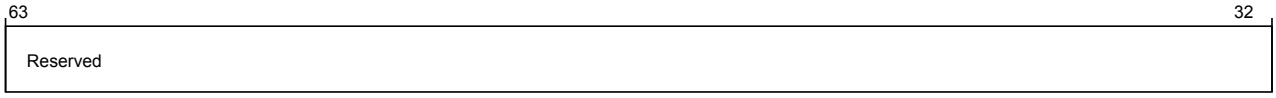


Figure 3-664 por_mxp_por_mxp_child_pointer_13 (high)

The following table shows the por_mxp_child_pointer_13 higher register bit assignments.

Table 3-678 por_mxp_por_mxp_child_pointer_13 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

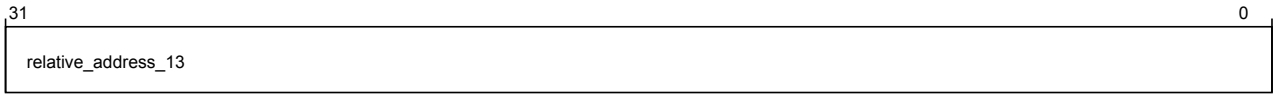


Figure 3-665 por_mxp_por_mxp_child_pointer_13 (low)

The following table shows the por_mxp_child_pointer_13 lower register bit assignments.

Table 3-679 por_mxp_por_mxp_child_pointer_13 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_13	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_14

Contains base address of the configuration slave for child 14.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h170
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

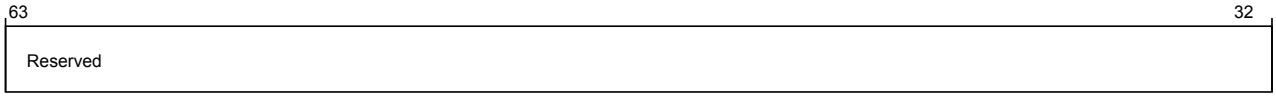


Figure 3-666 por_mxp_por_mxp_child_pointer_14 (high)

The following table shows the por_mxp_child_pointer_14 higher register bit assignments.

Table 3-680 por_mxp_por_mxp_child_pointer_14 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

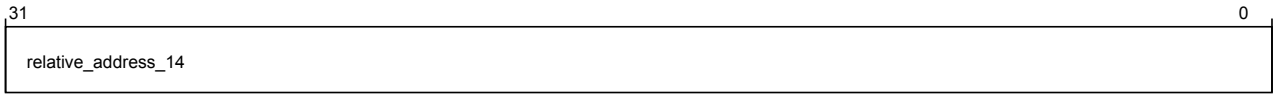


Figure 3-667 por_mxp_por_mxp_child_pointer_14 (low)

The following table shows the por_mxp_child_pointer_14 lower register bit assignments.

Table 3-681 por_mxp_por_mxp_child_pointer_14 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_14	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_child_pointer_15

Contains base address of the configuration slave for child 15.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h178
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

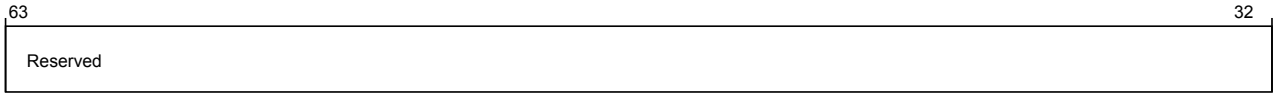


Figure 3-668 por_mxp_por_mxp_child_pointer_15 (high)

The following table shows the por_mxp_child_pointer_15 higher register bit assignments.

Table 3-682 por_mxp_por_mxp_child_pointer_15 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

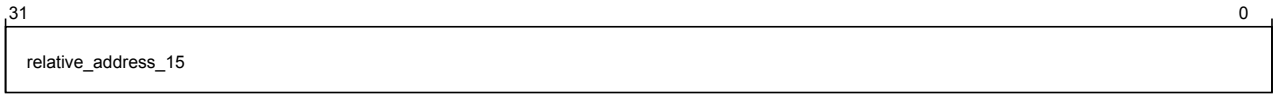


Figure 3-669 por_mxp_por_mxp_child_pointer_15 (low)

The following table shows the por_mxp_child_pointer_15 lower register bit assignments.

Table 3-683 por_mxp_por_mxp_child_pointer_15 (low)

Bits	Field name	Description	Type	Reset
31:0	relative_address_15	Bit [31]: External or internal child node 1'b1: Indicates this child pointer points to a configuration node that is external to CMN-600 1'b0: Indicates this child pointer points to a configuration node that is internal to CMN-600 Bits [30:28]: Set to 3'b000 Bits [27:0]: Child node address offset relative to PERIPHBASE	RO	32'b0

por_mxp_p0_info

Provides component identification information for XP port 0.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

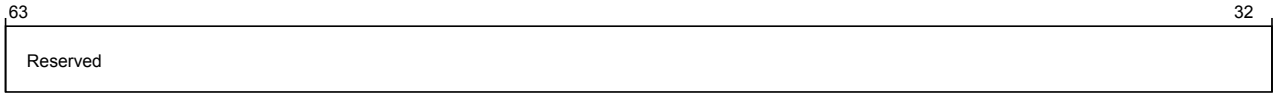


Figure 3-670 por_mxp_por_mxp_p0_info (high)

The following table shows the por_mxp_p0_info higher register bit assignments.

Table 3-684 por_mxp_por_mxp_p0_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

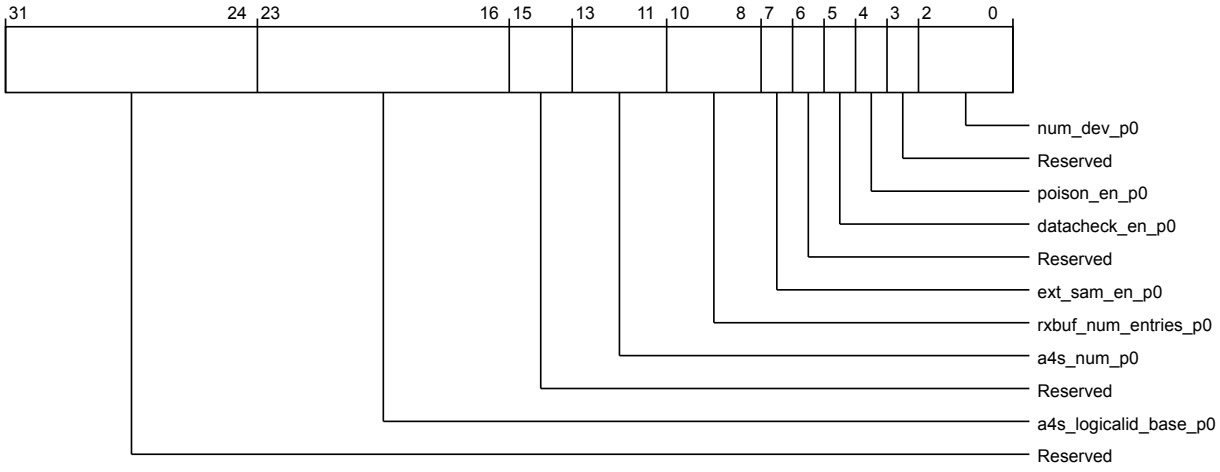


Figure 3-671 por_mxp_por_mxp_p0_info (low)

The following table shows the por_mxp_p0_info lower register bit assignments.

Table 3-685 por_mxp_por_mxp_p0_info (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	a4s_logicalid_base_p0	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p0	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p0	Number of input buffers for each device at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p0	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p0	Datacheck enable	RO	Configuration dependent
4	poison_en_p0	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p0	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

por_mxp_p1_info

Provides component identification information for XP port 1.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h908

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

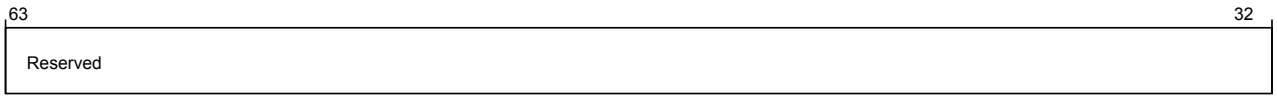


Figure 3-672 por_mxp_por_mxp_p1_info (high)

The following table shows the por_mxp_p1_info higher register bit assignments.

Table 3-686 por_mxp_por_mxp_p1_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

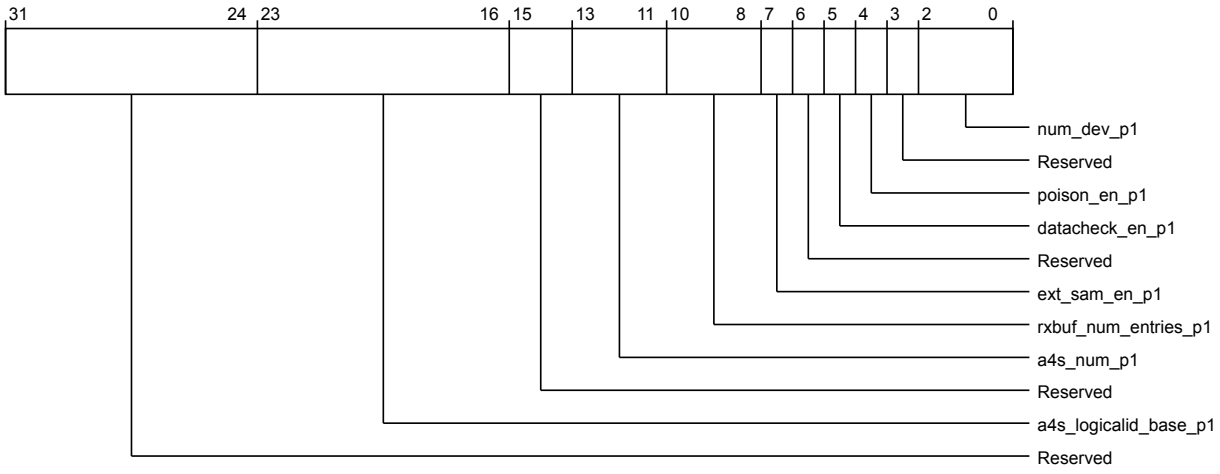


Figure 3-673 por_mxp_por_mxp_p1_info (low)

The following table shows the por_mxp_p1_info lower register bit assignments.

Table 3-687 por_mxp_por_mxp_p1_info (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:16	a4s_logicalid_base_p1	AXI4Stream interfaces logical ID base at this port (0 or 1)	RO	Configuration dependent
15:14	Reserved	Reserved	RO	-
13:11	a4s_num_p1	Total number of RN-F AXI4Stream interfaces at this port (0 to 4)	RO	Configuration dependent
10:8	rxbuf_num_entries_p1	Number of input buffers at this port (2 to 4)	RO	Configuration dependent
7	ext_sam_en_p1	ESAM enable	RO	Configuration dependent
6	Reserved	Reserved	RO	-
5	datacheck_en_p1	Datacheck enable	RO	Configuration dependent

Table 3-687 por_mxp_por_mxp_p1_info (low) (continued)

Bits	Field name	Description	Type	Reset
4	poison_en_p1	Poison enable	RO	Configuration dependent
3	Reserved	Reserved	RO	-
2:0	num_dev_p1	Number of devices connected to this port (0 to 4)	RO	Configuration dependent

por_mxp_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

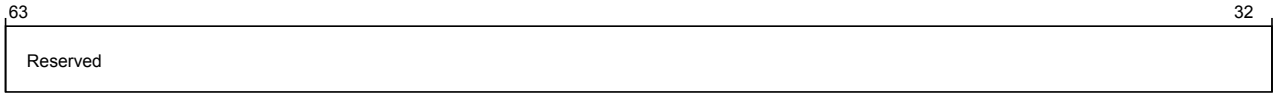


Figure 3-674 por_mxp_por_mxp_secure_register_groups_override (high)

The following table shows the por_mxp_secure_register_groups_override higher register bit assignments.

Table 3-688 por_mxp_por_mxp_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

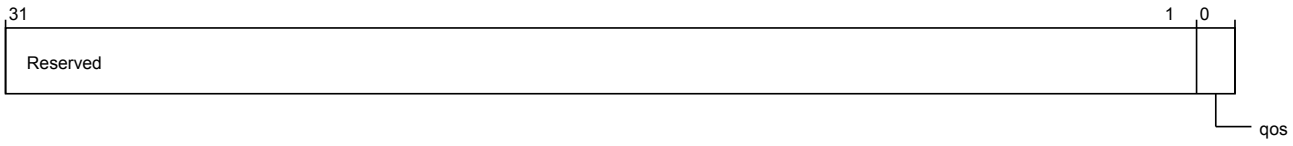


Figure 3-675 por_mxp_por_mxp_secure_register_groups_override (low)

The following table shows the por_mxp_secure_register_groups_override lower register bit assignments.

Table 3-689 por_mxp_por_mxp_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	qos	Allows non-secure access to secure QoS registers	RW	1'b0

por_mxp_aux_ctl

Functions as the auxiliary control register for XP.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

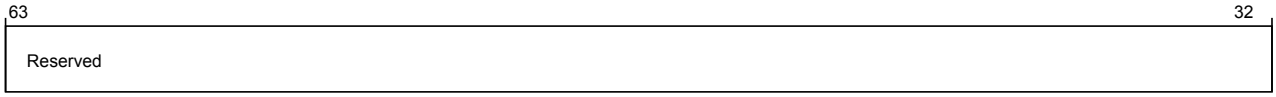


Figure 3-676 por_mxp_por_mxp_aux_ctl (high)

The following table shows the por_mxp_aux_ctl higher register bit assignments.

Table 3-690 por_mxp_por_mxp_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

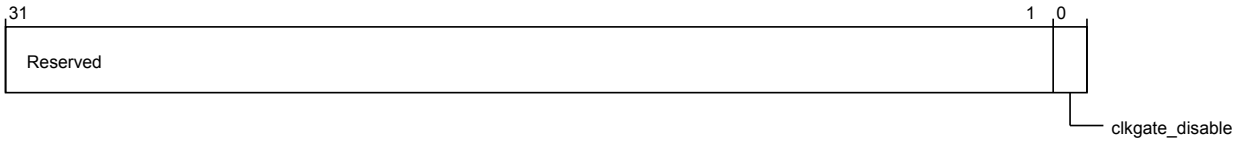


Figure 3-677 por_mxp_por_mxp_aux_ctl (low)

The following table shows the por_mxp_aux_ctl lower register bit assignments.

Table 3-691 por_mxp_por_mxp_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables clock gating when set	RW	1'b0

por_mxp_p0_qos_control

Controls QoS settings for devices connected to port 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA80
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

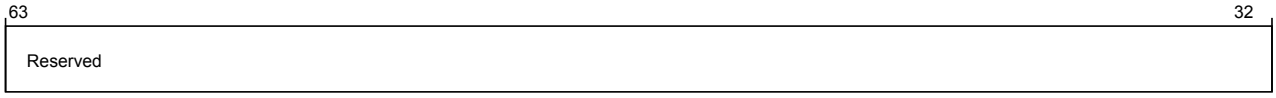


Figure 3-678 por_mxp_por_mxp_p0_qos_control (high)

The following table shows the por_mxp_p0_qos_control higher register bit assignments.

Table 3-692 por_mxp_por_mxp_p0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

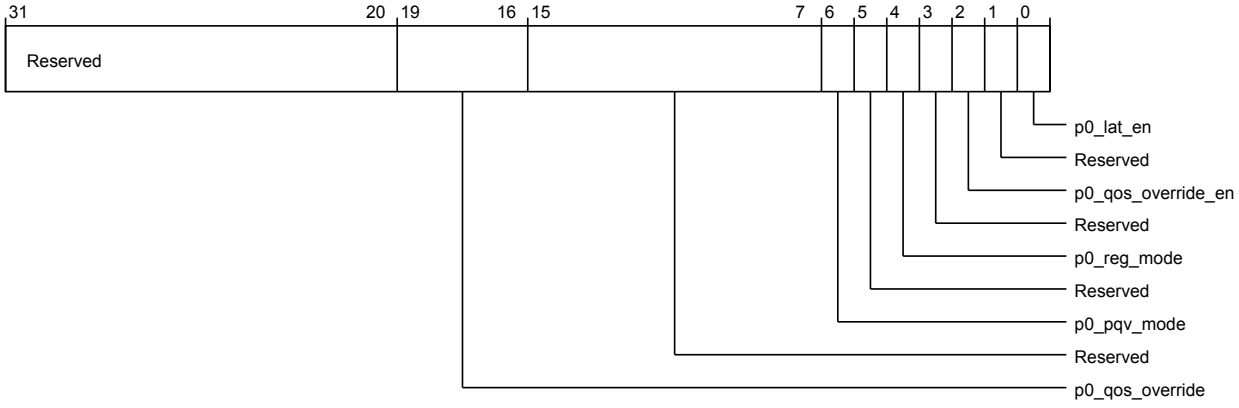


Figure 3-679 por_mxp_por_mxp_p0_qos_control (low)

The following table shows the por_mxp_p0_qos_control lower register bit assignments.

Table 3-693 por_mxp_por_mxp_p0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	p0_qos_override	QoS override value for port 0	RW	4'b0000
15:7	Reserved	Reserved	RO	-
6	p0_pqv_mode	Configures the QoS regulator mode during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	Reserved	Reserved	RO	-
4	p0_reg_mode	Configures the QoS regulator mode 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	Reserved	Reserved	RO	-
2	p0_qos_override_en	Enables port 0 QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
1	Reserved	Reserved	RO	-
0	p0_lat_en	Enables port 0 QoS regulation when set	RW	1'b0

por_mxp_p0_qos_lat_tgt

Controls QoS target latency/period (in cycles) for regulation of devices connected to port 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA88
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

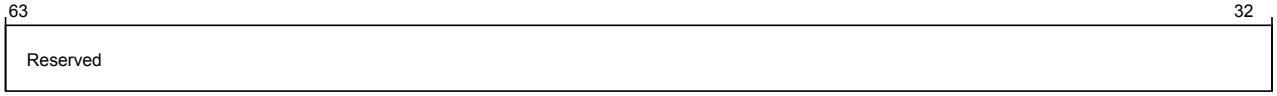


Figure 3-680 por_mxp_por_mxp_p0_qos_lat_tgt (high)

The following table shows the por_mxp_p0_qos_lat_tgt higher register bit assignments.

Table 3-694 por_mxp_por_mxp_p0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

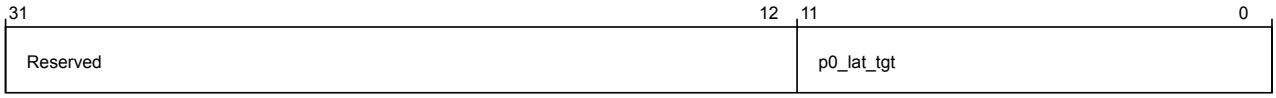


Figure 3-681 por_mxp_por_mxp_p0_qos_lat_tgt (low)

The following table shows the por_mxp_p0_qos_lat_tgt lower register bit assignments.

Table 3-695 por_mxp_por_mxp_p0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	p0_lat_tgt	Port 0 transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

por_mxp_p0_qos_lat_scale

Controls the QoS target scale factor for devices connected to port 0. The scale factor is represented in powers of two from the range 2^(-3) to 2^(-10).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

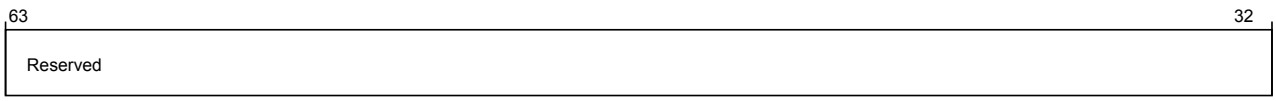


Figure 3-682 por_mxp_por_mxp_p0_qos_lat_scale (high)

The following table shows the por_mxp_p0_qos_lat_scale higher register bit assignments.

Table 3-696 por_mxp_por_mxp_p0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

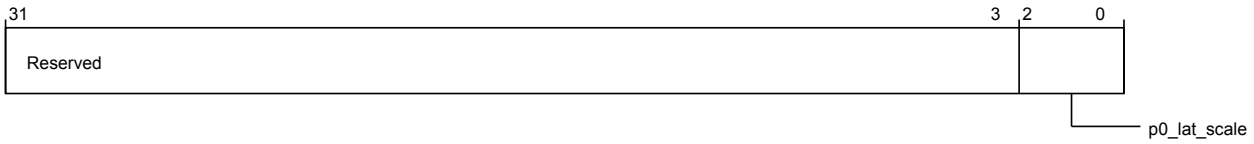


Figure 3-683 por_mxp_por_mxp_p0_qos_lat_scale (low)

The following table shows the por_mxp_p0_qos_lat_scale lower register bit assignments.

Table 3-697 por_mxp_por_mxp_p0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	p0_lat_scale	Port 0 QoS scale factor 3'b000: 2^(-3) 3'b001: 2^(-4) 3'b010: 2^(-5) 3'b011: 2^(-6) 3'b100: 2^(-7) 3'b101: 2^(-8) 3'b110: 2^(-9) 3'b111: 2^(-10)	RW	3'h0

por_mxp_p0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA98
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

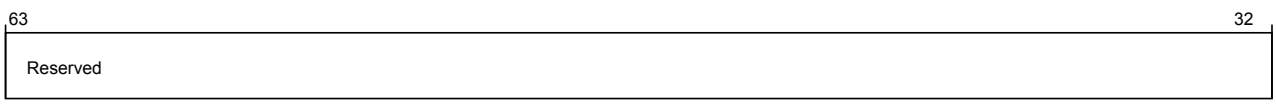


Figure 3-684 por_mxp_por_mxp_p0_qos_lat_range (high)

The following table shows the por_mxp_p0_qos_lat_range higher register bit assignments.

Table 3-698 por_mxp_por_mxp_p0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

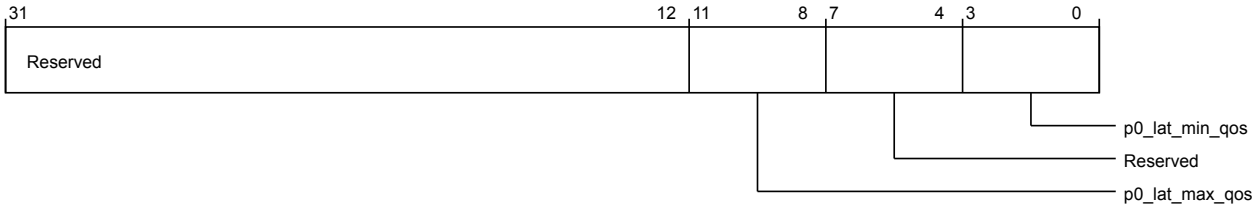


Figure 3-685 por_mxp_por_mxp_p0_qos_lat_range (low)

The following table shows the por_mxp_p0_qos_lat_range lower register bit assignments.

Table 3-699 por_mxp_por_mxp_p0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	p0_lat_max_qos	Port 0 QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	p0_lat_min_qos	Port 0 QoS minimum value	RW	4'h0

por_mxp_p1_qos_control

Controls QoS settings for devices connected to port 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hAA0
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

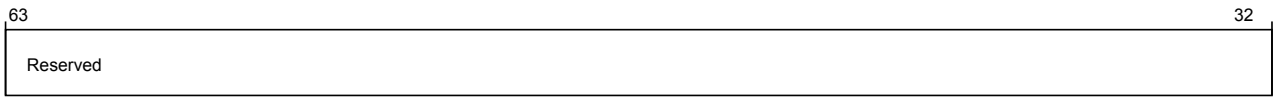


Figure 3-686 por_mxp_por_mxp_p1_qos_control (high)

The following table shows the por_mxp_p1_qos_control higher register bit assignments.

Table 3-700 por_mxp_por_mxp_p1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

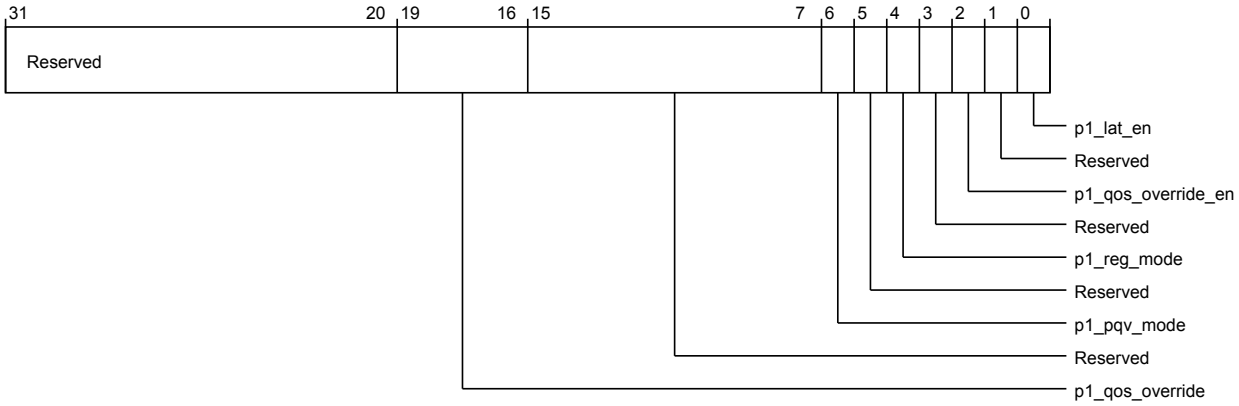


Figure 3-687 por_mxp_por_mxp_p1_qos_control (low)

The following table shows the por_mxp_p1_qos_control lower register bit assignments.

Table 3-701 por_mxp_por_mxp_p1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	p1_qos_override	QoS override value for port 1	RW	4'b0000
15:7	Reserved	Reserved	RO	-
6	p1_pqv_mode	Configures the QoS regulator mode during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	Reserved	Reserved	RO	-
4	p1_reg_mode	Configures the QoS regulator mode 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	Reserved	Reserved	RO	-
2	p1_qos_override_en	Enables port 1 QoS override; when set, allows QoS value on inbound transactions to be overridden	RW	1'b0
1	Reserved	Reserved	RO	-
0	p1_lat_en	Enables port 1 QoS regulation when set	RW	1'b0

por_mxp_p1_qos_lat_tgt

Controls QoS target latency/period (in cycles) for regulation of devices connected to port 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hAA8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

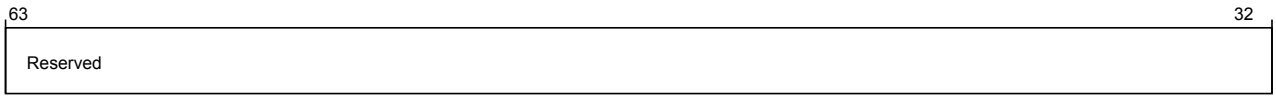


Figure 3-688 por_mxp_por_mxp_p1_qos_lat_tgt (high)

The following table shows the por_mxp_p1_qos_lat_tgt higher register bit assignments.

Table 3-702 por_mxp_por_mxp_p1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

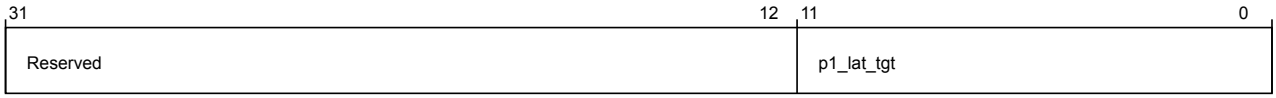


Figure 3-689 por_mxp_por_mxp_p1_qos_lat_tgt (low)

The following table shows the por_mxp_p1_qos_lat_tgt lower register bit assignments.

Table 3-703 por_mxp_por_mxp_p1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:0	p1_lat_tgt	Port 1 transaction target latency/period; a value of 0 corresponds to no regulation	RW	12'h000

por_mxp_p1_qos_lat_scale

Controls the QoS target scale factor for devices connected to port 1. The scale factor is represented in powers of two from the range 2^(-3) to 2^(-10).

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

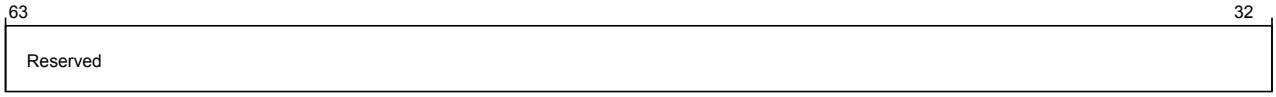


Figure 3-690 por_mxp_por_mxp_p1_qos_lat_scale (high)

The following table shows the por_mxp_p1_qos_lat_scale higher register bit assignments.

Table 3-704 por_mxp_por_mxp_p1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

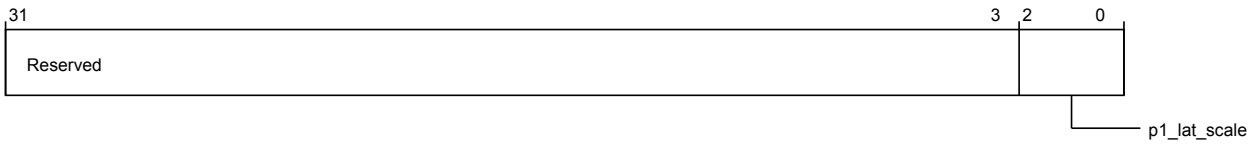


Figure 3-691 por_mxp_por_mxp_p1_qos_lat_scale (low)

The following table shows the por_mxp_p1_qos_lat_scale lower register bit assignments.

Table 3-705 por_mxp_por_mxp_p1_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2:0	p1_lat_scale	Port 1 QoS scale factor 3'b000: 2^(-3) 3'b001: 2^(-4) 3'b010: 2^(-5) 3'b011: 2^(-6) 3'b100: 2^(-7) 3'b101: 2^(-8) 3'b110: 2^(-9) 3'b111: 2^(-10)	RW	3'h0

por_mxp_p1_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS regulator for devices connected to port 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

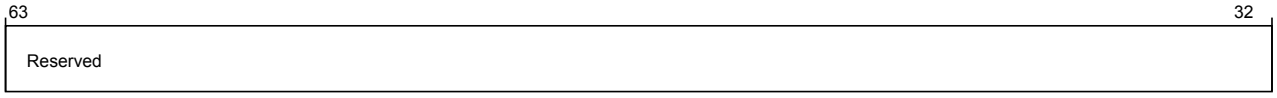


Figure 3-692 por_mxp_por_mxp_p1_qos_lat_range (high)

The following table shows the por_mxp_p1_qos_lat_range higher register bit assignments.

Table 3-706 por_mxp_por_mxp_p1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

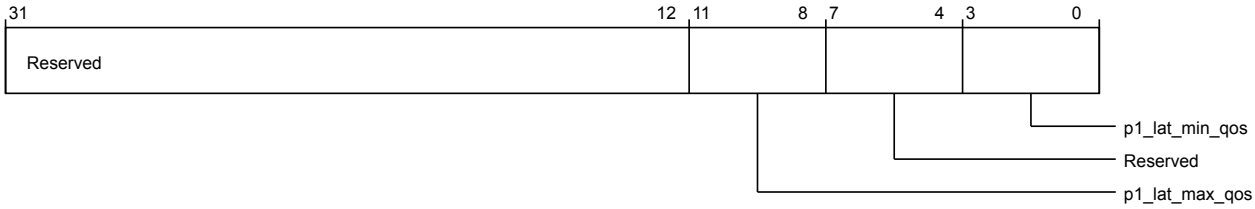


Figure 3-693 por_mxp_por_mxp_p1_qos_lat_range (low)

The following table shows the por_mxp_p1_qos_lat_range lower register bit assignments.

Table 3-707 por_mxp_por_mxp_p1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	p1_lat_max_qos	Port 1 QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	p1_lat_min_qos	Port 1 QoS minimum value	RW	4'h0

por_mxp_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

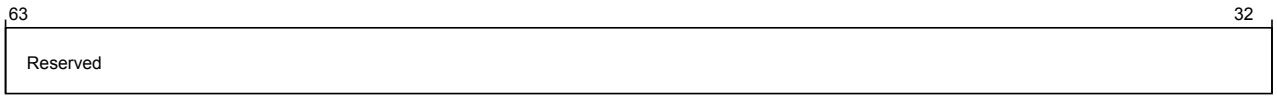


Figure 3-694 por_mxp_por_mxp_pmu_event_sel (high)

The following table shows the por_mxp_pmu_event_sel higher register bit assignments.

Table 3-708 por_mxp_por_mxp_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

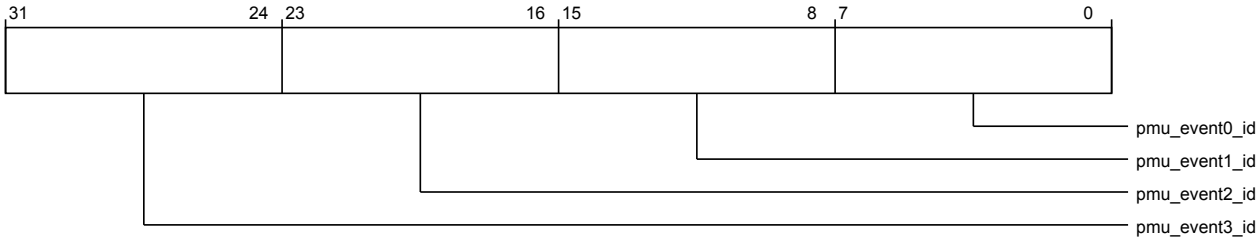


Figure 3-695 por_mxp_por_mxp_pmu_event_sel (low)

The following table shows the por_mxp_pmu_event_sel lower register bit assignments.

Table 3-709 por_mxp_por_mxp_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:24	pmu_event3_id	XP PMU Event 3 ID; see pmu_event0_id for encodings	RW	8'b0
23:16	pmu_event2_id	XP PMU Event 2 ID; see pmu_event0_id for encodings	RW	8'b0

Table 3-709 por_mxp_por_mxp_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
15:8	pmu_event1_id	XP PMU Event 1 ID; see pmu_event0_id for encodings	RW	8'b0
7:0	pmu_event0_id	XP PMU Event 0 ID Bits [7:5]: PC 3'b000: REQ 3'b001: RSP 3'b010: SNP 3'b011: DAT Bits [4:2]: Interface 3'b000: East 3'b001: West 3'b010: North 3'b011: South 3'b100: Device port 0 3'b101: Device port 1 Bits [1:0]: Event specifier 2'b00: No event 2'b01: TX flit valid; signaled when a flit is successfully transmitted 2'b10: TX flit stall; signaled when flit transmission is stalled and waiting on credits 2'b11: Partial DAT flit; signaled when 128-bit DAT flits could not be merged into a 256-bit DAT flit; only applicable on the DAT PC on RN-F CHIA and RN-F CHIA ESAM ports	RW	8'b0

por_mxp_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b0000010100101
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

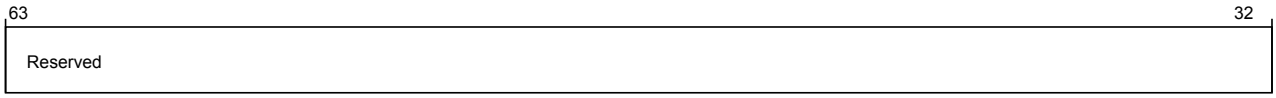


Figure 3-696 por_mxp_por_mxp_errfr (high)

The following table shows the por_mxp_errfr higher register bit assignments.

Table 3-710 por_mxp_por_mxp_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

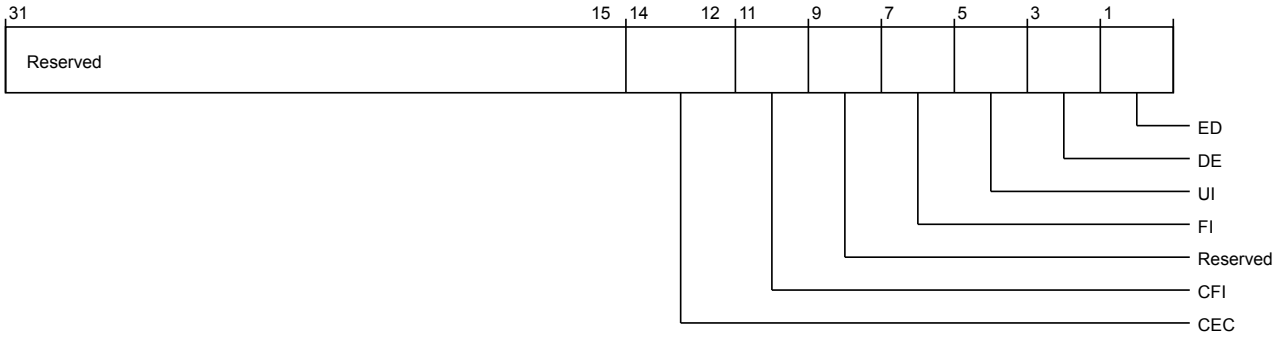


Figure 3-697 por_mxp_por_mxp_errfr (low)

The following table shows the por_mxp_errfr lower register bit assignments.

Table 3-711 por_mxp_por_mxp_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_mxp_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

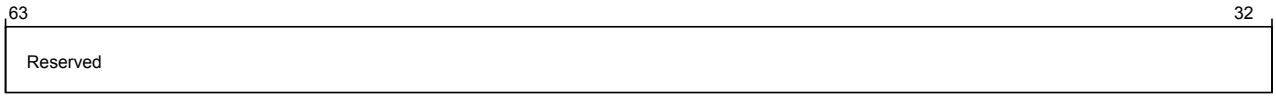


Figure 3-698 por_mxp_por_mxp_errctlr (high)

The following table shows the por_mxp_errctlr higher register bit assignments.

Table 3-712 por_mxp_por_mxp_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

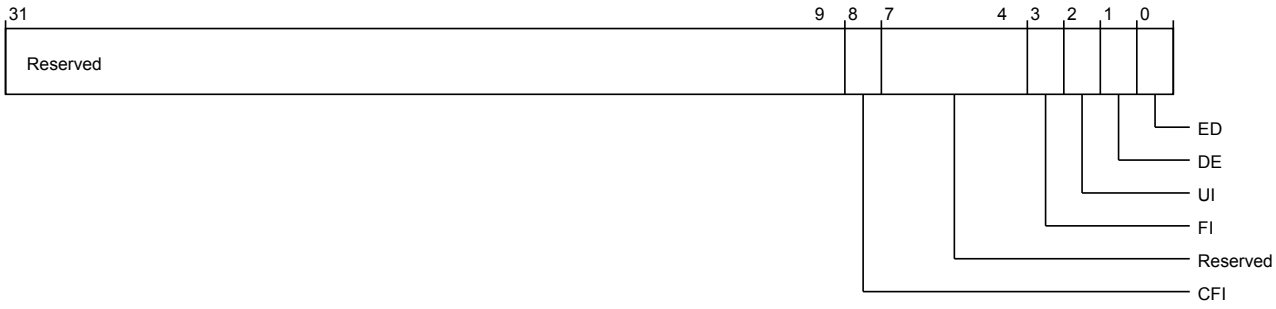


Figure 3-699 por_mxp_por_mxp_errctlr (low)

The following table shows the por_mxp_errctlr lower register bit assignments.

Table 3-713 por_mxp_por_mxp_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mxp_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mxp_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mxp_errfr.ED	RW	1'b0

por_mxp_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

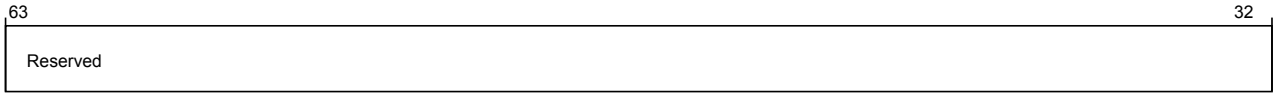


Figure 3-700 por_mxp_por_mxp_errstatus (high)

The following table shows the por_mxp_errstatus higher register bit assignments.

Table 3-714 por_mxp_por_mxp_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-701 por_mxp_por_mxp_errstatus (low)

The following table shows the por_mxp_errstatus lower register bit assignments.

Table 3-715 por_mxp_por_mxp_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mxp_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_mxp_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3028
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

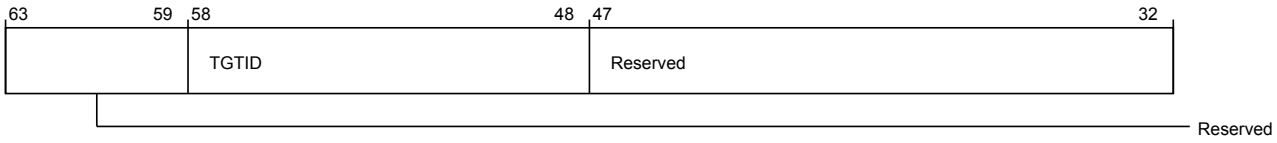


Figure 3-702 por_mxp_por_mxp_errmisc (high)

The following table shows the por_mxp_errmisc higher register bit assignments.

Table 3-716 por_mxp_por_mxp_errmisc (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

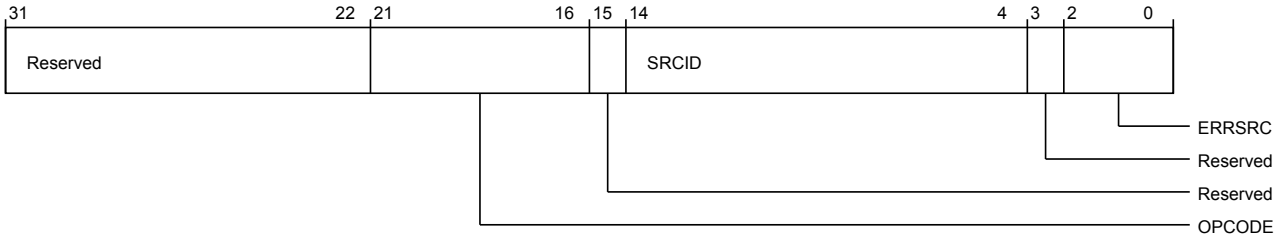


Figure 3-703 por_mxp_por_mxp_errmisc (low)

The following table shows the por_mxp_errmisc lower register bit assignments.

Table 3-717 por_mxp_por_mxp_errmisc (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error flit opcode	RW	6'b0
15	Reserved	Reserved	RO	-

Table 3-717 por_mxp_por_mxp_errmisc (low) (continued)

Bits	Field name	Description	Type	Reset
14:4	SRCID	Error flit source ID	RW	11'b0
3	Reserved	Reserved	RO	-
2:0	ERRSRC	Error source Bits [2:1]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bit [0]: Port 1'b0: Port 0 1'b1: Port 1	RW	3'b0

por_mxp_p0_byte_par_err_inj

Functions as the byte parity error injection register for XP port 0.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h3030
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

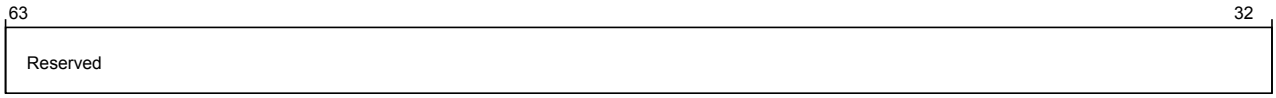


Figure 3-704 por_mxp_por_mxp_p0_byte_par_err_inj (high)

The following table shows the por_mxp_p0_byte_par_err_inj higher register bit assignments.

Table 3-718 por_mxp_por_mxp_p0_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

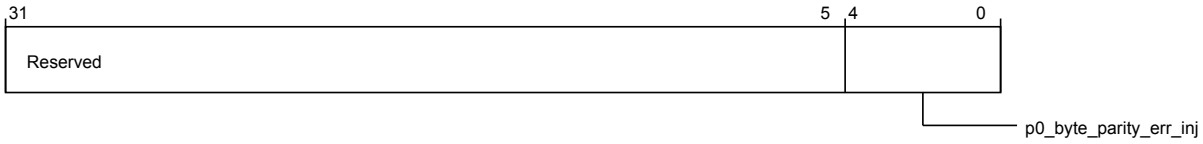


Figure 3-705 por_mxp_por_mxp_p0_byte_par_err_inj (low)

The following table shows the por_mxp_p0_byte_par_err_inj lower register bit assignments.

Table 3-719 por_mxp_por_mxp_p0_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	p0_byte_parity_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port 0. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

por_mxp_p1_byte_par_err_inj

Functions as the byte parity error injection register for XP port 1.

Its characteristics are:

Type WO
Register width (Bits) 64
Address offset 14'h3038
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

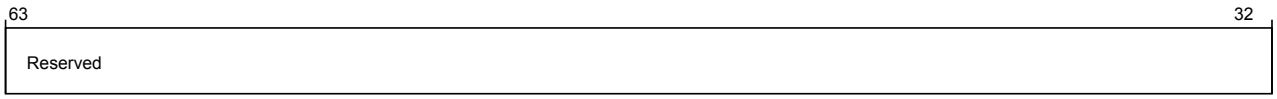


Figure 3-706 por_mxp_por_mxp_p1_byte_par_err_inj (high)

The following table shows the por_mxp_p1_byte_par_err_inj higher register bit assignments.

Table 3-720 por_mxp_por_mxp_p1_byte_par_err_inj (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

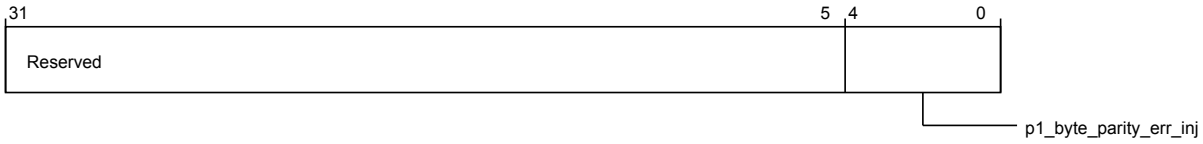


Figure 3-707 por_mxp_por_mxp_p1_byte_par_err_inj (low)

The following table shows the por_mxp_p1_byte_par_err_inj lower register bit assignments.

Table 3-721 por_mxp_por_mxp_p1_byte_par_err_inj (low)

Bits	Field name	Description	Type	Reset
31:5	Reserved	Reserved	RO	-
4:0	p1_byte_parity_err_inj	Specifies a byte lane; once this register is written, a byte parity error is injected in the specified byte lane on the next DAT flit upload NOTE: Only applicable if an RN-F is attached to port 0. Byte parity error is only injected if the RN-F is configured to not support Datacheck.	WO	5'h00

por_mxp_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b0000010100101
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

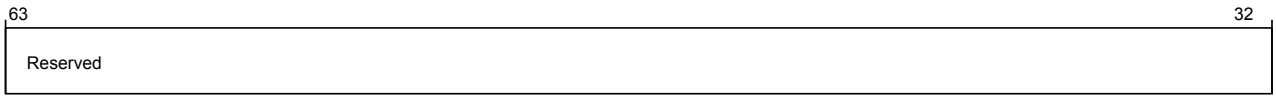


Figure 3-708 por_mxp_por_mxp_errfr_ns (high)

The following table shows the por_mxp_errfr_NS higher register bit assignments.

Table 3-722 por_mxp_por_mxp_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

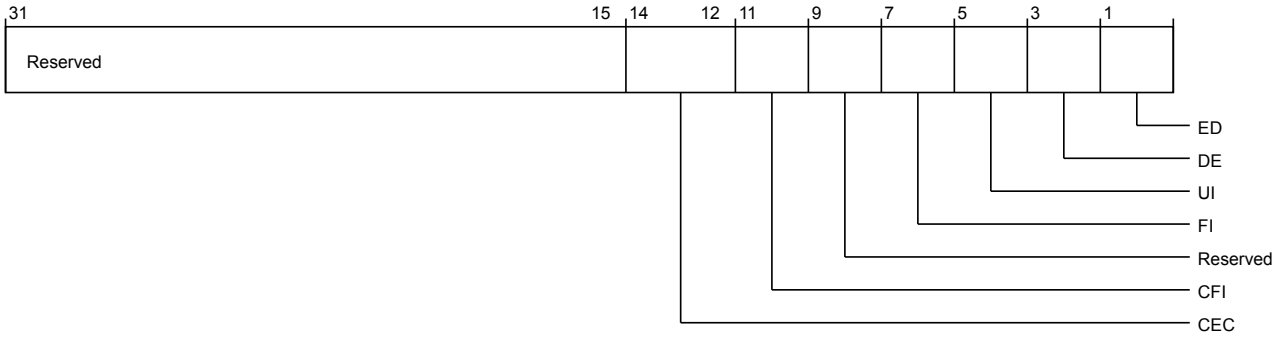


Figure 3-709 por_mxp_por_mxp_errfr_ns (low)

The following table shows the por_mxp_errfr_NS lower register bit assignments.

Table 3-723 por_mxp_por_mxp_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_mxp_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

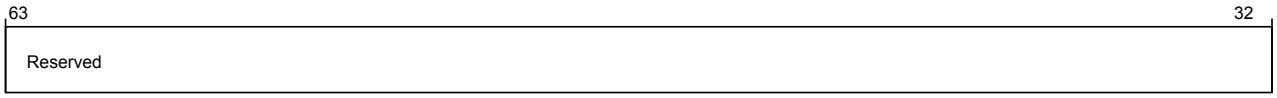


Figure 3-710 por_mxp_por_mxp_errctlr_ns (high)

The following table shows the por_mxp_errctlr_NS higher register bit assignments.

Table 3-724 por_mxp_por_mxp_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

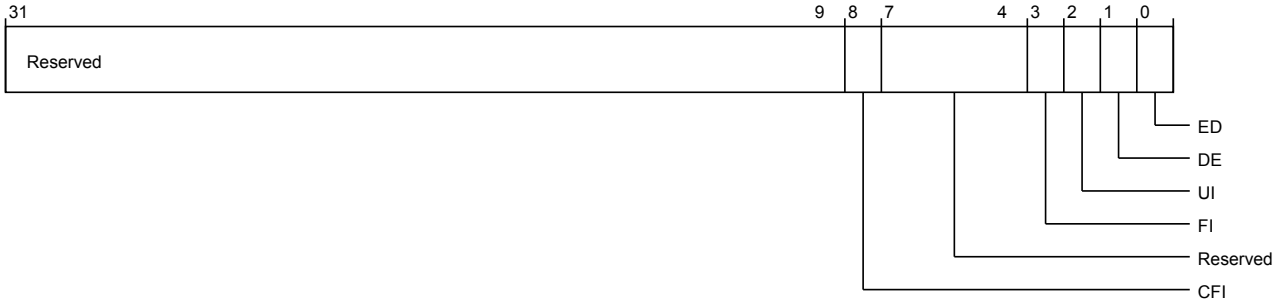


Figure 3-711 por_mxp_por_mxp_errctlr_ns (low)

The following table shows the por_mxp_errctlr_NS lower register bit assignments.

Table 3-725 por_mxp_por_mxp_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_mxp_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_mxp_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_mxp_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_mxp_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_mxp_errfr_NS.ED	RW	1'b0

por_mxp_errstatus_NS

Functions as the non-secure error status register.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3110

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

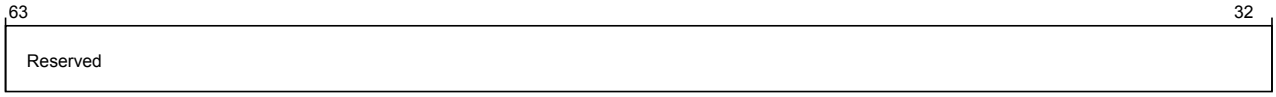


Figure 3-712 por_mxp_por_mxp_errstatus_ns (high)

The following table shows the por_mxp_errstatus_NS higher register bit assignments.

Table 3-726 por_mxp_por_mxp_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-713 por_mxp_por_mxp_errstatus_ns (low)

The following table shows the por_mxp_errstatus_NS lower register bit assignments.

Table 3-727 por_mxp_por_mxp_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_mxp_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_mxp_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

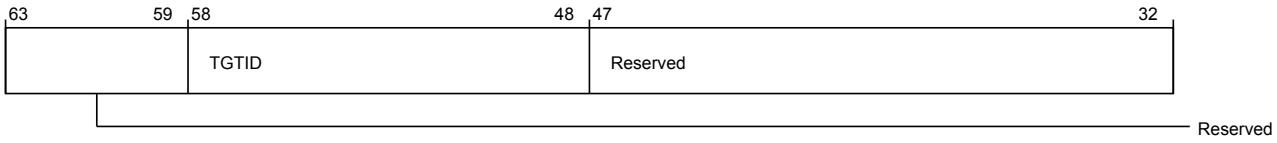


Figure 3-714 por_mxp_por_mxp_errmisc_ns (high)

The following table shows the por_mxp_errmisc_NS higher register bit assignments.

Table 3-728 por_mxp_por_mxp_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:59	Reserved	Reserved	RO	-
58:48	TGTID	Error flit target ID	RW	11'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

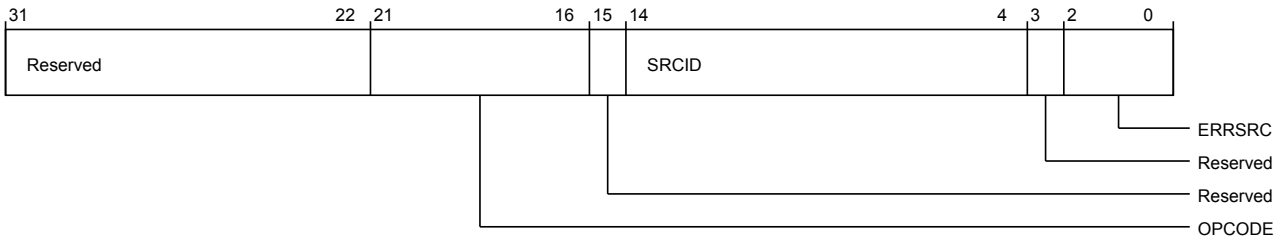


Figure 3-715 por_mxp_por_mxp_errmisc_ns (low)

The following table shows the por_mxp_errmisc_NS lower register bit assignments.

Table 3-729 por_mxp_por_mxp_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	OPCODE	Error flit opcode	RW	6'b0
15	Reserved	Reserved	RO	-

Table 3-729 por_mxp_por_mxp_errmisc_ns (low) (continued)

Bits	Field name	Description	Type	Reset
14:4	SRCID	Error flit source ID	RW	11'b0
3	Reserved	Reserved	RO	-
2:0	ERRSRC	Error source Bits [2:1]: Transaction type 2'b00: REQ 2'b01: RSP 2'b10: SNP 2'b11: DAT Bit [0]: Port 1'b0: Port 0 1'b1: Port 1	RW	3'b0

por_mxp_p0_syscoreq_ctl

Functions as the port 0 snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p0_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

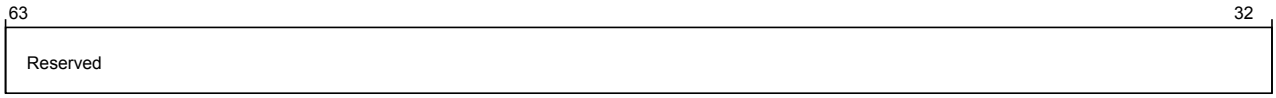


Figure 3-716 por_mxp_por_mxp_p0_syscoreq_ctl (high)

The following table shows the por_mxp_p0_syscoreq_ctl higher register bit assignments.

Table 3-730 por_mxp_por_mxp_p0_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

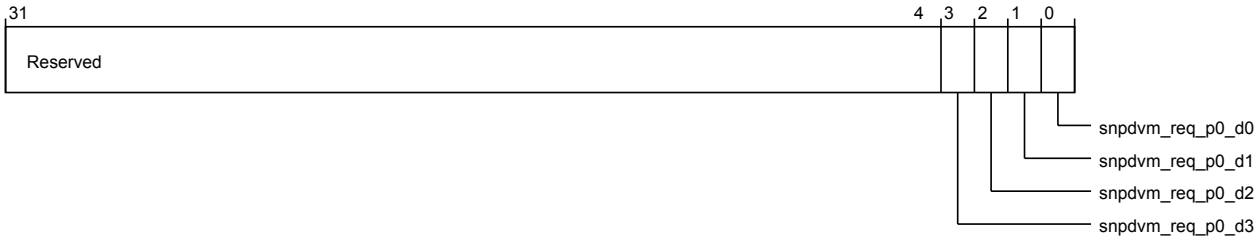


Figure 3-717 por_mxp_por_mxp_p0_syscoreq_ctl (low)

The following table shows the por_mxp_p0_syscoreq_ctl lower register bit assignments.

Table 3-731 por_mxp_por_mxp_p0_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p0_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port 0	RW	1'b0
2	snpdvm_req_p0_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port 0	RW	1'b0
1	snpdvm_req_p0_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port 0	RW	1'b0
0	snpdvm_req_p0_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port 0	RW	1'b0

por_mxp_p1_syscoreq_ctl

Functions as the port 1 snoop and DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p1_syscoack_status. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1008

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

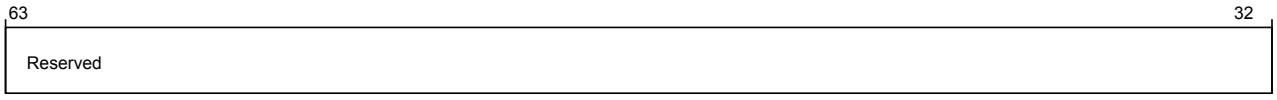


Figure 3-718 por_mxp_por_mxp_p1_syscoreq_ctl (high)

The following table shows the por_mxp_p1_syscoreq_ctl higher register bit assignments.

Table 3-732 por_mxp_por_mxp_p1_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

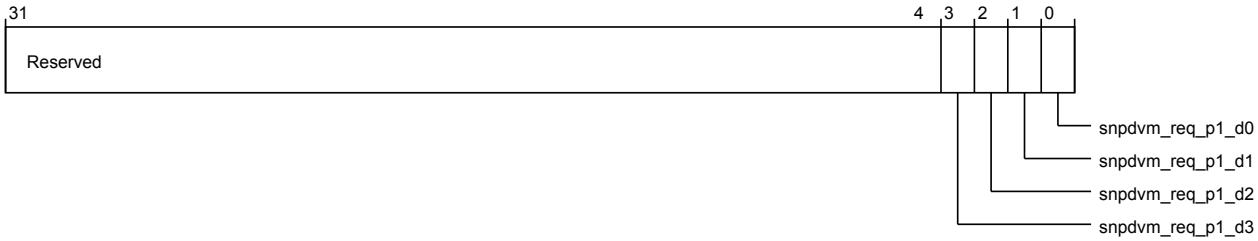


Figure 3-719 por_mxp_por_mxp_p1_syscoreq_ctl (low)

The following table shows the por_mxp_p1_syscoreq_ctl lower register bit assignments.

Table 3-733 por_mxp_por_mxp_p1_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_req_p1_d3	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 3 on port 1	RW	1'b0
2	snpdvm_req_p1_d2	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 2 on port 1	RW	1'b0
1	snpdvm_req_p1_d1	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 1 on port 1	RW	1'b0
0	snpdvm_req_p1_d0	When set, initiates the process of enabling snoop and DVM dispatches (SYSCOREQ) to device 0 on port 1	RW	1'b0

por_mxp_p0_syscoack_status

Functions as the port 0 snoop and DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p0_syscoreq_ctl. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

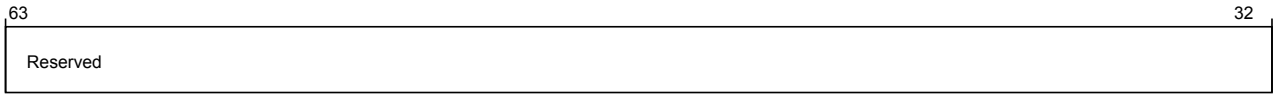


Figure 3-720 por_mxp_por_mxp_p0_syscoack_status (high)

The following table shows the por_mxp_p0_syscoack_status higher register bit assignments.

Table 3-734 por_mxp_por_mxp_p0_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

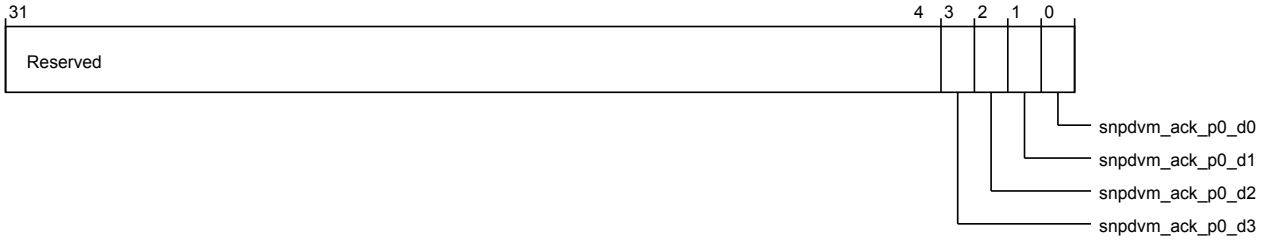


Figure 3-721 por_mxp_por_mxp_p0_syscoack_status (low)

The following table shows the por_mxp_p0_syscoack_status lower register bit assignments.

Table 3-735 por_mxp_por_mxp_p0_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_ack_p0_d3	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port 0	RO	1'b0
2	snpdvm_ack_p0_d2	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port 0	RO	1'b0
1	snpdvm_ack_p0_d1	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port 0	RO	1'b0
0	snpdvm_ack_p0_d0	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port 0	RO	1'b0

por_mxp_p1_syscoack_status

Functions as the port 1 snoop and DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_mxp_p1_syscoreq_ctl. NOTE: Only valid on RN-F ports.

Its characteristics are:

Type RO

Register width (Bits) 64
Address offset 14'h1018
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

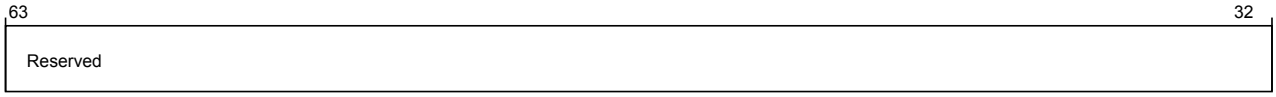


Figure 3-722 por_mxp_por_mxp_p1_syscoack_status (high)

The following table shows the por_mxp_p1_syscoack_status higher register bit assignments.

Table 3-736 por_mxp_por_mxp_p1_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

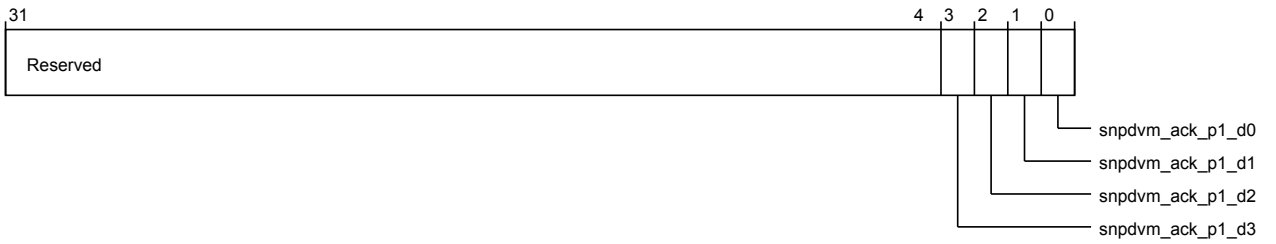


Figure 3-723 por_mxp_por_mxp_p1_syscoack_status (low)

The following table shows the por_mxp_p1_syscoack_status lower register bit assignments.

Table 3-737 por_mxp_por_mxp_p1_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	snpdvm_ack_p1_d3	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 3 on port 1	RO	1'b0
2	snpdvm_ack_p1_d2	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 2 on port 1	RO	1'b0
1	snpdvm_ack_p1_d1	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 1 on port 1	RO	1'b0
0	snpdvm_ack_p1_d0	When set, indicates snoop and DVM dispatches are enabled (SYSCOACK) for device 0 on port 1	RO	1'b0

por_dtm_control

Functions as the DTM control register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2100
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

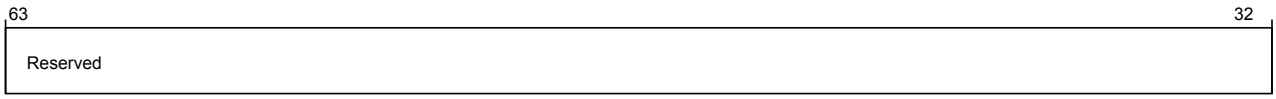


Figure 3-724 por_mxp_por_dtm_control (high)

The following table shows the por_dtm_control higher register bit assignments.

Table 3-738 por_mxp_por_dtm_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

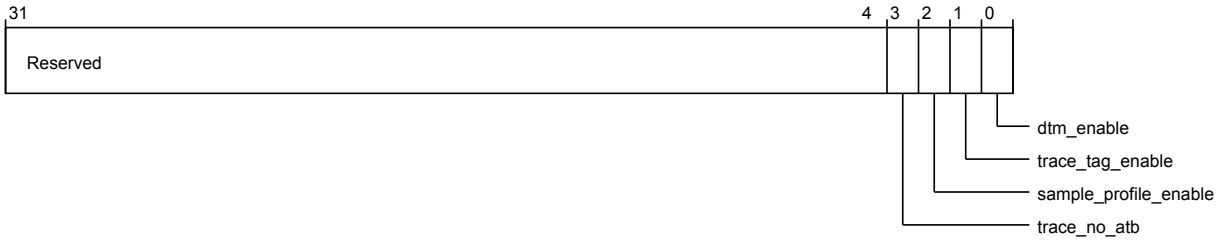


Figure 3-725 por_mxp_por_dtm_control (low)

The following table shows the por_dtm_control lower register bit assignments.

Table 3-739 por_mxp_por_dtm_control (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	trace_no_atb	When set, trace packet is not delivered out of ATB, and FIFO entry holds the first trace packet	RW	1'b0
2	sample_profile_enable	Enables sample profile function	RW	1'b0

Table 3-739 por_mxp_por_dtm_control (low) (continued)

Bits	Field name	Description	Type	Reset
1	trace_tag_enable	Watchpoint trace tag enable 1'b1: Trace tag enabled 1'b0: No trace tag	RW	1'b0
0	dtm_enable	Enables debug watchpoint and PMU function; prior to writing this bit, all other DT configuration registers must be programmed; once this bit is set, other DT configuration registers must not be modified	RW	1'b0

por_dtm_fifo_entry_ready

Controls status of DTM FIFO entries.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h2118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

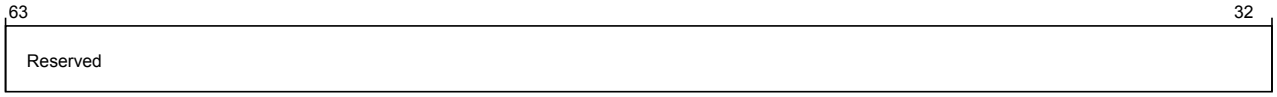


Figure 3-726 por_mxp_por_dtm_fifo_entry_ready (high)

The following table shows the por_dtm_fifo_entry_ready higher register bit assignments.

Table 3-740 por_mxp_por_dtm_fifo_entry_ready (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

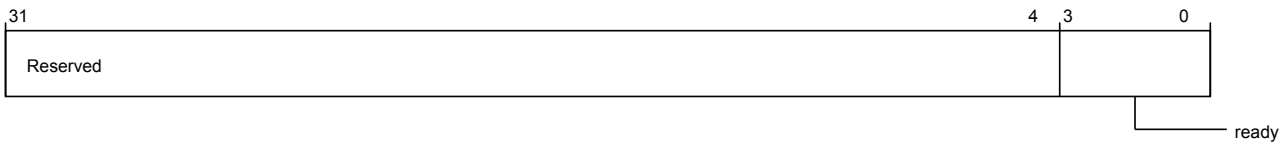


Figure 3-727 por_mxp_por_dtm_fifo_entry_ready (low)

The following table shows the por_dtm_fifo_entry_ready lower register bit assignments.

Table 3-741 por_mxp_por_dtm_fifo_entry_ready (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3:0	ready	Indicates which DTM FIFO entries are ready; write a 1 to clear Bit [3]: Entry 3 ready when set Bit [2]: Entry 2 ready when set Bit [1]: Entry 1 ready when set Bit [0]: Entry 0 ready when set	W1C	4'b0

por_dtm_fifo_entry0_0

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

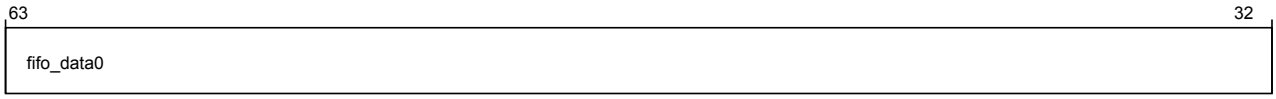


Figure 3-728 por_mxp_por_dtm_fifo_entry0_0 (high)

The following table shows the por_dtm_fifo_entry0_0 higher register bit assignments.

Table 3-742 por_mxp_por_dtm_fifo_entry0_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

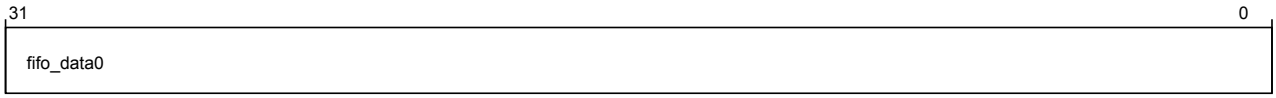


Figure 3-729 por_mxp_por_dtm_fifo_entry0_0 (low)

The following table shows the por_dtm_fifo_entry0_0 lower register bit assignments.

Table 3-743 por_mxp_por_dtm_fifo_entry0_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry0_1

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2128
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

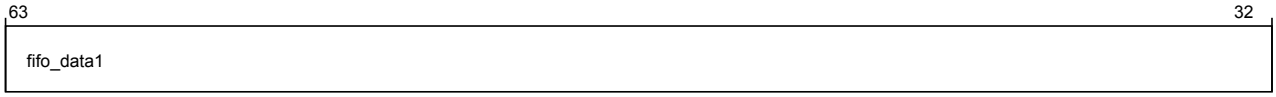


Figure 3-730 por_mxp_por_dtm_fifo_entry0_1 (high)

The following table shows the por_dtm_fifo_entry0_1 higher register bit assignments.

Table 3-744 por_mxp_por_dtm_fifo_entry0_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

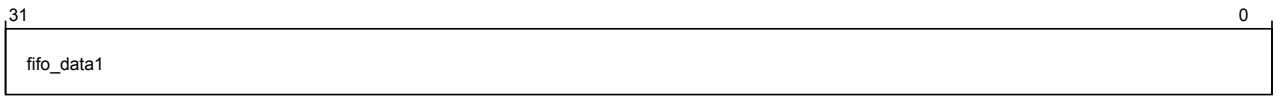


Figure 3-731 por_mxp_por_dtm_fifo_entry0_1 (low)

The following table shows the por_dtm_fifo_entry0_1 lower register bit assignments.

Table 3-745 por_mxp_por_dtm_fifo_entry0_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry0_2

Contains DTM FIFO entry 0 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2130
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

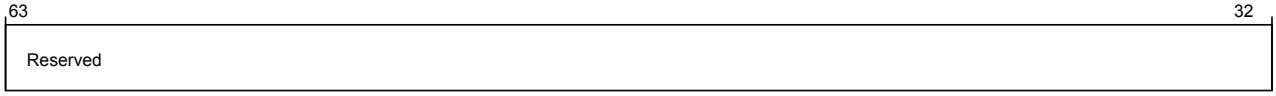


Figure 3-732 por_mxp_por_dtm_fifo_entry0_2 (high)

The following table shows the por_dtm_fifo_entry0_2 higher register bit assignments.

Table 3-746 por_mxp_por_dtm_fifo_entry0_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

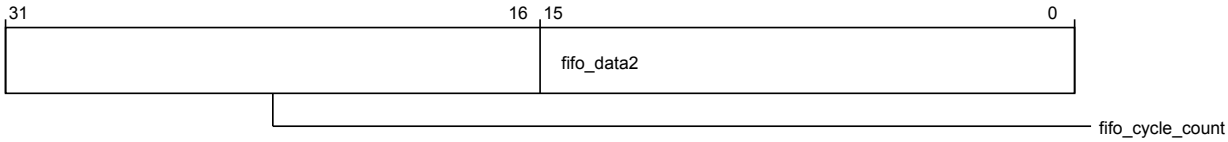


Figure 3-733 por_mxp_por_dtm_fifo_entry0_2 (low)

The following table shows the por_dtm_fifo_entry0_2 lower register bit assignments.

Table 3-747 por_mxp_por_dtm_fifo_entry0_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry1_0

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2138
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

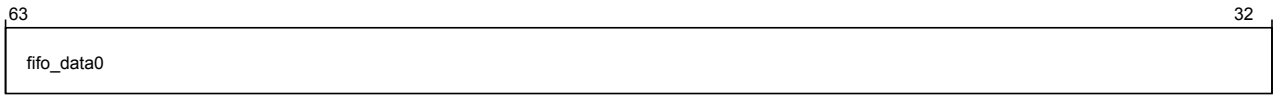


Figure 3-734 por_mxp_por_dtm_fifo_entry1_0 (high)

The following table shows the por_dtm_fifo_entry1_0 higher register bit assignments.

Table 3-748 por_mxp_por_dtm_fifo_entry1_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

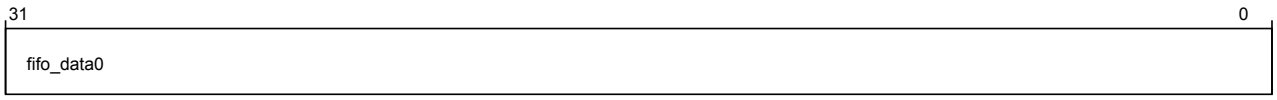


Figure 3-735 por_mxp_por_dtm_fifo_entry1_0 (low)

The following table shows the por_dtm_fifo_entry1_0 lower register bit assignments.

Table 3-749 por_mxp_por_dtm_fifo_entry1_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry1_1

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2140
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

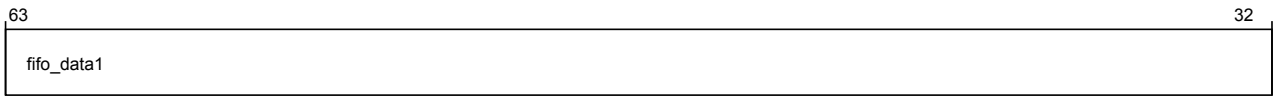


Figure 3-736 por_mxp_por_dtm_fifo_entry1_1 (high)

The following table shows the por_dtm_fifo_entry1_1 higher register bit assignments.

Table 3-750 por_mxp_por_dtm_fifo_entry1_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

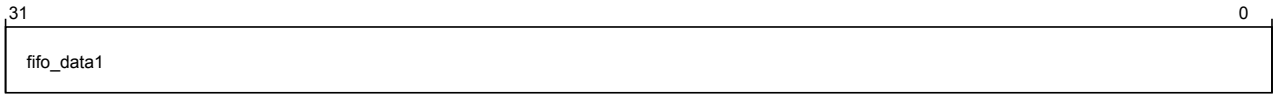


Figure 3-737 por_mxp_por_dtm_fifo_entry1_1 (low)

The following table shows the por_dtm_fifo_entry1_1 lower register bit assignments.

Table 3-751 por_mxp_por_dtm_fifo_entry1_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry1_2

Contains DTM FIFO entry 1 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2148
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

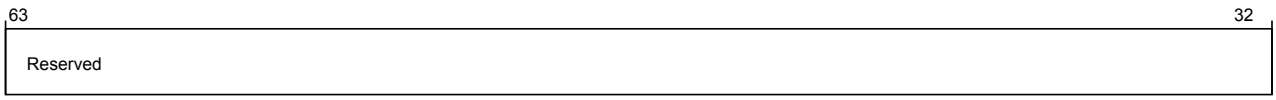


Figure 3-738 por_mxp_por_dtm_fifo_entry1_2 (high)

The following table shows the por_dtm_fifo_entry1_2 higher register bit assignments.

Table 3-752 por_mxp_por_dtm_fifo_entry1_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

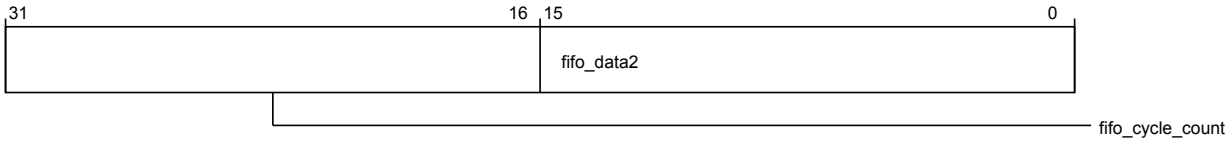


Figure 3-739 por_mxp_por_dtm_fifo_entry1_2 (low)

The following table shows the por_dtm_fifo_entry1_2 lower register bit assignments.

Table 3-753 por_mxp_por_dtm_fifo_entry1_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry2_0

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h2150

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

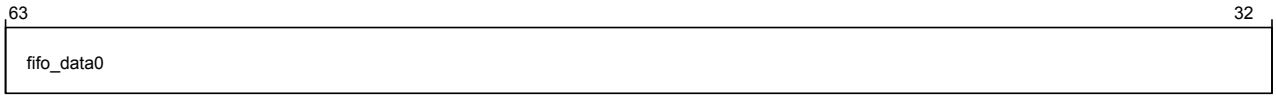


Figure 3-740 por_mxp_por_dtm_fifo_entry2_0 (high)

The following table shows the por_dtm_fifo_entry2_0 higher register bit assignments.

Table 3-754 por_mxp_por_dtm_fifo_entry2_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

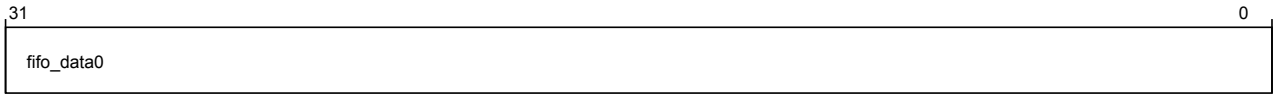


Figure 3-741 por_mxp_por_dtm_fifo_entry2_0 (low)

The following table shows the por_dtm_fifo_entry2_0 lower register bit assignments.

Table 3-755 por_mxp_por_dtm_fifo_entry2_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry2_1

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2158
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

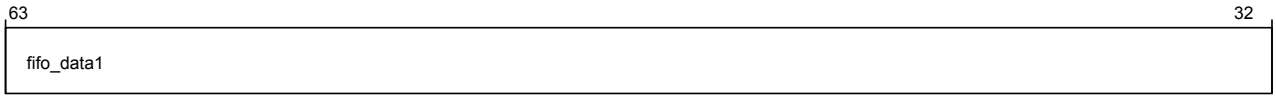


Figure 3-742 por_mxp_por_dtm_fifo_entry2_1 (high)

The following table shows the por_dtm_fifo_entry2_1 higher register bit assignments.

Table 3-756 por_mxp_por_dtm_fifo_entry2_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

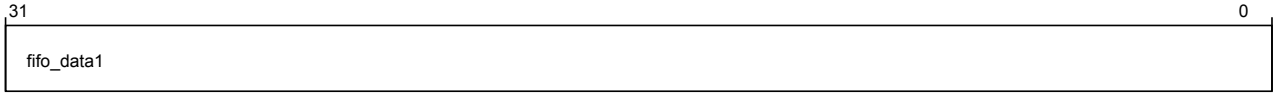


Figure 3-743 por_mxp_por_dtm_fifo_entry2_1 (low)

The following table shows the por_dtm_fifo_entry2_1 lower register bit assignments.

Table 3-757 por_mxp_por_dtm_fifo_entry2_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry2_2

Contains DTM FIFO entry 2 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2160
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

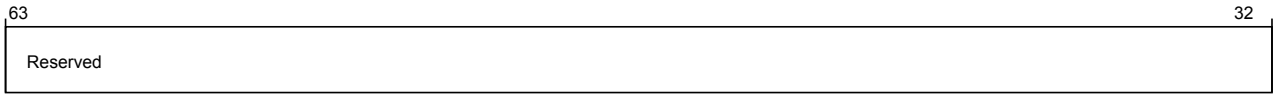


Figure 3-744 por_mxp_por_dtm_fifo_entry2_2 (high)

The following table shows the por_dtm_fifo_entry2_2 higher register bit assignments.

Table 3-758 por_mxp_por_dtm_fifo_entry2_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

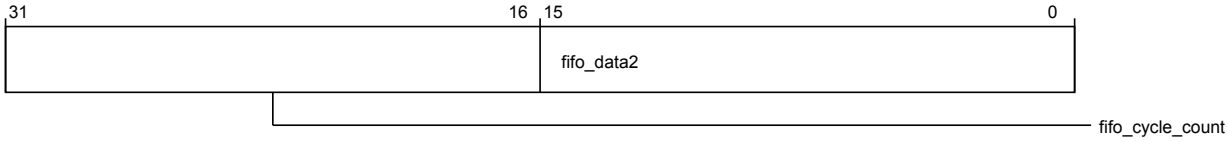


Figure 3-745 por_mxp_por_dtm_fifo_entry2_2 (low)

The following table shows the por_dtm_fifo_entry2_2 lower register bit assignments.

Table 3-759 por_mxp_por_dtm_fifo_entry2_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_fifo_entry3_0

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2168
Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

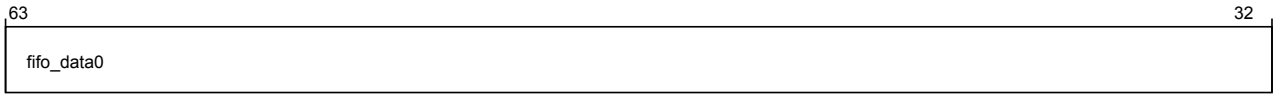


Figure 3-746 por_mxp_por_dtm_fifo_entry3_0 (high)

The following table shows the por_dtm_fifo_entry3_0 higher register bit assignments.

Table 3-760 por_mxp_por_dtm_fifo_entry3_0 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data0	Entry data bit vector 63:0	RO	64'b0

The following image shows the lower register bit assignments.

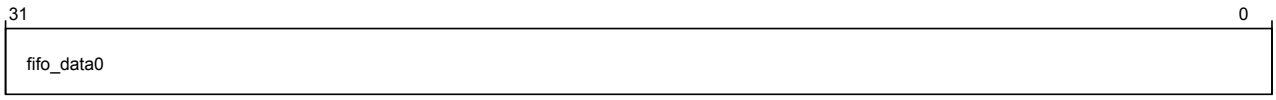


Figure 3-747 por_mxp_por_dtm_fifo_entry3_0 (low)

The following table shows the por_dtm_fifo_entry3_0 lower register bit assignments.

Table 3-761 por_mxp_por_dtm_fifo_entry3_0 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data0	Entry data bit vector 63:0	RO	64'b0

por_dtm_fifo_entry3_1

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2170
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

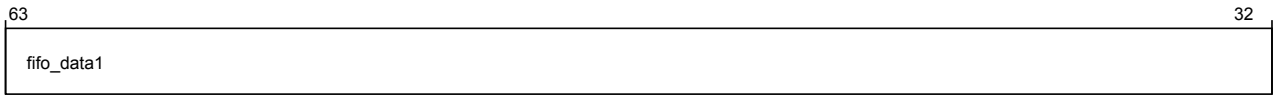


Figure 3-748 por_mxp_por_dtm_fifo_entry3_1 (high)

The following table shows the por_dtm_fifo_entry3_1 higher register bit assignments.

Table 3-762 por_mxp_por_dtm_fifo_entry3_1 (high)

Bits	Field name	Description	Type	Reset
63:32	fifo_data1	Entry data bit vector 127:64	RO	64'b0

The following image shows the lower register bit assignments.

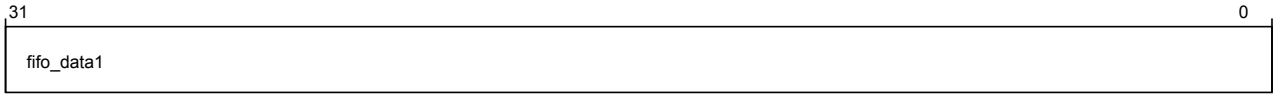


Figure 3-749 por_mxp_por_dtm_fifo_entry3_1 (low)

The following table shows the por_dtm_fifo_entry3_1 lower register bit assignments.

Table 3-763 por_mxp_por_dtm_fifo_entry3_1 (low)

Bits	Field name	Description	Type	Reset
31:0	fifo_data1	Entry data bit vector 127:64	RO	64'b0

por_dtm_fifo_entry3_2

Contains DTM FIFO entry 3 data.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h2178
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

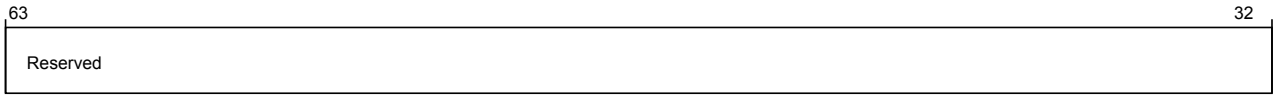


Figure 3-750 por_mxp_por_dtm_fifo_entry3_2 (high)

The following table shows the por_dtm_fifo_entry3_2 higher register bit assignments.

Table 3-764 por_mxp_por_dtm_fifo_entry3_2 (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

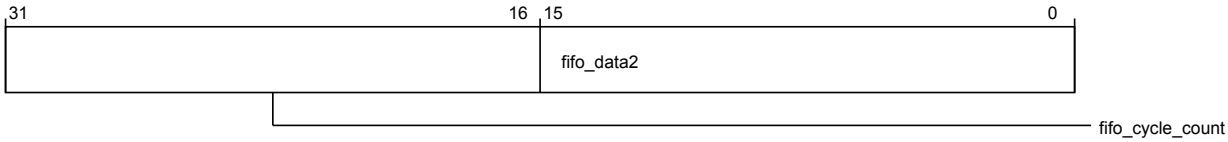


Figure 3-751 por_mxp_por_dtm_fifo_entry3_2 (low)

The following table shows the por_dtm_fifo_entry3_2 lower register bit assignments.

Table 3-765 por_mxp_por_dtm_fifo_entry3_2 (low)

Bits	Field name	Description	Type	Reset
31:16	fifo_cycle_count	Entry cycle count bit vector 15:0	RO	16'b0
15:0	fifo_data2	Entry data bit vector 143:128	RO	16'b0

por_dtm_wp0_config

Configures watchpoint 0.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21A0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

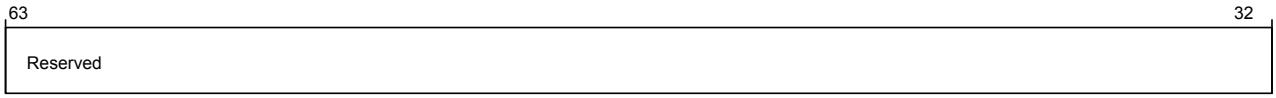


Figure 3-752 por_mxp_por_dtm_wp0_config (high)

The following table shows the por_dtm_wp0_config higher register bit assignments.

Table 3-766 por_mxp_por_dtm_wp0_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

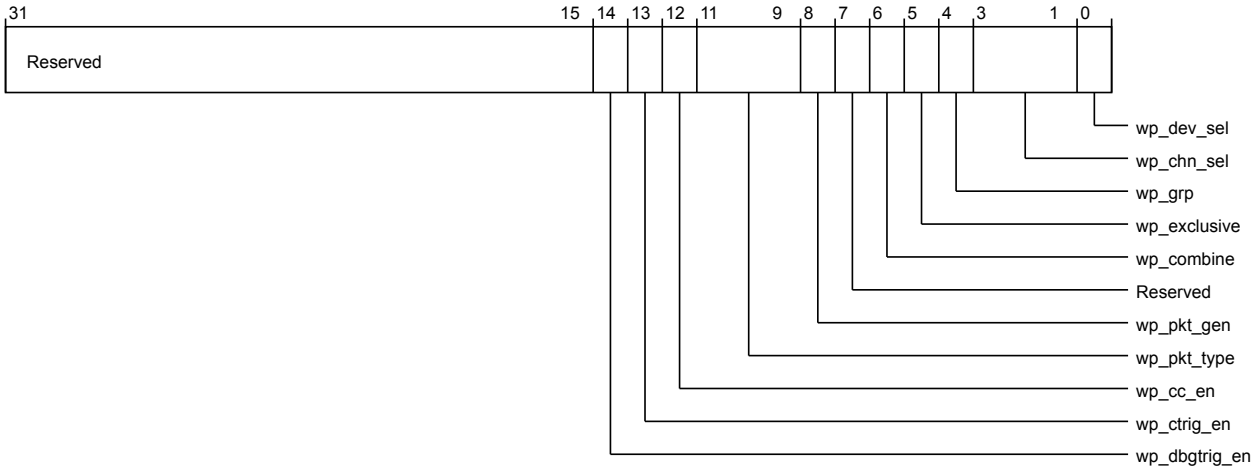


Figure 3-753 por_mxp_por_dtm_wp0_config (low)

The following table shows the por_dtm_wp0_config lower register bit assignments.

Table 3-767 por_mxp_por_dtm_wp0_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7	Reserved	Reserved	RO	-
6	wp_combine	Enables combination of watchpoints 0 and 1	RW	1'b0
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0

Table 3-767 por_mxp_por_dtm_wp0_config (low) (continued)

Bits	Field name	Description	Type	Reset
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp0_val

Configures watchpoint 0 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21A8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

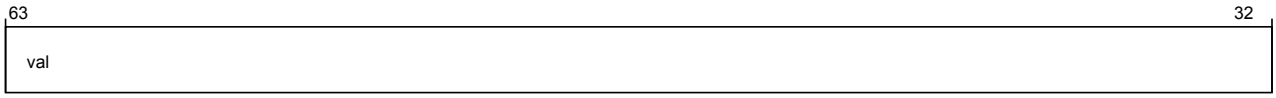


Figure 3-754 por_mxp_por_dtm_wp0_val (high)

The following table shows the por_dtm_wp0_val higher register bit assignments.

Table 3-768 por_mxp_por_dtm_wp0_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

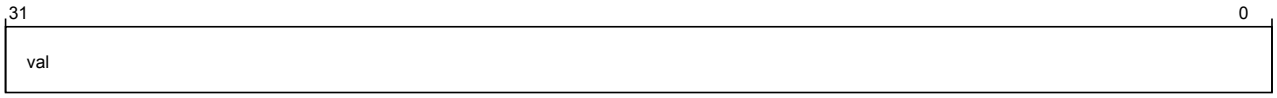


Figure 3-755 por_mxp_por_dtm_wp0_val (low)

The following table shows the por_dtm_wp0_val lower register bit assignments.

Table 3-769 por_mxp_por_dtm_wp0_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp0_mask

Configures watchpoint0 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21B0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

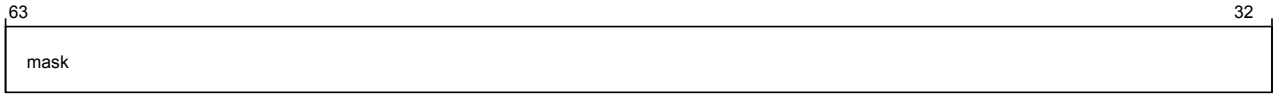


Figure 3-756 por_mxp_por_dtm_wp0_mask (high)

The following table shows the por_dtm_wp0_mask higher register bit assignments.

Table 3-770 por_mxp_por_dtm_wp0_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

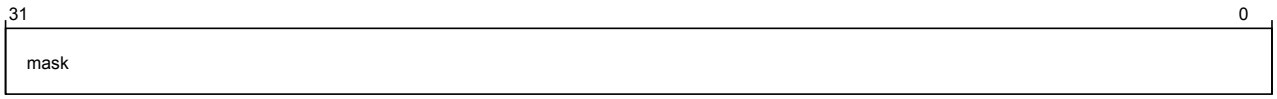


Figure 3-757 por_mxp_por_dtm_wp0_mask (low)

The following table shows the por_dtm_wp0_mask lower register bit assignments.

Table 3-771 por_mxp_por_dtm_wp0_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp1_config

Configures watchpoint 1.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21B8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

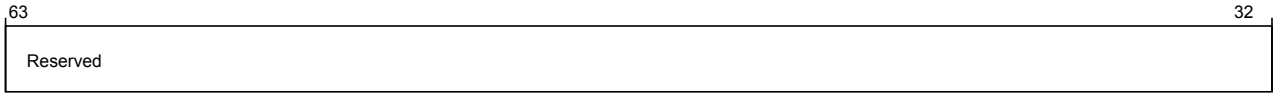


Figure 3-758 por_mxp_por_dtm_wp1_config (high)

The following table shows the por_dtm_wp1_config higher register bit assignments.

Table 3-772 por_mxp_por_dtm_wp1_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

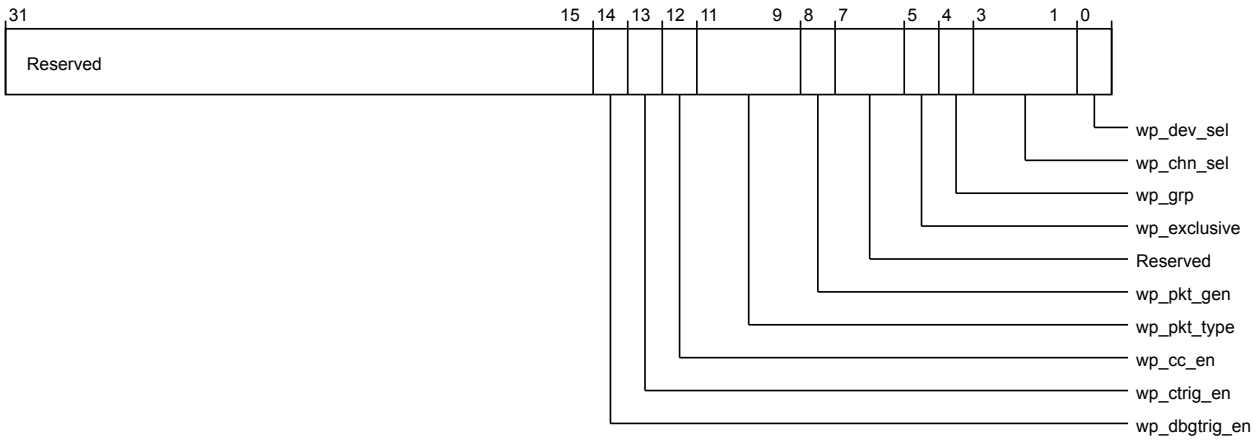


Figure 3-759 por_mxp_por_dtm_wp1_config (low)

The following table shows the por_dtm_wp1_config lower register bit assignments.

Table 3-773 por_mxp_por_dtm_wp1_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7:6	Reserved	Reserved	RO	-
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp1_val

Configures watchpoint 1 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21C0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

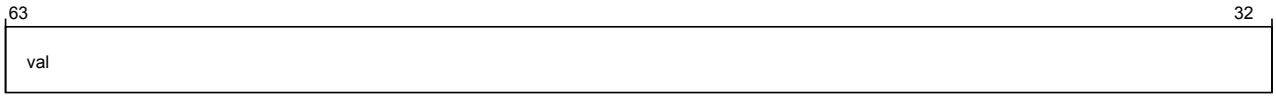


Figure 3-760 por_mxp_por_dtm_wp1_val (high)

The following table shows the por_dtm_wp1_val higher register bit assignments.

Table 3-774 por_mxp_por_dtm_wp1_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

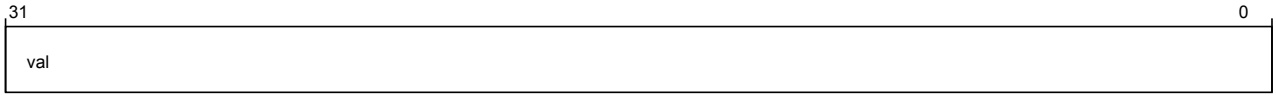


Figure 3-761 por_mxp_por_dtm_wp1_val (low)

The following table shows the por_dtm_wp1_val lower register bit assignments.

Table 3-775 por_mxp_por_dtm_wp1_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp1_mask

Configures watchpoint 1 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21C8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

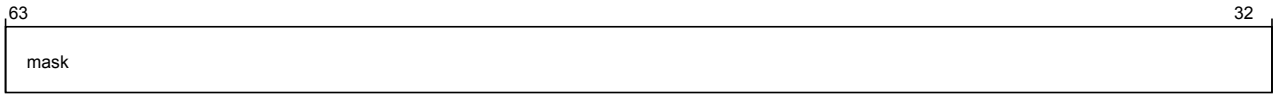


Figure 3-762 por_mxp_por_dtm_wp1_mask (high)

The following table shows the por_dtm_wp1_mask higher register bit assignments.

Table 3-776 por_mxp_por_dtm_wp1_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

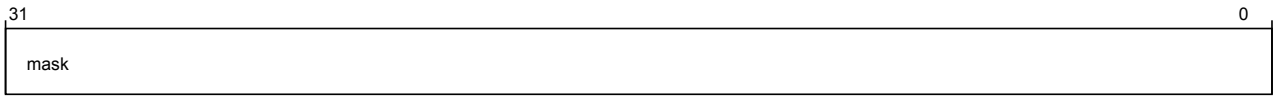


Figure 3-763 por_mxp_por_dtm_wp1_mask (low)

The following table shows the por_dtm_wp1_mask lower register bit assignments.

Table 3-777 por_mxp_por_dtm_wp1_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp2_config

Configures watchpoint 2.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21D0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

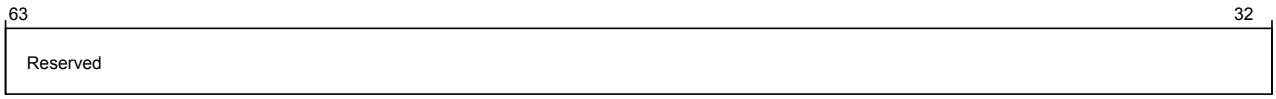


Figure 3-764 por_mxp_por_dtm_wp2_config (high)

The following table shows the por_dtm_wp2_config higher register bit assignments.

Table 3-778 por_mxp_por_dtm_wp2_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

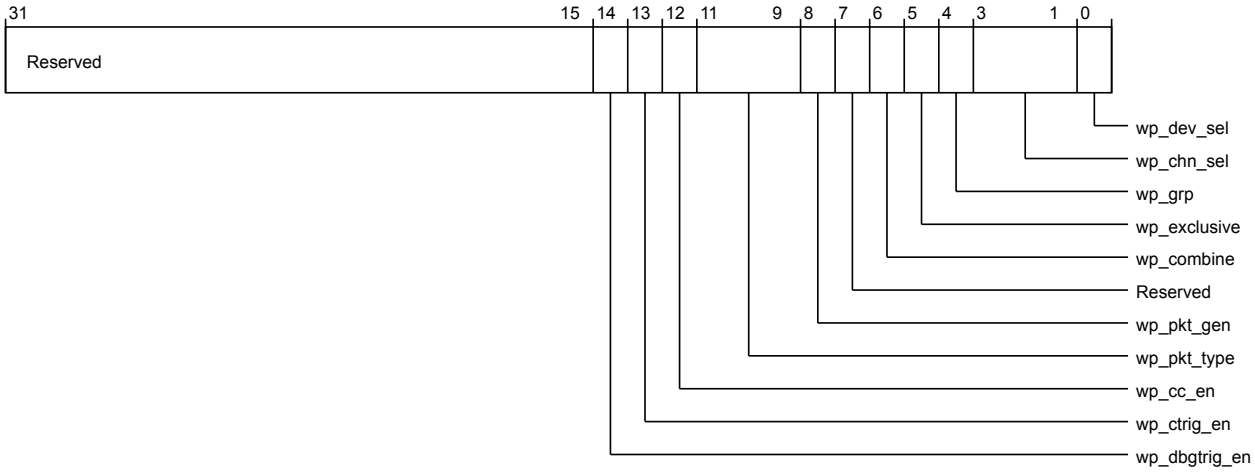


Figure 3-765 por_mxp_por_dtm_wp2_config (low)

The following table shows the por_dtm_wp2_config lower register bit assignments.

Table 3-779 por_mxp_por_dtm_wp2_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7	Reserved	Reserved	RO	-

Table 3-779 por_mxp_por_dtm_wp2_config (low) (continued)

Bits	Field name	Description	Type	Reset
6	wp_combine	Enables combination of watchpoints 2 and 3	RW	1'b0
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp2_val

Configures watchpoint 2 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21D8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

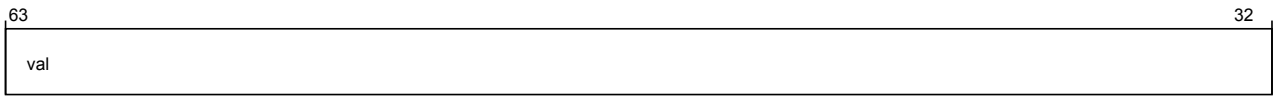


Figure 3-766 por_mxp_por_dtm_wp2_val (high)

The following table shows the por_dtm_wp2_val higher register bit assignments.

Table 3-780 por_mxp_por_dtm_wp2_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

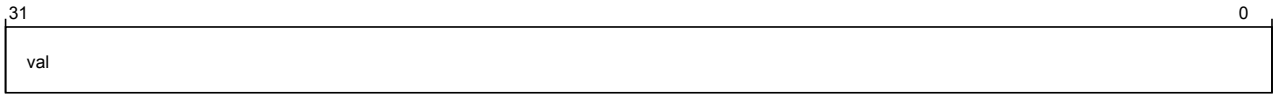


Figure 3-767 por_mxp_por_dtm_wp2_val (low)

The following table shows the por_dtm_wp2_val lower register bit assignments.

Table 3-781 por_mxp_por_dtm_wp2_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp2_mask

Configures watchpoint 2 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21E0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

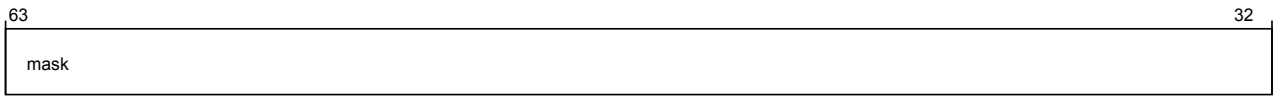


Figure 3-768 por_mxp_por_dtm_wp2_mask (high)

The following table shows the por_dtm_wp2_mask higher register bit assignments.

Table 3-782 por_mxp_por_dtm_wp2_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

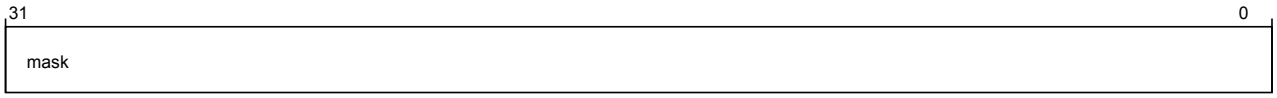


Figure 3-769 por_mxp_por_dtm_wp2_mask (low)

The following table shows the por_dtm_wp2_mask lower register bit assignments.

Table 3-783 por_mxp_por_dtm_wp2_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp3_config

Configures watchpoint 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21E8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

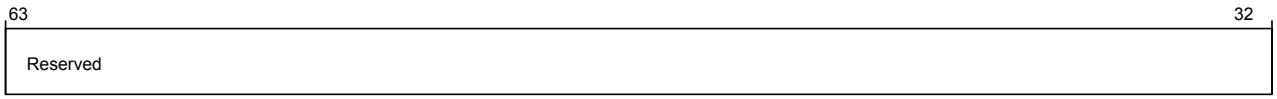


Figure 3-770 por_mxp_por_dtm_wp3_config (high)

The following table shows the por_dtm_wp3_config higher register bit assignments.

Table 3-784 por_mxp_por_dtm_wp3_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

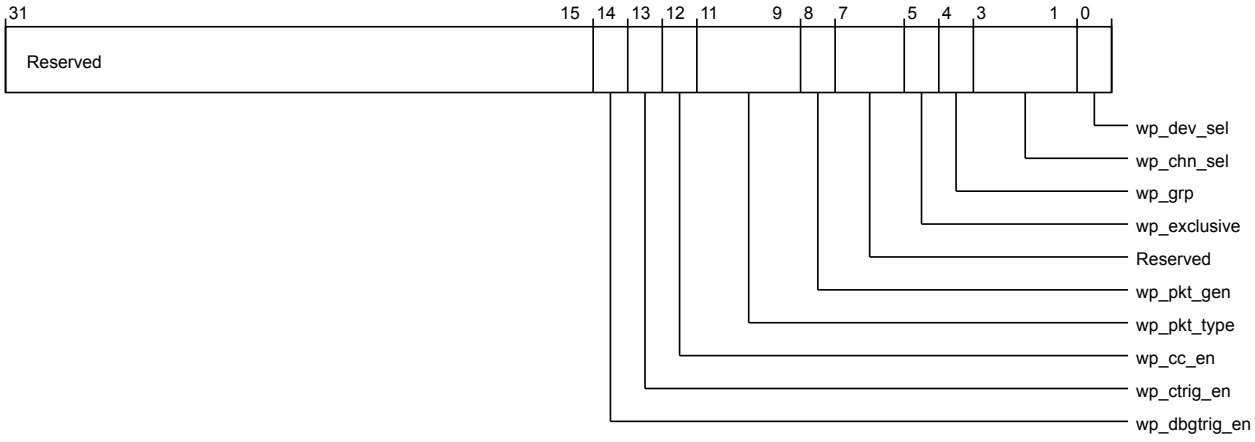


Figure 3-771 por_mxp_por_dtm_wp3_config (low)

The following table shows the por_dtm_wp3_config lower register bit assignments.

Table 3-785 por_mxp_por_dtm_wp3_config (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14	wp_dbgtrig_en	Enables watchpoint debug trigger packet generation	RW	1'b0
13	wp_ctrig_en	Enables watchpoint cross trigger packet generation	RW	1'b0
12	wp_cc_en	Enables inclusion of cycle count in watchpoint track packet generation	RW	1'b0
11:9	wp_pkt_type	Trace packet type 3'b000: TXNID (up to X18) 3'b001: TXNID + opcode (up to X9) 3'b010: TXNID + opcode + source ID + target ID (up to X4) 3'b011: Reserved 3'b100: Control flit 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	RW	3'b000
8	wp_pkt_gen	Enables watchpoint trace packet generation	RW	1'b0
7:6	Reserved	Reserved	RO	-
5	wp_exclusive	Watchpoint mode 1'b0: Regular mode 1'b1: Exclusive mode	RW	1'b0

Table 3-785 por_mxp_por_dtm_wp3_config (low) (continued)

Bits	Field name	Description	Type	Reset
4	wp_grp	Watchpoint register format group 1'b0: Select primary group 1'b1: Select secondary group	RW	1'b0
3:1	wp_chn_sel	VC selection 3'b000: Select REQ VC 3'b001: Select RSP VC 3'b010: Select SNP VC 3'b011: Select DATA VC NOTE: All other values are reserved.	RW	3'b000
0	wp_dev_sel	Device port selection in specified SMXP 1'b0: Select device port 0 1'b1: Select device port 1	RW	1'b0

por_dtm_wp3_val

Configures watchpoint 3 comparison value.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21F0
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

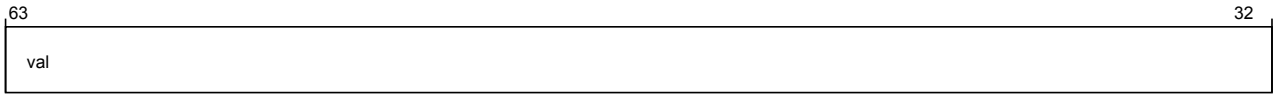


Figure 3-772 por_mxp_por_dtm_wp3_val (high)

The following table shows the por_dtm_wp3_val higher register bit assignments.

Table 3-786 por_mxp_por_dtm_wp3_val (high)

Bits	Field name	Description	Type	Reset
63:32	val	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

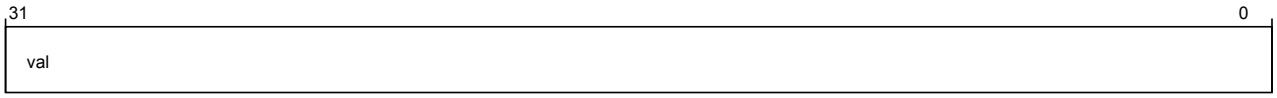


Figure 3-773 por_mxp_por_dtm_wp3_val (low)

The following table shows the por_dtm_wp3_val lower register bit assignments.

Table 3-787 por_mxp_por_dtm_wp3_val (low)

Bits	Field name	Description	Type	Reset
31:0	val	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_wp3_mask

Configures watchpoint 3 comparison mask.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h21F8
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

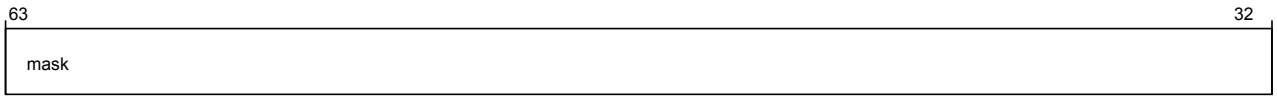


Figure 3-774 por_mxp_por_dtm_wp3_mask (high)

The following table shows the por_dtm_wp3_mask higher register bit assignments.

Table 3-788 por_mxp_por_dtm_wp3_mask (high)

Bits	Field name	Description	Type	Reset
63:32	mask	Refer to DTM watchpoint section for details	RW	64'b0

The following image shows the lower register bit assignments.

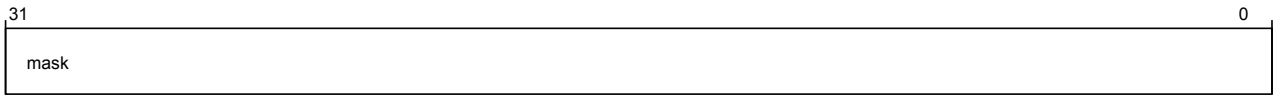


Figure 3-775 por_mxp_por_dtm_wp3_mask (low)

The following table shows the por_dtm_wp3_mask lower register bit assignments.

Table 3-789 por_mxp_por_dtm_wp3_mask (low)

Bits	Field name	Description	Type	Reset
31:0	mask	Refer to DTM watchpoint section for details	RW	64'b0

por_dtm_pmsicr

Functions as the sampling interval counter register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2200
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

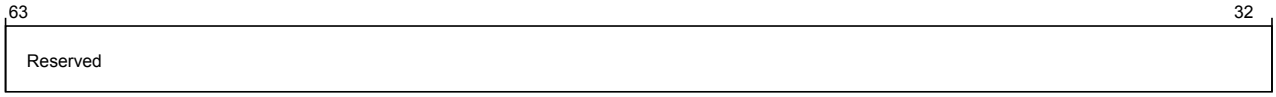


Figure 3-776 por_mxp_por_dtm_pmsicr (high)

The following table shows the por_dtm_pmsicr higher register bit assignments.

Table 3-790 por_mxp_por_dtm_pmsicr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

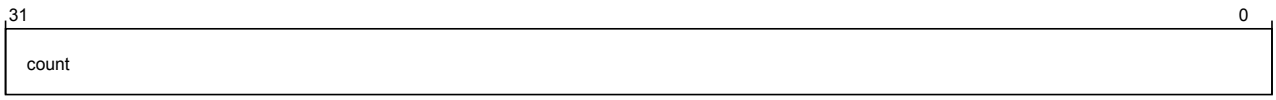


Figure 3-777 por_mxp_por_dtm_pmsicr (low)

The following table shows the por_dtm_pmsicr lower register bit assignments.

Table 3-791 por_mxp_por_dtm_pmsicr (low)

Bits	Field name	Description	Type	Reset
31:0	count	Current value of sample counter	RW	32'b0

por_dtm_pmsirr

Functions as the sampling interval reload register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2208
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

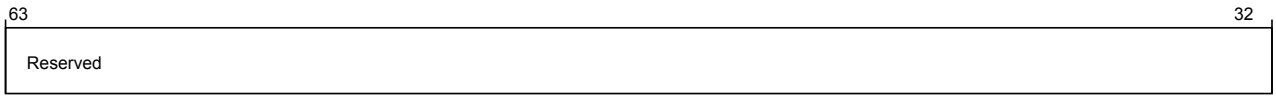


Figure 3-778 por_mxp_por_dtm_pmsirr (high)

The following table shows the por_dtm_pmsirr higher register bit assignments.

Table 3-792 por_mxp_por_dtm_pmsirr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

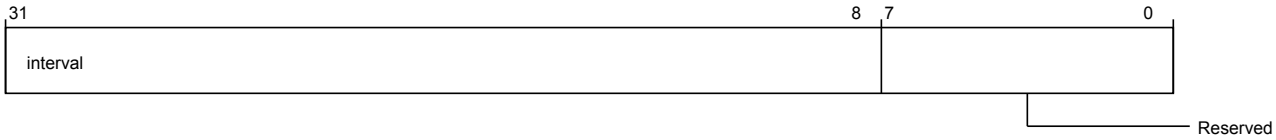


Figure 3-779 por_mxp_por_dtm_pmsirr (low)

The following table shows the por_dtm_pmsirr lower register bit assignments.

Table 3-793 por_mxp_por_dtm_pmsirr (low)

Bits	Field name	Description	Type	Reset
31:8	interval	Sampling interval to be reloaded	RW	24'b0
7:0	Reserved	Reserved	RO	-

por_dtm_pmu_config

Configures the DTM PMU.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2210
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

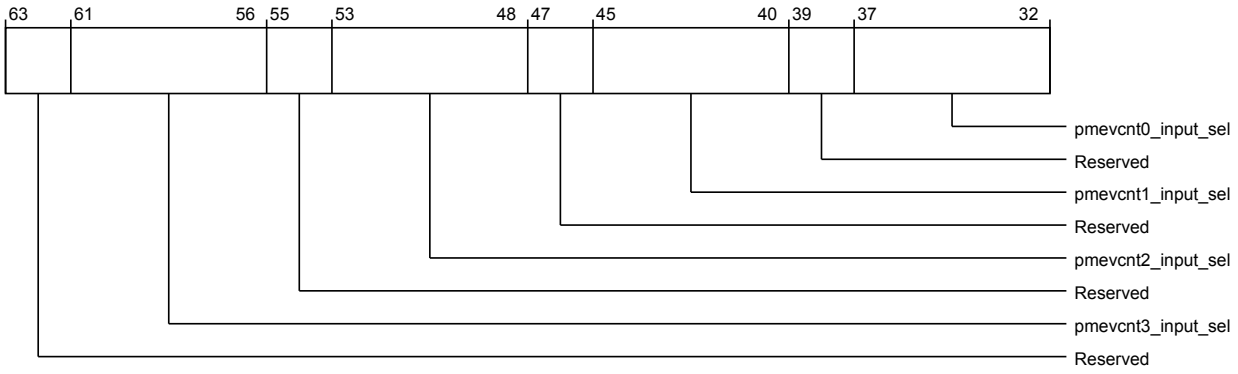


Figure 3-780 por_mxp_por_dtm_pmu_config (high)

The following table shows the por_dtm_pmu_config higher register bit assignments.

Table 3-794 por_mxp_por_dtm_pmu_config (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	pmevcnt3_input_sel	Source to be counted in PMU counter 3; see pmevcnt0_input_sel for encodings	RW	6'b0
55:54	Reserved	Reserved	RO	-
53:48	pmevcnt2_input_sel	Source to be counted in PMU counter 2; see pmevcnt0_input_sel for encodings	RW	6'b0
47:46	Reserved	Reserved	RO	-
45:40	pmevcnt1_input_sel	Source to be counted in PMU counter 1; see pmevcnt0_input_sel for encodings	RW	6'b0

Table 3-794 por_mxp_por_dtm_pmu_config (high) (continued)

Bits	Field name	Description	Type	Reset
39:38	Reserved	Reserved	RO	-

Table 3-794 por_mxp_por_dtm_pmu_config (high) (continued)

Bits	Field name	Description	Type	Reset
37:32	pmevcnt0_input_sel	Source to be counted in PMU counter 0 6'h00: Watchpoint 0 6'h01: Watchpoint 1 6'h02: Watchpoint 2 6'h03: Watchpoint 3 6'h04: XP PMU Event 0 6'h05: XP PMU Event 1 6'h06: XP PMU Event 2 6'h07: XP PMU Event 3 6'h10: Port 0 Device 0 PMU Event 0 6'h11: Port 0 Device 0 PMU Event 1 6'h12: Port 0 Device 0 PMU Event 2 6'h13: Port 0 Device 0 PMU Event 3 6'h14: Port 0 Device 1 PMU Event 0 6'h15: Port 0 Device 1 PMU Event 1 6'h16: Port 0 Device 1 PMU Event 2 6'h17: Port 0 Device 1 PMU Event 3 6'h18: Port 0 Device 2 PMU Event 0 6'h19: Port 0 Device 2 PMU Event 1 6'h1A: Port 0 Device 2 PMU Event 2 6'h1B: Port 0 Device 2 PMU Event 3 6'h1C: Port 0 Device 3 PMU Event 0 6'h1D: Port 0 Device 3 PMU Event 1 6'h1E: Port 0 Device 3 PMU Event 2 6'h1F: Port 0 Device 3 PMU Event 3 6'h20: Port 1 Device 0 PMU Event 0 6'h21: Port 1 Device 0 PMU Event 1 6'h22: Port 1 Device 0 PMU Event 2 6'h23: Port 1 Device 0 PMU Event 3 6'h24: Port 1 Device 1 PMU Event 0 6'h25: Port 1 Device 1 PMU Event 1 6'h26: Port 1 Device 1 PMU Event 2 6'h27: Port 1 Device 1 PMU Event 3 6'h28: Port 1 Device 2 PMU Event 0 6'h29: Port 1 Device 2 PMU Event 1 6'h2A: Port 1 Device 2 PMU Event 2 6'h2B: Port 1 Device 2 PMU Event 3 6'h2E: Port 1 Device 3 PMU Event 2	RW	6'b0

The following image shows the lower register bit assignments.

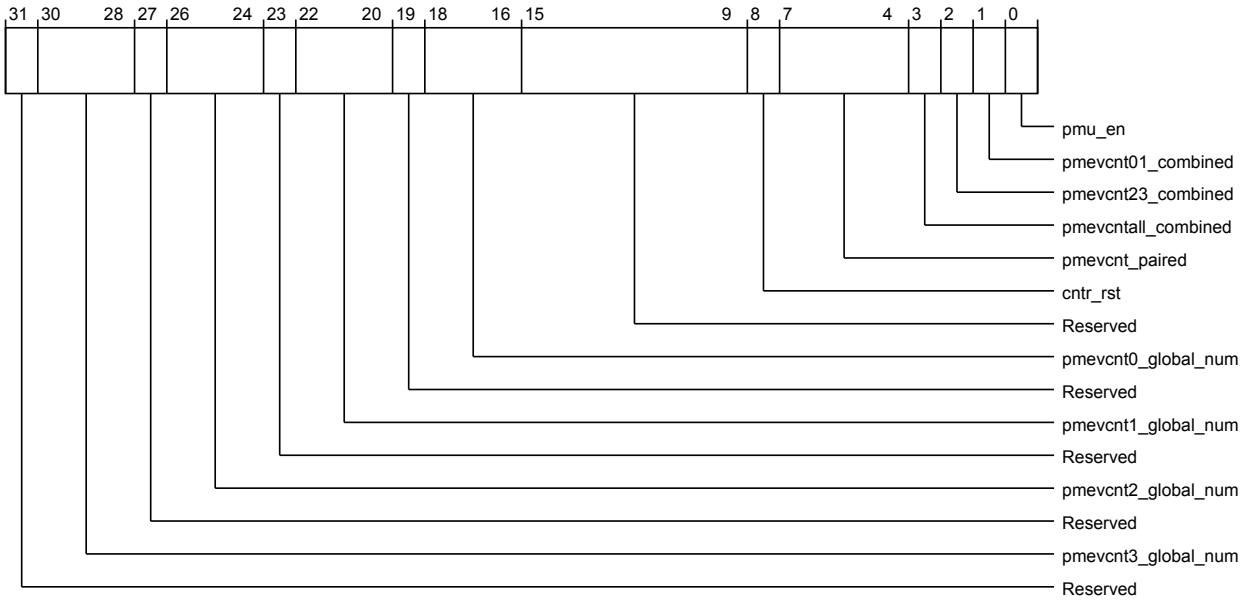


Figure 3-781 por_mxp_por_dtm_pmu_config (low)

The following table shows the por_dtm_pmu_config lower register bit assignments.

Table 3-795 por_mxp_por_dtm_pmu_config (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0
19	Reserved	Reserved	RO	-
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0

Table 3-795 por_mxp_por_dtm_pmu_config (low) (continued)

Bits	Field name	Description	Type	Reset
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	DTM PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

por_dtm_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2220
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

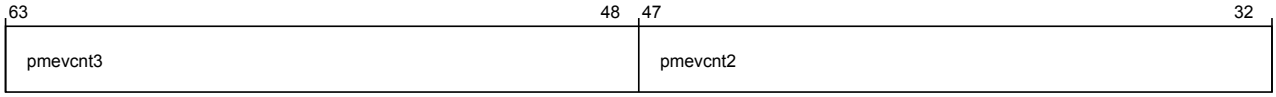


Figure 3-782 por_mxp_por_dtm_pmevcnt (high)

The following table shows the por_dtm_pmevcnt higher register bit assignments.

Table 3-796 por_mxp_por_dtm_pmevcnt (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcnt3	PMU event counter 3	RW	16'h0000
47:32	pmevcnt2	PMU event counter 2	RW	16'h0000

The following image shows the lower register bit assignments.

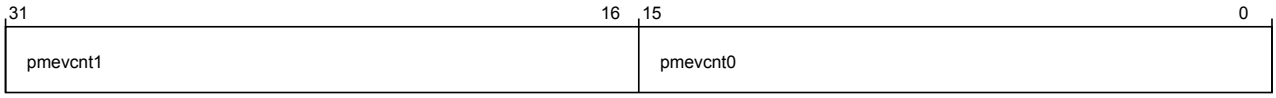


Figure 3-783 por_mxp_por_dtm_pmevcnt (low)

The following table shows the por_dtm_pmevcnt lower register bit assignments.

Table 3-797 por_mxp_por_dtm_pmevcnt (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcnt1	PMU event counter 1	RW	16'h0000
15:0	pmevcnt0	PMU event counter 0	RW	16'h0000

por_dtm_pmevcntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2240
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

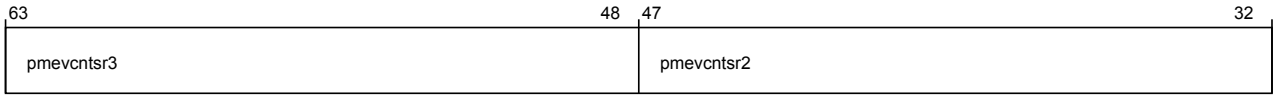


Figure 3-784 por_mxp_por_dtm_pmevcntsr (high)

The following table shows the por_dtm_pmevcntsr higher register bit assignments.

Table 3-798 por_mxp_por_dtm_pmevcntsr (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000

The following image shows the lower register bit assignments.

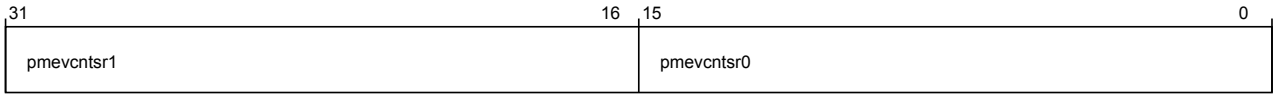


Figure 3-785 por_mxp_por_dtm_pmevcntsr (low)

The following table shows the por_dtm_pmevcntsr lower register bit assignments.

Table 3-799 por_mxp_por_dtm_pmevcntsr (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

3.3.7 RN-D register descriptions

Lists the RN-D registers.

por_rnd_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

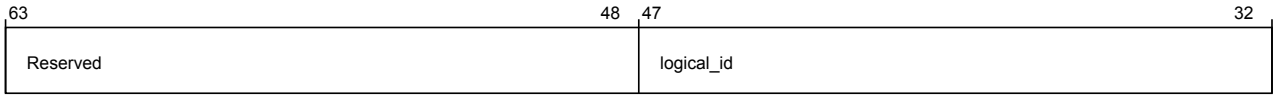


Figure 3-786 por_rnd_por_rnd_node_info (high)

The following table shows the por_rnd_node_info higher register bit assignments.

Table 3-800 por_rnd_por_rnd_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

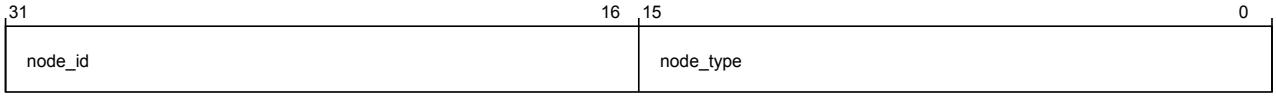


Figure 3-787 por_rnd_por_rnd_node_info (low)

The following table shows the por_rnd_node_info lower register bit assignments.

Table 3-801 por_rnd_por_rnd_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h000D

por_rnd_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

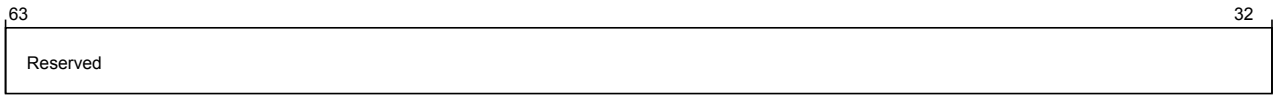


Figure 3-788 por_rnd_por_rnd_child_info (high)

The following table shows the por_rnd_child_info higher register bit assignments.

Table 3-802 por_rnd_por_rnd_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

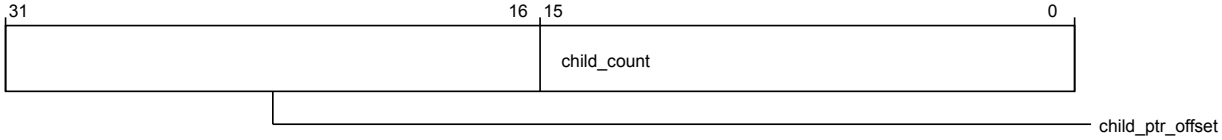


Figure 3-789 por_rnd_por_rnd_child_info (low)

The following table shows the por_rnd_child_info lower register bit assignments.

Table 3-803 por_rnd_por_rnd_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_rnd_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

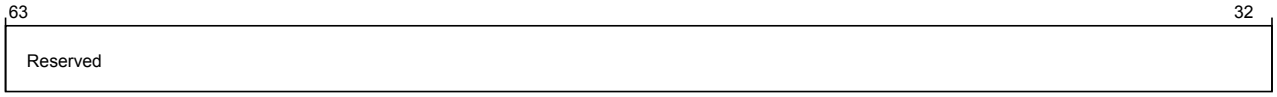


Figure 3-790 por_rnd_por_rnd_secure_register_groups_override (high)

The following table shows the por_rnd_secure_register_groups_override higher register bit assignments.

Table 3-804 por_rnd_por_rnd_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

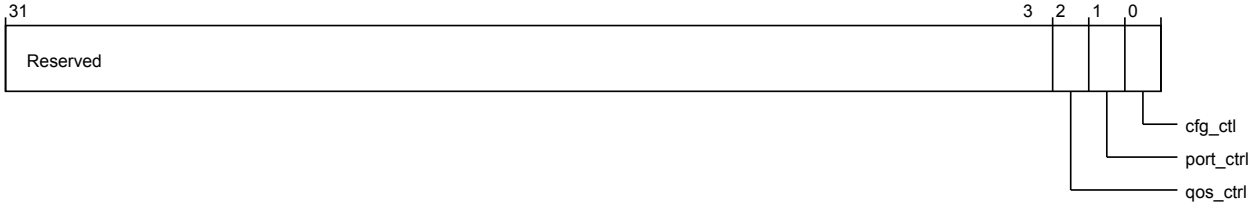


Figure 3-791 por_rnd_por_rnd_secure_register_groups_override (low)

The following table shows the por_rnd_secure_register_groups_override lower register bit assignments.

Table 3-805 por_rnd_por_rnd_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	qos_ctrl	Allows non-secure access to secure QoS control registers	RW	1'b0
1	port_ctrl	Allows non-secure access to secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_rnd_unit_info

Provides component identification information for RN-D.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

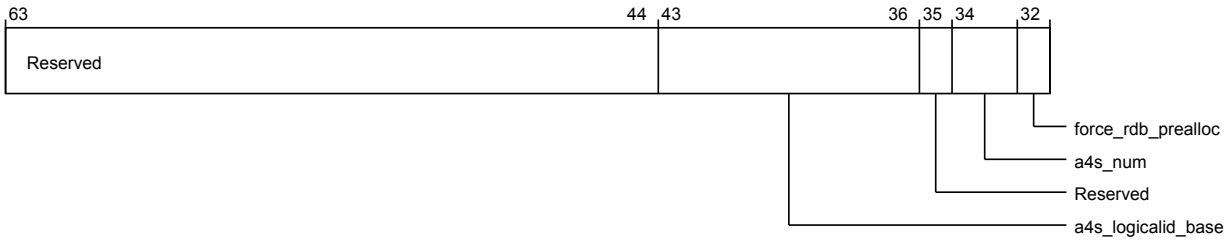


Figure 3-792 por_rnd_por_rnd_unit_info (high)

The following table shows the por_rnd_unit_info higher register bit assignments.

Table 3-806 por_rnd_por_rnd_unit_info (high)

Bits	Field name	Description	Type	Reset
63:44	Reserved	Reserved	RO	-
43:36	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
35	Reserved	Reserved	RO	-
34:33	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
32	force_rdb_prealloc	Force read data buffer preallocation 1'b1: yes 1'b0: no	RO	Configuration dependent

The following image shows the lower register bit assignments.

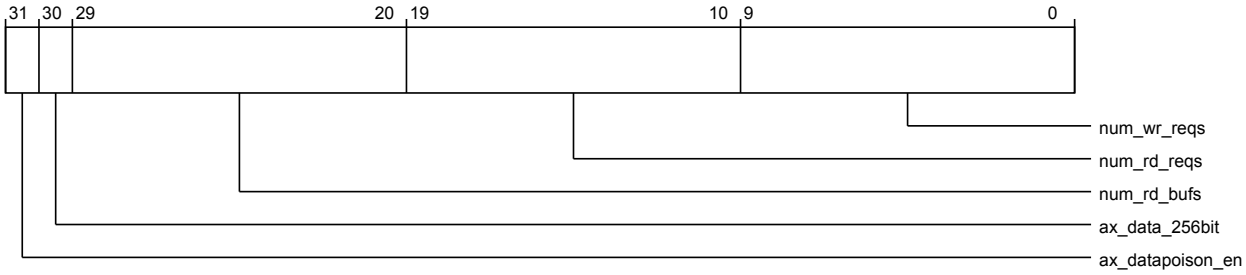


Figure 3-793 por_rnd_por_rnd_unit_info (low)

The following table shows the por_rnd_unit_info lower register bit assignments.

Table 3-807 por_rnd_por_rnd_unit_info (low)

Bits	Field name	Description	Type	Reset
31	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
30	ax_data_256bit	AXI interface data width 1'b1: 256 bits 1'b0: 128 bits	RO	Configuration dependent
29:20	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
19:10	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
9:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

por_rnd_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

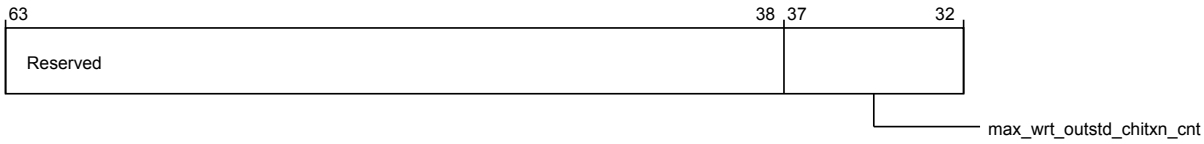


Figure 3-794 por_rnd_por_rnd_cfg_ctl (high)

The following table shows the por_rnd_cfg_ctl higher register bit assignments.

Table 3-808 por_rnd_por_rnd_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent

The following image shows the lower register bit assignments.

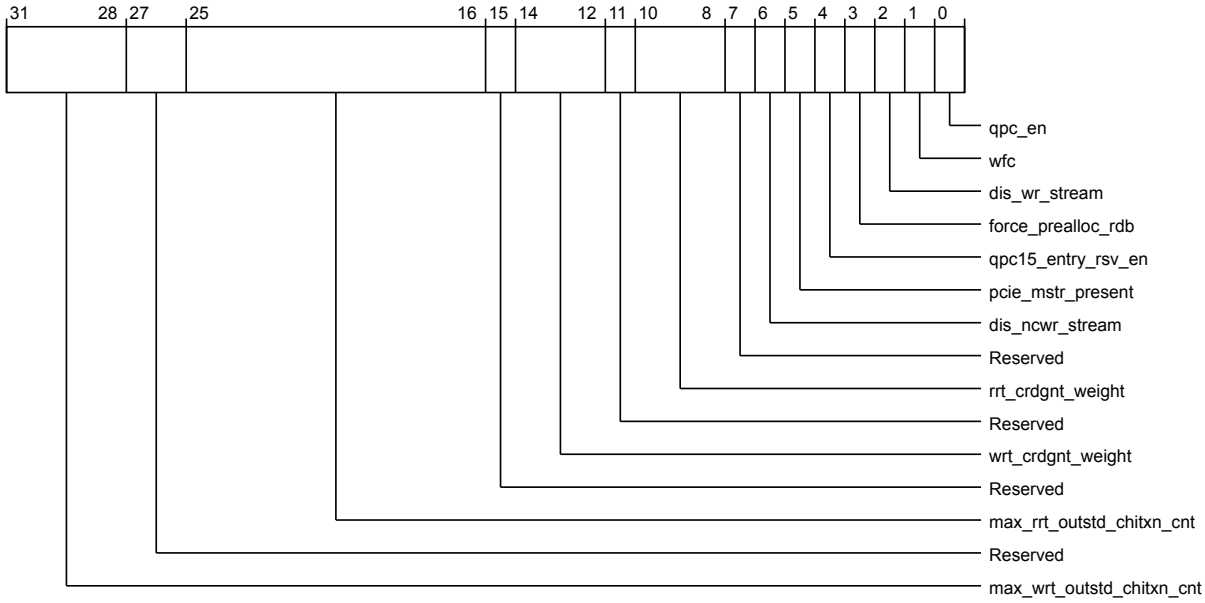


Figure 3-795 por_rnd_por_rnd_cfg_ctl (low)

The following table shows the por_rnd_cfg_ctl lower register bit assignments.

Table 3-809 por_rnd_por_rnd_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:28	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
27:26	Reserved	Reserved	RO	-
25:16	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	Reserved	Reserved	RO	-
10:8	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	Reserved	Reserved	RO	-
6	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	pcie_mstr_present	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0
4	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rnd_qpc_en is set	RW	1'b0

Table 3-809 por_rnd_por_rnd_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
3	force_prealloc_rdb	When set, all reads from the RN-D are sent with a preallocated read data buffer	RW	Configuration dependent
2	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
1	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

por_rnd_aux_ctl

Functions as the auxiliary control register for RN-D.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

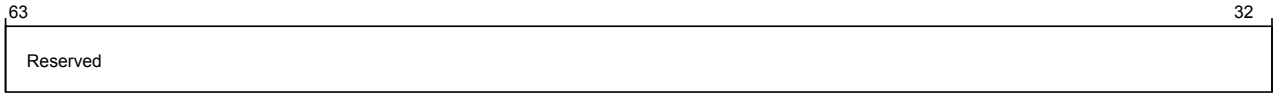


Figure 3-796 por_rnd_por_rnd_aux_ctl (high)

The following table shows the por_rnd_aux_ctl higher register bit assignments.

Table 3-810 por_rnd_por_rnd_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

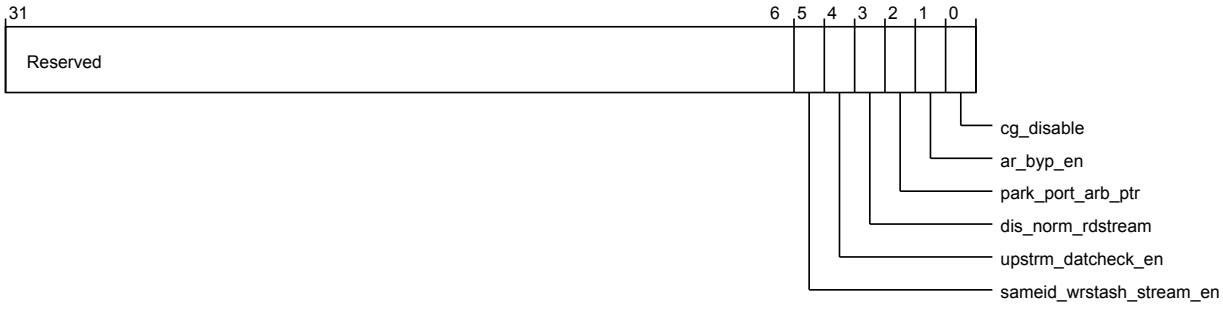


Figure 3-797 por_rnd_por_rnd_aux_ctl (low)

The following table shows the por_rnd_aux_ctl lower register bit assignments.

Table 3-811 por_rnd_por_rnd_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	sameid_wrstash_stream_en	Enables streaming of same-ID WrUniqStash	RW	Configuration dependent
4	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
3	dis_norm_rdstream	Disables streaming of same ARID normal memory reads to different address	RW	dis_norm_rdstream
2	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	cg_disable	Disables clock gating when set	RW	1'b0

por_rnd_s0_port_control

Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

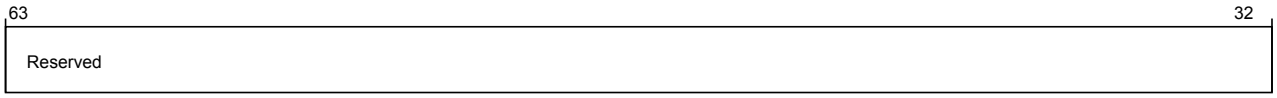


Figure 3-798 por_rnd_por_rnd_s0_port_control (high)

The following table shows the por_rnd_s0_port_control higher register bit assignments.

Table 3-812 por_rnd_por_rnd_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

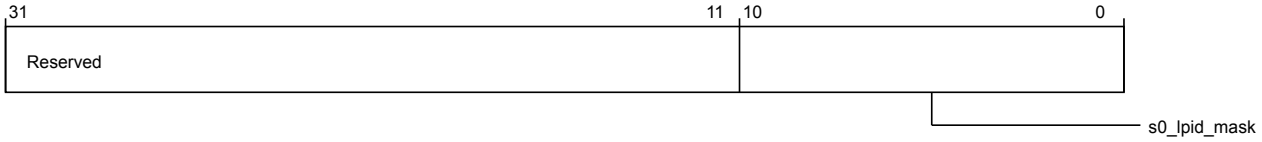


Figure 3-799 por_rnd_por_rnd_s0_port_control (low)

The following table shows the por_rnd_s0_port_control lower register bit assignments.

Table 3-813 por_rnd_por_rnd_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s1_port_control

Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

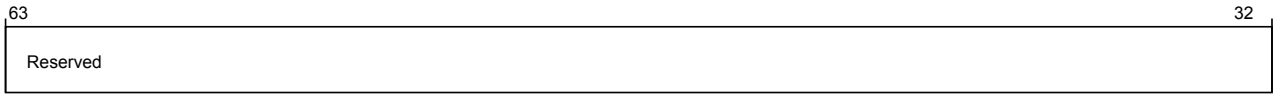


Figure 3-800 por_rnd_por_rnd_s1_port_control (high)

The following table shows the por_rnd_s1_port_control higher register bit assignments.

Table 3-814 por_rnd_por_rnd_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

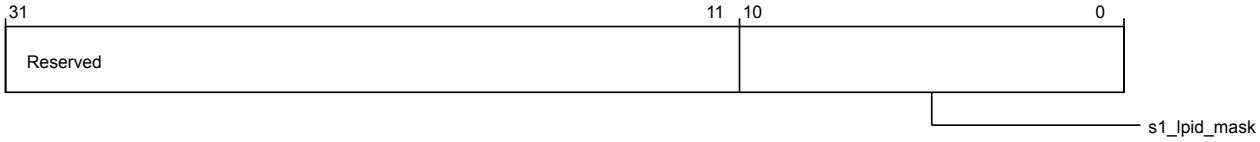


Figure 3-801 por_rnd_por_rnd_s1_port_control (low)

The following table shows the por_rnd_s1_port_control lower register bit assignments.

Table 3-815 por_rnd_por_rnd_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s2_port_control

Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

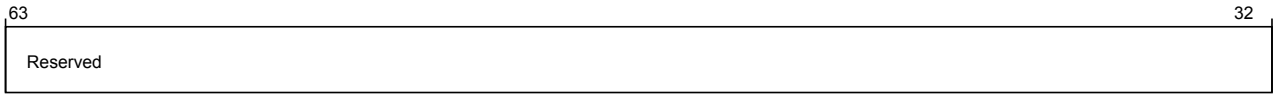


Figure 3-802 por_rnd_por_rnd_s2_port_control (high)

The following table shows the por_rnd_s2_port_control higher register bit assignments.

Table 3-816 por_rnd_por_rnd_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

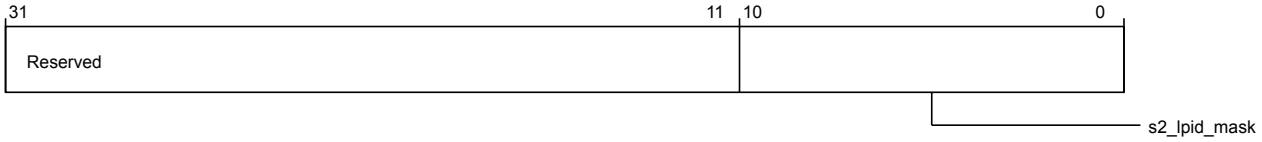


Figure 3-803 por_rnd_por_rnd_s2_port_control (low)

The following table shows the por_rnd_s2_port_control lower register bit assignments.

Table 3-817 por_rnd_por_rnd_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rnd_s0_qos_control

Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

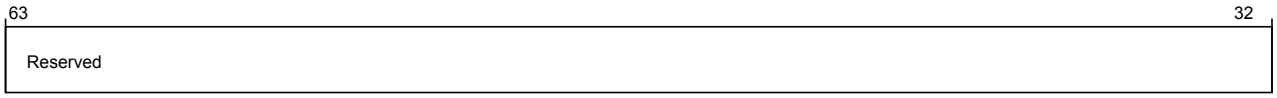


Figure 3-804 por_rnd_por_rnd_s0_qos_control (high)

The following table shows the por_rnd_s0_qos_control higher register bit assignments.

Table 3-818 por_rnd_por_rnd_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

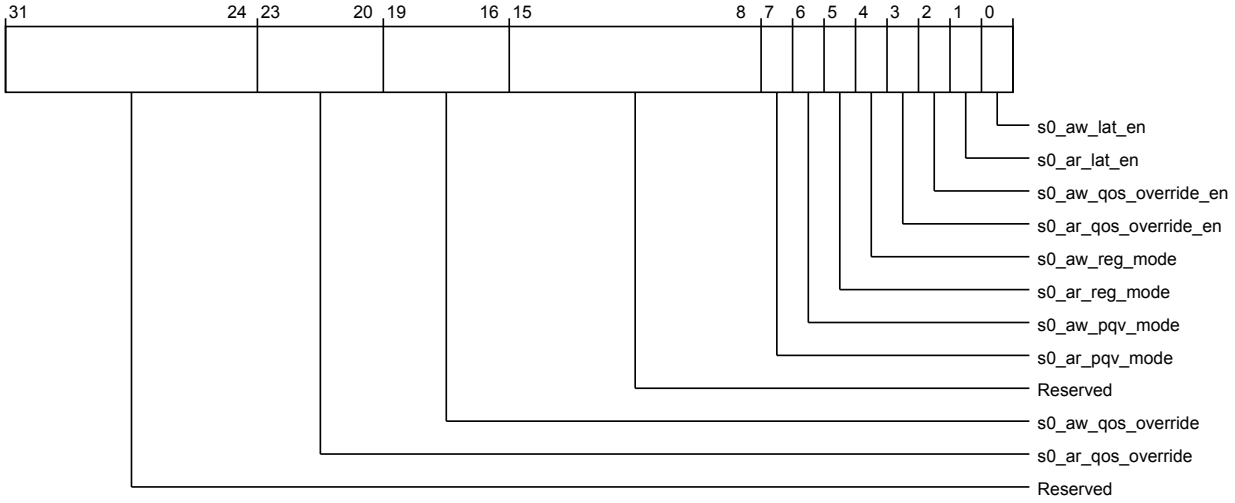


Figure 3-805 por_rnd_por_rnd_s0_qos_control (low)

The following table shows the por_rnd_s0_qos_control lower register bit assignments.

Table 3-819 por_rnd_por_rnd_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0

Table 3-819 por_rnd_por_rnd_s0_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
6	s0_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s0_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s0_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s0_ar_qos_override_en	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s0_aw_qos_override_en	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s0_ar_lat_en	Enables port S0 AR QoS regulation when set	RW	1'b0
0	s0_aw_lat_en	Enables port S0 AW QoS regulation when set	RW	1'b0

por_rnd_s0_qos_lat_tgt

Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

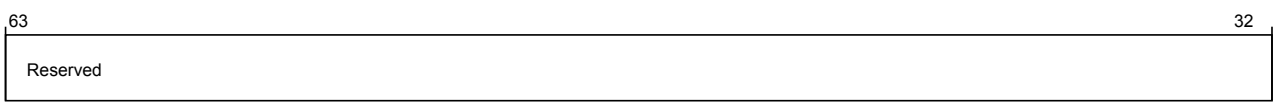


Figure 3-806 por_rnd_por_rnd_s0_qos_lat_tgt (high)

The following table shows the por_rnd_s0_qos_lat_tgt higher register bit assignments.

Table 3-820 por_rnd_por_rnd_s0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

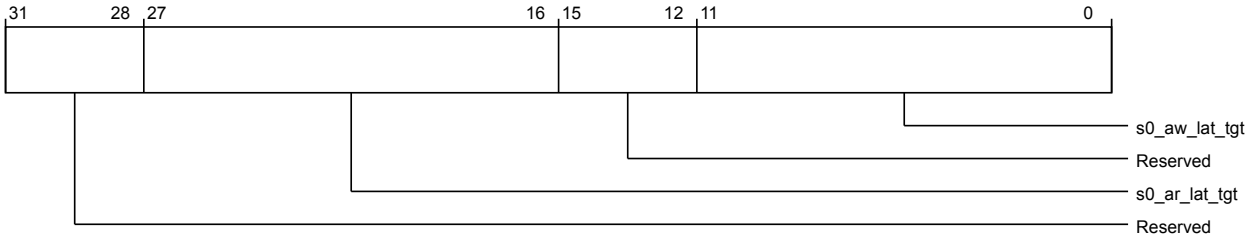


Figure 3-807 por_rnd_por_rnd_s0_qos_lat_tgt (low)

The following table shows the por_rnd_s0_qos_lat_tgt lower register bit assignments.

Table 3-821 por_rnd_por_rnd_s0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s0_ar_lat_tgt	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s0_aw_lat_tgt	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rnd_s0_qos_lat_scale

Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

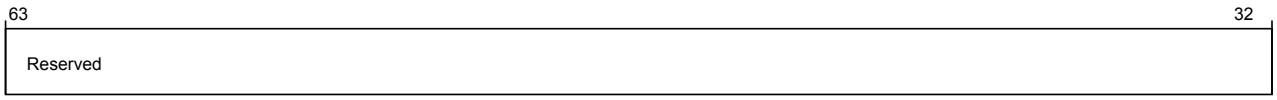


Figure 3-808 por_rnd_por_rnd_s0_qos_lat_scale (high)

The following table shows the por_rnd_s0_qos_lat_scale higher register bit assignments.

Table 3-822 por_rnd_por_rnd_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

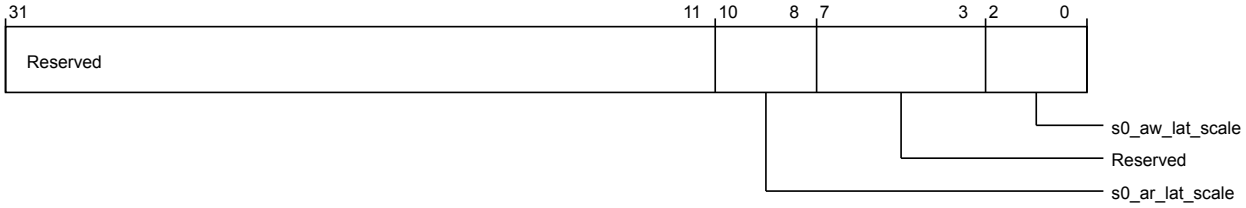


Figure 3-809 por_rnd_por_rnd_s0_qos_lat_scale (low)

The following table shows the por_rnd_s0_qos_lat_scale lower register bit assignments.

Table 3-823 por_rnd_por_rnd_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rnd_s0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hA98
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

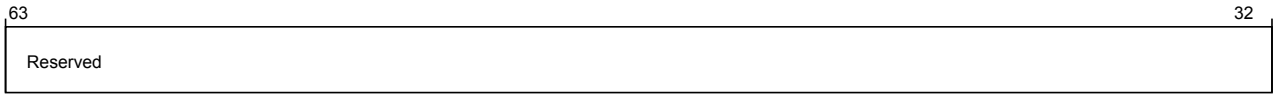


Figure 3-810 por_rnd_por_rnd_s0_qos_lat_range (high)

The following table shows the por_rnd_s0_qos_lat_range higher register bit assignments.

Table 3-824 por_rnd_por_rnd_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

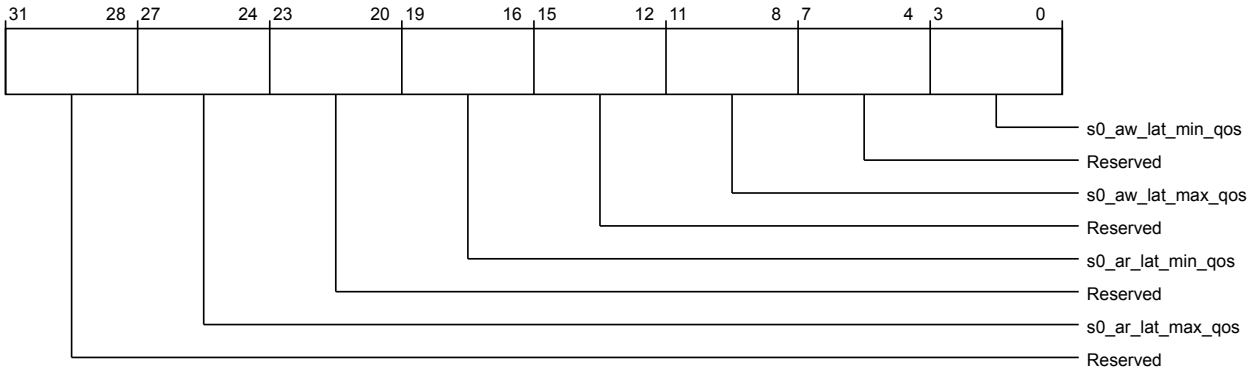


Figure 3-811 por_rnd_por_rnd_s0_qos_lat_range (low)

The following table shows the por_rnd_s0_qos_lat_range lower register bit assignments.

Table 3-825 por_rnd_por_rnd_s0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s0_ar_lat_max_qos	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s0_ar_lat_min_qos	Port S0 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s0_aw_lat_max_qos	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s0_aw_lat_min_qos	Port S0 AW QoS minimum value	RW	4'h0

por_rnd_s1_qos_control

Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

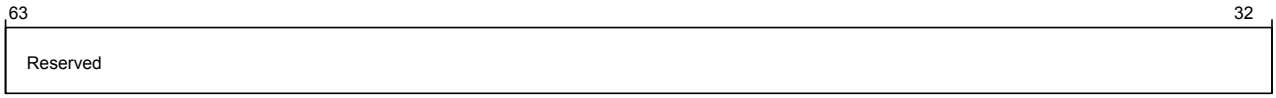


Figure 3-812 por_rnd_por_rnd_s1_qos_control (high)

The following table shows the por_rnd_s1_qos_control higher register bit assignments.

Table 3-826 por_rnd_por_rnd_s1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

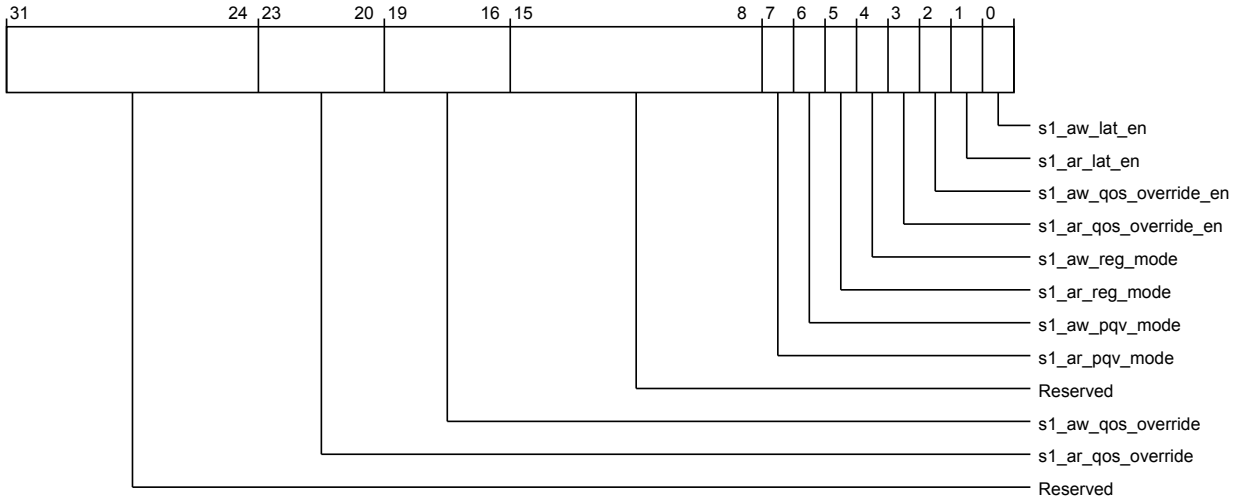


Figure 3-813 por_rnd_por_rnd_s1_qos_control (low)

The following table shows the por_rnd_s1_qos_control lower register bit assignments.

Table 3-827 por_rnd_por_rnd_s1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s1_ar_qos_override	AR QoS override value for port S1	RW	4'b0000
19:16	s1_aw_qos_override	AW QoS override value for port S1	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s1_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s1_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s1_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s1_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s1_ar_qos_override_en	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0

Table 3-827 por_rnd_por_rnd_s1_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
2	s1_aw_qos_override_en	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s1_ar_lat_en	Enables port S1 AR QoS regulation when set	RW	1'b0
0	s1_aw_lat_en	Enables port S1 AW QoS regulation when set	RW	1'b0

por_rnd_s1_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

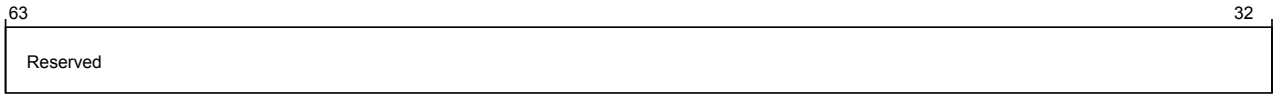


Figure 3-814 por_rnd_por_rnd_s1_qos_lat_tgt (high)

The following table shows the por_rnd_s1_qos_lat_tgt higher register bit assignments.

Table 3-828 por_rnd_por_rnd_s1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

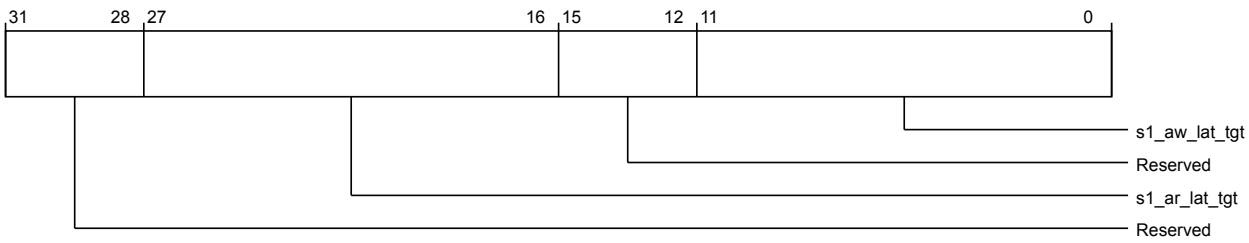


Figure 3-815 por_rnd_por_rnd_s1_qos_lat_tgt (low)

The following table shows the por_rnd_s1_qos_lat_tgt lower register bit assignments.

Table 3-829 por_rnd_por_rnd_s1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s1_ar_lat_tgt	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s1_aw_lat_tgt	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rnd_s1_qos_lat_scale

Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

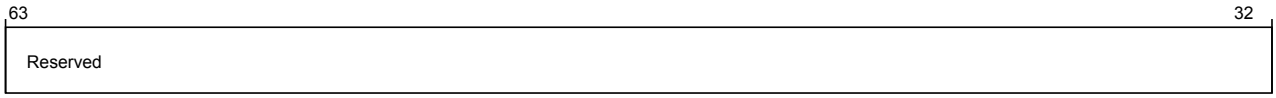


Figure 3-816 por_rnd_por_rnd_s1_qos_lat_scale (high)

The following table shows the por_rnd_s1_qos_lat_scale higher register bit assignments.

Table 3-830 por_rnd_por_rnd_s1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

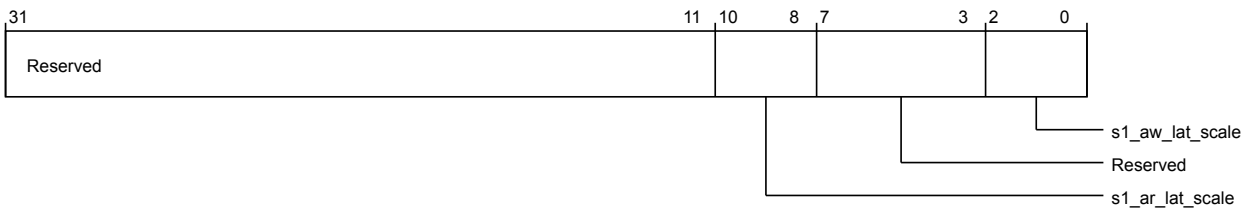


Figure 3-817 por_rnd_por_rnd_s1_qos_lat_scale (low)

The following table shows the por_rnd_s1_qos_lat_scale lower register bit assignments.

Table 3-831 por_rnd_por_rnd_s1_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s1_ar_lat_scale	Port S1 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s1_aw_lat_scale	Port S1 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rnd_s1_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

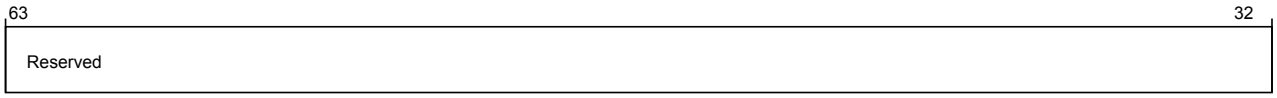


Figure 3-818 por_rnd_por_rnd_s1_qos_lat_range (high)

The following table shows the por_rnd_s1_qos_lat_range higher register bit assignments.

Table 3-832 por_rnd_por_rnd_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

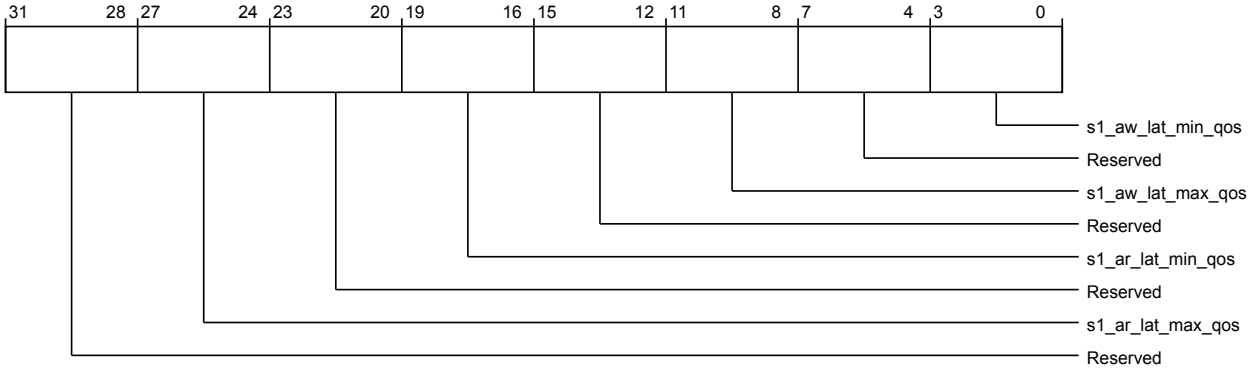


Figure 3-819 por_rnd_por_rnd_s1_qos_lat_range (low)

The following table shows the por_rnd_s1_qos_lat_range lower register bit assignments.

Table 3-833 por_rnd_por_rnd_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

por_rnd_s2_qos_control

Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

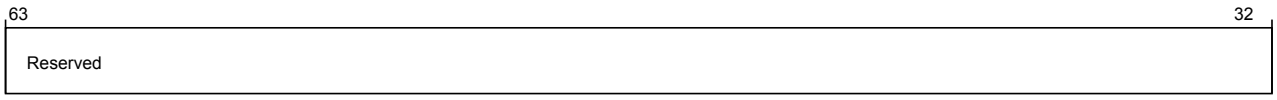


Figure 3-820 por_rnd_por_rnd_s2_qos_control (high)

The following table shows the por_rnd_s2_qos_control higher register bit assignments.

Table 3-834 por_rnd_por_rnd_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

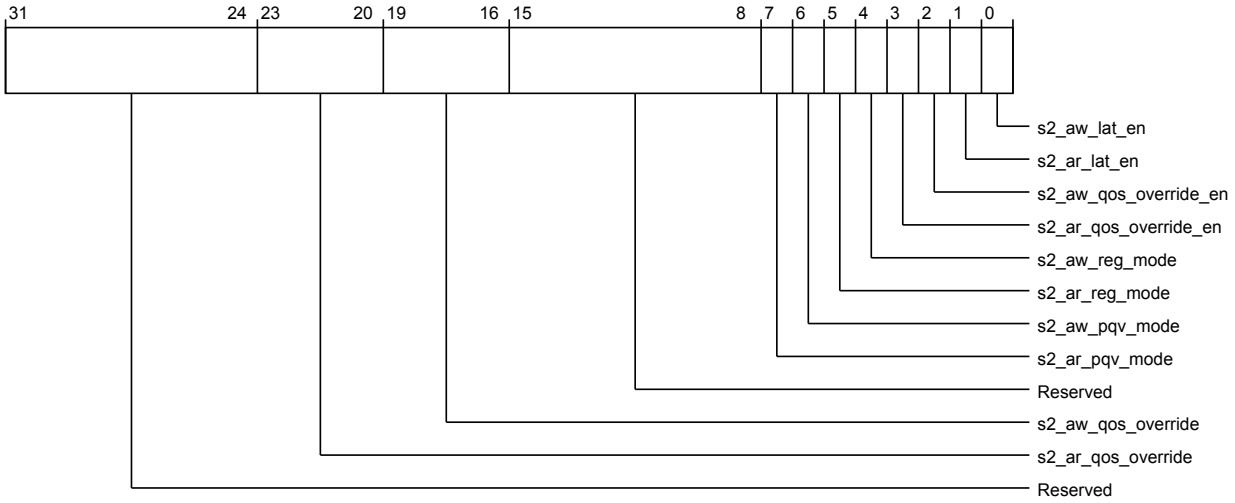


Figure 3-821 por_rnd_por_rnd_s2_qos_control (low)

The following table shows the por_rnd_s2_qos_control lower register bit assignments.

Table 3-835 por_rnd_por_rnd_s2_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s2_ar_qos_override	AR QoS override value for port S2	RW	4'b0000
19:16	s2_aw_qos_override	AW QoS override value for port S2	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s2_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s2_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s2_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s2_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s2_ar_qos_override_en	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s2_aw_qos_override_en	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s2_ar_lat_en	Enables port S2 AR QoS regulation when set	RW	1'b0
0	s2_aw_lat_en	Enables port S2 AW QoS regulation when set	RW	1'b0

por_rnd_s2_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

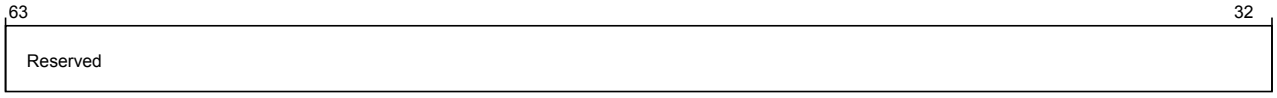


Figure 3-822 por_rnd_por_rnd_s2_qos_lat_tgt (high)

The following table shows the por_rnd_s2_qos_lat_tgt higher register bit assignments.

Table 3-836 por_rnd_por_rnd_s2_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

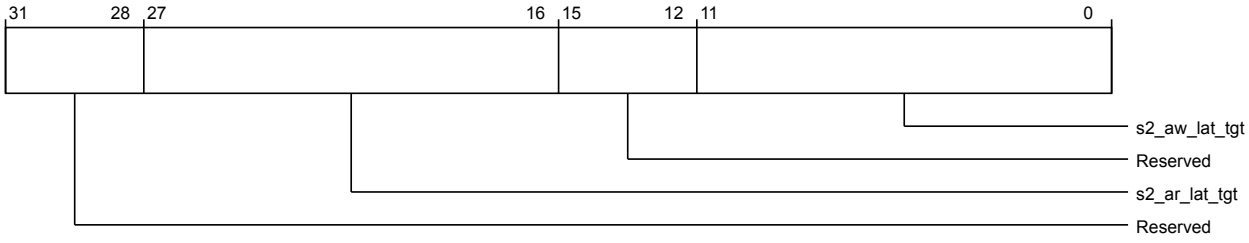


Figure 3-823 por_rnd_por_rnd_s2_qos_lat_tgt (low)

The following table shows the por_rnd_s2_qos_lat_tgt lower register bit assignments.

Table 3-837 por_rnd_por_rnd_s2_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s2_ar_lat_tgt	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s2_aw_lat_tgt	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rnd_s2_qos_lat_scale

Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

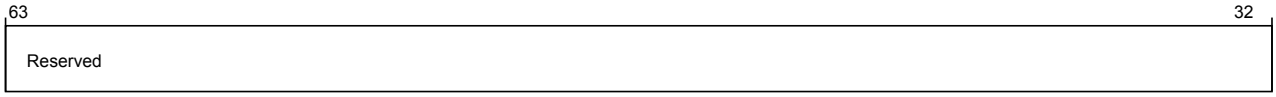


Figure 3-824 por_rnd_por_rnd_s2_qos_lat_scale (high)

The following table shows the por_rnd_s2_qos_lat_scale higher register bit assignments.

Table 3-838 por_rnd_por_rnd_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

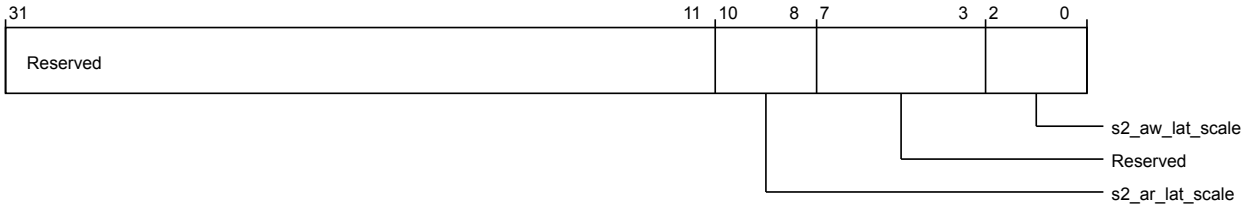


Figure 3-825 por_rnd_por_rnd_s2_qos_lat_scale (low)

The following table shows the por_rnd_s2_qos_lat_scale lower register bit assignments.

Table 3-839 por_rnd_por_rnd_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

Table 3-839 por_rnd_por_rnd_s2_qos_lat_scale (low) (continued)

Bits	Field name	Description	Type	Reset
7:3	Reserved	Reserved	RO	-
2:0	s2_aw_lat_scale	Port S2 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rnd_s2_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnd_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

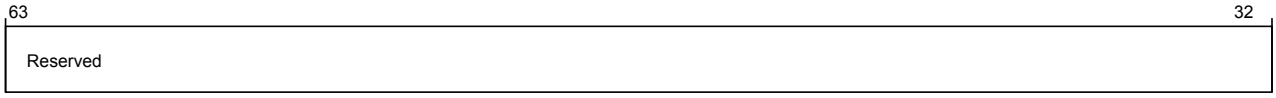


Figure 3-826 por_rnd_por_rnd_s2_qos_lat_range (high)

The following table shows the por_rnd_s2_qos_lat_range higher register bit assignments.

Table 3-840 por_rnd_por_rnd_s2_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

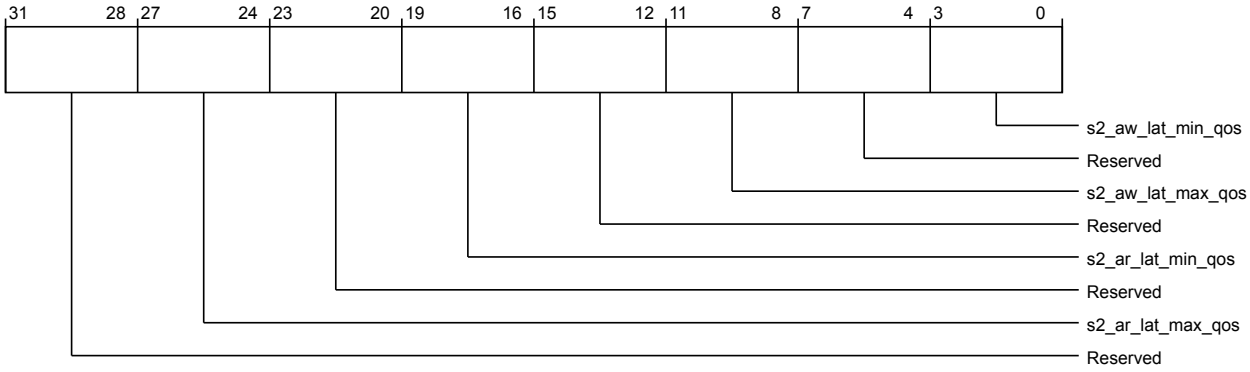


Figure 3-827 por_rnd_por_rnd_s2_qos_lat_range (low)

The following table shows the por_rnd_s2_qos_lat_range lower register bit assignments.

Table 3-841 por_rnd_por_rnd_s2_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s2_ar_lat_max_qos	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s2_ar_lat_min_qos	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s2_aw_lat_max_qos	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s2_aw_lat_min_qos	Port S2 AW QoS minimum value	RW	4'h0

por_rnd_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

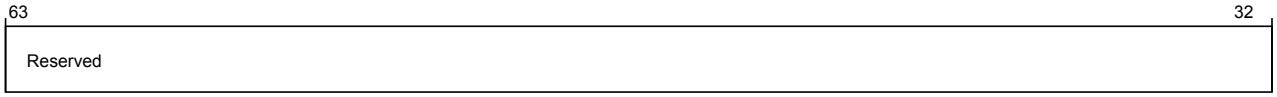


Figure 3-828 por_rnd_por_rnd_pmu_event_sel (high)

The following table shows the por_rnd_pmu_event_sel higher register bit assignments.

Table 3-842 por_rnd_por_rnd_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

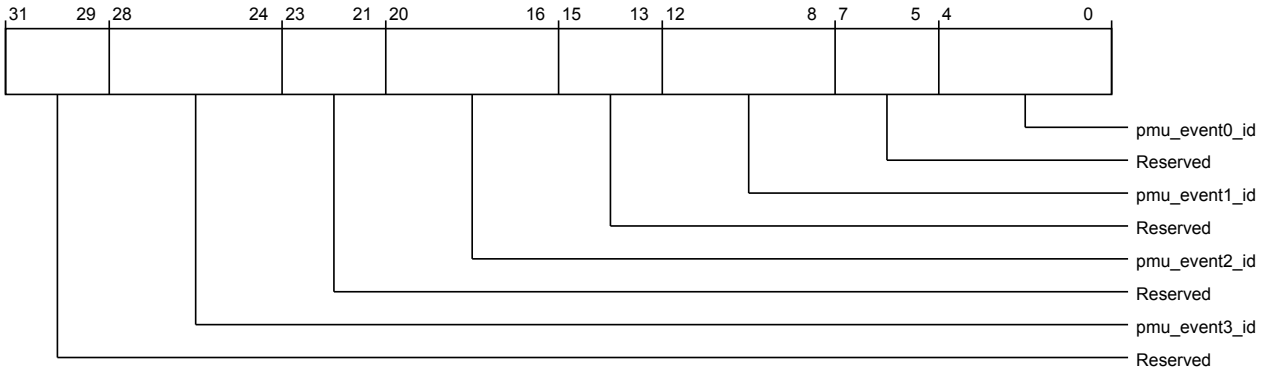


Figure 3-829 por_rnd_por_rnd_pmu_event_sel (low)

The following table shows the por_rnd_pmu_event_sel lower register bit assignments.

Table 3-843 por_rnd_por_rnd_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	RN-D PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	RN-D PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	RN-D PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 3-843 por_rnd_por_rnd_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	pmu_event0_id	RN-D PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: RDB pool state is all unordered 5'h12: RDB pool state is replay 5'h13: RDB pool state is hybrid 5'h14: RDB pool state is all ordered	RW	5'b0

por_rnd_syscoreq_ctl

Functions as the RN-D DVM domain control register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoack_status.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1000
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

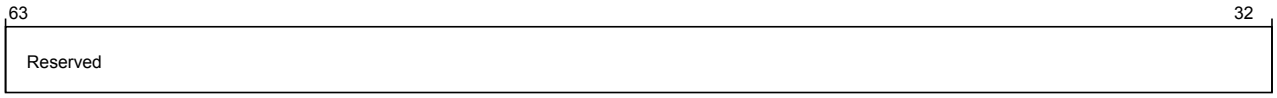


Figure 3-830 por_rnd_por_rnd_syscoreq_ctl (high)

The following table shows the por_rnd_syscoreq_ctl higher register bit assignments.

Table 3-844 por_rnd_por_rnd_syscoreq_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

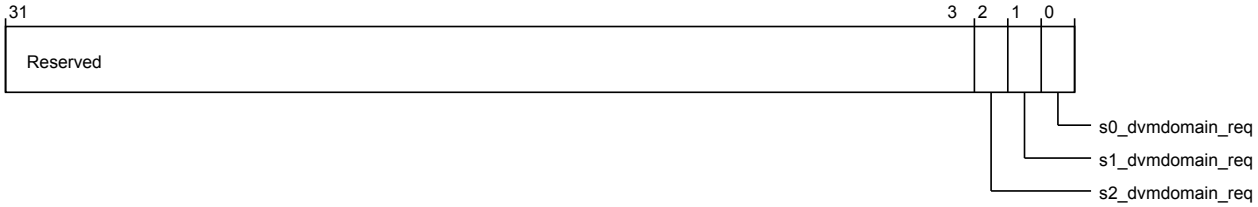


Figure 3-831 por_rnd_por_rnd_syscoreq_ctl (low)

The following table shows the por_rnd_syscoreq_ctl lower register bit assignments.

Table 3-845 por_rnd_por_rnd_syscoreq_ctl (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	s2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S2	RW	1'b0
1	s1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S1	RW	1'b0
0	s0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for port S0	RW	1'b0

por_rnd_syscoack_status

Functions as the RN-D DVM domain status register. Provides a software alternative to hardware SYSCOREQ/SYSCOACK handshake. Works with por_rnd_syscoreq_ctl.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h1008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

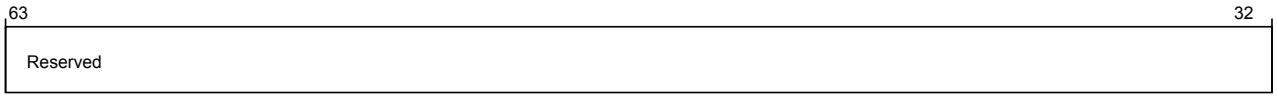


Figure 3-832 por_rnd_por_rnd_syscoack_status (high)

The following table shows the por_rnd_syscoack_status higher register bit assignments.

Table 3-846 por_rnd_por_rnd_syscoack_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

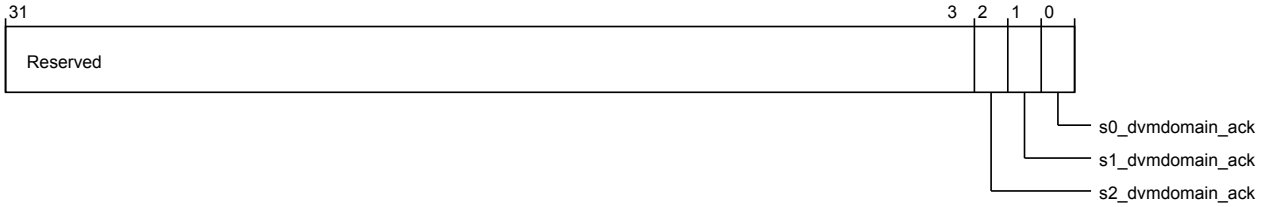


Figure 3-833 por_rnd_por_rnd_syscoack_status (low)

The following table shows the por_rnd_syscoack_status lower register bit assignments.

Table 3-847 por_rnd_por_rnd_syscoack_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	s2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S2	RO	1'b0
1	s1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S1	RO	1'b0
0	s0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for port S0	RO	1'b0

3.3.8 RN-I register descriptions

Lists the RN-I registers.

por_rni_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

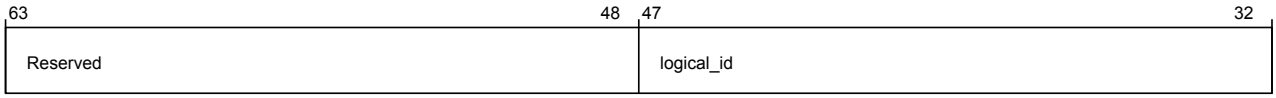


Figure 3-834 por_rni_por_rni_node_info (high)

The following table shows the por_rni_node_info higher register bit assignments.

Table 3-848 por_rni_por_rni_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

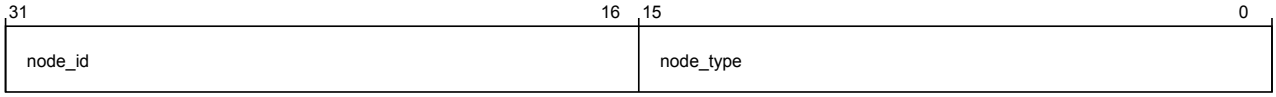


Figure 3-835 por_rni_por_rni_node_info (low)

The following table shows the por_rni_node_info lower register bit assignments.

Table 3-849 por_rni_por_rni_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h000A

por_rni_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

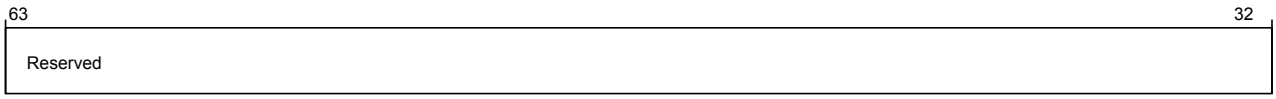


Figure 3-836 por_rni_por_rni_child_info (high)

The following table shows the por_rni_child_info higher register bit assignments.

Table 3-850 por_rni_por_rni_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

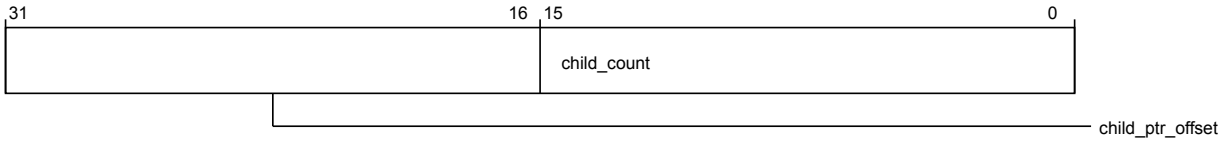


Figure 3-837 por_rni_por_rni_child_info (low)

The following table shows the por_rni_child_info lower register bit assignments.

Table 3-851 por_rni_por_rni_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_rni_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

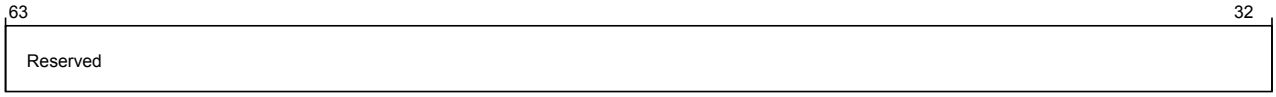


Figure 3-838 por_rni_por_rni_secure_register_groups_override (high)

The following table shows the por_rni_secure_register_groups_override higher register bit assignments.

Table 3-852 por_rni_por_rni_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

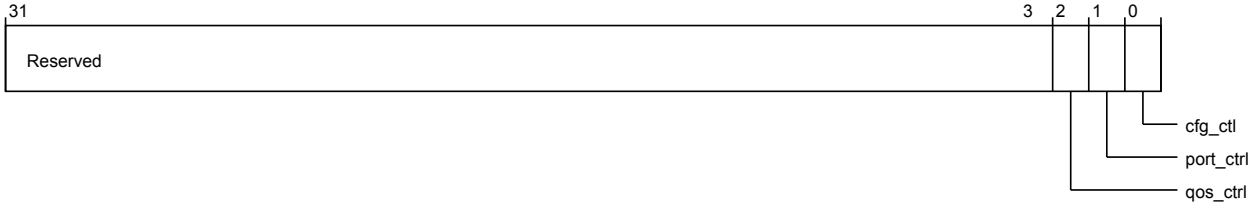


Figure 3-839 por_rni_por_rni_secure_register_groups_override (low)

The following table shows the por_rni_secure_register_groups_override lower register bit assignments.

Table 3-853 por_rni_por_rni_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	qos_ctrl	Allows non-secure access to secure QoS control registers	RW	1'b0
1	port_ctrl	Allows non-secure access to secure AXI port control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_rni_unit_info

Provides component identification information for RN-I.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

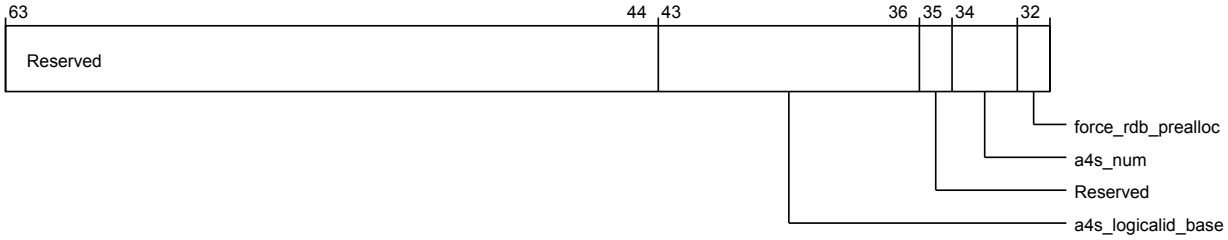


Figure 3-840 por_rni_por_rni_unit_info (high)

The following table shows the por_rni_unit_info higher register bit assignments.

Table 3-854 por_rni_por_rni_unit_info (high)

Bits	Field name	Description	Type	Reset
63:44	Reserved	Reserved	RO	-
43:36	a4s_logicalid_base	AXI4Stream interfaces logical ID base	RO	Configuration dependent
35	Reserved	Reserved	RO	-
34:33	a4s_num	Number of AXI4Stream interfaces present	RO	Configuration dependent
32	force_rdb_prealloc	Force read data buffer preallocation 1'b1: yes 1'b0: no	RO	Configuration dependent

The following image shows the lower register bit assignments.

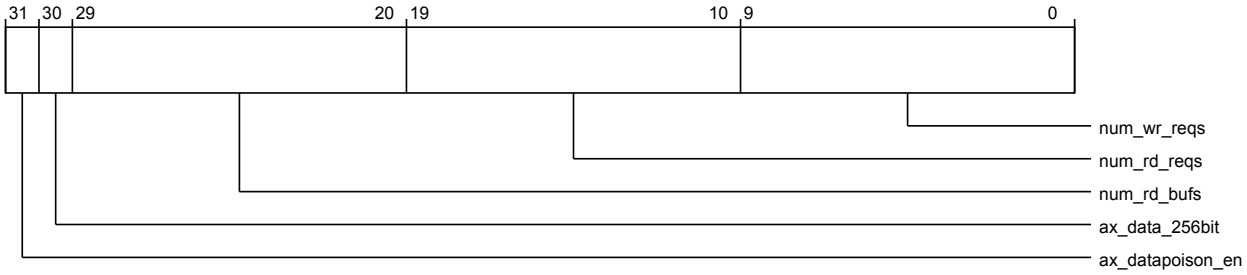


Figure 3-841 por_rni_por_rni_unit_info (low)

The following table shows the por_rni_unit_info lower register bit assignments.

Table 3-855 por_rni_por_rni_unit_info (low)

Bits	Field name	Description	Type	Reset
31	ax_datapoison_en	Data Poison enable on ACE-Lite/AXI4 interface 1'b1: Enabled 1'b0: Not enabled	RO	Configuration dependent
30	ax_data_256bit	AXI interface data width 1'b1: 256 bits 1'b0: 128 bits	RO	Configuration dependent
29:20	num_rd_bufs	Number of read data buffers	RO	Configuration dependent
19:10	num_rd_reqs	Number of outstanding read requests	RO	Configuration dependent
9:0	num_wr_reqs	Number of outstanding write requests	RO	Configuration dependent

por_rni_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

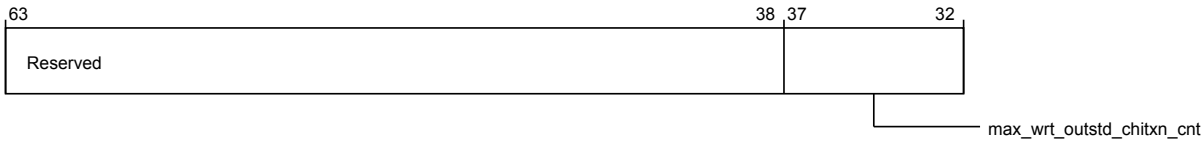


Figure 3-842 por_rni_por_rni_cfg_ctl (high)

The following table shows the por_rni_cfg_ctl higher register bit assignments.

Table 3-856 por_rni_por_rni_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent

The following image shows the lower register bit assignments.

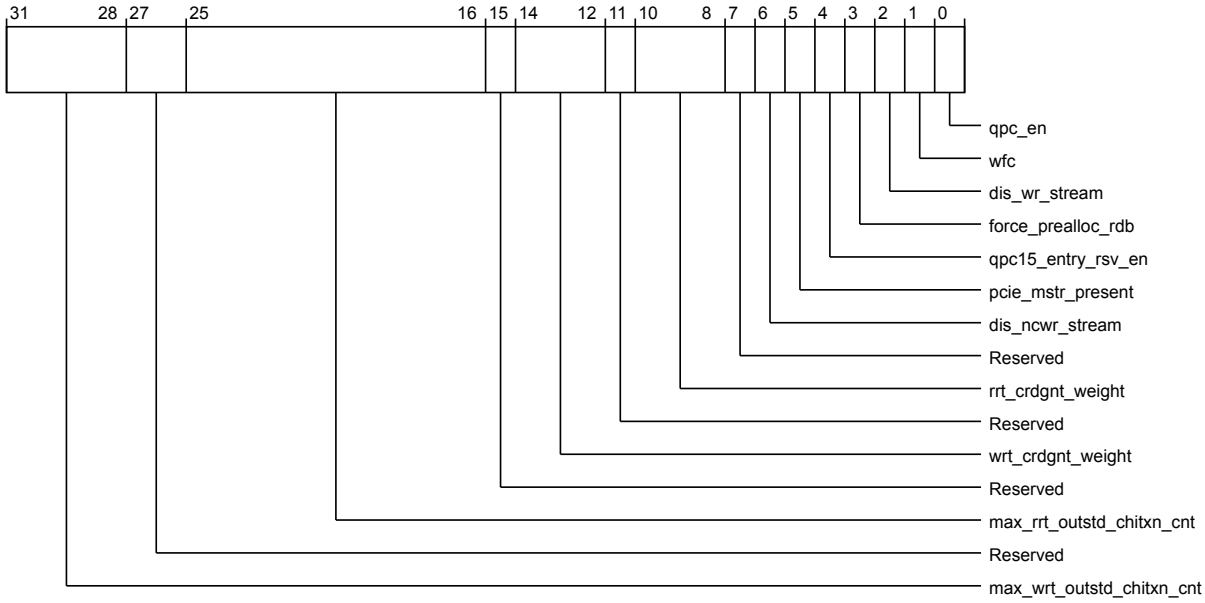


Figure 3-843 por_rni_por_rni_cfg_ctl (low)

The following table shows the por_rni_cfg_ctl lower register bit assignments.

Table 3-857 por_rni_por_rni_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:28	max_wrt_outstd_chitxn_cnt	Maximum number of outstanding writes allowed on CHI-side	RW	Configuration dependent
27:26	Reserved	Reserved	RO	-
25:16	max_rrt_outstd_chitxn_cnt	Maximum number of outstanding reads allowed on CHI-side	RW	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	wrt_crdgnt_weight	Determines weight of credit grant allocated to retried writes in presence of pending retried reads	RW	3'b001
11	Reserved	Reserved	RO	-
10:8	rrt_crdgnt_weight	Determines weight of credit grant allocated to retried reads in presence of pending retried writes	RW	3'b100
7	Reserved	Reserved	RO	-
6	dis_ncwr_stream	Disables streaming of ordered non-cacheable writes when set	RW	1'b0
5	pcie_mstr_present	Indicates PCIe master is present; must be set if PCIe master is present upstream of RN-I or RN-D	RW	1'b0
4	qpc15_entry_rsv_en	Enables QPC15 entry reservation 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests NOTE: Only valid and applicable when por_rni_qpc_en is set	RW	1'b0

Table 3-857 por_rni_por_rni_cfg_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
3	force_prealloc_rdb	When set, all reads from the RN-I are sent with a preallocated read data buffer	RW	Configuration dependent
2	dis_wr_stream	Disables streaming of ordered writes when set	RW	1'b0
1	wfc	When set, enables waiting for completion (COMP) before dispatching dependent transaction (TXN)	RW	1'b0
0	qpc_en	When set, enables QPC-based scheduling using two QoS priority classes (QoS15 and non-QoS15)	RW	1'b1

por_rni_aux_ctl

Functions as the auxiliary control register for RN-I.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

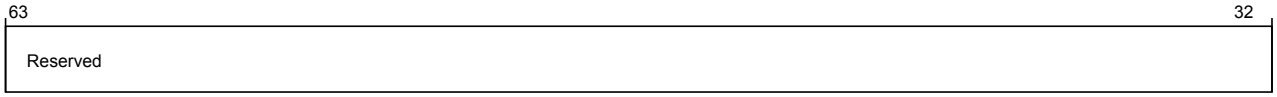


Figure 3-844 por_rni_por_rni_aux_ctl (high)

The following table shows the por_rni_aux_ctl higher register bit assignments.

Table 3-858 por_rni_por_rni_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

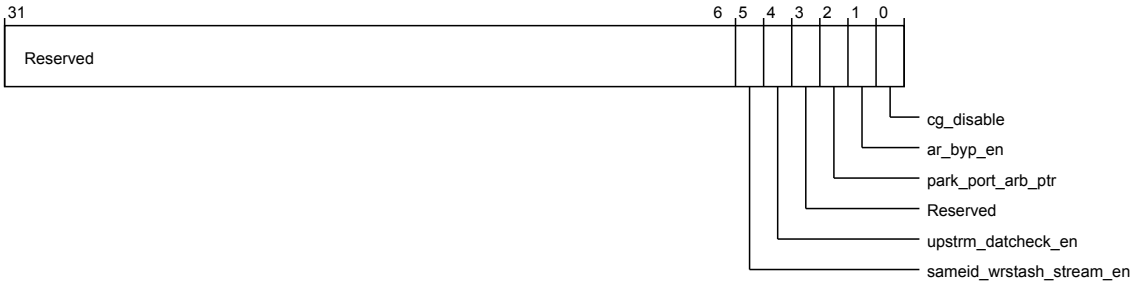


Figure 3-845 por_rni_por_rni_aux_ctl (low)

The following table shows the por_rni_aux_ctl lower register bit assignments.

Table 3-859 por_rni_por_rni_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5	sameid_wrstash_stream_en	Enables streaming of same-ID WrUniqStash	RW	Configuration dependent
4	upstrm_datcheck_en	Upstream supports Datacheck	RW	Configuration dependent
3	Reserved	Reserved	RO	-
2	park_port_arb_ptr	Parks the AXI port arbitration pointer for Burst	RW	1'b0
1	ar_byp_en	AR bypass enable; enables bypass path in the AR pipeline	RW	1'b1
0	cg_disable	Disables clock gating when set	RW	1'b0

por_rni_s0_port_control

Controls port S0 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

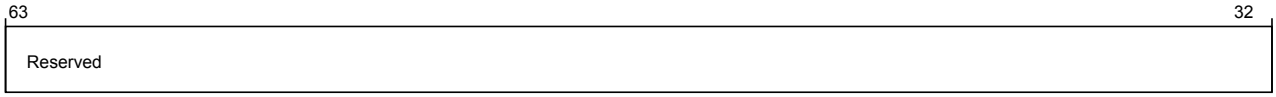


Figure 3-846 por_rni_por_rni_s0_port_control (high)

The following table shows the por_rni_s0_port_control higher register bit assignments.

Table 3-860 por_rni_por_rni_s0_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

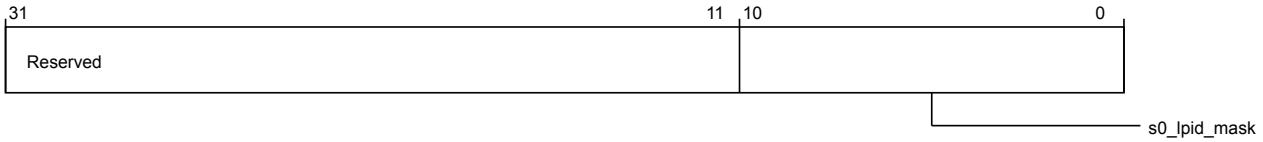


Figure 3-847 por_rni_por_rni_s0_port_control (low)

The following table shows the por_rni_s0_port_control lower register bit assignments.

Table 3-861 por_rni_por_rni_s0_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s0_lpid_mask	Port S0 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s1_port_control

Controls port S1 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

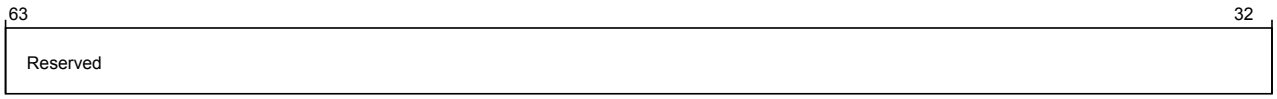


Figure 3-848 por_rni_por_rni_s1_port_control (high)

The following table shows the por_rni_s1_port_control higher register bit assignments.

Table 3-862 por_rni_por_rni_s1_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

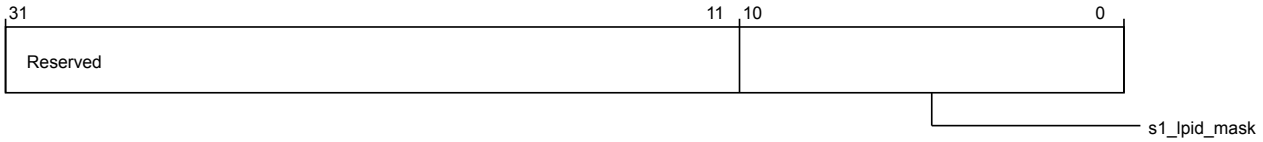


Figure 3-849 por_rni_por_rni_s1_port_control (low)

The following table shows the por_rni_s1_port_control lower register bit assignments.

Table 3-863 por_rni_por_rni_s1_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s1_lpid_mask	Port S1 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s2_port_control

Controls port S2 AXI/ACE slave interface settings.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.port_ctrl

The following image shows the higher register bit assignments.

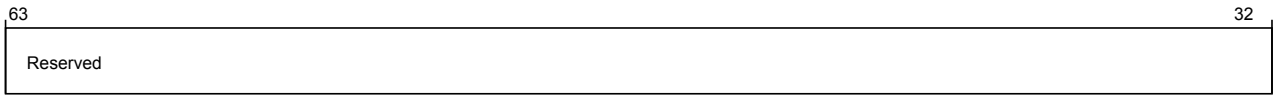


Figure 3-850 por_rni_por_rni_s2_port_control (high)

The following table shows the por_rni_s2_port_control higher register bit assignments.

Table 3-864 por_rni_por_rni_s2_port_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

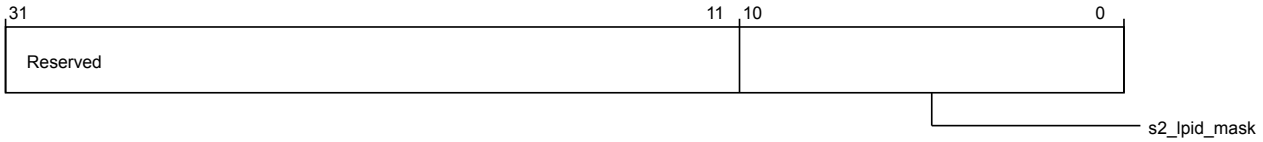


Figure 3-851 por_rni_por_rni_s2_port_control (low)

The following table shows the por_rni_s2_port_control lower register bit assignments.

Table 3-865 por_rni_por_rni_s2_port_control (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:0	s2_lpid_mask	Port S2 LPID mask LPID[0]: Equal to the result of UnaryOR of BitwiseAND of LPID mask and AXID (LPID[0] = (AXID and mask)); specifies which AXID bit is reflected in the LSB of LPID LPID[2:1]: Equal to port ID[1:0]; the MSB of LPID contains port ID	RW	11'b000_0000_0000

por_rni_s0_qos_control

Controls QoS settings for port S0 AXI/ACE slave interface.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

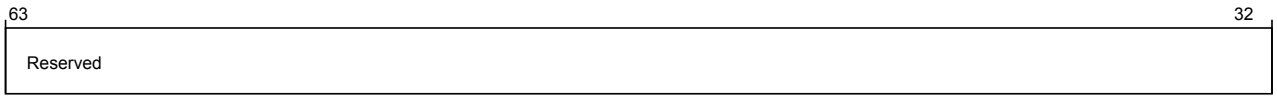


Figure 3-852 por_rni_por_rni_s0_qos_control (high)

The following table shows the por_rni_s0_qos_control higher register bit assignments.

Table 3-866 por_rni_por_rni_s0_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

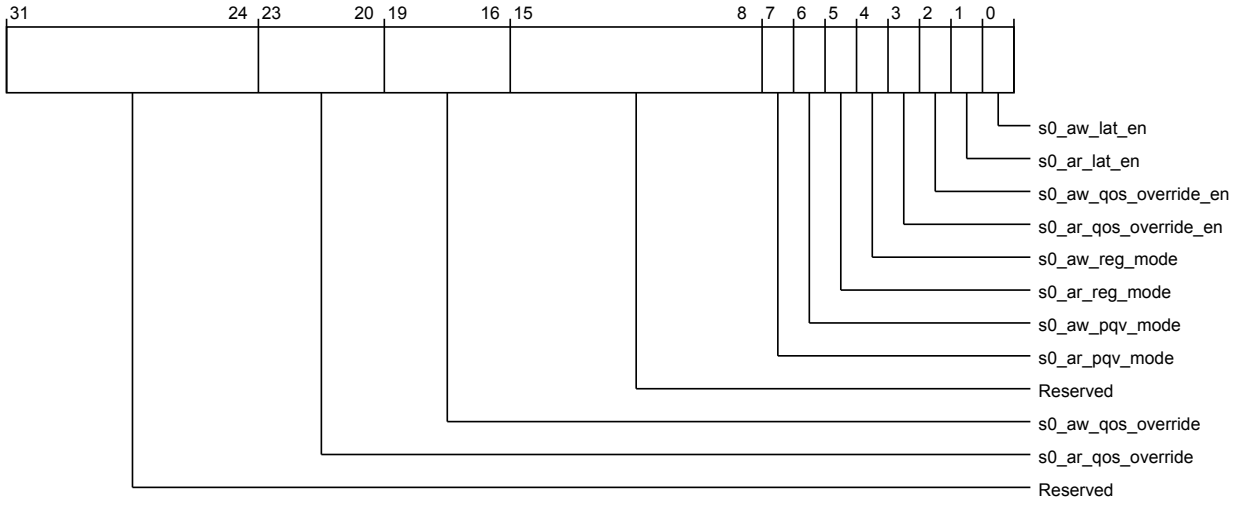


Figure 3-853 por_rni_por_rni_s0_qos_control (low)

The following table shows the por_rni_s0_qos_control lower register bit assignments.

Table 3-867 por_rni_por_rni_s0_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s0_ar_qos_override	AR QoS override value for port S0	RW	4'b0000
19:16	s0_aw_qos_override	AW QoS override value for port S0	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s0_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s0_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s0_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0

Table 3-867 por_rni_por_rni_s0_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
4	s0_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s0_ar_qos_override_en	Enables port S0 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s0_aw_qos_override_en	Enables port S0 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s0_ar_lat_en	Enables port S0 AR QoS regulation when set	RW	1'b0
0	s0_aw_lat_en	Enables port S0 AW QoS regulation when set	RW	1'b0

por_rni_s0_qos_lat_tgt

Controls QoS target latency (in cycles) for regulations of port S0 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

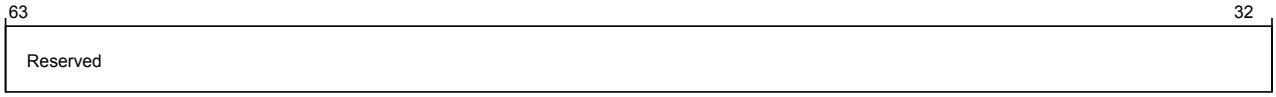


Figure 3-854 por_rni_por_rni_s0_qos_lat_tgt (high)

The following table shows the por_rni_s0_qos_lat_tgt higher register bit assignments.

Table 3-868 por_rni_por_rni_s0_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

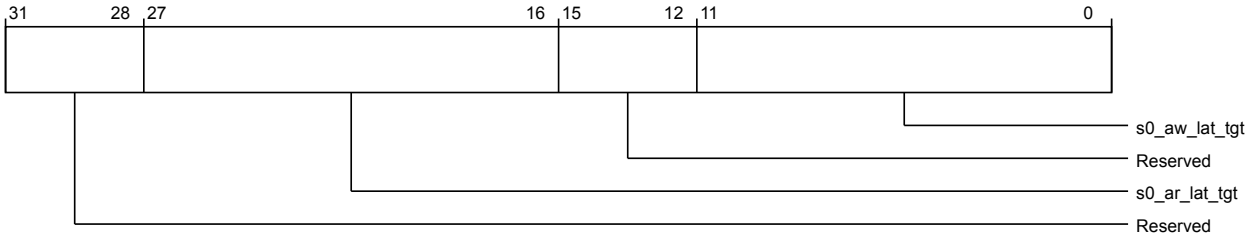


Figure 3-855 por_rni_por_rni_s0_qos_lat_tgt (low)

The following table shows the por_rni_s0_qos_lat_tgt lower register bit assignments.

Table 3-869 por_rni_por_rni_s0_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s0_ar_lat_tgt	Port S0 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s0_aw_lat_tgt	Port S0 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rni_s0_qos_lat_scale

Controls the QoS target latency scale factor for port S0 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

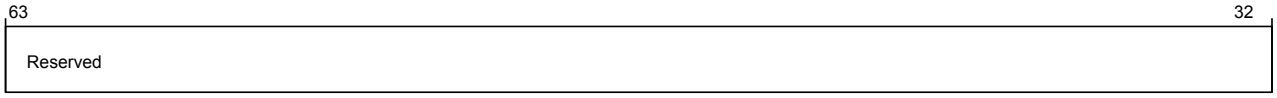


Figure 3-856 por_rni_por_rni_s0_qos_lat_scale (high)

The following table shows the por_rni_s0_qos_lat_scale higher register bit assignments.

Table 3-870 por_rni_por_rni_s0_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

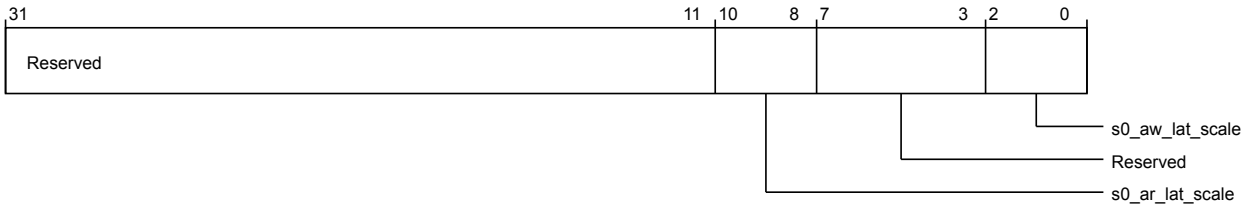


Figure 3-857 por_rni_por_rni_s0_qos_lat_scale (low)

The following table shows the por_rni_s0_qos_lat_scale lower register bit assignments.

Table 3-871 por_rni_por_rni_s0_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s0_ar_lat_scale	Port S0 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s0_aw_lat_scale	Port S0 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rni_s0_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S0 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

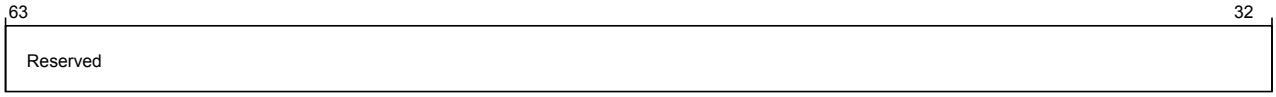


Figure 3-858 por_rni_por_rni_s0_qos_lat_range (high)

The following table shows the por_rni_s0_qos_lat_range higher register bit assignments.

Table 3-872 por_rni_por_rni_s0_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

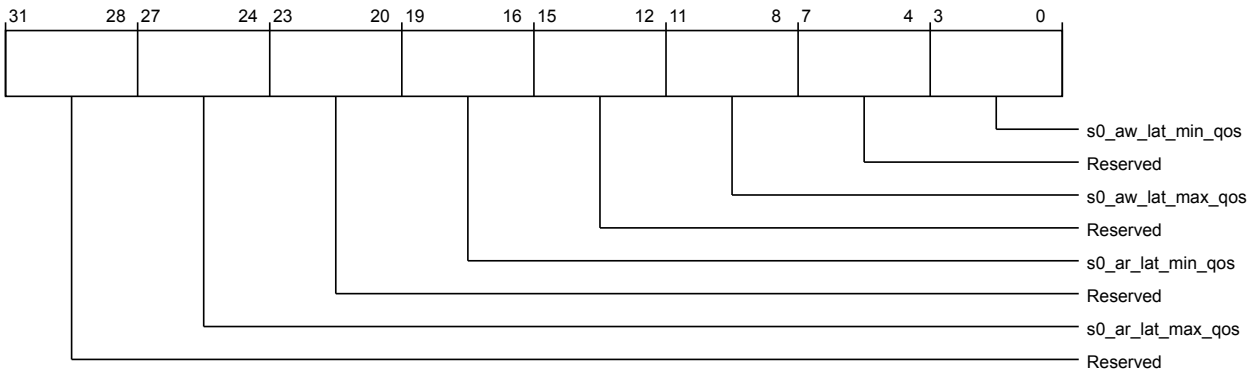


Figure 3-859 por_rni_por_rni_s0_qos_lat_range (low)

The following table shows the por_rni_s0_qos_lat_range lower register bit assignments.

Table 3-873 por_rni_por_rni_s0_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s0_ar_lat_max_qos	Port S0 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s0_ar_lat_min_qos	Port S0 AR QoS minimum value	RW	4'h0

Table 3-873 por_rni_por_rni_s0_qos_lat_range (low) (continued)

Bits	Field name	Description	Type	Reset
15:12	Reserved	Reserved	RO	-
11:8	s0_aw_lat_max_qos	Port S0 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s0_aw_lat_min_qos	Port S0 AW QoS minimum value	RW	4'h0

por_rni_s1_qos_control

Controls QoS settings for port S1 AXI/ACE slave interface.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

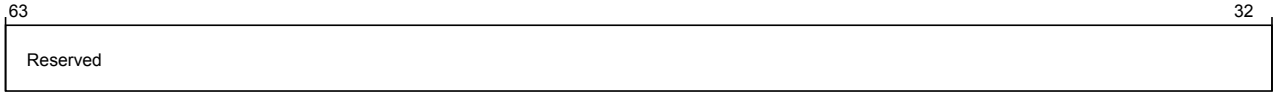


Figure 3-860 por_rni_por_rni_s1_qos_control (high)

The following table shows the por_rni_s1_qos_control higher register bit assignments.

Table 3-874 por_rni_por_rni_s1_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

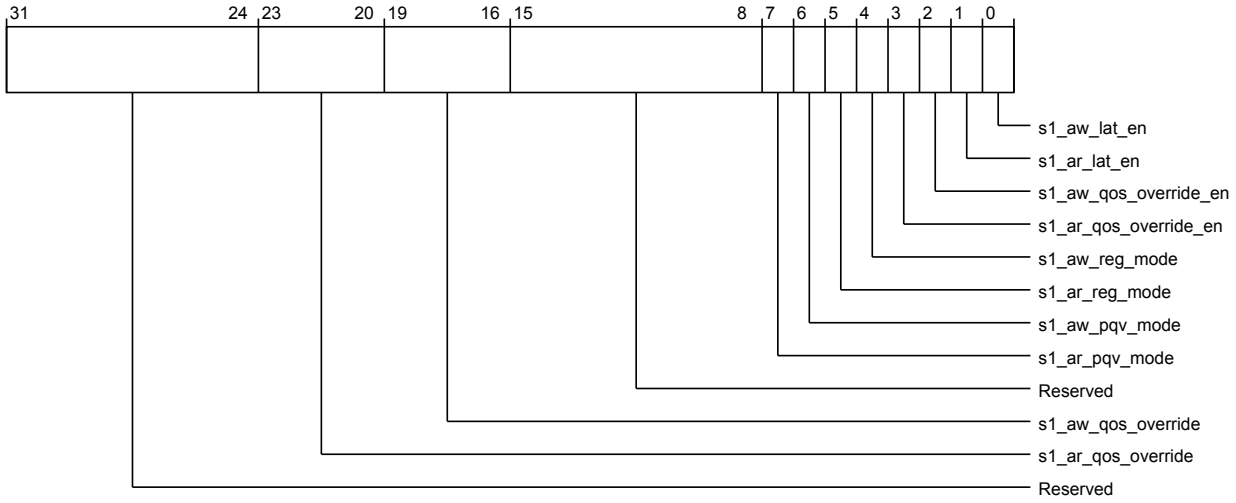


Figure 3-861 por_rni_por_rni_s1_qos_control (low)

The following table shows the por_rni_s1_qos_control lower register bit assignments.

Table 3-875 por_rni_por_rni_s1_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s1_ar_qos_override	AR QoS override value for port S1	RW	4'b0000
19:16	s1_aw_qos_override	AW QoS override value for port S1	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s1_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s1_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s1_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s1_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s1_ar_qos_override_en	Enables port S1 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0

Table 3-875 por_rni_por_rni_s1_qos_control (low) (continued)

Bits	Field name	Description	Type	Reset
2	s1_aw_qos_override_en	Enables port S1 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s1_ar_lat_en	Enables port S1 AR QoS regulation when set	RW	1'b0
0	s1_aw_lat_en	Enables port S1 AW QoS regulation when set	RW	1'b0

por_rni_s1_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

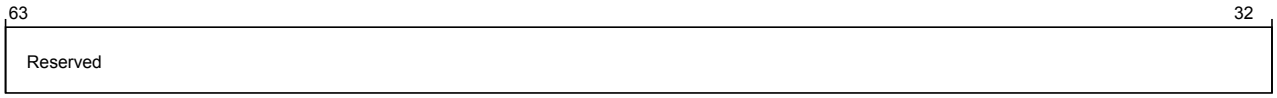


Figure 3-862 por_rni_por_rni_s1_qos_lat_tgt (high)

The following table shows the por_rni_s1_qos_lat_tgt higher register bit assignments.

Table 3-876 por_rni_por_rni_s1_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

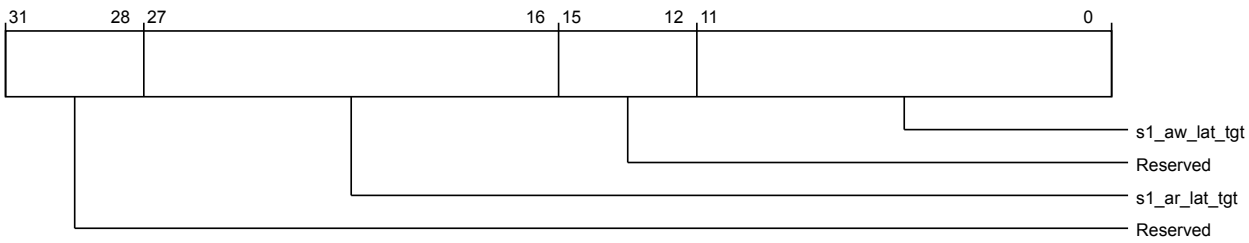


Figure 3-863 por_rni_por_rni_s1_qos_lat_tgt (low)

The following table shows the por_rni_s1_qos_lat_tgt lower register bit assignments.

Table 3-877 por_rni_por_rni_s1_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s1_ar_lat_tgt	Port S1 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s1_aw_lat_tgt	Port S1 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rni_s1_qos_lat_scale

Controls the QoS target latency scale factor for port S1 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

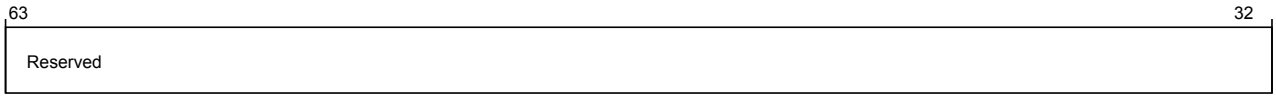


Figure 3-864 por_rni_por_rni_s1_qos_lat_scale (high)

The following table shows the por_rni_s1_qos_lat_scale higher register bit assignments.

Table 3-878 por_rni_por_rni_s1_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

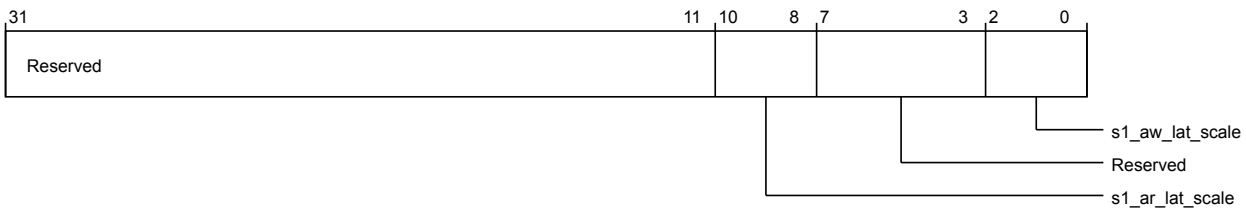


Figure 3-865 por_rni_por_rni_s1_qos_lat_scale (low)

The following table shows the por_rni_s1_qos_lat_scale lower register bit assignments.

Table 3-879 por_rni_por_rni_s1_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s1_ar_lat_scale	Port S1 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0
7:3	Reserved	Reserved	RO	-
2:0	s1_aw_lat_scale	Port S1 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rni_s1_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S1 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

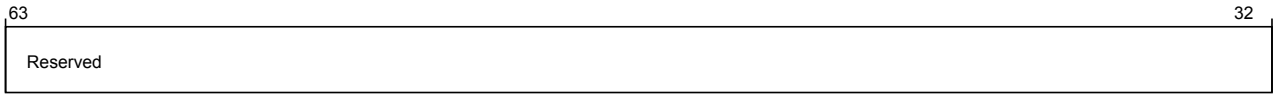


Figure 3-866 por_rni_por_rni_s1_qos_lat_range (high)

The following table shows the por_rni_s1_qos_lat_range higher register bit assignments.

Table 3-880 por_rni_por_rni_s1_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

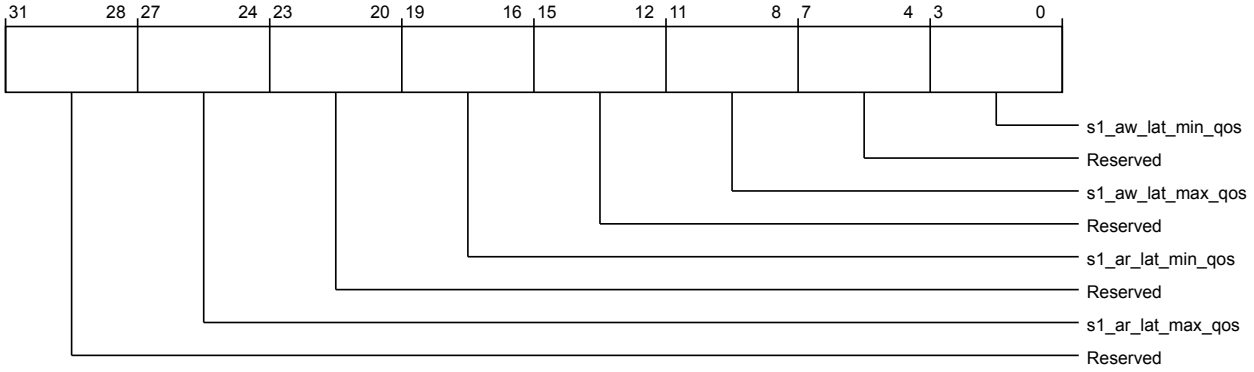


Figure 3-867 por_rni_por_rni_s1_qos_lat_range (low)

The following table shows the por_rni_s1_qos_lat_range lower register bit assignments.

Table 3-881 por_rni_por_rni_s1_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s1_ar_lat_max_qos	Port S1 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s1_ar_lat_min_qos	Port S1 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s1_aw_lat_max_qos	Port S1 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s1_aw_lat_min_qos	Port S1 AW QoS minimum value	RW	4'h0

por_rni_s2_qos_control

Controls QoS settings for port S2 AXI/ACE slave interface.

Its characteristics are:

Type	RW
Register width (Bits)	64
Address offset	14'hAC0
Register reset	64'b0
Usage constraints	Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.
Secure group override	por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

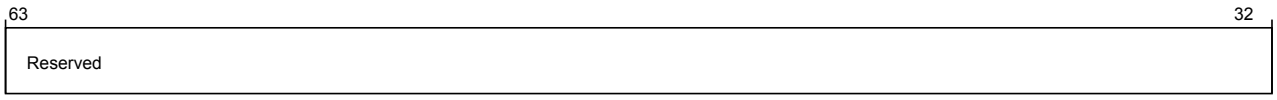


Figure 3-868 por_rni_por_rni_s2_qos_control (high)

The following table shows the por_rni_s2_qos_control higher register bit assignments.

Table 3-882 por_rni_por_rni_s2_qos_control (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

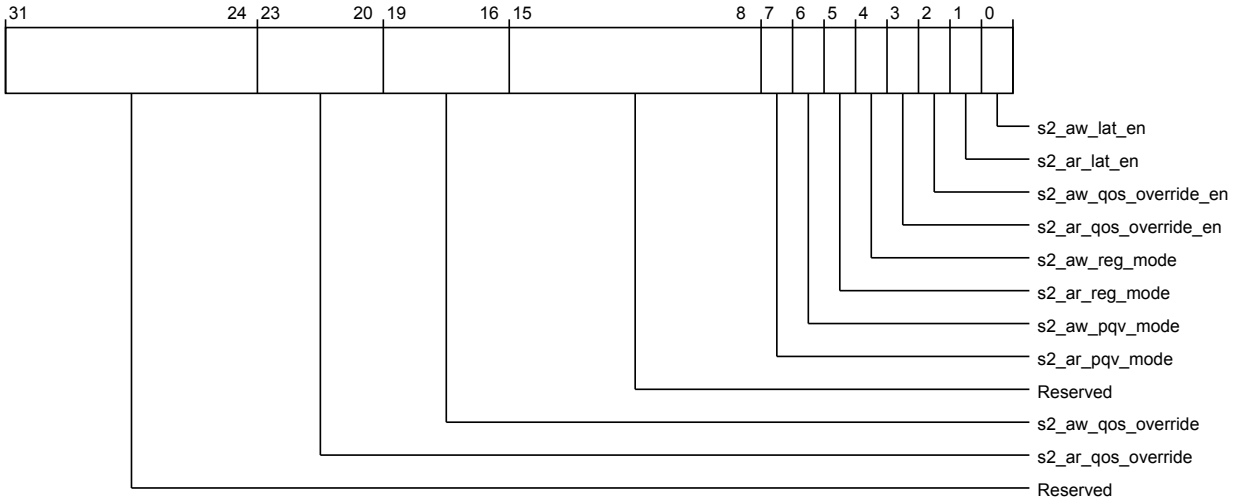


Figure 3-869 por_rni_por_rni_s2_qos_control (low)

The following table shows the por_rni_s2_qos_control lower register bit assignments.

Table 3-883 por_rni_por_rni_s2_qos_control (low)

Bits	Field name	Description	Type	Reset
31:24	Reserved	Reserved	RO	-
23:20	s2_ar_qos_override	AR QoS override value for port S2	RW	4'b0000
19:16	s2_aw_qos_override	AW QoS override value for port S2	RW	4'b0000
15:8	Reserved	Reserved	RO	-
7	s2_ar_pqv_mode	Configures the QoS regulator mode for read transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
6	s2_aw_pqv_mode	Configures the QoS regulator mode for write transactions during period mode 1'b0: Normal mode; QoS value is stable when the master is idle 1'b1: Quiesce high mode; QoS value tends to the maximum value when the master is idle	RW	1'b0
5	s2_ar_reg_mode	Configures the QoS regulator mode for read transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
4	s2_aw_reg_mode	Configures the QoS regulator mode for write transactions 1'b0: Latency mode 1'b1: Period mode; used for bandwidth regulation	RW	1'b0
3	s2_ar_qos_override_en	Enables port S2 AR QoS override; when set, allows QoS value on inbound AR transactions to be overridden	RW	1'b0
2	s2_aw_qos_override_en	Enables port S2 AW QoS override; when set, allows QoS value on inbound AW transactions to be overridden	RW	1'b0
1	s2_ar_lat_en	Enables port S2 AR QoS regulation when set	RW	1'b0
0	s2_aw_lat_en	Enables port S2 AW QoS regulation when set	RW	1'b0

por_rni_s2_qos_lat_tgt

Controls QoS target latency (in cycles) for regulation of port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

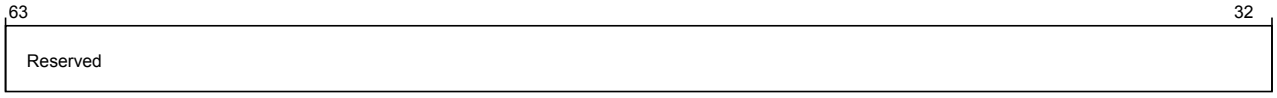


Figure 3-870 por_rni_por_rni_s2_qos_lat_tgt (high)

The following table shows the por_rni_s2_qos_lat_tgt higher register bit assignments.

Table 3-884 por_rni_por_rni_s2_qos_lat_tgt (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

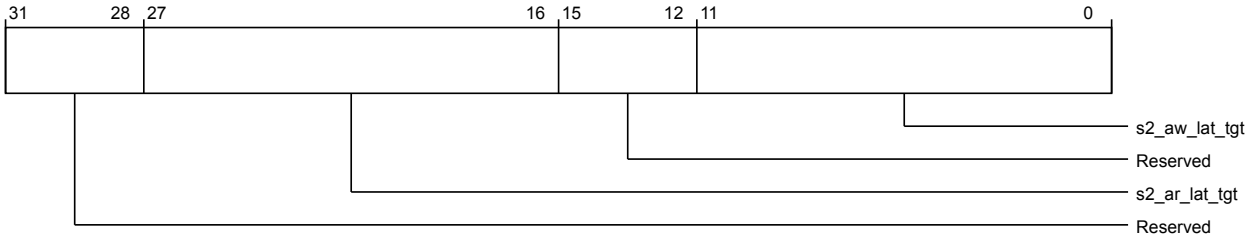


Figure 3-871 por_rni_por_rni_s2_qos_lat_tgt (low)

The following table shows the por_rni_s2_qos_lat_tgt lower register bit assignments.

Table 3-885 por_rni_por_rni_s2_qos_lat_tgt (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:16	s2_ar_lat_tgt	Port S2 AR channel target latency; a value of 0 corresponds to no regulation	RW	12'h000
15:12	Reserved	Reserved	RO	-
11:0	s2_aw_lat_tgt	Port S2 AW channel target latency; a value of 0 corresponds to no regulation	RW	12'h000

por_rni_s2_qos_lat_scale

Controls the QoS target latency scale factor for port S2 read and write transactions. This register represents powers of two from the range 2^(-5) to 2^(-12); it is used to match a 16-bit integrator.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

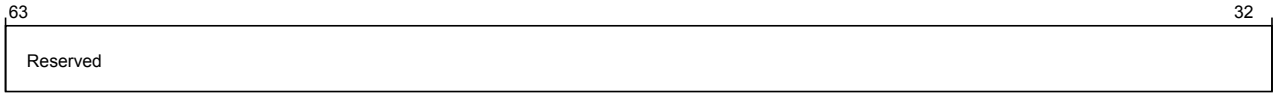


Figure 3-872 por_rni_por_rni_s2_qos_lat_scale (high)

The following table shows the por_rni_s2_qos_lat_scale higher register bit assignments.

Table 3-886 por_rni_por_rni_s2_qos_lat_scale (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

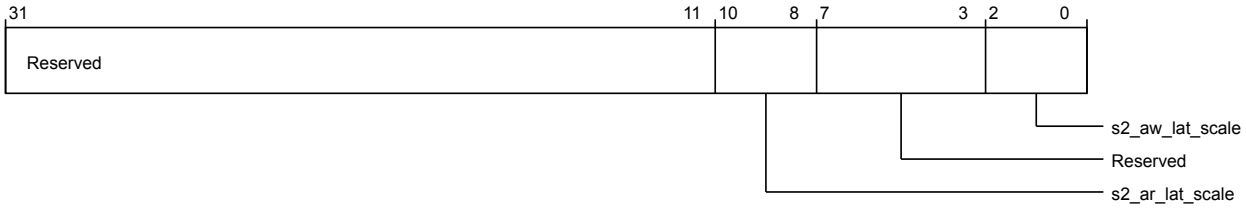


Figure 3-873 por_rni_por_rni_s2_qos_lat_scale (low)

The following table shows the por_rni_s2_qos_lat_scale lower register bit assignments.

Table 3-887 por_rni_por_rni_s2_qos_lat_scale (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10:8	s2_ar_lat_scale	Port S2 AR QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

Table 3-887 por_rni_por_rni_s2_qos_lat_scale (low) (continued)

Bits	Field name	Description	Type	Reset
7:3	Reserved	Reserved	RO	-
2:0	s2_aw_lat_scale	Port S2 AW QoS scale factor 3'b000: 2^(-5) 3'b001: 2^(-6) 3'b010: 2^(-7) 3'b011: 2^(-8) 3'b100: 2^(-9) 3'b101: 2^(-10) 3'b110: 2^(-11) 3'b111: 2^(-12)	RW	3'h0

por_rni_s2_qos_lat_range

Controls the minimum and maximum QoS values generated by the QoS latency regulator for port S2 read and write transactions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hAD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rni_secure_register_groups_override.qos_ctrl

The following image shows the higher register bit assignments.

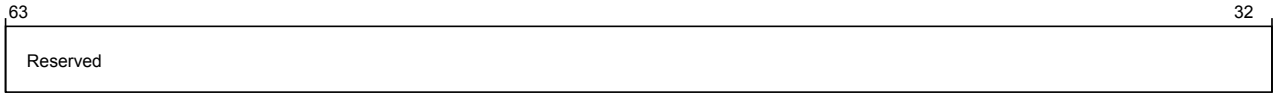


Figure 3-874 por_rni_por_rni_s2_qos_lat_range (high)

The following table shows the por_rni_s2_qos_lat_range higher register bit assignments.

Table 3-888 por_rni_por_rni_s2_qos_lat_range (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

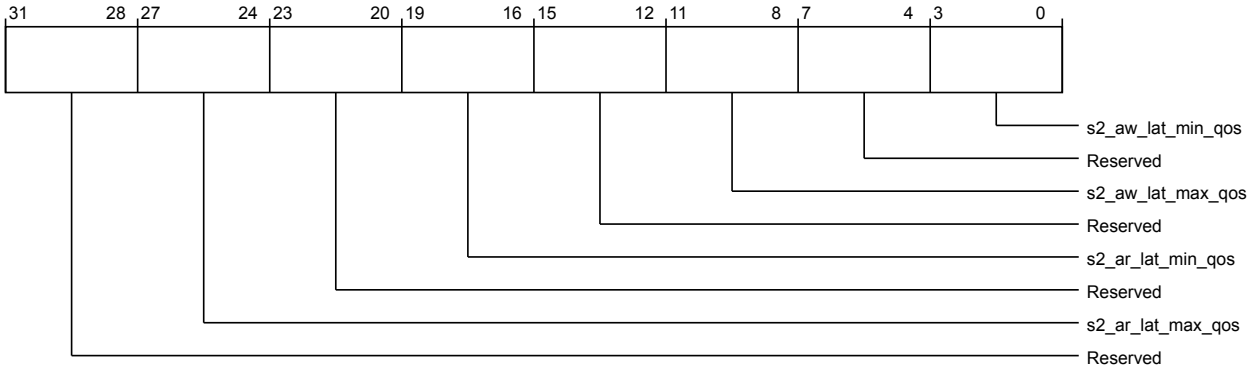


Figure 3-875 por_rni_por_rni_s2_qos_lat_range (low)

The following table shows the por_rni_s2_qos_lat_range lower register bit assignments.

Table 3-889 por_rni_por_rni_s2_qos_lat_range (low)

Bits	Field name	Description	Type	Reset
31:28	Reserved	Reserved	RO	-
27:24	s2_ar_lat_max_qos	Port S2 AR QoS maximum value	RW	4'h0
23:20	Reserved	Reserved	RO	-
19:16	s2_ar_lat_min_qos	Port S2 AR QoS minimum value	RW	4'h0
15:12	Reserved	Reserved	RO	-
11:8	s2_aw_lat_max_qos	Port S2 AW QoS maximum value	RW	4'h0
7:4	Reserved	Reserved	RO	-
3:0	s2_aw_lat_min_qos	Port S2 AW QoS minimum value	RW	4'h0

por_rni_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

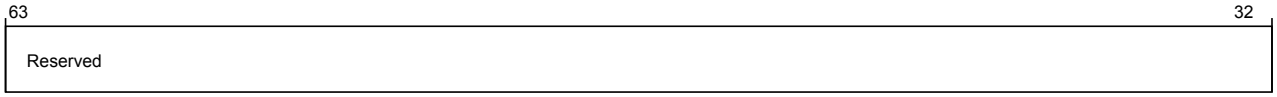


Figure 3-876 por_rni_por_rni_pmu_event_sel (high)

The following table shows the por_rni_pmu_event_sel higher register bit assignments.

Table 3-890 por_rni_por_rni_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

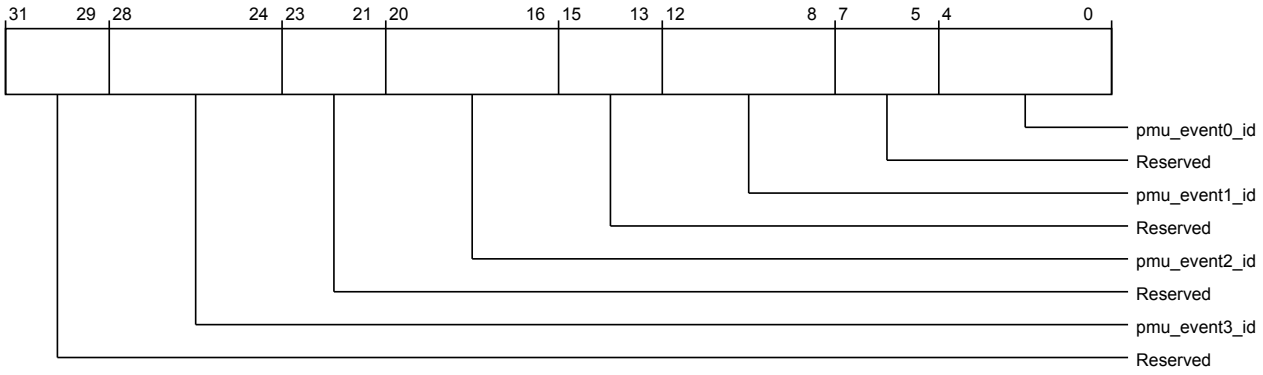


Figure 3-877 por_rni_por_rni_pmu_event_sel (low)

The following table shows the por_rni_pmu_event_sel lower register bit assignments.

Table 3-891 por_rni_por_rni_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	RN-I PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	RN-I PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	RN-I PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 3-891 por_rni_por_rni_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	pmu_event0_id	RN-I PMU Event 0 ID 5'h00: No event 5'h01: Port S0 RDataBeats 5'h02: Port S1 RDataBeats 5'h03: Port S2 RDataBeats 5'h04: RXDAT flits received 5'h05: TXDAT flits sent 5'h06: Total TXREQ flits sent 5'h07: Retried TXREQ flits sent 5'h08: RRT occupancy count overflow 5'h09: WRT occupancy count overflow 5'h0A: Replayed TXREQ flits 5'h0B: WriteCancel sent 5'h0C: Port S0 WDataBeats 5'h0D: Port S1 WDataBeats 5'h0E: Port S2 WDataBeats 5'h0F: RRT allocation 5'h10: WRT allocation 5'h11: RDB pool state is all unordered 5'h12: RDB pool state is replay 5'h13: RDB pool state is hybrid 5'h14: RDB pool state is all ordered	RW	5'b0

3.3.9 RN SAM register descriptions

Lists the RN SAM registers.

por_rnsam_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

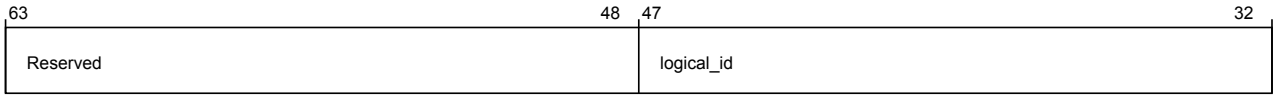


Figure 3-878 por_rnsam_por_rnsam_node_info (high)

The following table shows the por_rnsam_node_info higher register bit assignments.

Table 3-892 por_rnsam_por_rnsam_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID NOTE: RN SAM logical ID is always set to 16'b0.	RO	16'h0

The following image shows the lower register bit assignments.

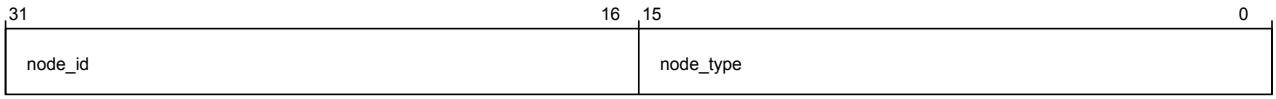


Figure 3-879 por_rnsam_por_rnsam_node_info (low)

The following table shows the por_rnsam_node_info lower register bit assignments.

Table 3-893 por_rnsam_por_rnsam_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h000F

por_rnsam_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

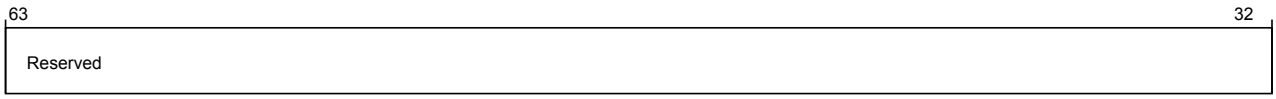


Figure 3-880 por_rnsam_por_rnsam_child_info (high)

The following table shows the por_rnsam_child_info higher register bit assignments.

Table 3-894 por_rnsam_por_rnsam_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

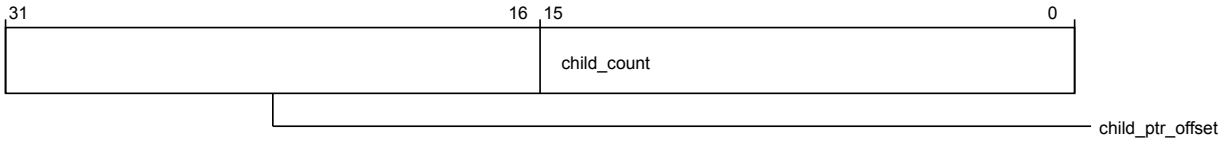


Figure 3-881 por_rnsam_por_rnsam_child_info (low)

The following table shows the por_rnsam_child_info lower register bit assignments.

Table 3-895 por_rnsam_por_rnsam_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_rnsam_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

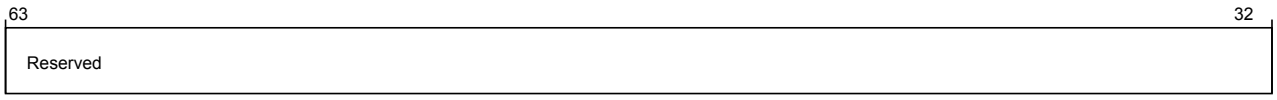


Figure 3-882 por_rnsam_por_rnsam_secure_register_groups_override (high)

The following table shows the por_rnsam_secure_register_groups_override higher register bit assignments.

Table 3-896 por_rnsam_por_rnsam_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

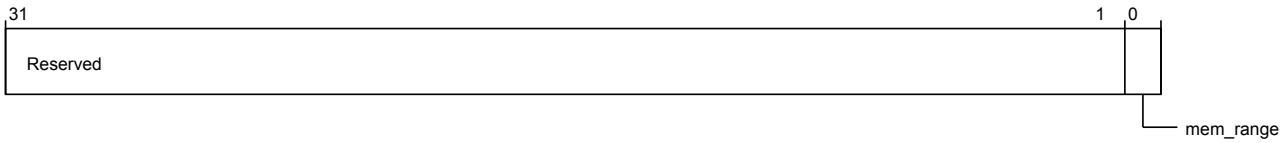


Figure 3-883 por_rnsam_por_rnsam_secure_register_groups_override (low)

The following table shows the por_rnsam_secure_register_groups_override lower register bit assignments.

Table 3-897 por_rnsam_por_rnsam_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	mem_range	Allows non-secure access to secure mem_ranges registers	RW	1'b0

por_rnsam_unit_info

Provides component identification information for RN SAM.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

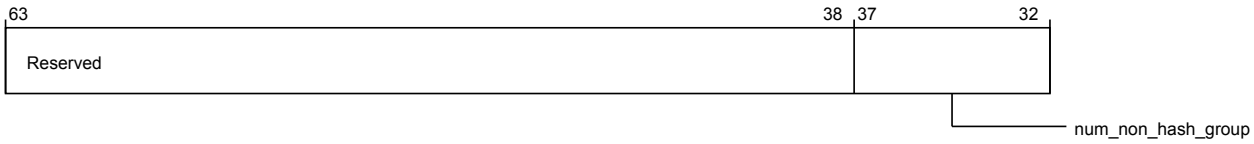


Figure 3-884 por_rnsam_por_rnsam_unit_info (high)

The following table shows the por_rnsam_unit_info higher register bit assignments.

Table 3-898 por_rnsam_por_rnsam_unit_info (high)

Bits	Field name	Description	Type	Reset
63:38	Reserved	Reserved	RO	-
37:32	num_non_hash_group	Number of non-hashed groups supported	RO	Configuration dependent

The following image shows the lower register bit assignments.

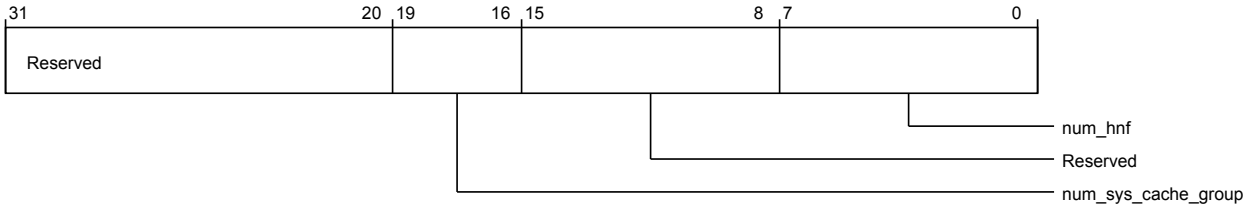


Figure 3-885 por_rnsam_por_rnsam_unit_info (low)

The following table shows the por_rnsam_unit_info lower register bit assignments.

Table 3-899 por_rnsam_por_rnsam_unit_info (low)

Bits	Field name	Description	Type	Reset
31:20	Reserved	Reserved	RO	-
19:16	num_sys_cache_group	Number of system cache groups supported	RO	Configuration dependent
15:8	Reserved	Reserved	RO	-
7:0	num_hnf	Number of hashed targets supported	RO	Configuration dependent

rnsam_status

Functions as the default and programming mode status register.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC00
Register reset 64'b01

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

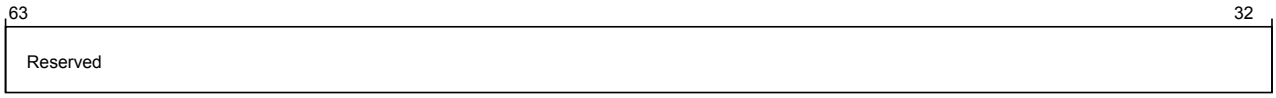


Figure 3-886 por_rnsam_rnsam_status (high)

The following table shows the rnsam_status higher register bit assignments.

Table 3-900 por_rnsam_rnsam_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

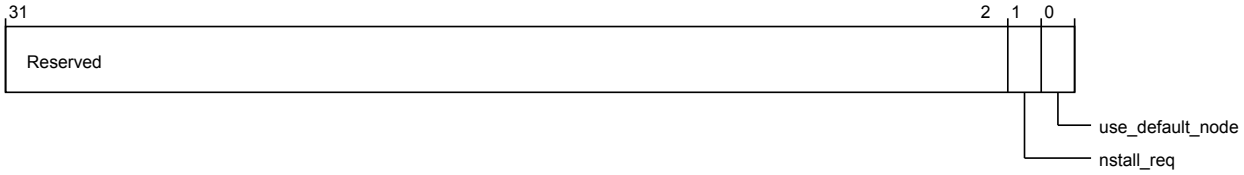


Figure 3-887 por_rnsam_rnsam_status (low)

The following table shows the rnsam_status lower register bit assignments.

Table 3-901 por_rnsam_rnsam_status (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	nstall_req	Indicates RN SAM is programmed and ready 1'b0: STALL requests 1'b1: UNSTALL requests	RW	1'b0
0	use_default_node	Indicates target ID selection mode 1'b0: Enables RN SAM to hash address bits and generate target ID 1'b1: Uses default target ID	RW	1'b1

non_hash_mem_region_reg0

Configures non-hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

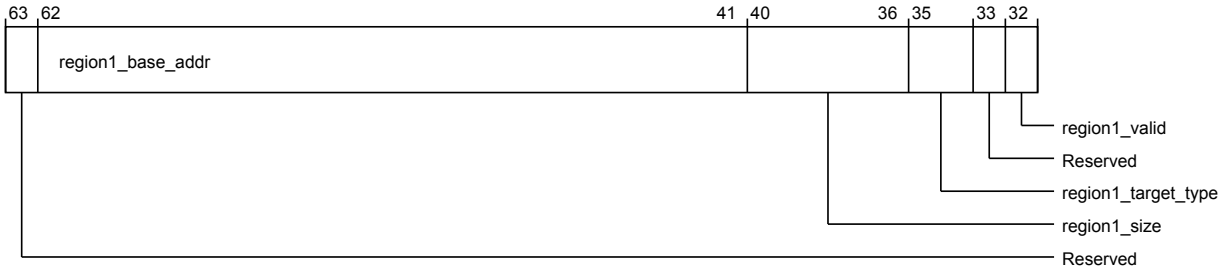


Figure 3-888 por_rnsam_non_hash_mem_region_reg0 (high)

The following table shows the non_hash_mem_region_reg0 higher register bit assignments.

Table 3-902 por_rnsam_non_hash_mem_region_reg0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region1_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b0000000000000000000000
40:36	region1_size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region1_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region1_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

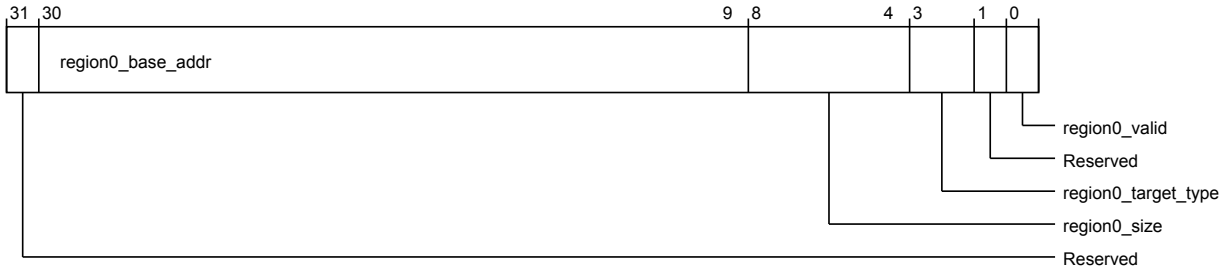


Figure 3-889 por_rnsam_non_hash_mem_region_reg0 (low)

The following table shows the non_hash_mem_region_reg0 lower register bit assignments.

Table 3-903 por_rnsam_non_hash_mem_region_reg0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b0000000000000000000000
8:4	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg1

Configures non-hashed memory regions 2 and 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC10
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

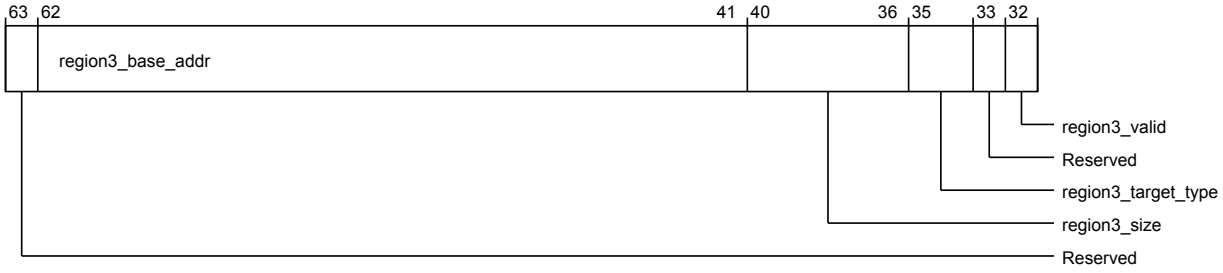


Figure 3-890 por_rnsam_non_hash_mem_region_reg1 (high)

The following table shows the non_hash_mem_region_reg1 higher register bit assignments.

Table 3-904 por_rnsam_non_hash_mem_region_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b0000000000000000000000
40:36	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

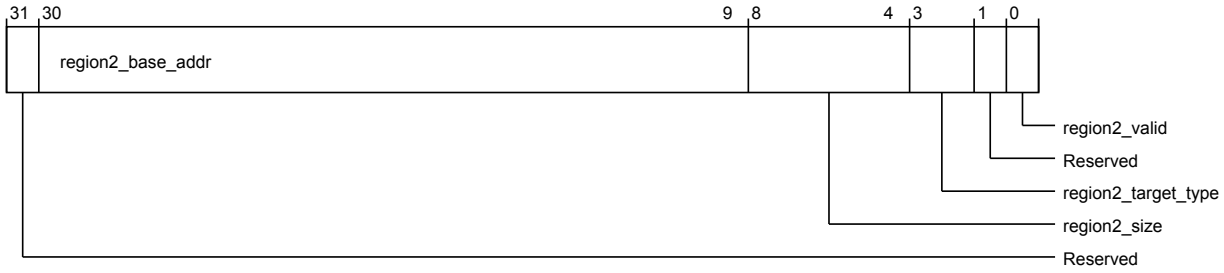


Figure 3-891 por_rnsam_non_hash_mem_region_reg1 (low)

The following table shows the non_hash_mem_region_reg1 lower register bit assignments.

Table 3-905 por_rnsam_non_hash_mem_region_reg1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region2_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b0000000000000000000000
8:4	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg2

Configures non-hashed memory regions 4 and 5.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC18
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

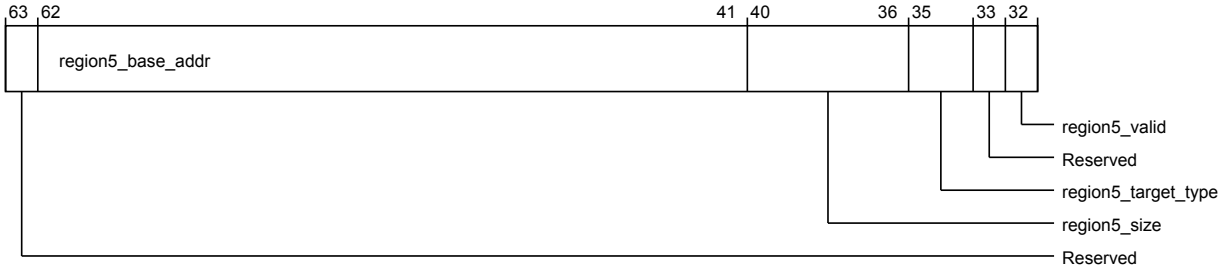


Figure 3-892 por_rnsam_non_hash_mem_region_reg2 (high)

The following table shows the non_hash_mem_region_reg2 higher register bit assignments.

Table 3-906 por_rnsam_non_hash_mem_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region5_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 5 size	RW	22'b0000000000000000000000
40:36	region5_size	Memory region 5 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region5_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region5_valid	Memory region 5 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

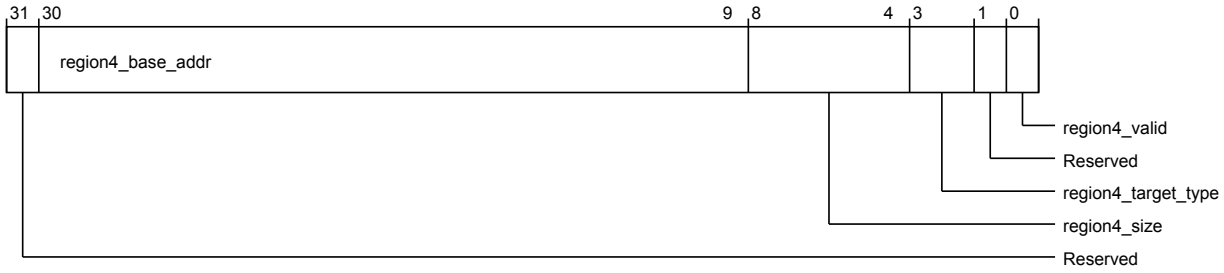


Figure 3-893 por_rnsam_non_hash_mem_region_reg2 (low)

The following table shows the non_hash_mem_region_reg2 lower register bit assignments.

Table 3-907 por_rnsam_non_hash_mem_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region4_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 4 size	RW	22'b0000000000000000000000
8:4	region4_size	Memory region 4 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region4_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region4_valid	Memory region 4 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg3

Configures non-hashed memory regions 6 and 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC20
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

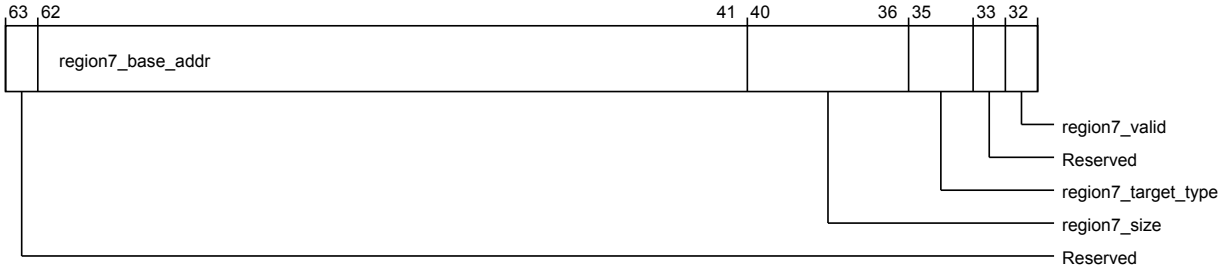


Figure 3-894 por_rnsam_non_hash_mem_region_reg3 (high)

The following table shows the non_hash_mem_region_reg3 higher register bit assignments.

Table 3-908 por_rnsam_non_hash_mem_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region7_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 7 size	RW	22'b0000000000000000000000
40:36	region7_size	Memory region 7 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region7_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region7_valid	Memory region 7 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

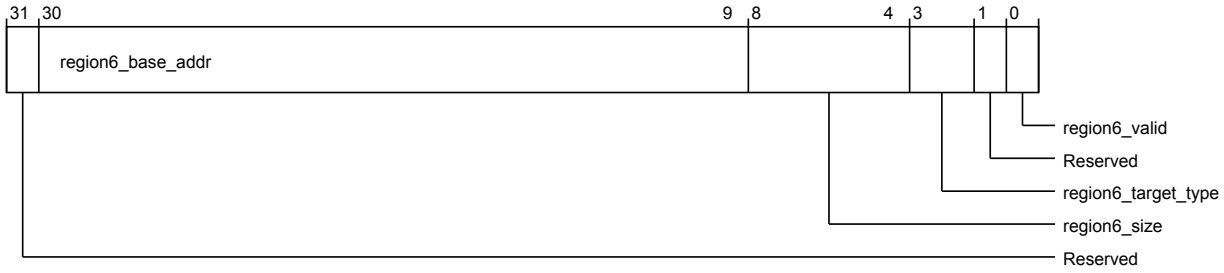


Figure 3-895 por_rnsam_non_hash_mem_region_reg3 (low)

The following table shows the non_hash_mem_region_reg3 lower register bit assignments.

Table 3-909 por_rnsam_non_hash_mem_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region6_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 6 size	RW	22'b0000000000000000000000
8:4	region6_size	Memory region 6 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region6_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region6_valid	Memory region 6 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg4

Configures non-hashed memory regions 8 and 9.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC28
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

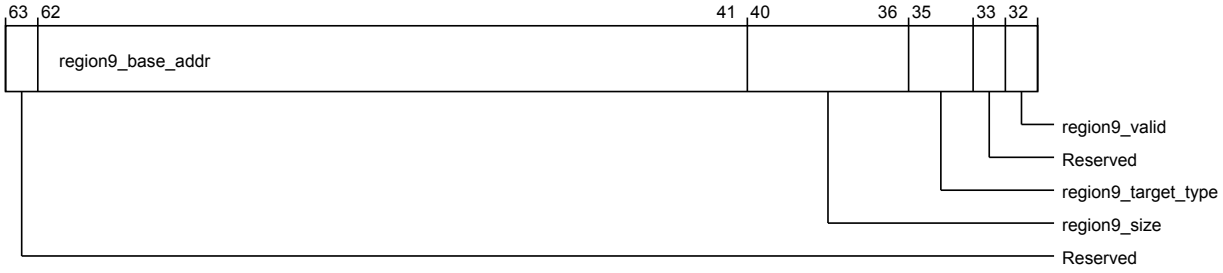


Figure 3-896 por_rnsam_non_hash_mem_region_reg4 (high)

The following table shows the non_hash_mem_region_reg4 higher register bit assignments.

Table 3-910 por_rnsam_non_hash_mem_region_reg4 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region9_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 9 size	RW	22'b0000000000000000000000
40:36	region9_size	Memory region 9 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region9_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region9_valid	Memory region 9 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

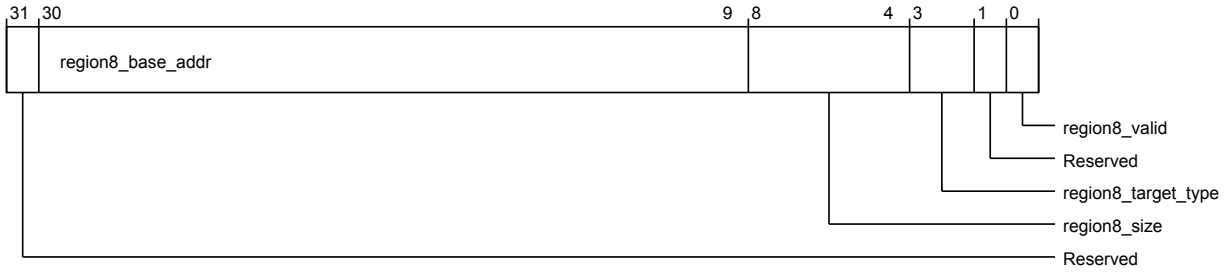


Figure 3-897 por_rnsam_non_hash_mem_region_reg4 (low)

The following table shows the non_hash_mem_region_reg4 lower register bit assignments.

Table 3-911 por_rnsam_non_hash_mem_region_reg4 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region8_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 8 size	RW	22'b0000000000000000000000
8:4	region8_size	Memory region 8 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region8_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region8_valid	Memory region 8 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg5

Configures non-hashed memory regions 10 and 11.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hCA0
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

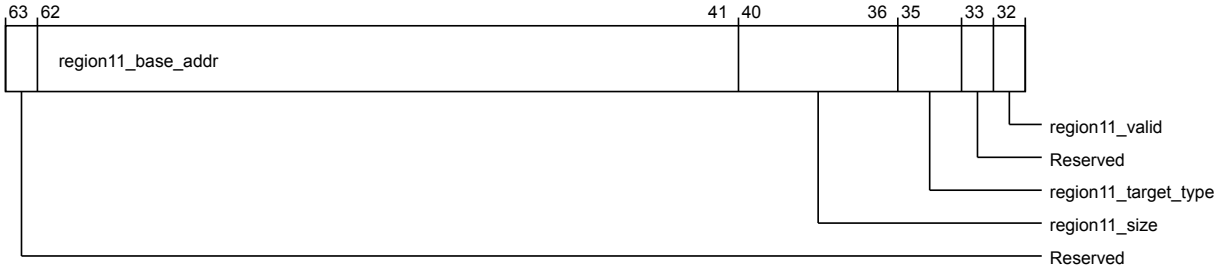


Figure 3-898 por_rnsam_non_hash_mem_region_reg5 (high)

The following table shows the non_hash_mem_region_reg5 higher register bit assignments.

Table 3-912 por_rnsam_non_hash_mem_region_reg5 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region11_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 11 size	RW	22'b0000000000000000000000
40:36	region11_size	Memory region 11 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region11_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region11_valid	Memory region 11 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

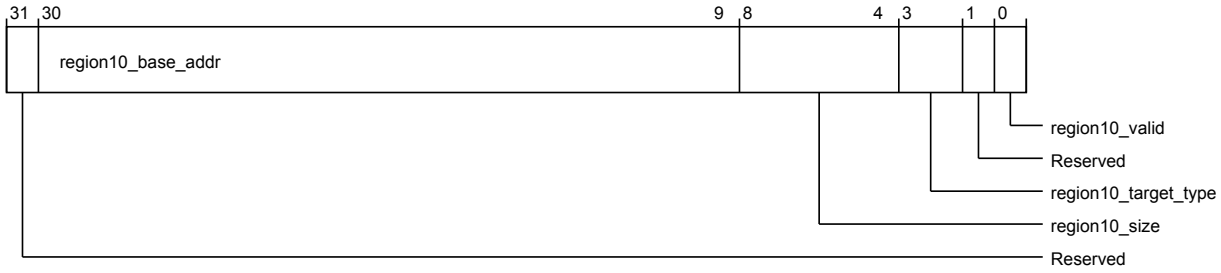


Figure 3-899 por_rnsam_non_hash_mem_region_reg5 (low)

The following table shows the non_hash_mem_region_reg5 lower register bit assignments.

Table 3-913 por_rnsam_non_hash_mem_region_reg5 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region10_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 10 size	RW	22'b0000000000000000000000
8:4	region10_size	Memory region 10 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region10_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region10_valid	Memory region 10 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg6

Configures non-hashed memory regions 12 and 13.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hCA8
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

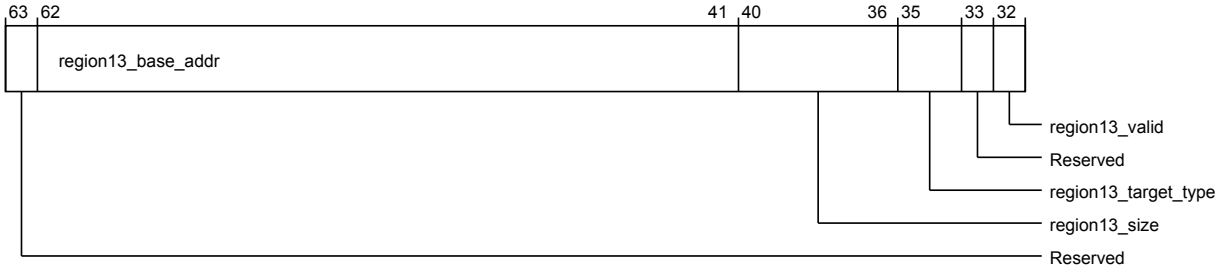


Figure 3-900 por_rnsam_non_hash_mem_region_reg6 (high)

The following table shows the non_hash_mem_region_reg6 higher register bit assignments.

Table 3-914 por_rnsam_non_hash_mem_region_reg6 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region13_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 13 size	RW	22'b0000000000000000000000
40:36	region13_size	Memory region 13 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region13_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region13_valid	Memory region 13 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

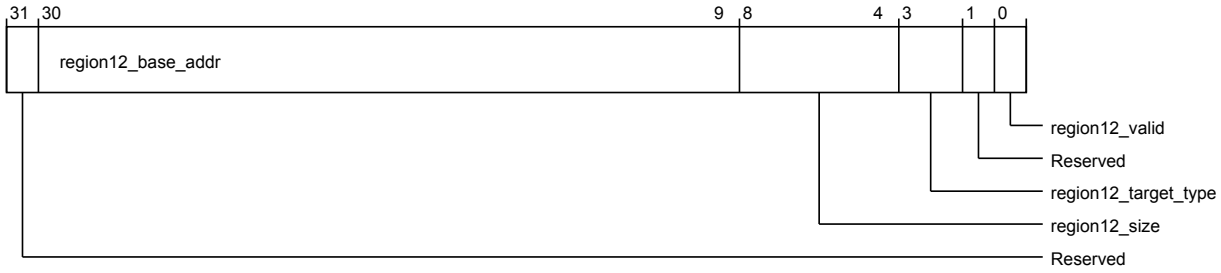


Figure 3-901 por_rnsam_non_hash_mem_region_reg6 (low)

The following table shows the non_hash_mem_region_reg6 lower register bit assignments.

Table 3-915 por_rnsam_non_hash_mem_region_reg6 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region12_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 12 size	RW	22'b0000000000000000000000
8:4	region12_size	Memory region 12 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region12_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region12_valid	Memory region 12 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg7

Configures non-hashed memory regions 14 and 15.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hCB0
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

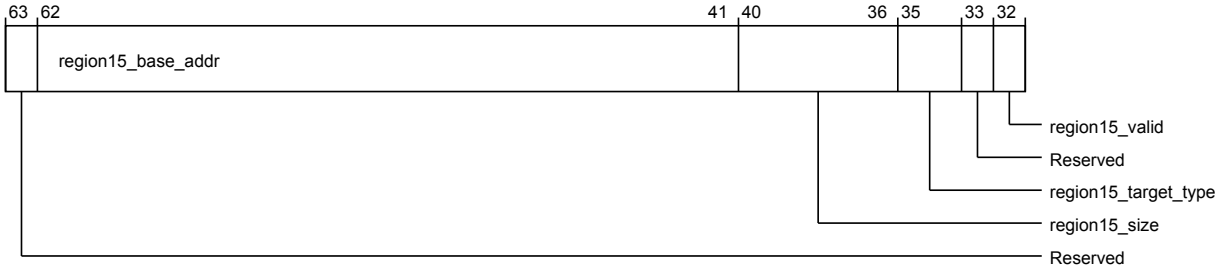


Figure 3-902 por_rnsam_non_hash_mem_region_reg7 (high)

The following table shows the non_hash_mem_region_reg7 higher register bit assignments.

Table 3-916 por_rnsam_non_hash_mem_region_reg7 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region15_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 15 size	RW	22'b0000000000000000000000
40:36	region15_size	Memory region 15 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region15_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region15_valid	Memory region 15 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

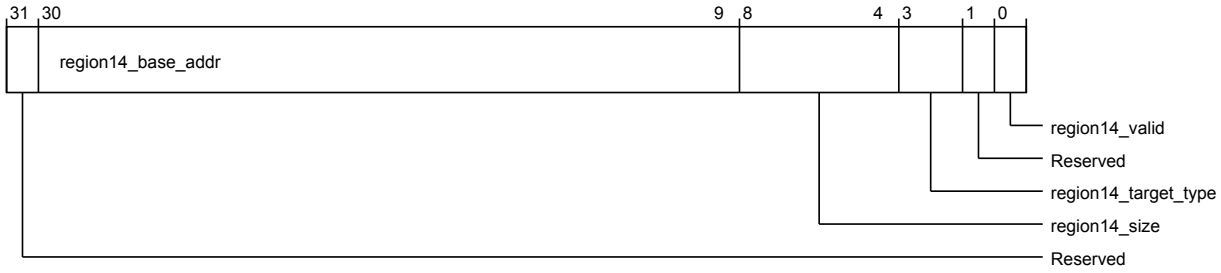


Figure 3-903 por_rnsam_non_hash_mem_region_reg7 (low)

The following table shows the non_hash_mem_region_reg7 lower register bit assignments.

Table 3-917 por_rnsam_non_hash_mem_region_reg7 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region14_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 14 size	RW	22'b0000000000000000000000
8:4	region14_size	Memory region 14 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region14_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region14_valid	Memory region 14 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg8

Configures non-hashed memory regions 16 and 17.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hCB8
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

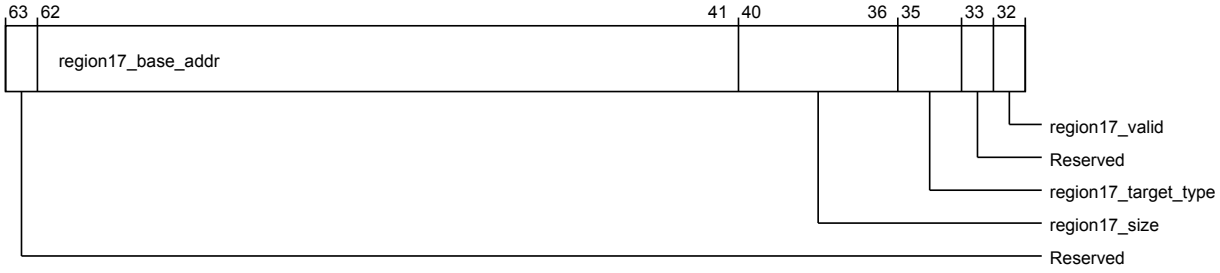


Figure 3-904 por_rnsam_non_hash_mem_region_reg8 (high)

The following table shows the non_hash_mem_region_reg8 higher register bit assignments.

Table 3-918 por_rnsam_non_hash_mem_region_reg8 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region17_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 17 size	RW	22'b0000000000000000000000
40:36	region17_size	Memory region 17 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region17_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region17_valid	Memory region 17 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

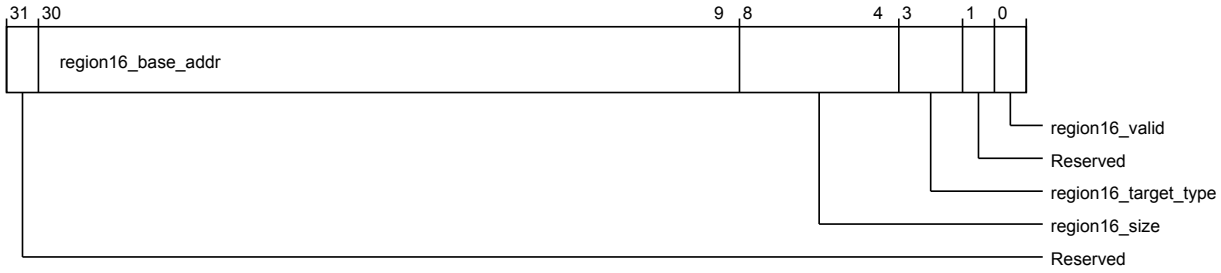


Figure 3-905 por_rnsam_non_hash_mem_region_reg8 (low)

The following table shows the non_hash_mem_region_reg8 lower register bit assignments.

Table 3-919 por_rnsam_non_hash_mem_region_reg8 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region16_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 16 size	RW	22'b0000000000000000000000
8:4	region16_size	Memory region 16 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region16_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region16_valid	Memory region 16 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_mem_region_reg9

Configures non-hashed memory regions 18 and 19.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hCC0
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

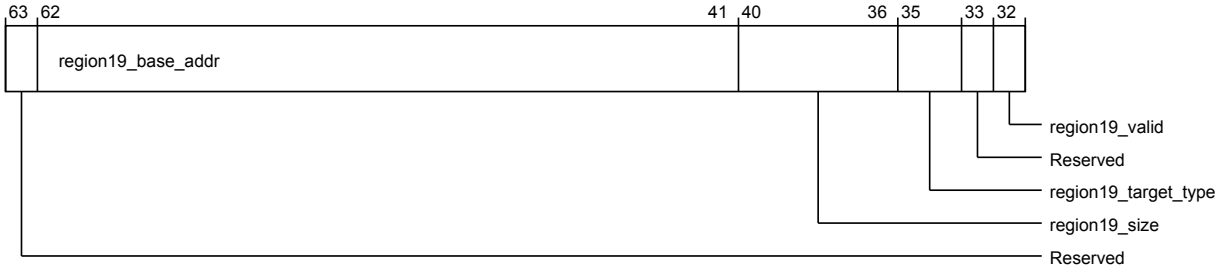


Figure 3-906 por_rnsam_non_hash_mem_region_reg9 (high)

The following table shows the non_hash_mem_region_reg9 higher register bit assignments.

Table 3-920 por_rnsam_non_hash_mem_region_reg9 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region19_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 19 size	RW	22'b0000000000000000000000
40:36	region19_size	Memory region 19 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region19_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region19_valid	Memory region 19 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

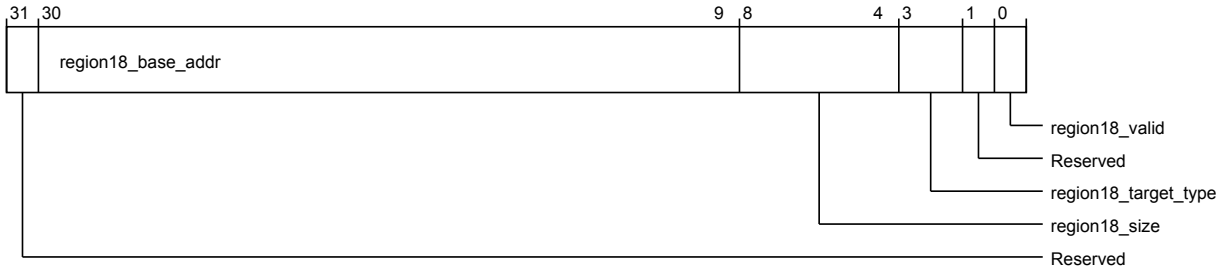


Figure 3-907 por_rnsam_non_hash_mem_region_reg9 (low)

The following table shows the non_hash_mem_region_reg9 lower register bit assignments.

Table 3-921 por_rnsam_non_hash_mem_region_reg9 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region18_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 18 size	RW	22'b0000000000000000000000
8:4	region18_size	Memory region 18 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region18_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region18_valid	Memory region 18 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

non_hash_tgt_nodeid0

Configures non-hashed target node IDs 0 to 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC30
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

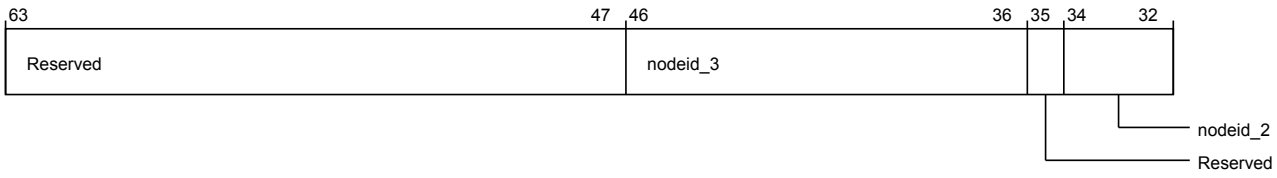


Figure 3-908 por_rnsam_non_hash_tgt_nodeid0 (high)

The following table shows the non_hash_tgt_nodeid0 higher register bit assignments.

Table 3-922 por_rnsam_non_hash_tgt_nodeid0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_3	Non-hashed target node ID 3	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_2	Non-hashed target node ID 2	RW	11'b00000000000

The following image shows the lower register bit assignments.

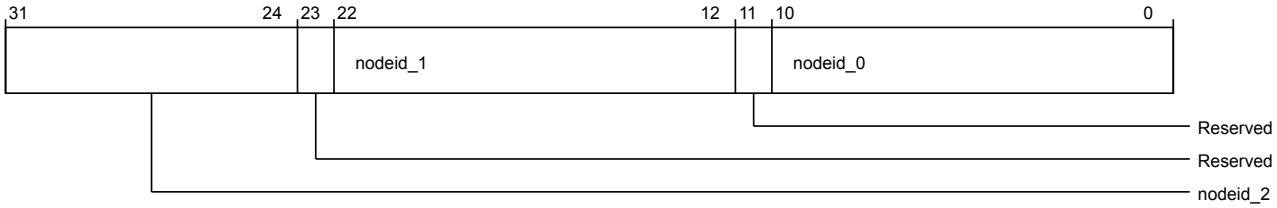


Figure 3-909 por_rnsam_non_hash_tgt_nodeid0 (low)

The following table shows the non_hash_tgt_nodeid0 lower register bit assignments.

Table 3-923 por_rnsam_non_hash_tgt_nodeid0 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_2	Non-hashed target node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_1	Non-hashed target node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_0	Non-hashed target node ID 0	RW	11'b00000000000

non_hash_tgt_nodeid1

Configures non-hashed target node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

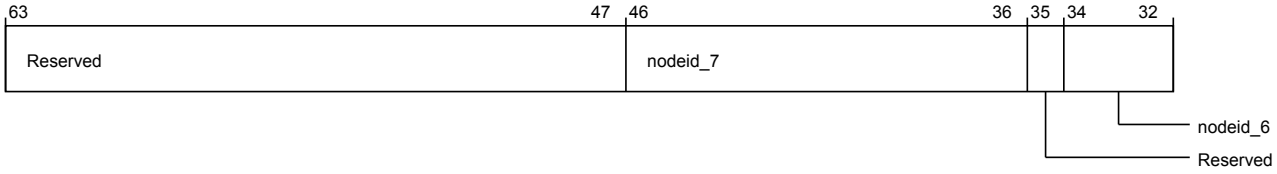


Figure 3-910 por_rnsam_non_hash_tgt_nodeid1 (high)

The following table shows the non_hash_tgt_nodeid1 higher register bit assignments.

Table 3-924 por_rnsam_non_hash_tgt_nodeid1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_7	Non-hashed target node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_6	Non-hashed target node ID 6	RW	11'b00000000000

The following image shows the lower register bit assignments.

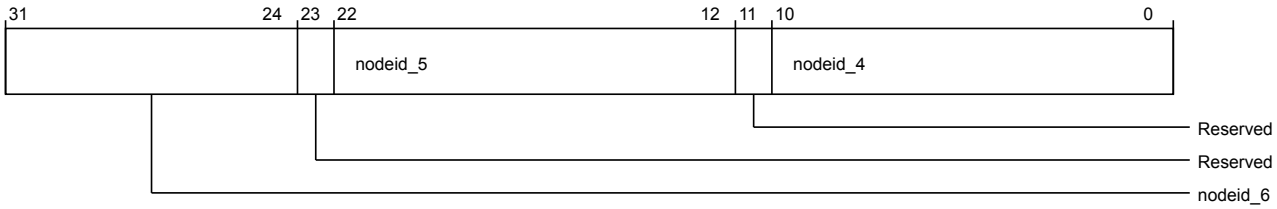


Figure 3-911 por_rnsam_non_hash_tgt_nodeid1 (low)

The following table shows the non_hash_tgt_nodeid1 lower register bit assignments.

Table 3-925 por_rnsam_non_hash_tgt_nodeid1 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_6	Non-hashed target node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_5	Non-hashed target node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_4	Non-hashed target node ID 4	RW	11'b00000000000

non_hash_tgt_nodeid2

Configures non-hashed target node IDs 8 to 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

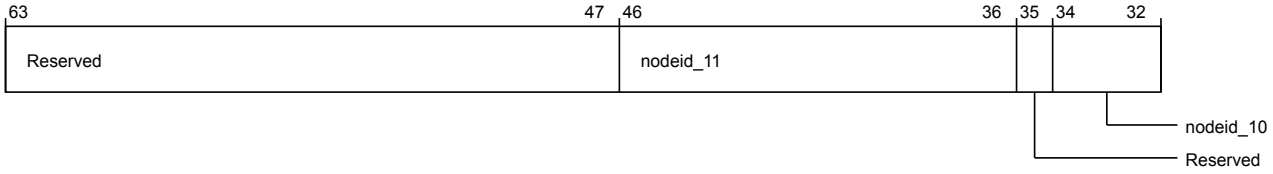


Figure 3-912 por_rnsam_non_hash_tgt_nodeid2 (high)

The following table shows the non_hash_tgt_nodeid2 higher register bit assignments.

Table 3-926 por_rnsam_non_hash_tgt_nodeid2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_11	Non-hashed target node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_10	Non-hashed target node ID 10	RW	11'b00000000000

The following image shows the lower register bit assignments.

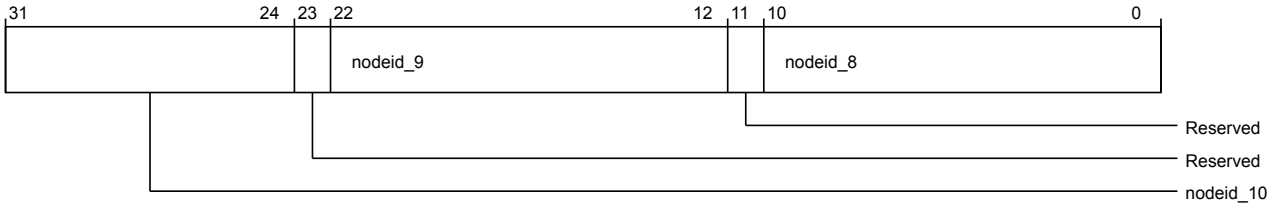


Figure 3-913 por_rnsam_non_hash_tgt_nodeid2 (low)

The following table shows the non_hash_tgt_nodeid2 lower register bit assignments.

Table 3-927 por_rnsam_non_hash_tgt_nodeid2 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_10	Non-hashed target node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_9	Non-hashed target node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Non-hashed target node ID 8	RW	11'b00000000000

non_hash_tgt_nodeid3

Configures non-hashed target node IDs 12 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

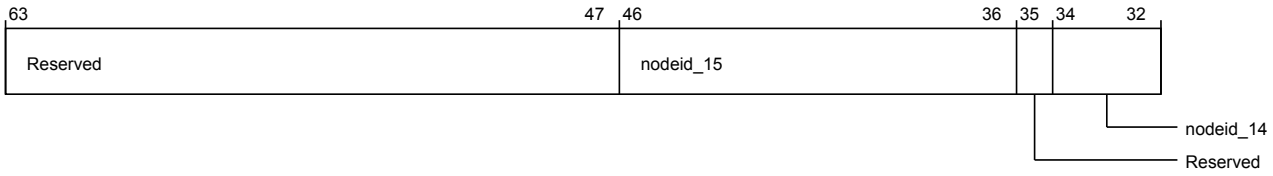


Figure 3-914 por_rnsam_non_hash_tgt_nodeid3 (high)

The following table shows the non_hash_tgt_nodeid3 higher register bit assignments.

Table 3-928 por_rnsam_non_hash_tgt_nodeid3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_15	Non-hashed target node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_14	Non-hashed target node ID 14	RW	11'b00000000000

The following image shows the lower register bit assignments.

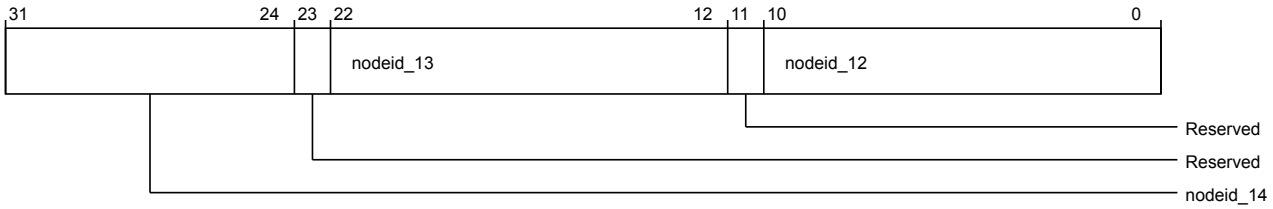


Figure 3-915 por_rnsam_non_hash_tgt_nodeid3 (low)

The following table shows the non_hash_tgt_nodeid3 lower register bit assignments.

Table 3-929 por_rnsam_non_hash_tgt_nodeid3 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_14	Non-hashed target node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_13	Non-hashed target node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_12	Non-hashed target node ID 12	RW	11'b00000000000

non_hash_tgt_nodeid4

Configures non-hashed target node IDs 16 to 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hCE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

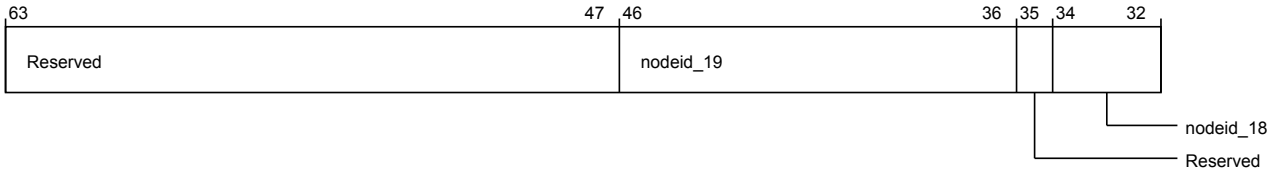


Figure 3-916 por_rnsam_non_hash_tgt_nodeid4 (high)

The following table shows the non_hash_tgt_nodeid4 higher register bit assignments.

Table 3-930 por_rnsam_non_hash_tgt_nodeid4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_19	Non-hashed target node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_18	Non-hashed target node ID 18	RW	11'b00000000000

The following image shows the lower register bit assignments.

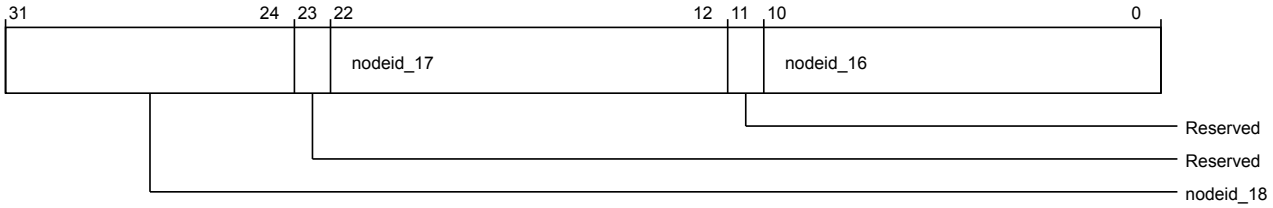


Figure 3-917 por_rnsam_non_hash_tgt_nodeid4 (low)

The following table shows the non_hash_tgt_nodeid4 lower register bit assignments.

Table 3-931 por_rnsam_non_hash_tgt_nodeid4 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_18	Non-hashed target node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_17	Non-hashed target node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_16	Non-hashed target node ID 16	RW	11'b00000000000

sys_cache_grp_region0

Configures hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

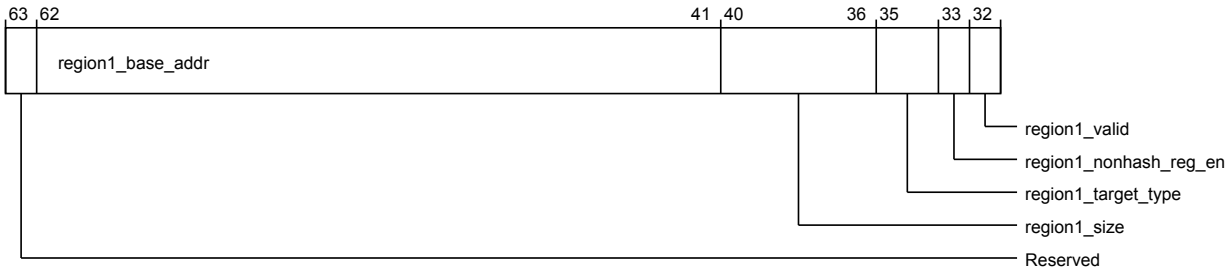


Figure 3-918 por_rnsam_sys_cache_grp_region0 (high)

The following table shows the sys_cache_grp_region0 higher register bit assignments.

Table 3-932 por_rnsam_sys_cache_grp_region0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region1_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b0000000000000000000000
40:36	region1_size	Memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region1_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00

Table 3-932 por_rnsam_sys_cache_grp_region0 (high) (continued)

Bits	Field name	Description	Type	Reset
33	region1_nonhash_reg_en	Enables hashed region 1 to select non-hashed node	RW	1'b0
32	region1_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

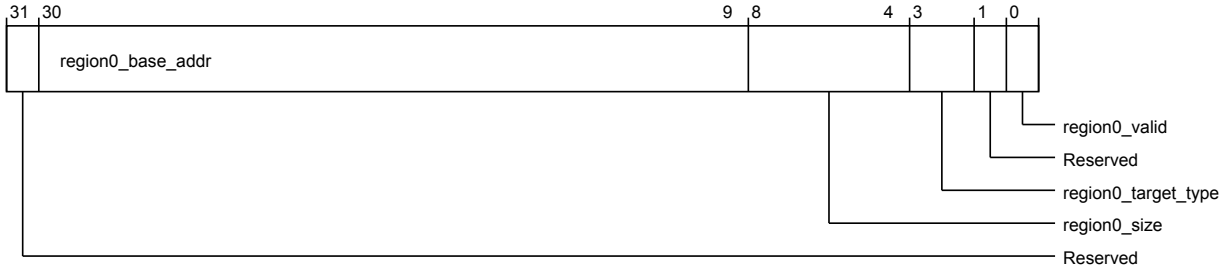


Figure 3-919 por_rnsam_sys_cache_grp_region0 (low)

The following table shows the sys_cache_grp_region0 lower register bit assignments.

Table 3-933 por_rnsam_sys_cache_grp_region0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b0000000000000000000000
8:4	region0_size	Memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region0_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00

Table 3-933 por_rnsam_sys_cache_grp_region0 (low) (continued)

Bits	Field name	Description	Type	Reset
1	Reserved	Reserved	RO	-
0	region0_valid	Memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_region1

Configures hashed memory regions 2 and 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

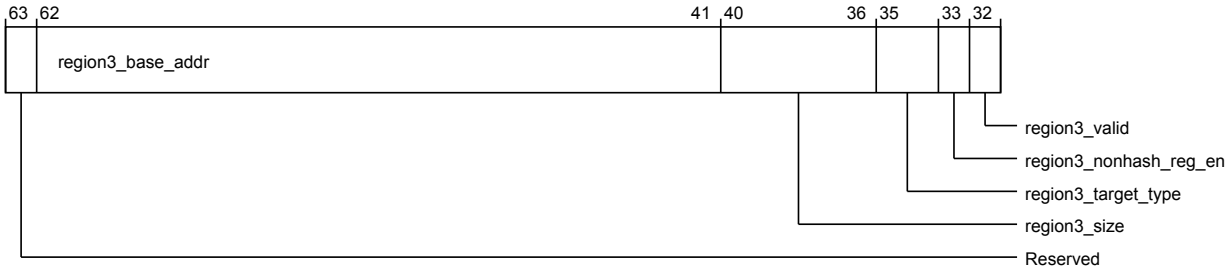


Figure 3-920 por_rnsam_sys_cache_grp_region1 (high)

The following table shows the sys_cache_grp_region1 higher register bit assignments.

Table 3-934 por_rnsam_sys_cache_grp_region1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b0000000000000000000000

Table 3-934 por_rnsam_sys_cache_grp_region1 (high) (continued)

Bits	Field name	Description	Type	Reset
40:36	region3_size	Memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region3_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	region3_nonhash_reg_en	Enables hashed region 3 to select non-hashed node	RW	1'b0
32	region3_valid	Memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

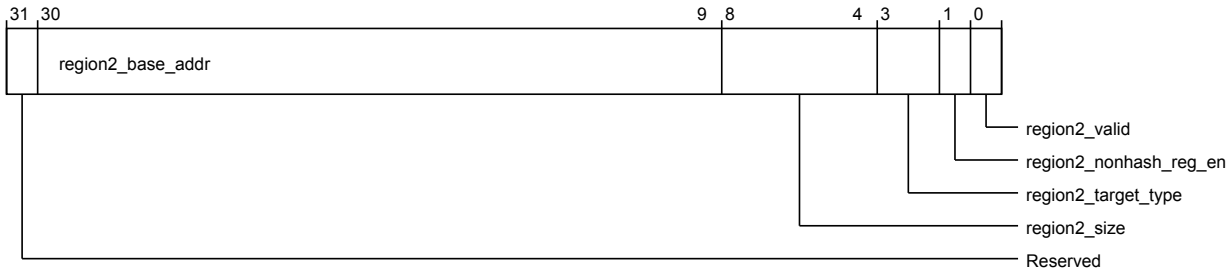


Figure 3-921 por_rnsam_sys_cache_grp_region1 (low)

The following table shows the sys_cache_grp_region1 lower register bit assignments.

Table 3-935 por_rnsam_sys_cache_grp_region1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region2_base_addr	Bits [47:26] of base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b0000000000000000000000
8:4	region2_size	Memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000

Table 3-935 por_rnsam_sys_cache_grp_region1 (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	region2_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	region2_nonhash_reg_en	Enables hashed region 2 to select non-hashed node	RW	1'b0
0	region2_valid	Memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_hn_nodeid_reg0

Configures hashed node IDs for system cache groups. Controls target HN node IDs 0 to 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

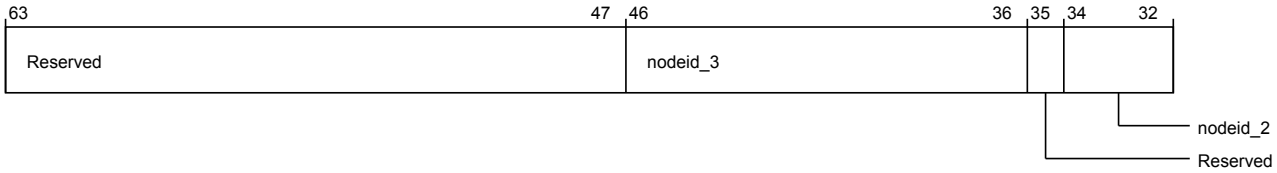


Figure 3-922 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg0 higher register bit assignments.

Table 3-936 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_3	Hashed target node ID 3	RW	11'b00000000000

Table 3-936 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (high) (continued)

Bits	Field name	Description	Type	Reset
35	Reserved	Reserved	RO	-
34:32	nodeid_2	Hashed target node ID 2	RW	11'b00000000000

The following image shows the lower register bit assignments.

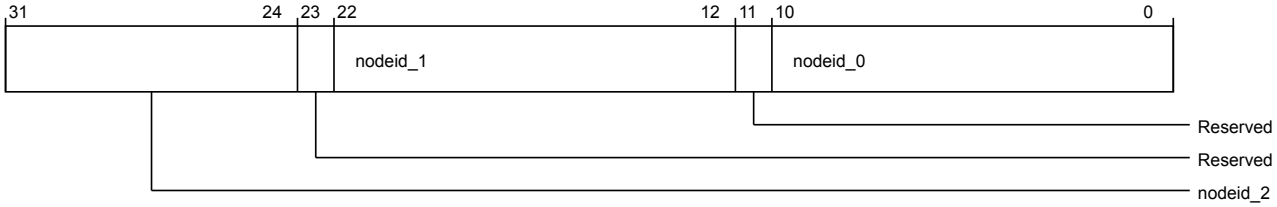


Figure 3-923 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg0 lower register bit assignments.

Table 3-937 por_rnsam_sys_cache_grp_hn_nodeid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_2	Hashed target node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_1	Hashed target node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_0	Hashed target node ID 0	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg1

Configures hashed node IDs for system cache groups. Controls target HN node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

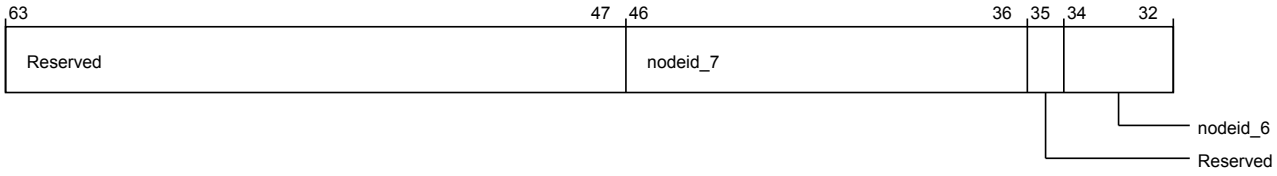


Figure 3-924 por_rnsam_sys_cache_grp_hn_nodeid_reg1 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg1 higher register bit assignments.

Table 3-938 por_rnsam_sys_cache_grp_hn_nodeid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_7	Hashed target node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_6	Hashed target node ID 6	RW	11'b00000000000

The following image shows the lower register bit assignments.

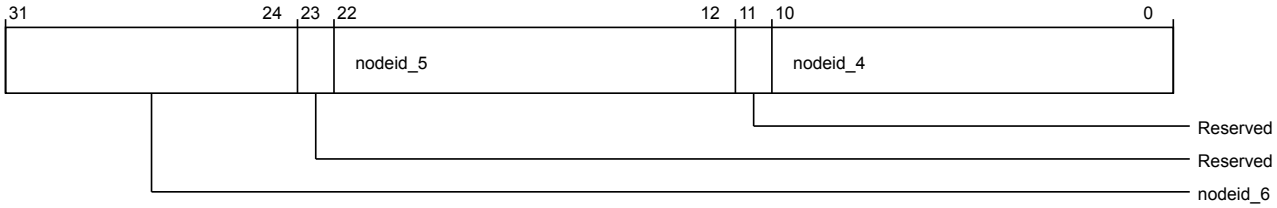


Figure 3-925 por_rnsam_sys_cache_grp_hn_nodeid_reg1 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg1 lower register bit assignments.

Table 3-939 por_rnsam_sys_cache_grp_hn_nodeid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_6	Hashed target node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_5	Hashed target node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_4	Hashed target node ID 4	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg2

Configures hashed node IDs for system cache groups. Controls target HN node IDs 8 to 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC68

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

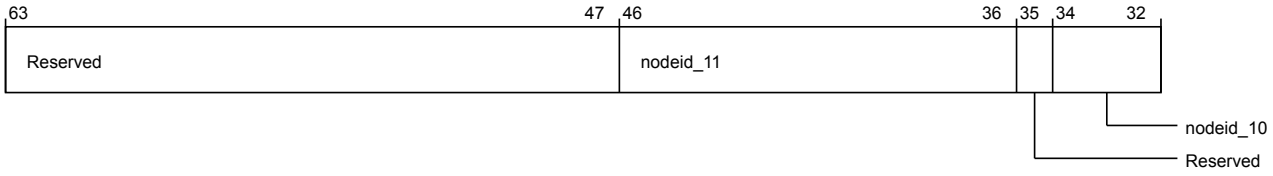


Figure 3-926 por_rnsam_sys_cache_grp_hn_nodeid_reg2 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg2 higher register bit assignments.

Table 3-940 por_rnsam_sys_cache_grp_hn_nodeid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_11	Hashed target node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_10	Hashed target node ID 10	RW	11'b00000000000

The following image shows the lower register bit assignments.

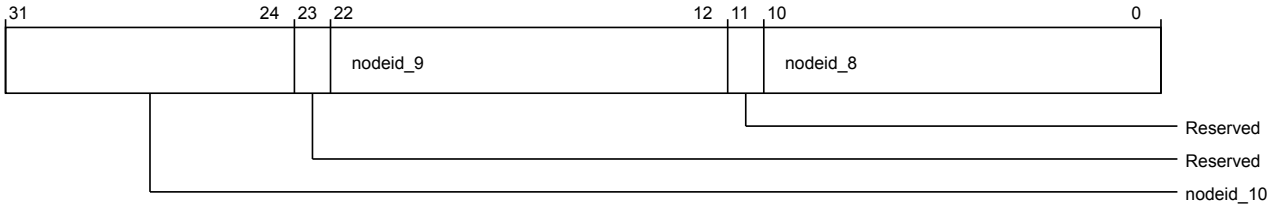


Figure 3-927 por_rnsam_sys_cache_grp_hn_nodeid_reg2 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg2 lower register bit assignments.

Table 3-941 por_rnsam_sys_cache_grp_hn_nodeid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_10	Hashed target node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_9	Hashed target node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_8	Hashed target node ID 8	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg3

Configures hashed node IDs for system cache groups. Controls target HN node IDs 12 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

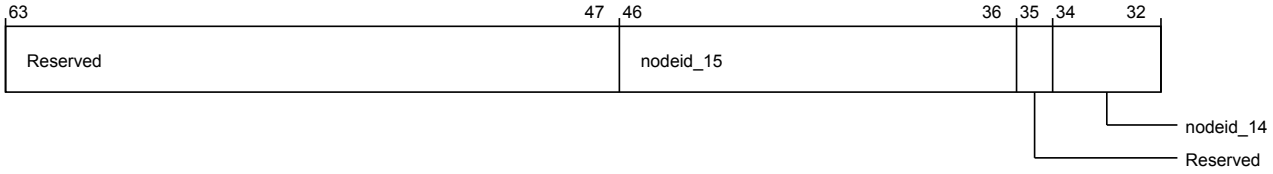


Figure 3-928 por_rnsam_sys_cache_grp_hn_nodeid_reg3 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg3 higher register bit assignments.

Table 3-942 por_rnsam_sys_cache_grp_hn_nodeid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_15	Hashed target node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_14	Hashed target node ID 14	RW	11'b00000000000

The following image shows the lower register bit assignments.

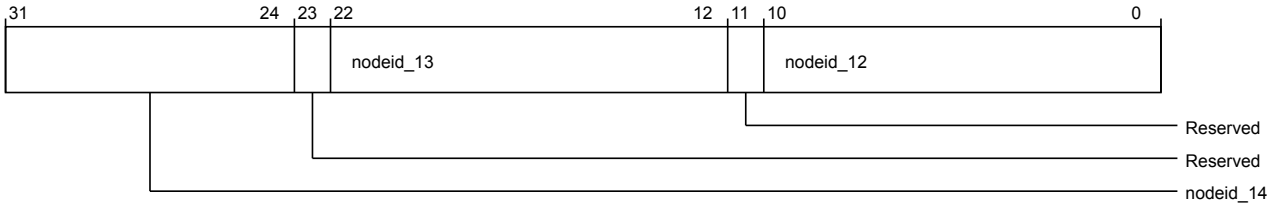


Figure 3-929 por_rnsam_sys_cache_grp_hn_nodeid_reg3 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg3 lower register bit assignments.

Table 3-943 por_rnsam_sys_cache_grp_hn_nodeid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_14	Hashed target node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_13	Hashed target node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_12	Hashed target node ID 12	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg4

Configures hashed node IDs for system cache groups. Controls target HN node IDs 16 to 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

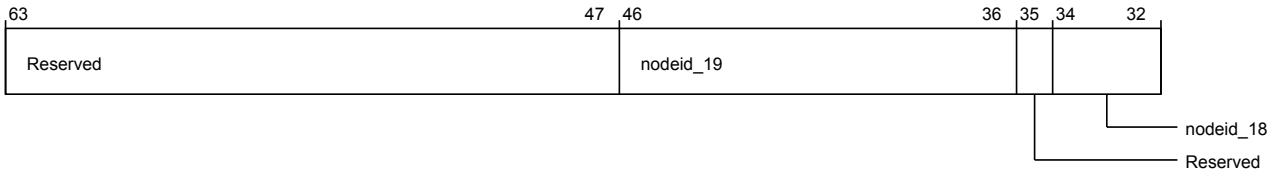


Figure 3-930 por_rnsam_sys_cache_grp_hn_nodeid_reg4 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg4 higher register bit assignments.

Table 3-944 por_rnsam_sys_cache_grp_hn_nodeid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_19	Hashed target node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_18	Hashed target node ID 18	RW	11'b00000000000

The following image shows the lower register bit assignments.

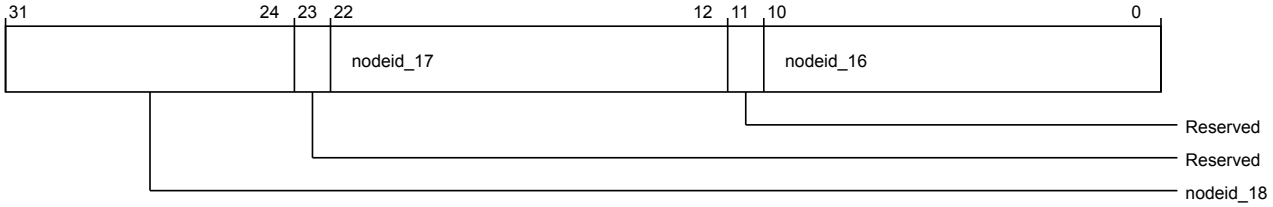


Figure 3-931 por_rnsam_sys_cache_grp_hn_nodeid_reg4 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg4 lower register bit assignments.

Table 3-945 por_rnsam_sys_cache_grp_hn_nodeid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_18	Hashed target node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_17	Hashed target node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_16	Hashed target node ID 16	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg5

Configures hashed node IDs for system cache groups. Controls target HN node IDs 20 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

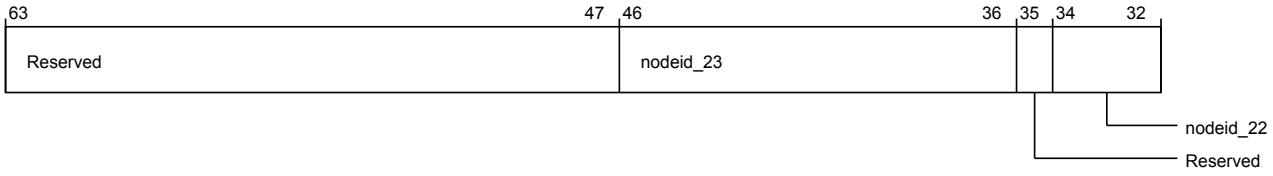


Figure 3-932 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg5 higher register bit assignments.

Table 3-946 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_23	Hashed target node ID 23	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_22	Hashed target node ID 22	RW	11'b00000000000

The following image shows the lower register bit assignments.

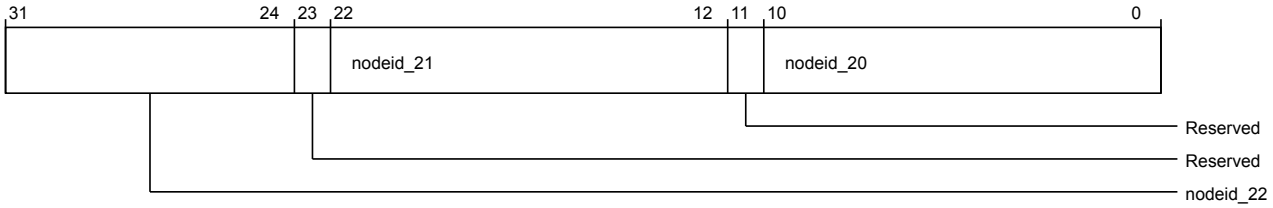


Figure 3-933 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg5 lower register bit assignments.

Table 3-947 por_rnsam_sys_cache_grp_hn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_22	Hashed target node ID 22	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_21	Hashed target node ID 21	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_20	Hashed target node ID 20	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg6

Configures hashed node IDs for system cache groups. Controls target HN node IDs 24 to 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

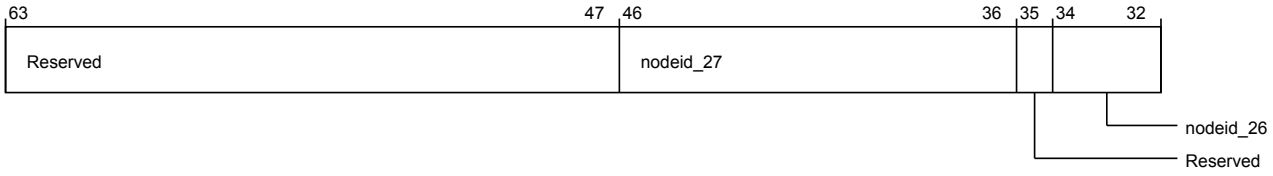


Figure 3-934 por_rnsam_sys_cache_grp_hn_nodeid_reg6 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg6 higher register bit assignments.

Table 3-948 por_rnsam_sys_cache_grp_hn_nodeid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_27	Hashed target node ID 27	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_26	Hashed target node ID 26	RW	11'b00000000000

The following image shows the lower register bit assignments.

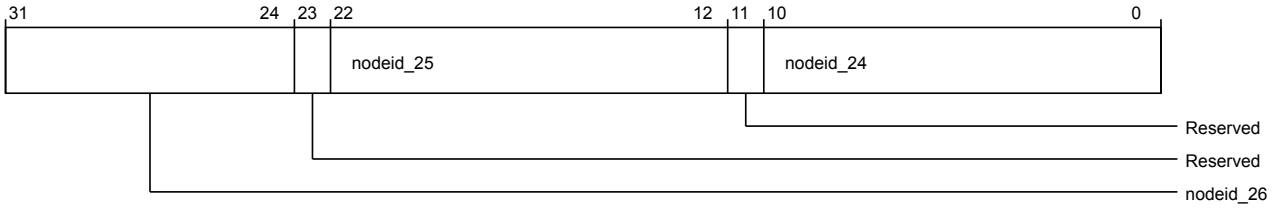


Figure 3-935 por_rnsam_sys_cache_grp_hn_nodeid_reg6 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg6 lower register bit assignments.

Table 3-949 por_rnsam_sys_cache_grp_hn_nodeid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_26	Hashed target node ID 26	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_25	Hashed target node ID 25	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_24	Hashed target node ID 24	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg7

Configures hashed node IDs for system cache groups. Controls target HN node IDs 28 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

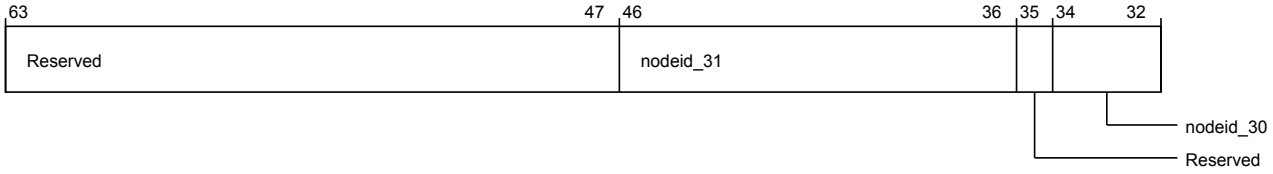


Figure 3-936 por_rnsam_sys_cache_grp_hn_nodeid_reg7 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg7 higher register bit assignments.

Table 3-950 por_rnsam_sys_cache_grp_hn_nodeid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_31	Hashed target node ID 31	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_30	Hashed target node ID 30	RW	11'b00000000000

The following image shows the lower register bit assignments.

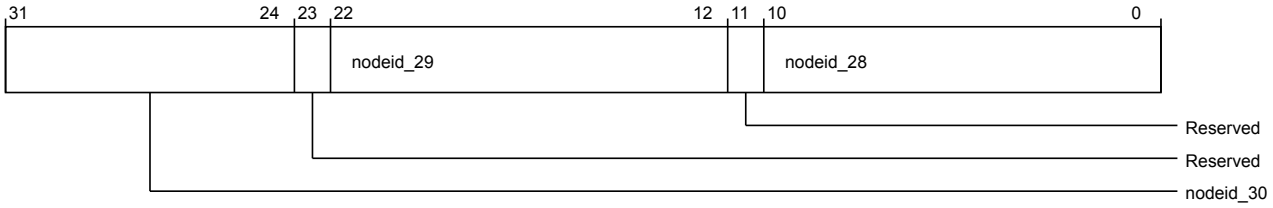


Figure 3-937 por_rnsam_sys_cache_grp_hn_nodeid_reg7 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg7 lower register bit assignments.

Table 3-951 por_rnsam_sys_cache_grp_hn_nodeid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_30	Hashed target node ID 30	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_29	Hashed target node ID 29	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_28	Hashed target node ID 28	RW	11'b00000000000

sys_cache_grp_nonhash_nodeid

Configures non-hashed node IDs for system cache groups 1 to 3. NOTE: Only applicable in the non-hashed mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC98

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

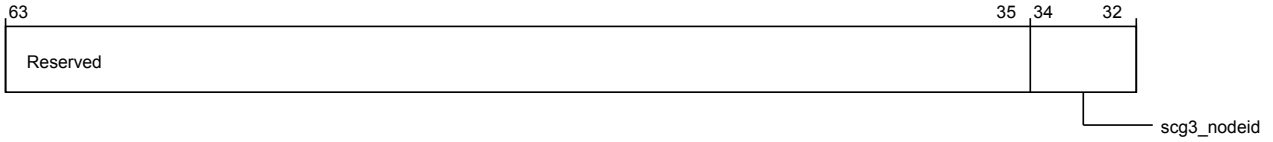


Figure 3-938 por_rnsam_sys_cache_grp_nonhash_nodeid (high)

The following table shows the sys_cache_grp_nonhash_nodeid higher register bit assignments.

Table 3-952 por_rnsam_sys_cache_grp_nonhash_nodeid (high)

Bits	Field name	Description	Type	Reset
63:35	Reserved	Reserved	RO	-
34:32	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b00000000000

The following image shows the lower register bit assignments.

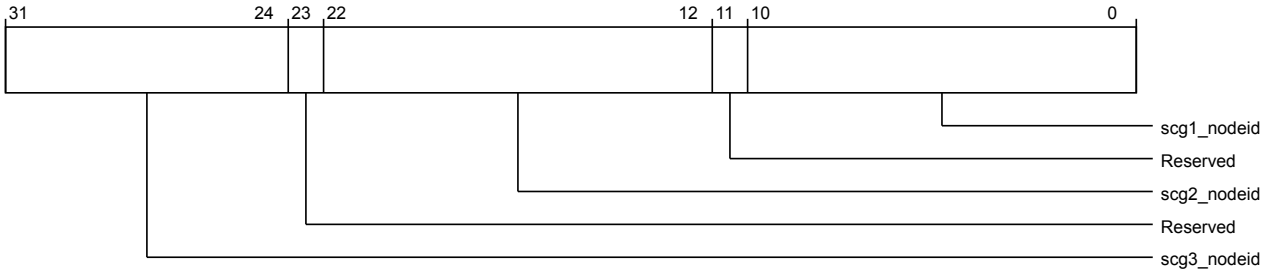


Figure 3-939 por_rnsam_sys_cache_grp_nonhash_nodeid (low)

The following table shows the sys_cache_grp_nonhash_nodeid lower register bit assignments.

Table 3-953 por_rnsam_sys_cache_grp_nonhash_nodeid (low)

Bits	Field name	Description	Type	Reset
31:24	scg3_nodeid	Non-hashed node ID for system cache group 3	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	scg2_nodeid	Non-hashed node ID for system cache group 2	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	scg1_nodeid	Non-hashed node ID for system cache group 1	RW	11'b00000000000

sys_cache_group_hn_count

Indicates number of HN-Fs in system cache groups 0 to 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

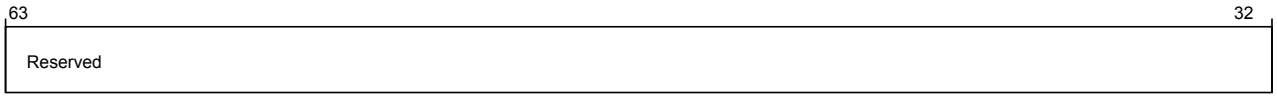


Figure 3-940 por_rnsam_sys_cache_group_hn_count (high)

The following table shows the sys_cache_group_hn_count higher register bit assignments.

Table 3-954 por_rnsam_sys_cache_group_hn_count (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

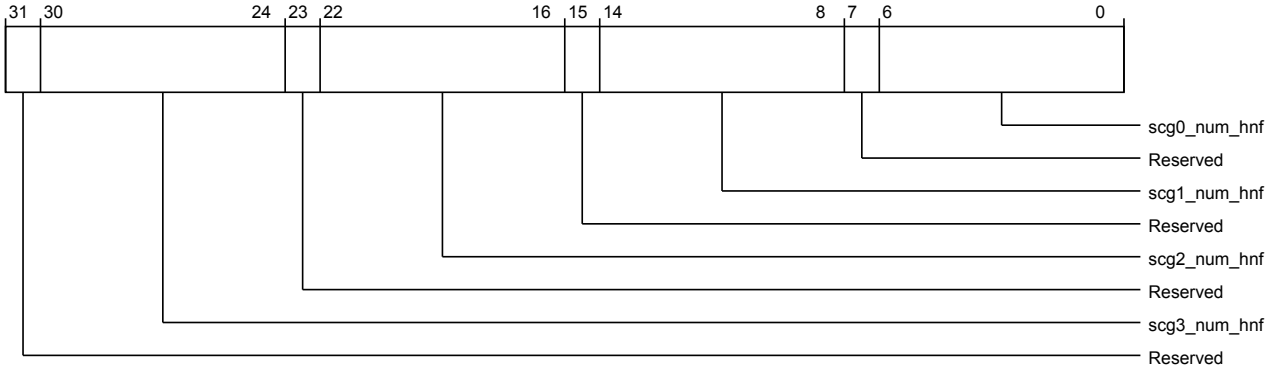


Figure 3-941 por_rnsam_sys_cache_group_hn_count (low)

The following table shows the sys_cache_group_hn_count lower register bit assignments.

Table 3-955 por_rnsam_sys_cache_group_hn_count (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:24	scg3_num_hnf	HN-F count for system cache group 3	RW	7'b00000
23	Reserved	Reserved	RO	-
22:16	scg2_num_hnf	HN-F count for system cache group 2	RW	7'b00000
15	Reserved	Reserved	RO	-
14:8	scg1_num_hnf	HN-F count for system cache group 1	RW	7'b00000
7	Reserved	Reserved	RO	-
6:0	scg0_num_hnf	HN-F count for system cache group 0	RW	7'b00000

sys_cache_grp_sn_nodeid_reg0

Configures hashed node IDs for system cache groups. Controls target SN node IDs 0 to 3.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

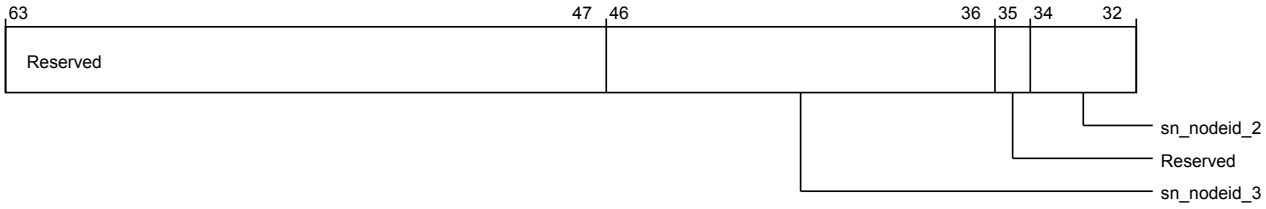


Figure 3-942 por_rnsam_sys_cache_grp_sn_nodeid_reg0 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg0 higher register bit assignments.

Table 3-956 por_rnsam_sys_cache_grp_sn_nodeid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_3	Hashed target SN node ID 3	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_2	Hashed target SN node ID 2	RW	11'b00000000000

The following image shows the lower register bit assignments.

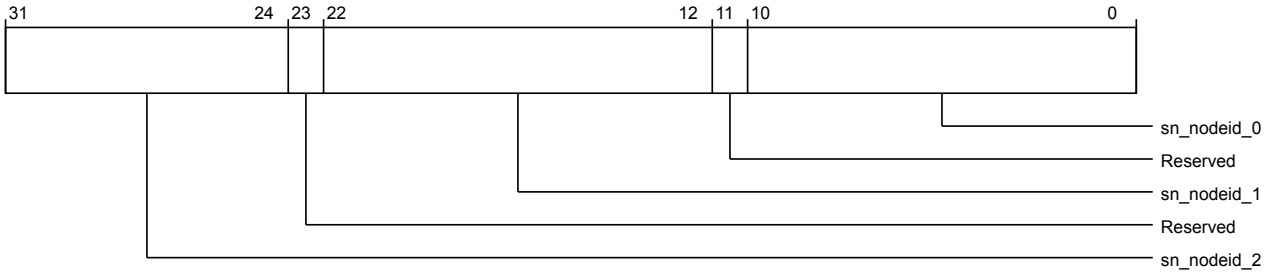


Figure 3-943 por_rnsam_sys_cache_grp_sn_nodeid_reg0 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg0 lower register bit assignments.

Table 3-957 por_rnsam_sys_cache_grp_sn_nodeid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_2	Hashed target SN node ID 2	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_1	Hashed target SN node ID 1	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_0	Hashed target SN node ID 0	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg1

Configures hashed node IDs for system cache groups. Controls target SN node IDs 4 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD10

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

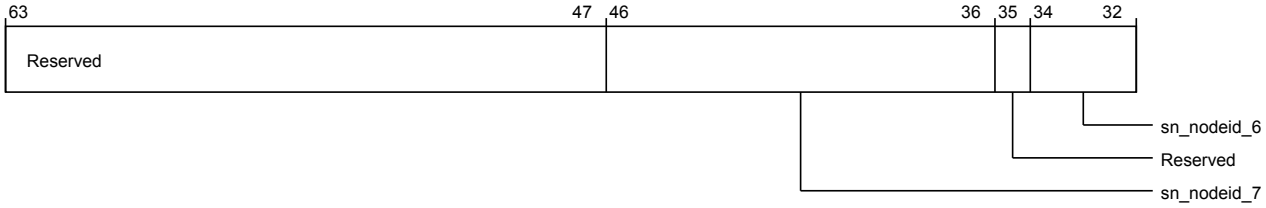


Figure 3-944 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg1 higher register bit assignments.

Table 3-958 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_7	Hashed target SN node ID 7	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_6	Hashed target SN node ID 6	RW	11'b00000000000

The following image shows the lower register bit assignments.

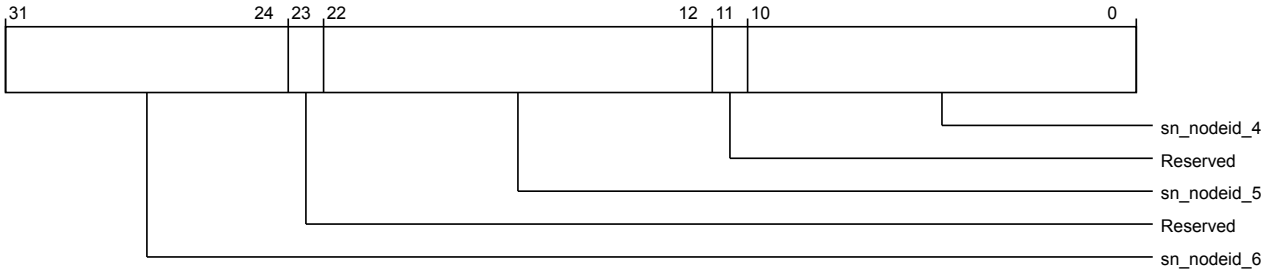


Figure 3-945 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg1 lower register bit assignments.

Table 3-959 por_rnsam_sys_cache_grp_sn_nodeid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_6	Hashed target SN node ID 6	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_5	Hashed target SN node ID 5	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_4	Hashed target SN node ID 4	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg2

Configures hashed node IDs for system cache groups. Controls target SN node IDs 8 to 11.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD18

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

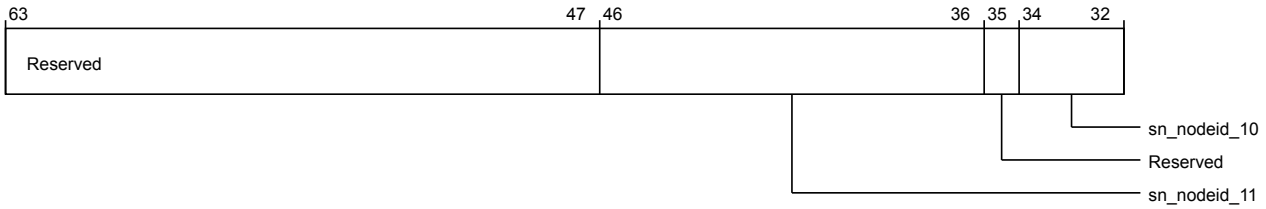


Figure 3-946 por_rnsam_sys_cache_grp_sn_nodeid_reg2 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg2 higher register bit assignments.

Table 3-960 por_rnsam_sys_cache_grp_sn_nodeid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_11	Hashed target SN node ID 11	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_10	Hashed target SN node ID 10	RW	11'b00000000000

The following image shows the lower register bit assignments.

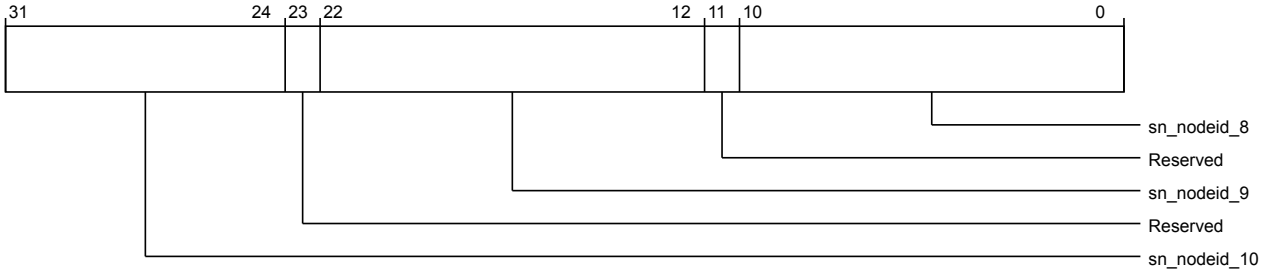


Figure 3-947 por_rnsam_sys_cache_grp_sn_nodeid_reg2 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg2 lower register bit assignments.

Table 3-961 por_rnsam_sys_cache_grp_sn_nodeid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_10	Hashed target SN node ID 10	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_9	Hashed target SN node ID 9	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_8	Hashed target SN node ID 8	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg3

Configures hashed node IDs for system cache groups. Controls target SN node IDs 12 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD20

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

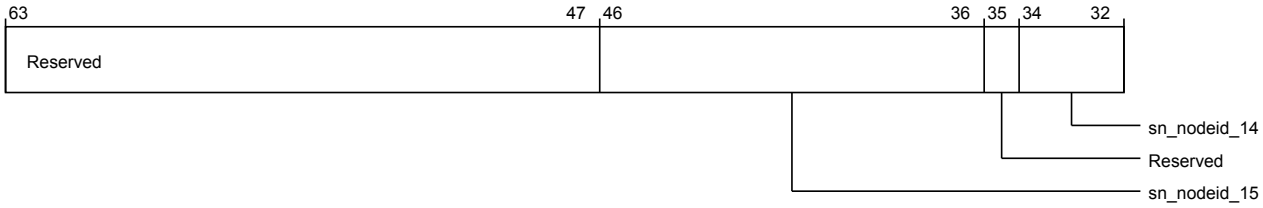


Figure 3-948 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg3 higher register bit assignments.

Table 3-962 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_15	Hashed target SN node ID 15	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b00000000000

The following image shows the lower register bit assignments.

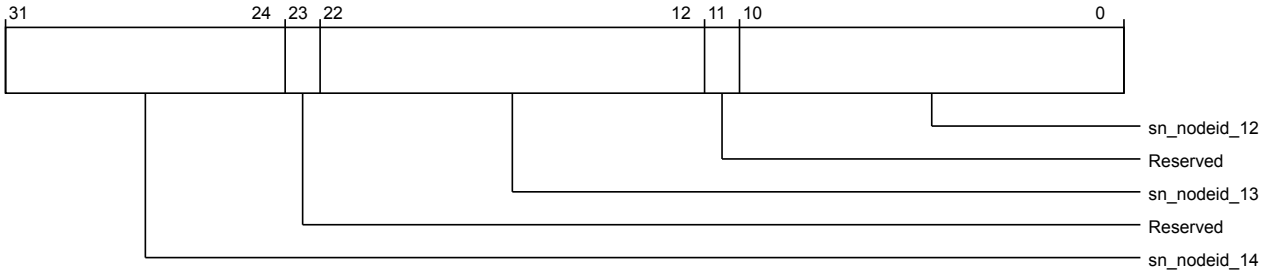


Figure 3-949 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg3 lower register bit assignments.

Table 3-963 por_rnsam_sys_cache_grp_sn_nodeid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_14	Hashed target SN node ID 14	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_13	Hashed target SN node ID 13	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_12	Hashed target SN node ID 12	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg4

Configures hashed node IDs for system cache groups. Controls target SN node IDs 16 to 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD28

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

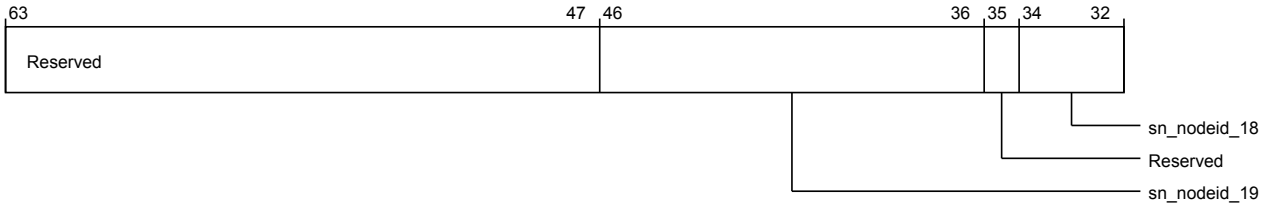


Figure 3-950 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg4 higher register bit assignments.

Table 3-964 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_19	Hashed target SN node ID 19	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_18	Hashed target SN node ID 18	RW	11'b00000000000

The following image shows the lower register bit assignments.

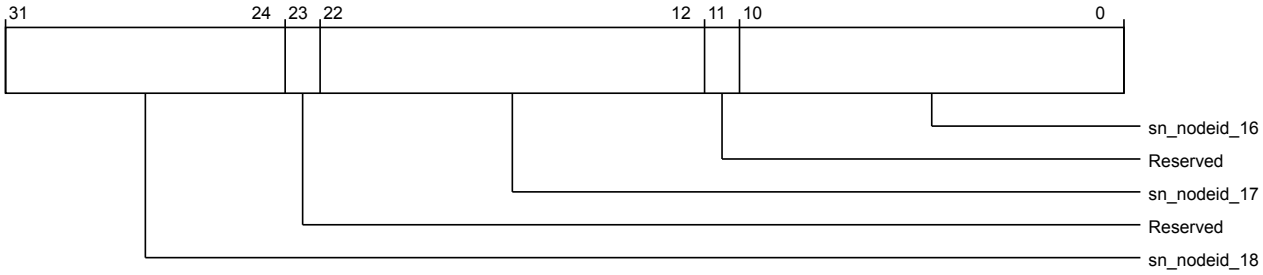


Figure 3-951 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg4 lower register bit assignments.

Table 3-965 por_rnsam_sys_cache_grp_sn_nodeid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_18	Hashed target SN node ID 18	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_17	Hashed target SN node ID 17	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_16	Hashed target SN node ID 16	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg5

Configures hashed node IDs for system cache groups. Controls target SN node IDs 20 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

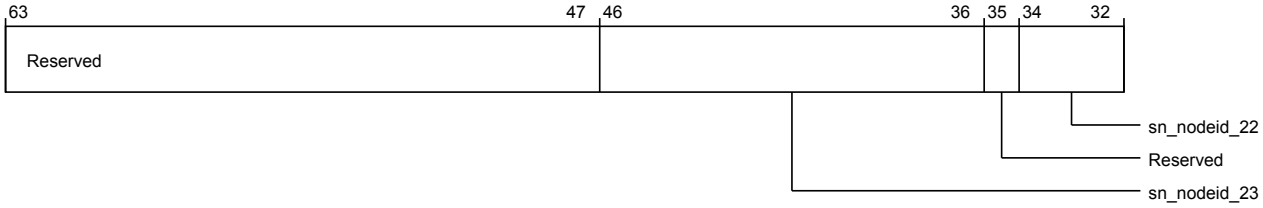


Figure 3-952 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg5 higher register bit assignments.

Table 3-966 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_23	Hashed target SN node ID 23	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_22	Hashed target SN node ID 22	RW	11'b00000000000

The following image shows the lower register bit assignments.

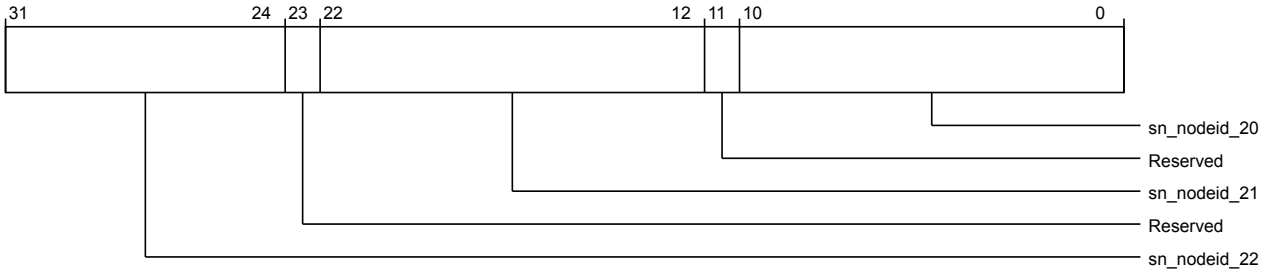


Figure 3-953 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg5 lower register bit assignments.

Table 3-967 por_rnsam_sys_cache_grp_sn_nodeid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_22	Hashed target SN node ID 22	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_21	Hashed target SN node ID 21	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_20	Hashed target SN node ID 20	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg6

Configures hashed node IDs for system cache groups. Controls target SN node IDs 24 to 27.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD38

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

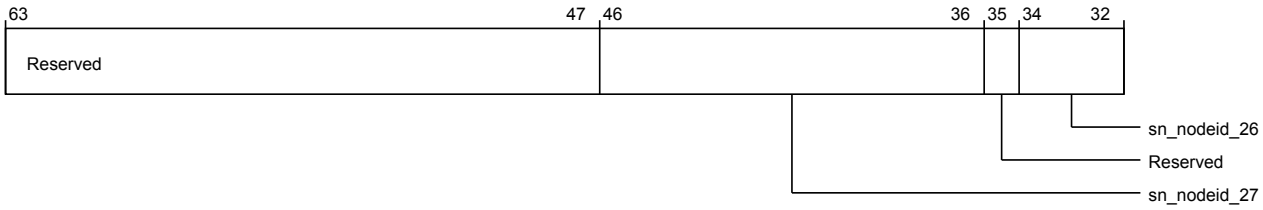


Figure 3-954 por_rnsam_sys_cache_grp_sn_nodeid_reg6 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg6 higher register bit assignments.

Table 3-968 por_rnsam_sys_cache_grp_sn_nodeid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_27	Hashed target SN node ID 27	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_26	Hashed target SN node ID 26	RW	11'b00000000000

The following image shows the lower register bit assignments.

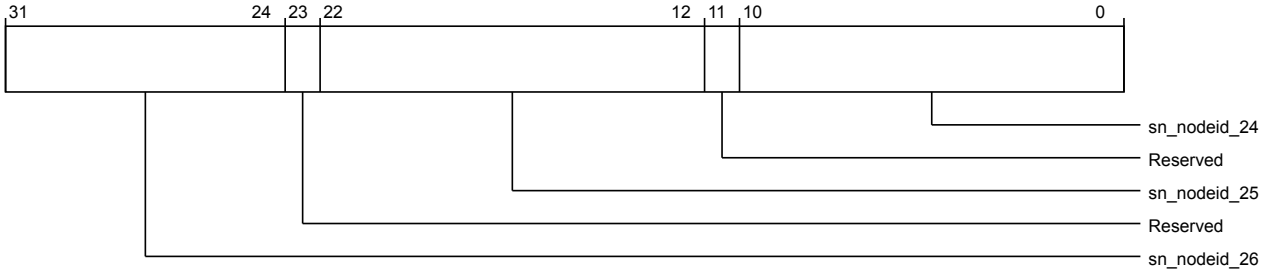


Figure 3-955 por_rnsam_sys_cache_grp_sn_nodeid_reg6 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg6 lower register bit assignments.

Table 3-969 por_rnsam_sys_cache_grp_sn_nodeid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_26	Hashed target SN node ID 26	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_25	Hashed target SN node ID 25	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_24	Hashed target SN node ID 24	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg7

Configures hashed node IDs for system cache groups. Controls target SN node IDs 28 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD40

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

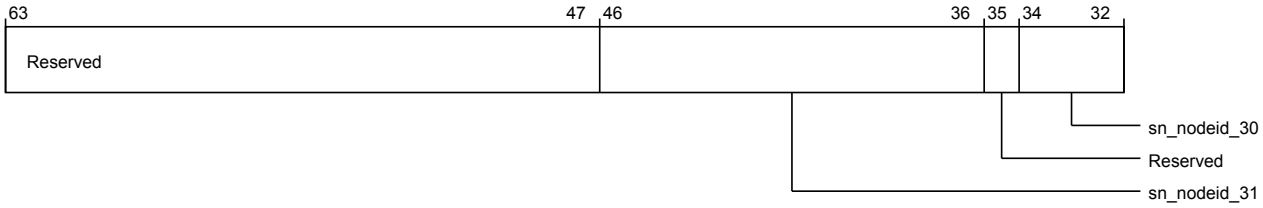


Figure 3-956 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg7 higher register bit assignments.

Table 3-970 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_31	Hashed target SN node ID 31	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b00000000000

The following image shows the lower register bit assignments.

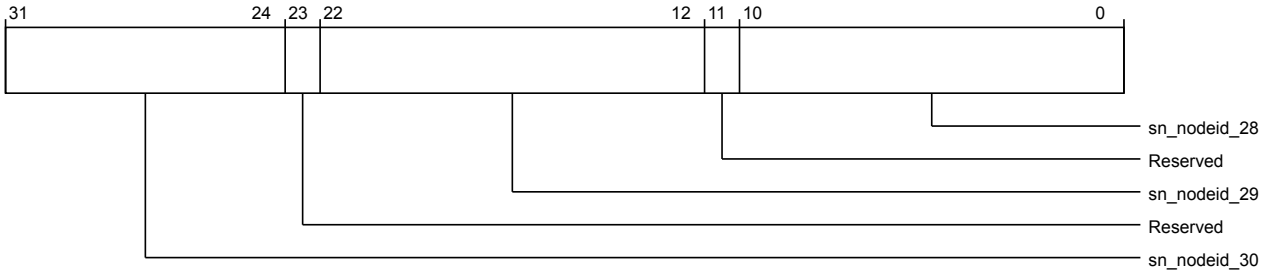


Figure 3-957 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg7 lower register bit assignments.

Table 3-971 por_rnsam_sys_cache_grp_sn_nodeid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_30	Hashed target SN node ID 30	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_29	Hashed target SN node ID 29	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_28	Hashed target SN node ID 28	RW	11'b00000000000

sys_cache_grp_sn_sam_cfg0

Configures top address bits for SN SAM system cache groups 0 and 1. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 > top_address_bit1 > top_address_bit0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

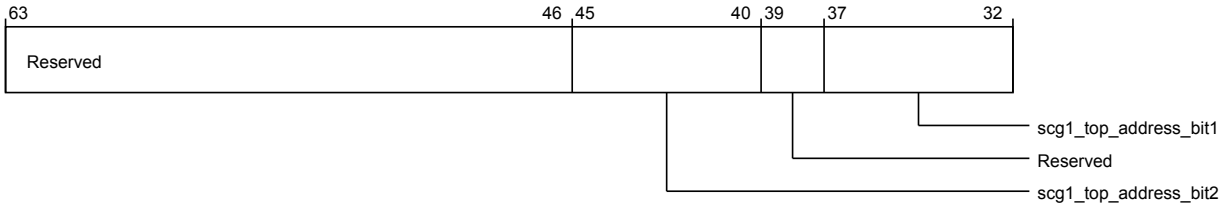


Figure 3-958 por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)

The following table shows the sys_cache_grp_sn_sam_cfg0 higher register bit assignments.

Table 3-972 por_rnsam_sys_cache_grp_sn_sam_cfg0 (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	scg1_top_address_bit2	Top address bit 2 for system cache group 1	RW	6'h00
39:38	Reserved	Reserved	RO	-
37:32	scg1_top_address_bit1	Top address bit 1 for system cache group 1	RW	6'h00

The following image shows the lower register bit assignments.

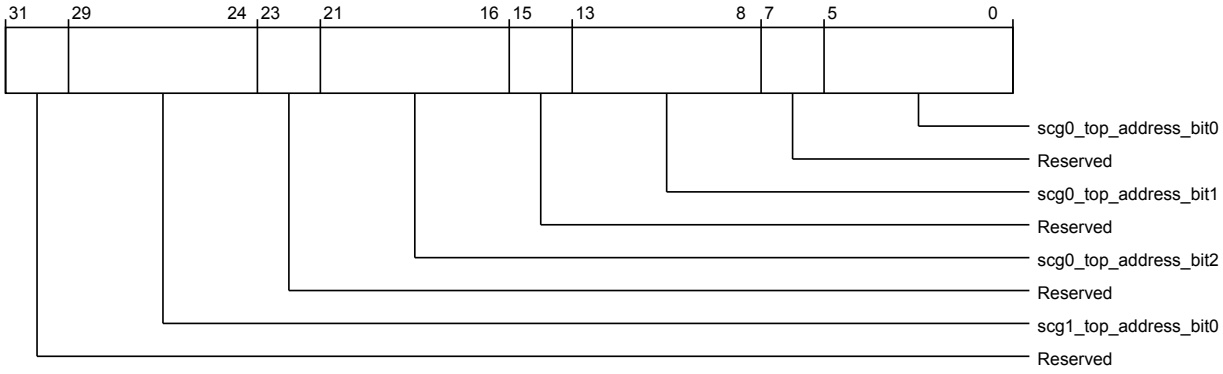


Figure 3-959 por_rnsam_sys_cache_grp_sn_sam_cfg0 (low)

The following table shows the sys_cache_grp_sn_sam_cfg0 lower register bit assignments.

Table 3-973 por_rnsam_sys_cache_grp_sn_sam_cfg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	scg1_top_address_bit0	Top address bit 0 for system cache group 1	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	scg0_top_address_bit2	Top address bit 2 for system cache group 0	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	scg0_top_address_bit1	Top address bit 1 for system cache group 0	RW	6'h00
7:6	Reserved	Reserved	RO	-
5:0	scg0_top_address_bit0	Top address bit 0 for system cache group 0	RW	6'h00

sys_cache_grp_sn_sam_cfg1

Configures top address bits for SN SAM system cache groups 2 and 3. All top_address_bit fields must be between bits 47 and 28. top_address_bit2 andgt; top_address_bit1 andgt; top_address_bit0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD50

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

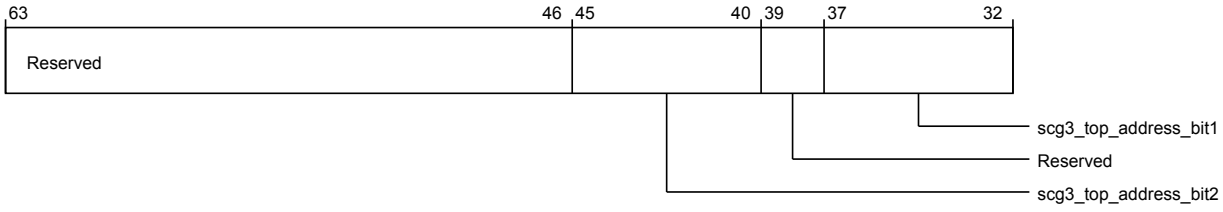


Figure 3-960 por_rnsam_sys_cache_grp_sn_sam_cfg1 (high)

The following table shows the sys_cache_grp_sn_sam_cfg1 higher register bit assignments.

Table 3-974 por_rnsam_sys_cache_grp_sn_sam_cfg1 (high)

Bits	Field name	Description	Type	Reset
63:46	Reserved	Reserved	RO	-
45:40	scg3_top_address_bit2	Top address bit 2 for system cache group 3	RW	6'h00

Table 3-974 por_rnsam_sys_cache_grp_sn_sam_cfg1 (high) (continued)

Bits	Field name	Description	Type	Reset
39:38	Reserved	Reserved	RO	-
37:32	scg3_top_address_bit1	Top address bit 1 for system cache group 3	RW	6'h00

The following image shows the lower register bit assignments.

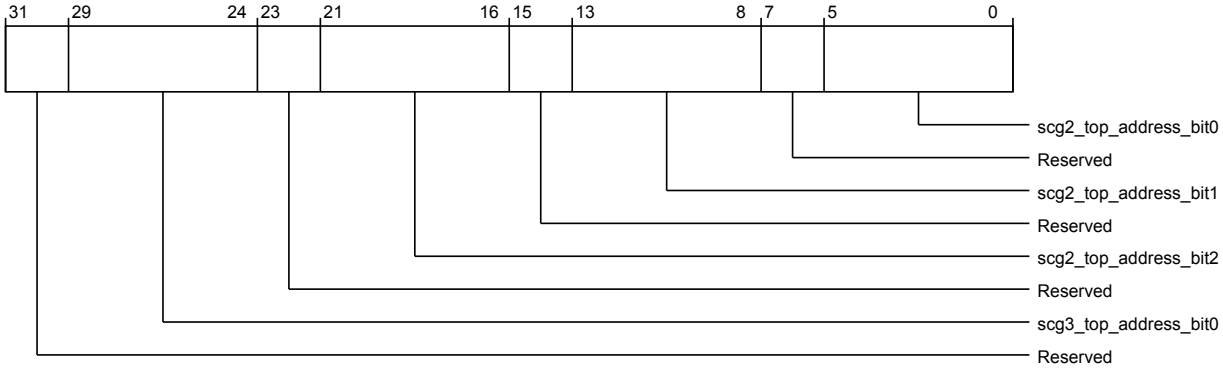


Figure 3-961 por_rnsam_sys_cache_grp_sn_sam_cfg1 (low)

The following table shows the sys_cache_grp_sn_sam_cfg1 lower register bit assignments.

Table 3-975 por_rnsam_sys_cache_grp_sn_sam_cfg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	scg3_top_address_bit0	Top address bit 0 for system cache group 3	RW	6'h00
23:22	Reserved	Reserved	RO	-
21:16	scg2_top_address_bit2	Top address bit 2 for system cache group 2	RW	6'h00
15:14	Reserved	Reserved	RO	-
13:8	scg2_top_address_bit1	Top address bit 1 for system cache group 2	RW	6'h00
7:6	Reserved	Reserved	RO	-
5:0	scg2_top_address_bit0	Top address bit 0 for system cache group 2	RW	6'h00

gic_mem_region_reg

Configures GIC memory region.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD58
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

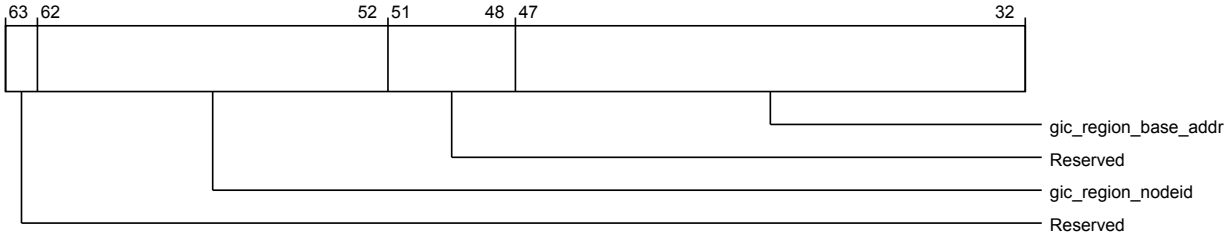


Figure 3-962 por_rnsam_gic_mem_region_reg (high)

The following table shows the gic_mem_region_reg higher register bit assignments.

Table 3-976 por_rnsam_gic_mem_region_reg (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:52	gic_region_nodeid	GIC node ID 30	RW	11'b00000000000
51:48	Reserved	Reserved	RO	-
47:32	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	32'h00000000

The following image shows the lower register bit assignments.

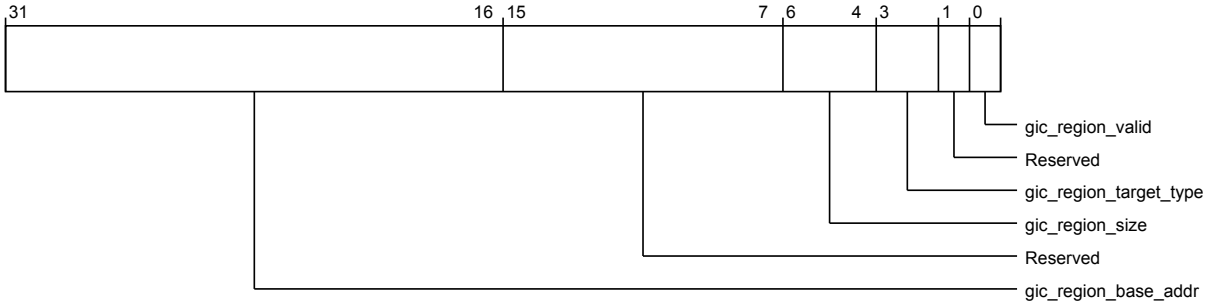


Figure 3-963 por_rnsam_gic_mem_region_reg (low)

The following table shows the gic_mem_region_reg lower register bit assignments.

Table 3-977 por_rnsam_gic_mem_region_reg (low)

Bits	Field name	Description	Type	Reset
31:16	gic_region_base_addr	Base address of the GIC memory region CONSTRAINT: Must be an integer multiple of region size	RW	32'h00000000
15:7	Reserved	Reserved	RO	-
6:4	gic_region_size	GIC memory region size 3'b000: 64KB 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB CONSTRAINT: Memory region must be a power of 2.	RW	3'b000
3:2	gic_region_target_type	Indicates node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	gic_region_valid	Memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_sn_attr

Configures attributes for SN node IDs for system cache groups.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD60
Register reset 64'b0
Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

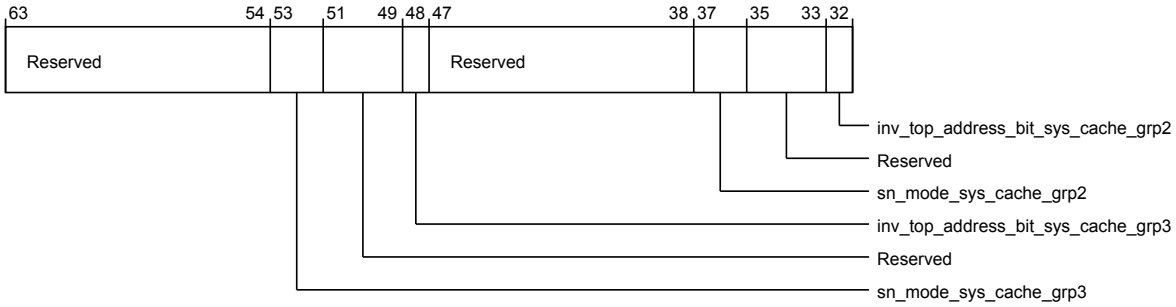


Figure 3-964 por_rnsam_sys_cache_grp_sn_attr (high)

The following table shows the sys_cache_grp_sn_attr higher register bit assignments.

Table 3-978 por_rnsam_sys_cache_grp_sn_attr (high)

Bits	Field name	Description	Type	Reset
63:54	Reserved	Reserved	RO	-
53:52	sn_mode_sys_cache_grp3	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
51:49	Reserved	Reserved	RO	-
48	inv_top_address_bit_sys_cache_grp3	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
47:38	Reserved	Reserved	RO	-
37:36	sn_mode_sys_cache_grp2	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b00
35:33	Reserved	Reserved	RO	-
32	inv_top_address_bit_sys_cache_grp2	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

The following image shows the lower register bit assignments.

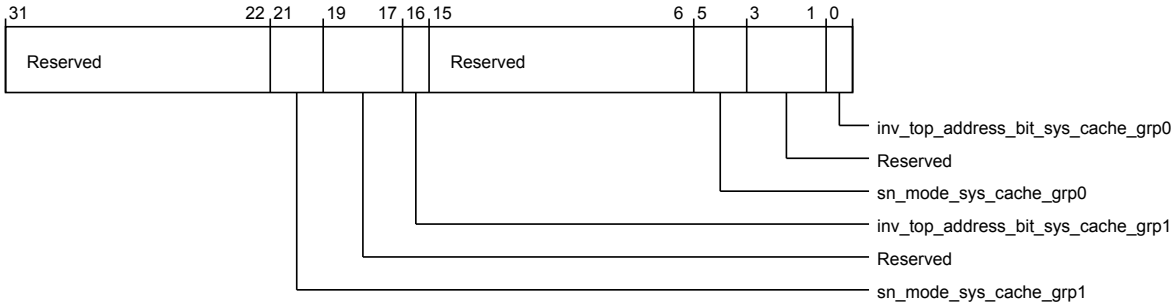


Figure 3-965 por_rnsam_sys_cache_grp_sn_attr (low)

The following table shows the sys_cache_grp_sn_attr lower register bit assignments.

Table 3-979 por_rnsam_sys_cache_grp_sn_attr (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:20	sn_mode_sys_cache_grp1	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
19:17	Reserved	Reserved	RO	-
16	inv_top_address_bit_sys_cache_grp1	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0
15:6	Reserved	Reserved	RO	-
5:4	sn_mode_sys_cache_grp0	SN selection mode 2'b00: 1-SN mode (SN0) 2'b01: 3-SN mode (SN0, SN1, SN2) 2'b10: 6-SN mode (SN0, SN1, SN2, SN3, SN4, SN5) 2'b11: Reserved	RW	2'b0
3:1	Reserved	Reserved	RO	-
0	inv_top_address_bit_sys_cache_grp0	Inverts the top address bit (top_address_bit1 if 3-SN, top_address_bit2 if 6-SN); only used when the address map does not have unique address bit combinations	RW	1'h0

sys_cache_grp_hn_cpa_en_reg

Configures CCIX port aggregation mode for hashed HN node IDs

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD68

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

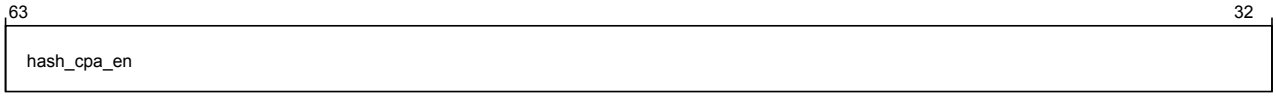


Figure 3-966 por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)

The following table shows the sys_cache_grp_hn_cpa_en_reg higher register bit assignments.

Table 3-980 por_rnsam_sys_cache_grp_hn_cpa_en_reg (high)

Bits	Field name	Description	Type	Reset
63:32	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

The following image shows the lower register bit assignments.

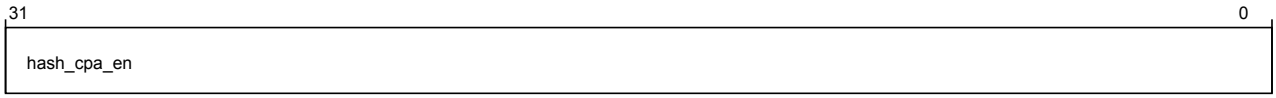


Figure 3-967 por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)

The following table shows the sys_cache_grp_hn_cpa_en_reg lower register bit assignments.

Table 3-981 por_rnsam_sys_cache_grp_hn_cpa_en_reg (low)

Bits	Field name	Description	Type	Reset
31:0	hash_cpa_en	Enable CPA for each hashed node ID	RW	64'h0000000000000000

sys_cache_grp_hn_cpa_grp_reg

Configures CCIX port aggregation group ID for each System Cache Group

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD70

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

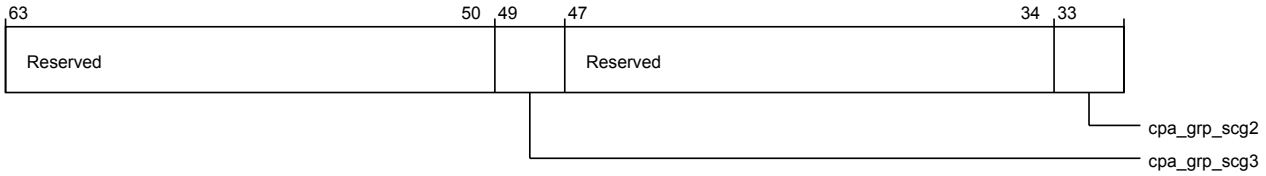


Figure 3-968 por_rnsam_sys_cache_grp_hn_cpa_grp_reg (high)

The following table shows the sys_cache_grp_hn_cpa_grp_reg higher register bit assignments.

Table 3-982 por_rnsam_sys_cache_grp_hn_cpa_grp_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	cpa_grp_scg3	Specifies CCIX port aggregation group ID for System Cache Group 3 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00
47:34	Reserved	Reserved	RO	-
33:32	cpa_grp_scg2	Specifies CCIX port aggregation group ID for System Cache Group 2 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00

The following image shows the lower register bit assignments.

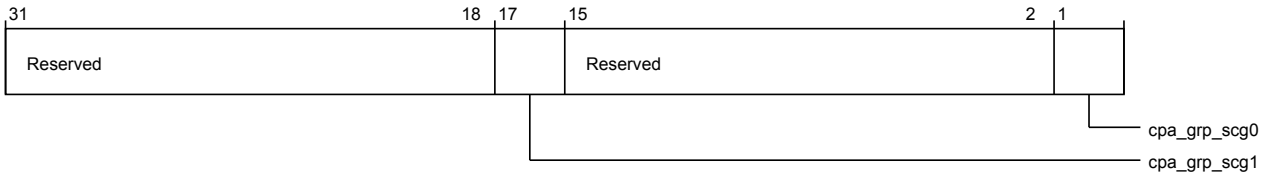


Figure 3-969 por_rnsam_sys_cache_grp_hn_cpa_grp_reg (low)

The following table shows the sys_cache_grp_hn_cpa_grp_reg lower register bit assignments.

Table 3-983 por_rnsam_sys_cache_grp_hn_cpa_grp_reg (low)

Bits	Field name	Description	Type	Reset
31:18	Reserved	Reserved	RO	-
17:16	cpa_grp_scg1	Specifies CCIX port aggregation group ID for System Cache Group 1 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00
15:2	Reserved	Reserved	RO	-
1:0	cpa_grp_scg0	Specifies CCIX port aggregation group ID for System Cache Group 0 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved	RW	2'b00

cml_port_aggr_mode_ctrl_reg

Configures the CCIX port aggregation modes for all non-hashed memory regions.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

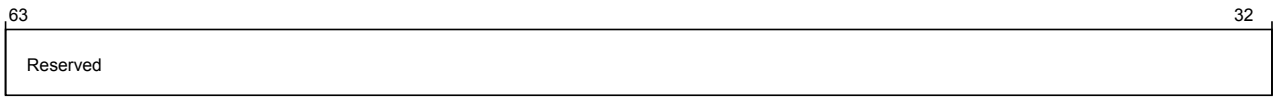


Figure 3-970 por_rnsam_cml_port_aggr_mode_ctrl_reg (high)

The following table shows the cml_port_aggr_mode_ctrl_reg higher register bit assignments.

Table 3-984 por_rnsam_cml_port_aggr_mode_ctrl_reg (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

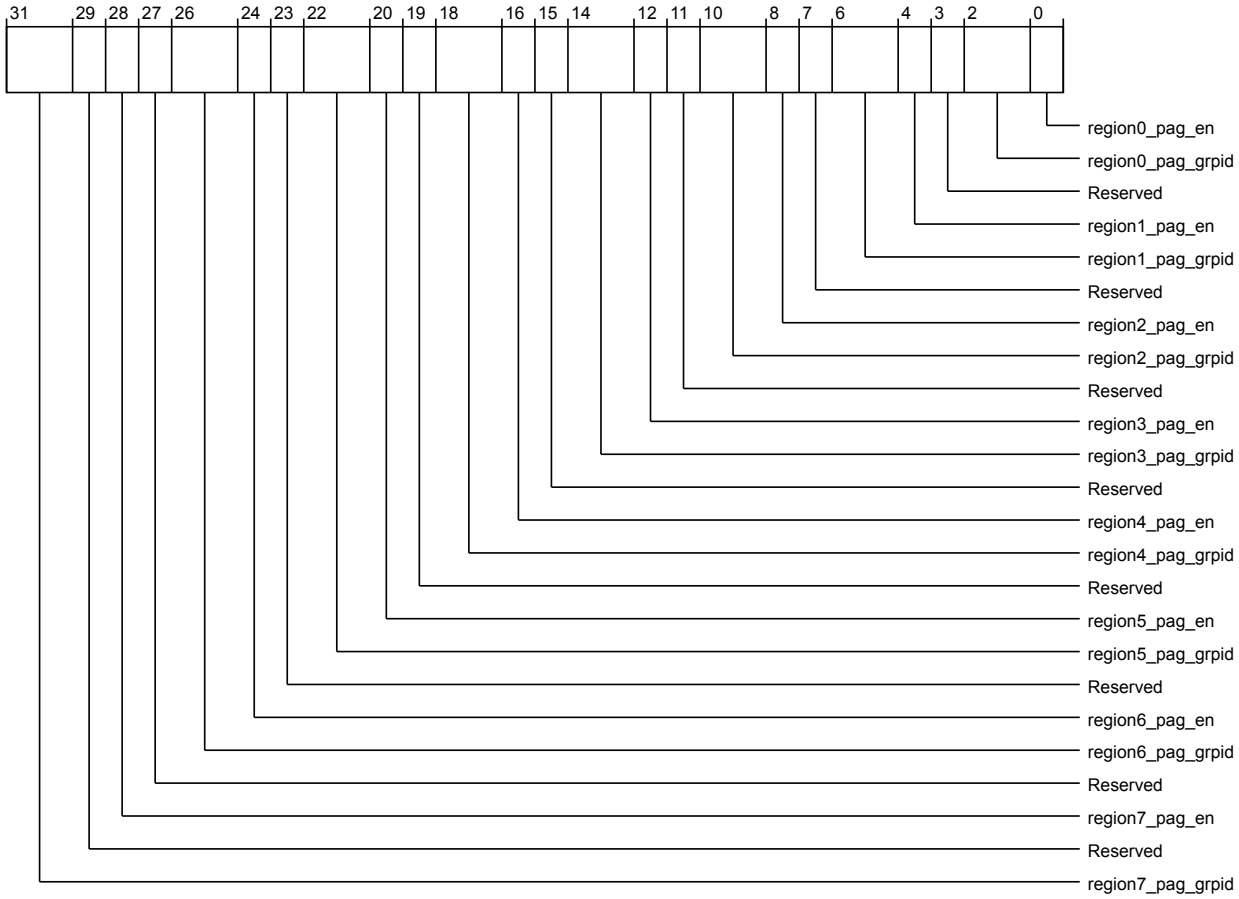


Figure 3-971 por_rnsam_cml_port_aggr_mode_ctrl_reg (low)

The following table shows the cml_port_aggr_mode_ctrl_reg lower register bit assignments.

Table 3-985 por_rnsam_cml_port_aggr_mode_ctrl_reg (low)

Bits	Field name	Description	Type	Reset
31:30	region7_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
29	Reserved	Reserved	RO	-
28	region7_pag_en	Enables the CPA mode for non-hashed memory region 7	RW	1'b0
27	Reserved	Reserved	RO	-

Table 3-985 por_rnsam_cml_port_aggr_mode_ctrl_reg (low) (continued)

Bits	Field name	Description	Type	Reset
26:25	region6_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved6	RW	2'b0
24	region6_pag_en	Enables the CPA mode for non-hashed memory region 6	RW	1'b0
23	Reserved	Reserved	RO	-
22:21	region5_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved5	RW	2'b0
20	region5_pag_en	Enables the CPA mode for non-hashed memory region 5	RW	1'b0
19	Reserved	Reserved	RO	-
18:17	region4_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved4	RW	2'b0
16	region4_pag_en	Enables the CPA mode for non-hashed memory region 4	RW	1'b0
15	Reserved	Reserved	RO	-
14:13	region3_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved3	RW	2'b0
12	region3_pag_en	Enables the CPA mode for non-hashed memory region 3	RW	1'b0
11	Reserved	Reserved	RO	-

Table 3-985 por_rnsam_cml_port_aggr_mode_ctrl_reg (low) (continued)

Bits	Field name	Description	Type	Reset
10:9	region2_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved2	RW	2'b0
8	region2_pag_en	Enables the CPA mode for non-hashed memory region 2	RW	1'b0
7	Reserved	Reserved	RO	-
6:5	region1_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved1	RW	2'b0
4	region1_pag_en	Enables the CPA mode for non-hashed memory region 1	RW	1'b0
3	Reserved	Reserved	RO	-
2:1	region0_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved0	RW	2'b0
0	region0_pag_en	Enables the CPA mode for non-hashed memory region 0	RW	1'b0

cml_port_aggr_mode_ctrl_reg1

Configures the CCIX port aggregation modes for non-hashed memory regions 8 through 19.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE30

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

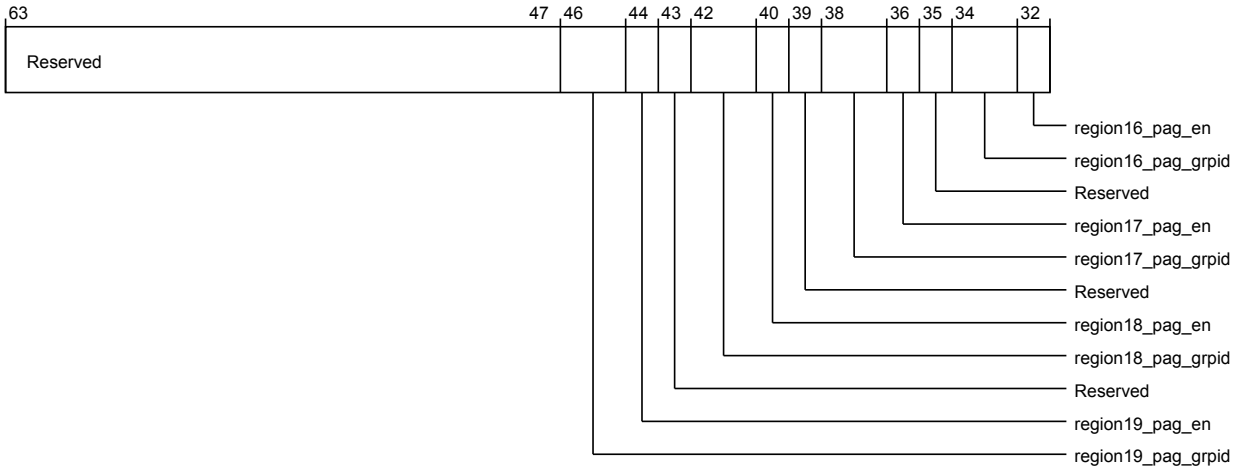


Figure 3-972 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (high)

The following table shows the cml_port_aggr_mode_ctrl_reg1 higher register bit assignments.

Table 3-986 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:45	region19_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
44	region19_pag_en	Enables the CPA mode for non-hashed memory region 19	RW	1'b0
43	Reserved	Reserved	RO	-
42:41	region18_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
40	region18_pag_en	Enables the CPA mode for non-hashed memory region 18	RW	1'b0
39	Reserved	Reserved	RO	-
38:37	region17_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0

Table 3-986 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (high) (continued)

Bits	Field name	Description	Type	Reset
36	region17_pag_en	Enables the CPA mode for non-hashed memory region 17	RW	1'b0
35	Reserved	Reserved	RO	-
34:33	region16_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
32	region16_pag_en	Enables the CPA mode for non-hashed memory region 16	RW	1'b0

The following image shows the lower register bit assignments.

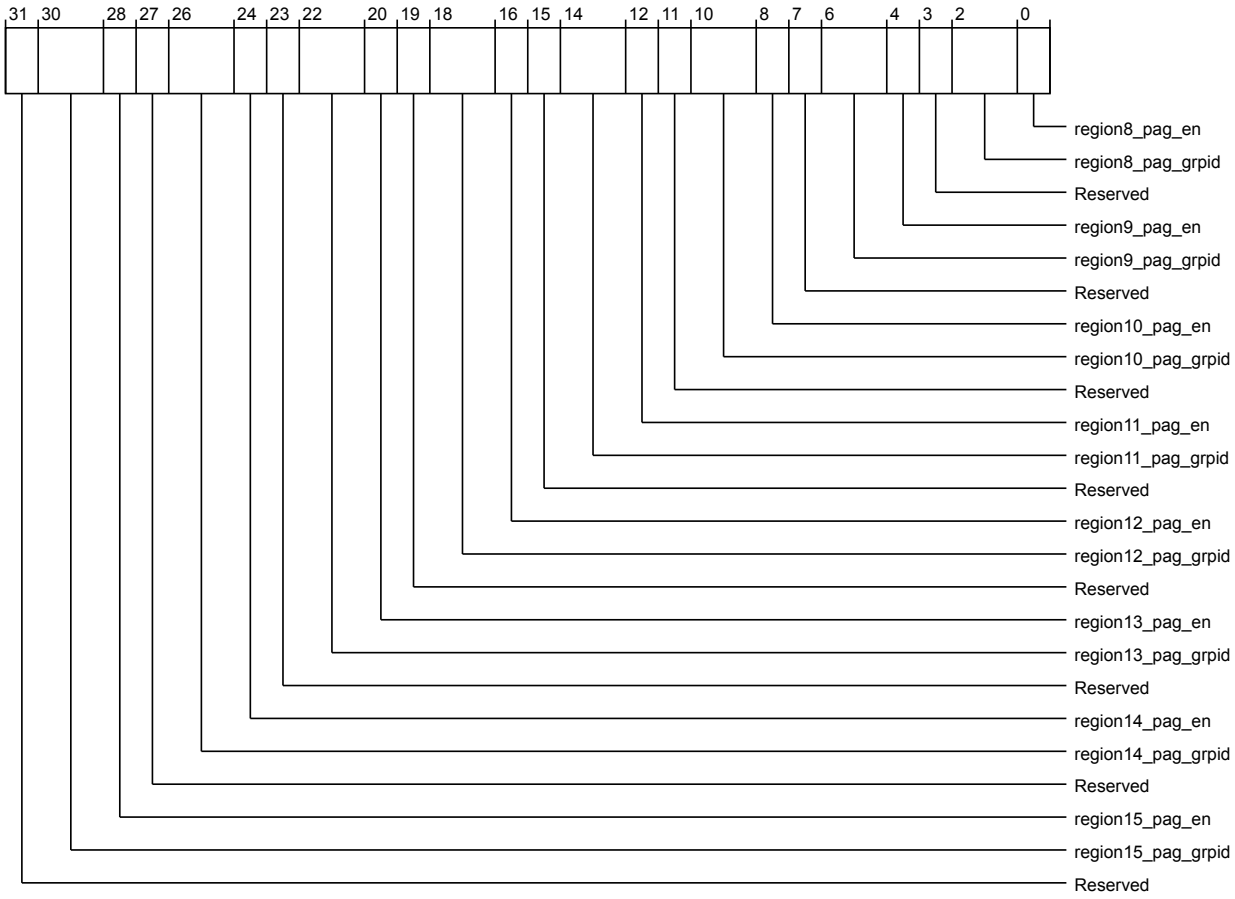


Figure 3-973 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (low)

The following table shows the cml_port_aggr_mode_ctrl_reg1 lower register bit assignments.

Table 3-987 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:29	region15_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved7	RW	2'b0
28	region15_pag_en	Enables the CPA mode for non-hashed memory region 15	RW	1'b0
27	Reserved	Reserved	RO	-
26:25	region14_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved6	RW	2'b0
24	region14_pag_en	Enables the CPA mode for non-hashed memory region 14	RW	1'b0
23	Reserved	Reserved	RO	-
22:21	region13_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved5	RW	2'b0
20	region13_pag_en	Enables the CPA mode for non-hashed memory region 13	RW	1'b0
19	Reserved	Reserved	RO	-
18:17	region12_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved4	RW	2'b0
16	region12_pag_en	Enables the CPA mode for non-hashed memory region 12	RW	1'b0
15	Reserved	Reserved	RO	-

Table 3-987 por_rnsam_cml_port_aggr_mode_ctrl_reg1 (low) (continued)

Bits	Field name	Description	Type	Reset
14:13	region11_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved3	RW	2'b0
12	region11_pag_en	Enables the CPA mode for non-hashed memory region 11	RW	1'b0
11	Reserved	Reserved	RO	-
10:9	region10_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved2	RW	2'b0
8	region10_pag_en	Enables the CPA mode for non-hashed memory region 10	RW	1'b0
7	Reserved	Reserved	RO	-
6:5	region9_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved1	RW	2'b0
4	region9_pag_en	Enables the CPA mode for non-hashed memory region 9	RW	1'b0
3	Reserved	Reserved	RO	-
2:1	region8_pag_grpid	Specifies CCIX port aggregation group ID 2'b00: CPA Group ID 0 2'b01: CPA Group ID 1 2'b10: Reserved 2'b11: Reserved0	RW	2'b0
0	region8_pag_en	Enables the CPA mode for non-hashed memory region 8	RW	1'b0

cml_port_aggr_grp0_add_mask

Configures the CCIX port aggregation address mask for group 0.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'hE08

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

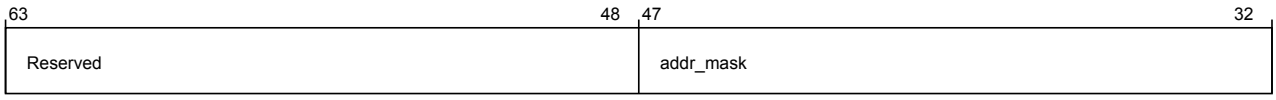


Figure 3-974 por_rnsam_cml_port_aggr_grp0_add_mask (high)

The following table shows the cml_port_aggr_grp0_add_mask higher register bit assignments.

Table 3-988 por_rnsam_cml_port_aggr_grp0_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

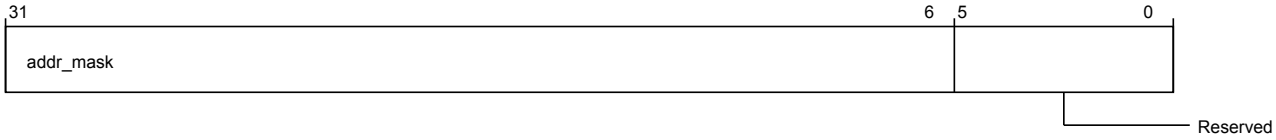


Figure 3-975 por_rnsam_cml_port_aggr_grp0_add_mask (low)

The following table shows the cml_port_aggr_grp0_add_mask lower register bit assignments.

Table 3-989 por_rnsam_cml_port_aggr_grp0_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

cml_port_aggr_grp1_add_mask

Configures the CCIX port aggregation address mask for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE10

Register reset 64'b1

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

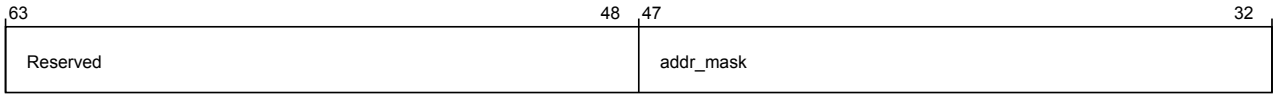


Figure 3-976 por_rnsam_cml_port_aggr_grp1_add_mask (high)

The following table shows the cml_port_aggr_grp1_add_mask higher register bit assignments.

Table 3-990 por_rnsam_cml_port_aggr_grp1_add_mask (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask to be applied before hashing	RW	42'b1

The following image shows the lower register bit assignments.

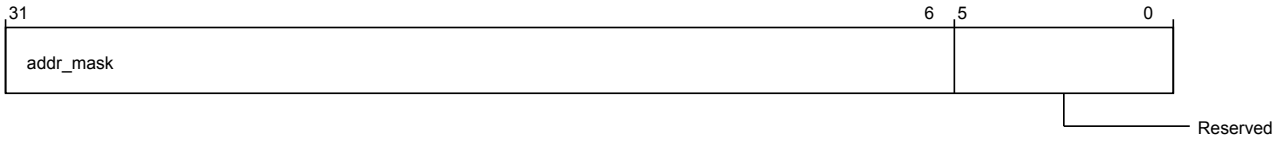


Figure 3-977 por_rnsam_cml_port_aggr_grp1_add_mask (low)

The following table shows the cml_port_aggr_grp1_add_mask lower register bit assignments.

Table 3-991 por_rnsam_cml_port_aggr_grp1_add_mask (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask to be applied before hashing	RW	42'b1
5:0	Reserved	Reserved	RO	-

cml_port_aggr_grp0_reg

Configures the CCIX port aggregation port IDs for group 0.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE40

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

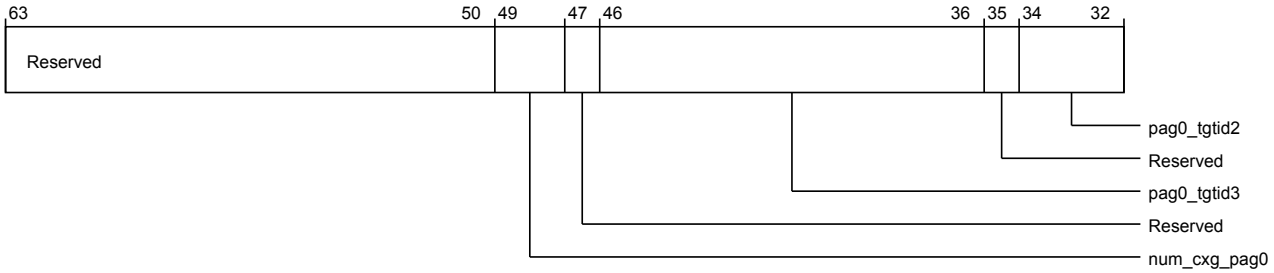


Figure 3-978 por_rnsam_cml_port_aggr_grp0_reg (high)

The following table shows the cml_port_aggr_grp0_reg higher register bit assignments.

Table 3-992 por_rnsam_cml_port_aggr_grp0_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag0	Specifies the number of CXRAs in CPAG 0 2'b00: 1 port used 2'b01: 2 ports used 2'b10: 4 ports used 2'b11: Reserved	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag0_tgtid3	Specifies target ID 3 for CPAG 0	RW	11'b0
35	Reserved	Reserved	RO	-
34:32	pag0_tgtid2	Specifies target ID 2 for CPAG 0	RW	11'b0

The following image shows the lower register bit assignments.

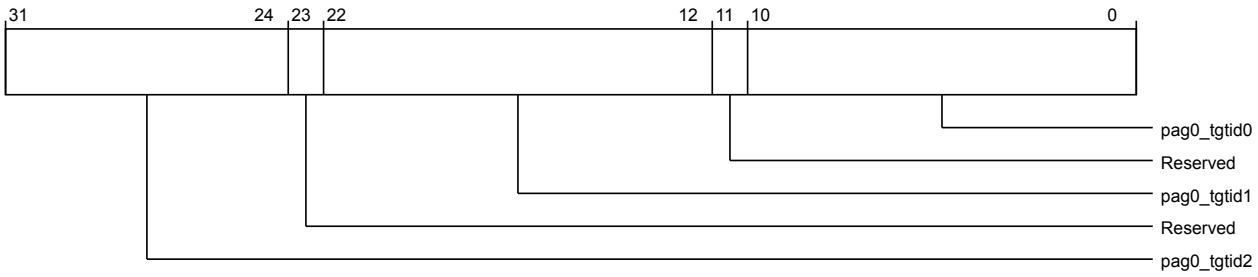


Figure 3-979 por_rnsam_cml_port_aggr_grp0_reg (low)

The following table shows the cml_port_aggr_grp0_reg lower register bit assignments.

Table 3-993 por_rnsam_cml_port_aggr_grp0_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag0_tgtid2	Specifies target ID 2 for CPAG 0	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag0_tgtid1	Specifies target ID 1 for CPAG 0	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag0_tgtid0	Specifies target ID 0 for CPAG 0	RW	11'b0

cml_port_aggr_grp1_reg

Configures the CCIX port aggregation port IDs for group 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE48

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

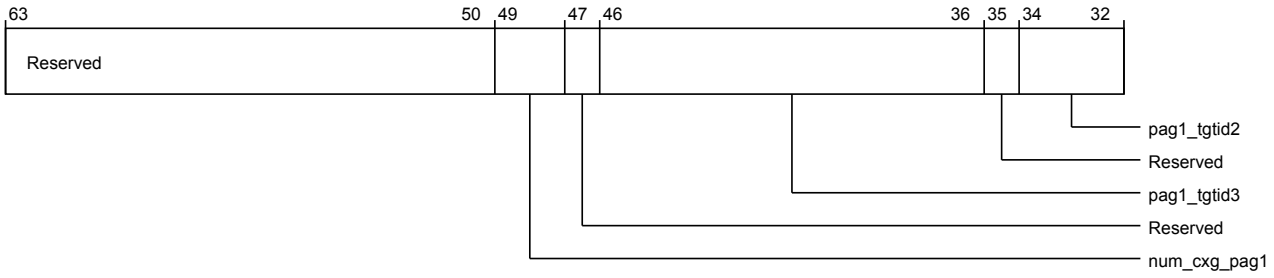


Figure 3-980 por_rnsam_cml_port_aggr_grp1_reg (high)

The following table shows the cml_port_aggr_grp1_reg higher register bit assignments.

Table 3-994 por_rnsam_cml_port_aggr_grp1_reg (high)

Bits	Field name	Description	Type	Reset
63:50	Reserved	Reserved	RO	-
49:48	num_cxg_pag1	Specifies the number of CXRAs in CPAG 1	RW	2'b0
47	Reserved	Reserved	RO	-
46:36	pag1_tgtid3	Specifies target ID 3 for CPAG 1	RW	11'b0

Table 3-994 por_rnsam_cml_port_aggr_grp1_reg (high) (continued)

Bits	Field name	Description	Type	Reset
35	Reserved	Reserved	RO	-
34:32	pag1_tgtid2	Specifies target ID 2 for CPAG 1	RW	11'b0

The following image shows the lower register bit assignments.

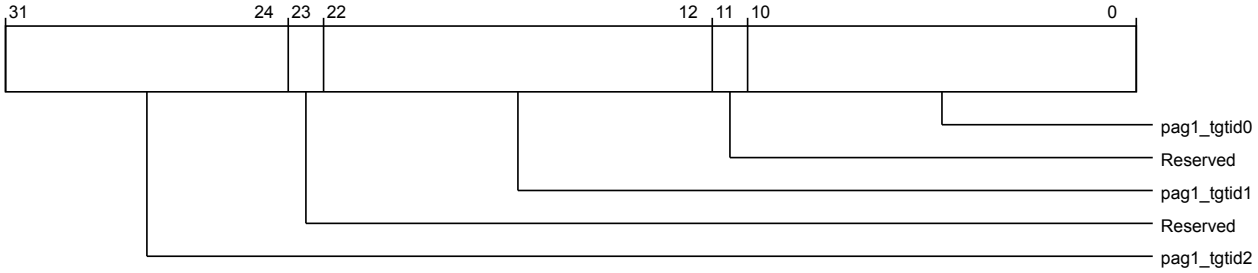


Figure 3-981 por_rnsam_cml_port_aggr_grp1_reg (low)

The following table shows the cml_port_aggr_grp1_reg lower register bit assignments.

Table 3-995 por_rnsam_cml_port_aggr_grp1_reg (low)

Bits	Field name	Description	Type	Reset
31:24	pag1_tgtid2	Specifies target ID 2 for CPAG 1	RW	11'b0
23	Reserved	Reserved	RO	-
22:12	pag1_tgtid1	Specifies target ID 1 for CPAG 1	RW	11'b0
11	Reserved	Reserved	RO	-
10:0	pag1_tgtid0	Specifies target ID 0 for CPAG 1	RW	11'b0

sys_cache_grp_secondary_reg0

Configures secondary hashed memory regions 0 and 1.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF00

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

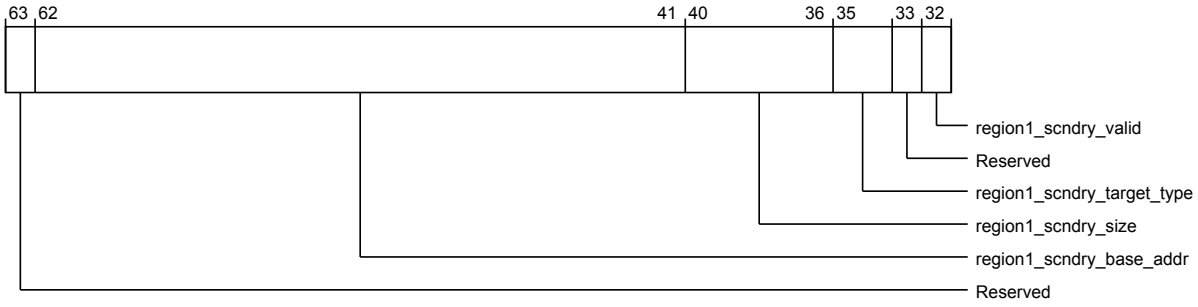


Figure 3-982 por_rnsam_sys_cache_grp_secondary_reg0 (high)

The following table shows the sys_cache_grp_secondary_reg0 higher register bit assignments.

Table 3-996 por_rnsam_sys_cache_grp_secondary_reg0 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region1_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 1 size	RW	22'b0000000000000000000000
40:36	region1_scndry_size	Secondary memory region 1 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region1_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region1_scndry_valid	Secondary memory region 1 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

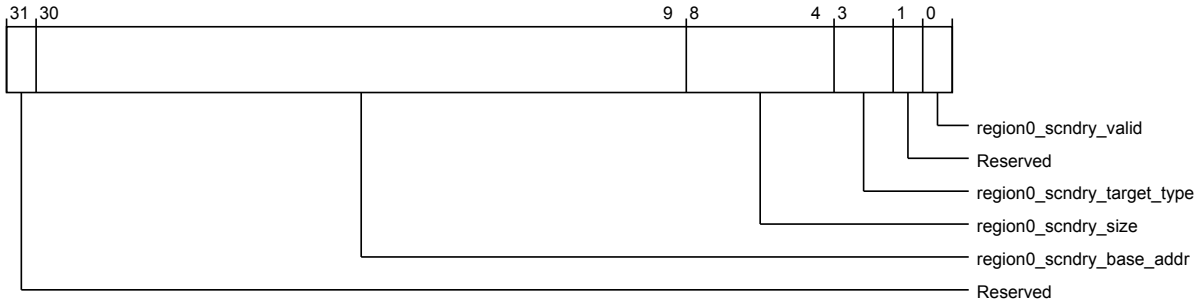


Figure 3-983 por_rnsam_sys_cache_grp_secondary_reg0 (low)

The following table shows the sys_cache_grp_secondary_reg0 lower register bit assignments.

Table 3-997 por_rnsam_sys_cache_grp_secondary_reg0 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region0_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 0 size	RW	22'b0000000000000000000000
8:4	region0_scndry_size	Secondary memory region 0 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region0_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region0_scndry_valid	Secondary memory region 0 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_secondary_reg1

Configures secondary hashed memory regions 2 and 3.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hF08
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

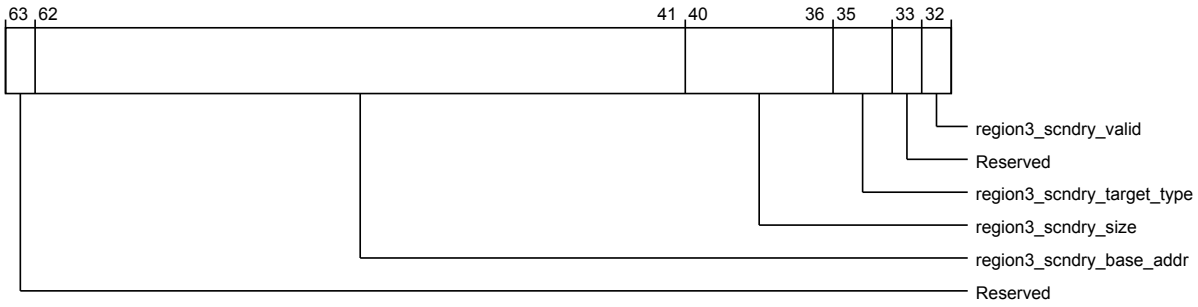


Figure 3-984 por_rnsam_sys_cache_grp_secondary_reg1 (high)

The following table shows the sys_cache_grp_secondary_reg1 higher register bit assignments.

Table 3-998 por_rnsam_sys_cache_grp_secondary_reg1 (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:41	region3_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 3 size	RW	22'b0000000000000000000000
40:36	region3_scndry_size	Secondary memory region 3 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
35:34	region3_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
33	Reserved	Reserved	RO	-
32	region3_scndry_valid	Secondary memory region 3 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

The following image shows the lower register bit assignments.

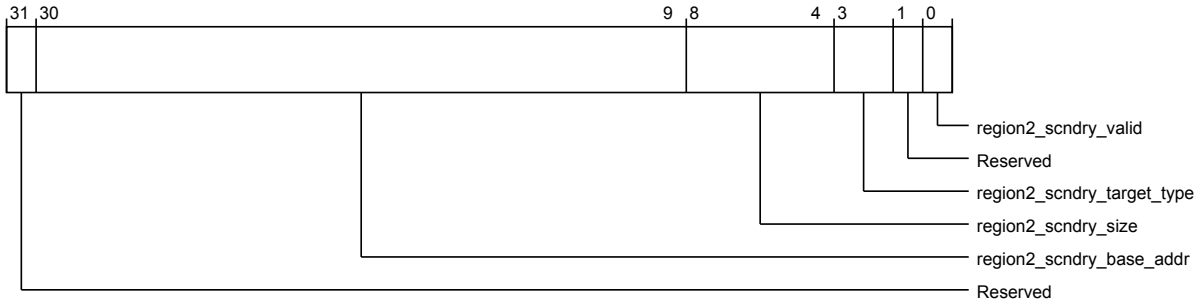


Figure 3-985 por_rnsam_sys_cache_grp_secondary_reg1 (low)

The following table shows the sys_cache_grp_secondary_reg1 lower register bit assignments.

Table 3-999 por_rnsam_sys_cache_grp_secondary_reg1 (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:9	region2_scndry_base_addr	Bits [47:26] of secondary base address of the range CONSTRAINT: Must be an integer multiple of region 2 size	RW	22'b0000000000000000000000
8:4	region2_scndry_size	Secondary memory region 2 size CONSTRAINT: Memory region must be a power of two, from minimum size supported to maximum memory size (2^address width).	RW	5'b00000
3:2	region2_scndry_target_type	Indicates secondary node type 2'b00: HN-F 2'b01: HN-I 2'b10: CXRA 2'b11: Reserved CONSTRAINT: Only applicable for RN-I	RW	2'b00
1	Reserved	Reserved	RO	-
0	region2_scndry_valid	Secondary memory region 2 valid 1'b0: Not valid 1'b1: Valid for memory region comparison	RW	1'b0

sys_cache_grp_cal_mode_reg

Configures the HN-F CAL mode support for all system cache groups.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hF10
Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

Secure group override por_rnsam_secure_register_groups_override.mem_range

The following image shows the higher register bit assignments.

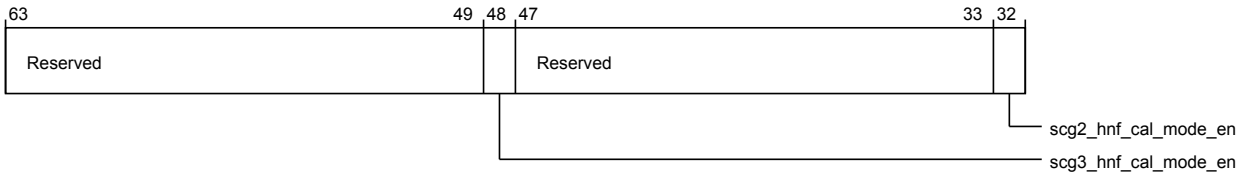


Figure 3-986 por_rnsam_sys_cache_grp_cal_mode_reg (high)

The following table shows the sys_cache_grp_cal_mode_reg higher register bit assignments.

Table 3-1000 por_rnsam_sys_cache_grp_cal_mode_reg (high)

Bits	Field name	Description	Type	Reset
63:49	Reserved	Reserved	RO	-
48	scg3_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 3	RW	1'b0
47:33	Reserved	Reserved	RO	-
32	scg2_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 2	RW	1'b0

The following image shows the lower register bit assignments.

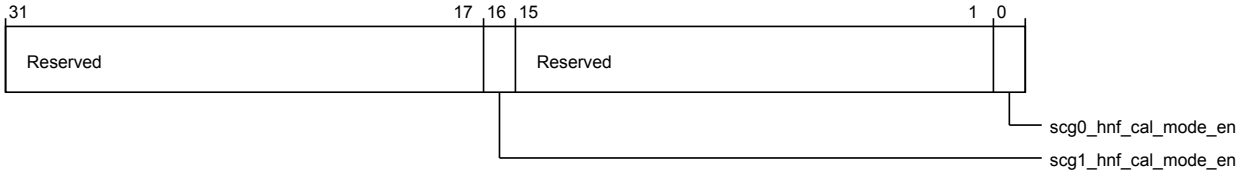


Figure 3-987 por_rnsam_sys_cache_grp_cal_mode_reg (low)

The following table shows the sys_cache_grp_cal_mode_reg lower register bit assignments.

Table 3-1001 por_rnsam_sys_cache_grp_cal_mode_reg (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	scg1_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 1	RW	1'b0
15:1	Reserved	Reserved	RO	-
0	scg0_hnf_cal_mode_en	Enables support for HN-F CAL for SCG 0	RW	1'b0

rnsam_hash_addr_mask_reg

Configures the address mask that is applied before hashing the address bits.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF18

Register reset 64'b1111111111111111111111111111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

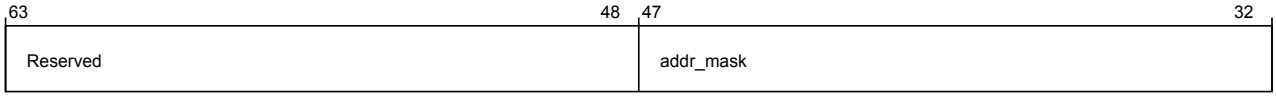


Figure 3-988 por_rnsam_rnsam_hash_addr_mask_reg (high)

The following table shows the rnsam_hash_addr_mask_reg higher register bit assignments.

Table 3-1002 por_rnsam_rnsam_hash_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF

The following image shows the lower register bit assignments.

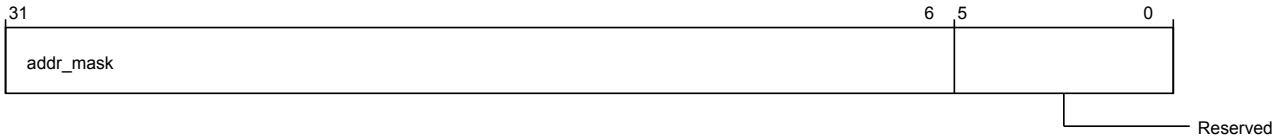


Figure 3-989 por_rnsam_rnsam_hash_addr_mask_reg (low)

The following table shows the rnsam_hash_addr_mask_reg lower register bit assignments.

Table 3-1003 por_rnsam_rnsam_hash_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:6	addr_mask	Address mask applied before hashing	RW	42'h3FFFFFFFFF
5:0	Reserved	Reserved	RO	-

rnsam_region_cmp_addr_mask_reg

Configures the address mask that is applied before region compare.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF20

Register reset 64'b11111111111111111111111111111111

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device. and This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

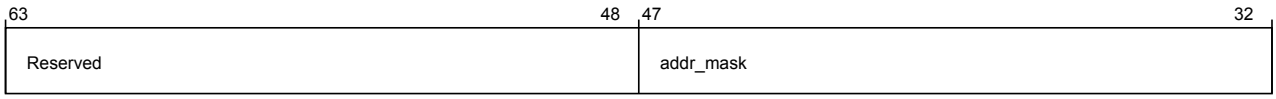


Figure 3-990 por_rnsam_rnsam_region_cmp_addr_mask_reg (high)

The following table shows the rnsam_region_cmp_addr_mask_reg higher register bit assignments.

Table 3-1004 por_rnsam_rnsam_region_cmp_addr_mask_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	addr_mask	Address mask applied before memory region compare	RW	32'hFFFFFFFF

The following image shows the lower register bit assignments.

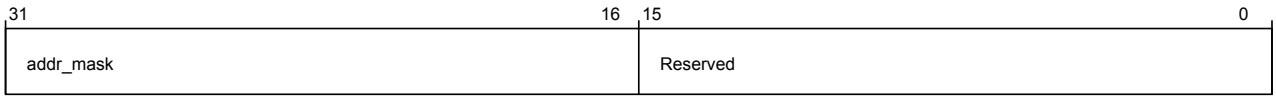


Figure 3-991 por_rnsam_rnsam_region_cmp_addr_mask_reg (low)

The following table shows the rnsam_region_cmp_addr_mask_reg lower register bit assignments.

Table 3-1005 por_rnsam_rnsam_region_cmp_addr_mask_reg (low)

Bits	Field name	Description	Type	Reset
31:16	addr_mask	Address mask applied before memory region compare	RW	32'hFFFFFFFF
15:0	Reserved	Reserved	RO	-

sys_cache_grp_hn_nodeid_reg8

Configures hashed node IDs for system cache groups. Controls target HN node IDs 32 to 35.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF58

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

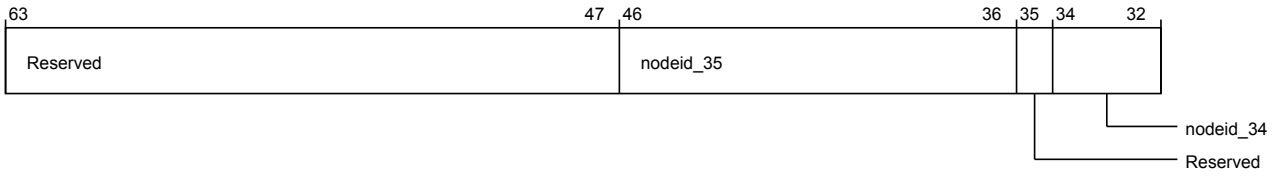


Figure 3-992 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg8 higher register bit assignments.

Table 3-1006 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_35	Hashed target node ID 35	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_34	Hashed target node ID 34	RW	11'b00000000000

The following image shows the lower register bit assignments.

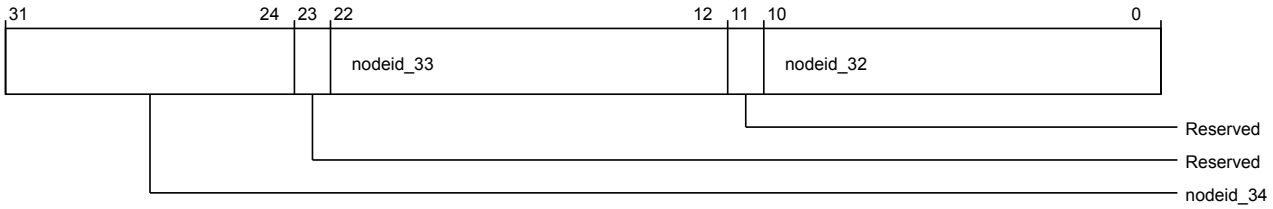


Figure 3-993 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg8 lower register bit assignments.

Table 3-1007 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_34	Hashed target node ID 34	RW	11'b00000000000
23	Reserved	Reserved	RO	-

Table 3-1007 por_rnsam_sys_cache_grp_hn_nodeid_reg8 (low) (continued)

Bits	Field name	Description	Type	Reset
22:12	nodeid_33	Hashed target node ID 33	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_32	Hashed target node ID 32	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg9

Configures hashed node IDs for system cache groups. Controls target HN node IDs 36 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF60

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

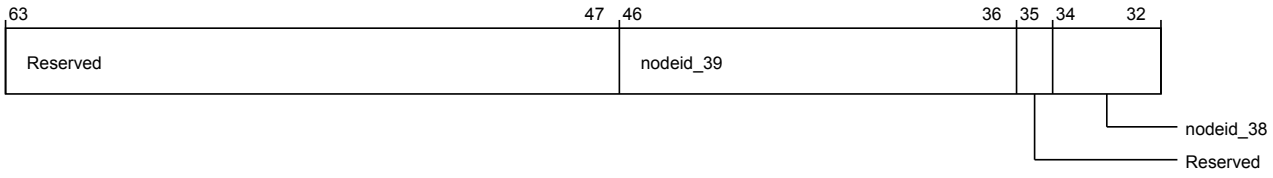


Figure 3-994 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg9 higher register bit assignments.

Table 3-1008 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_39	Hashed target node ID 39	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_38	Hashed target node ID 38	RW	11'b00000000000

The following image shows the lower register bit assignments.

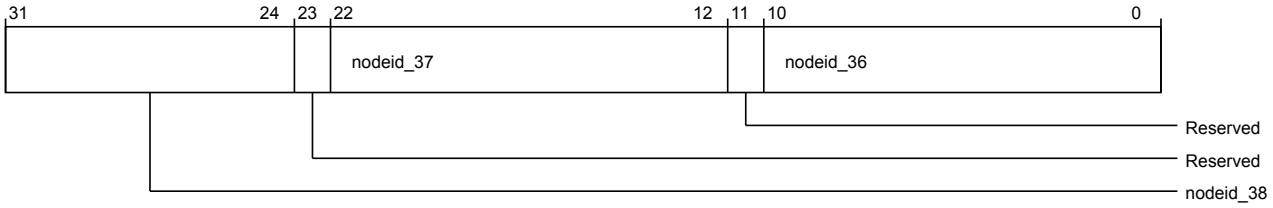


Figure 3-995 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg9 lower register bit assignments.

Table 3-1009 por_rnsam_sys_cache_grp_hn_nodeid_reg9 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_38	Hashed target node ID 38	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_37	Hashed target node ID 37	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_36	Hashed target node ID 36	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg10

Configures hashed node IDs for system cache groups. Controls target HN node IDs 40 to 43.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF68

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

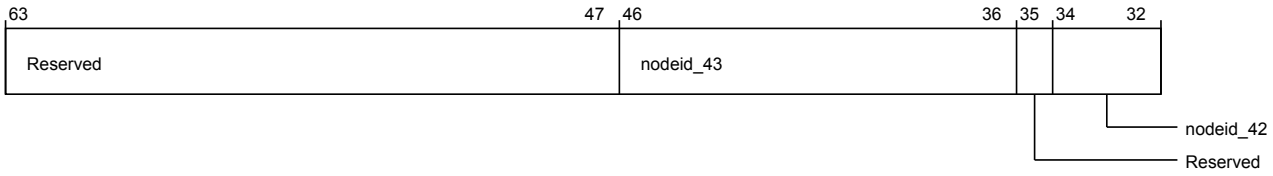


Figure 3-996 por_rnsam_sys_cache_grp_hn_nodeid_reg10 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg10 higher register bit assignments.

Table 3-1010 por_rnsam_sys_cache_grp_hn_nodeid_reg10 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_43	Hashed target node ID 43	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_42	Hashed target node ID 42	RW	11'b00000000000

The following image shows the lower register bit assignments.

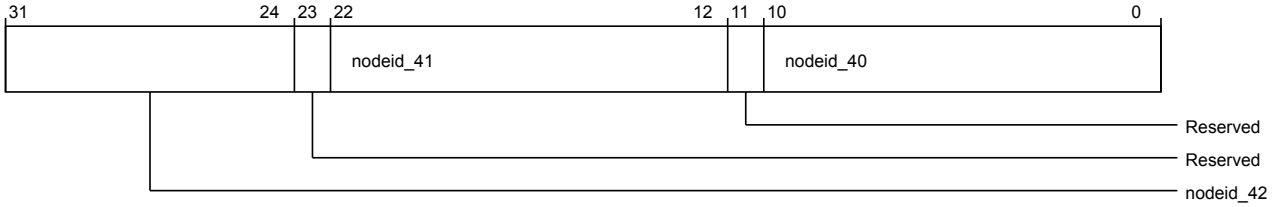


Figure 3-997 por_rnsam_sys_cache_grp_hn_nodeid_reg10 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg10 lower register bit assignments.

Table 3-1011 por_rnsam_sys_cache_grp_hn_nodeid_reg10 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_42	Hashed target node ID 42	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_41	Hashed target node ID 41	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_40	Hashed target node ID 40	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg11

Configures hashed node IDs for system cache groups. Controls target HN node IDs 44 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF70

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

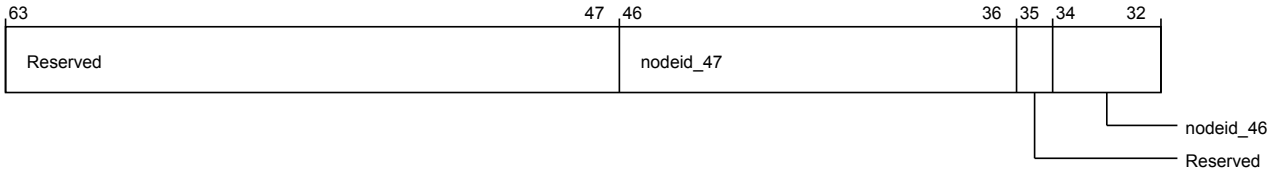


Figure 3-998 por_rnsam_sys_cache_grp_hn_nodeid_reg11 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg11 higher register bit assignments.

Table 3-1012 por_rnsam_sys_cache_grp_hn_nodeid_reg11 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_47	Hashed target node ID 47	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_46	Hashed target node ID 46	RW	11'b00000000000

The following image shows the lower register bit assignments.

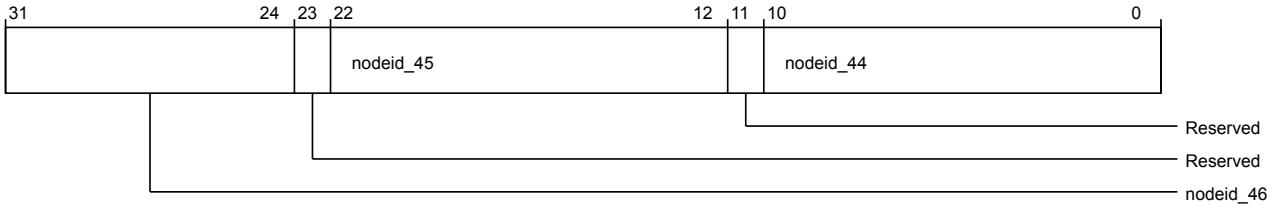


Figure 3-999 por_rnsam_sys_cache_grp_hn_nodeid_reg11 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg11 lower register bit assignments.

Table 3-1013 por_rnsam_sys_cache_grp_hn_nodeid_reg11 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_46	Hashed target node ID 46	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_45	Hashed target node ID 45	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_44	Hashed target node ID 44	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg12

Configures hashed node IDs for system cache groups. Controls target HN node IDs 48 to 51.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF78

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

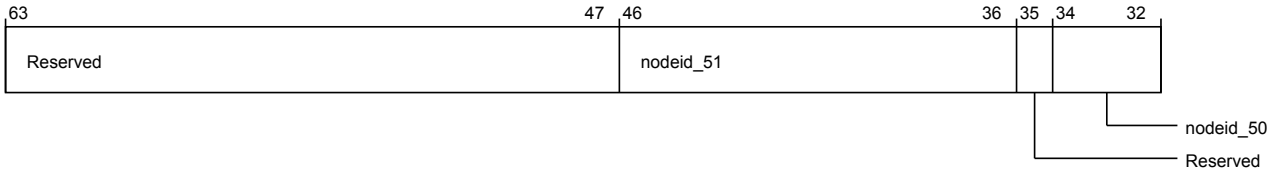


Figure 3-1000 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg12 higher register bit assignments.

Table 3-1014 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_51	Hashed target node ID 51	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_50	Hashed target node ID 50	RW	11'b00000000000

The following image shows the lower register bit assignments.

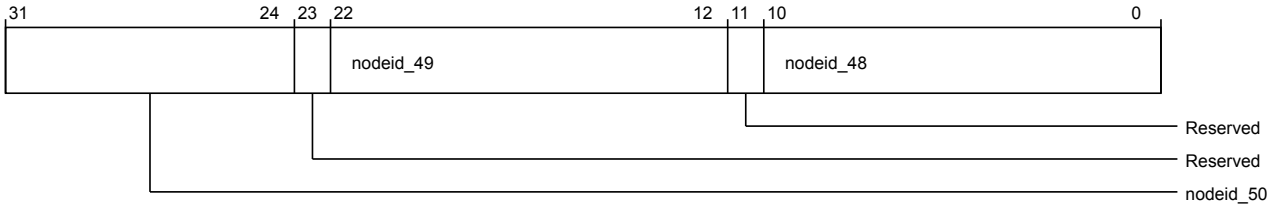


Figure 3-1001 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg12 lower register bit assignments.

Table 3-1015 por_rnsam_sys_cache_grp_hn_nodeid_reg12 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_50	Hashed target node ID 50	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_49	Hashed target node ID 49	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_48	Hashed target node ID 48	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg13

Configures hashed node IDs for system cache groups. Controls target HN node IDs 52 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF80

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

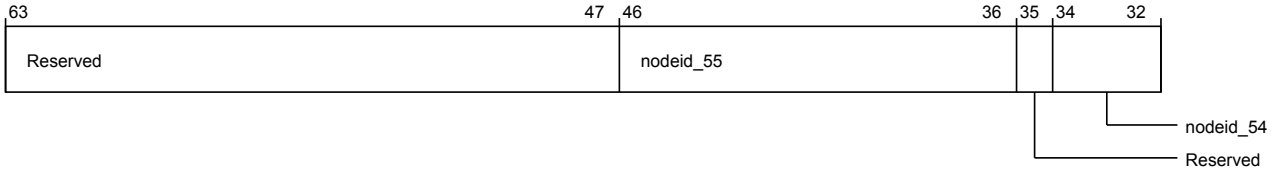


Figure 3-1002 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg13 higher register bit assignments.

Table 3-1016 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_55	Hashed target node ID 55	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_54	Hashed target node ID 54	RW	11'b00000000000

The following image shows the lower register bit assignments.

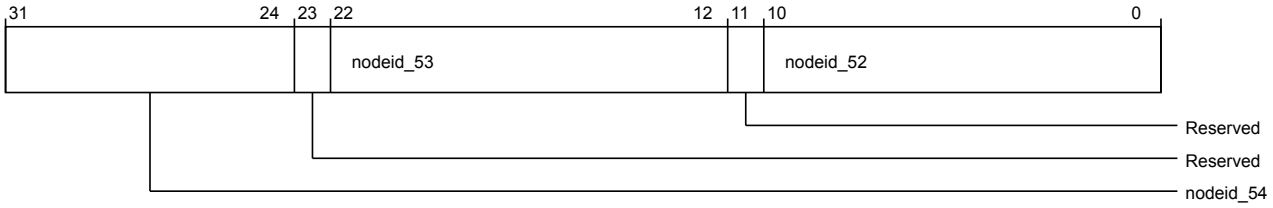


Figure 3-1003 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg13 lower register bit assignments.

Table 3-1017 por_rnsam_sys_cache_grp_hn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_54	Hashed target node ID 54	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_53	Hashed target node ID 53	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_52	Hashed target node ID 52	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg14

Configures hashed node IDs for system cache groups. Controls target HN node IDs 56 to 59.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF88

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

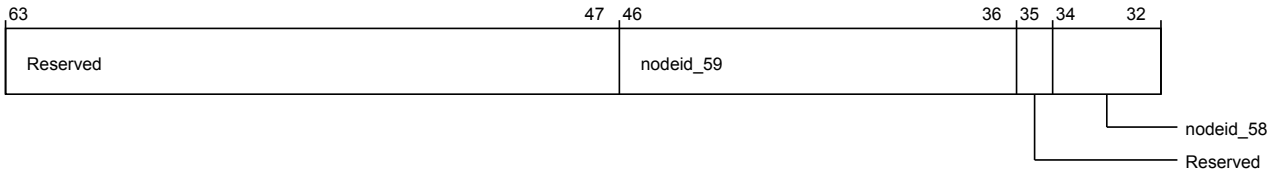


Figure 3-1004 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg14 higher register bit assignments.

Table 3-1018 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_59	Hashed target node ID 59	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_58	Hashed target node ID 58	RW	11'b00000000000

The following image shows the lower register bit assignments.

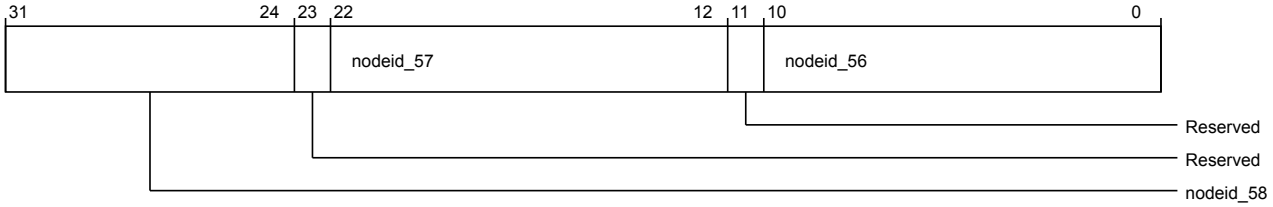


Figure 3-1005 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg14 lower register bit assignments.

Table 3-1019 por_rnsam_sys_cache_grp_hn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_58	Hashed target node ID 58	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_57	Hashed target node ID 57	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_56	Hashed target node ID 56	RW	11'b00000000000

sys_cache_grp_hn_nodeid_reg15

Configures hashed node IDs for system cache groups. Controls target HN node IDs 60 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF90

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

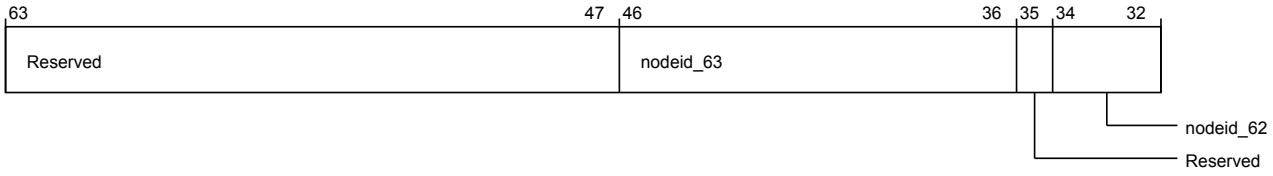


Figure 3-1006 por_rnsam_sys_cache_grp_hn_nodeid_reg15 (high)

The following table shows the sys_cache_grp_hn_nodeid_reg15 higher register bit assignments.

Table 3-1020 por_rnsam_sys_cache_grp_hn_nodeid_reg15 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	nodeid_63	Hashed target node ID 63	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	nodeid_62	Hashed target node ID 62	RW	11'b00000000000

The following image shows the lower register bit assignments.

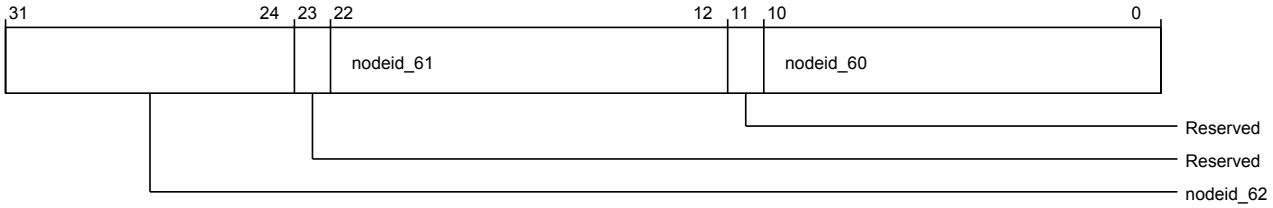


Figure 3-1007 por_rnsam_sys_cache_grp_hn_nodeid_reg15 (low)

The following table shows the sys_cache_grp_hn_nodeid_reg15 lower register bit assignments.

Table 3-1021 por_rnsam_sys_cache_grp_hn_nodeid_reg15 (low)

Bits	Field name	Description	Type	Reset
31:24	nodeid_62	Hashed target node ID 62	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	nodeid_61	Hashed target node ID 61	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	nodeid_60	Hashed target node ID 60	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg8

Configures hashed node IDs for system cache groups. Controls target SN node IDs 32 to 35.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1008

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

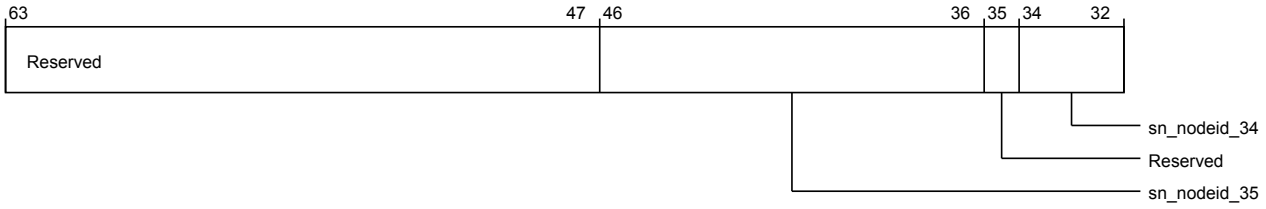


Figure 3-1008 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg8 higher register bit assignments.

Table 3-1022 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_35	Hashed target SN node ID 35	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b00000000000

The following image shows the lower register bit assignments.

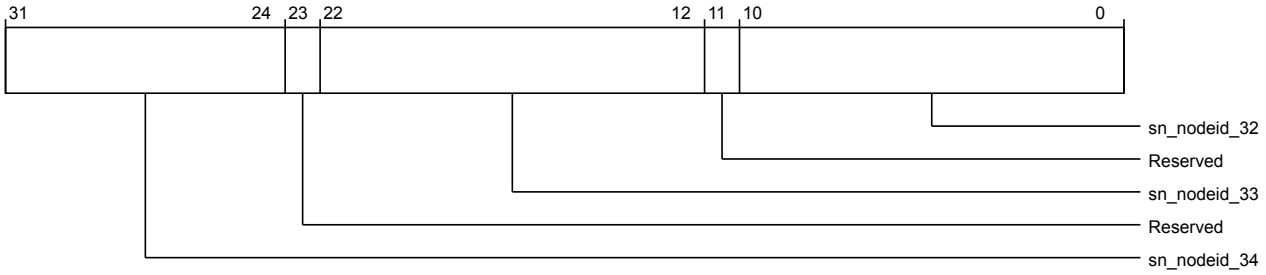


Figure 3-1009 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg8 lower register bit assignments.

Table 3-1023 por_rnsam_sys_cache_grp_sn_nodeid_reg8 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_34	Hashed target SN node ID 34	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_33	Hashed target SN node ID 33	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_32	Hashed target SN node ID 32	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg9

Configures hashed node IDs for system cache groups. Controls target SN node IDs 36 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

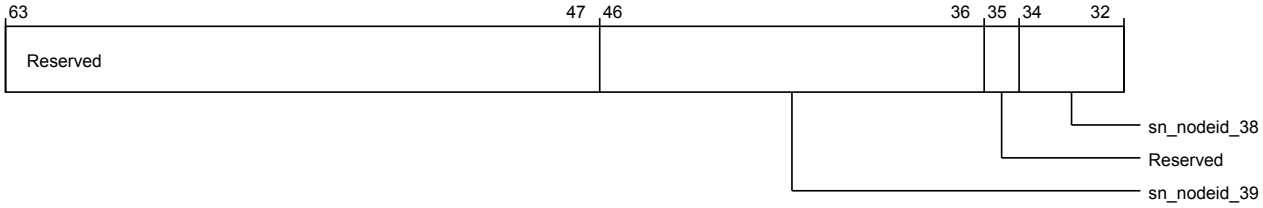


Figure 3-1010 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg9 higher register bit assignments.

Table 3-1024 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_39	Hashed target SN node ID 39	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b00000000000

The following image shows the lower register bit assignments.

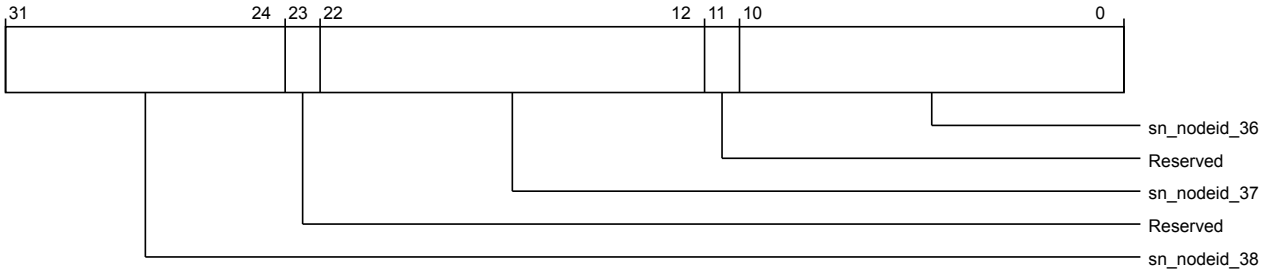


Figure 3-1011 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg9 lower register bit assignments.

Table 3-1025 por_rnsam_sys_cache_grp_sn_nodeid_reg9 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_38	Hashed target SN node ID 38	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_37	Hashed target SN node ID 37	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_36	Hashed target SN node ID 36	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg10

Configures hashed node IDs for system cache groups. Controls target SN node IDs 40 to 43.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1018

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

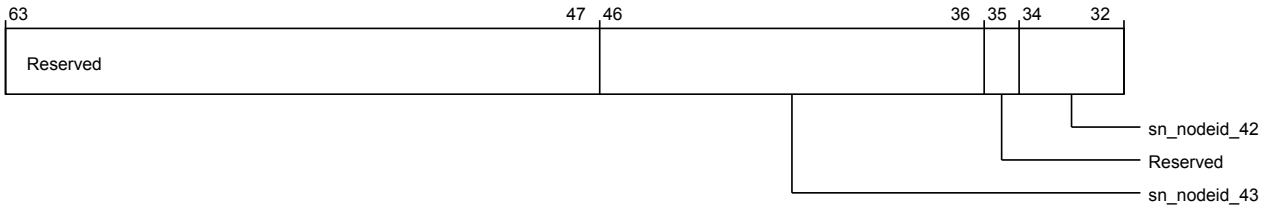


Figure 3-1012 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg10 higher register bit assignments.

Table 3-1026 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_43	Hashed target SN node ID 43	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b00000000000

The following image shows the lower register bit assignments.

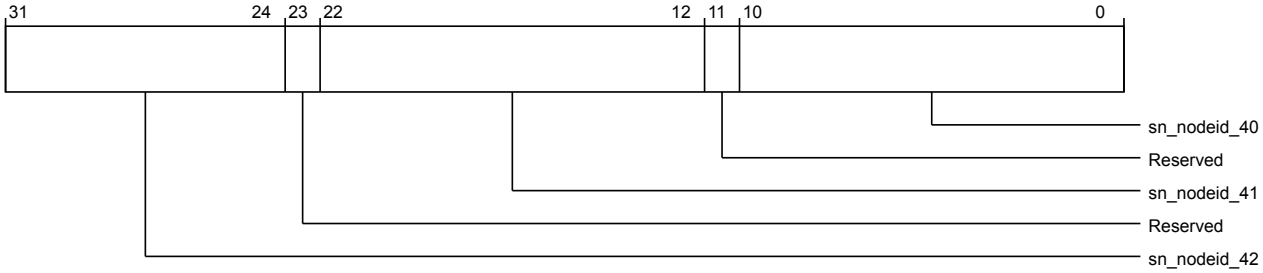


Figure 3-1013 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg10 lower register bit assignments.

Table 3-1027 por_rnsam_sys_cache_grp_sn_nodeid_reg10 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_42	Hashed target SN node ID 42	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_41	Hashed target SN node ID 41	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_40	Hashed target SN node ID 40	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg11

Configures hashed node IDs for system cache groups. Controls target SN node IDs 44 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1020

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

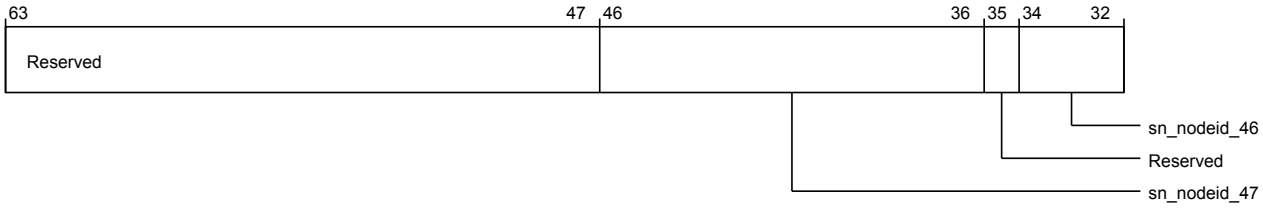


Figure 3-1014 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg11 higher register bit assignments.

Table 3-1028 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_47	Hashed target SN node ID 47	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b00000000000

The following image shows the lower register bit assignments.

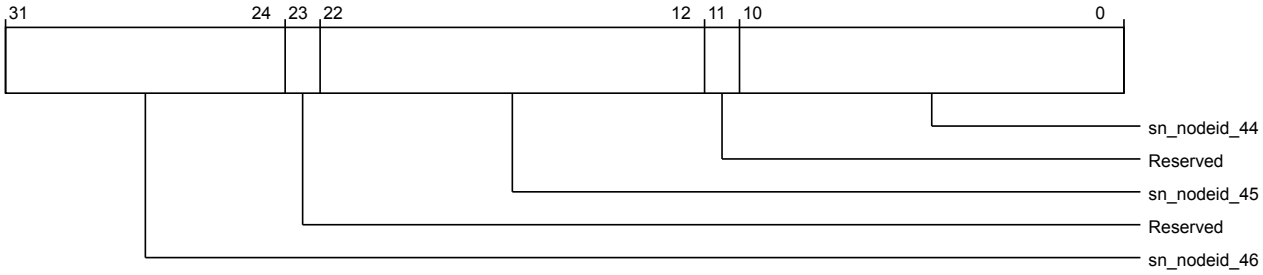


Figure 3-1015 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg11 lower register bit assignments.

Table 3-1029 por_rnsam_sys_cache_grp_sn_nodeid_reg11 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_46	Hashed target SN node ID 46	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_45	Hashed target SN node ID 45	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_44	Hashed target SN node ID 44	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg12

Configures hashed node IDs for system cache groups. Controls target SN node IDs 48 to 51.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1028

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

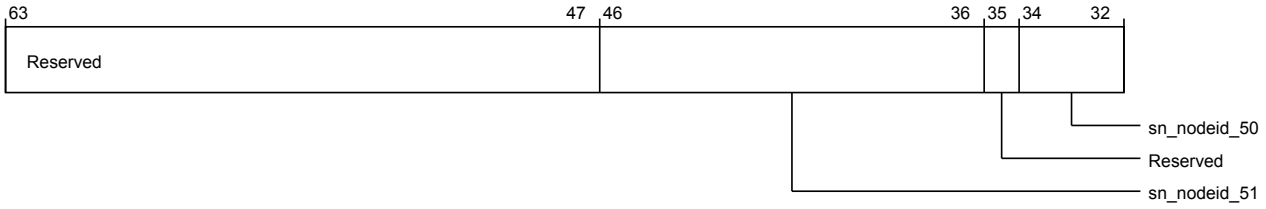


Figure 3-1016 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg12 higher register bit assignments.

Table 3-1030 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_51	Hashed target SN node ID 51	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_50	Hashed target SN node ID 50	RW	11'b00000000000

The following image shows the lower register bit assignments.

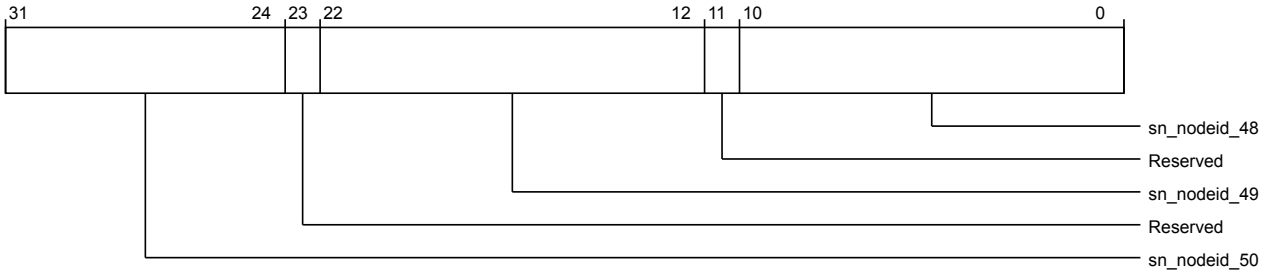


Figure 3-1017 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg12 lower register bit assignments.

Table 3-1031 por_rnsam_sys_cache_grp_sn_nodeid_reg12 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_50	Hashed target SN node ID 50	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_49	Hashed target SN node ID 49	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_48	Hashed target SN node ID 48	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg13

Configures hashed node IDs for system cache groups. Controls target SN node IDs 52 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1030

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

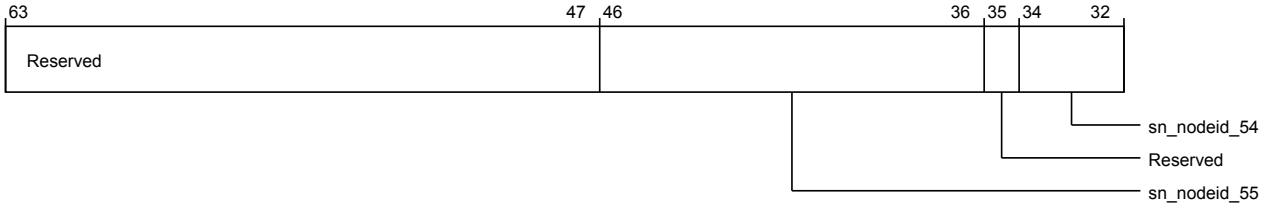


Figure 3-1018 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg13 higher register bit assignments.

Table 3-1032 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_55	Hashed target SN node ID 55	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_54	Hashed target SN node ID 54	RW	11'b00000000000

The following image shows the lower register bit assignments.

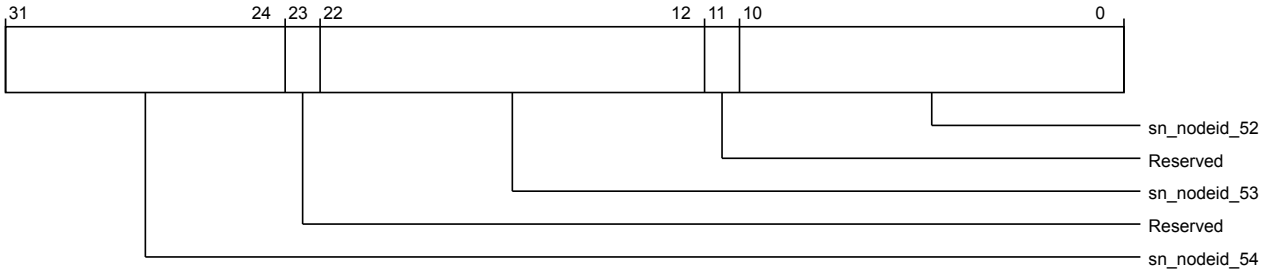


Figure 3-1019 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg13 lower register bit assignments.

Table 3-1033 por_rnsam_sys_cache_grp_sn_nodeid_reg13 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_54	Hashed target SN node ID 54	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_53	Hashed target SN node ID 53	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_52	Hashed target SN node ID 52	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg14

Configures hashed node IDs for system cache groups. Controls target SN node IDs 56 to 59.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1038

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

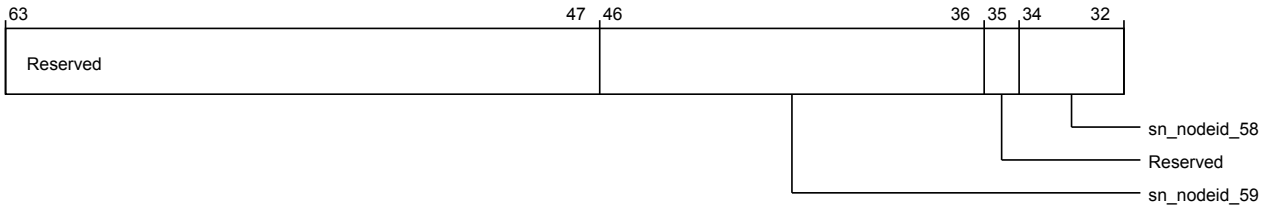


Figure 3-1020 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg14 higher register bit assignments.

Table 3-1034 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_59	Hashed target SN node ID 59	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b00000000000

The following image shows the lower register bit assignments.

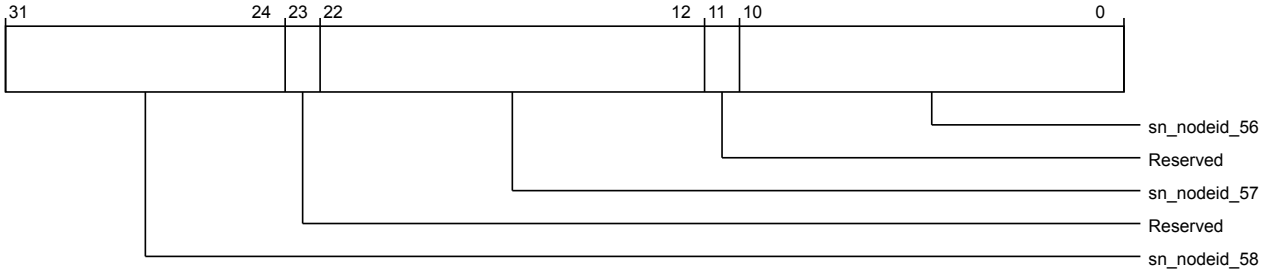


Figure 3-1021 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg14 lower register bit assignments.

Table 3-1035 por_rnsam_sys_cache_grp_sn_nodeid_reg14 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_58	Hashed target SN node ID 58	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_57	Hashed target SN node ID 57	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_56	Hashed target SN node ID 56	RW	11'b00000000000

sys_cache_grp_sn_nodeid_reg15

Configures hashed node IDs for system cache groups. Controls target SN node IDs 60 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1040

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

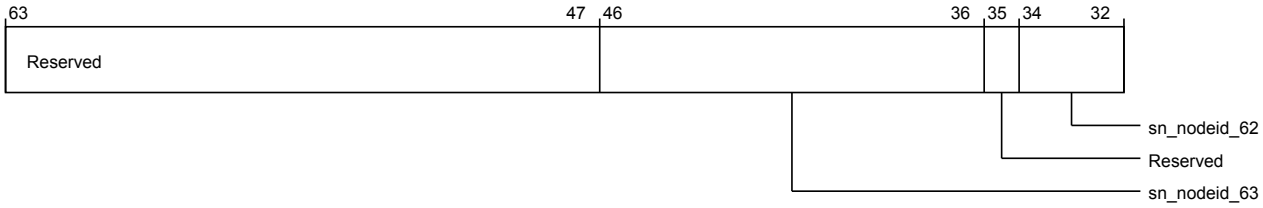


Figure 3-1022 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)

The following table shows the sys_cache_grp_sn_nodeid_reg15 higher register bit assignments.

Table 3-1036 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (high)

Bits	Field name	Description	Type	Reset
63:47	Reserved	Reserved	RO	-
46:36	sn_nodeid_63	Hashed target SN node ID 63	RW	11'b00000000000
35	Reserved	Reserved	RO	-
34:32	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b00000000000

The following image shows the lower register bit assignments.

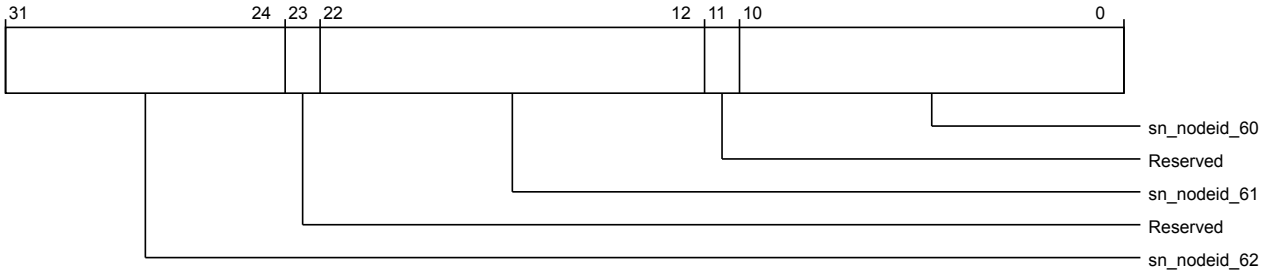


Figure 3-1023 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)

The following table shows the sys_cache_grp_sn_nodeid_reg15 lower register bit assignments.

Table 3-1037 por_rnsam_sys_cache_grp_sn_nodeid_reg15 (low)

Bits	Field name	Description	Type	Reset
31:24	sn_nodeid_62	Hashed target SN node ID 62	RW	11'b00000000000
23	Reserved	Reserved	RO	-
22:12	sn_nodeid_61	Hashed target SN node ID 61	RW	11'b00000000000
11	Reserved	Reserved	RO	-
10:0	sn_nodeid_60	Hashed target SN node ID 60	RW	11'b00000000000

3.3.10 SBSX register descriptions

This section lists the SBSX registers.

por_sbsx_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

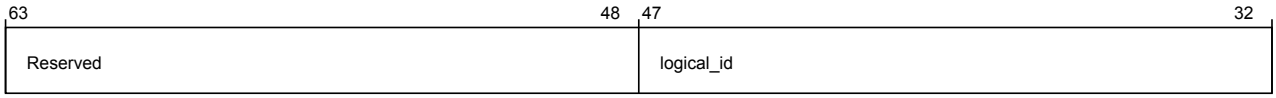


Figure 3-1024 por_sbsx_por_sbsx_node_info (high)

The following table shows the por_sbsx_node_info higher register bit assignments.

Table 3-1038 por_sbsx_por_sbsx_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

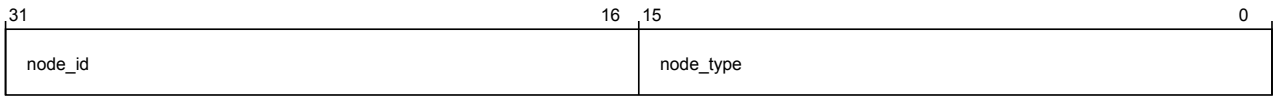


Figure 3-1025 por_sbsx_por_sbsx_node_info (low)

The following table shows the por_sbsx_node_info lower register bit assignments.

Table 3-1039 por_sbsx_por_sbsx_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0007

por_sbsx_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

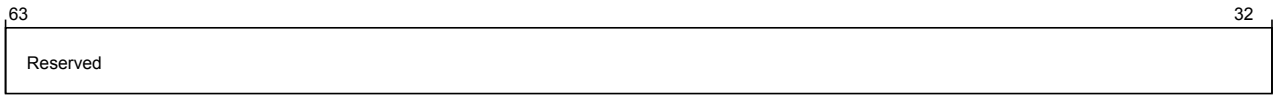


Figure 3-1026 por_sbsx_por_sbsx_child_info (high)

The following table shows the por_sbsx_child_info higher register bit assignments.

Table 3-1040 por_sbsx_por_sbsx_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

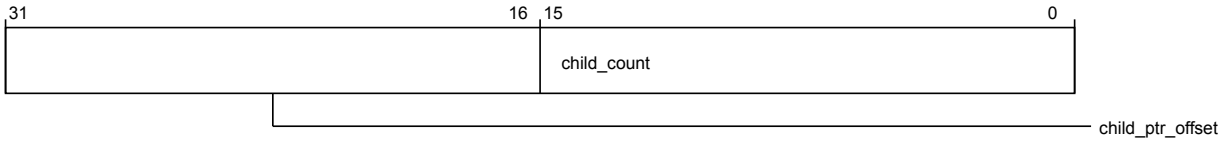


Figure 3-1027 por_sbsx_por_sbsx_child_info (low)

The following table shows the por_sbsx_child_info lower register bit assignments.

Table 3-1041 por_sbsx_por_sbsx_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_sbsx_unit_info

Provides component identification information for SBSX.

Its characteristics are:

Type RO
Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

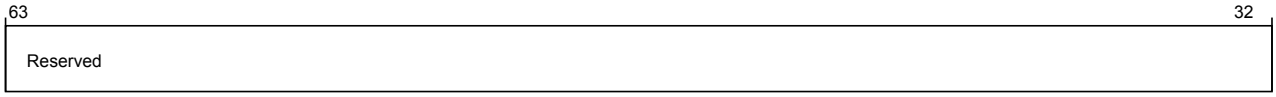


Figure 3-1028 por_sbsx_por_sbsx_unit_info (high)

The following table shows the por_sbsx_unit_info higher register bit assignments.

Table 3-1042 por_sbsx_por_sbsx_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

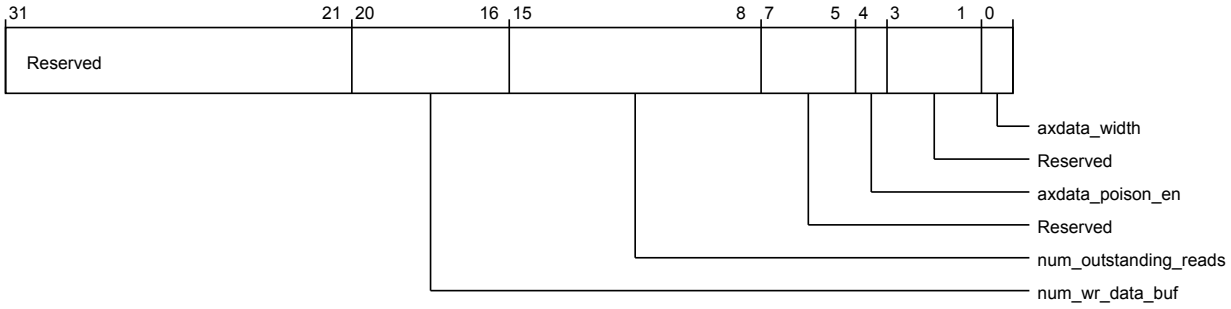


Figure 3-1029 por_sbsx_por_sbsx_unit_info (low)

The following table shows the por_sbsx_unit_info lower register bit assignments.

Table 3-1043 por_sbsx_por_sbsx_unit_info (low)

Bits	Field name	Description	Type	Reset
31:21	Reserved	Reserved	RO	-
20:16	num_wr_data_buf	Number of write data buffers in SBSX	RO	Configuration dependent
15:8	num_outstanding_reads	Maximum number of outstanding AXI read requests from SBSX	RO	Configuration dependent
7:5	Reserved	Reserved	RO	-
4	axdata_poison_en	Data poison support on ACE-Lite/AXI4 interface 1'b0: Not supported 1'b1: Supported	RO	Configuration dependent

Table 3-1043 por_sbsx_por_sbsx_unit_info (low) (continued)

Bits	Field name	Description	Type	Reset
3:1	Reserved	Reserved	RO	-
0	axdata_width	Data width on ACE-Lite/AXI4 interface 1'b0: 128 bits 1'b1: 256 bits	RO	Configuration dependent

por_sbsx_aux_ctl

Functions as the auxiliary control register for the SBSX bridge.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 64'b0

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

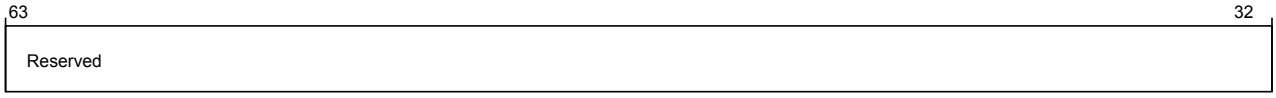


Figure 3-1030 por_sbsx_por_sbsx_aux_ctl (high)

The following table shows the por_sbsx_aux_ctl higher register bit assignments.

Table 3-1044 por_sbsx_por_sbsx_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

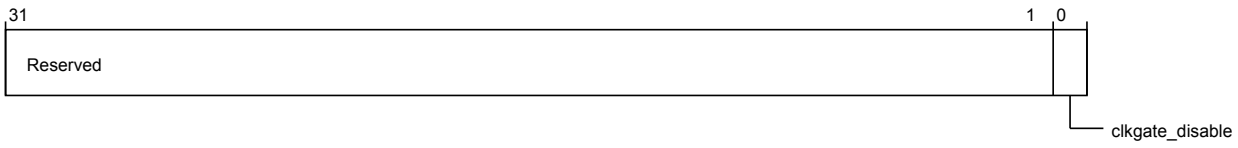


Figure 3-1031 por_sbsx_por_sbsx_aux_ctl (low)

The following table shows the por_sbsx_aux_ctl lower register bit assignments.

Table 3-1045 por_sbsx_por_sbsx_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:1	Reserved	Reserved	RO	-
0	clkgate_disable	Disables internal clock gating in SBSX bridge	RW	1'b0

por_sbsx_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b0000010100001
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

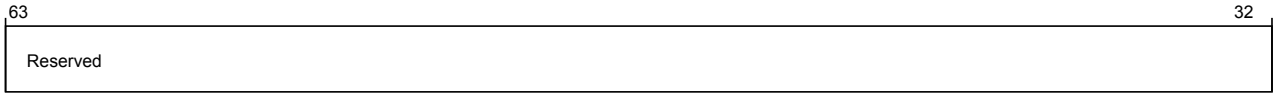


Figure 3-1032 por_sbsx_por_sbsx_errfr (high)

The following table shows the por_sbsx_errfr higher register bit assignments.

Table 3-1046 por_sbsx_por_sbsx_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

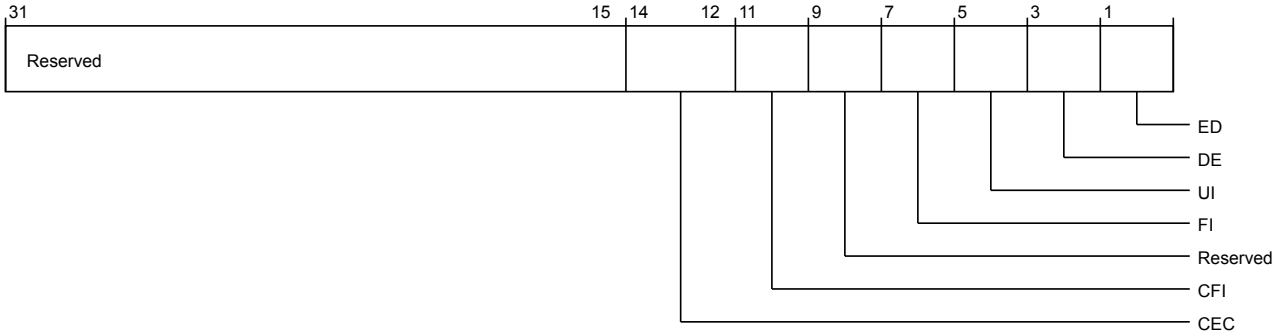


Figure 3-1033 por_sbsx_por_sbsx_errfr (low)

The following table shows the por_sbsx_errfr lower register bit assignments.

Table 3-1047 por_sbsx_por_sbsx_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

por_sbsx_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3008
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

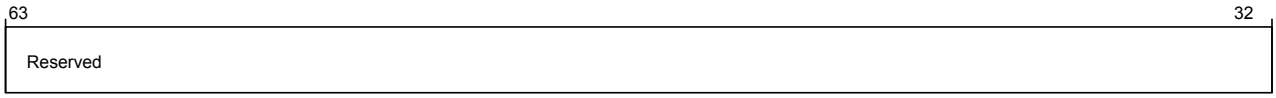


Figure 3-1034 por_sbsx_por_sbsx_errctlr (high)

The following table shows the por_sbsx_errctlr higher register bit assignments.

Table 3-1048 por_sbsx_por_sbsx_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

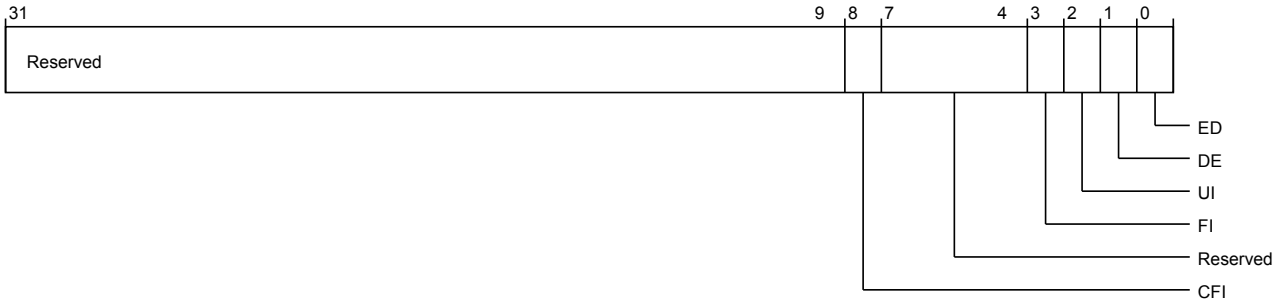


Figure 3-1035 por_sbsx_por_sbsx_errctlr (low)

The following table shows the por_sbsx_errctlr lower register bit assignments.

Table 3-1049 por_sbsx_por_sbsx_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_sbsx_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_sbsx_errfr.ED	RW	1'b0

por_sbsx_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3010
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

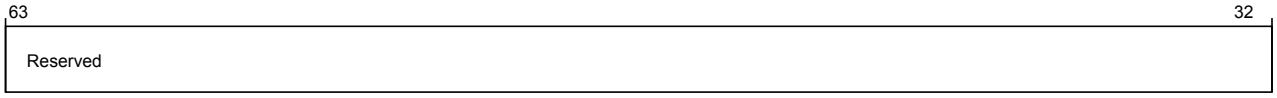


Figure 3-1036 por_sbsx_por_sbsx_errstatus (high)

The following table shows the por_sbsx_errstatus higher register bit assignments.

Table 3-1050 por_sbsx_por_sbsx_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-1037 por_sbsx_por_sbsx_errstatus (low)

The following table shows the por_sbsx_errstatus lower register bit assignments.

Table 3-1051 por_sbsx_por_sbsx_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_sbsx_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0

Table 3-1051 por_sbsx_por_sbsx_errstatus (low) (continued)

Bits	Field name	Description	Type	Reset
26	MV	por_sbsx_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_sbsx_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

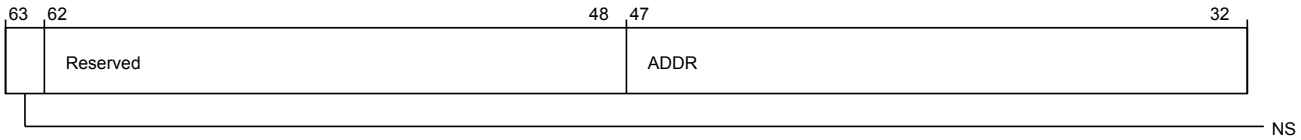


Figure 3-1038 por_sbsx_por_sbsx_erraddr (high)

The following table shows the por_sbsx_erraddr higher register bit assignments.

Table 3-1052 por_sbsx_por_sbsx_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_sbsx_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

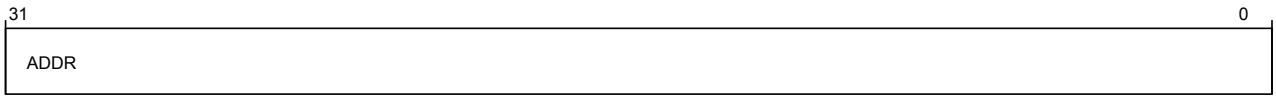


Figure 3-1039 por_sbsx_por_sbsx_erraddr (low)

The following table shows the por_sbsx_erraddr lower register bit assignments.

Table 3-1053 por_sbsx_por_sbsx_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_sbsx_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/ uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

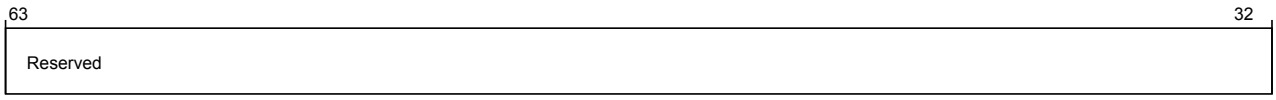


Figure 3-1040 por_sbsx_por_sbsx_errmisc (high)

The following table shows the por_sbsx_errmisc higher register bit assignments.

Table 3-1054 por_sbsx_por_sbsx_errmisc (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

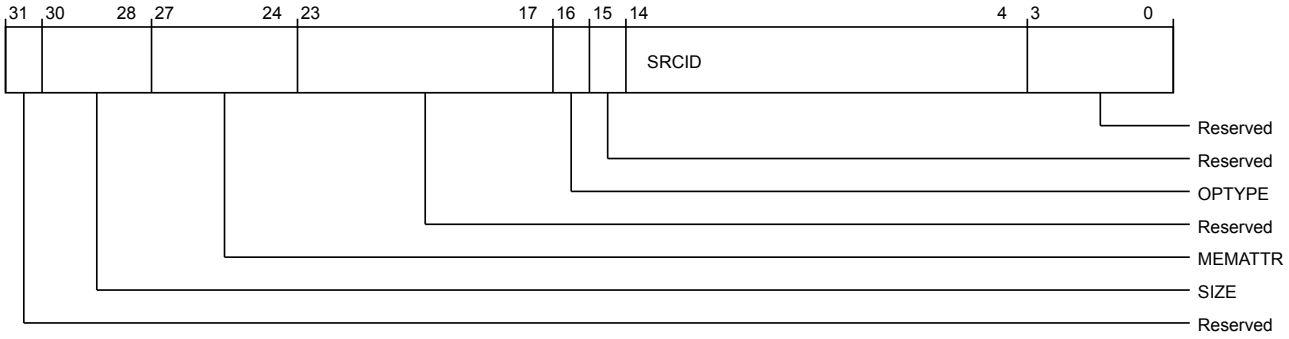


Figure 3-1041 por_sbsx_por_sbsx_errmisc (low)

The following table shows the por_sbsx_errmisc lower register bit assignments.

Table 3-1055 por_sbsx_por_sbsx_errmisc (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

por_sbsx_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3100
Register reset 64'b0000010100001

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

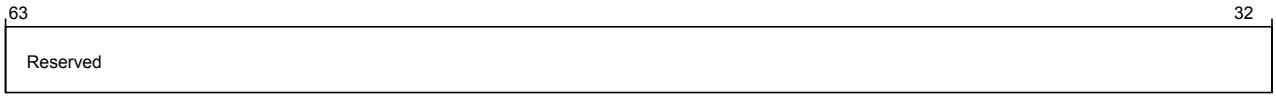


Figure 3-1042 por_sbsx_por_sbsx_errfr_ns (high)

The following table shows the por_sbsx_errfr_NS higher register bit assignments.

Table 3-1056 por_sbsx_por_sbsx_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

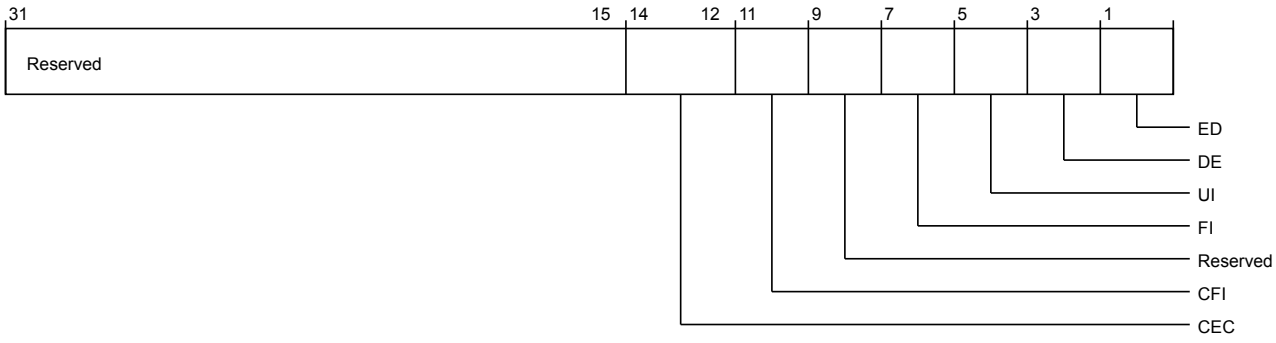


Figure 3-1043 por_sbsx_por_sbsx_errfr_ns (low)

The following table shows the por_sbsx_errfr_NS lower register bit assignments.

Table 3-1057 por_sbsx_por_sbsx_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10

Table 3-1057 por_sbsx_por_sbsx_errfr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	DE	Deferred errors	RO	2'b00
1:0	ED	Error detection	RO	2'b01

por_sbsx_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

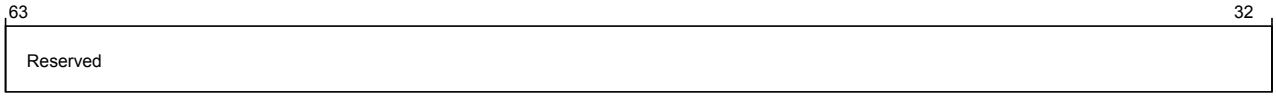


Figure 3-1044 por_sbsx_por_sbsx_errctlr_ns (high)

The following table shows the por_sbsx_errctlr_NS higher register bit assignments.

Table 3-1058 por_sbsx_por_sbsx_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

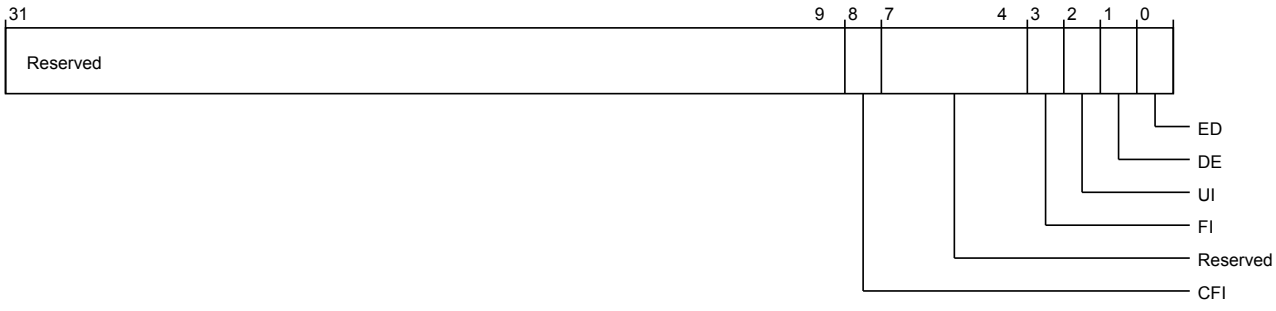


Figure 3-1045 por_sbsx_por_sbsx_errctlr_ns (low)

The following table shows the por_sbsx_errctlr_NS lower register bit assignments.

Table 3-1059 por_sbsx_por_sbsx_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_sbsx_errfr_NS.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_sbsx_errfr_NS.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_sbsx_errfr_NS.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_sbsx_errfr_NS.DE	RW	1'b0
0	ED	Enables error detection as specified in por_sbsx_errfr_NS.ED	RW	1'b0

por_sbsx_errstatus_NS

Functions as the non-secure error status register.

Its characteristics are:

Type W1C
Register width (Bits) 64
Address offset 14'h3110
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

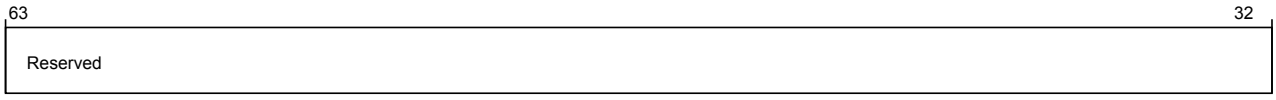


Figure 3-1046 por_sbsx_por_sbsx_errstatus_ns (high)

The following table shows the por_sbsx_errstatus_NS higher register bit assignments.

Table 3-1060 por_sbsx_por_sbsx_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-1047 por_sbsx_por_sbsx_errstatus_ns (low)

The following table shows the por_sbsx_errstatus_NS lower register bit assignments.

Table 3-1061 por_sbsx_por_sbsx_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_sbsx_erraddr_NS contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_sbsx_errmisc_NS valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 3-1061 por_sbsx_por_sbsx_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_sbsx_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3118
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

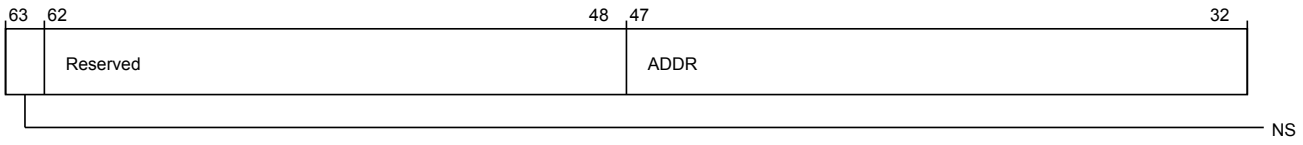


Figure 3-1048 por_sbsx_por_sbsx_erraddr_ns (high)

The following table shows the por_sbsx_erraddr_NS higher register bit assignments.

Table 3-1062 por_sbsx_por_sbsx_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_sbsx_erraddr_NS.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

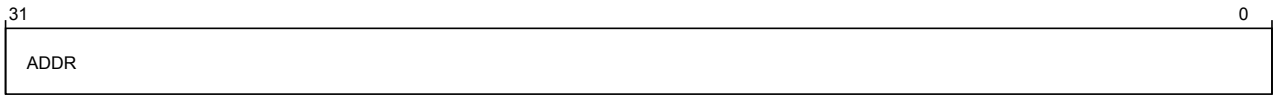


Figure 3-1049 por_sbsx_por_sbsx_erraddr_ns (low)

The following table shows the por_sbsx_erraddr_NS lower register bit assignments.

Table 3-1063 por_sbsx_por_sbsx_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_sbsx_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3120
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

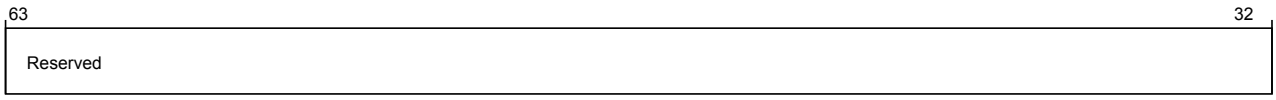


Figure 3-1050 por_sbsx_por_sbsx_errmisc_ns (high)

The following table shows the por_sbsx_errmisc_NS higher register bit assignments.

Table 3-1064 por_sbsx_por_sbsx_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

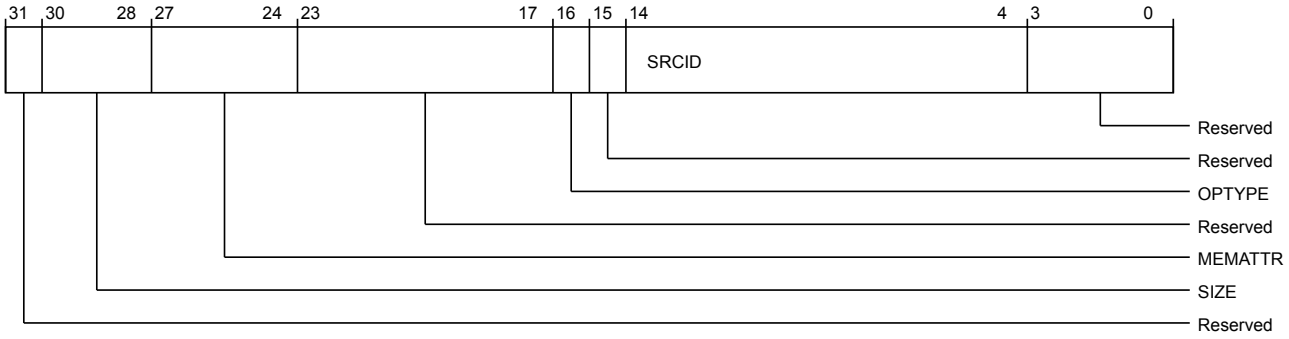


Figure 3-1051 por_sbsx_por_sbsx_errmisc_ns (low)

The following table shows the por_sbsx_errmisc_NS lower register bit assignments.

Table 3-1065 por_sbsx_por_sbsx_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	SIZE	Error transaction size	RW	3'b0
27:24	MEMATTR	Error memory attributes	RW	4'b0
23:17	Reserved	Reserved	RO	-
16	OPTYPE	Error opcode type 1'b1: WR_NO_SNP_PTL (partial) 1'b0: WR_NO_SNP_FULL	RW	1'b0
15	Reserved	Reserved	RO	-
14:4	SRCID	Error source ID	RW	11'b0
3:0	Reserved	Reserved	RO	-

por_sbsx_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

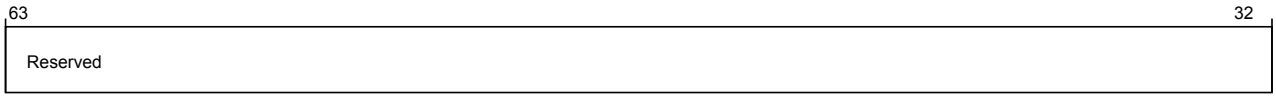


Figure 3-1052 por_sbsx_por_sbsx_pmu_event_sel (high)

The following table shows the por_sbsx_pmu_event_sel higher register bit assignments.

Table 3-1066 por_sbsx_por_sbsx_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

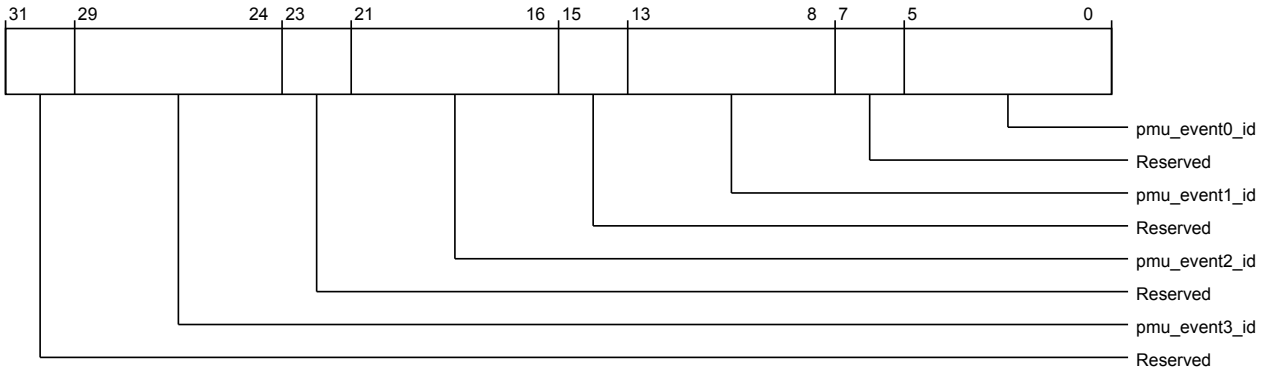


Figure 3-1053 por_sbsx_por_sbsx_pmu_event_sel (low)

The following table shows the por_sbsx_pmu_event_sel lower register bit assignments.

Table 3-1067 por_sbsx_por_sbsx_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	SBSX PMU Event 3 select; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	SBSX PMU Event 2 select; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	SBSX PMU Event 1 select; see pmu_event0_id for encodings	RW	6'b0

Table 3-1067 por_sbsx_por_sbsx_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	SBSX PMU Event 0 select 6'h00: No event 6'h01: Read request 6'h02: Write request 6'h03: CMO request 6'h04: RETRYACK TXRSP flit sent 6'h05: TXDAT flit seen 6'h06: TXRSP flit seen 6'h11: Read request tracker occupancy count overflow 6'h12: Write request tracker occupancy count overflow 6'h13: CMO request tracker occupancy count overflow 6'h14: WDB occupancy count overflow 6'h15: Read AXI pending tracker occupancy count overflow 6'h16: CMO AXI pending tracker occupancy count overflow 6'h21: ARVALID set without ARREADY 6'h22: AWVALID set without AWREADY 6'h23: WVALID set without WREADY 6'h24: TXDAT stall (TXDAT valid but no link credit available) 6'h25: TXRSP stall (TXRSP valid but no link credit available) NOTE: All other encodings are reserved.	RW	6'b0

3.3.11 CXHA configuration registers

This section lists the CXHA configuration registers.

por_cxg_ha_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

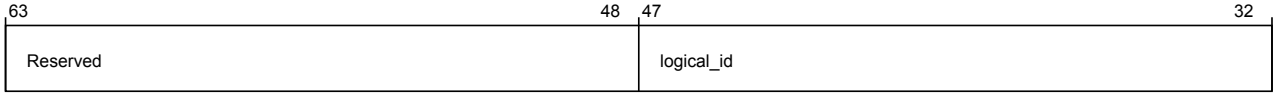


Figure 3-1054 por_cxg_ha_por_cxg_ha_node_info (high)

The following table shows the por_cxg_ha_node_info higher register bit assignments.

Table 3-1068 por_cxg_ha_por_cxg_ha_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

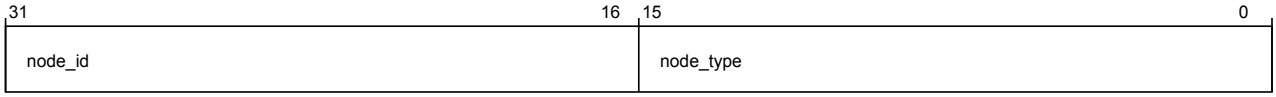


Figure 3-1055 por_cxg_ha_por_cxg_ha_node_info (low)

The following table shows the por_cxg_ha_node_info lower register bit assignments.

Table 3-1069 por_cxg_ha_por_cxg_ha_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0101

por_cxg_ha_id

Contains the CCIX-assigned HAID.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h8
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

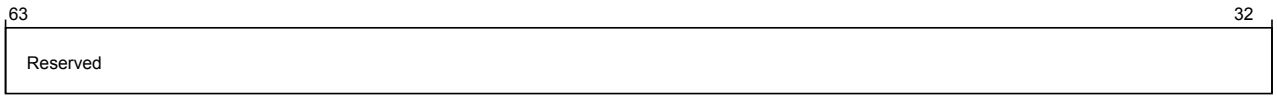


Figure 3-1056 por_cxg_ha_por_cxg_ha_id (high)

The following table shows the por_cxg_ha_id higher register bit assignments.

Table 3-1070 por_cxg_ha_por_cxg_ha_id (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

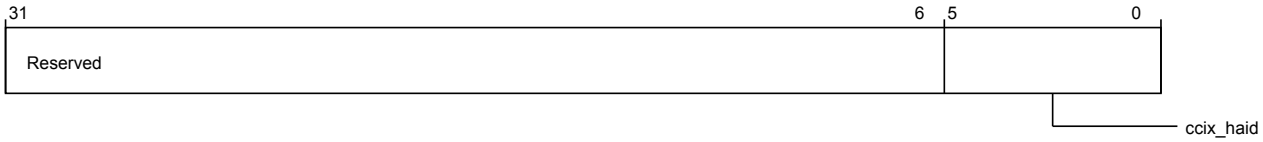


Figure 3-1057 por_cxg_ha_por_cxg_ha_id (low)

The following table shows the por_cxg_ha_id lower register bit assignments.

Table 3-1071 por_cxg_ha_por_cxg_ha_id (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	ccix_haid	CCIX HAID	RW	6'h0

por_cxg_ha_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64

Address offset 14'h80

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

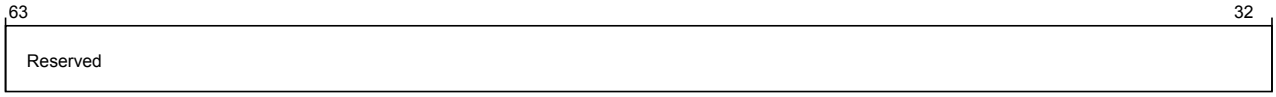


Figure 3-1058 por_cxg_ha_por_cxg_ha_child_info (high)

The following table shows the por_cxg_ha_child_info higher register bit assignments.

Table 3-1072 por_cxg_ha_por_cxg_ha_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

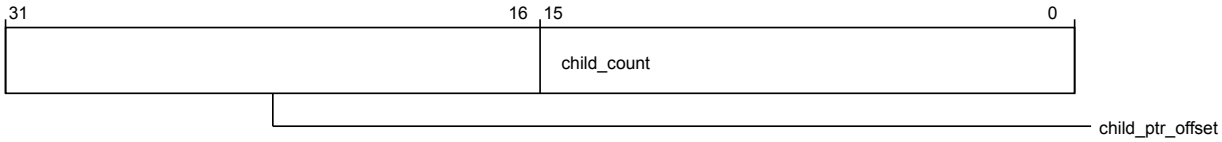


Figure 3-1059 por_cxg_ha_por_cxg_ha_child_info (low)

The following table shows the por_cxg_ha_child_info lower register bit assignments.

Table 3-1073 por_cxg_ha_por_cxg_ha_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_cxg_ha_aux_ctl

Functions as the auxiliary control register for CXHA.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset Configuration dependent

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

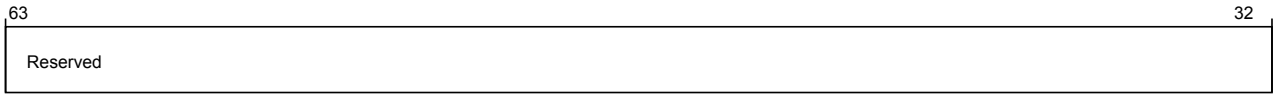


Figure 3-1060 por_cxg_ha_por_cxg_ha_aux_ctl (high)

The following table shows the por_cxg_ha_aux_ctl higher register bit assignments.

Table 3-1074 por_cxg_ha_por_cxg_ha_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

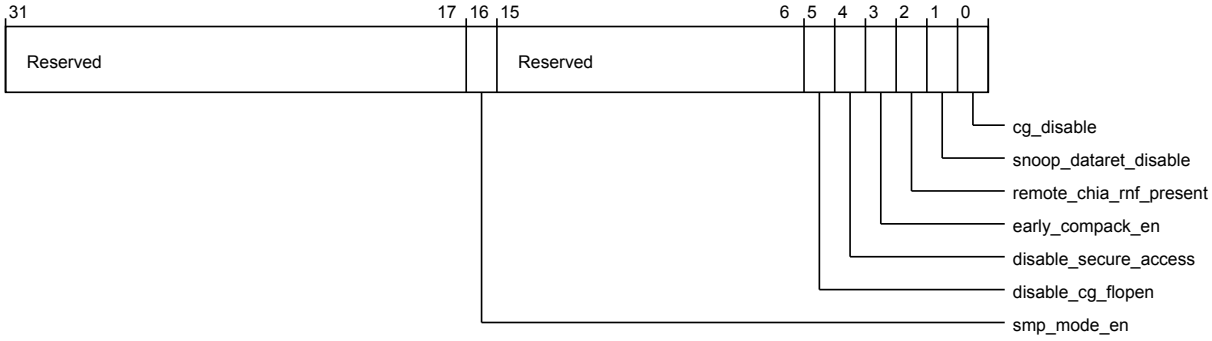


Figure 3-1061 por_cxg_ha_por_cxg_ha_aux_ctl (low)

The following table shows the por_cxg_ha_aux_ctl lower register bit assignments.

Table 3-1075 por_cxg_ha_por_cxg_ha_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode.	RW	1'b0
15:6	Reserved	Reserved	RO	-
5	disable_cg_flopen	Disables enhanced flop enable control for dynamic power savings	RW	1'b0
4	disable_secure_access	Converts all accesses to non-secure	RW	1'b0
3	early_compack_en	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1
2	remote_chia_rnf_present	Indicates existence of CHIA RN-F in system; HA uses this indication to send SnpToS or SnpToSC 1'b0: HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToSC 1'b1: HA converts SnpShared, SnpClean, and SnpNotSharedDirty to SnpToS	RW	1'b0

Table 3-1075 por_cxg_ha_por_cxg_ha_aux_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
1	snoop_dataret_disable	Disables setting data return for CCIX snoop requests for all CHI snoop opcodes	RW	1'b0
0	cg_disable	Disables clock gating when set	RW	1'b0

por_cxg_ha_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

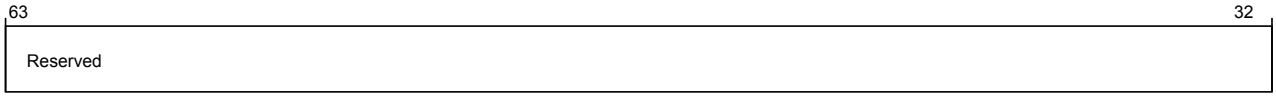


Figure 3-1062 por_cxg_ha_por_cxg_ha_secure_register_groups_override (high)

The following table shows the por_cxg_ha_secure_register_groups_override higher register bit assignments.

Table 3-1076 por_cxg_ha_por_cxg_ha_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

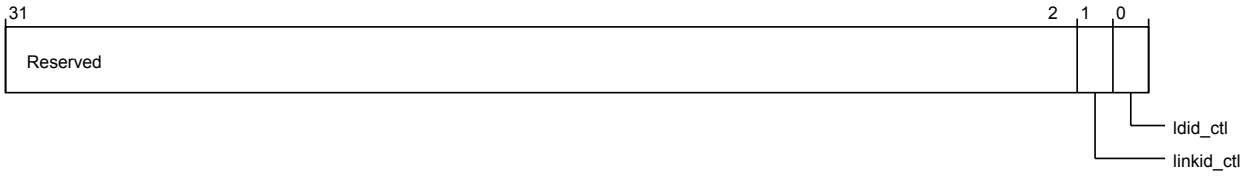


Figure 3-1063 por_cxg_ha_por_cxg_ha_secure_register_groups_override (low)

The following table shows the por_cxg_ha_secure_register_groups_override lower register bit assignments.

Table 3-1077 por_cxg_ha_por_cxg_ha_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:2	Reserved	Reserved	RO	-
1	linkid_ctl	Allows non-secure access to secure HA Link ID registers	RW	1'b0
0	ldid_ctl	Allows non-secure access to secure HA LDID registers	RW	1'b0

por_cxg_ha_unit_info

Provides component identification information for CXHA.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h900
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

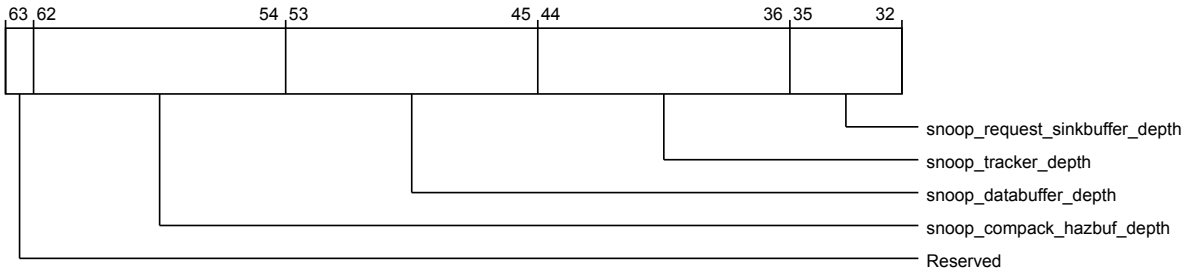


Figure 3-1064 por_cxg_ha_por_cxg_ha_unit_info (high)

The following table shows the por_cxg_ha_unit_info higher register bit assignments.

Table 3-1078 por_cxg_ha_por_cxg_ha_unit_info (high)

Bits	Field name	Description	Type	Reset
63	Reserved	Reserved	RO	-
62:54	snoop_compack_hazbuf_depth	Depth of CompAck snoop hazard buffer	RO	Configuration dependent
53:45	snoop_databuffer_depth	Depth of snoop data buffer	RO	Configuration dependent
44:36	snoop_tracker_depth	Depth of snoop tracker; number of outstanding SNP requests on CCIX	RO	Configuration dependent
35:32	snoop_request_sinkbuffer_depth	Depth of snoop request sink buffer; number of CHI SNP requests that can be sunk by CXHA	RO	Configuration dependent

The following image shows the lower register bit assignments.

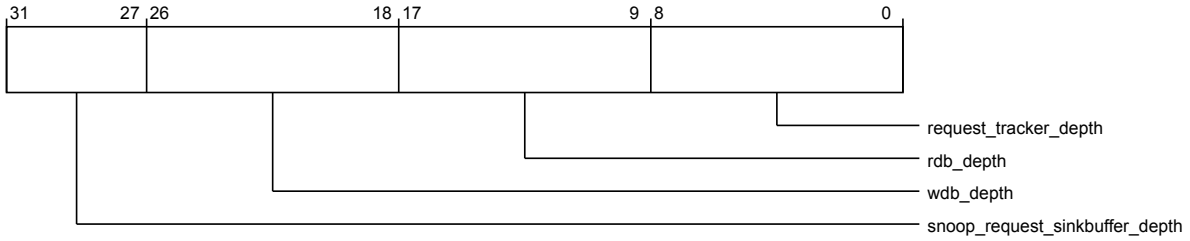


Figure 3-1065 por_cxg_ha_por_cxg_ha_unit_info (low)

The following table shows the por_cxg_ha_unit_info lower register bit assignments.

Table 3-1079 por_cxg_ha_por_cxg_ha_unit_info (low)

Bits	Field name	Description	Type	Reset
31:27	snoop_request_sinkbuffer_depth	Depth of snoop request sink buffer; number of CHI SNP requests that can be sunk by CXHA	RO	Configuration dependent
26:18	wdb_depth	Depth of write data buffer	RO	Configuration dependent
17:9	rdb_depth	Depth of read data buffer	RO	Configuration dependent
8:0	request_tracker_depth	Depth of request tracker	RO	Configuration dependent

por_cxg_ha_rnf_raid_to_ldid_reg0

Specifies the mapping of RAID to RN-F LDID for RAIDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

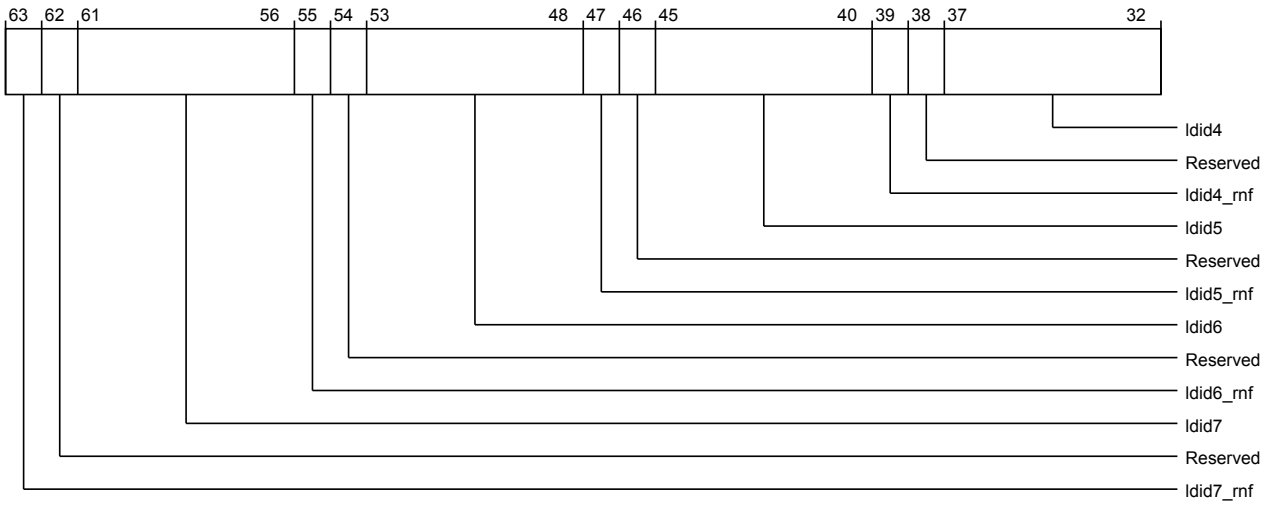


Figure 3-1066 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg0 higher register bit assignments.

Table 3-1080 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (high)

Bits	Field name	Description	Type	Reset
63	ldid7_rnf	Specifies if RAID 7 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid7	Specifies the LDID for RAID 7	RW	6'h0
55	ldid6_rnf	Specifies if RAID 6 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid6	Specifies the LDID for RAID 6	RW	6'h0
47	ldid5_rnf	Specifies if RAID 5 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid5	Specifies the LDID for RAID 5	RW	6'h0
39	ldid4_rnf	Specifies if RAID 4 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid4	Specifies the LDID for RAID 4	RW	6'h0

The following image shows the lower register bit assignments.

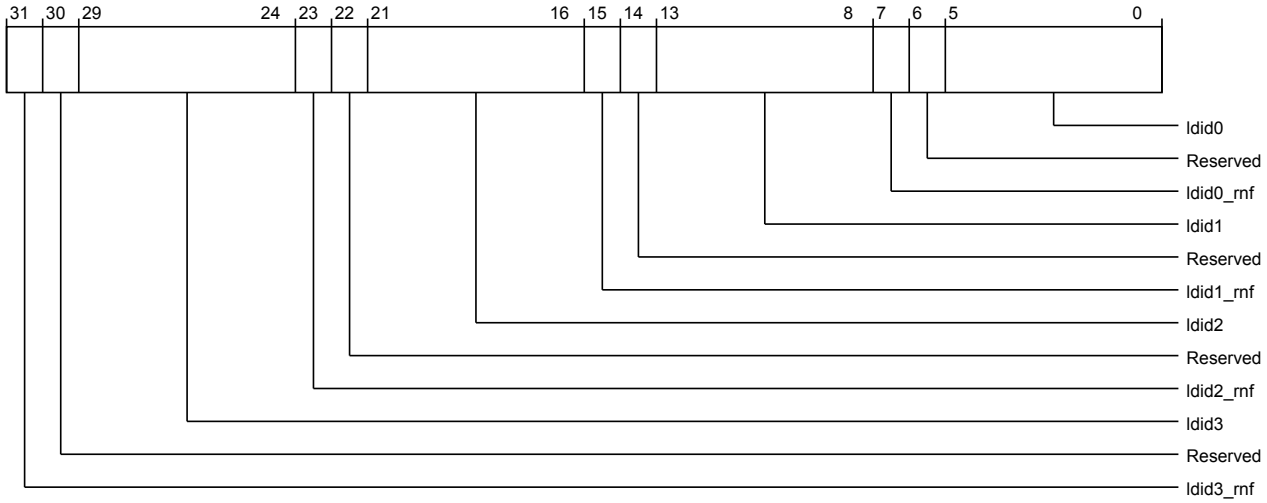


Figure 3-1067 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg0 lower register bit assignments.

Table 3-1081 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg0 (low)

Bits	Field name	Description	Type	Reset
31	ldid3_rnf	Specifies if RAID 3 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid3	Specifies the LDID for RAID 3	RW	6'h0
23	ldid2_rnf	Specifies if RAID 2 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid2	Specifies the LDID for RAID 2	RW	6'h0
15	ldid1_rnf	Specifies if RAID 1 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid1	Specifies the LDID for RAID 1	RW	6'h0
7	ldid0_rnf	Specifies if RAID 0 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid0	Specifies the LDID for RAID 0	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg1

Specifies the mapping of RAID to RN-F LDID for RAIDs 8 to 15.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

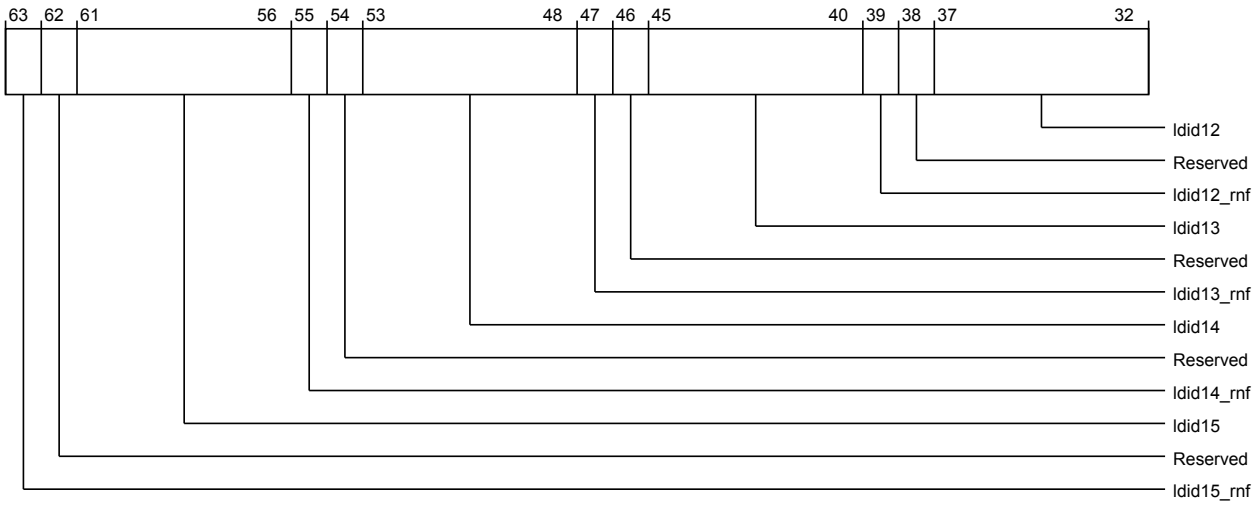


Figure 3-1068 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg1 higher register bit assignments.

Table 3-1082 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (high)

Bits	Field name	Description	Type	Reset
63	ldid15_rnf	Specifies if RAID 15 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid15	Specifies the LDID for RAID 15	RW	6'h0
55	ldid14_rnf	Specifies if RAID 14 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid14	Specifies the LDID for RAID 14	RW	6'h0
47	ldid13_rnf	Specifies if RAID 13 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid13	Specifies the LDID for RAID 13	RW	6'h0
39	ldid12_rnf	Specifies if RAID 12 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid12	Specifies the LDID for RAID 12	RW	6'h0

The following image shows the lower register bit assignments.

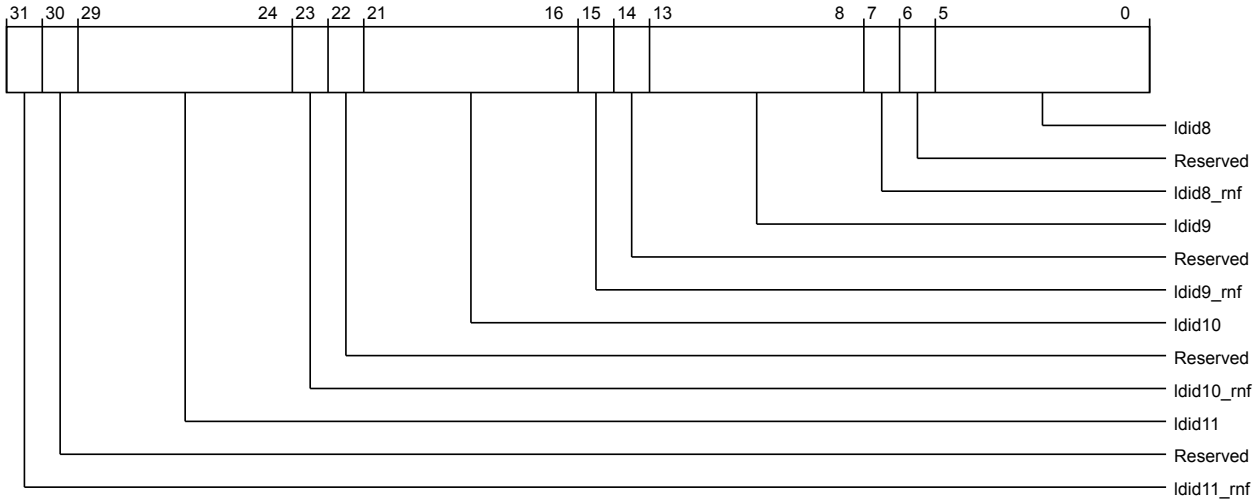


Figure 3-1069 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg1 lower register bit assignments.

Table 3-1083 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg1 (low)

Bits	Field name	Description	Type	Reset
31	ldid11_rnf	Specifies if RAID 11 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid11	Specifies the LDID for RAID 11	RW	6'h0
23	ldid10_rnf	Specifies if RAID 10 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid10	Specifies the LDID for RAID 10	RW	6'h0
15	ldid9_rnf	Specifies if RAID 9 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid9	Specifies the LDID for RAID 9	RW	6'h0
7	ldid8_rnf	Specifies if RAID 8 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid8	Specifies the LDID for RAID 8	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg2

Specifies the mapping of RAID to RN-F LDID for RAIDs 16 to 23.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

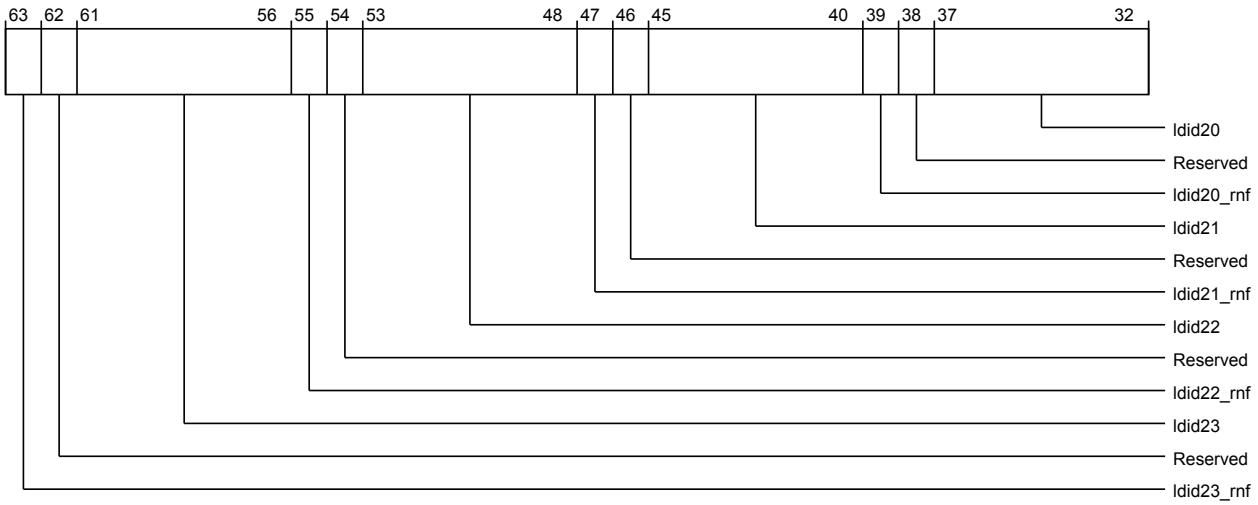


Figure 3-1070 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg2 higher register bit assignments.

Table 3-1084 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (high)

Bits	Field name	Description	Type	Reset
63	ldid23_rnf	Specifies if RAID 23 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid23	Specifies the LDID for RAID 23	RW	6'h0
55	ldid22_rnf	Specifies if RAID 22 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid22	Specifies the LDID for RAID 22	RW	6'h0
47	ldid21_rnf	Specifies if RAID 21 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid21	Specifies the LDID for RAID 21	RW	6'h0
39	ldid20_rnf	Specifies if RAID 20 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid20	Specifies the LDID for RAID 20	RW	6'h0

The following image shows the lower register bit assignments.

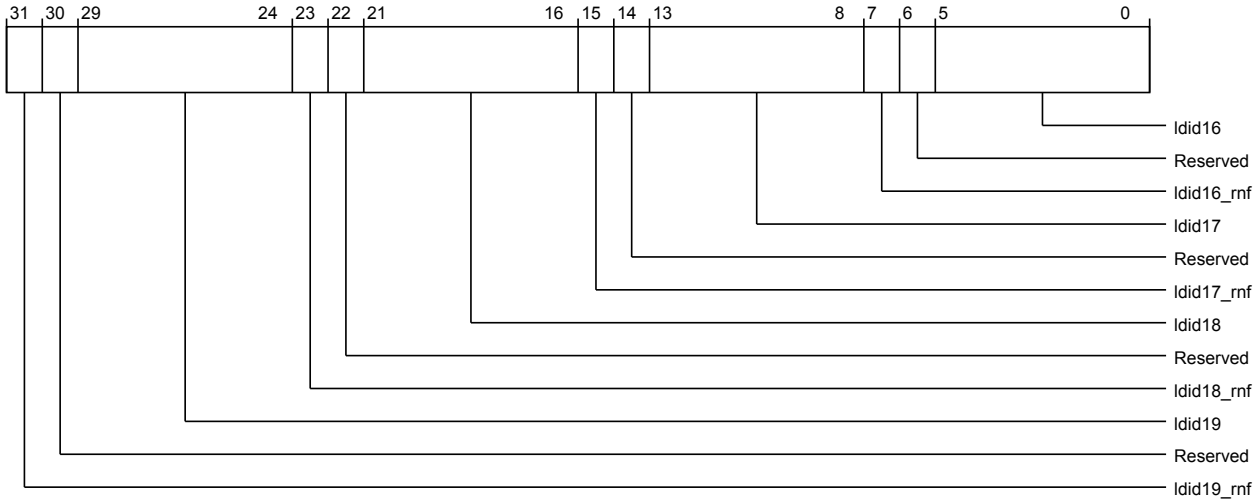


Figure 3-1071 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg2 lower register bit assignments.

Table 3-1085 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg2 (low)

Bits	Field name	Description	Type	Reset
31	ldid19_rnf	Specifies if RAID 19 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid19	Specifies the LDID for RAID 19	RW	6'h0
23	ldid18_rnf	Specifies if RAID 18 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid18	Specifies the LDID for RAID 18	RW	6'h0
15	ldid17_rnf	Specifies if RAID 17 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid17	Specifies the LDID for RAID 17	RW	6'h0
7	ldid16_rnf	Specifies if RAID 16 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid16	Specifies the LDID for RAID 16	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg3

Specifies the mapping of RAID to RN-F LDID for RAIDs 24 to 31.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

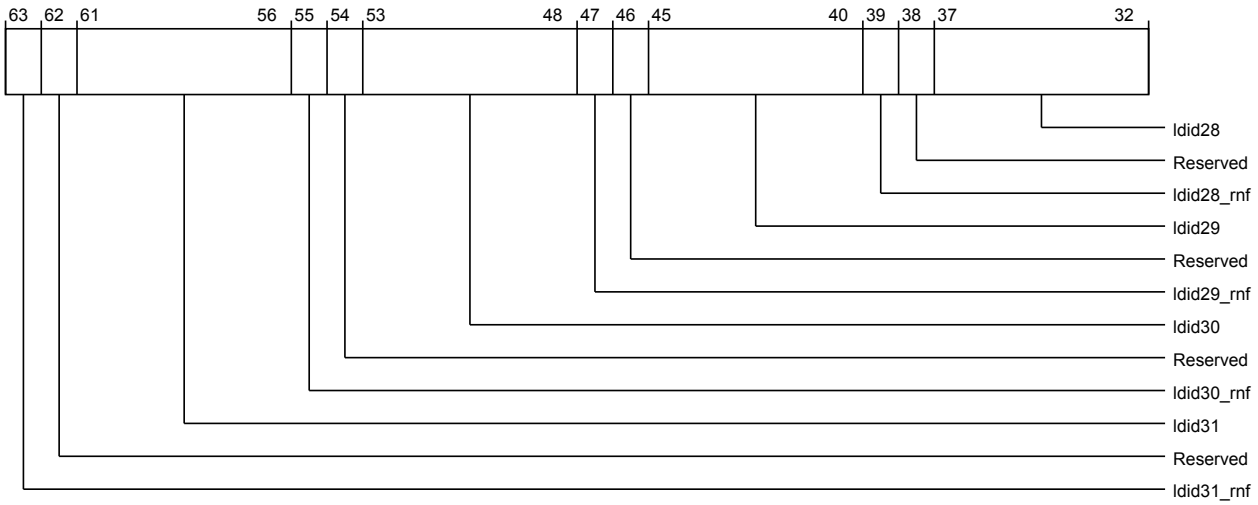


Figure 3-1072 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg3 higher register bit assignments.

Table 3-1086 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (high)

Bits	Field name	Description	Type	Reset
63	ldid31_rnf	Specifies if RAID 31 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid31	Specifies the LDID for RAID 31	RW	6'h0
55	ldid30_rnf	Specifies if RAID 30 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid30	Specifies the LDID for RAID 30	RW	6'h0
47	ldid29_rnf	Specifies if RAID 29 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid29	Specifies the LDID for RAID 29	RW	6'h0
39	ldid28_rnf	Specifies if RAID 28 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid28	Specifies the LDID for RAID 28	RW	6'h0

The following image shows the lower register bit assignments.

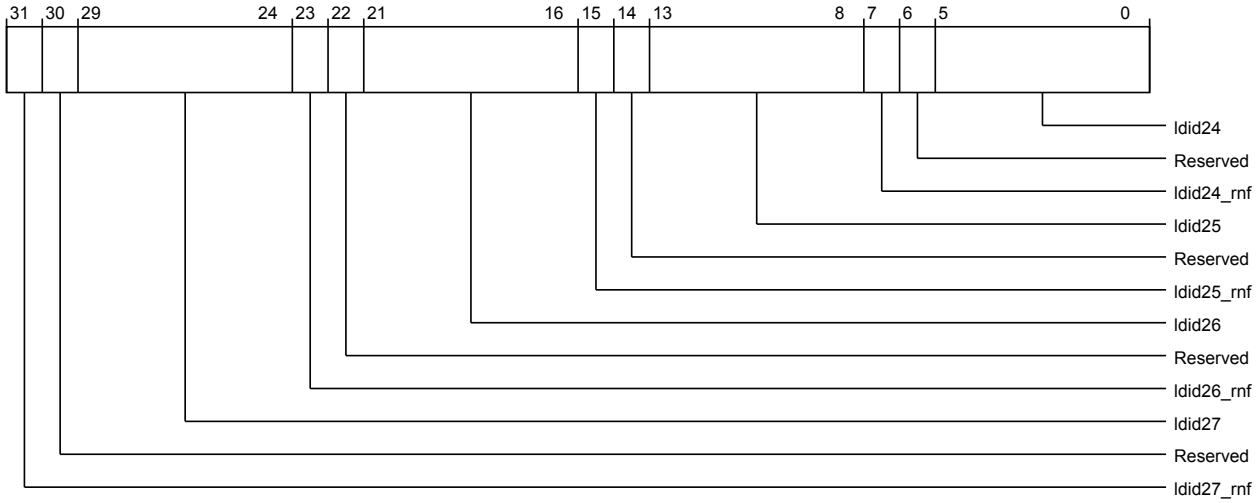


Figure 3-1073 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg3 lower register bit assignments.

Table 3-1087 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg3 (low)

Bits	Field name	Description	Type	Reset
31	ldid27_rnf	Specifies if RAID 27 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid27	Specifies the LDID for RAID 27	RW	6'h0
23	ldid26_rnf	Specifies if RAID 26 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid26	Specifies the LDID for RAID 26	RW	6'h0
15	ldid25_rnf	Specifies if RAID 25 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid25	Specifies the LDID for RAID 25	RW	6'h0
7	ldid24_rnf	Specifies if RAID 24 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid24	Specifies the LDID for RAID 24	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg4

Specifies the mapping of RAID to RN-F LDID for RAIDs 32 to 39.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

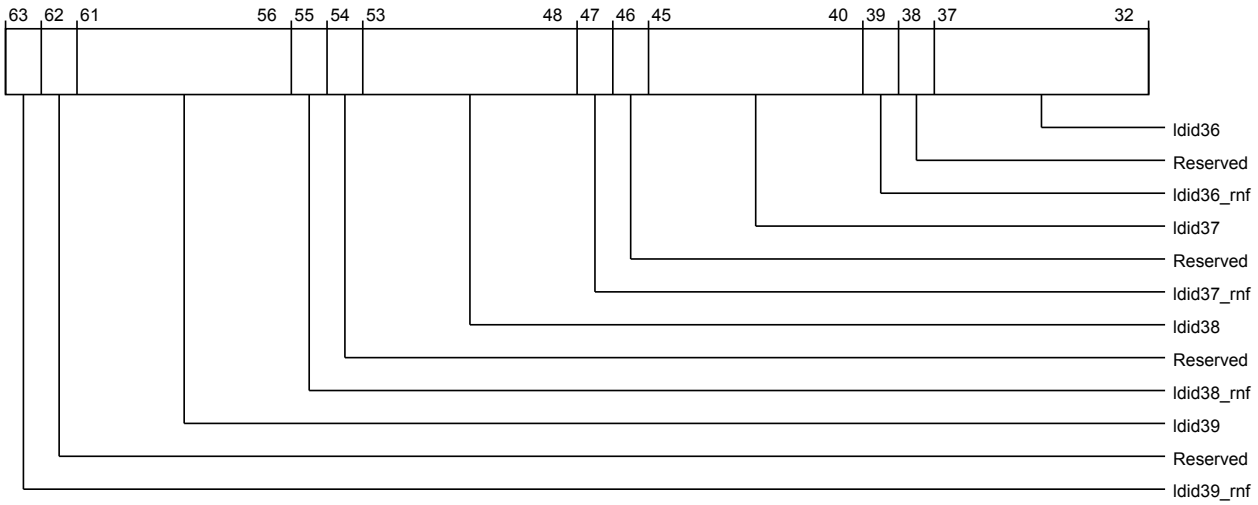


Figure 3-1074 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg4 higher register bit assignments.

Table 3-1088 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (high)

Bits	Field name	Description	Type	Reset
63	ldid39_rnf	Specifies if RAID 39 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid39	Specifies the LDID for RAID 39	RW	6'h0
55	ldid38_rnf	Specifies if RAID 38 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid38	Specifies the LDID for RAID 38	RW	6'h0
47	ldid37_rnf	Specifies if RAID 37 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid37	Specifies the LDID for RAID 37	RW	6'h0
39	ldid36_rnf	Specifies if RAID 36 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid36	Specifies the LDID for RAID 36	RW	6'h0

The following image shows the lower register bit assignments.

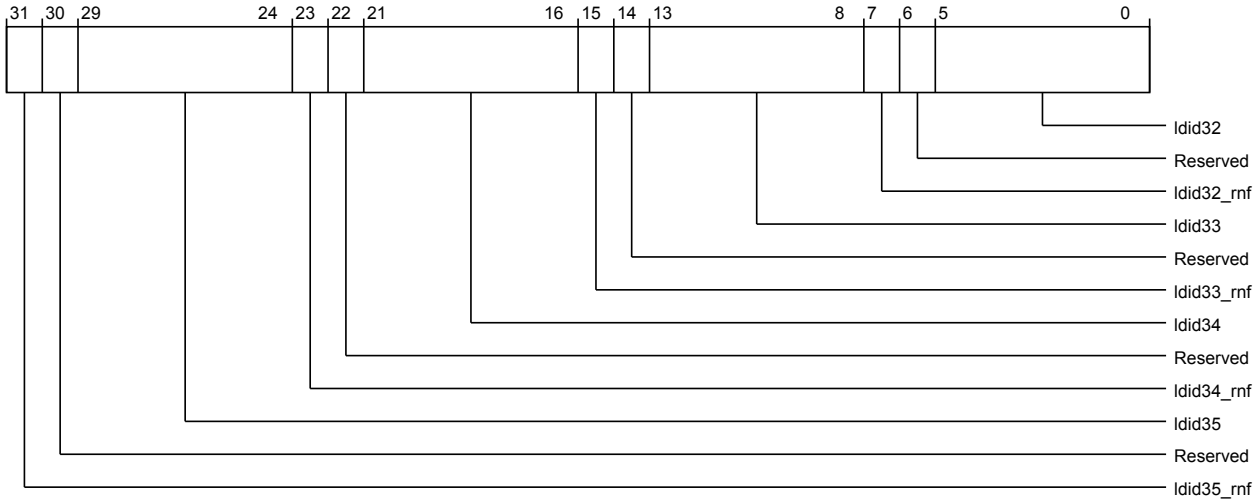


Figure 3-1075 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg4 lower register bit assignments.

Table 3-1089 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg4 (low)

Bits	Field name	Description	Type	Reset
31	ldid35_rnf	Specifies if RAID 35 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid35	Specifies the LDID for RAID 35	RW	6'h0
23	ldid34_rnf	Specifies if RAID 34 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid34	Specifies the LDID for RAID 34	RW	6'h0
15	ldid33_rnf	Specifies if RAID 33 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid33	Specifies the LDID for RAID 33	RW	6'h0
7	ldid32_rnf	Specifies if RAID 32 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid32	Specifies the LDID for RAID 32	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg5

Specifies the mapping of RAID to RN-F LDID for RAIDs 40 to 47.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

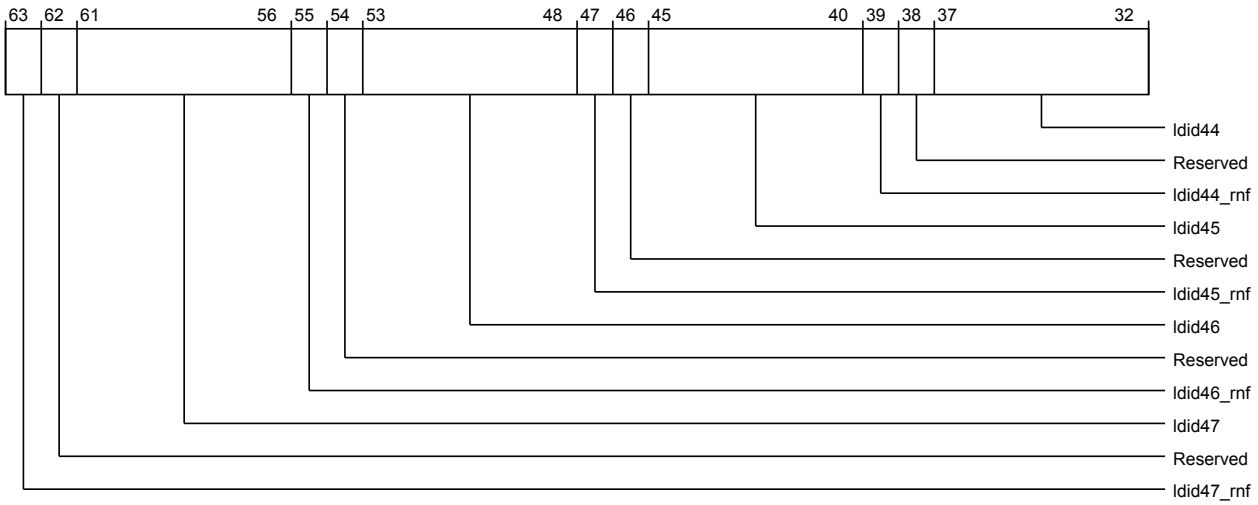


Figure 3-1076 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg5 higher register bit assignments.

Table 3-1090 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (high)

Bits	Field name	Description	Type	Reset
63	ldid47_rnf	Specifies if RAID 47 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid47	Specifies the LDID for RAID 47	RW	6'h0
55	ldid46_rnf	Specifies if RAID 46 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid46	Specifies the LDID for RAID 46	RW	6'h0
47	ldid45_rnf	Specifies if RAID 45 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid45	Specifies the LDID for RAID 45	RW	6'h0
39	ldid44_rnf	Specifies if RAID 44 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid44	Specifies the LDID for RAID 44	RW	6'h0

The following image shows the lower register bit assignments.

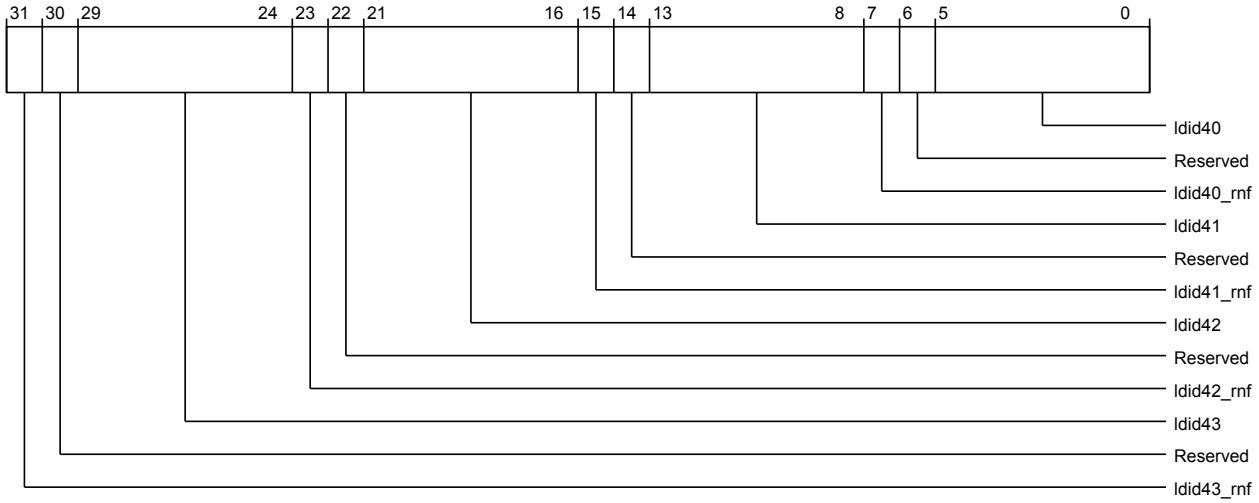


Figure 3-1077 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg5 lower register bit assignments.

Table 3-1091 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg5 (low)

Bits	Field name	Description	Type	Reset
31	ldid43_rnf	Specifies if RAID 43 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid43	Specifies the LDID for RAID 43	RW	6'h0
23	ldid42_rnf	Specifies if RAID 42 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid42	Specifies the LDID for RAID 42	RW	6'h0
15	ldid41_rnf	Specifies if RAID 41 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid41	Specifies the LDID for RAID 41	RW	6'h0
7	ldid40_rnf	Specifies if RAID 40 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid40	Specifies the LDID for RAID 40	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg6

Specifies the mapping of RAID to RN-F LDID for RAIDs 48 to 55.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

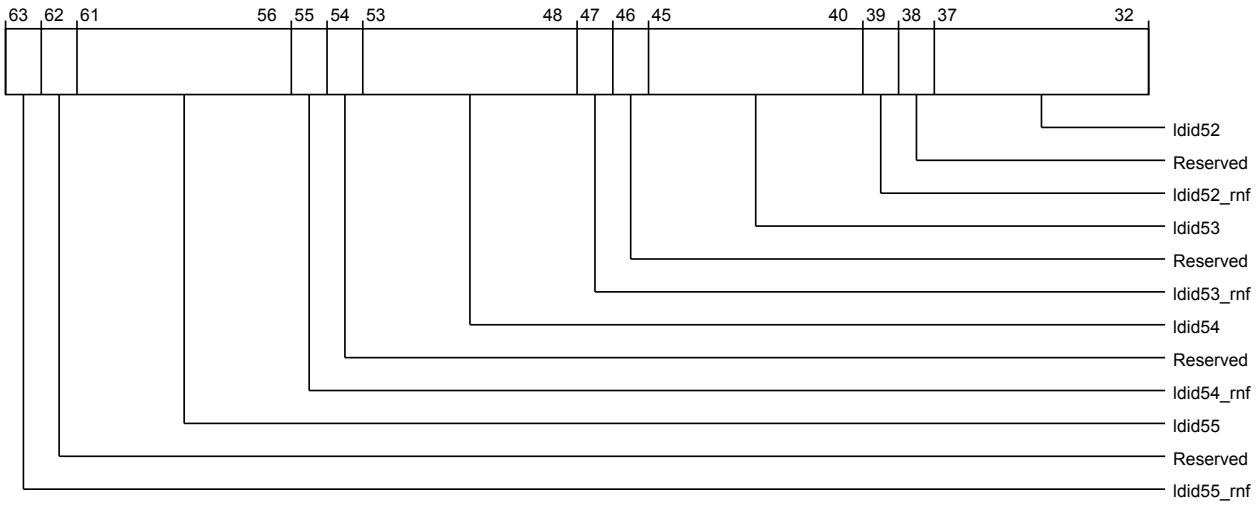


Figure 3-1078 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg6 higher register bit assignments.

Table 3-1092 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (high)

Bits	Field name	Description	Type	Reset
63	ldid55_rnf	Specifies if RAID 55 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid55	Specifies the LDID for RAID 55	RW	6'h0
55	ldid54_rnf	Specifies if RAID 54 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid54	Specifies the LDID for RAID 54	RW	6'h0
47	ldid53_rnf	Specifies if RAID 53 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid53	Specifies the LDID for RAID 53	RW	6'h0
39	ldid52_rnf	Specifies if RAID 52 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid52	Specifies the LDID for RAID 52	RW	6'h0

The following image shows the lower register bit assignments.

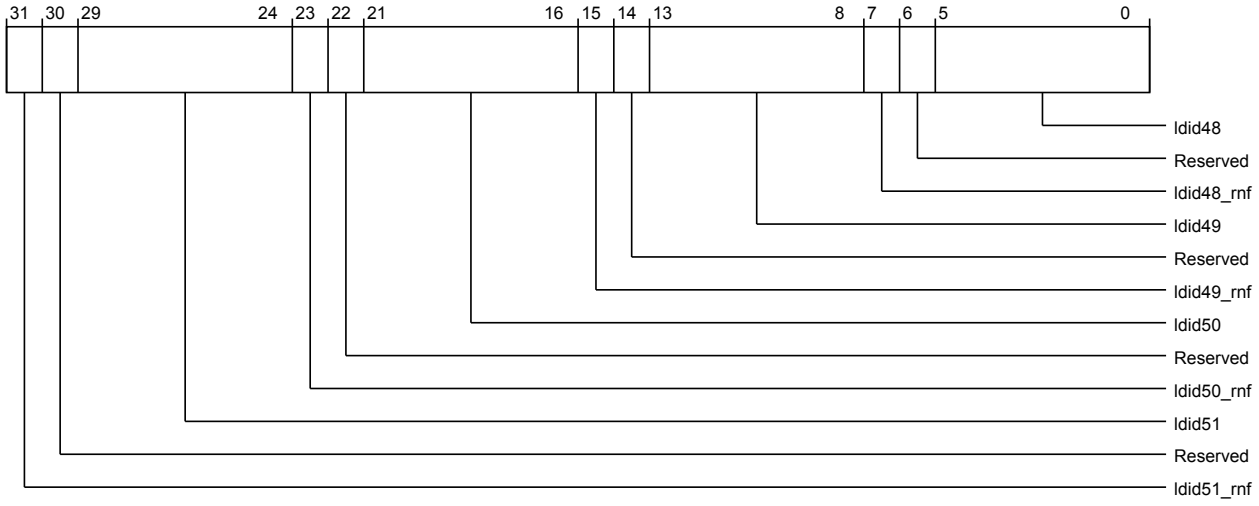


Figure 3-1079 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg6 lower register bit assignments.

Table 3-1093 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg6 (low)

Bits	Field name	Description	Type	Reset
31	ldid51_rnf	Specifies if RAID 51 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid51	Specifies the LDID for RAID 51	RW	6'h0
23	ldid50_rnf	Specifies if RAID 50 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid50	Specifies the LDID for RAID 50	RW	6'h0
15	ldid49_rnf	Specifies if RAID 49 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid49	Specifies the LDID for RAID 49	RW	6'h0
7	ldid48_rnf	Specifies if RAID 48 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid48	Specifies the LDID for RAID 48	RW	6'h0

por_cxg_ha_rnf_raid_to_ldid_reg7

Specifies the mapping of RAID to RN-F LDID for RAIDs 56 to 63.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

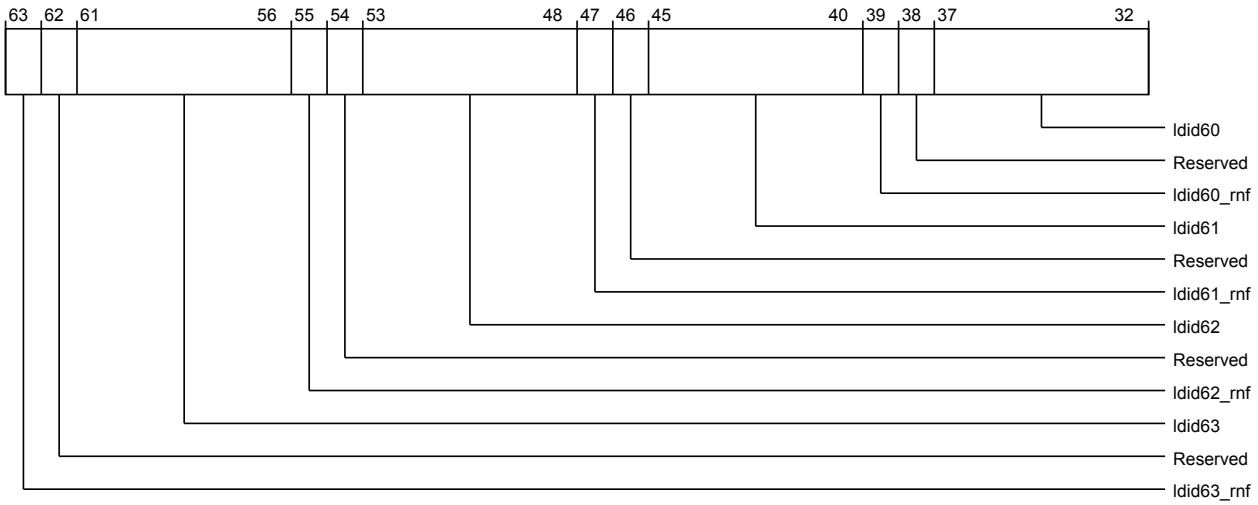


Figure 3-1080 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg7 higher register bit assignments.

Table 3-1094 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (high)

Bits	Field name	Description	Type	Reset
63	ldid63_rnf	Specifies if RAID 63 is RN-F	RW	1'b0
62	Reserved	Reserved	RO	-
61:56	ldid63	Specifies the LDID for RAID 63	RW	6'h0
55	ldid62_rnf	Specifies if RAID 62 is RN-F	RW	1'b0
54	Reserved	Reserved	RO	-
53:48	ldid62	Specifies the LDID for RAID 62	RW	6'h0
47	ldid61_rnf	Specifies if RAID 61 is RN-F	RW	1'b0
46	Reserved	Reserved	RO	-
45:40	ldid61	Specifies the LDID for RAID 61	RW	6'h0
39	ldid60_rnf	Specifies if RAID 60 is RN-F	RW	1'b0
38	Reserved	Reserved	RO	-
37:32	ldid60	Specifies the LDID for RAID 60	RW	6'h0

The following image shows the lower register bit assignments.

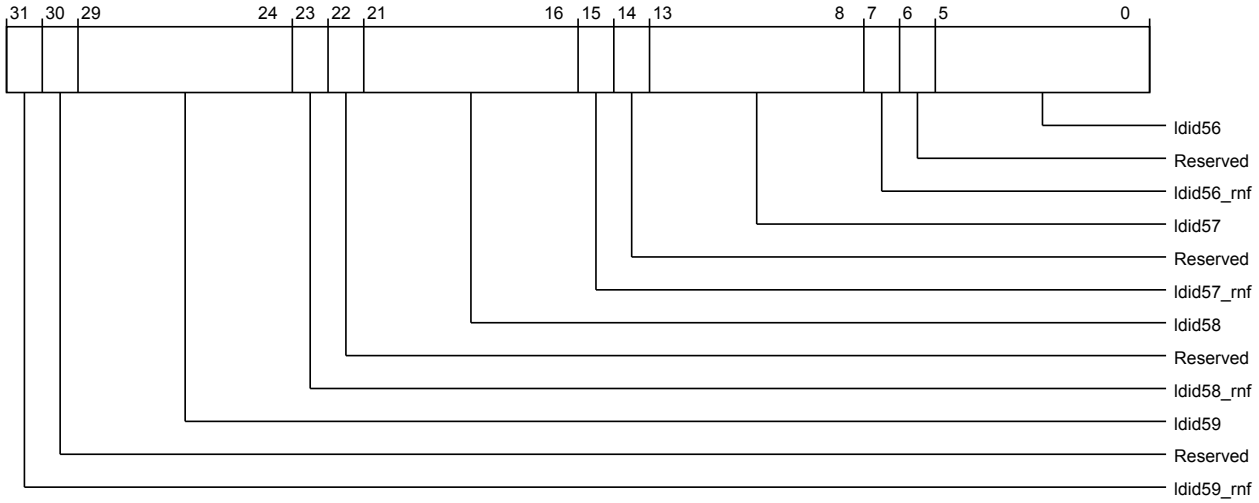


Figure 3-1081 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_reg7 lower register bit assignments.

Table 3-1095 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_reg7 (low)

Bits	Field name	Description	Type	Reset
31	ldid59_rnf	Specifies if RAID 59 is RN-F	RW	1'b0
30	Reserved	Reserved	RO	-
29:24	ldid59	Specifies the LDID for RAID 59	RW	6'h0
23	ldid58_rnf	Specifies if RAID 58 is RN-F	RW	1'b0
22	Reserved	Reserved	RO	-
21:16	ldid58	Specifies the LDID for RAID 58	RW	6'h0
15	ldid57_rnf	Specifies if RAID 57 is RN-F	RW	1'b0
14	Reserved	Reserved	RO	-
13:8	ldid57	Specifies the LDID for RAID 57	RW	6'h0
7	ldid56_rnf	Specifies if RAID 56 is RN-F	RW	1'b0
6	Reserved	Reserved	RO	-
5:0	ldid56	Specifies the LDID for RAID 56	RW	6'h0

por_cxg_ha_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

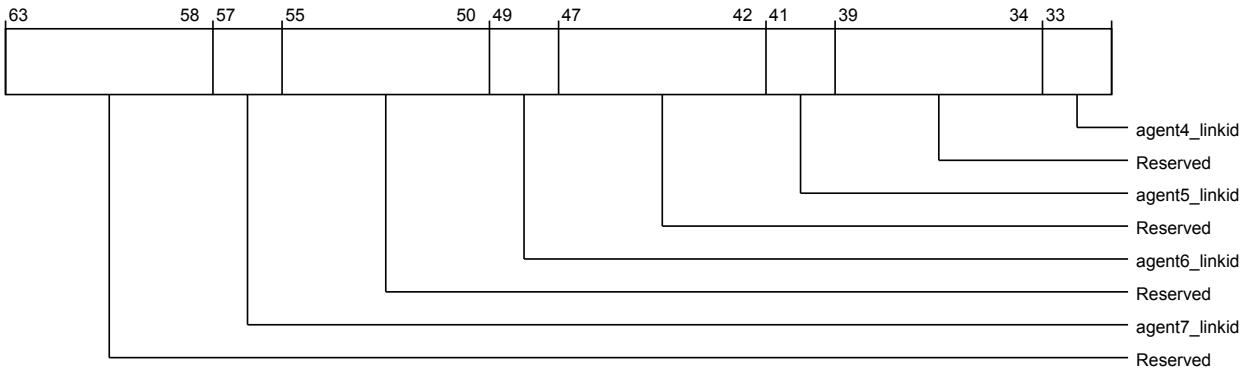


Figure 3-1082 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg0 higher register bit assignments.

Table 3-1096 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies Link ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies Link ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies Link ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies Link ID 4	RW	2'h0

The following image shows the lower register bit assignments.

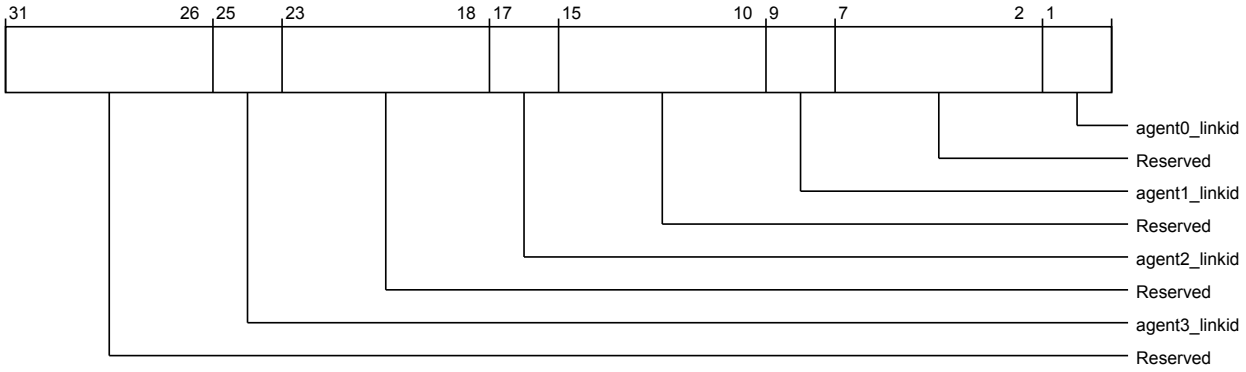


Figure 3-1083 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg0 lower register bit assignments.

Table 3-1097 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies Link ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies Link ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies Link ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies Link ID 0	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

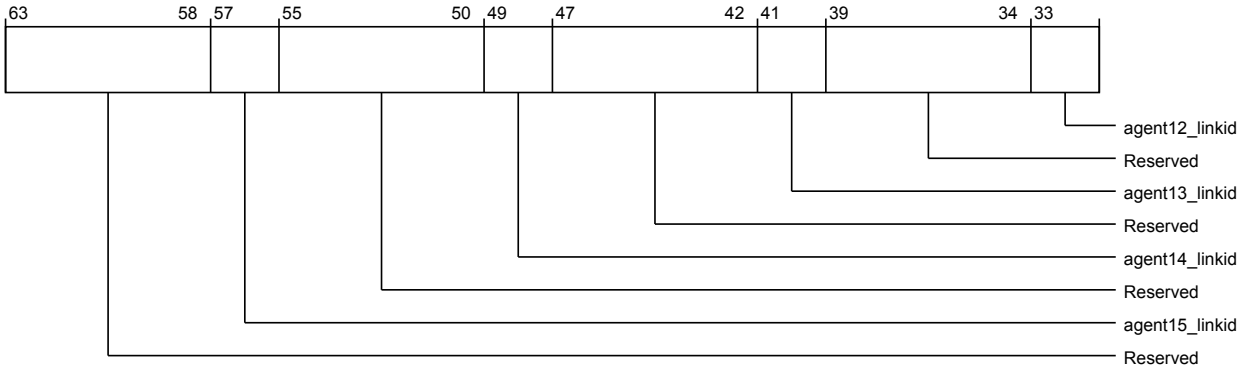


Figure 3-1084 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg1 higher register bit assignments.

Table 3-1098 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies Link ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies Link ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies Link ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies Link ID 12	RW	2'h0

The following image shows the lower register bit assignments.

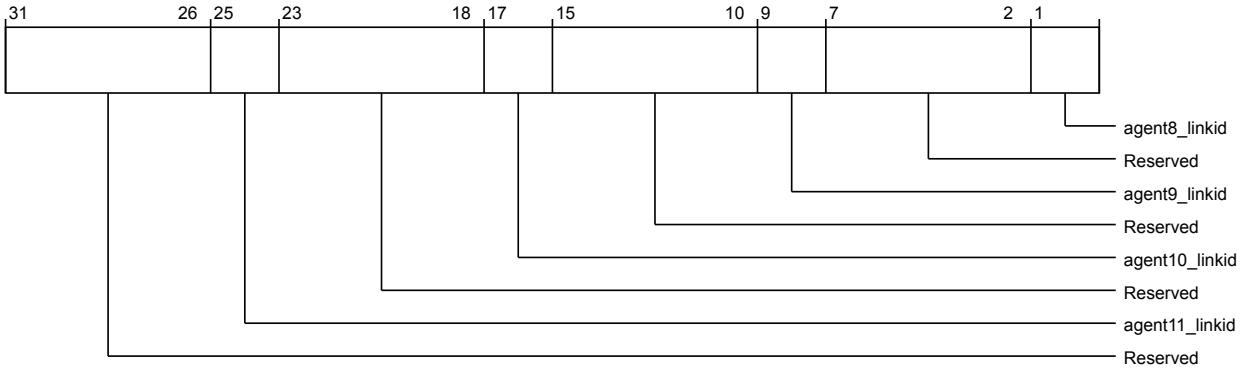


Figure 3-1085 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg1 lower register bit assignments.

Table 3-1099 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies Link ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies Link ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies Link ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies Link ID 8	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg2

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

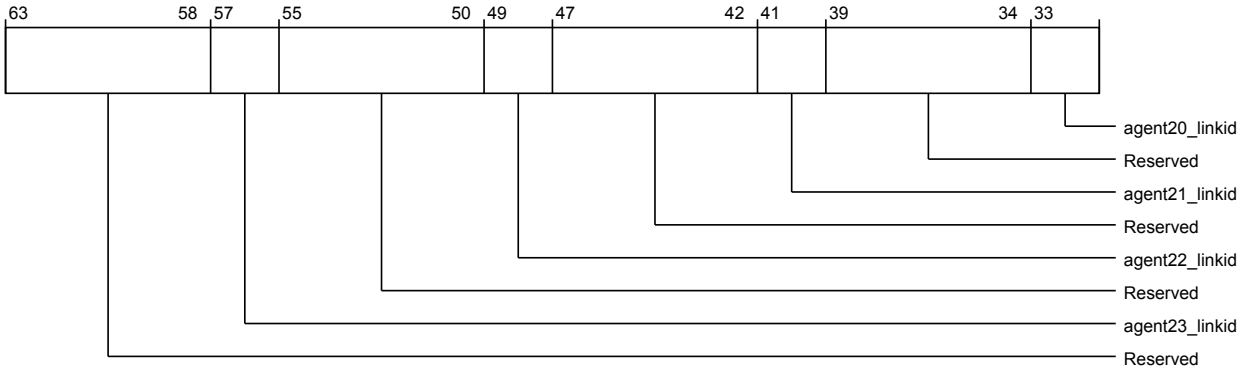


Figure 3-1086 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg2 higher register bit assignments.

Table 3-1100 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies Link ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies Link ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies Link ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies Link ID 20	RW	2'h0

The following image shows the lower register bit assignments.

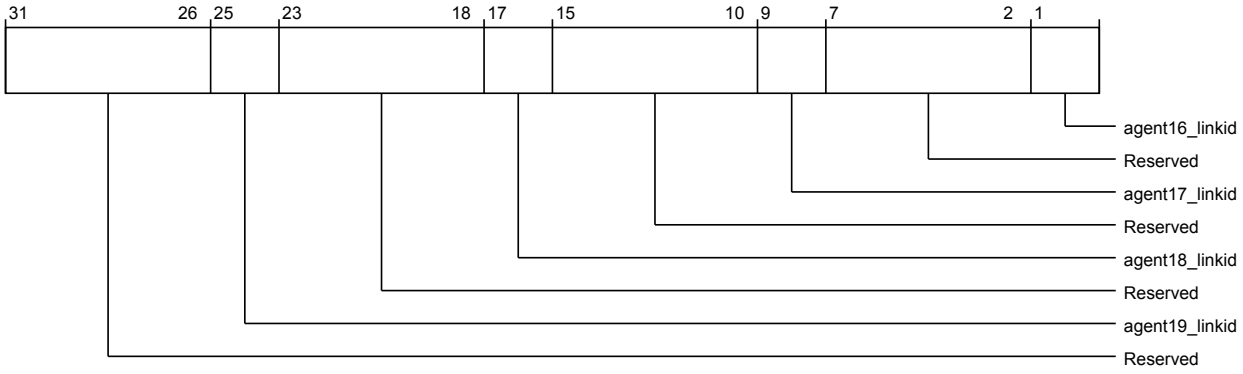


Figure 3-1087 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg2 lower register bit assignments.

Table 3-1101 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies Link ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies Link ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies Link ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies Link ID 16	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

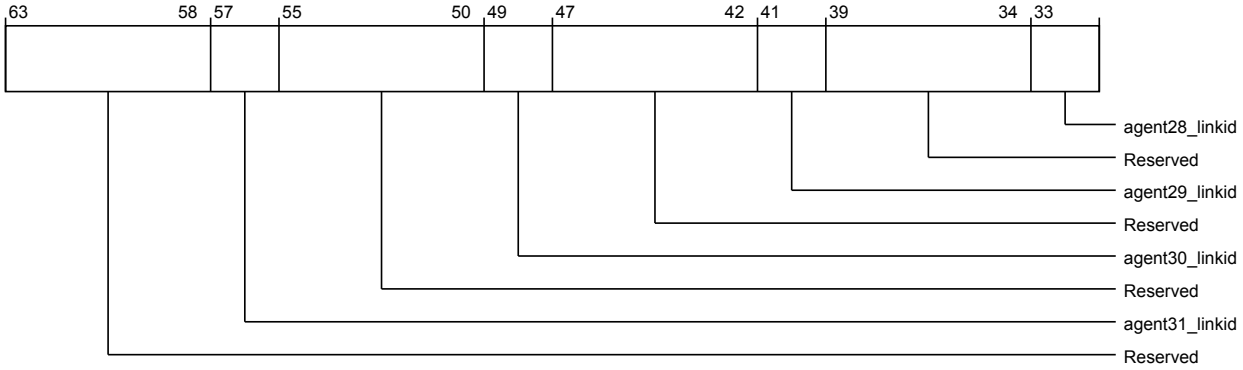


Figure 3-1088 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg3 higher register bit assignments.

Table 3-1102 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies Link ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies Link ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies Link ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies Link ID 28	RW	2'h0

The following image shows the lower register bit assignments.

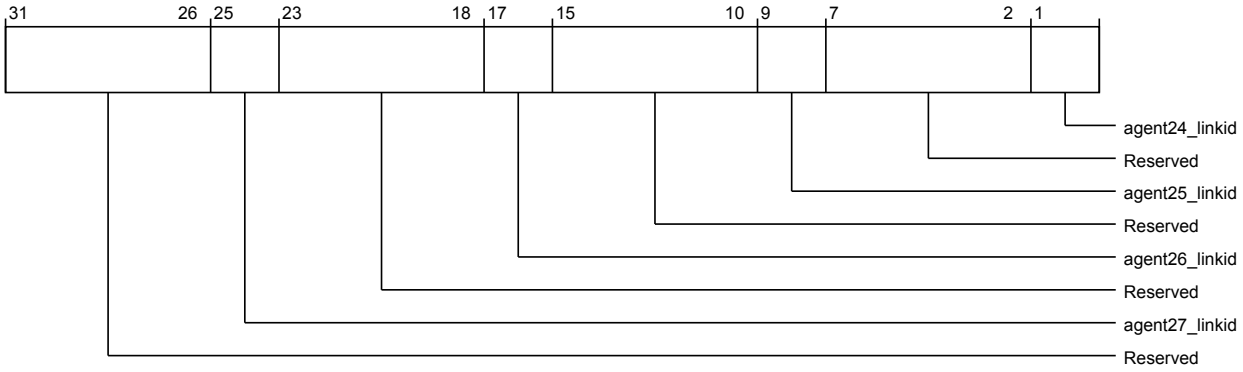


Figure 3-1089 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg3 lower register bit assignments.

Table 3-1103 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies Link ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies Link ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies Link ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies Link ID 24	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

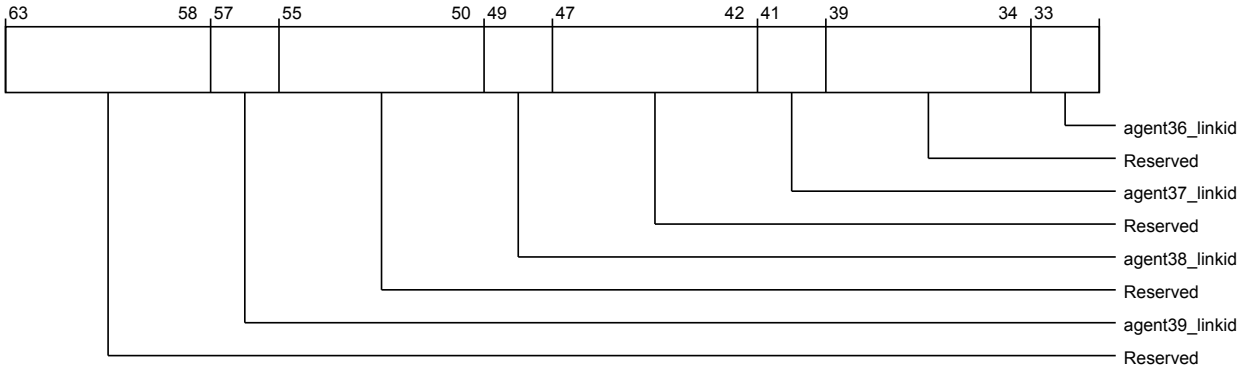


Figure 3-1090 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg4 higher register bit assignments.

Table 3-1104 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies Link ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies Link ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies Link ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies Link ID 36	RW	2'h0

The following image shows the lower register bit assignments.

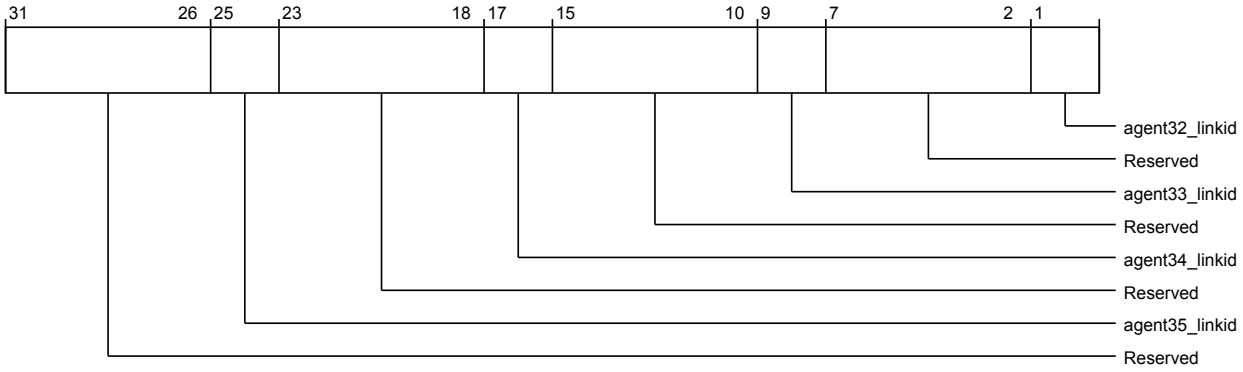


Figure 3-1091 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg4 lower register bit assignments.

Table 3-1105 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies Link ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies Link ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies Link ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies Link ID 32	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg5

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

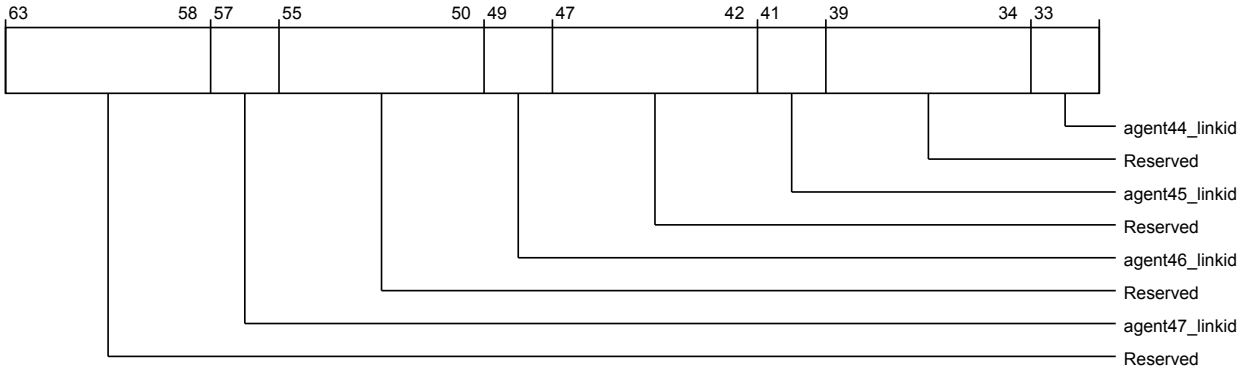


Figure 3-1092 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg5 higher register bit assignments.

Table 3-1106 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies Link ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies Link ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies Link ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies Link ID 44	RW	2'h0

The following image shows the lower register bit assignments.

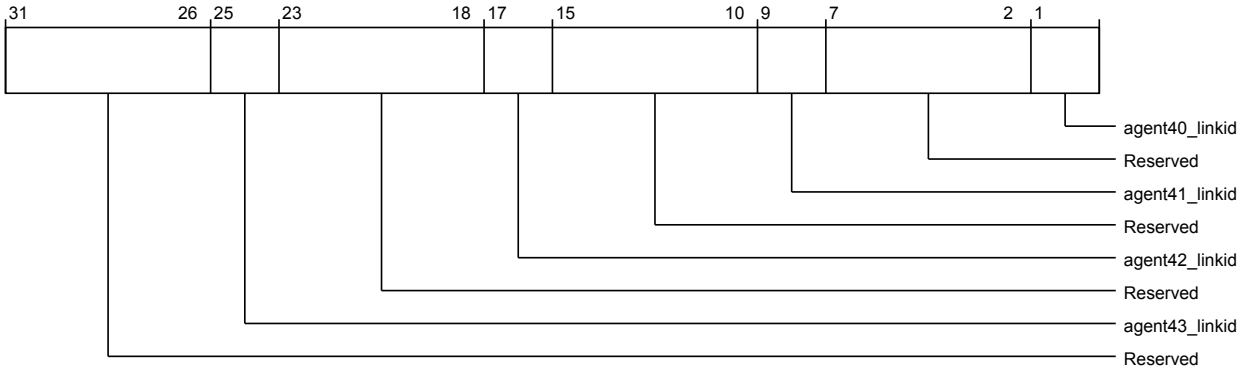


Figure 3-1093 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg5 lower register bit assignments.

Table 3-1107 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies Link ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies Link ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies Link ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies Link ID 40	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

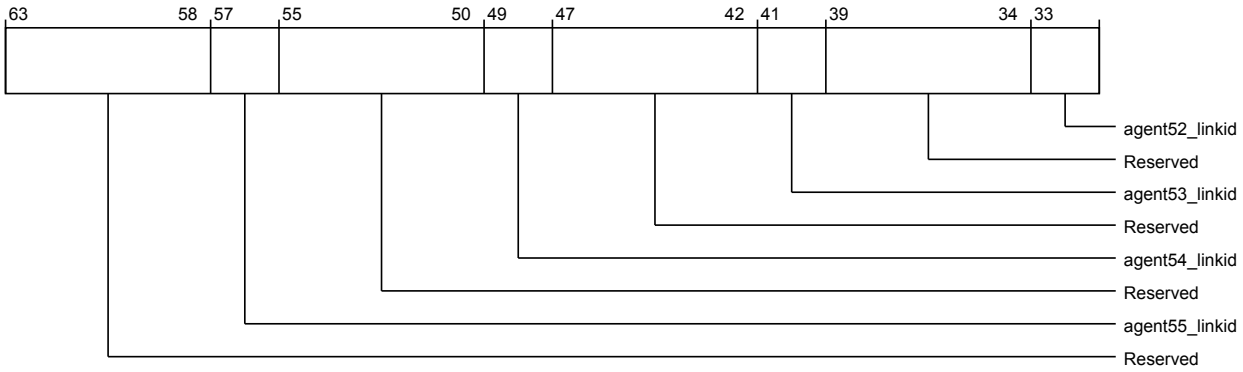


Figure 3-1094 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg6 higher register bit assignments.

Table 3-1108 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies Link ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies Link ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies Link ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies Link ID 52	RW	2'h0

The following image shows the lower register bit assignments.

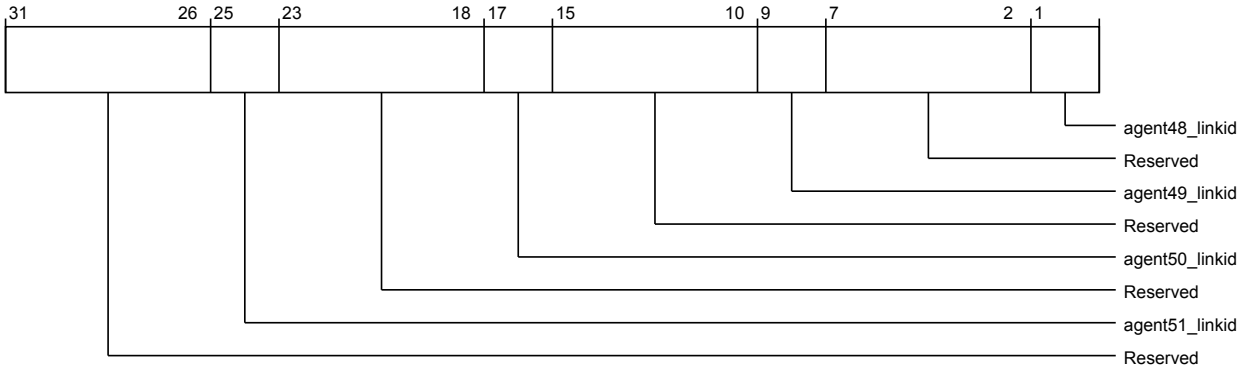


Figure 3-1095 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg6 lower register bit assignments.

Table 3-1109 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies Link ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies Link ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies Link ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies Link ID 48	RW	2'h0

por_cxg_ha_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

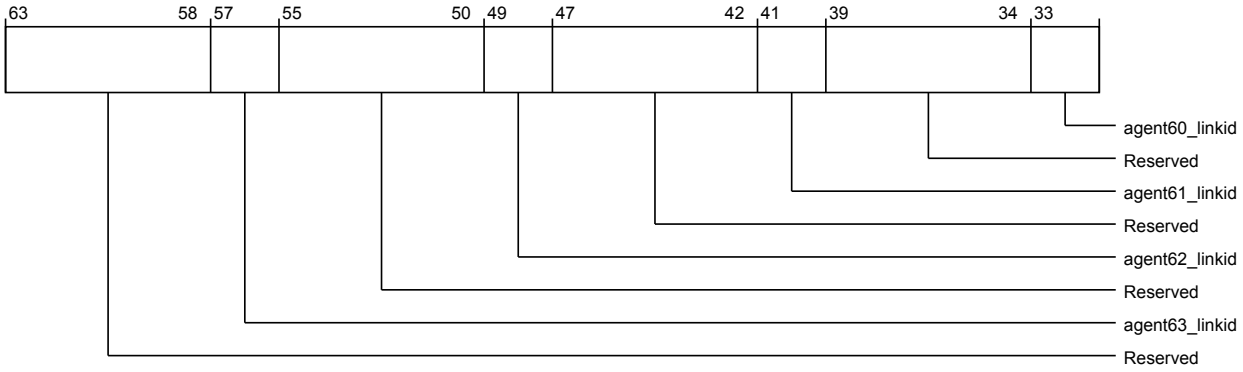


Figure 3-1096 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7 (high)

The following table shows the por_cxg_ha_agentid_to_linkid_reg7 higher register bit assignments.

Table 3-1110 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies Link ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies Link ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies Link ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies Link ID 60	RW	2'h0

The following image shows the lower register bit assignments.

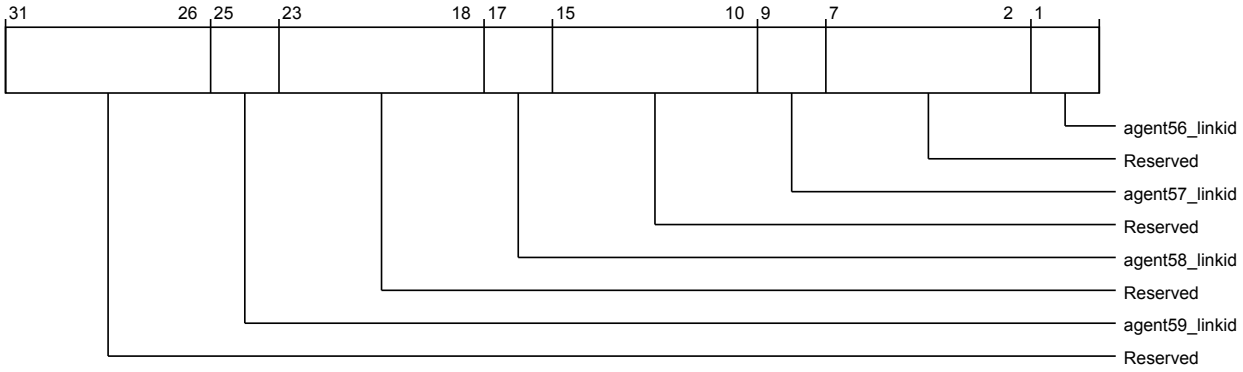


Figure 3-1097 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7 (low)

The following table shows the por_cxg_ha_agentid_to_linkid_reg7 lower register bit assignments.

Table 3-1111 por_cxg_ha_por_cxg_ha_agentid_to_linkid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies Link ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies Link ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies Link ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies Link ID 56	RW	2'h0

por_cxg_ha_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

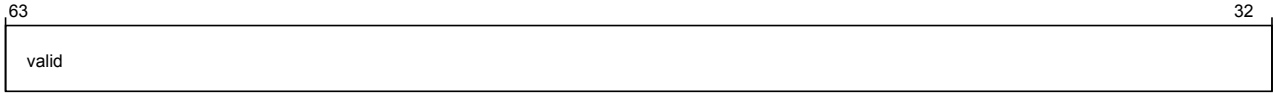


Figure 3-1098 por_cxg_ha_por_cxg_ha_agentid_to_linkid_val (high)

The following table shows the por_cxg_ha_agentid_to_linkid_val higher register bit assignments.

Table 3-1112 por_cxg_ha_por_cxg_ha_agentid_to_linkid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

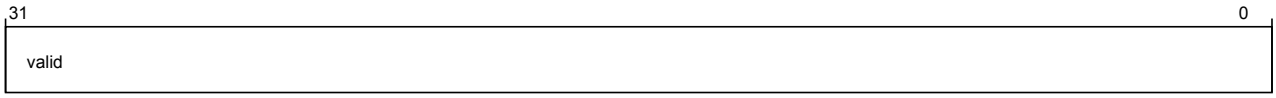


Figure 3-1099 por_cxg_ha_por_cxg_ha_agentid_to_linkid_val (low)

The following table shows the por_cxg_ha_agentid_to_linkid_val lower register bit assignments.

Table 3-1113 por_cxg_ha_por_cxg_ha_agentid_to_linkid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

por_cxg_ha_rnf_raid_to_ldid_val

Specifies which RAID to RN-F LDID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ha_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

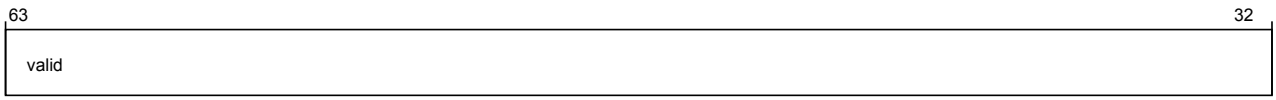


Figure 3-1100 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val (high)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_val higher register bit assignments.

Table 3-1114 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the LDID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

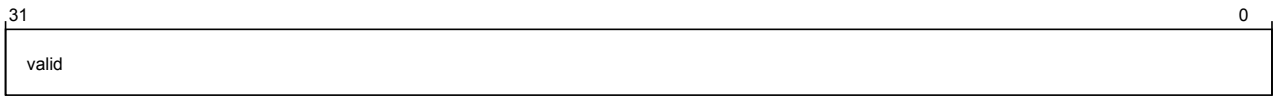


Figure 3-1101 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val (low)

The following table shows the por_cxg_ha_rnf_raid_to_ldid_val lower register bit assignments.

Table 3-1115 por_cxg_ha_por_cxg_ha_rnf_raid_to_ldid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the LDID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

por_cxg_ha_pmu_event_sel

Specifies the PMU event to be counted as a 6-bit ID with the following encodings: 6'b000000: CXHA_PMU_EVENT_NULL 6'b100001: CXHA_PMU_EVENT_RDDATBYP 6'b100010: CXHA_PMU_EVENT_CHIRSP_UP_STALL 6'b100011: CXHA_PMU_EVENT_CHIDAT_UP_STALL 6'b100100: CXHA_PMU_EVENT_SNPPCRD_LNK0_STALL 6'b100101: CXHA_PMU_EVENT_SNPPCRD_LNK1_STALL 6'b100110: CXHA_PMU_EVENT_SNPPCRD_LNK2_STALL 6'b100111: CXHA_PMU_EVENT_REQTRK_OCC 6'b101000: CXHA_PMU_EVENT_RDB_OCC 6'b101001: CXHA_PMU_EVENT_RDBBYP_OCC 6'b101010: CXHA_PMU_EVENT_WDB_OCC 6'b101011: CXHA_PMU_EVENT_SNPTRK_OCC 6'b101100: CXHA_PMU_EVENT_SDB_OCC 6'b101101: CXHA_PMU_EVENT_SNPHAZ_OCC

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

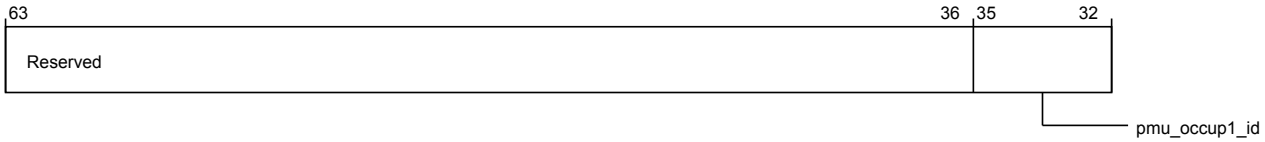


Figure 3-1102 por_cxg_ha_por_cxg_ha_pmu_event_sel (high)

The following table shows the por_cxg_ha_pmu_event_sel higher register bit assignments.

Table 3-1116 por_cxg_ha_por_cxg_ha_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	CXHA PMU occupancy event selector ID	RW	4'b0

The following image shows the lower register bit assignments.

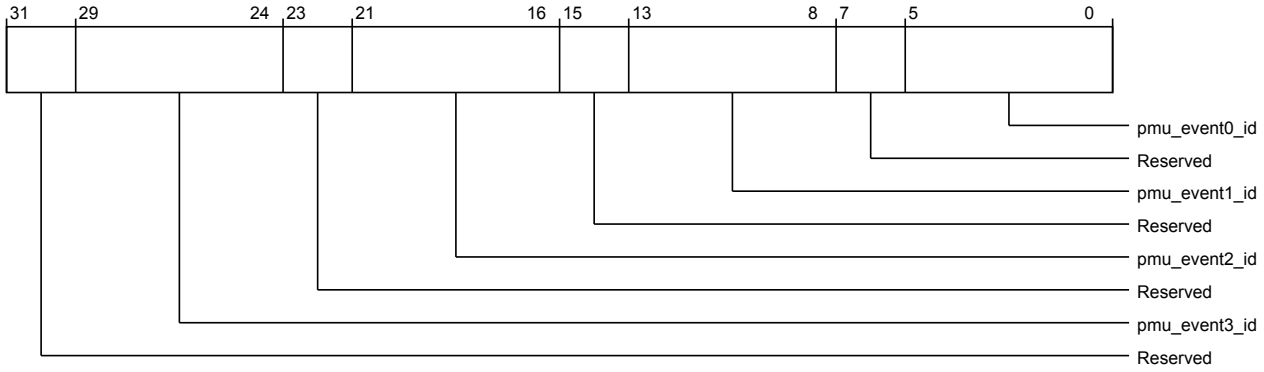


Figure 3-1103 por_cxg_ha_por_cxg_ha_pmu_event_sel (low)

The following table shows the por_cxg_ha_pmu_event_sel lower register bit assignments.

Table 3-1117 por_cxg_ha_por_cxg_ha_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	CXHA PMU Event 3 ID	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	CXHA PMU Event 2 ID	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	CXHA PMU Event 1 ID	RW	6'b0
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	CXHA PMU Event 0 ID	RW	6'b0

por_cxg_ha_cxprtcl_link0_ctl

Functions as the CXHA CCIX Protocol Link 0 control register. Works with por_cxg_ha_cxprtcl_link0_status.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1000

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

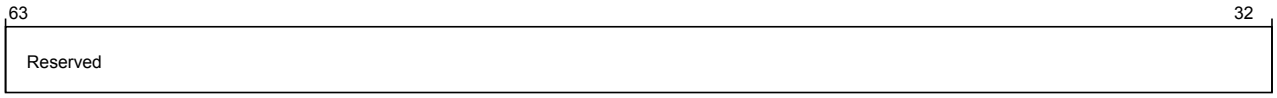


Figure 3-1104 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link0_ctl higher register bit assignments.

Table 3-1118 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

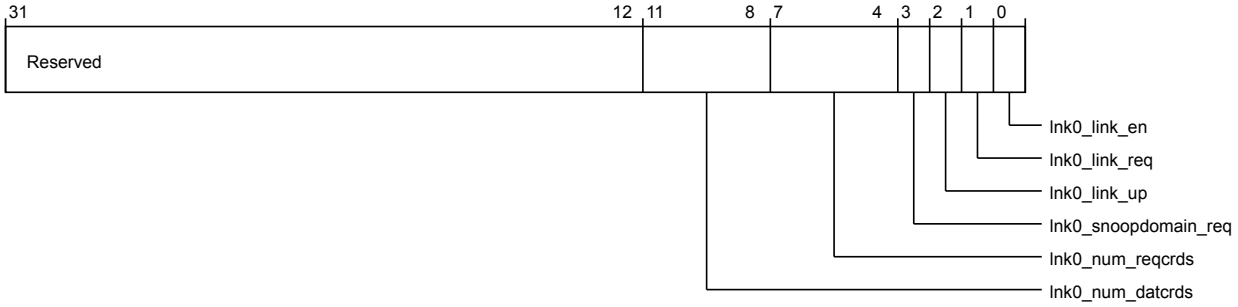


Figure 3-1105 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link0_ctl lower register bit assignments.

Table 3-1119 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	lnk0_num_datcrds	Controls the number of CCIX data credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0

Table 3-1119 por_cxg_ha_por_cxg_ha_cxprtcl_link0_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
7:4	lnk0_num_reqcrds	Controls the number of CCIX request credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk0_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0
2	lnk0_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk0_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk0_link_en	Enables CCIX Link 0 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link0_status

Functions as the CXHA CCIX Protocol Link 0 status register. Works with por_cxg_ha_cxprtcl_link0_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1008
Register reset 64'b010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

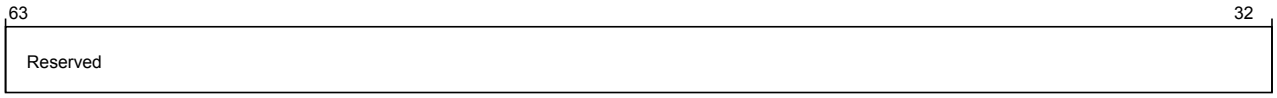


Figure 3-1106 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (high)

The following table shows the por_cxg_ha_cxprtcl_link0_status higher register bit assignments.

Table 3-1120 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

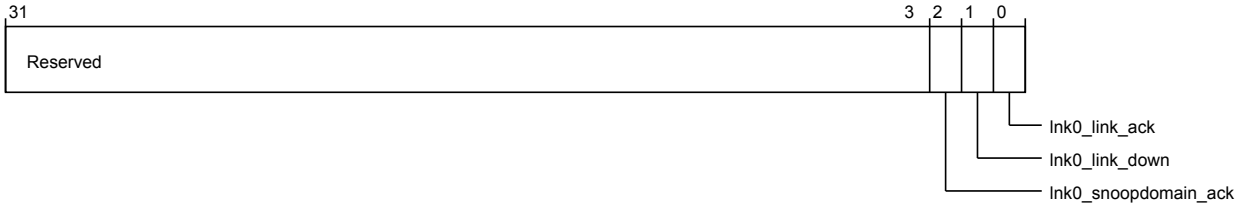


Figure 3-1107 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (low)

The following table shows the por_cxg_ha_cxprtcl_link0_status lower register bit assignments.

Table 3-1121 por_cxg_ha_por_cxg_ha_cxprtcl_link0_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	lnk0_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
1	lnk0_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk0_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_cxprtcl_link1_ctl

Functions as the CXHA CCIX Protocol Link 1 control register. Works with por_cxg_ha_cxprtcl_link1_status.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

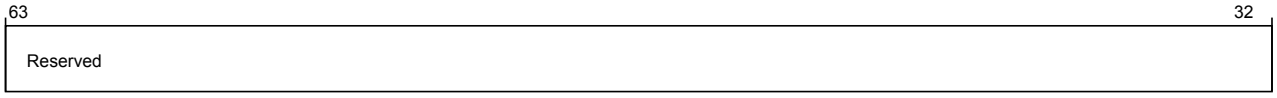


Figure 3-1108 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link1_ctl higher register bit assignments.

Table 3-1122 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

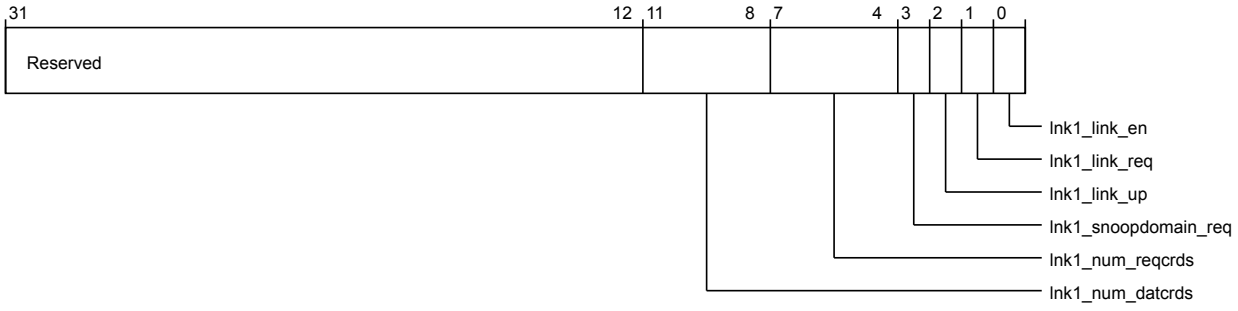


Figure 3-1109 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link1_ctl lower register bit assignments.

Table 3-1123 por_cxg_ha_por_cxg_ha_cxprtcl_link1_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	lnk1_num_datcrds	Controls the number of CCIX data credits assigned to Link 1 4'h0: Total credits equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
7:4	lnk1_num_reqcrds	Controls the number of CCIX request credits assigned to Link 1 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk1_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0
2	lnk1_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk1_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk1_link_en	Enables CCIX Link 1 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link1_status

Functions as the CXHA CCIX Protocol Link 1 status register. Works with por_cxg_ha_cxprtcl_link1_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1018
Register reset 64'b010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

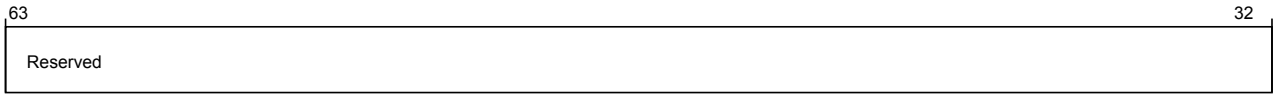


Figure 3-1110 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (high)

The following table shows the por_cxg_ha_cxprtcl_link1_status higher register bit assignments.

Table 3-1124 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

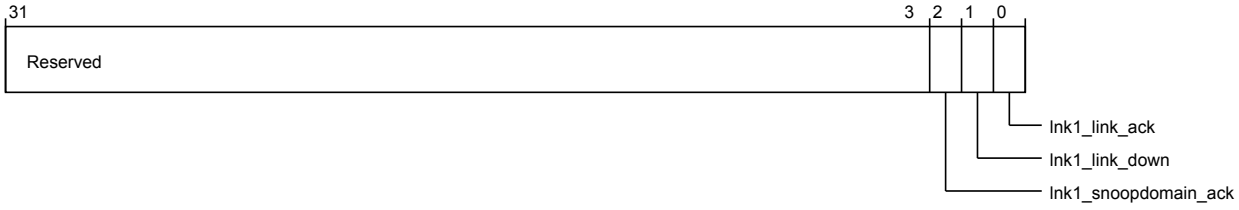


Figure 3-1111 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low)

The following table shows the por_cxg_ha_cxprtcl_link1_status lower register bit assignments.

Table 3-1125 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	lnk1_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 1	RO	1'b0

Table 3-1125 por_cxg_ha_por_cxg_ha_cxprtcl_link1_status (low) (continued)

Bits	Field name	Description	Type	Reset
1	lnk1_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk1_link_ack	Link Up/Down Acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_cxprtcl_link2_ctl

Functions as the CXHA CCIX Protocol Link 2 control register. Works with por_cxg_ha_cxprtcl_link2_status.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

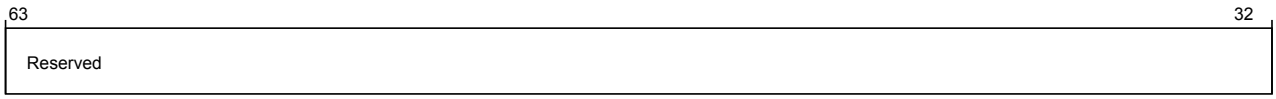


Figure 3-1112 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (high)

The following table shows the por_cxg_ha_cxprtcl_link2_ctl higher register bit assignments.

Table 3-1126 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

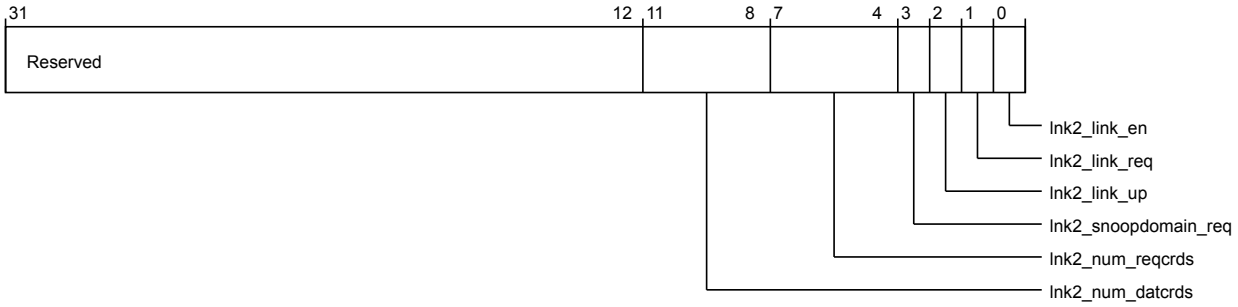


Figure 3-1113 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low)

The following table shows the por_cxg_ha_cxprtcl_link2_ctl lower register bit assignments.

Table 3-1127 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low)

Bits	Field name	Description	Type	Reset
31:12	Reserved	Reserved	RO	-
11:8	lnk2_num_datcrds	Controls the number of CCIX data credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
7:4	lnk2_num_reqcrds	Controls the number of CCIX request credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk2_snoopdomain_req	Controls Snoop domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0
2	lnk2_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0

Table 3-1127 por_cxg_ha_por_cxg_ha_cxprtcl_link2_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
1	lnk2_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk2_link_en	Enables CCIX Link 2 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ha_cxprtcl_link2_status

Functions as the CXHA CCIX Protocol Link 2 status register. Works with por_cxg_ha_cxprtcl_link2_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1028
Register reset 64'b010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

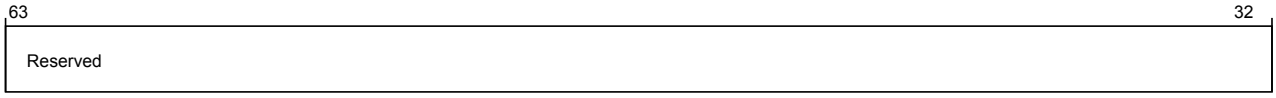


Figure 3-1114 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (high)

The following table shows the por_cxg_ha_cxprtcl_link2_status higher register bit assignments.

Table 3-1128 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

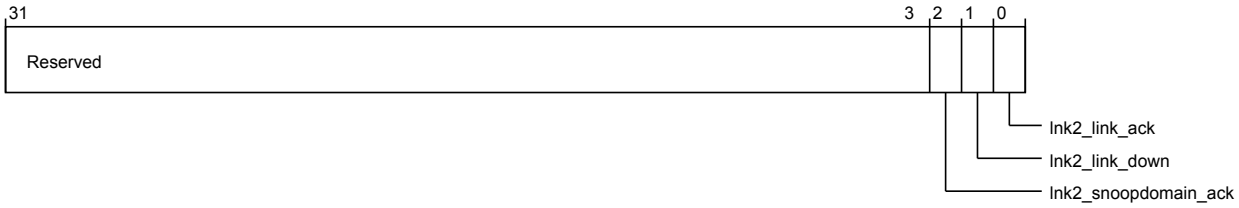


Figure 3-1115 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (low)

The following table shows the por_cxg_ha_cxprtcl_link2_status lower register bit assignments.

Table 3-1129 por_cxg_ha_por_cxg_ha_cxprtcl_link2_status (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	lnk2_snoopdomain_ack	Provides Snoop domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
1	lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk2_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ha_errfr

Functions as the error feature register.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h3000
Register reset 64'b0000010100101
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

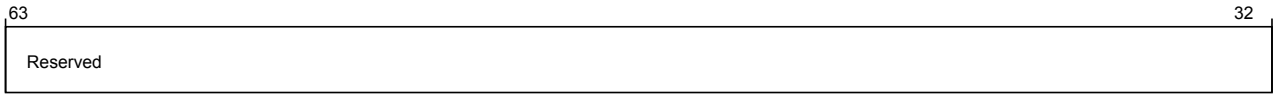


Figure 3-1116 por_cxg_ha_por_cxg_ha_errfr (high)

The following table shows the por_cxg_ha_errfr higher register bit assignments.

Table 3-1130 por_cxg_ha_por_cxg_ha_errfr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

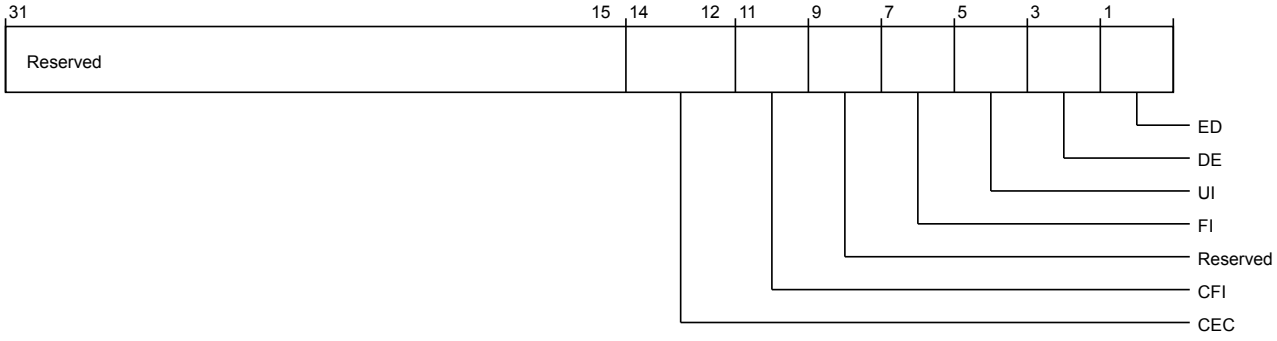


Figure 3-1117 por_cxg_ha_por_cxg_ha_errfr (low)

The following table shows the por_cxg_ha_errfr lower register bit assignments.

Table 3-1131 por_cxg_ha_por_cxg_ha_errfr (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_cxg_ha_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_cxg_ha_errmisc[47:32]	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_cxg_ha_errctlr

Functions as the error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3008

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

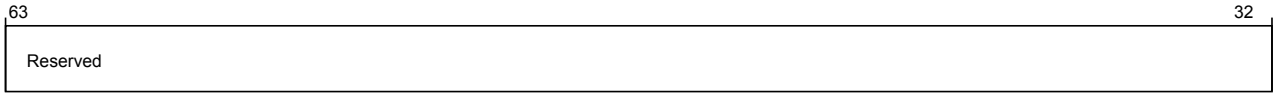


Figure 3-1118 por_cxg_ha_por_cxg_ha_errctlr (high)

The following table shows the por_cxg_ha_errctlr higher register bit assignments.

Table 3-1132 por_cxg_ha_por_cxg_ha_errctlr (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

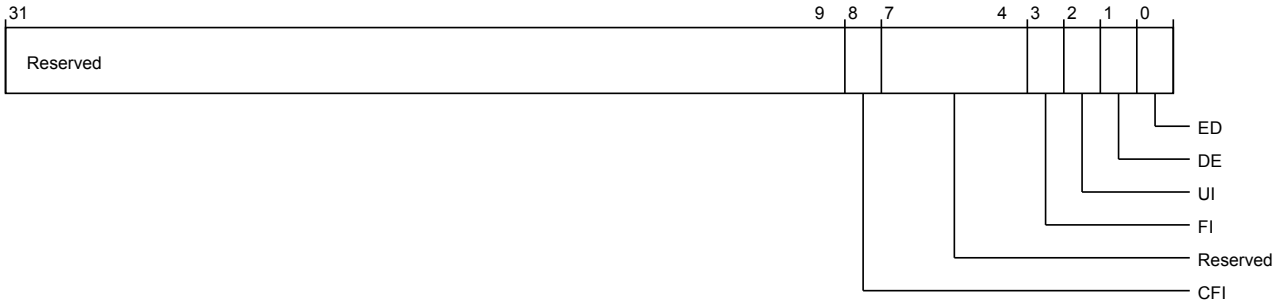


Figure 3-1119 por_cxg_ha_por_cxg_ha_errctlr (low)

The following table shows the por_cxg_ha_errctlr lower register bit assignments.

Table 3-1133 por_cxg_ha_por_cxg_ha_errctlr (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_cxg_ha_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 3-1133 por_cxg_ha_por_cxg_ha_errctlr (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_cxg_ha_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_cxg_ha_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_cxg_ha_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_cxg_ha_errfr.ED	RW	1'b0

por_cxg_ha_errstatus

Functions as the error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

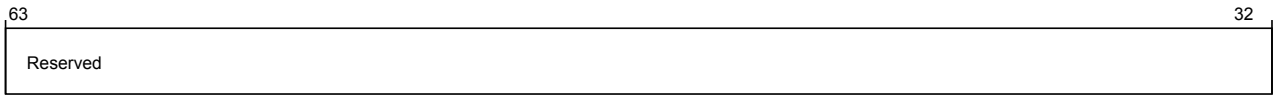


Figure 3-1120 por_cxg_ha_por_cxg_ha_errstatus (high)

The following table shows the por_cxg_ha_errstatus higher register bit assignments.

Table 3-1134 por_cxg_ha_por_cxg_ha_errstatus (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-1121 por_cxg_ha_por_cxg_ha_errstatus (low)

The following table shows the por_cxg_ha_errstatus lower register bit assignments.

Table 3-1135 por_cxg_ha_por_cxg_ha_errstatus (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_cxg_ha_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_cxg_ha_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 3-1135 por_cxg_ha_por_cxg_ha_errstatus (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_cxg_ha_erraddr

Contains the error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3018
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

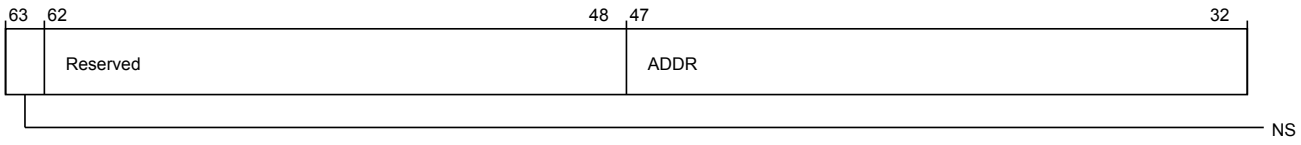


Figure 3-1122 por_cxg_ha_por_cxg_ha_erraddr (high)

The following table shows the por_cxg_ha_erraddr higher register bit assignments.

Table 3-1136 por_cxg_ha_por_cxg_ha_erraddr (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_cxg_ha_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

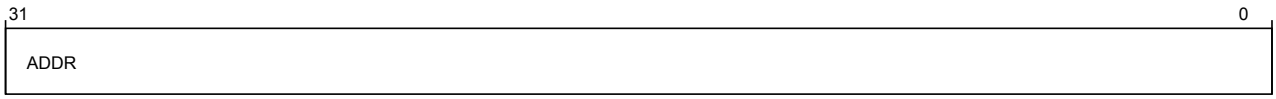


Figure 3-1123 por_cxg_ha_por_cxg_ha_erraddr (low)

The following table shows the por_cxg_ha_erraddr lower register bit assignments.

Table 3-1137 por_cxg_ha_por_cxg_ha_erraddr (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_cxg_ha_errmisc

Functions as the miscellaneous error register. Contains miscellaneous information about deferred/ uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3020
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

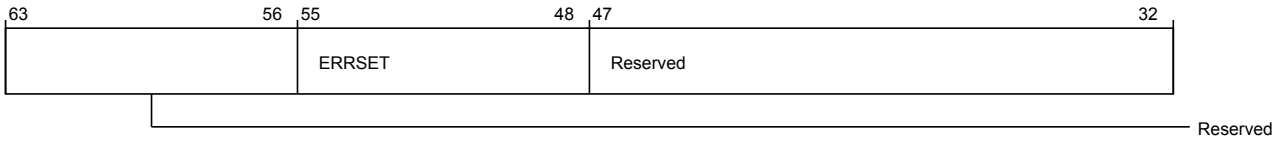


Figure 3-1124 por_cxg_ha_por_cxg_ha_errmisc (high)

The following table shows the por_cxg_ha_errmisc higher register bit assignments.

Table 3-1138 por_cxg_ha_por_cxg_ha_errmisc (high)

Bits	Field name	Description	Type	Reset
63:56	Reserved	Reserved	RO	-
55:48	ERRSET	RAM entry set address for parity error	RW	8'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

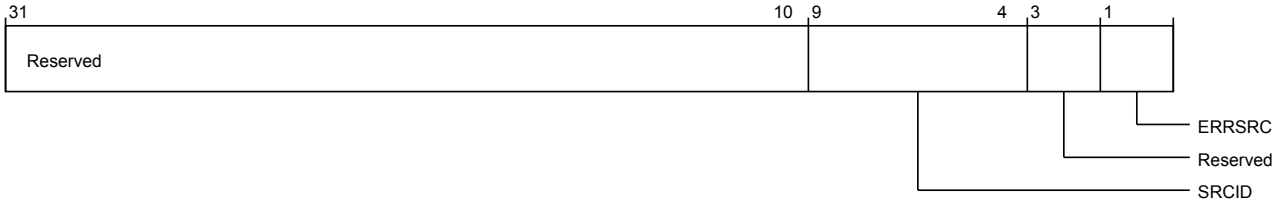


Figure 3-1125 por_cxg_ha_por_cxg_ha_errmisc (low)

The following table shows the por_cxg_ha_errmisc lower register bit assignments.

Table 3-1139 por_cxg_ha_por_cxg_ha_errmisc (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:4	SRCID	CCIX RAID of the requestor or the snoop target	RW	6'b0
3:2	Reserved	Reserved	RO	-
1:0	ERRSRC	Source of the parity error 2'b00: Read data buffer 0 2'b01: Read data buffer 1 2'b10: Write data buffer 0 2'b11: Write data buffer 1	RW	2'b00

por_cxg_ha_errfr_NS

Functions as the non-secure error feature register.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h3100

Register reset 64'b0000010100101

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

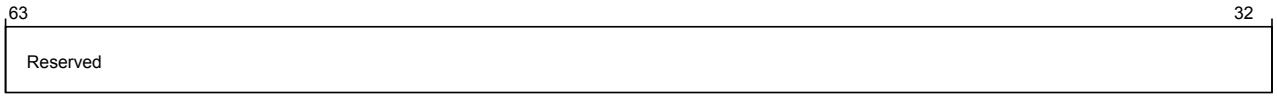


Figure 3-1126 por_cxg_ha_por_cxg_ha_errfr_ns (high)

The following table shows the por_cxg_ha_errfr_NS higher register bit assignments.

Table 3-1140 por_cxg_ha_por_cxg_ha_errfr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

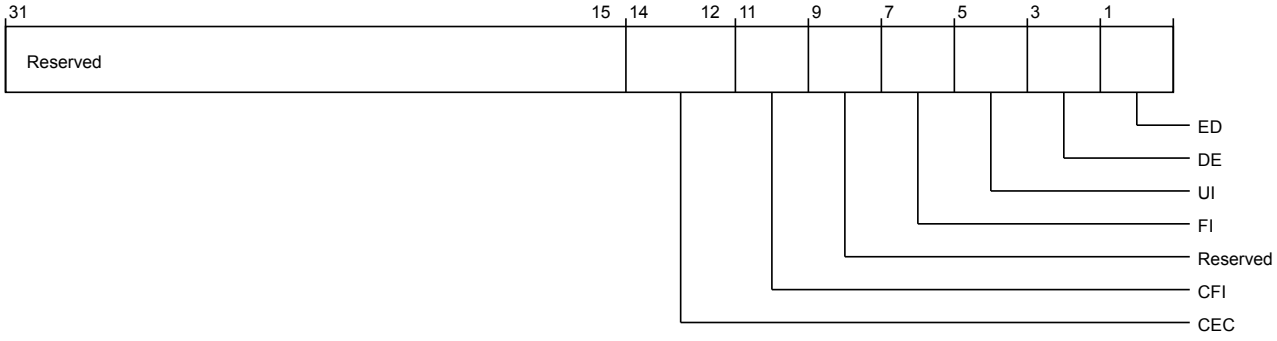


Figure 3-1127 por_cxg_ha_por_cxg_ha_errfr_ns (low)

The following table shows the por_cxg_ha_errfr_NS lower register bit assignments.

Table 3-1141 por_cxg_ha_por_cxg_ha_errfr_ns (low)

Bits	Field name	Description	Type	Reset
31:15	Reserved	Reserved	RO	-
14:12	CEC	Standard corrected error count mechanism 3'b000: Does not implement standardized error counter model 3'b010: Implements 8-bit error counter in por_cxg_ha_errmisc[39:32] 3'b100: Implements 16-bit error counter in por_cxg_ha_errmisc[47:32]	RO	3'b000
11:10	CFI	Corrected error interrupt	RO	2'b00
9:8	Reserved	Reserved	RO	-
7:6	FI	Fault handling interrupt	RO	2'b10
5:4	UI	Uncorrected error interrupt	RO	2'b10
3:2	DE	Deferred errors for data poison	RO	2'b01
1:0	ED	Error detection	RO	2'b01

por_cxg_ha_errctlr_NS

Functions as the non-secure error control register. Controls whether specific error-handling interrupts and error detection/deferment are enabled.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h3108

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

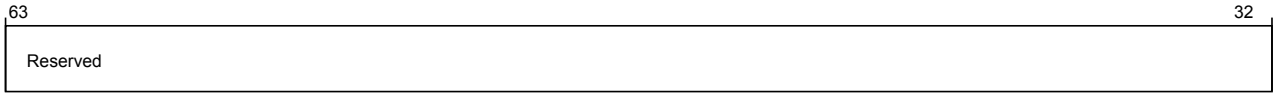


Figure 3-1128 por_cxg_ha_por_cxg_ha_errctlr_ns (high)

The following table shows the por_cxg_ha_errctlr_NS higher register bit assignments.

Table 3-1142 por_cxg_ha_por_cxg_ha_errctlr_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

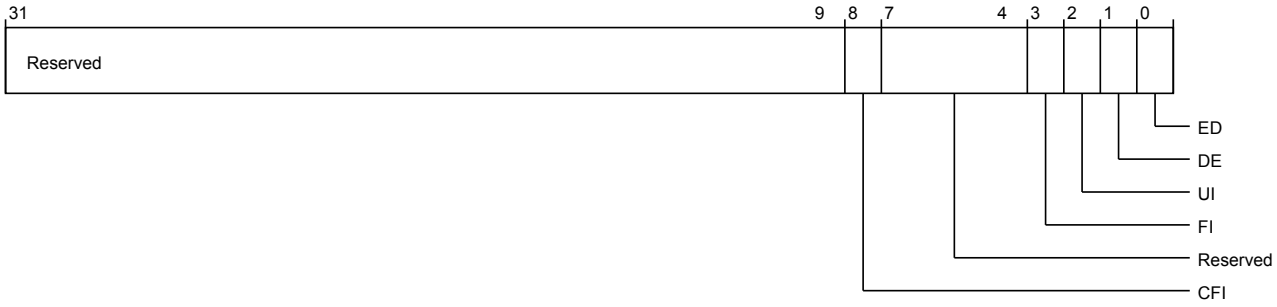


Figure 3-1129 por_cxg_ha_por_cxg_ha_errctlr_ns (low)

The following table shows the por_cxg_ha_errctlr_NS lower register bit assignments.

Table 3-1143 por_cxg_ha_por_cxg_ha_errctlr_ns (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	CFI	Enables corrected error interrupt as specified in por_cxg_ha_errfr.CFI	RW	1'b0
7:4	Reserved	Reserved	RO	-

Table 3-1143 por_cxg_ha_por_cxg_ha_errctlr_ns (low) (continued)

Bits	Field name	Description	Type	Reset
3	FI	Enables fault handling interrupt for all detected deferred errors as specified in por_cxg_ha_errfr.FI	RW	1'b0
2	UI	Enables uncorrected error interrupt as specified in por_cxg_ha_errfr.UI	RW	1'b0
1	DE	Enables error deferment as specified in por_cxg_ha_errfr.DE	RW	1'b0
0	ED	Enables error detection as specified in por_cxg_ha_errfr.ED	RW	1'b0

por_cxg_ha_errstatus_NS

Functions as the non-secure error status register. AV and MV bits must be cleared in the same cycle, otherwise the error record does not have a consistent view.

Its characteristics are:

Type W1C

Register width (Bits) 64

Address offset 14'h3110

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

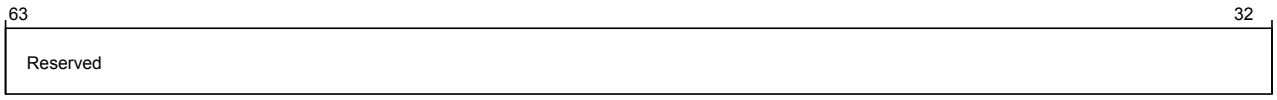


Figure 3-1130 por_cxg_ha_por_cxg_ha_errstatus_ns (high)

The following table shows the por_cxg_ha_errstatus_NS higher register bit assignments.

Table 3-1144 por_cxg_ha_por_cxg_ha_errstatus_ns (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

Figure 3-1131 por_cxg_ha_por_cxg_ha_errstatus_ns (low)

The following table shows the por_cxg_ha_errstatus_NS lower register bit assignments.

Table 3-1145 por_cxg_ha_por_cxg_ha_errstatus_ns (low)

Bits	Field name	Description	Type	Reset
31	AV	Address register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Address is valid; por_cxg_ha_erraddr contains a physical address for that recorded error 1'b0: Address is not valid	W1C	1'b0
30	V	Register valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and are not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error recorded; register is valid 1'b0: No errors recorded	W1C	1'b0
29	UE	Uncorrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error detected that is not corrected and is not deferred to a slave 1'b0: No uncorrected errors detected	W1C	1'b0
28	Reserved	Reserved	RO	-
27	OF	Overflow; asserted when multiple errors of the highest priority type are detected; write a 1 to clear 1'b1: More than one error detected 1'b0: Only one error of the highest priority type detected as described by UE/DE/CE fields	W1C	1'b0
26	MV	por_cxg_ha_errmisc valid; writes to this bit are ignored if any of the UE, DE, or CE bits are set to 1, and the highest priority are not cleared to 0 in the same write; write a 1 to clear 1'b1: Miscellaneous registers are valid 1'b0: Miscellaneous registers are not valid	W1C	1'b0
25	Reserved	Reserved	RO	-

Table 3-1145 por_cxg_ha_por_cxg_ha_errstatus_ns (low) (continued)

Bits	Field name	Description	Type	Reset
24	CE	Corrected errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one transient corrected error recorded 1'b0: No corrected errors recorded	W1C	1'b0
23	DE	Deferred errors; writes to this bit are ignored if the OF bit is set to 1, and is not cleared to 0 in the same write; write a 1 to clear 1'b1: At least one error is not corrected and is deferred 1'b0: No errors deferred	W1C	1'b0
22:0	Reserved	Reserved	RO	-

por_cxg_ha_erraddr_NS

Contains the non-secure error record address.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3118
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

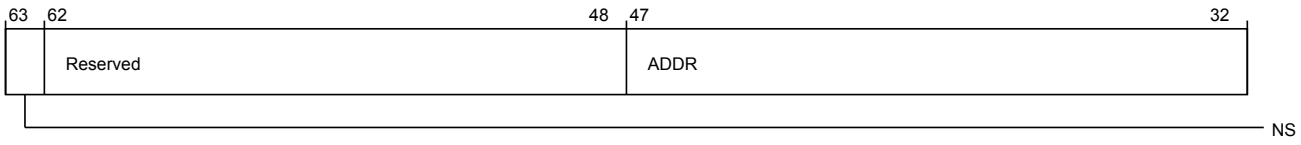


Figure 3-1132 por_cxg_ha_por_cxg_ha_erraddr_ns (high)

The following table shows the por_cxg_ha_erraddr_NS higher register bit assignments.

Table 3-1146 por_cxg_ha_por_cxg_ha_erraddr_ns (high)

Bits	Field name	Description	Type	Reset
63	NS	Security status of transaction 1'b1: Non-secure transaction 1'b0: Secure transaction CONSTRAINT: por_cxg_ha_erraddr.NS is redundant. Since it is writable, it cannot be used for logic qualification.	RW	1'b0
62:48	Reserved	Reserved	RO	-
47:32	ADDR	Transaction address	RW	48'b0

The following image shows the lower register bit assignments.

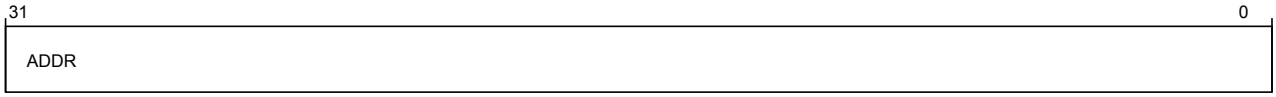


Figure 3-1133 por_cxg_ha_por_cxg_ha_erraddr_ns (low)

The following table shows the por_cxg_ha_erraddr_NS lower register bit assignments.

Table 3-1147 por_cxg_ha_por_cxg_ha_erraddr_ns (low)

Bits	Field name	Description	Type	Reset
31:0	ADDR	Transaction address	RW	48'b0

por_cxg_ha_errmisc_NS

Functions as the non-secure miscellaneous error register. Contains miscellaneous information about deferred/uncorrected errors.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h3120
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

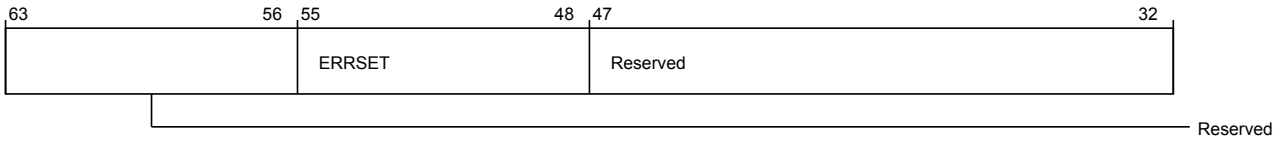


Figure 3-1134 por_cxg_ha_por_cxg_ha_errmisc_ns (high)

The following table shows the por_cxg_ha_errmisc_NS higher register bit assignments.

Table 3-1148 por_cxg_ha_por_cxg_ha_errmisc_ns (high)

Bits	Field name	Description	Type	Reset
63:56	Reserved	Reserved	RO	-
55:48	ERRSET	RAM entry set address for parity error	RW	8'b0
47:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

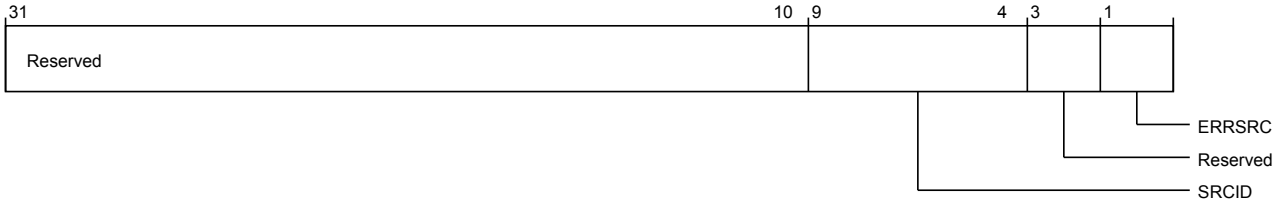


Figure 3-1135 por_cxg_ha_por_cxg_ha_errmisc_ns (low)

The following table shows the por_cxg_ha_errmisc_NS lower register bit assignments.

Table 3-1149 por_cxg_ha_por_cxg_ha_errmisc_ns (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:4	SRCID	CCIX RAID of the requestor or the snoop target	RW	6'b0
3:2	Reserved	Reserved	RO	-
1:0	ERRSRC	Source of the parity error 2'b00: Read data buffer 0 2'b01: Read data buffer 1 2'b10: Write data buffer 0 2'b11: Write data buffer 1	RW	2'b00

3.3.12 CXRA configuration registers

This section lists the CXRA configuration registers.

por_cxg_ra_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

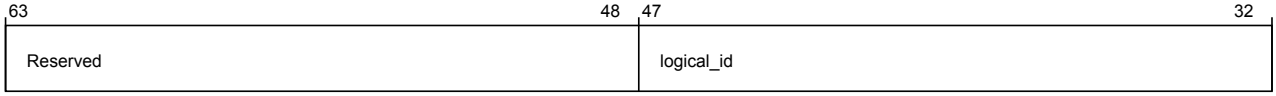


Figure 3-1136 por_cxg_ra_por_cxg_ra_node_info (high)

The following table shows the por_cxg_ra_node_info higher register bit assignments.

Table 3-1150 por_cxg_ra_por_cxg_ra_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

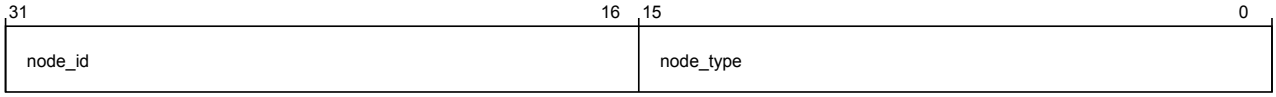


Figure 3-1137 por_cxg_ra_por_cxg_ra_node_info (low)

The following table shows the por_cxg_ra_node_info lower register bit assignments.

Table 3-1151 por_cxg_ra_por_cxg_ra_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0100

por_cxg_ra_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

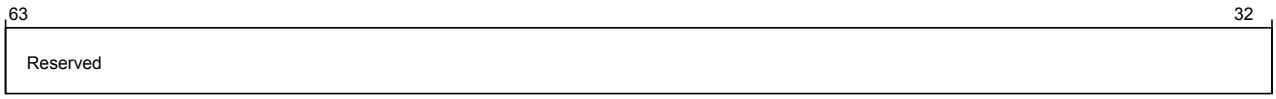


Figure 3-1138 por_cxg_ra_por_cxg_ra_child_info (high)

The following table shows the por_cxg_ra_child_info higher register bit assignments.

Table 3-1152 por_cxg_ra_por_cxg_ra_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

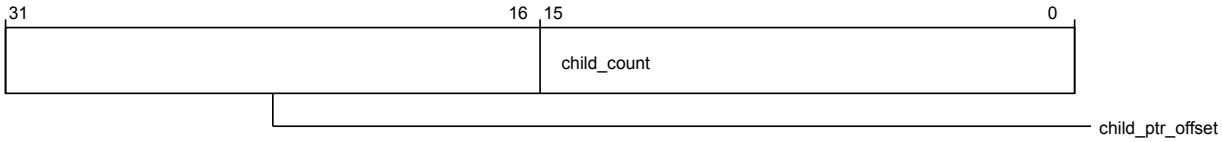


Figure 3-1139 por_cxg_ra_por_cxg_ra_child_info (low)

The following table shows the por_cxg_ra_child_info lower register bit assignments.

Table 3-1153 por_cxg_ra_por_cxg_ra_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'h0

por_cxg_ra_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

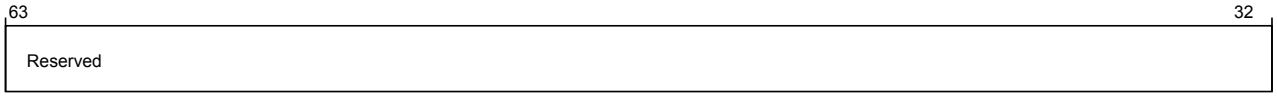


Figure 3-1140 por_cxg_ra_por_cxg_ra_secure_register_groups_override (high)

The following table shows the por_cxg_ra_secure_register_groups_override higher register bit assignments.

Table 3-1154 por_cxg_ra_por_cxg_ra_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

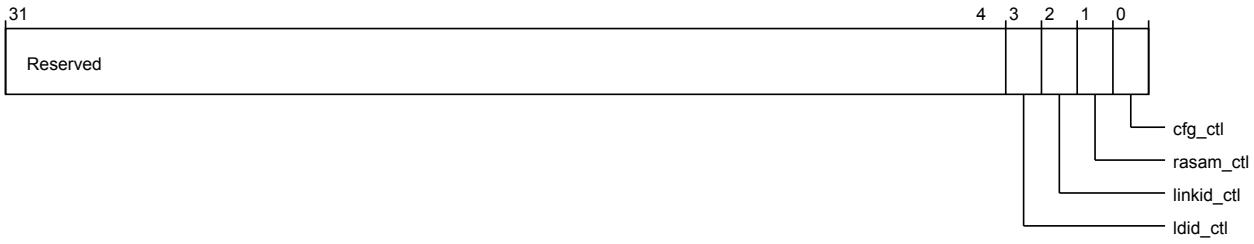


Figure 3-1141 por_cxg_ra_por_cxg_ra_secure_register_groups_override (low)

The following table shows the por_cxg_ra_secure_register_groups_override lower register bit assignments.

Table 3-1155 por_cxg_ra_por_cxg_ra_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	ldid_ctl	Allows non-secure access to secure RA LDID registers	RW	1'b0
2	linkid_ctl	Allows non-secure access to secure RA Link ID registers	RW	1'b0
1	rasam_ctl	Allows non-secure access to secure RA SAM control registers	RW	1'b0
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_cxg_ra_unit_info

Provides component identification information for CXRA.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

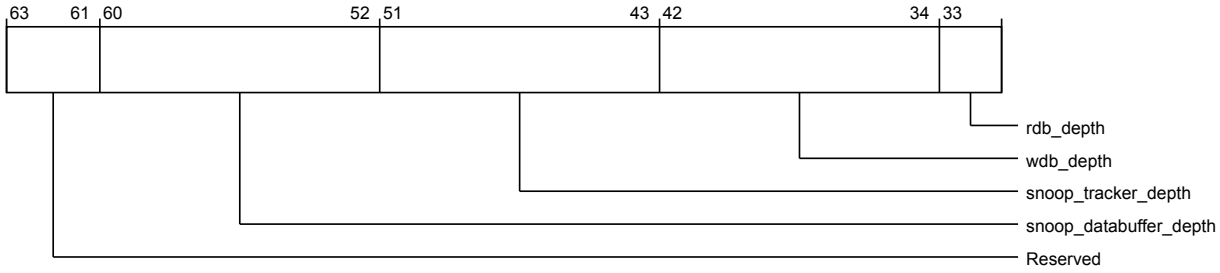


Figure 3-1142 por_cxg_ra_por_cxg_ra_unit_info (high)

The following table shows the por_cxg_ra_unit_info higher register bit assignments.

Table 3-1156 por_cxg_ra_por_cxg_ra_unit_info (high)

Bits	Field name	Description	Type	Reset
63:61	Reserved	Reserved	RO	-
60:52	snoop_databuffer_depth	Depth of Snoop Data Buffer - number of outstanding SNP requests on CHI	RO	Configuration dependent
51:43	snoop_tracker_depth	Depth of Snoop Tracker - number of outstanding SNP requests on CCIX	RO	Configuration dependent
42:34	wdb_depth	Depth of Write Data Buffer	RO	Configuration dependent
33:32	rdb_depth	Depth of Read Data Buffer	RO	Configuration dependent

The following image shows the lower register bit assignments.

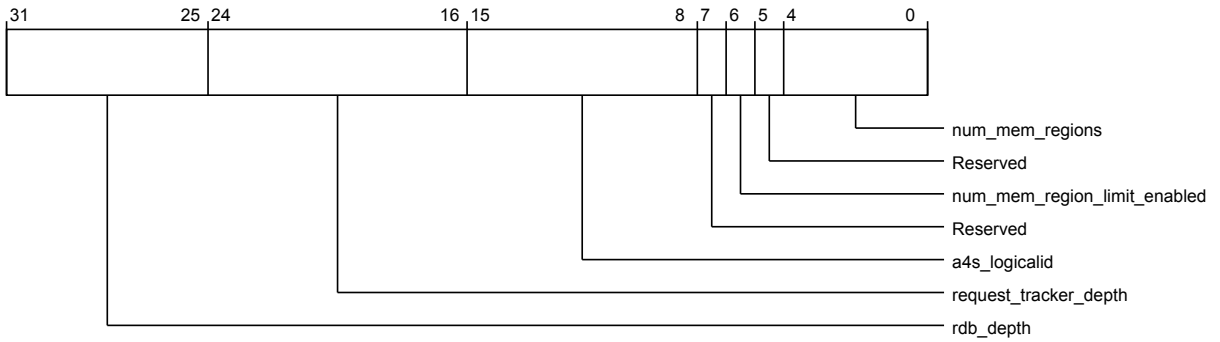


Figure 3-1143 por_cxg_ra_por_cxg_ra_unit_info (low)

The following table shows the por_cxg_ra_unit_info lower register bit assignments.

Table 3-1157 por_cxg_ra_por_cxg_ra_unit_info (low)

Bits	Field name	Description	Type	Reset
31:25	rdb_depth	Depth of Read Data Buffer	RO	Configuration dependent
24:16	request_tracker_depth	Depth of Request Tracker - number of outstanding Memory requests on CCIX	RO	Configuration dependent
15:8	a4s_logicalid	AXI4Stream interfaces logical ID	RO	Configuration dependent
7	Reserved	Reserved	RO	-
6	num_mem_region_limit_enabled	Memory region limiting enabled	RO	Configuration dependent
5	Reserved	Reserved	RO	-
4:0	num_mem_regions	Number of memory regions supported	RO	Configuration dependent

por_cxg_ra_cfg_ctl

Functions as the configuration control register. Specifies the current mode.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA00

Register reset 10'h2

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

Secure group override por_cxg_ra_secure_register_groups_override.cfg_ctl

The following image shows the higher register bit assignments.

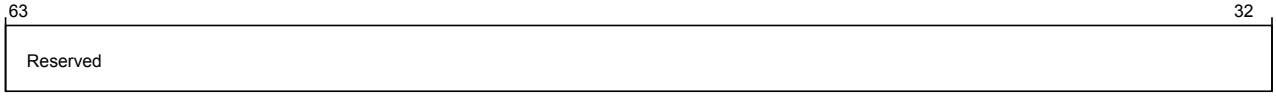


Figure 3-1144 por_cxg_ra_por_cxg_ra_cfg_ctl (high)

The following table shows the por_cxg_ra_cfg_ctl higher register bit assignments.

Table 3-1158 por_cxg_ra_por_cxg_ra_cfg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

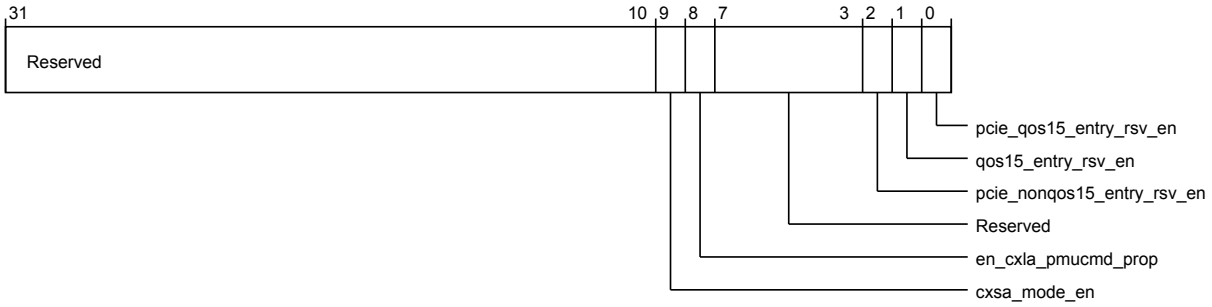


Figure 3-1145 por_cxg_ra_por_cxg_ra_cfg_ctl (low)

The following table shows the por_cxg_ra_cfg_ctl lower register bit assignments.

Table 3-1159 por_cxg_ra_por_cxg_ra_cfg_ctl (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9	cxsa_mode_en	When set, enables the CCIX Slave Agent mode.In this mode RA functions as a CCIX Slave Agent 1'b1: CCIX Slave Agent 1'b0: CCIX Requesting Agent	RW	1'b0
8	en_cxla_pmucmd_prop	When set, enables the propagation of PMU commands to CXLA NOTE: By default, CXLA PMU command propagation is disabled.	RW	1'b0
7:3	Reserved	Reserved	RO	-
2	pcie_nonqos15_entry_rsv_en	Enables entry reservation for non QoS15 traffic from PCIe RN-I/RN-D 1'b1: Reserves tracker entry for non QoS15 requests from PCIe RN-I/RN-D 1'b0: Does not reserve tracker entry for non QoS15 requests from PCIe RN-I/RN-D	RW	1'b0
1	qos15_entry_rsv_en	Enables entry reservation for QoS15 traffic 1'b1: Reserves tracker entry for QoS15 requests 1'b0: Does not reserve tracker entry for QoS15 requests	RW	1'b1
0	pcie_qos15_entry_rsv_en	Enables entry reservation for QoS15 traffic from PCIe RN-I/RN-D 1'b1: Reserves tracker entry for QoS15 requests from PCIe RN-I/RN-D 1'b0: Does not reserve tracker entry for QoS15 requests from PCIe RN-I/RN-D	RW	1'b0

por_cxg_ra_aux_ctl

Functions as the auxiliary control register for CXRA.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hA08

Register reset 17'h6

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

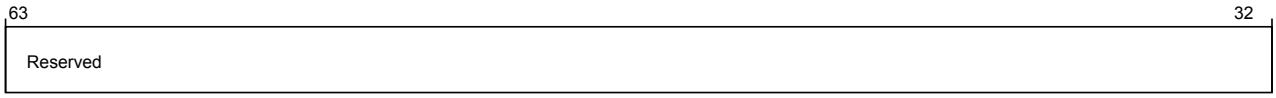


Figure 3-1146 por_cxg_ra_por_cxg_ra_aux_ctl (high)

The following table shows the por_cxg_ra_aux_ctl higher register bit assignments.

Table 3-1160 por_cxg_ra_por_cxg_ra_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

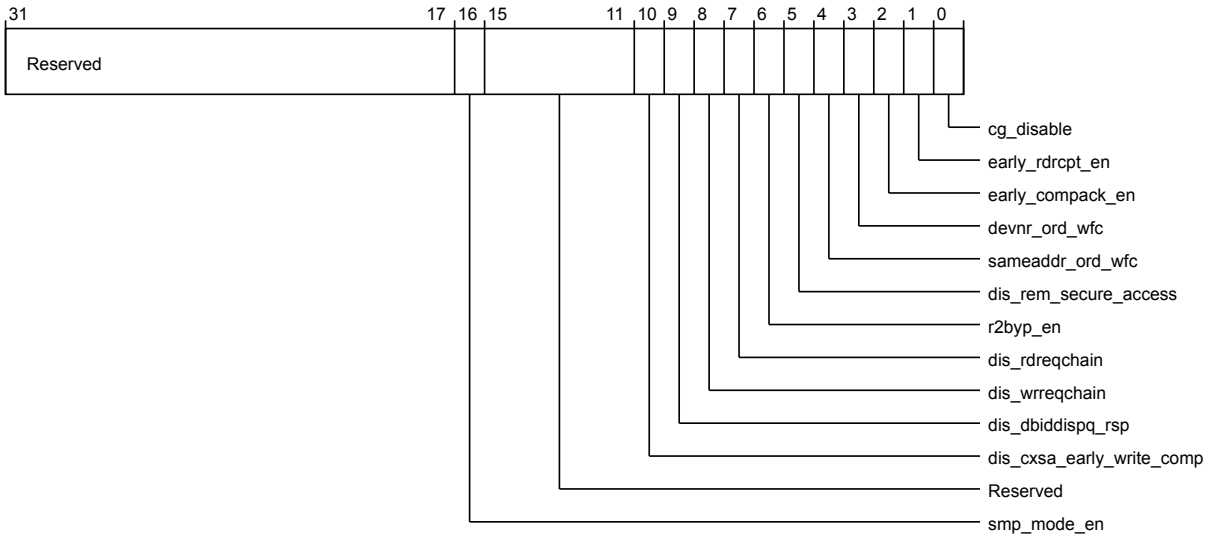


Figure 3-1147 por_cxg_ra_por_cxg_ra_aux_ctl (low)

The following table shows the por_cxg_ra_aux_ctl lower register bit assignments.

Table 3-1161 por_cxg_ra_por_cxg_ra_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31:17	Reserved	Reserved	RO	-
16	smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode.	RW	1'b0
15:11	Reserved	Reserved	RO	-
10	dis_cxsa_early_write_comp	When set, disables early write completions in CCIX Slave Agent mode.	RW	1'b0

Table 3-1161 por_cxg_ra_por_cxg_ra_aux_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
9	dis_dbiddispq_rsp	When set, disables the dispatch of DBID responses from a separate DispatchQ.	RW	1'b0
8	dis_wrreqchain	When set, disables chaining of write requests.	RW	1'b0
7	dis_rdreqchain	When set, disables chaining of read and dataless requests.	RW	1'b0
6	r2byp_en	When set, enables request bypass. Applies to read and dataless requests only. Note: When set will affect the capability to chain a request on the TX side	RW	1'b0
5	dis_rem_secure_access	When set, treats all the incoming snoops as non-secure and forces the NS bit to 1	RW	1'b0
4	sameaddr_ord_wfc	When set, enables waiting for completion (COMP) before dispatching next same Addr dependent transaction (TXN)	RW	1'b0
3	devnr_ord_wfc	When set, enables waiting for completion (COMP) before dispatching next Device-nR dependent transaction (TXN)	RW	1'b0
2	early_compack_en	Early CompAck enable; enables sending early CompAck on CCIX for requests that require CompAck	RW	1'b1
1	early_rdrcpt_en	Early ReadReceipt enable; enables sending early ReadReceipt for ordered read requests	RW	1'b1
0	cg_disable	Disables clock gating when set	RW	1'b0

por_cxg_ra_sam_addr_region_reg0

Configures Address Region 0 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

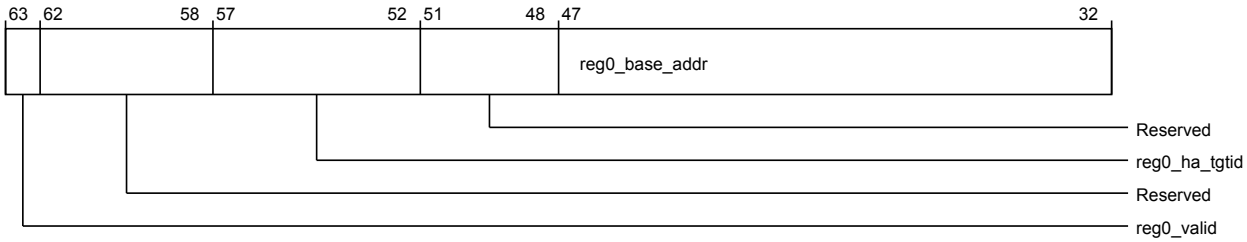


Figure 3-1148 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg0 higher register bit assignments.

Table 3-1162 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (high)

Bits	Field name	Description	Type	Reset
63	reg0_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg0_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg0_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

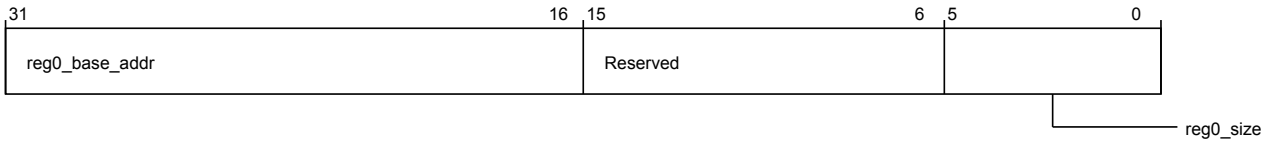


Figure 3-1149 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg0 lower register bit assignments.

Table 3-1163 por_cxg_ra_por_cxg_ra_sam_addr_region_reg0 (low)

Bits	Field name	Description	Type	Reset
31:16	reg0_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg0_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg1

Configures Address Region 1 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

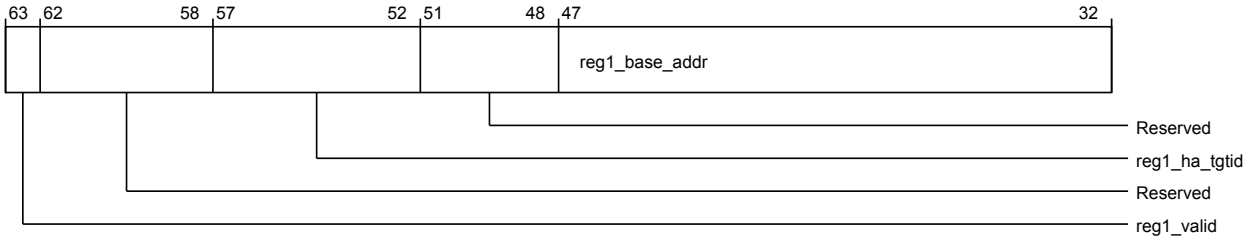


Figure 3-1150 por_cxg_ra_por_cxg_ra_sam_addr_region_reg1 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg1 higher register bit assignments.

Table 3-1164 por_cxg_ra_por_cxg_ra_sam_addr_region_reg1 (high)

Bits	Field name	Description	Type	Reset
63	reg1_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg1_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg1_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

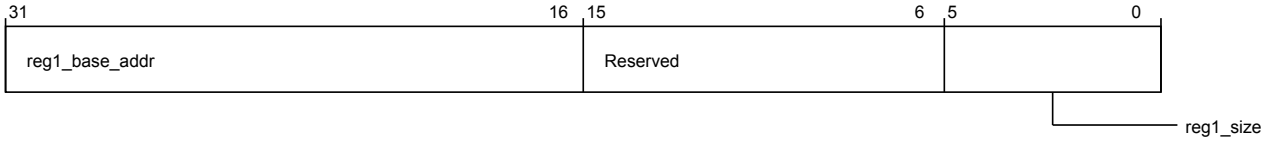


Figure 3-1151 por_cxg_ra_por_cxg_ra_sam_addr_region_reg1 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg1 lower register bit assignments.

Table 3-1165 por_cxg_ra_por_cxg_ra_sam_addr_region_reg1 (low)

Bits	Field name	Description	Type	Reset
31:16	reg1_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg1_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg2

Configures Address Region 2 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

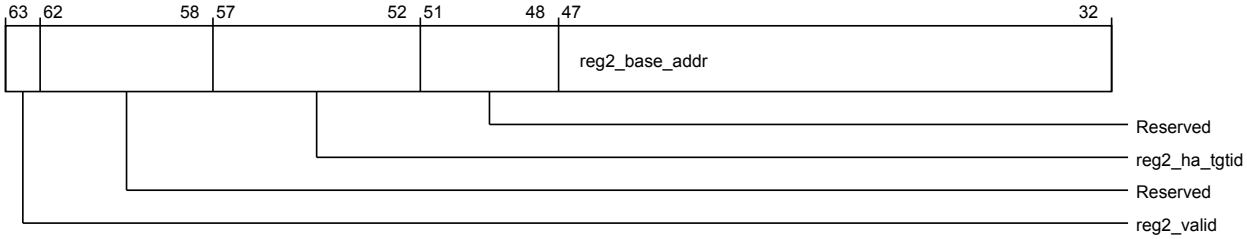


Figure 3-1152 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg2 higher register bit assignments.

Table 3-1166 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (high)

Bits	Field name	Description	Type	Reset
63	reg2_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg2_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg2_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

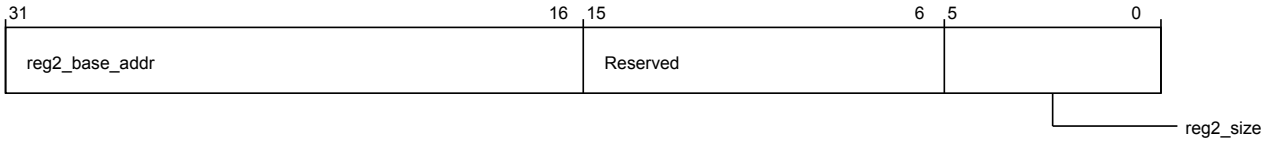


Figure 3-1153 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg2 lower register bit assignments.

Table 3-1167 por_cxg_ra_por_cxg_ra_sam_addr_region_reg2 (low)

Bits	Field name	Description	Type	Reset
31:16	reg2_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg2_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg3

Configures Address Region 3 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

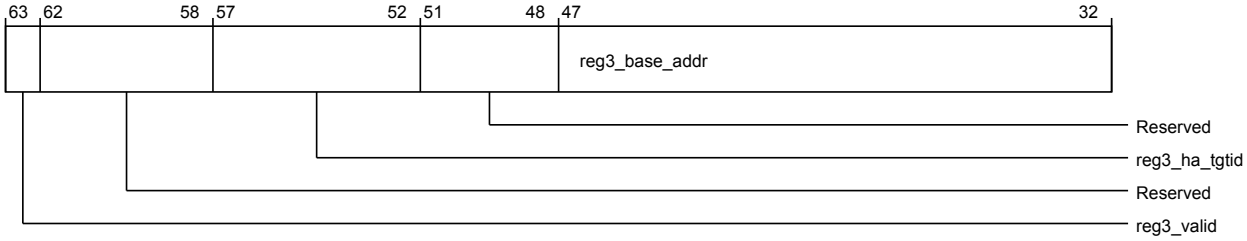


Figure 3-1154 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg3 higher register bit assignments.

Table 3-1168 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (high)

Bits	Field name	Description	Type	Reset
63	reg3_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg3_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg3_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

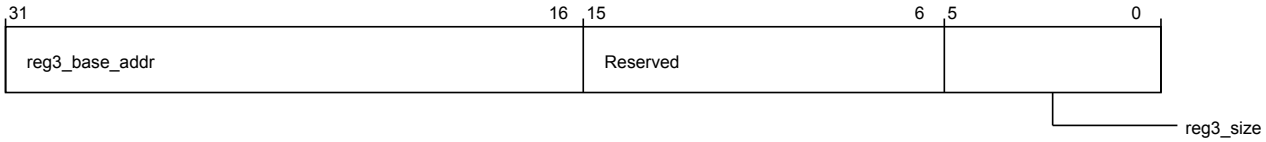


Figure 3-1155 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg3 lower register bit assignments.

Table 3-1169 por_cxg_ra_por_cxg_ra_sam_addr_region_reg3 (low)

Bits	Field name	Description	Type	Reset
31:16	reg3_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg3_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg4

Configures Address Region 4 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

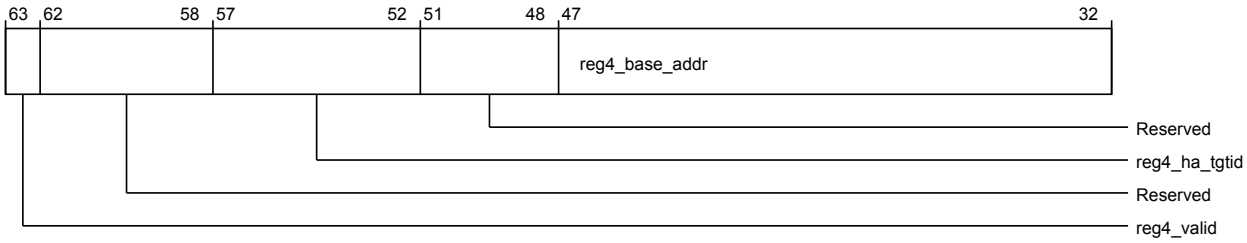


Figure 3-1156 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg4 higher register bit assignments.

Table 3-1170 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (high)

Bits	Field name	Description	Type	Reset
63	reg4_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg4_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg4_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

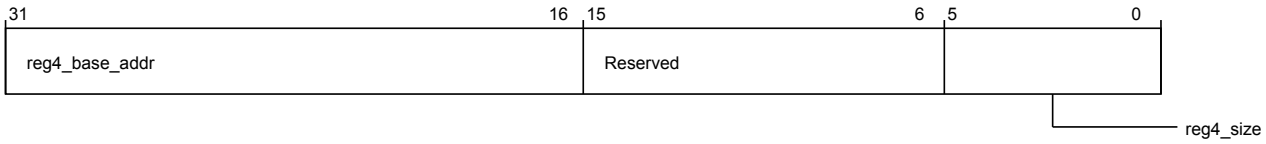


Figure 3-1157 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg4 lower register bit assignments.

Table 3-1171 por_cxg_ra_por_cxg_ra_sam_addr_region_reg4 (low)

Bits	Field name	Description	Type	Reset
31:16	reg4_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg4_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg5

Configures Address Region 5 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDD0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

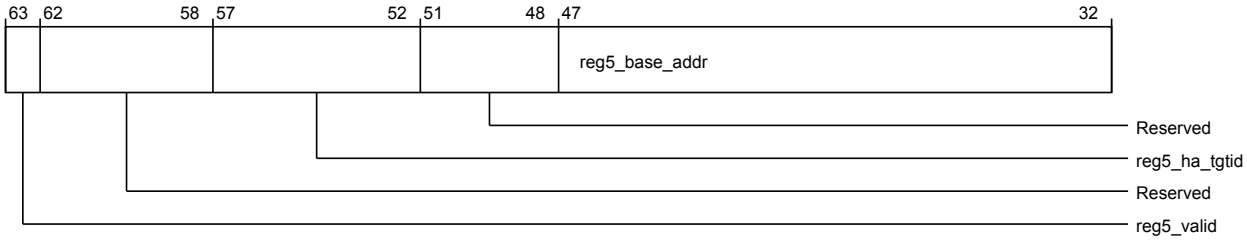


Figure 3-1158 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg5 higher register bit assignments.

Table 3-1172 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (high)

Bits	Field name	Description	Type	Reset
63	reg5_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg5_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg5_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

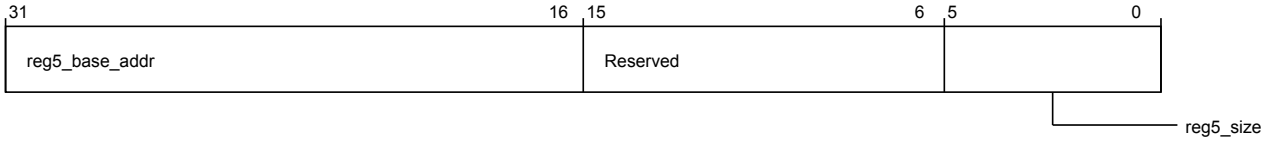


Figure 3-1159 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg5 lower register bit assignments.

Table 3-1173 por_cxg_ra_por_cxg_ra_sam_addr_region_reg5 (low)

Bits	Field name	Description	Type	Reset
31:16	reg5_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg5_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg6

Configures Address Region 6 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDD8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

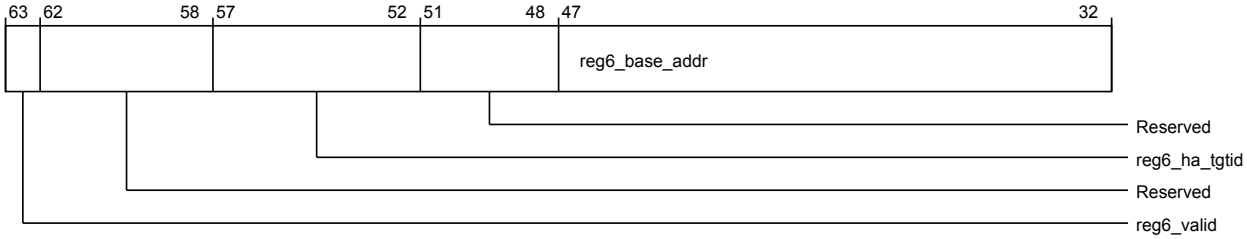


Figure 3-1160 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg6 higher register bit assignments.

Table 3-1174 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (high)

Bits	Field name	Description	Type	Reset
63	reg6_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg6_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg6_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

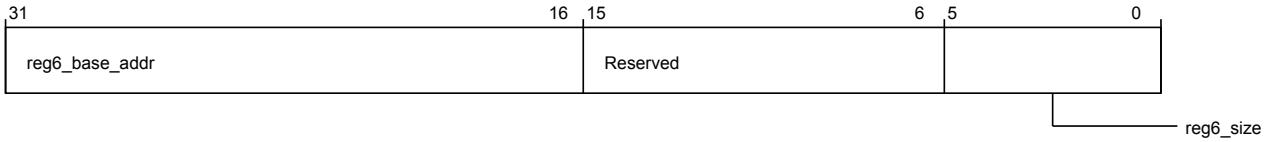


Figure 3-1161 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg6 lower register bit assignments.

Table 3-1175 por_cxg_ra_por_cxg_ra_sam_addr_region_reg6 (low)

Bits	Field name	Description	Type	Reset
31:16	reg6_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg6_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_addr_region_reg7

Configures Address Region 7 for RA SAM.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hDE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

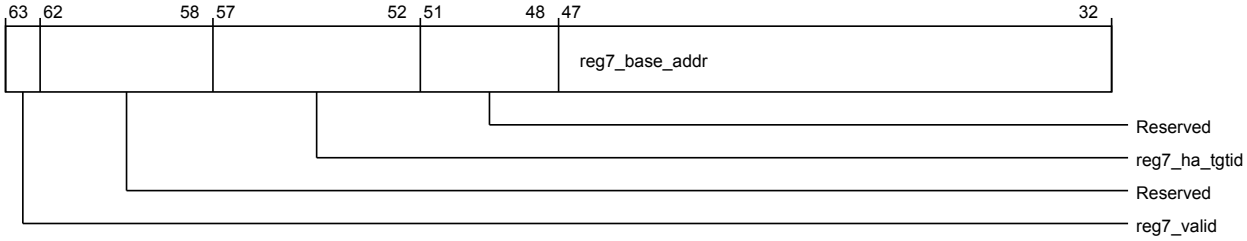


Figure 3-1162 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (high)

The following table shows the por_cxg_ra_sam_addr_region_reg7 higher register bit assignments.

Table 3-1176 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (high)

Bits	Field name	Description	Type	Reset
63	reg7_valid	Specifies if the memory region is valid	RW	1'b0
62:58	Reserved	Reserved	RO	-
57:52	reg7_ha_tgtid	Specifies the target HAID	RW	6'b0
51:48	Reserved	Reserved	RO	-
47:32	reg7_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0

The following image shows the lower register bit assignments.

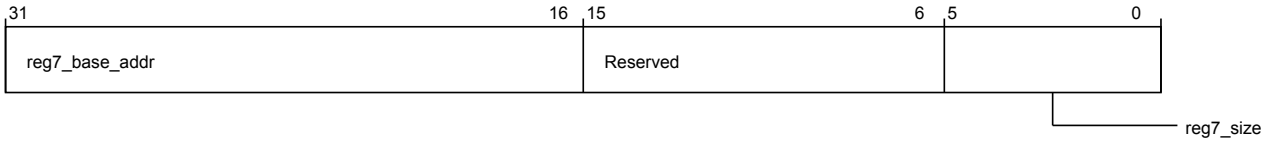


Figure 3-1163 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (low)

The following table shows the por_cxg_ra_sam_addr_region_reg7 lower register bit assignments.

Table 3-1177 por_cxg_ra_por_cxg_ra_sam_addr_region_reg7 (low)

Bits	Field name	Description	Type	Reset
31:16	reg7_base_addr	Specifies the 2^n-aligned base address for the memory region	RW	32'h0
15:6	Reserved	Reserved	RO	-
5:0	reg7_size	Specifies the size of the memory region	RW	1'b0

por_cxg_ra_sam_mem_region0_limit_reg

Specifies the memory region 0 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

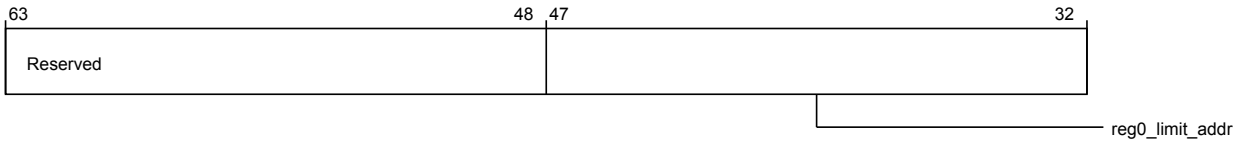


Figure 3-1164 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region0_limit_reg higher register bit assignments.

Table 3-1178 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg0_limit_addr	Memory region 0 limit address	RW	32'h0

The following image shows the lower register bit assignments.

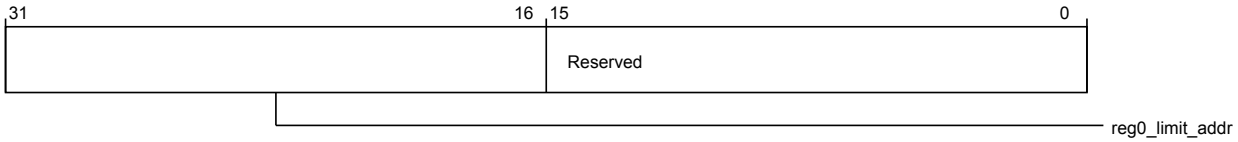


Figure 3-1165 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region0_limit_reg lower register bit assignments.

Table 3-1179 por_cxg_ra_por_cxg_ra_sam_mem_region0_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg0_limit_addr	Memory region 0 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region1_limit_reg

Specifies the memory region 1 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

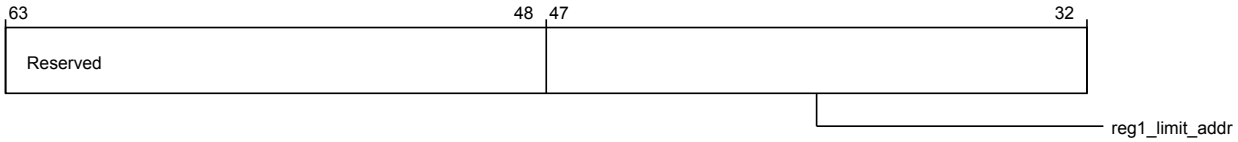


Figure 3-1166 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region1_limit_reg higher register bit assignments.

Table 3-1180 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg1_limit_addr	Memory region 1 limit address	RW	32'h0

The following image shows the lower register bit assignments.

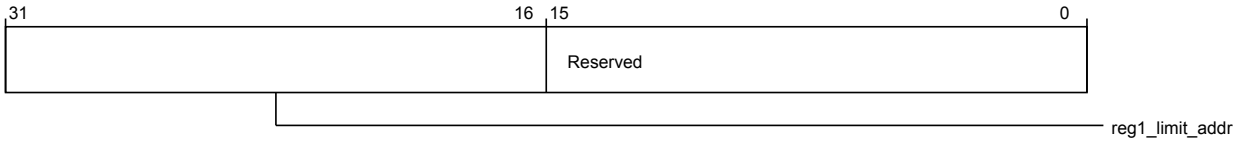


Figure 3-1167 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region1_limit_reg lower register bit assignments.

Table 3-1181 por_cxg_ra_por_cxg_ra_sam_mem_region1_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg1_limit_addr	Memory region 1 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region2_limit_reg

Specifies the memory region 2 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

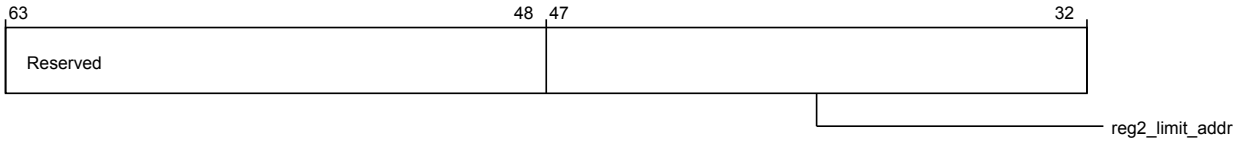


Figure 3-1168 por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region2_limit_reg higher register bit assignments.

Table 3-1182 por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg2_limit_addr	Memory region 2 limit address	RW	32'h0

The following image shows the lower register bit assignments.

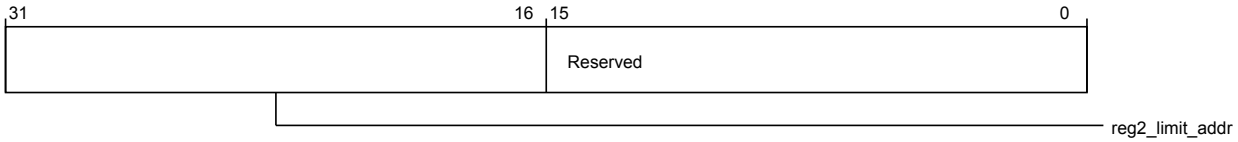


Figure 3-1169 por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region2_limit_reg lower register bit assignments.

Table 3-1183 por_cxg_ra_por_cxg_ra_sam_mem_region2_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg2_limit_addr	Memory region 2 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region3_limit_reg

Specifies the memory region 3 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

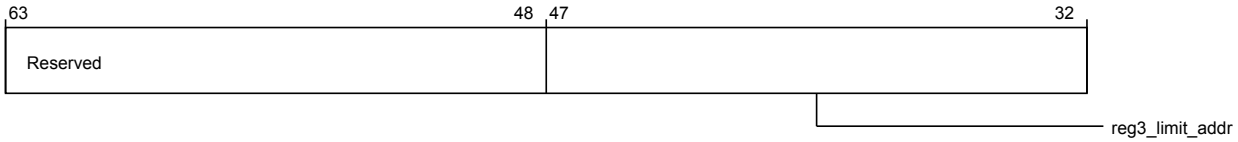


Figure 3-1170 por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region3_limit_reg higher register bit assignments.

Table 3-1184 por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg3_limit_addr	Memory region 3 limit address	RW	32'h0

The following image shows the lower register bit assignments.

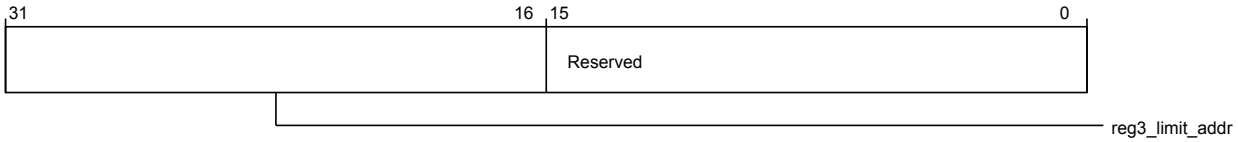


Figure 3-1171 por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region3_limit_reg lower register bit assignments.

Table 3-1185 por_cxg_ra_por_cxg_ra_sam_mem_region3_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg3_limit_addr	Memory region 3 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region4_limit_reg

Specifies the memory region 4 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

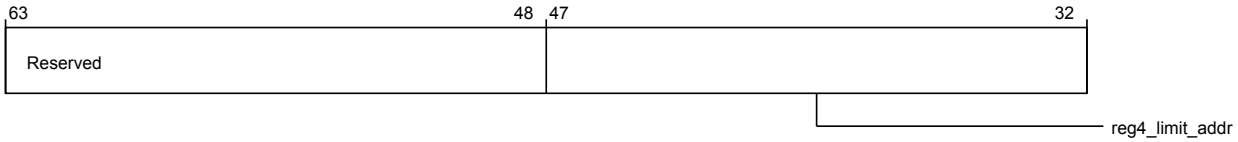


Figure 3-1172 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region4_limit_reg higher register bit assignments.

Table 3-1186 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg4_limit_addr	Memory region 4 limit address	RW	32'h0

The following image shows the lower register bit assignments.

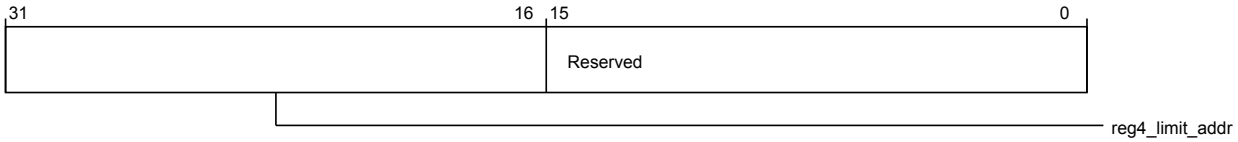


Figure 3-1173 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region4_limit_reg lower register bit assignments.

Table 3-1187 por_cxg_ra_por_cxg_ra_sam_mem_region4_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg4_limit_addr	Memory region 4 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region5_limit_reg

Specifies the memory region 5 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

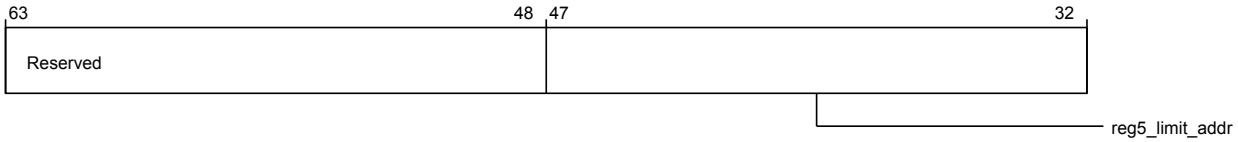


Figure 3-1174 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region5_limit_reg higher register bit assignments.

Table 3-1188 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg5_limit_addr	Memory region 5 limit address	RW	32'h0

The following image shows the lower register bit assignments.

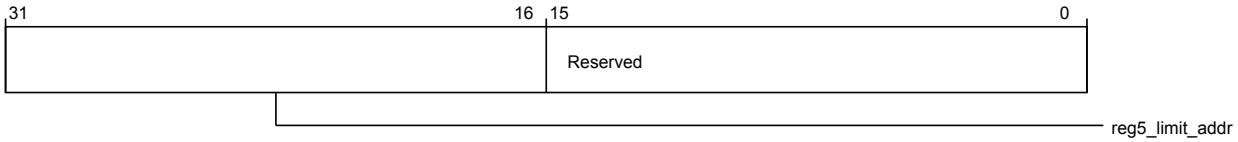


Figure 3-1175 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region5_limit_reg lower register bit assignments.

Table 3-1189 por_cxg_ra_por_cxg_ra_sam_mem_region5_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg5_limit_addr	Memory region 5 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region6_limit_reg

Specifies the memory region 6 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

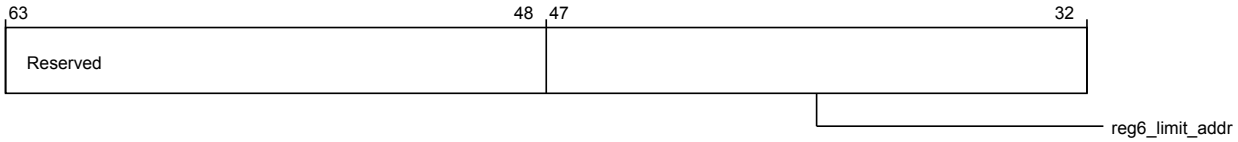


Figure 3-1176 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region6_limit_reg higher register bit assignments.

Table 3-1190 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg6_limit_addr	Memory region 6 limit address	RW	32'h0

The following image shows the lower register bit assignments.

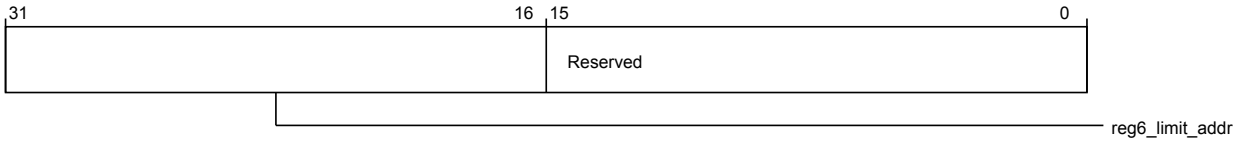


Figure 3-1177 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region6_limit_reg lower register bit assignments.

Table 3-1191 por_cxg_ra_por_cxg_ra_sam_mem_region6_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg6_limit_addr	Memory region 6 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_sam_mem_region7_limit_reg

Specifies the memory region 7 limit address.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.rasam_ctl

The following image shows the higher register bit assignments.

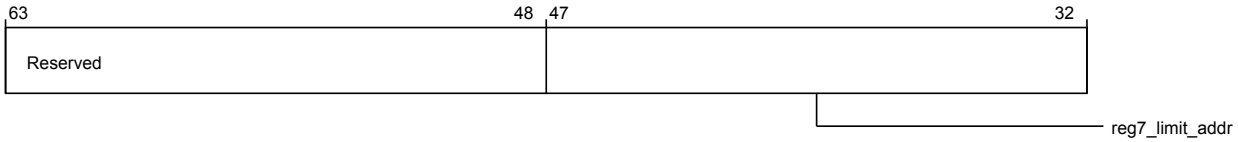


Figure 3-1178 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (high)

The following table shows the por_cxg_ra_sam_mem_region7_limit_reg higher register bit assignments.

Table 3-1192 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	reg7_limit_addr	Memory region 7 limit address	RW	32'h0

The following image shows the lower register bit assignments.

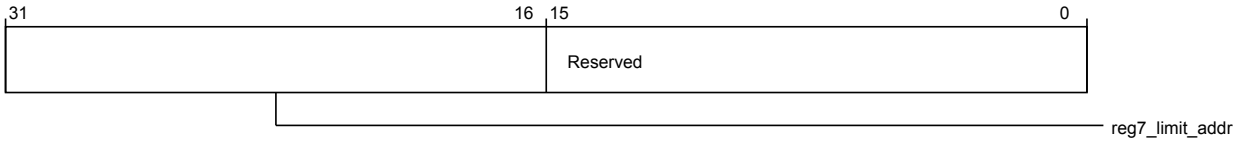


Figure 3-1179 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (low)

The following table shows the por_cxg_ra_sam_mem_region7_limit_reg lower register bit assignments.

Table 3-1193 por_cxg_ra_por_cxg_ra_sam_mem_region7_limit_reg (low)

Bits	Field name	Description	Type	Reset
31:16	reg7_limit_addr	Memory region 7 limit address	RW	32'h0
15:0	Reserved	Reserved	RO	-

por_cxg_ra_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

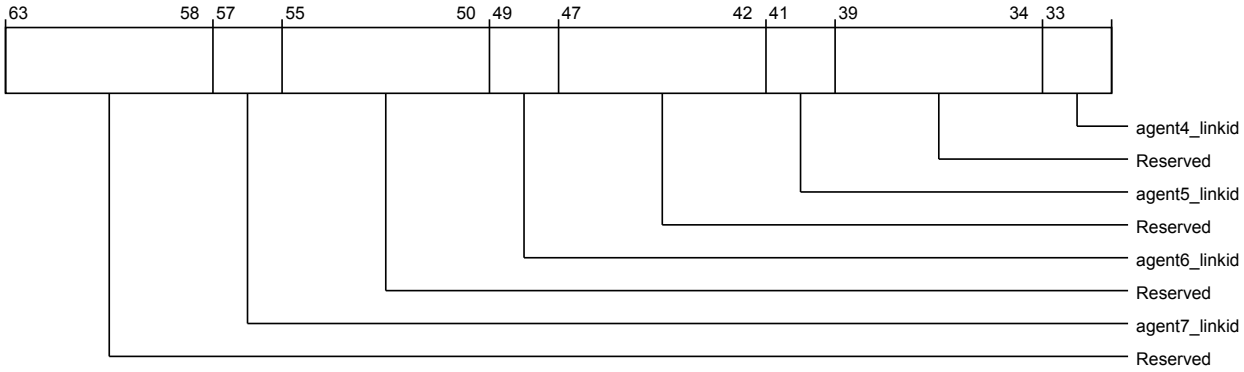


Figure 3-1180 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg0 higher register bit assignments.

Table 3-1194 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies the Link ID for Agent ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies the Link ID for Agent ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies the Link ID for Agent ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies the Link ID for Agent ID 4	RW	2'h0

The following image shows the lower register bit assignments.

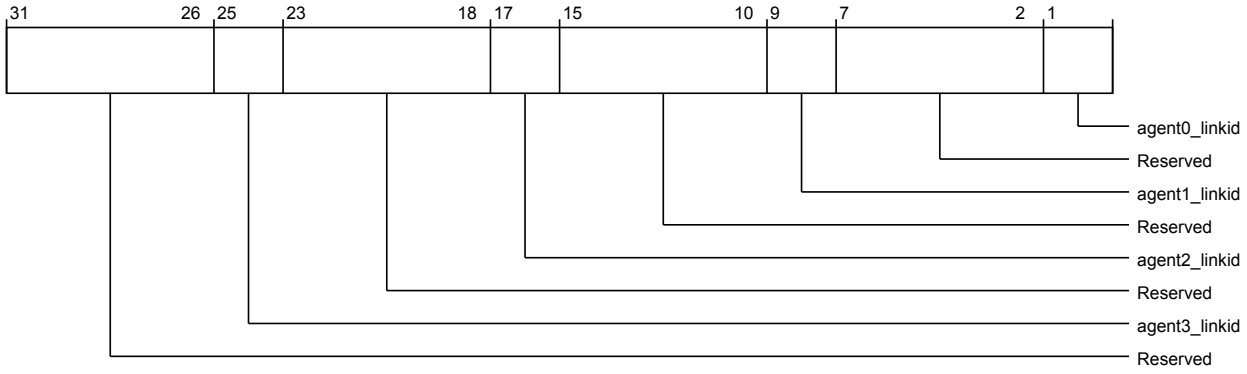


Figure 3-1181 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg0 lower register bit assignments.

Table 3-1195 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies the Link ID for Agent ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies the Link ID for Agent ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies the Link ID for Agent ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies the Link ID for Agent ID 0	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

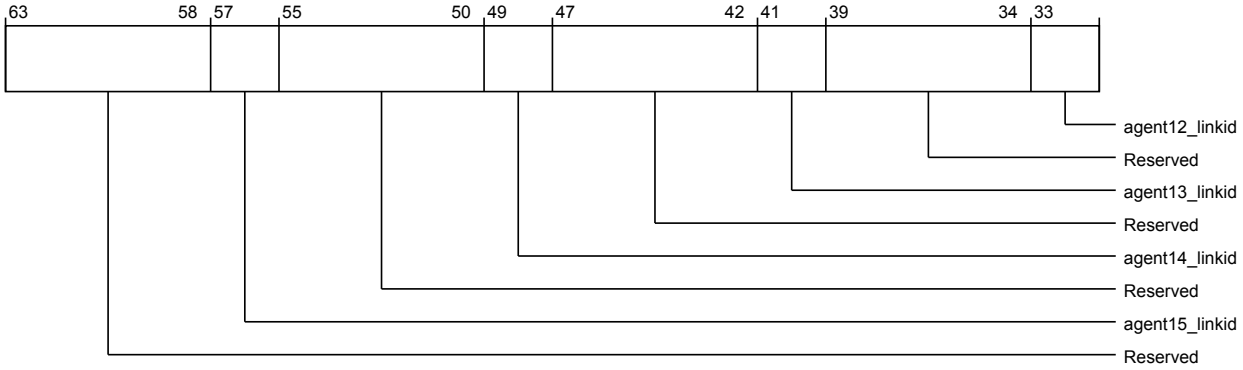


Figure 3-1182 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg1 higher register bit assignments.

Table 3-1196 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies the Link ID for Agent ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies the Link ID for Agent ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies the Link ID for Agent ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies the Link ID for Agent ID 12	RW	2'h0

The following image shows the lower register bit assignments.

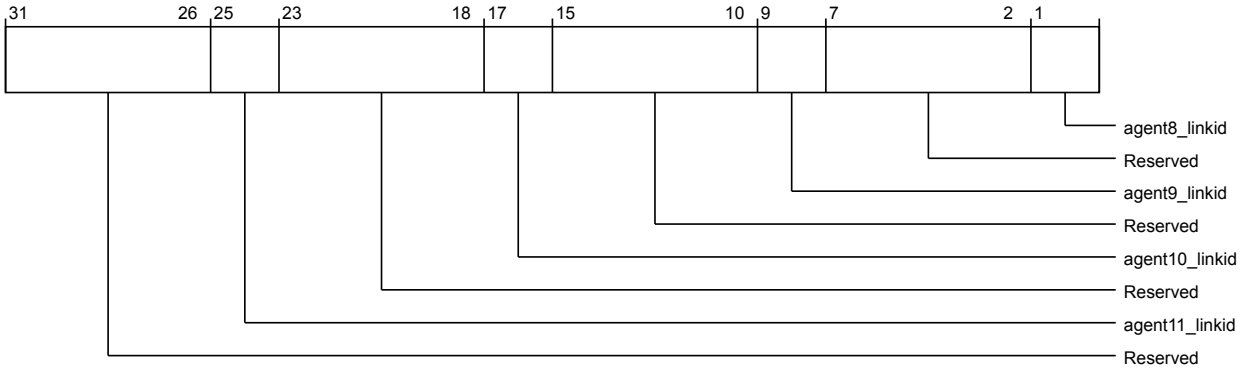


Figure 3-1183 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg1 lower register bit assignments.

Table 3-1197 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies the Link ID for Agent ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies the Link ID for Agent ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies the Link ID for Agent ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies the Link ID for Agent ID 8	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg2

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

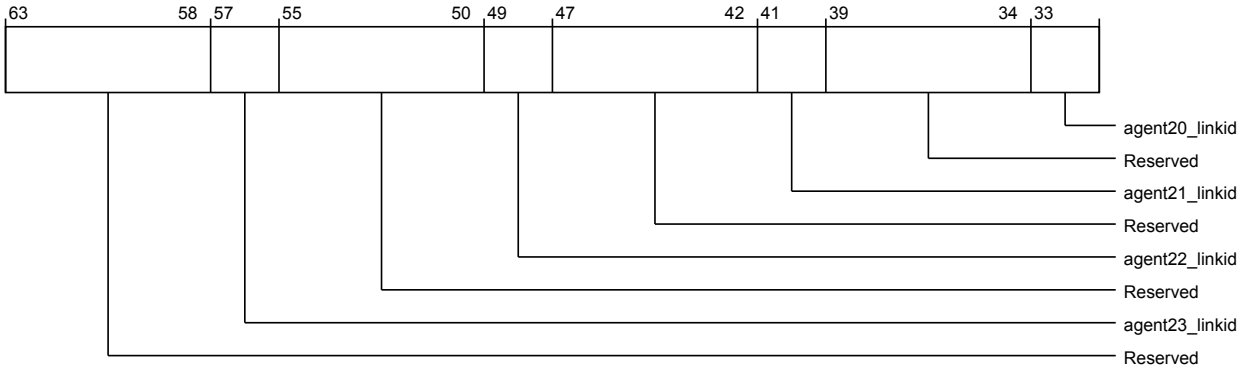


Figure 3-1184 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg2 higher register bit assignments.

Table 3-1198 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies the Link ID for Agent ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies the Link ID for Agent ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies the Link ID for Agent ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies the Link ID for Agent ID 20	RW	2'h0

The following image shows the lower register bit assignments.

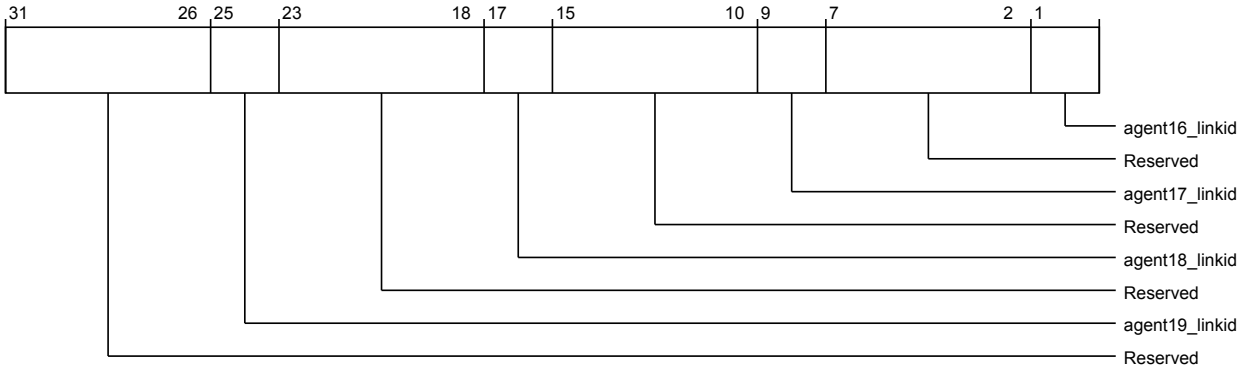


Figure 3-1185 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg2 lower register bit assignments.

Table 3-1199 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies the Link ID for Agent ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies the Link ID for Agent ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies the Link ID for Agent ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies the Link ID for Agent ID 16	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE78

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

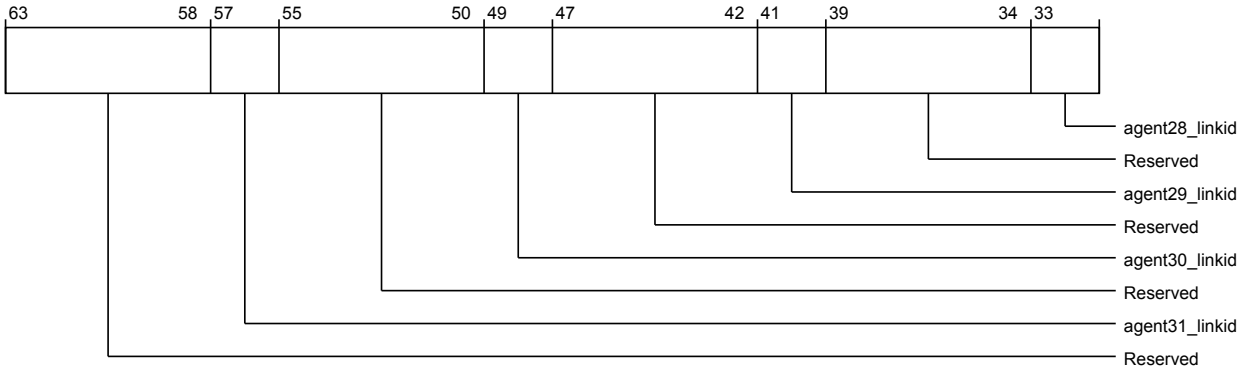


Figure 3-1186 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg3 higher register bit assignments.

Table 3-1200 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies the Link ID for Agent ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies the Link ID for Agent ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies the Link ID for Agent ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies the Link ID for Agent ID 28	RW	2'h0

The following image shows the lower register bit assignments.

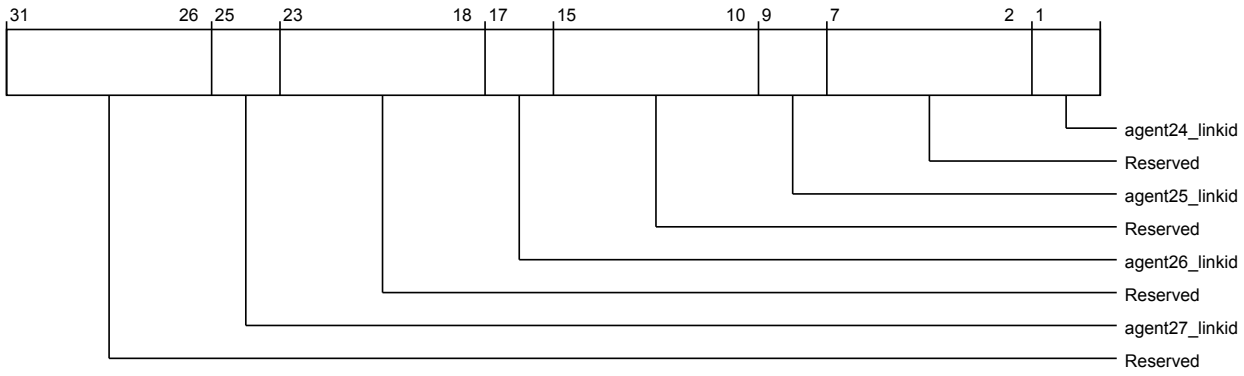


Figure 3-1187 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg3 lower register bit assignments.

Table 3-1201 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies the Link ID for Agent ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies the Link ID for Agent ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies the Link ID for Agent ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies the Link ID for Agent ID 24	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE80

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

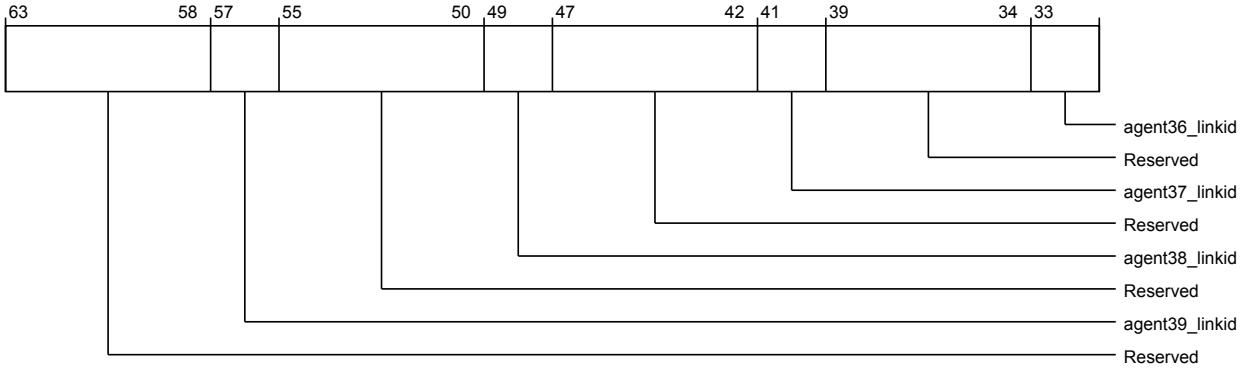


Figure 3-1188 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg4 higher register bit assignments.

Table 3-1202 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies the Link ID for Agent ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies the Link ID for Agent ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies the Link ID for Agent ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies the Link ID for Agent ID 36	RW	2'h0

The following image shows the lower register bit assignments.

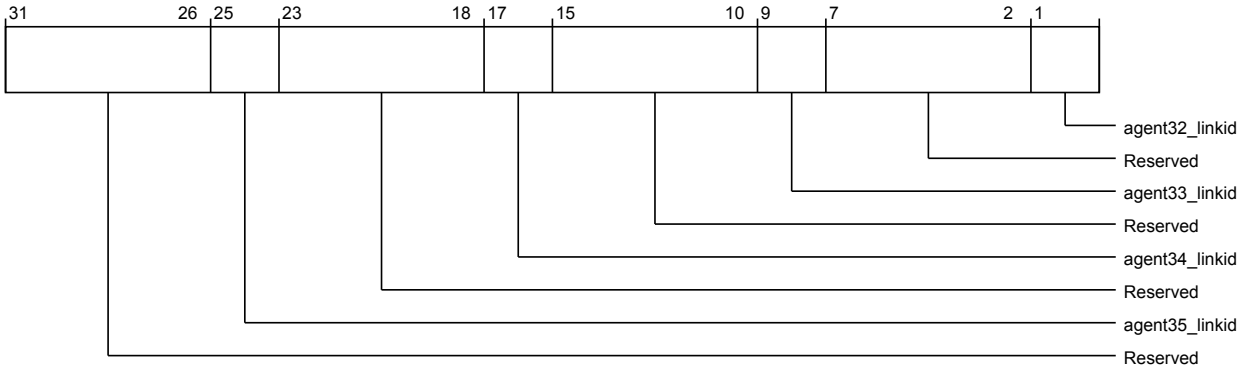


Figure 3-1189 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg4 lower register bit assignments.

Table 3-1203 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies the Link ID for Agent ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies the Link ID for Agent ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies the Link ID for Agent ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies the Link ID for Agent ID 32	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg5

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE88

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

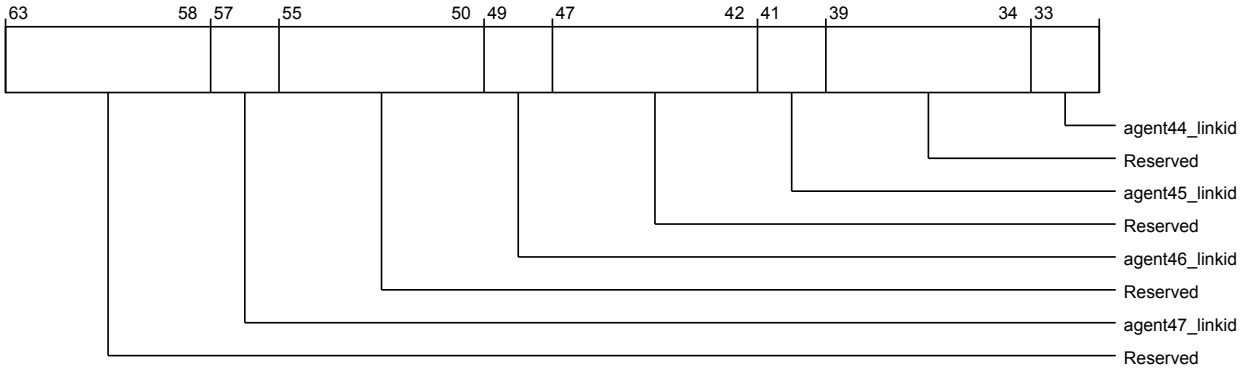


Figure 3-1190 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg5 higher register bit assignments.

Table 3-1204 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies the Link ID for Agent ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies the Link ID for Agent ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies the Link ID for Agent ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies the Link ID for Agent ID 44	RW	2'h0

The following image shows the lower register bit assignments.

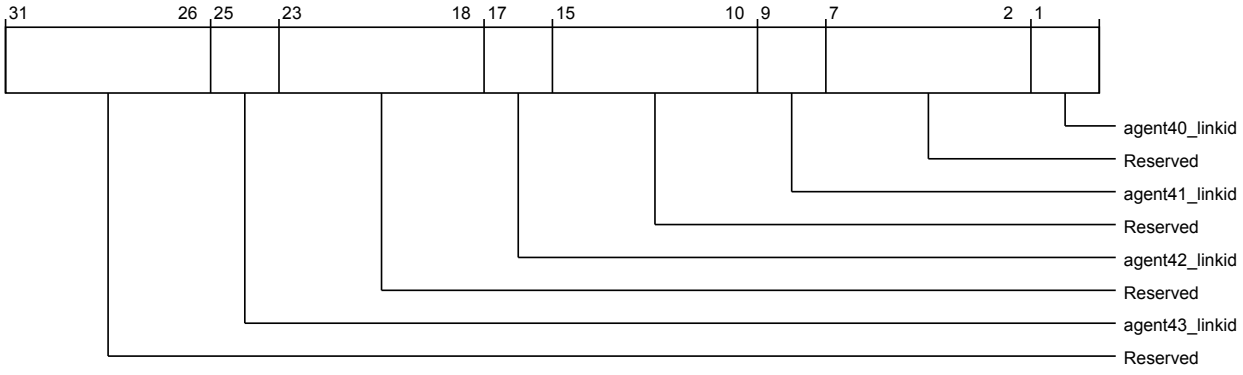


Figure 3-1191 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg5 lower register bit assignments.

Table 3-1205 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies the Link ID for Agent ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies the Link ID for Agent ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies the Link ID for Agent ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies the Link ID for Agent ID 40	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE90

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

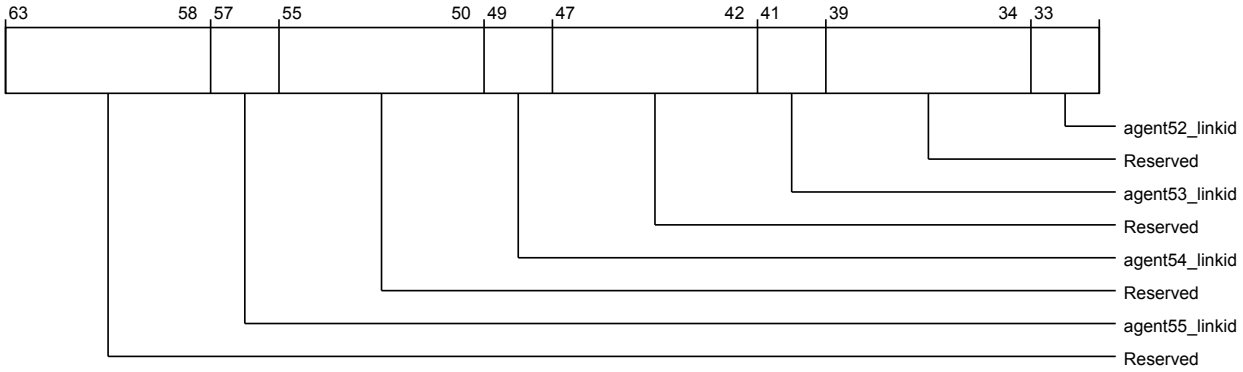


Figure 3-1192 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg6 higher register bit assignments.

Table 3-1206 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies the Link ID for Agent ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies the Link ID for Agent ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies the Link ID for Agent ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies the Link ID for Agent ID 52	RW	2'h0

The following image shows the lower register bit assignments.

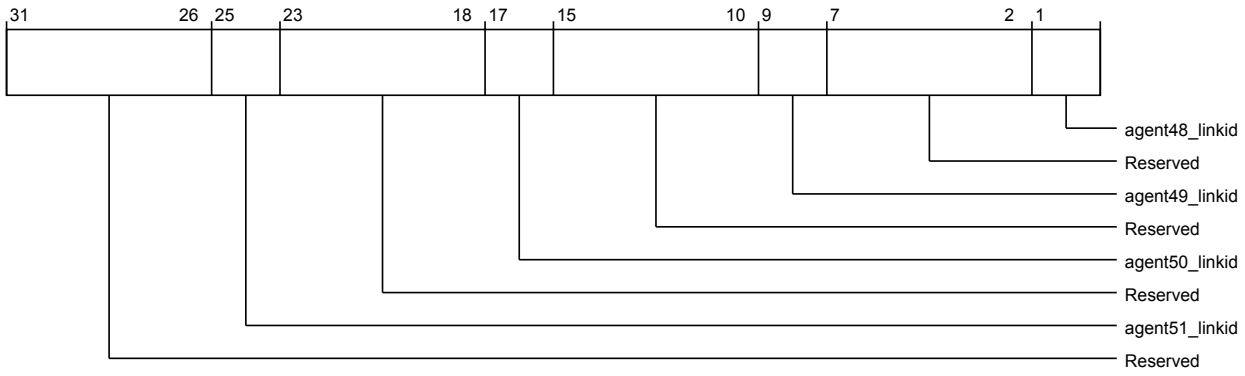


Figure 3-1193 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg6 lower register bit assignments.

Table 3-1207 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies the Link ID for Agent ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies the Link ID for Agent ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies the Link ID for Agent ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies the Link ID for Agent ID 48	RW	2'h0

por_cxg_ra_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hE98

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

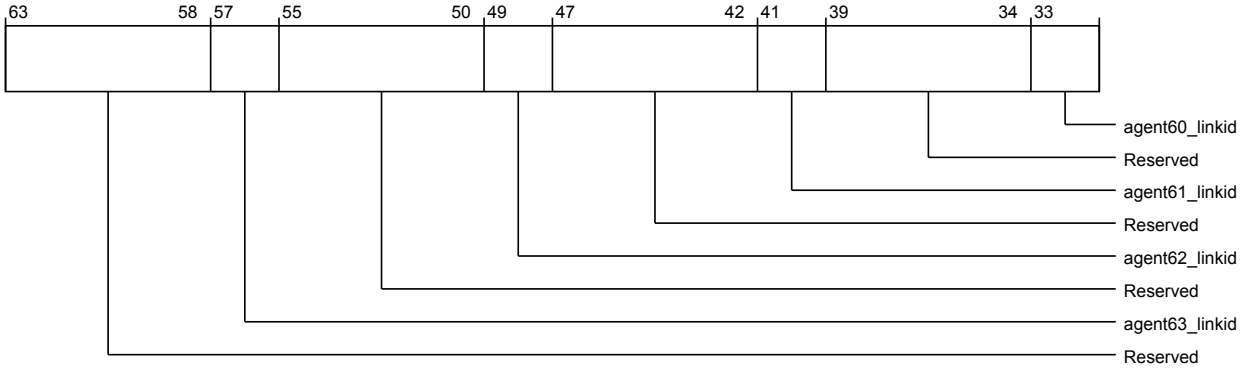


Figure 3-1194 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7 (high)

The following table shows the por_cxg_ra_agentid_to_linkid_reg7 higher register bit assignments.

Table 3-1208 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies the Link ID for Agent ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies the Link ID for Agent ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies the Link ID for Agent ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies the Link ID for Agent ID 60	RW	2'h0

The following image shows the lower register bit assignments.

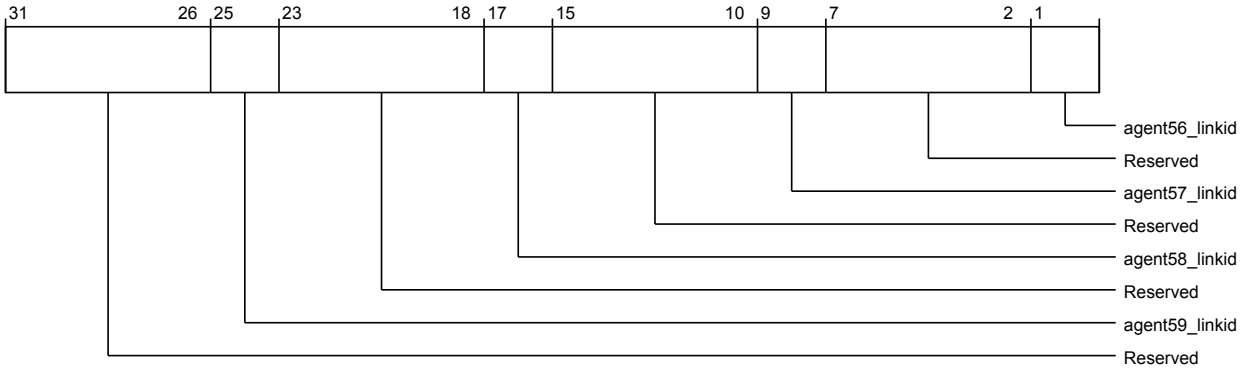


Figure 3-1195 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7 (low)

The following table shows the por_cxg_ra_agentid_to_linkid_reg7 lower register bit assignments.

Table 3-1209 por_cxg_ra_por_cxg_ra_agentid_to_linkid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies the Link ID for Agent ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies the Link ID for Agent ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies the Link ID for Agent ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies the Link ID for Agent ID 56	RW	2'h0

por_cxg_ra_rnf_ldid_to_raid_reg0

Specifies the mapping of RN-F LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEA0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

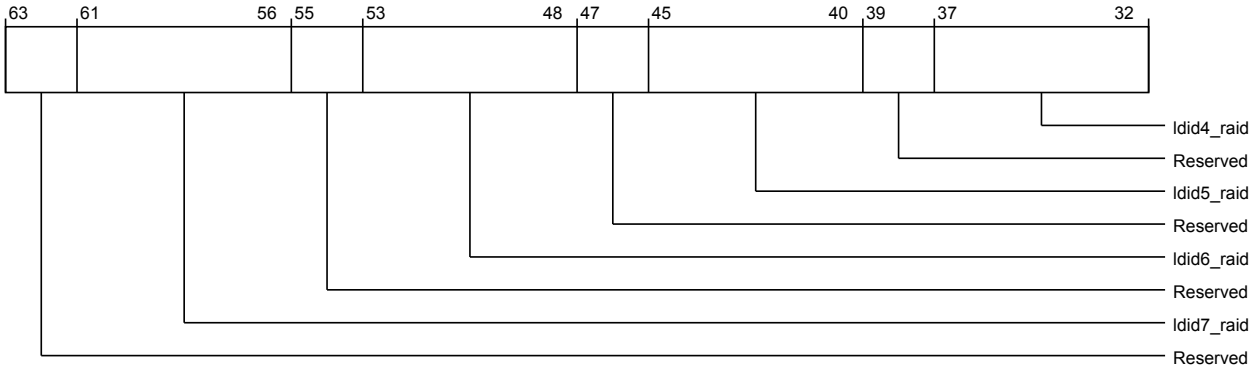


Figure 3-1196 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg0 higher register bit assignments.

Table 3-1210 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid7_raid	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid6_raid	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid5_raid	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid4_raid	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

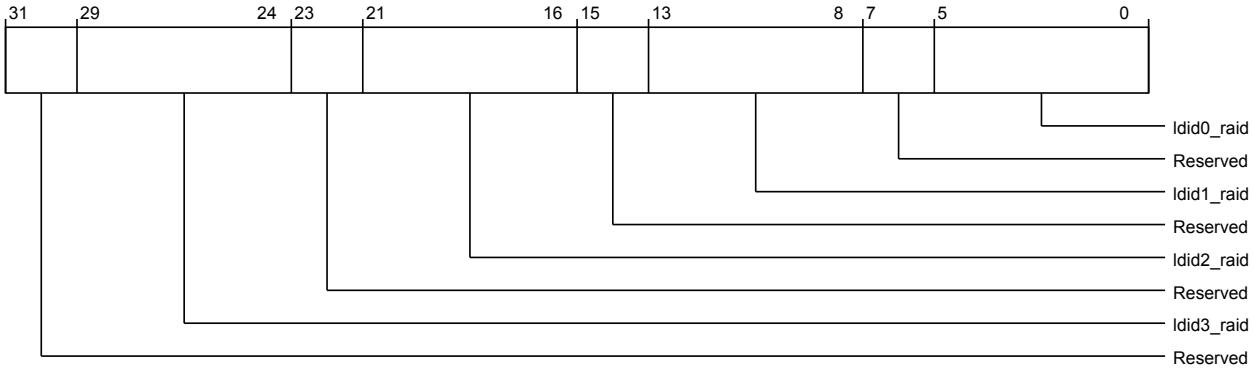


Figure 3-1197 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg0 lower register bit assignments.

Table 3-1211 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid3_raid	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid2_raid	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid1_raid	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid0_raid	Specifies the RAID for LDID 0	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg1

Specifies the mapping of RN-F LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEA8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

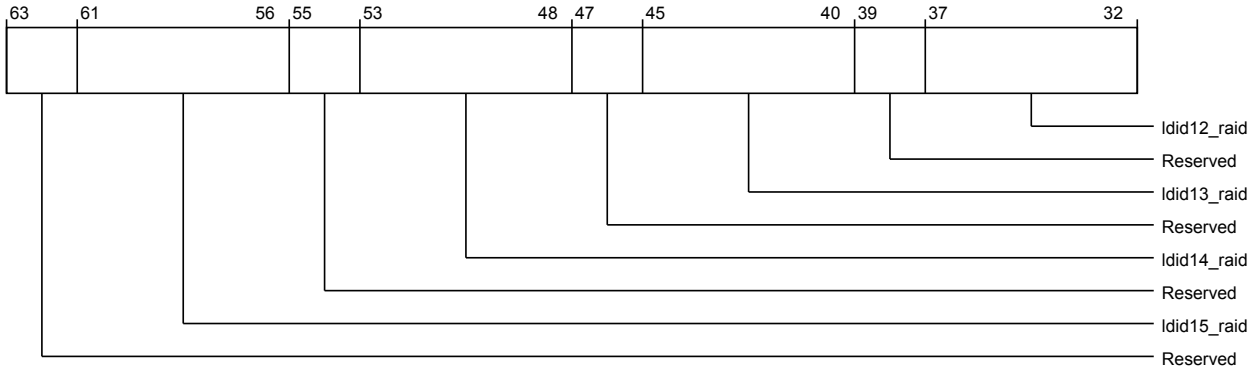


Figure 3-1198 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg1 higher register bit assignments.

Table 3-1212 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

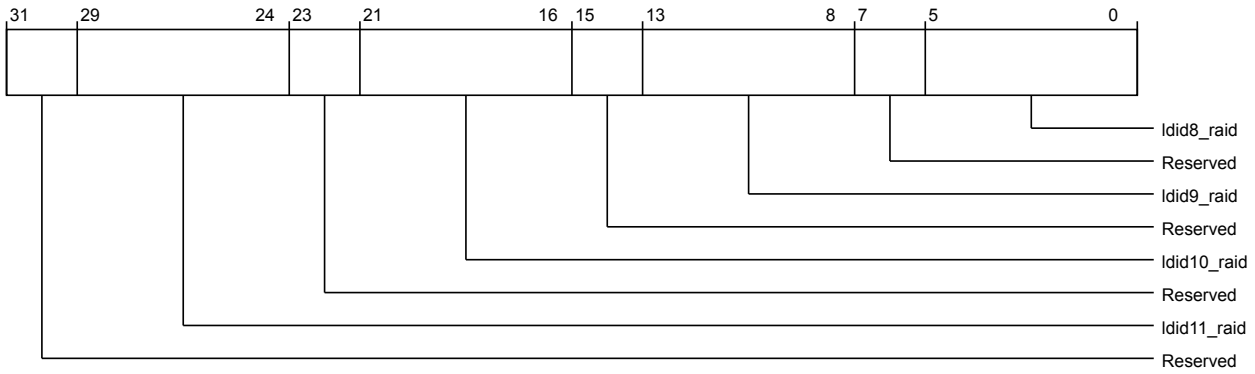


Figure 3-1199 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg1 lower register bit assignments.

Table 3-1213 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid11_raid	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid10_raid	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid9_raid	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid8_raid	Specifies the RAID for LDID 8	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg2

Specifies the mapping of RN-F LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

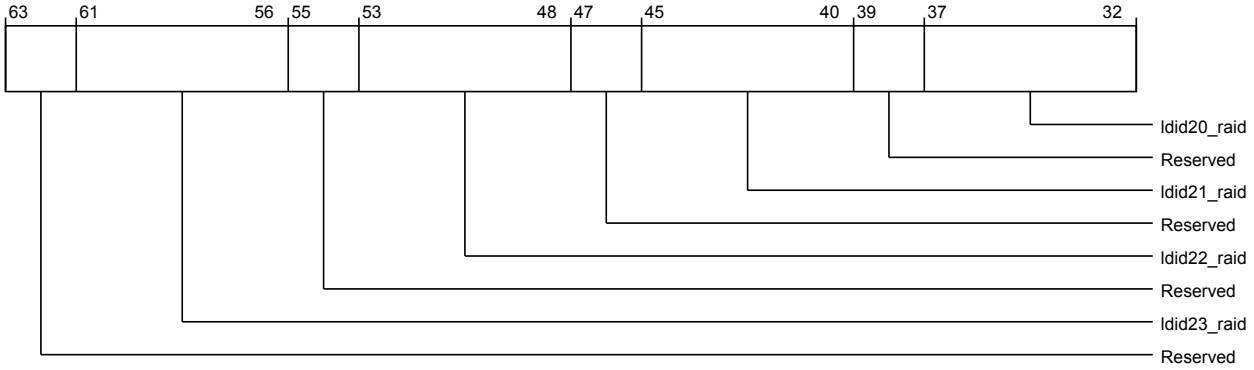


Figure 3-1200 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg2 higher register bit assignments.

Table 3-1214 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid23_raid	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid22_raid	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid21_raid	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid20_raid	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

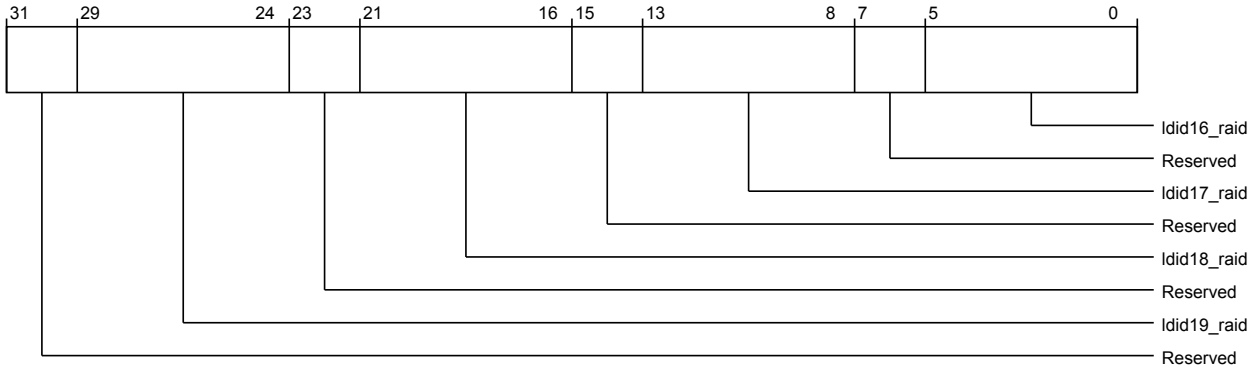


Figure 3-1201 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg2 lower register bit assignments.

Table 3-1215 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid19_raid	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid18_raid	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid17_raid	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid16_raid	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg3

Specifies the mapping of RN-F LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEB8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

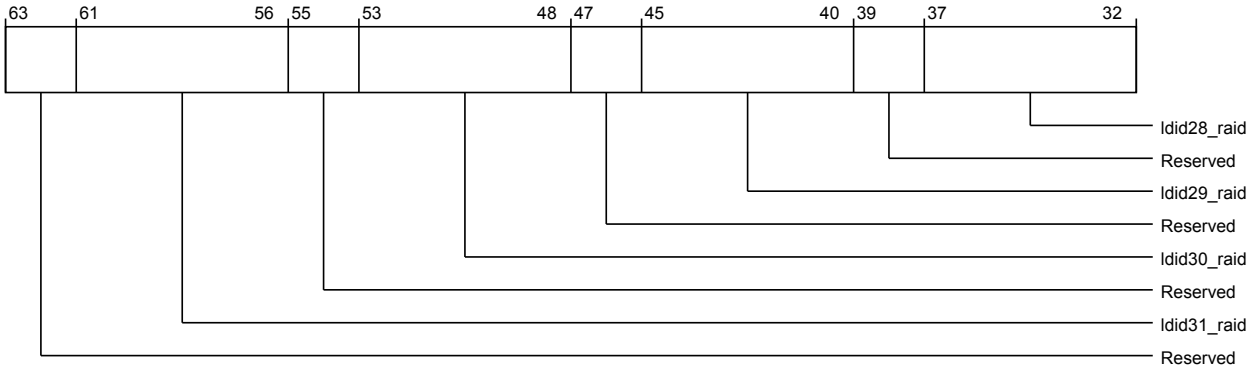


Figure 3-1202 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg3 higher register bit assignments.

Table 3-1216 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid31_raid	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid30_raid	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid29_raid	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid28_raid	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

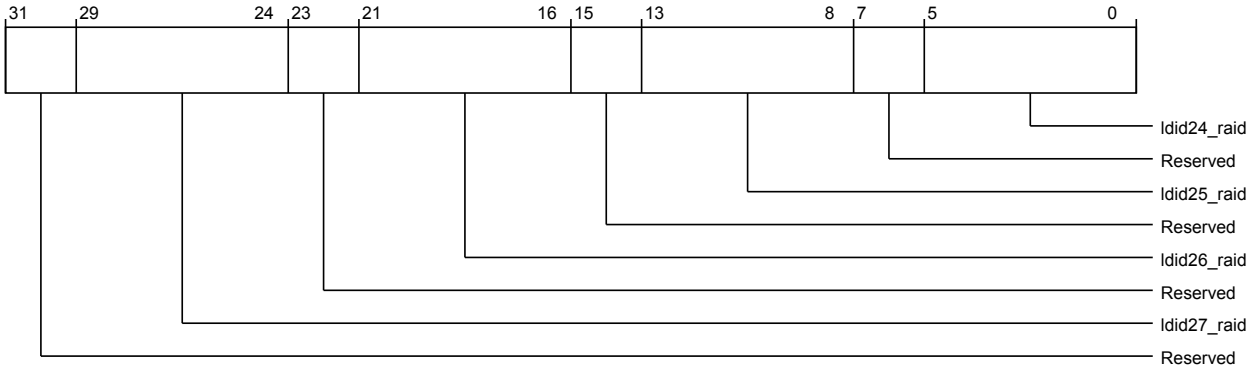


Figure 3-1203 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg3 lower register bit assignments.

Table 3-1217 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid27_raid	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid26_raid	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid25_raid	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid24_raid	Specifies the RAID for LDID 24	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg4

Specifies the mapping of RN-F LDID to RAID for LDIDs 32 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

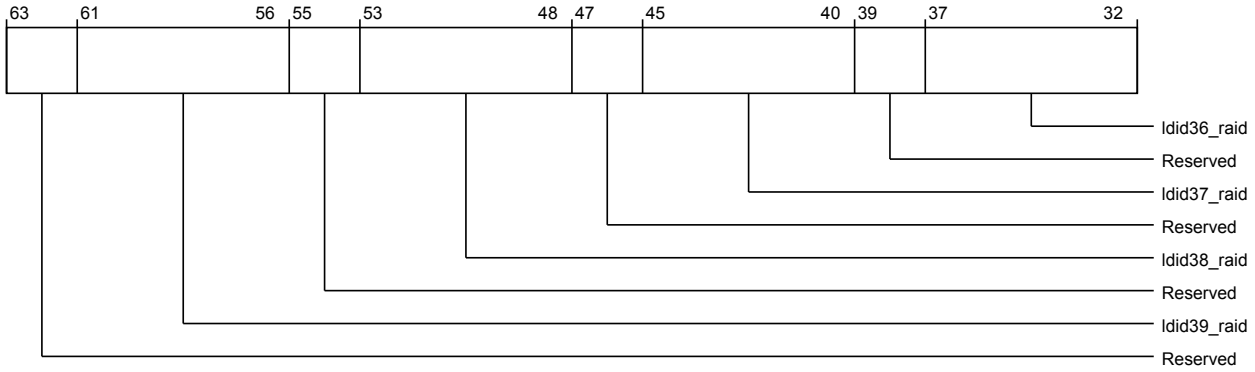


Figure 3-1204 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg4 higher register bit assignments.

Table 3-1218 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid39_raid	Specifies the RAID for LDID 39	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid38_raid	Specifies the RAID for LDID 38	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid37_raid	Specifies the RAID for LDID 37	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid36_raid	Specifies the RAID for LDID 36	RW	6'h0

The following image shows the lower register bit assignments.

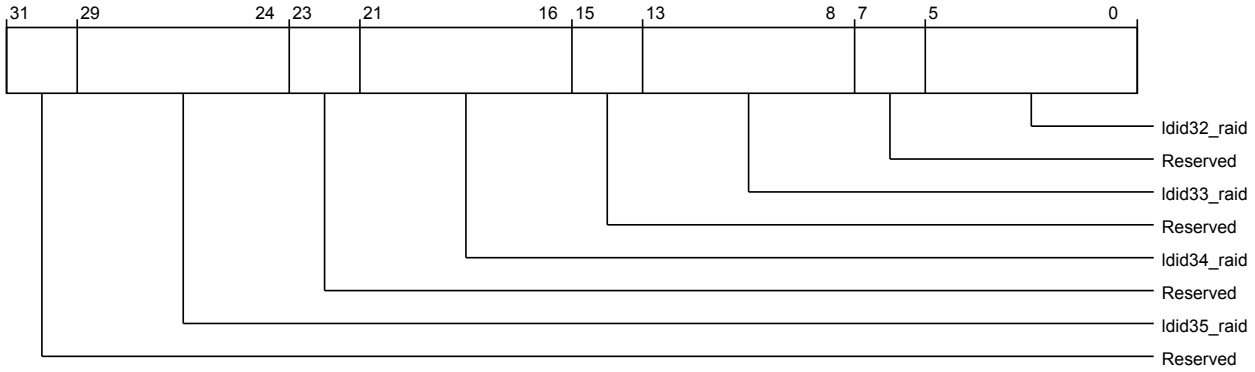


Figure 3-1205 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg4 lower register bit assignments.

Table 3-1219 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid35_raid	Specifies the RAID for LDID 35	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid34_raid	Specifies the RAID for LDID 34	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid33_raid	Specifies the RAID for LDID 33	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid32_raid	Specifies the RAID for LDID 32	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg5

Specifies the mapping of RN-F LDID to RAID for LDIDs 40 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEC8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

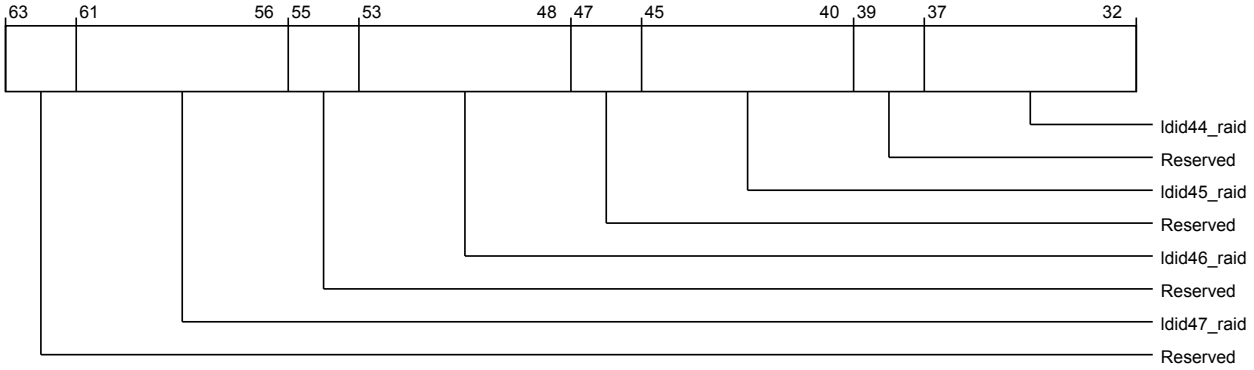


Figure 3-1206 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg5 higher register bit assignments.

Table 3-1220 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid47_raid	Specifies the RAID for LDID 47	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid46_raid	Specifies the RAID for LDID 46	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid45_raid	Specifies the RAID for LDID 45	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid44_raid	Specifies the RAID for LDID 44	RW	6'h0

The following image shows the lower register bit assignments.

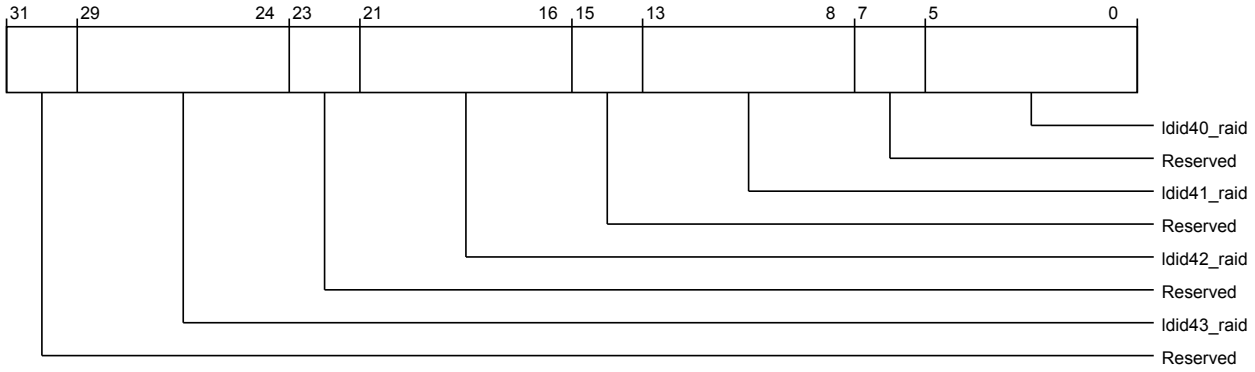


Figure 3-1207 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg5 lower register bit assignments.

Table 3-1221 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid43_raid	Specifies the RAID for LDID 43	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid42_raid	Specifies the RAID for LDID 42	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid41_raid	Specifies the RAID for LDID 41	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid40_raid	Specifies the RAID for LDID 40	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg6

Specifies the mapping of RN-F LDID to RAID for LDIDs 48 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

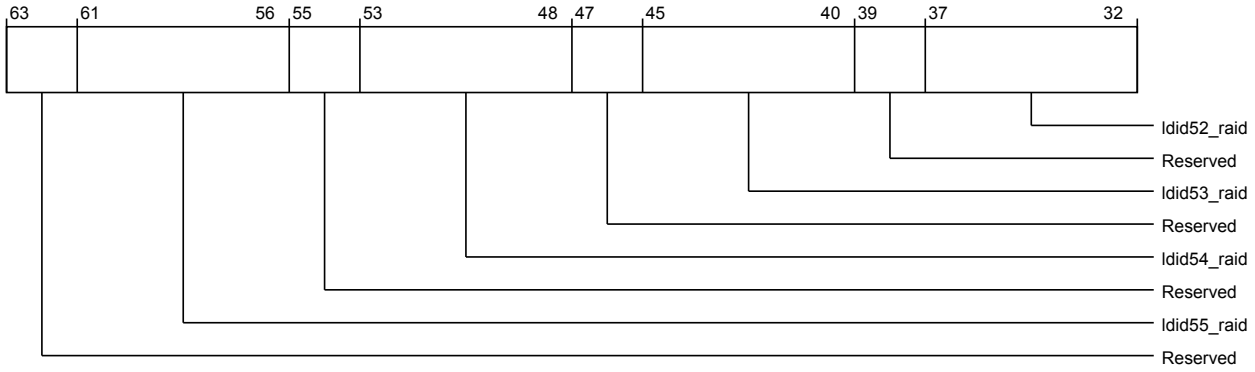


Figure 3-1208 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg6 higher register bit assignments.

Table 3-1222 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid55_raid	Specifies the RAID for LDID 55	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid54_raid	Specifies the RAID for LDID 54	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid53_raid	Specifies the RAID for LDID 53	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid52_raid	Specifies the RAID for LDID 52	RW	6'h0

The following image shows the lower register bit assignments.

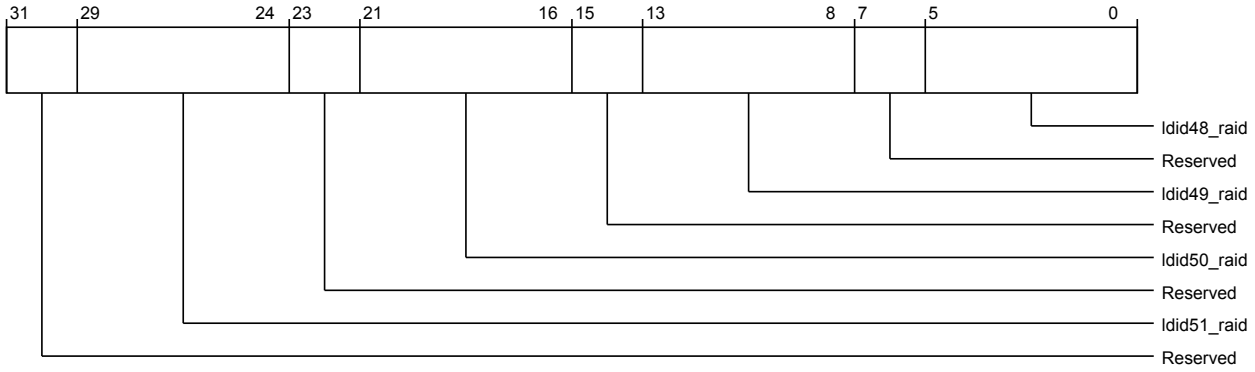


Figure 3-1209 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg6 lower register bit assignments.

Table 3-1223 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid51_raid	Specifies the RAID for LDID 51	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid50_raid	Specifies the RAID for LDID 50	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid49_raid	Specifies the RAID for LDID 49	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid48_raid	Specifies the RAID for LDID 48	RW	6'h0

por_cxg_ra_rnf_ldid_to_raid_reg7

Specifies the mapping of RN-F LDID to RAID for LDIDs 56 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hED8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

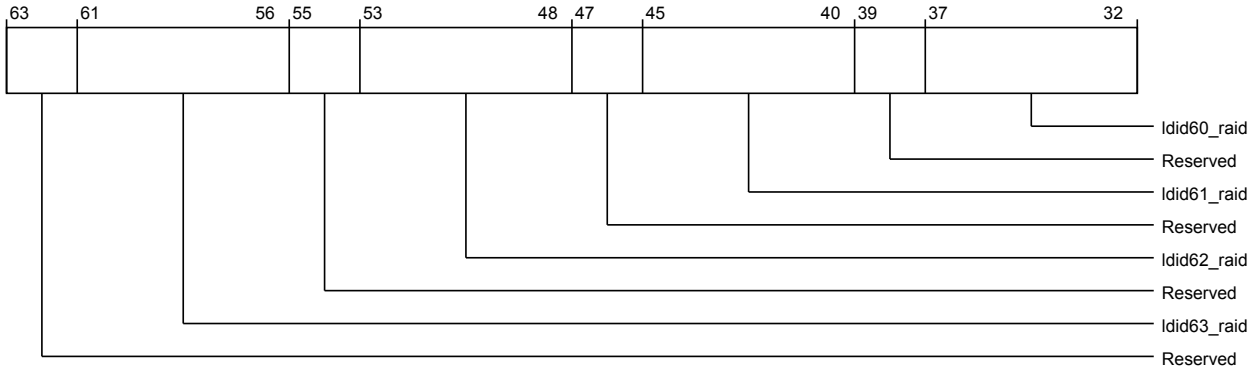


Figure 3-1210 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg7 higher register bit assignments.

Table 3-1224 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid63_raid	Specifies the RAID for LDID 63	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid62_raid	Specifies the RAID for LDID 62	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid61_raid	Specifies the RAID for LDID 61	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid60_raid	Specifies the RAID for LDID 60	RW	6'h0

The following image shows the lower register bit assignments.

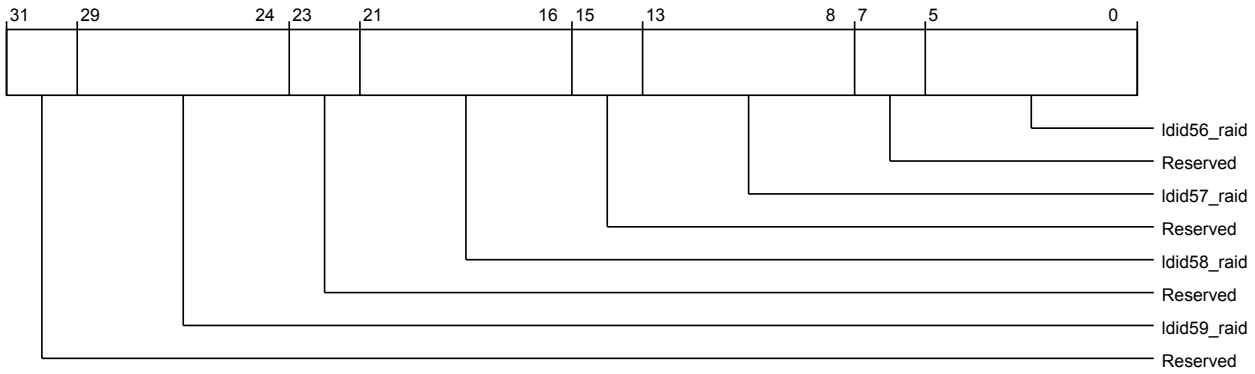


Figure 3-1211 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_reg7 lower register bit assignments.

Table 3-1225 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid59_raid	Specifies the RAID for LDID 59	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid58_raid	Specifies the RAID for LDID 58	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid57_raid	Specifies the RAID for LDID 57	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid56_raid	Specifies the RAID for LDID 56	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg0

Specifies the mapping of RN-I LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

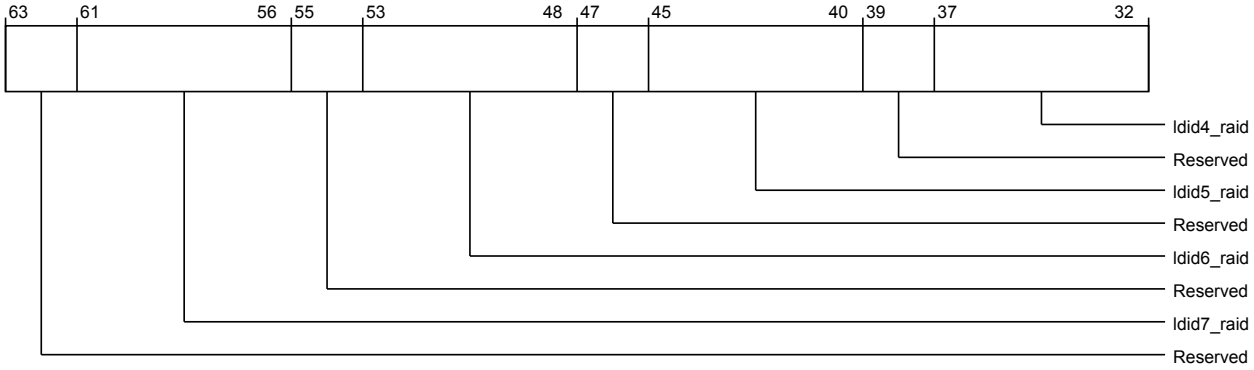


Figure 3-1212 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0 (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg0 higher register bit assignments.

Table 3-1226 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid7_raid	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid6_raid	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid5_raid	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid4_raid	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

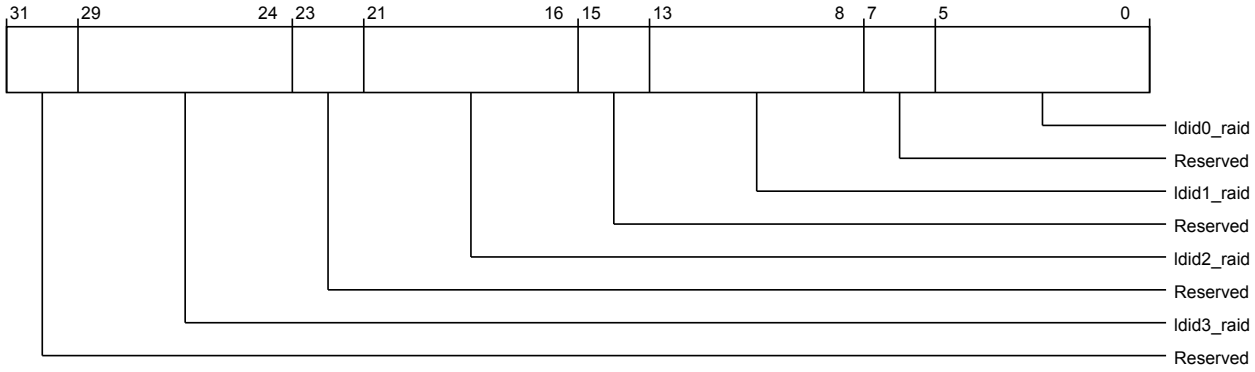


Figure 3-1213 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg0 lower register bit assignments.

Table 3-1227 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid3_raid	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid2_raid	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid1_raid	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid0_raid	Specifies the RAID for LDID 0	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg1

Specifies the mapping of RN-I LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEE8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

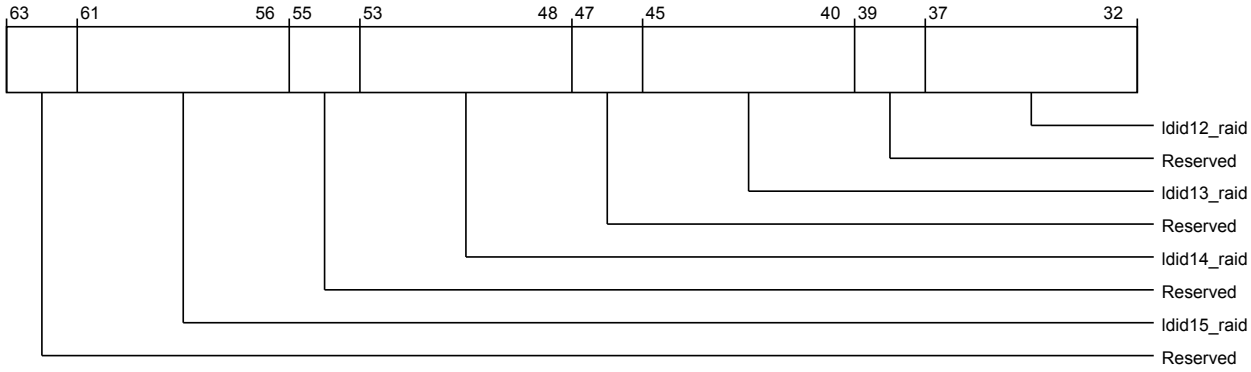


Figure 3-1214 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg1 higher register bit assignments.

Table 3-1228 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

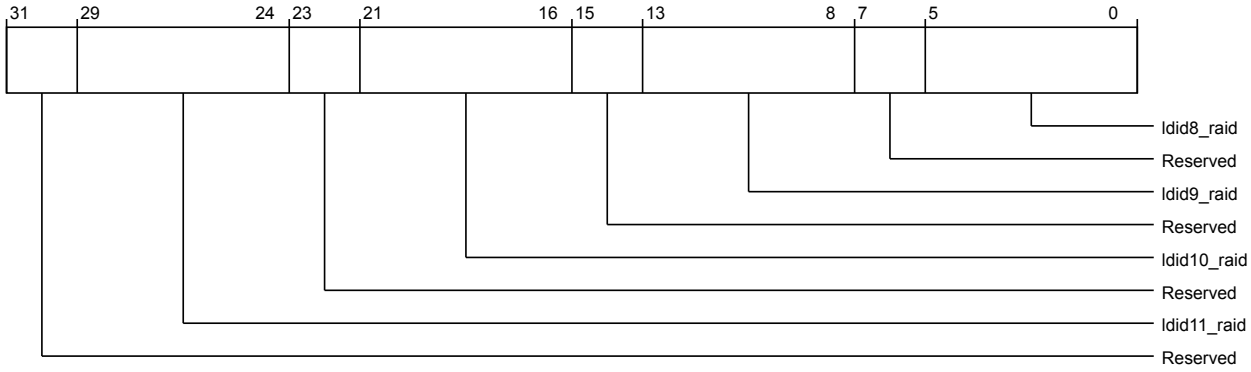


Figure 3-1215 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg1 lower register bit assignments.

Table 3-1229 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid11_raid	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid10_raid	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid9_raid	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid8_raid	Specifies the RAID for LDID 8	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg2

Specifies the mapping of RN-I LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF0

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

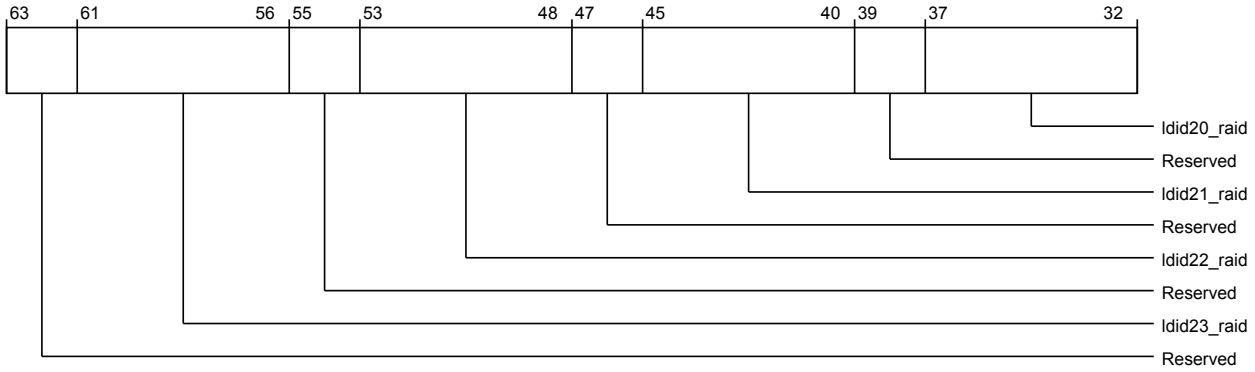


Figure 3-1216 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg2 higher register bit assignments.

Table 3-1230 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid23_raid	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid22_raid	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid21_raid	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid20_raid	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

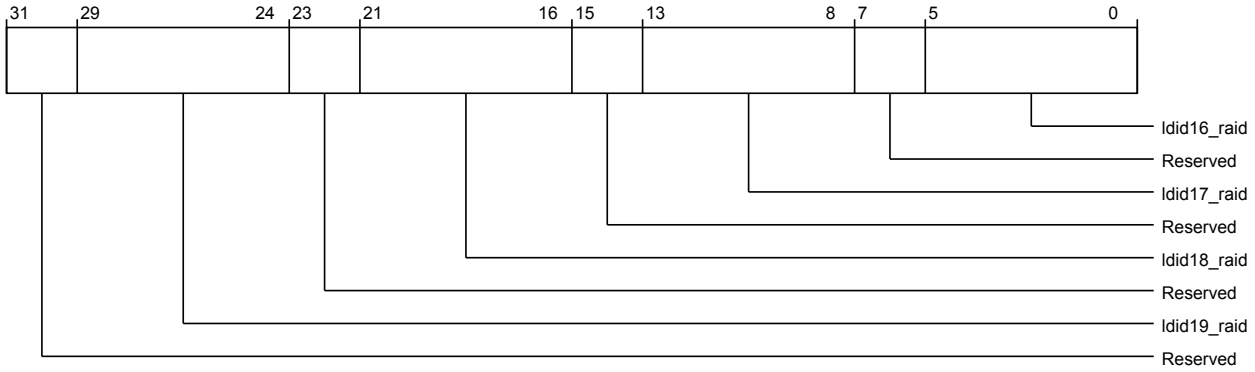


Figure 3-1217 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg2 lower register bit assignments.

Table 3-1231 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid19_raid	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid18_raid	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid17_raid	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid16_raid	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rni_ldid_to_raid_reg3

Specifies the mapping of RN-I LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hEF8

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

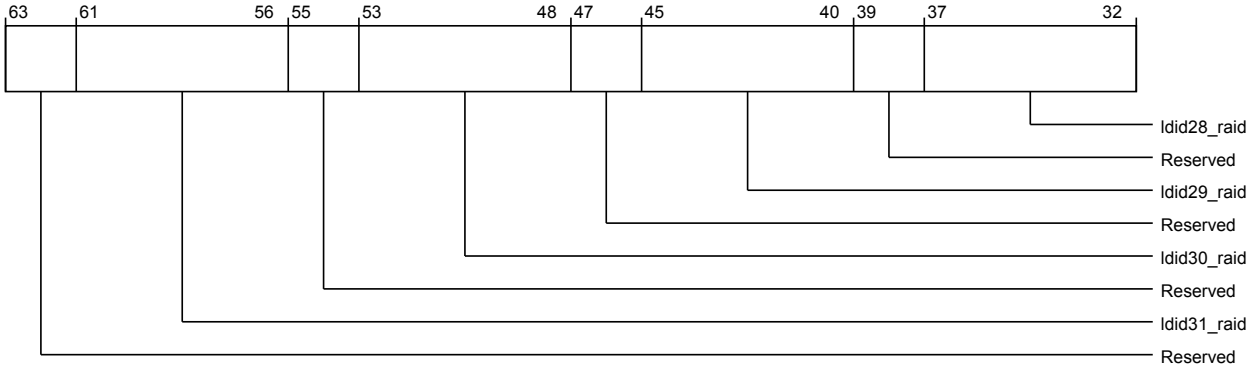


Figure 3-1218 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3 (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg3 higher register bit assignments.

Table 3-1232 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid31_raid	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid30_raid	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid29_raid	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid28_raid	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

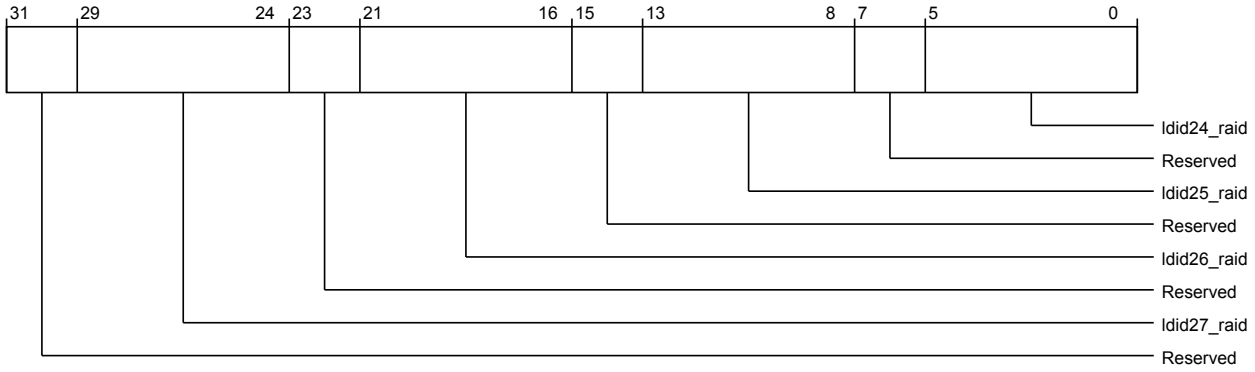


Figure 3-1219 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3 (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_reg3 lower register bit assignments.

Table 3-1233 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid27_raid	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid26_raid	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid25_raid	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid24_raid	Specifies the RAID for LDID 24	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg0

Specifies the mapping of RN-D LDID to RAID for LDIDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF00

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

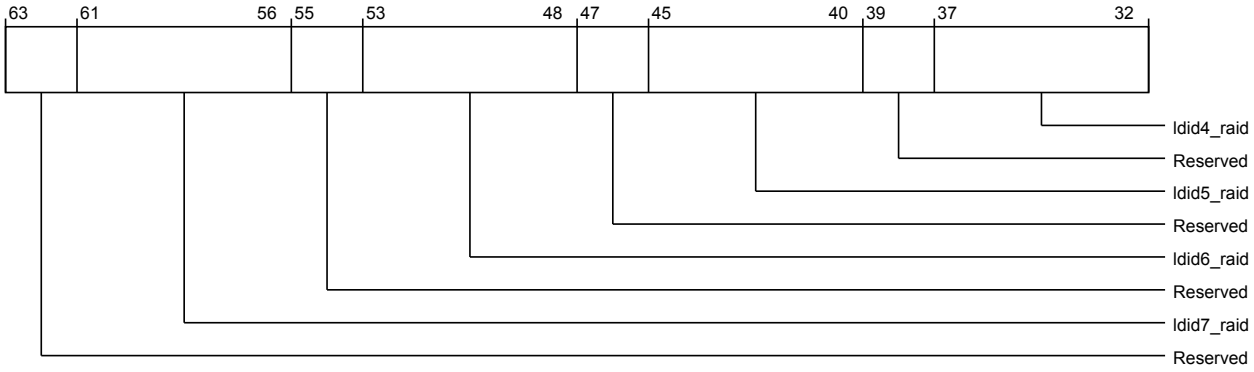


Figure 3-1220 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg0 higher register bit assignments.

Table 3-1234 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid7_raid	Specifies the RAID for LDID 7	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid6_raid	Specifies the RAID for LDID 6	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid5_raid	Specifies the RAID for LDID 5	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid4_raid	Specifies the RAID for LDID 4	RW	6'h0

The following image shows the lower register bit assignments.

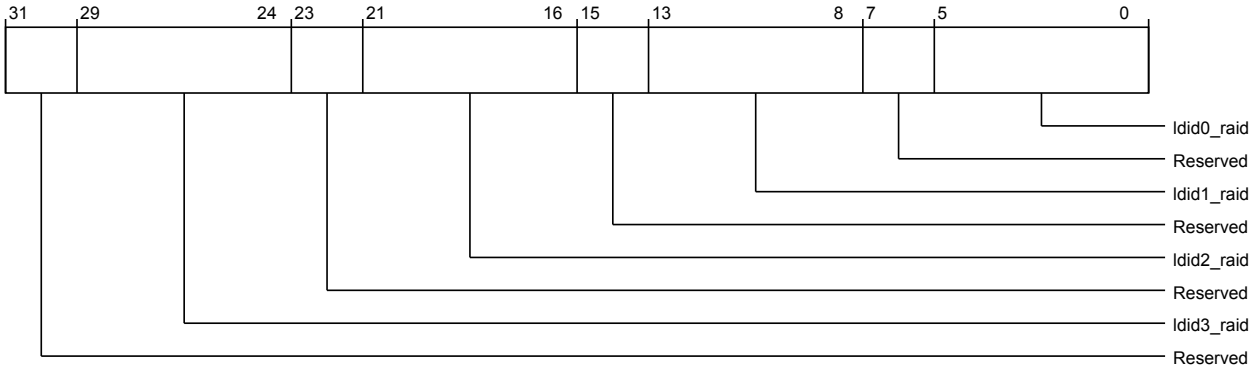


Figure 3-1221 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (low)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg0 lower register bit assignments.

Table 3-1235 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid3_raid	Specifies the RAID for LDID 3	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid2_raid	Specifies the RAID for LDID 2	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid1_raid	Specifies the RAID for LDID 1	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid0_raid	Specifies the RAID for LDID 0	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg1

Specifies the mapping of RN-D LDID to RAID for LDIDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF08

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

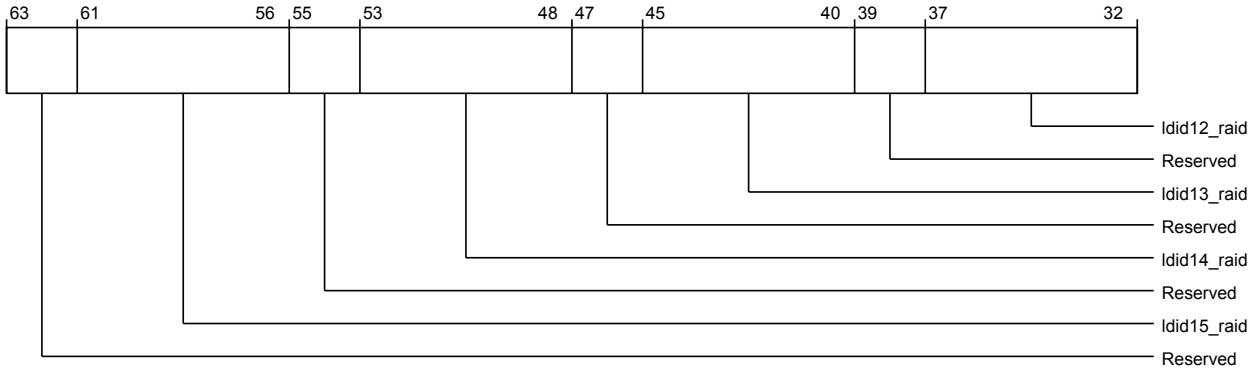


Figure 3-1222 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg1 higher register bit assignments.

Table 3-1236 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid15_raid	Specifies the RAID for LDID 15	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid14_raid	Specifies the RAID for LDID 14	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid13_raid	Specifies the RAID for LDID 13	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid12_raid	Specifies the RAID for LDID 12	RW	6'h0

The following image shows the lower register bit assignments.

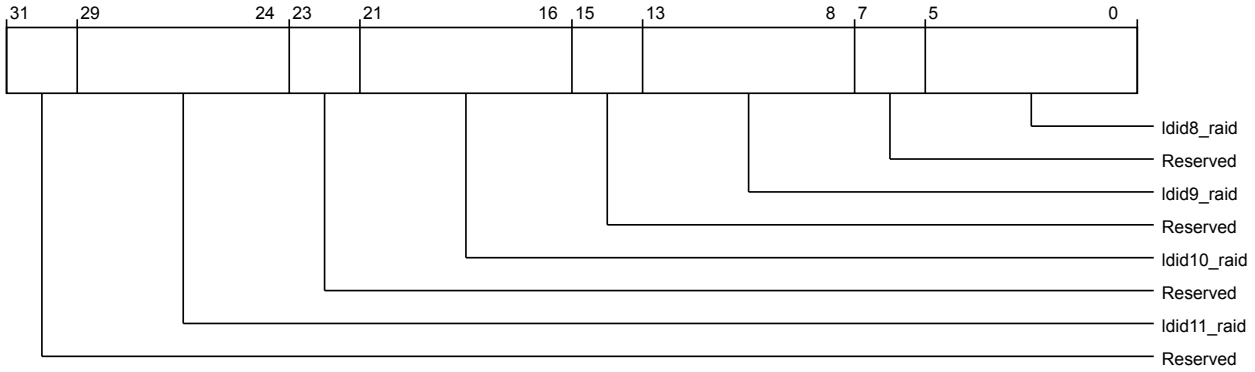


Figure 3-1223 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1 (low)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg1 lower register bit assignments.

Table 3-1237 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid11_raid	Specifies the RAID for LDID 11	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid10_raid	Specifies the RAID for LDID 10	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid9_raid	Specifies the RAID for LDID 9	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid8_raid	Specifies the RAID for LDID 8	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg2

Specifies the mapping of RN-D LDID to RAID for LDIDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF10

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

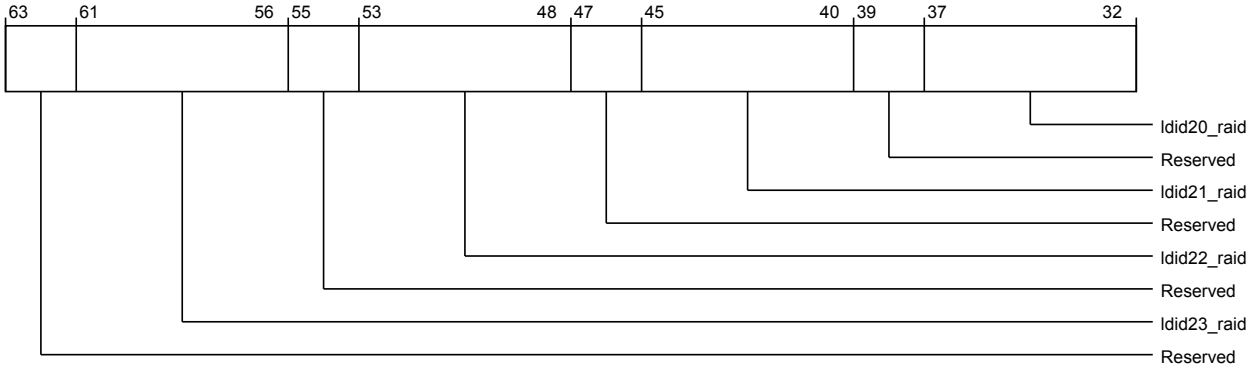


Figure 3-1224 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg2 higher register bit assignments.

Table 3-1238 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid23_raid	Specifies the RAID for LDID 23	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid22_raid	Specifies the RAID for LDID 22	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid21_raid	Specifies the RAID for LDID 21	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid20_raid	Specifies the RAID for LDID 20	RW	6'h0

The following image shows the lower register bit assignments.

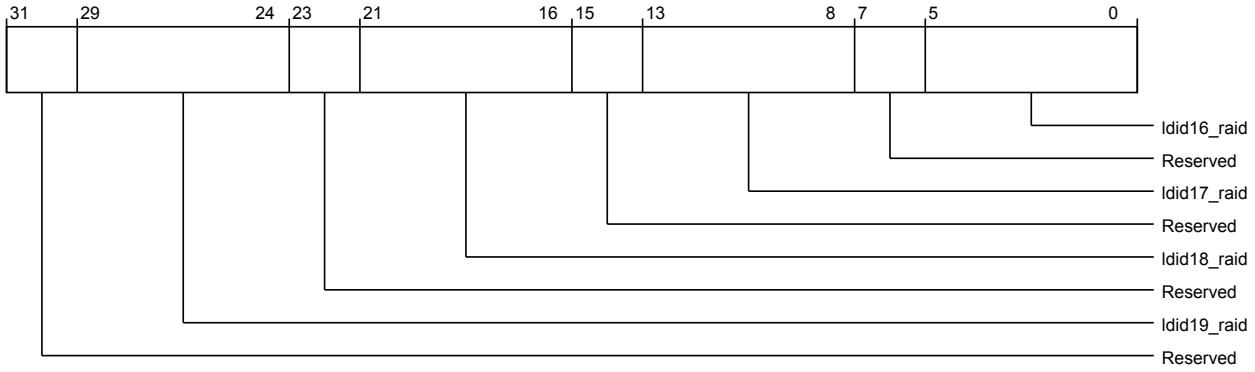


Figure 3-1225 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2 (low)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg2 lower register bit assignments.

Table 3-1239 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid19_raid	Specifies the RAID for LDID 19	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid18_raid	Specifies the RAID for LDID 18	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid17_raid	Specifies the RAID for LDID 17	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid16_raid	Specifies the RAID for LDID 16	RW	6'h0

por_cxg_ra_rnd_ldid_to_raid_reg3

Specifies the mapping of RN-D LDID to RAID for LDIDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF18

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

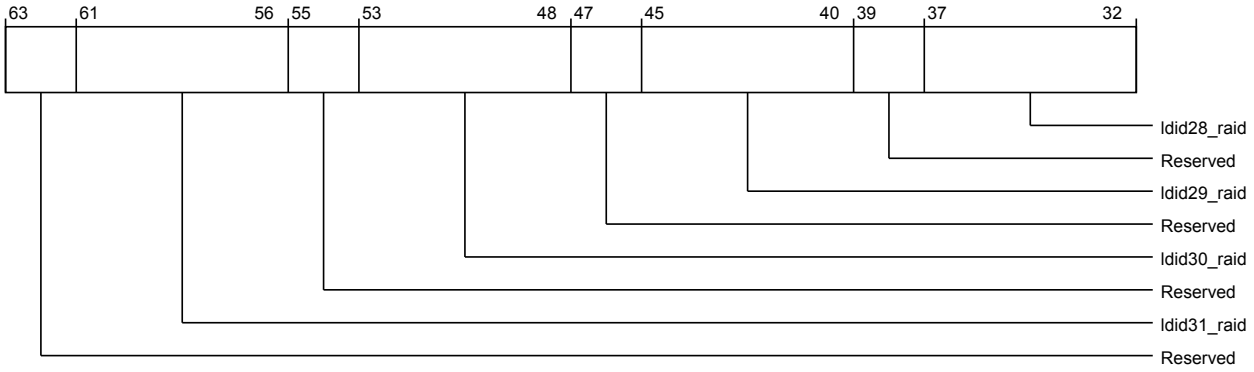


Figure 3-1226 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg3 higher register bit assignments.

Table 3-1240 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:62	Reserved	Reserved	RO	-
61:56	ldid31_raid	Specifies the RAID for LDID 31	RW	6'h0
55:54	Reserved	Reserved	RO	-
53:48	ldid30_raid	Specifies the RAID for LDID 30	RW	6'h0
47:46	Reserved	Reserved	RO	-
45:40	ldid29_raid	Specifies the RAID for LDID 29	RW	6'h0
39:38	Reserved	Reserved	RO	-
37:32	ldid28_raid	Specifies the RAID for LDID 28	RW	6'h0

The following image shows the lower register bit assignments.

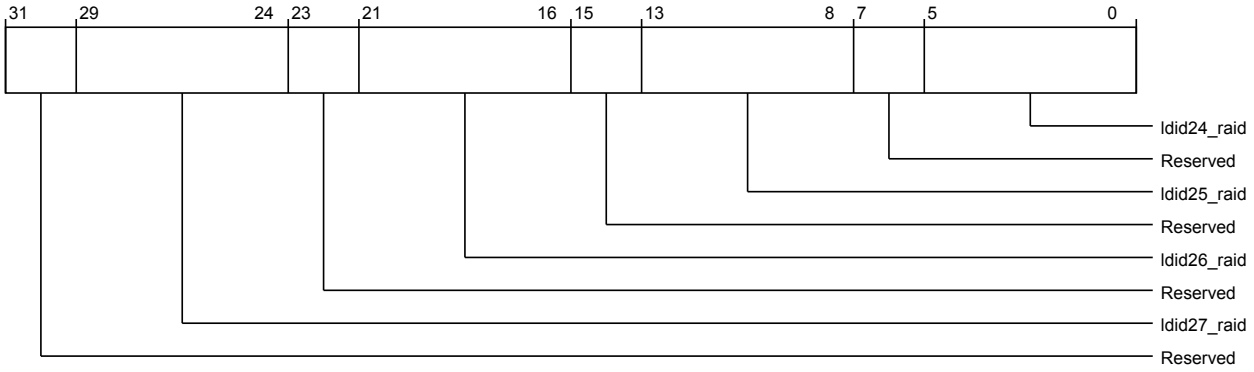


Figure 3-1227 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (low)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_reg3 lower register bit assignments.

Table 3-1241 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	ldid27_raid	Specifies the RAID for LDID 27	RW	6'h0
23:22	Reserved	Reserved	RO	-
21:16	ldid26_raid	Specifies the RAID for LDID 26	RW	6'h0
15:14	Reserved	Reserved	RO	-
13:8	ldid25_raid	Specifies the RAID for LDID 25	RW	6'h0
7:6	Reserved	Reserved	RO	-
5:0	ldid24_raid	Specifies the RAID for LDID 24	RW	6'h0

por_cxg_ra_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF20

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

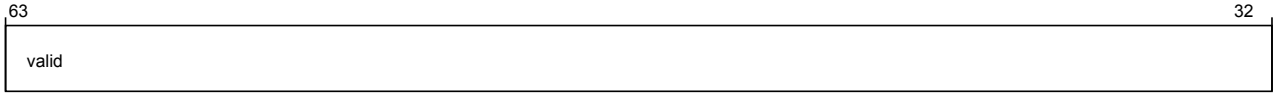


Figure 3-1228 por_cxg_ra_por_cxg_ra_agentid_to_linkid_val (high)

The following table shows the por_cxg_ra_agentid_to_linkid_val higher register bit assignments.

Table 3-1242 por_cxg_ra_por_cxg_ra_agentid_to_linkid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

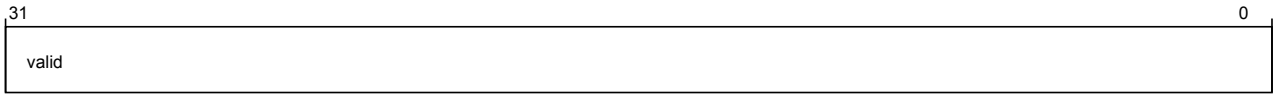


Figure 3-1229 por_cxg_ra_por_cxg_ra_agentid_to_linkid_val (low)

The following table shows the por_cxg_ra_agentid_to_linkid_val lower register bit assignments.

Table 3-1243 por_cxg_ra_por_cxg_ra_agentid_to_linkid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

por_cxg_ra_rnf_ldid_to_raid_val

Specifies which RN-F LDID to RAID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF28

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

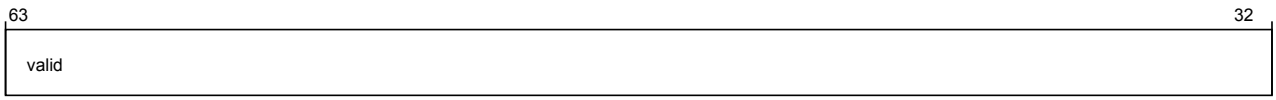


Figure 3-1230 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val (high)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_val higher register bit assignments.

Table 3-1244 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

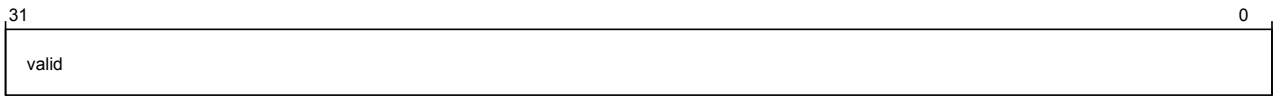


Figure 3-1231 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val (low)

The following table shows the por_cxg_ra_rnf_ldid_to_raid_val lower register bit assignments.

Table 3-1245 por_cxg_ra_por_cxg_ra_rnf_ldid_to_raid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-F LDID number (from 0 to 63)	RW	63'h0

por_cxg_ra_rni_ldid_to_raid_val

Specifies which RN-I LDID to RAID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

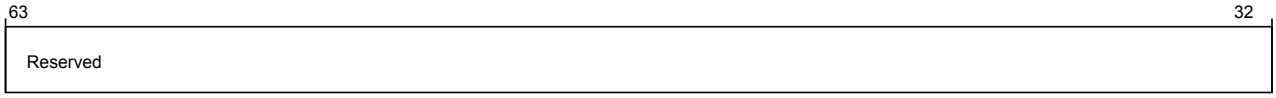


Figure 3-1232 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val (high)

The following table shows the por_cxg_ra_rni_ldid_to_raid_val higher register bit assignments.

Table 3-1246 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

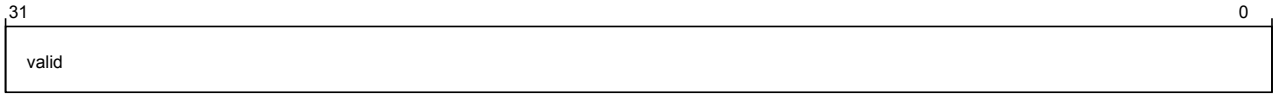


Figure 3-1233 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val (low)

The following table shows the por_cxg_ra_rni_ldid_to_raid_val lower register bit assignments.

Table 3-1247 por_cxg_ra_por_cxg_ra_rni_ldid_to_raid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-I LDID number (from 0 to 31)	RW	32'h0

por_cxg_ra_rnd_ldid_to_raid_val

Specifies which RN-D LDID to RAID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hF38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxg_ra_secure_register_groups_override.ldid_ctl

The following image shows the higher register bit assignments.

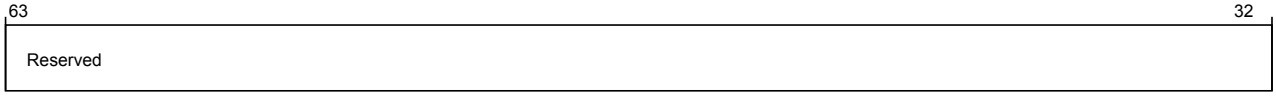


Figure 3-1234 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val (high)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_val higher register bit assignments.

Table 3-1248 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

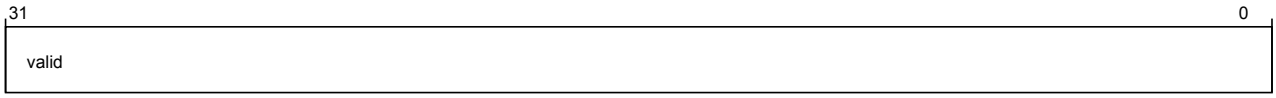


Figure 3-1235 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val (low)

The following table shows the por_cxg_ra_rnd_ldid_to_raid_val lower register bit assignments.

Table 3-1249 por_cxg_ra_por_cxg_ra_rnd_ldid_to_raid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the RAID is valid; bit number corresponds to logical RN-D LDID number (from 0 to 31)	RW	32'h0

por_cxg_ra_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2000
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

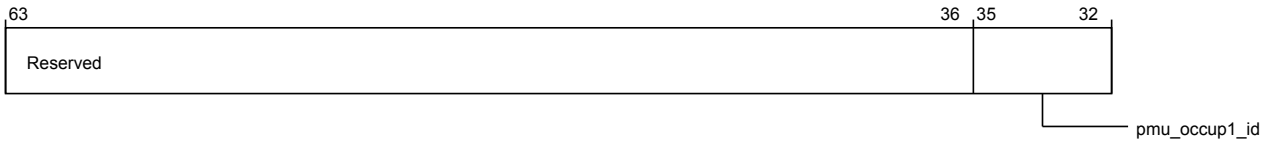


Figure 3-1236 por_cxg_ra_por_cxg_ra_pmu_event_sel (high)

The following table shows the por_cxg_ra_pmu_event_sel higher register bit assignments.

Table 3-1250 por_cxg_ra_por_cxg_ra_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:36	Reserved	Reserved	RO	-
35:32	pmu_occup1_id	PMU occupancy event selector ID	RW	4'b0

The following image shows the lower register bit assignments.

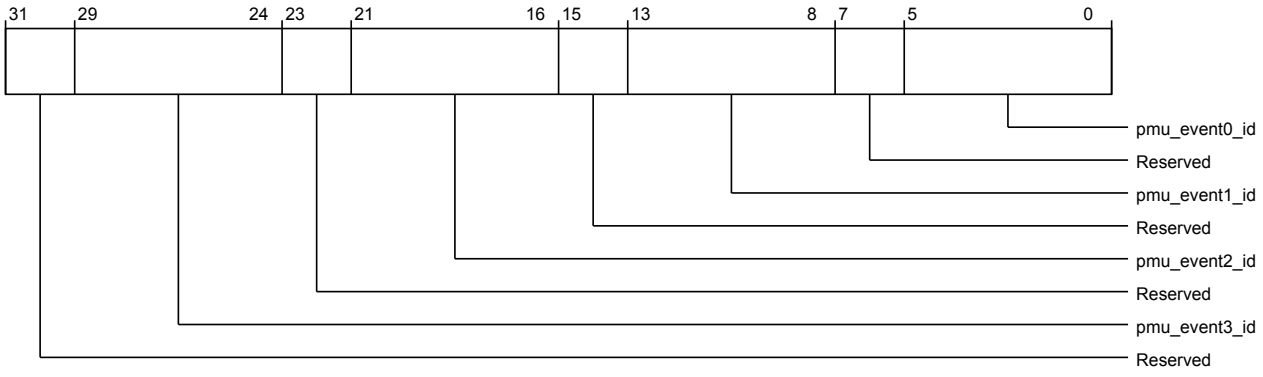


Figure 3-1237 por_cxg_ra_por_cxg_ra_pmu_event_sel (low)

The following table shows the por_cxg_ra_pmu_event_sel lower register bit assignments.

Table 3-1251 por_cxg_ra_por_cxg_ra_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:30	Reserved	Reserved	RO	-
29:24	pmu_event3_id	CXRA PMU Event 3 ID; see pmu_event0_id for encodings	RW	6'b0
23:22	Reserved	Reserved	RO	-
21:16	pmu_event2_id	CXRA PMU Event 2 ID; see pmu_event0_id for encodings	RW	6'b0
15:14	Reserved	Reserved	RO	-
13:8	pmu_event1_id	CXRA PMU Event 1 ID; see pmu_event0_id for encodings	RW	6'b0
7:6	Reserved	Reserved	RO	-
5:0	pmu_event0_id	CXRA PMU Event 0 ID 6'h00: No event 6'h01: Request Tracker (RHT) occupancy count overflow 6'h02: Snoop Tracker (SHT) occupancy count overflow 6'h03: Read Data Buffer (RDB) occupancy count overflow 6'h04: Write Data Buffer (WDB) occupancy count overflow 6'h05: Snoop Sink Buffer (SSB) occupancy count overflow 6'h06: CCIX RX broadcast snoops 6'h07: CCIX TX request chain 6'h08: CCIX TX request chain average length 6'h09: CHI internal RSP stall 6'h0A: CHI internal DAT stall 6'h0B: CCIX REQ Protocol credit Link 0 stall 6'h0C: CCIX REQ Protocol credit Link 1 stall 6'h0D: CCIX REQ Protocol credit Link 2 stall 6'h0E: CCIX DAT Protocol credit Link 0 stall 6'h0F: CCIX DAT Protocol credit Link 1 stall 6'h10: CCIX DAT Protocol credit Link 2 stall 6'h11: CHI external RSP stall 6'h12: CHI external DAT stall	RW	6'b0

por_cxg_ra_cxprtcl_link0_ctl

Functions as the CXRA CCIX Protocol Link 0 control register. Works with por_cxg_ra_cxprtcl_link0_status.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h1000

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

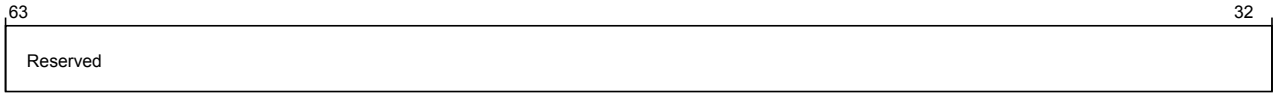


Figure 3-1238 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link0_ctl higher register bit assignments.

Table 3-1252 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

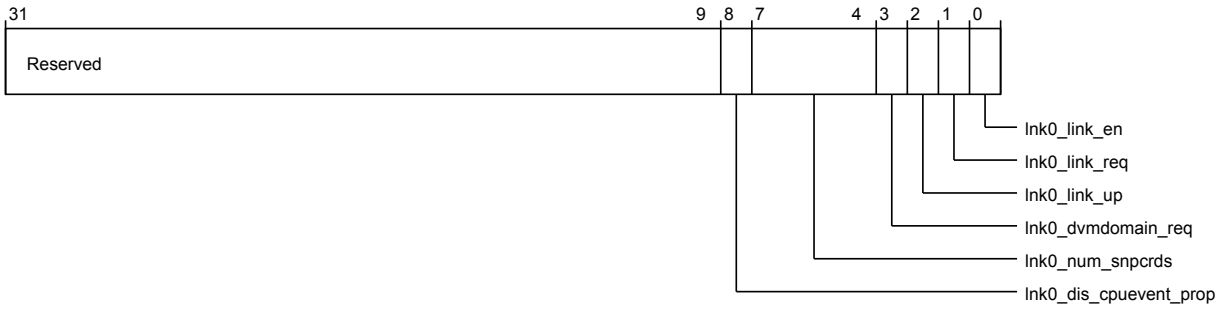


Figure 3-1239 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link0_ctl lower register bit assignments.

Table 3-1253 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	lnk0_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 0 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0
7:4	lnk0_num_snpcrds	Controls the number of CCIX snoop credits assigned to Link 0 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0

Table 3-1253 por_cxg_ra_por_cxg_ra_cxprtcl_link0_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
3	lnk0_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 0	RW	1'b0
2	lnk0_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk0_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk0_link_en	Enables CCIX Link 0 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ra_cxprtcl_link0_status

Functions as the CXRA CCIX Protocol Link 0 status register. Works with por_cxg_ra_cxprtcl_link0_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1008
Register reset 64'b0010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

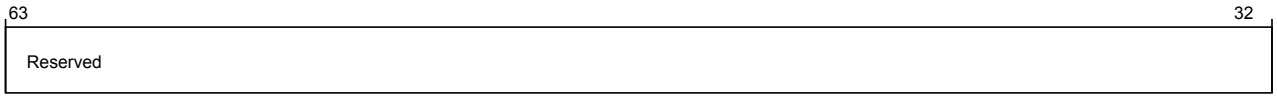


Figure 3-1240 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (high)

The following table shows the por_cxg_ra_cxprtcl_link0_status higher register bit assignments.

Table 3-1254 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

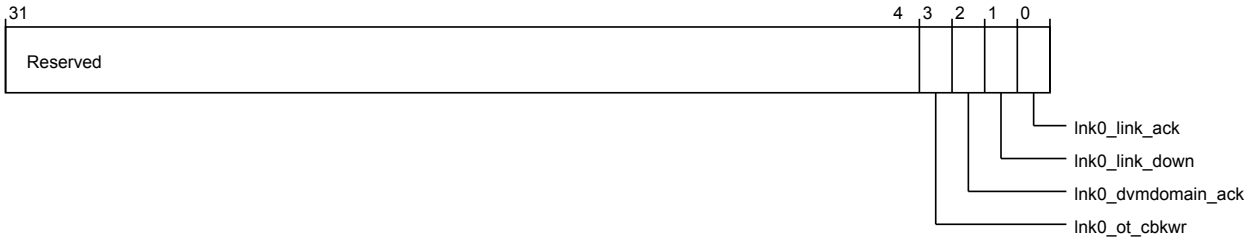


Figure 3-1241 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (low)

The following table shows the por_cxg_ra_cxprtcl_link0_status lower register bit assignments.

Table 3-1255 por_cxg_ra_por_cxg_ra_cxprtcl_link0_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk0_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link0	RO	1'b0
2	lnk0_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 0	RO	1'b0
1	lnk0_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk0_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops granting protocol credits and starts returning protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ra_cxprtcl_link1_ctl

Functions as the CXRA CCIX Protocol Link 1 control register. Works with por_cxg_ra_cxprtcl_link1_status.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1010

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

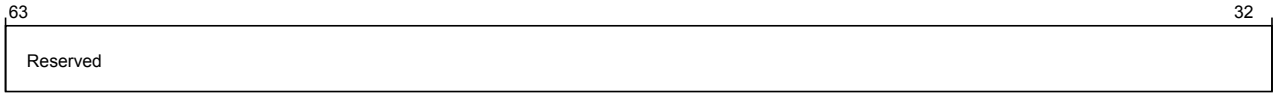


Figure 3-1242 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link1_ctl higher register bit assignments.

Table 3-1256 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

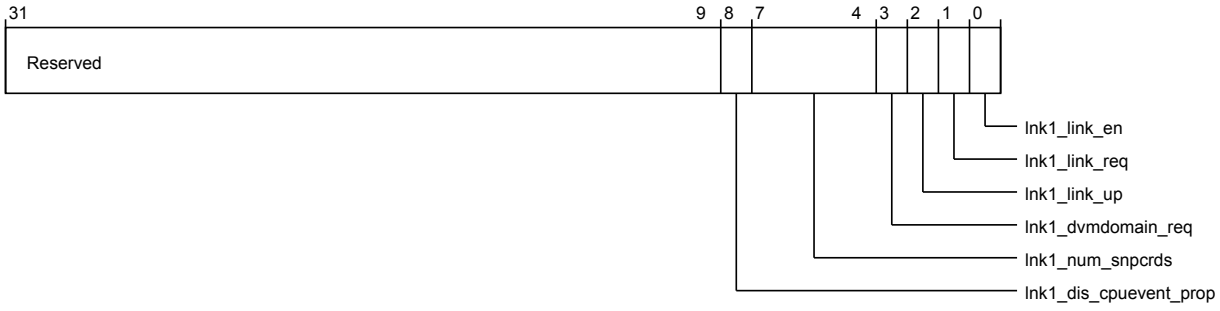


Figure 3-1243 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link1_ctl lower register bit assignments.

Table 3-1257 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	lnk1_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 1 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0

Table 3-1257 por_cxg_ra_por_cxg_ra_cxprtcl_link1_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
7:4	lnk1_num_snpcrds	Controls the number of CCIX snoop credits assigned to Link 1 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk1_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 1	RW	1'b0
2	lnk1_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk1_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk1_link_en	Enables CCIX Link 1 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ra_cxprtcl_link1_status

Functions as the CXRA CCIX Protocol Link 1 status register. Works with por_cxg_ra_cxprtcl_link1_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1018
Register reset 64'b0010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

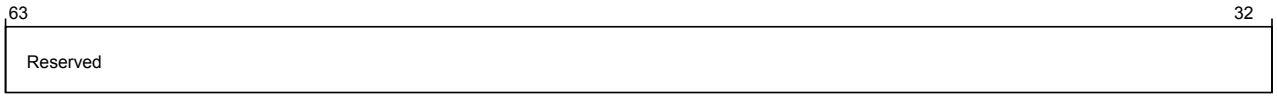


Figure 3-1244 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (high)

The following table shows the por_cxg_ra_cxprtcl_link1_status higher register bit assignments.

Table 3-1258 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

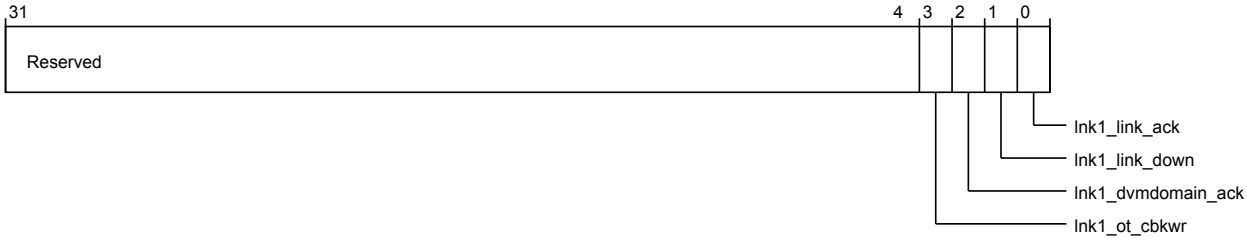


Figure 3-1245 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (low)

The following table shows the por_cxg_ra_cxprtcl_link1_status lower register bit assignments.

Table 3-1259 por_cxg_ra_por_cxg_ra_cxprtcl_link1_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk1_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link1	RO	1'b0
2	lnk1_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 1	RO	1'b0
1	lnk1_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk1_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

por_cxg_ra_cxprtcl_link2_ctl

Functions as the CXRA CCIX Protocol Link 2 control register. Works with por_cxg_ra_cxprtcl_link2_status.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h1020

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

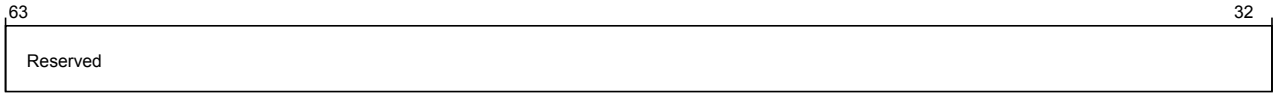


Figure 3-1246 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (high)

The following table shows the por_cxg_ra_cxprtcl_link2_ctl higher register bit assignments.

Table 3-1260 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

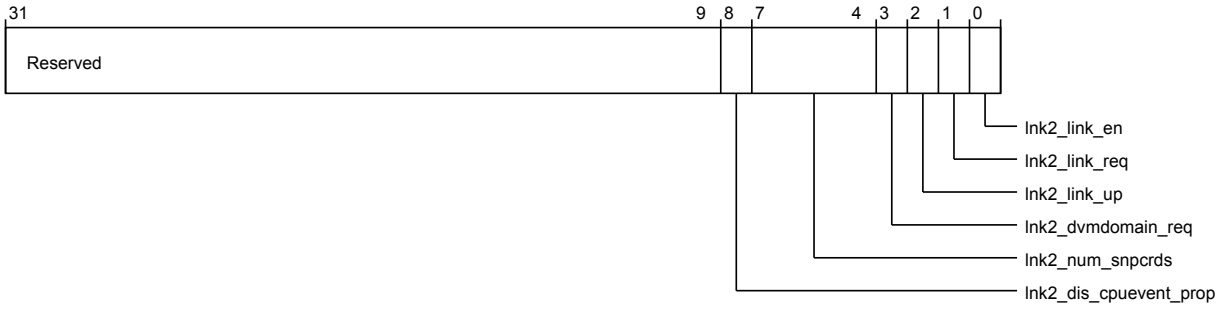


Figure 3-1247 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (low)

The following table shows the por_cxg_ra_cxprtcl_link2_ctl lower register bit assignments.

Table 3-1261 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (low)

Bits	Field name	Description	Type	Reset
31:9	Reserved	Reserved	RO	-
8	lnk2_dis_cpuevent_prop	When set, disables the propagation of CPU Events on CCIX Link 2 NOTE: This field is applicable only when SMP Mode enable parameter is set.	RW	1'b0

Table 3-1261 por_cxg_ra_por_cxg_ra_cxprtcl_link2_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
7:4	lnk2_num_snpcrds	Controls the number of CCIX snoop credits assigned to Link 2 4'h0: Total credits are equally divided across all links 4'h1: 25% of credits assigned 4'h2: 50% of credits assigned 4'h3: 75% of credits assigned 4'h4: 100% of credits assigned 4'hF: 0% of credits assigned	RW	4'b0
3	lnk2_dvmdomain_req	Controls DVM domain enable (SYSCOREQ) for CCIX Link 2	RW	1'b0
2	lnk2_link_up	Link Up status. Software writes this register bit to indicate Link status after polling Link_ACK and Link_DN status in the remote agent 1'b0: Link is not Up. Software clears Link_UP when Link_ACK status is clear and Link_DN status is set in both local and remote agents. The local agent stops responding to any protocol activity from remote agent, including acceptance of protocol credits, when Link_UP is clear 1'b1: Link is Up. Software sets Link_UP when Link_ACK status is set and Link_DN status is clear in both local and remote agents; the local agent starts sending local protocol credits to remote agent	RW	1'b0
1	lnk2_link_req	Link Up/Down request; software writes this register bit to request a Link Up or Link Down in the local agent 1'b0: Link Down request NOTE: The local agent does not return remote protocol credits yet since remote agent may still be in Link_UP state. 1'b1: Link Up request	RW	1'b0
0	lnk2_link_en	Enables CCIX Link 2 when set 1'b0: Link is disabled 1'b1: Link is enabled	RW	1'b0

por_cxg_ra_cxprtcl_link2_status

Functions as the CXRA CCIX Protocol Link 2 status register. Works with por_cxg_ra_cxprtcl_link2_ctl.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h1028
Register reset 64'b0010
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

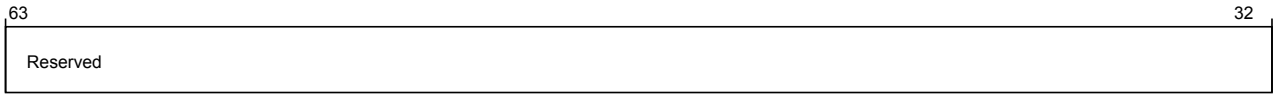


Figure 3-1248 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (high)

The following table shows the por_cxg_ra_cxprtcl_link2_status higher register bit assignments.

Table 3-1262 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

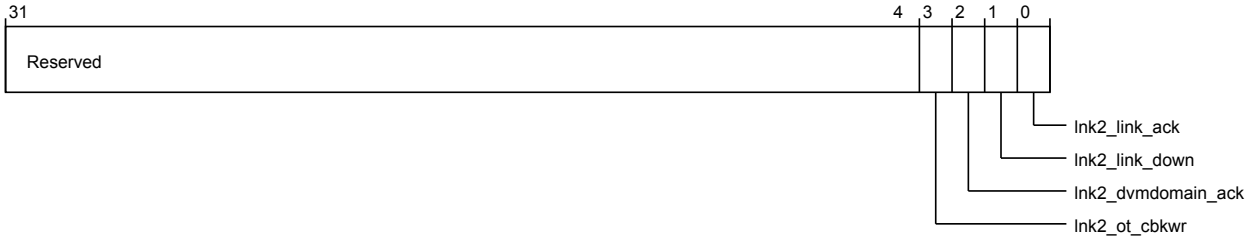


Figure 3-1249 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (low)

The following table shows the por_cxg_ra_cxprtcl_link2_status lower register bit assignments.

Table 3-1263 por_cxg_ra_por_cxg_ra_cxprtcl_link2_status (low)

Bits	Field name	Description	Type	Reset
31:4	Reserved	Reserved	RO	-
3	lnk2_ot_cbkwr	Provides status for outstanding CopyBack Write for CCIX Link2	RO	1'b0
2	lnk2_dvmdomain_ack	Provides DVM domain status (SYSCOACK) for CCIX Link 2	RO	1'b0
1	lnk2_link_down	Link Down status; hardware updates this register bit to indicate Link Down status 1'b0: Link is not Down; hardware clears Link_DN when it receives a Link Up request 1'b1: Link is Down; hardware sets Link_DN after the local agent has received all local protocol credits. The local agent must continue to respond to any remote protocol activity, including accepting and returning remote protocol credits until Link Up is clear	RO	1'b1
0	lnk2_link_ack	Link Up/Down acknowledge; hardware updates this register bit to acknowledge the software link request 1'b0: Link Down acknowledge; hardware clears Link_ACK on receiving a Link Down request; the local agent stops sending protocol credits to the remote agent when Link_ACK is clear 1'b1: Link Up acknowledge; hardware sets Link_ACK when the local agent is ready to start accepting protocol credits from the remote agent NOTE: The local agent must clear Link_DN before setting Link_ACK.	RO	1'b0

3.3.13 CXLA configuration registers

This section lists the CXLA configuration registers.

por_cxla_node_info

Provides component identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h0
Register reset Configuration dependent
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

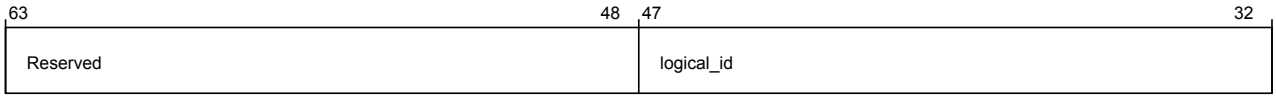


Figure 3-1250 por_cxla_por_cxla_node_info (high)

The following table shows the por_cxla_node_info higher register bit assignments.

Table 3-1264 por_cxla_por_cxla_node_info (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:32	logical_id	Component logical ID	RO	Configuration dependent

The following image shows the lower register bit assignments.

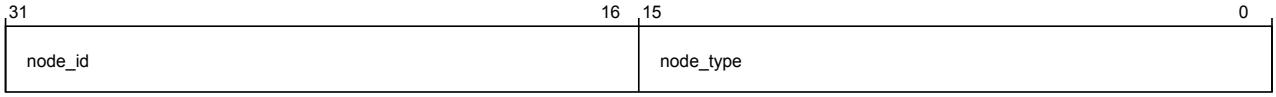


Figure 3-1251 por_cxla_por_cxla_node_info (low)

The following table shows the por_cxla_node_info lower register bit assignments.

Table 3-1265 por_cxla_por_cxla_node_info (low)

Bits	Field name	Description	Type	Reset
31:16	node_id	Component CHI node ID	RO	Configuration dependent
15:0	node_type	CMN-600 node type identifier	RO	16'h0102

por_cxla_child_info

Provides component child identification information.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'h80
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

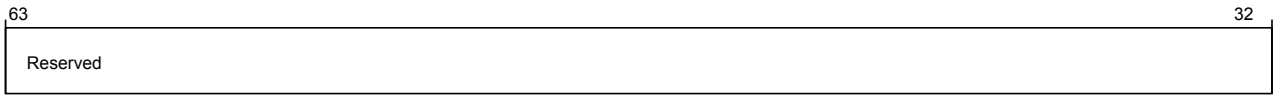


Figure 3-1252 por_cxla_por_cxla_child_info (high)

The following table shows the por_cxla_child_info higher register bit assignments.

Table 3-1266 por_cxla_por_cxla_child_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

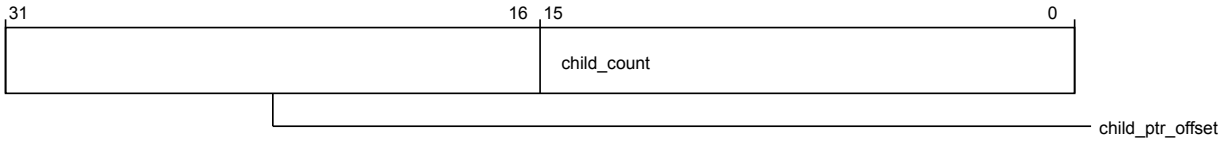


Figure 3-1253 por_cxla_por_cxla_child_info (low)

The following table shows the por_cxla_child_info lower register bit assignments.

Table 3-1267 por_cxla_por_cxla_child_info (low)

Bits	Field name	Description	Type	Reset
31:16	child_ptr_offset	Starting register offset which contains pointers to the child nodes	RO	16'h0
15:0	child_count	Number of child nodes; used in discovery process	RO	16'b0

por_cxla_secure_register_groups_override

Allows non-secure access to predefined groups of secure registers.

Its characteristics are:

Type RW
Register width (Bits) 64

Address offset 14'h980

Register reset 64'b0

Usage constraints Only accessible by secure accesses. Writes to this register must occur prior to the first non-configuration access targeting the device.

The following image shows the higher register bit assignments.

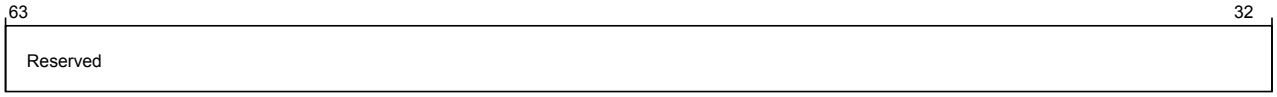


Figure 3-1254 por_cxla_por_cxla_secure_register_groups_override (high)

The following table shows the por_cxla_secure_register_groups_override higher register bit assignments.

Table 3-1268 por_cxla_por_cxla_secure_register_groups_override (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

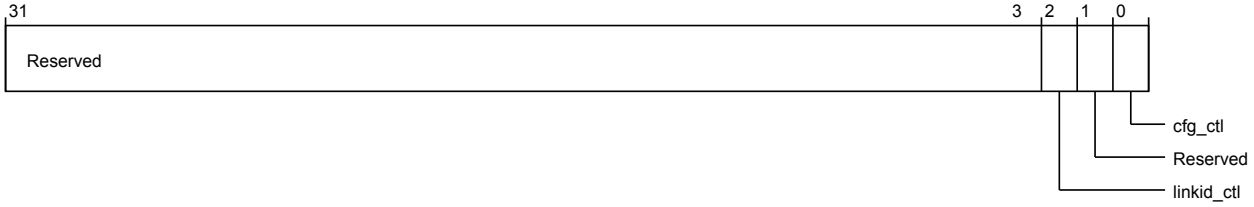


Figure 3-1255 por_cxla_por_cxla_secure_register_groups_override (low)

The following table shows the por_cxla_secure_register_groups_override lower register bit assignments.

Table 3-1269 por_cxla_por_cxla_secure_register_groups_override (low)

Bits	Field name	Description	Type	Reset
31:3	Reserved	Reserved	RO	-
2	linkid_ctl	Allows non-secure access to secure LA Link ID registers	RW	1'b0
1	Reserved	Reserved	RO	-
0	cfg_ctl	Allows non-secure access to secure configuration control register	RW	1'b0

por_cxla_unit_info

Provides component identification information for CXLA.

Its characteristics are:

Type RO

Register width (Bits) 64

Address offset 14'h900

Register reset Configuration dependent

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

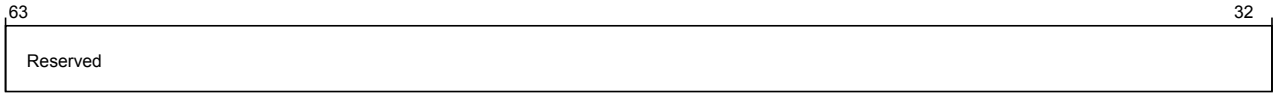


Figure 3-1256 por_cxla_por_cxla_unit_info (high)

The following table shows the por_cxla_unit_info higher register bit assignments.

Table 3-1270 por_cxla_por_cxla_unit_info (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

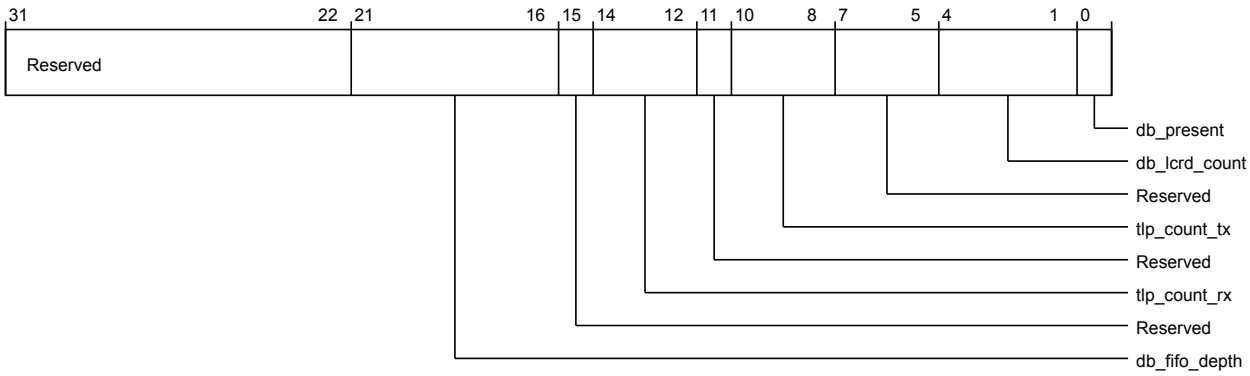


Figure 3-1257 por_cxla_por_cxla_unit_info (low)

The following table shows the por_cxla_unit_info lower register bit assignments.

Table 3-1271 por_cxla_por_cxla_unit_info (low)

Bits	Field name	Description	Type	Reset
31:22	Reserved	Reserved	RO	-
21:16	db_fifo_depth	FIFO Depth in CXLA Domain Bridges - CXDB, PDB	RO	Configuration dependent
15	Reserved	Reserved	RO	-
14:12	tlp_count_rx	Maximum number of TLPs supported by RX TLP buffer	RO	Configuration dependent
11	Reserved	Reserved	RO	-
10:8	tlp_count_tx	Maximum number of TLPs supported by TX TLP buffer	RO	Configuration dependent

Table 3-1271 por_cxla_por_cxla_unit_info (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:1	db_lcrd_count	Number of flit credits between CXG and CXLA	RO	Configuration dependent
0	db_present	DB present in CXLA	RO	Configuration dependent

por_cxla_aux_ctl

Functions as the auxiliary control register for CXLA.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hA08

Register reset 1'b1

Usage constraints Only accessible by secure accesses. This register can be modified only with prior written permission from Arm.

The following image shows the higher register bit assignments.

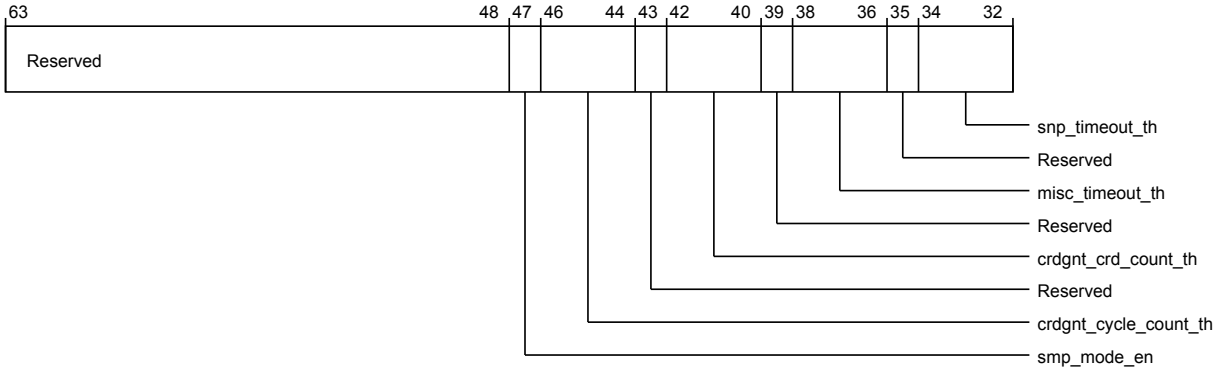


Figure 3-1258 por_cxla_por_cxla_aux_ctl (high)

The following table shows the por_cxla_aux_ctl higher register bit assignments.

Table 3-1272 por_cxla_por_cxla_aux_ctl (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47	smp_mode_en	When set, enables Symmetric Multiprocessor Mode (SMP) Mode.	RW	1'b1

Table 3-1272 por_cxla_por_cxla_aux_ctl (high) (continued)

Bits	Field name	Description	Type	Reset
46:44	crdgnt_cycle_count_th	Maximum number of cycles that need to be elapsed since the end of previous TLP to send a credit grant message 3'b000: 32 cycles 3'b001: 64 cycles 3'b010: 128 cycles 3'b011: 256 cycles	RW	3'b010
43	Reserved	Reserved	RO	-
42:40	crdgnt_crd_count_th	Maximum number of credits that need to be accumulated to send a credit grant message 3'b000: 16 credits 3'b001: 32 credits 3'b010: 64 credits 3'b011: 128 credits	RW	3'b010
39	Reserved	Reserved	RO	-
38:36	misc_timeout_th	Maximum number of cycles a MISC message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
35	Reserved	Reserved	RO	-
34:32	snp_timeout_th	Maximum number of cycles a SNP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000

The following image shows the lower register bit assignments.

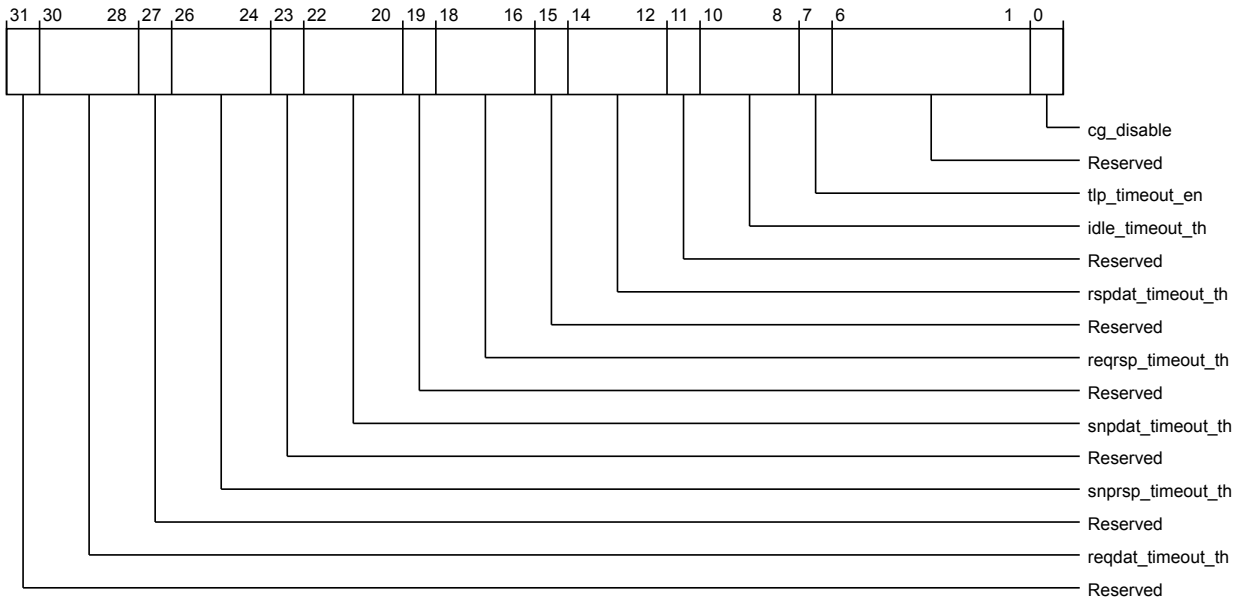


Figure 3-1259 por_cxla_por_cxla_aux_ctl (low)

The following table shows the por_cxla_aux_ctl lower register bit assignments.

Table 3-1273 por_cxla_por_cxla_aux_ctl (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	reqdat_timeout_th	Maximum number of cycles a REQDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
27	Reserved	Reserved	RO	-
26:24	snprsp_timeout_th	Maximum number of cycles a SNPRSP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
23	Reserved	Reserved	RO	-

Table 3-1273 por_cxla_por_cxla_aux_ctl (low) (continued)

Bits	Field name	Description	Type	Reset
22:20	snpdat_timeout_th	Maximum number of cycles a SNPDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
19	Reserved	Reserved	RO	-
18:16	reqrsp_timeout_th	Maximum number of cycles a REQRSP message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
15	Reserved	Reserved	RO	-
14:12	rspdat_timeout_th	Maximum number of cycles a RSPDAT message packed into a TLP waits to complete/end the TLP; applies for message packing 3'b000: same as idle_timeout_th 3'b001: 4 cycles 3'b010: 8 cycles 3'b011: 16 cycles 3'b100: 32 cycles	RW	3'b000
11	Reserved	Reserved	RO	-
10:8	idle_timeout_th	Maximum number of idle cycles a TLP waits for a message to pack to complete/end the TLP; applies for message packing 3'b000: 4 cycles 3'b001: 8 cycles 3'b010: 16 cycles 3'b011: 32 cycles	RW	3'b001
7	tlp_timeout_en	Enables TLP timeout based on thresholds set for each message type; doesn't apply for idle timeout; applies for message packing	RW	1'b1
6:1	Reserved	Reserved	RO	-
0	cg_disable	Disables CXLA architectural clock gates	RW	1'b0

por_cxla_ccix_prop_capabilities

Contains CCIX-supported properties.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'hC00
Register reset Configuration dependent
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

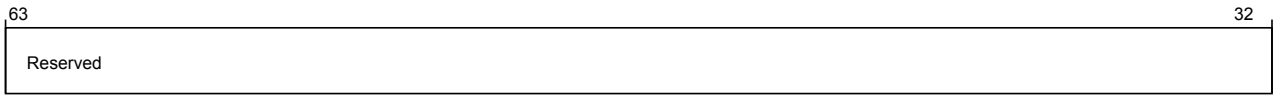


Figure 3-1260 por_cxla_por_cxla_ccix_prop_capabilities (high)

The following table shows the por_cxla_ccix_prop_capabilities higher register bit assignments.

Table 3-1274 por_cxla_por_cxla_ccix_prop_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

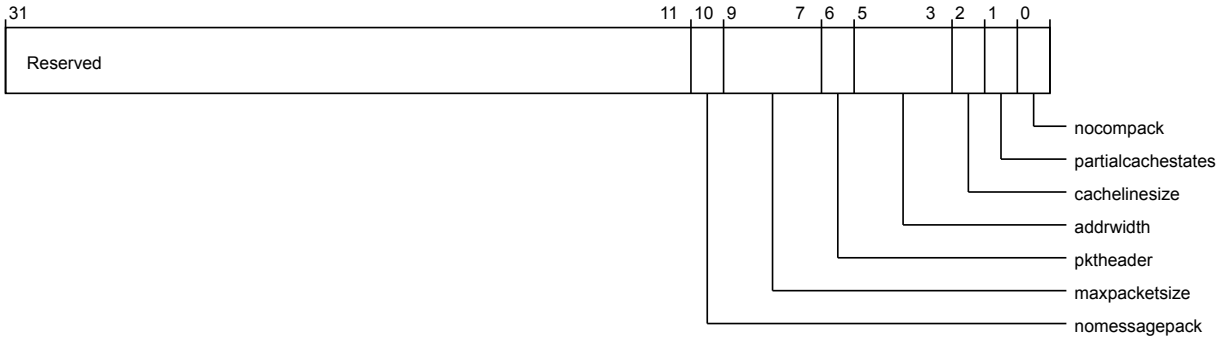


Figure 3-1261 por_cxla_por_cxla_ccix_prop_capabilities (low)

The following table shows the por_cxla_ccix_prop_capabilities lower register bit assignments.

Table 3-1275 por_cxla_por_cxla_ccix_prop_capabilities (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	nomessagepack	No message packing only supported 1'b0: False 1'b1: True	RO	1'b1
9:7	maxpacketsize	Maximum packet size supported 3'b000: 128B 3'b001: 256B 3'b010: 512B	RO	3'b010
6	pktheader	Packet header supported 1'b0: PCIe compatible header 1'b1: Optimized header	RO	1'b0
5:3	addrwidth	Address width supported 3'b000: 48b 3'b001: 52b 3'b010: 56b 3'b011: 60b 3'b100: 64b	RO	3'b000
2	cachelinesize	Cacheline size supported 1'b0: 64B 1'b1: 128B	RO	1'b0
1	partialcachestates	Partial cache states supported 1'b0: False 1'b1: True	RO	1'b0
0	nocompack	No CompAck supported 1'b0: False 1'b1: True	RO	1'b0

por_cxla_ccix_prop_configured

Contains CCIX-configured properties.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC08
Register reset 64'b10000000000

Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

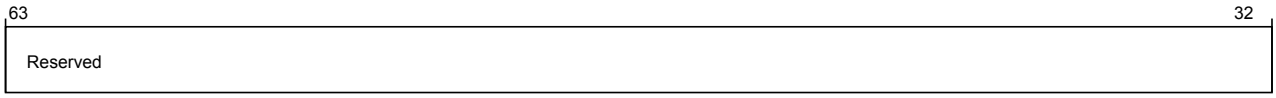


Figure 3-1262 por_cxla_por_cxla_ccix_prop_configured (high)

The following table shows the por_cxla_ccix_prop_configured higher register bit assignments.

Table 3-1276 por_cxla_por_cxla_ccix_prop_configured (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

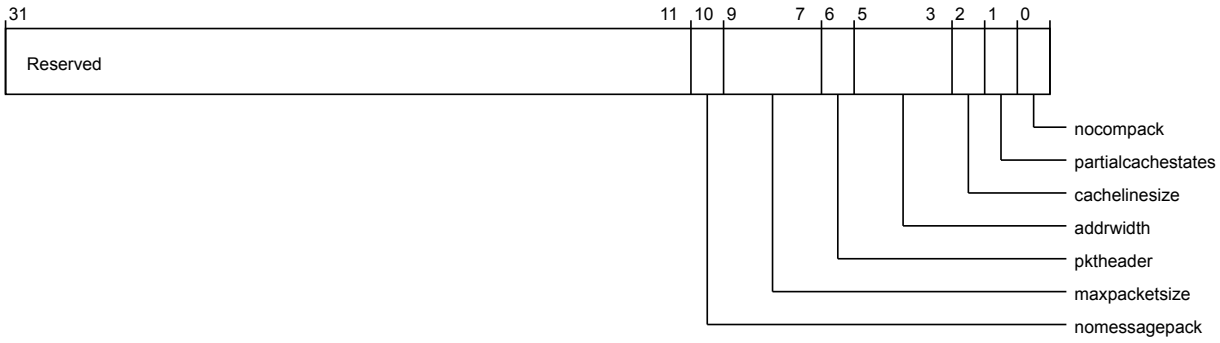


Figure 3-1263 por_cxla_por_cxla_ccix_prop_configured (low)

The following table shows the por_cxla_ccix_prop_configured lower register bit assignments.

Table 3-1277 por_cxla_por_cxla_ccix_prop_configured (low)

Bits	Field name	Description	Type	Reset
31:11	Reserved	Reserved	RO	-
10	nomessagepack	No message packing configured 1'b0: False 1'b1: True	RW	1'b1
9:7	maxpacketsize	Maximum packet size configured 3'b000: 128B 3'b001: 256B 3'b010: 512B	RW	3'b000

Table 3-1277 por_cxla_por_cxla_ccix_prop_configured (low) (continued)

Bits	Field name	Description	Type	Reset
6	pktheader	Packet header configured 1'b0: PCIe compatible header 1'b1: Optimized header	RW	1'b0
5:3	addrwidth	Address width configured 3'b000: 48b 3'b001: 52b 3'b010: 56b 3'b011: 60b 3'b100: 64b	RW	3'b000
2	cachelinesize	CacheLine size configured 1'b0: 64B 1'b1: 128B	RW	1'b0
1	partialcachestates	Partial cache states configured 1'b0: False 1'b1: True	RW	1'b0
0	nocompack	No CompAck configured 1'b0: False 1'b1: True	RW	1'b0

por_cxla_tx_cxs_attr_capabilities

Contains TX CXS supported attributes.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'hC10
Register reset Configuration dependent
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

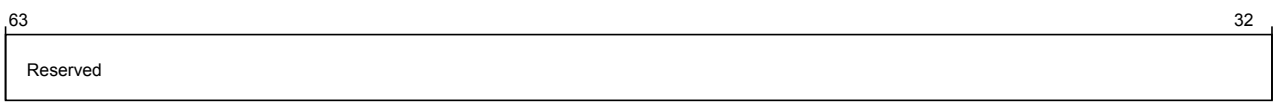


Figure 3-1264 por_cxla_por_cxla_tx_cxs_attr_capabilities (high)

The following table shows the por_cxla_tx_cxs_attr_capabilities higher register bit assignments.

Table 3-1278 por_cxla_por_cxla_tx_cxs_attr_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

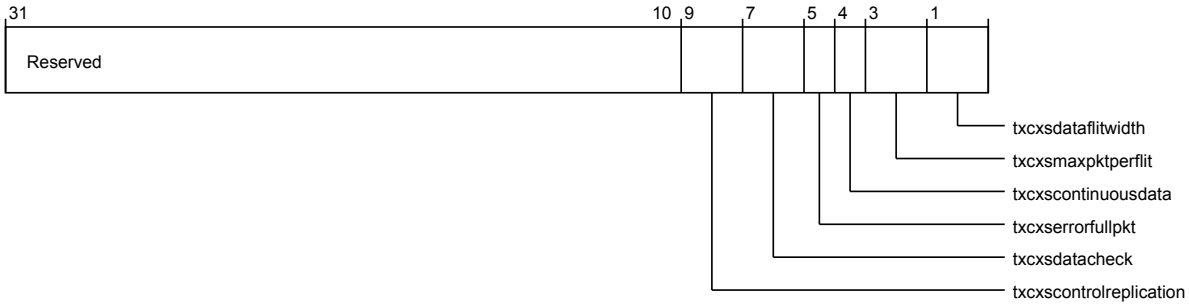


Figure 3-1265 por_cxla_por_cxla_tx_cxs_attr_capabilities (low)

The following table shows the por_cxla_tx_cxs_attr_capabilities lower register bit assignments.

Table 3-1279 por_cxla_por_cxla_tx_cxs_attr_capabilities (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:8	txcxscontrolreplication	TX CXS control replication supported 2'b00: None 2'b01: Duplicate 2'b10: Triplicate	RO	2'b00
7:6	txcxsdatacheck	TX CXS datacheck supported 2'b00: None 2'b01: Parity 2'b10: SECDED	RO	2'b00
5	txcxserrorfullpkt	TX CXS error full packet supported 1'b0: False 1'b1: True	RO	1'b1
4	txcxscontinuousdata	TX CXS continuous data supported 1'b0: False 1'b1: True	RO	1'b0

Table 3-1279 por_cxla_por_cxla_tx_cxs_attr_capabilities (low) (continued)

Bits	Field name	Description	Type	Reset
3:2	txcxsmaxpktperflit	TX CXS maximum packets per flit supported 2'b00: 2 2'b01: 3 2'b10: 4	RO	2'b00
1:0	txcxsdataflitwidth	TX CXS data flit width supported 2'b00: 256b 2'b01: 512b 2'b10: 1024b	RO	2'b00

por_cxla_rx_cxs_attr_capabilities

Contains RX CXS supported attributes.

Its characteristics are:

Type RO
Register width (Bits) 64
Address offset 14'hC18
Register reset Configuration dependent
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

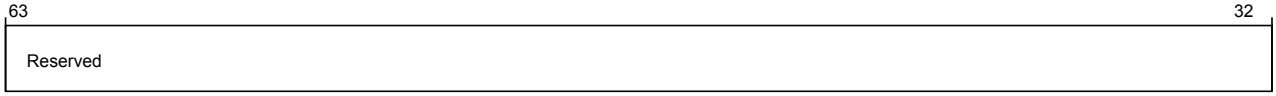


Figure 3-1266 por_cxla_por_cxla_rx_cxs_attr_capabilities (high)

The following table shows the por_cxla_rx_cxs_attr_capabilities higher register bit assignments.

Table 3-1280 por_cxla_por_cxla_rx_cxs_attr_capabilities (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

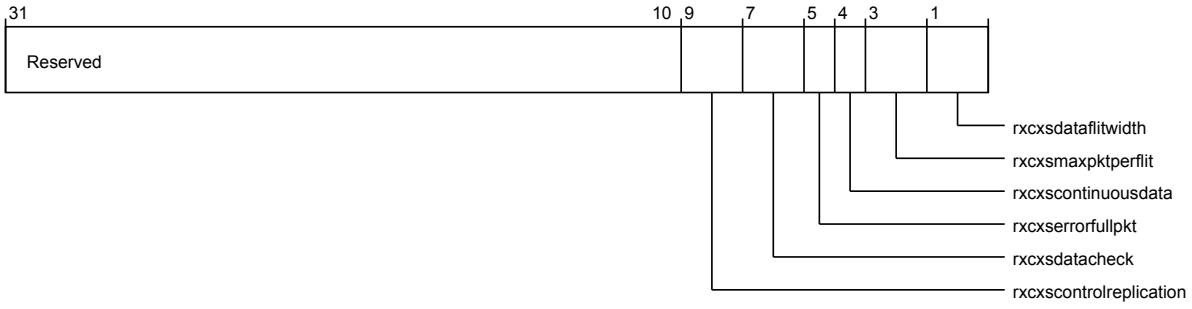


Figure 3-1267 por_cxla_por_cxla_rx_cxs_attr_capabilities (low)

The following table shows the por_cxla_rx_cxs_attr_capabilities lower register bit assignments.

Table 3-1281 por_cxla_por_cxla_rx_cxs_attr_capabilities (low)

Bits	Field name	Description	Type	Reset
31:10	Reserved	Reserved	RO	-
9:8	rxcxscontrolreplication	RX CXS control replication supported 2'b00: None 2'b01: Duplicate 2'b10: Triplicate	RO	2'b00
7:6	rxcxsdatacheck	RX CXS datacheck supported 2'b00: None 2'b01: Parity 2'b10: SECDED	RO	2'b00
5	rxcxserrorfullpkt	RX CXS error full packet supported 1'b0: False 1'b1: True	RO	1'b1
4	rxcxscontinuousdata	RX CXS continuous data supported 1'b0: False 1'b1: True	RO	1'b1
3:2	rxcxsmaxpktperflit	RX CXS maximum packets per flit supported 2'b00: 2 2'b01: 3 2'b10: 4	RO	2'b00
1:0	rxcxsdataflitwidth	RX CXS data flit width supported 2'b00: 256b 2'b01: 512b 2'b10: 1024b	RO	2'b00

por_cxla_agentid_to_linkid_reg0

Specifies the mapping of Agent ID to Link ID for Agent IDs 0 to 7.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC30

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

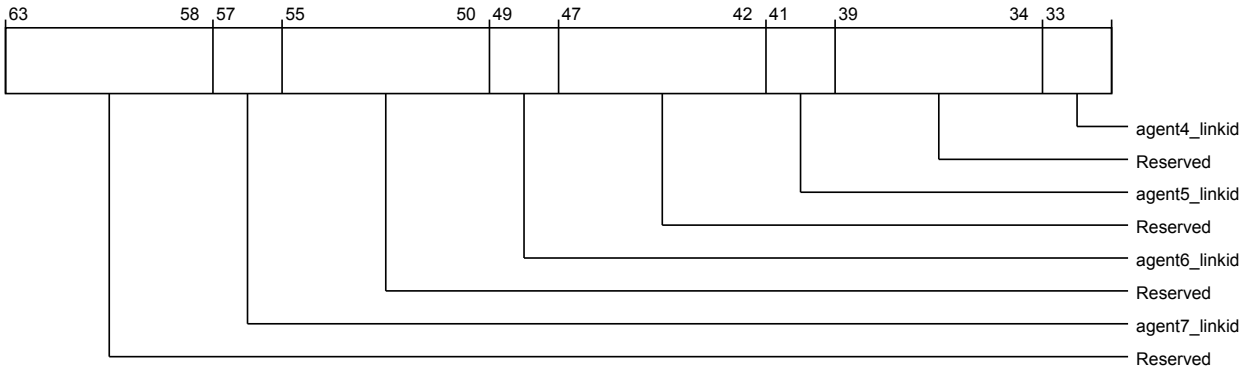


Figure 3-1268 por_cxla_por_cxla_agentid_to_linkid_reg0 (high)

The following table shows the por_cxla_agentid_to_linkid_reg0 higher register bit assignments.

Table 3-1282 por_cxla_por_cxla_agentid_to_linkid_reg0 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent7_linkid	Specifies the Link ID for Agent ID 7	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent6_linkid	Specifies the Link ID for Agent ID 6	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent5_linkid	Specifies the Link ID for Agent ID 5	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent4_linkid	Specifies the Link ID for Agent ID 4	RW	2'h0

The following image shows the lower register bit assignments.

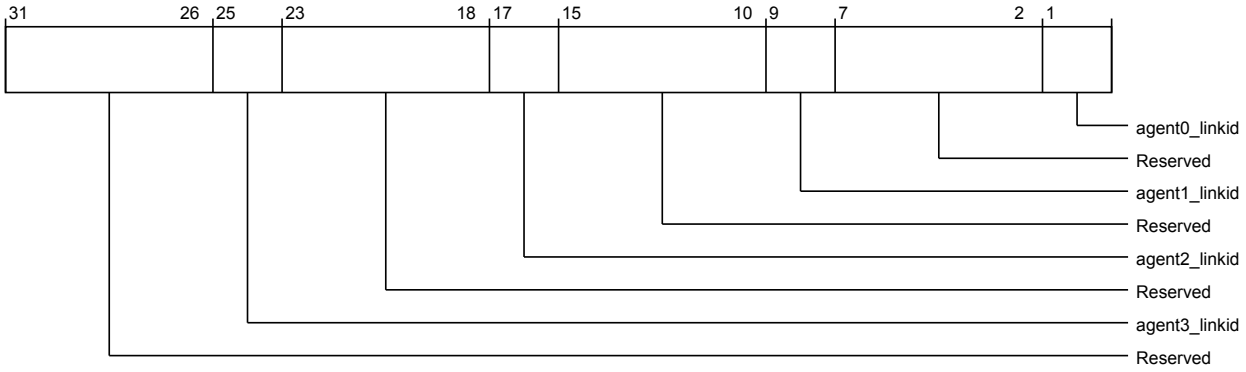


Figure 3-1269 por_cxla_por_cxla_agentid_to_linkid_reg0 (low)

The following table shows the por_cxla_agentid_to_linkid_reg0 lower register bit assignments.

Table 3-1283 por_cxla_por_cxla_agentid_to_linkid_reg0 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent3_linkid	Specifies the Link ID for Agent ID 3	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent2_linkid	Specifies the Link ID for Agent ID 2	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent1_linkid	Specifies the Link ID for Agent ID 1	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent0_linkid	Specifies the Link ID for Agent ID 0	RW	2'h0

por_cxla_agentid_to_linkid_reg1

Specifies the mapping of Agent ID to Link ID for Agent IDs 8 to 15.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC38

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

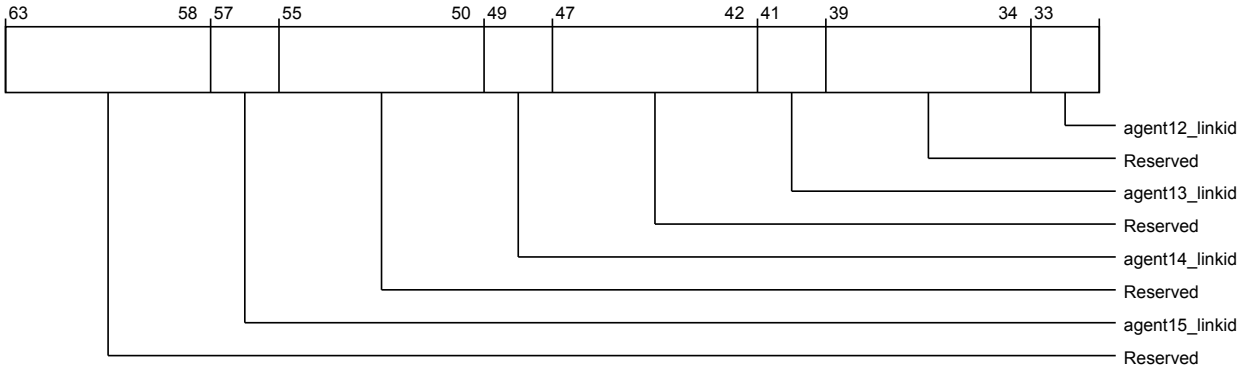


Figure 3-1270 por_cxla_por_cxla_agentid_to_linkid_reg1 (high)

The following table shows the por_cxla_agentid_to_linkid_reg1 higher register bit assignments.

Table 3-1284 por_cxla_por_cxla_agentid_to_linkid_reg1 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent15_linkid	Specifies the Link ID for Agent ID 15	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent14_linkid	Specifies the Link ID for Agent ID 14	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent13_linkid	Specifies the Link ID for Agent ID 13	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent12_linkid	Specifies the Link ID for Agent ID 12	RW	2'h0

The following image shows the lower register bit assignments.

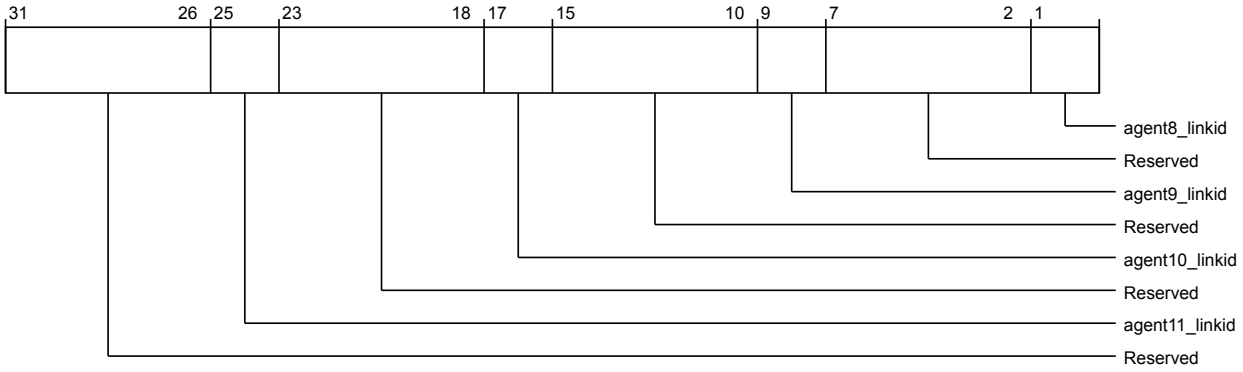


Figure 3-1271 por_cxla_por_cxla_agentid_to_linkid_reg1 (low)

The following table shows the por_cxla_agentid_to_linkid_reg1 lower register bit assignments.

Table 3-1285 por_cxla_por_cxla_agentid_to_linkid_reg1 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent11_linkid	Specifies the Link ID for Agent ID 11	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent10_linkid	Specifies the Link ID for Agent ID 10	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent9_linkid	Specifies the Link ID for Agent ID 9	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent8_linkid	Specifies the Link ID for Agent ID 8	RW	2'h0

por_cxla_agentid_to_linkid_reg2

Specifies the mapping of Agent ID to Link ID for Agent IDs 16 to 23.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC40

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

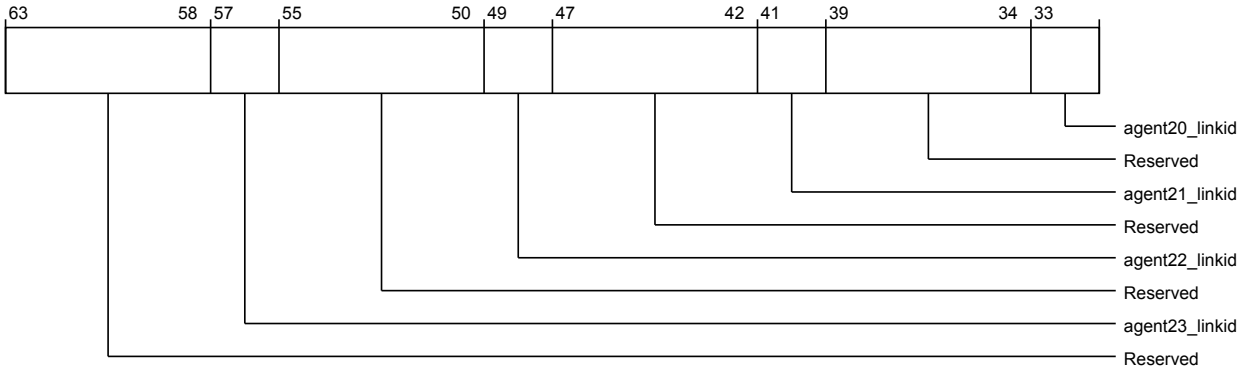


Figure 3-1272 por_cxla_por_cxla_agentid_to_linkid_reg2 (high)

The following table shows the por_cxla_agentid_to_linkid_reg2 higher register bit assignments.

Table 3-1286 por_cxla_por_cxla_agentid_to_linkid_reg2 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent23_linkid	Specifies the Link ID for Agent ID 23	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent22_linkid	Specifies the Link ID for Agent ID 22	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent21_linkid	Specifies the Link ID for Agent ID 21	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent20_linkid	Specifies the Link ID for Agent ID 20	RW	2'h0

The following image shows the lower register bit assignments.

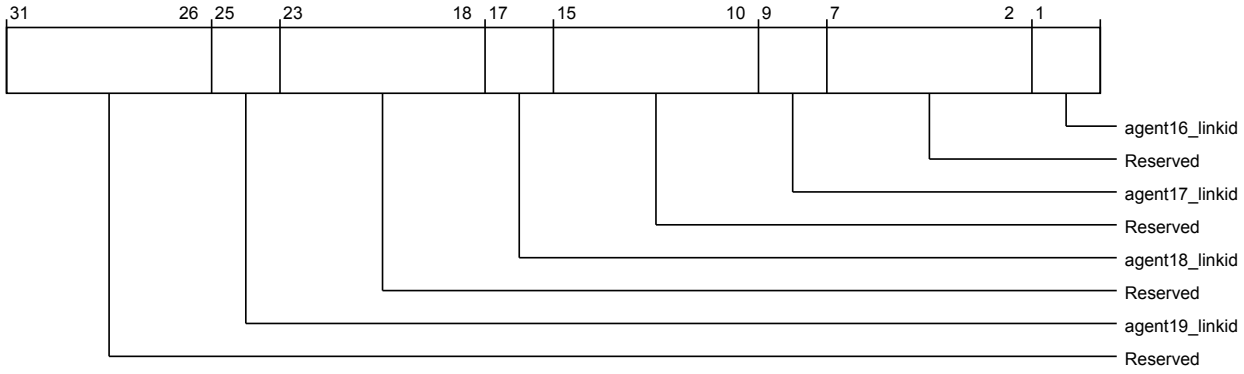


Figure 3-1273 por_cxla_por_cxla_agentid_to_linkid_reg2 (low)

The following table shows the por_cxla_agentid_to_linkid_reg2 lower register bit assignments.

Table 3-1287 por_cxla_por_cxla_agentid_to_linkid_reg2 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent19_linkid	Specifies the Link ID for Agent ID 19	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent18_linkid	Specifies the Link ID for Agent ID 18	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent17_linkid	Specifies the Link ID for Agent ID 17	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent16_linkid	Specifies the Link ID for Agent ID 16	RW	2'h0

por_cxla_agentid_to_linkid_reg3

Specifies the mapping of Agent ID to Link ID for Agent IDs 24 to 31.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC48

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

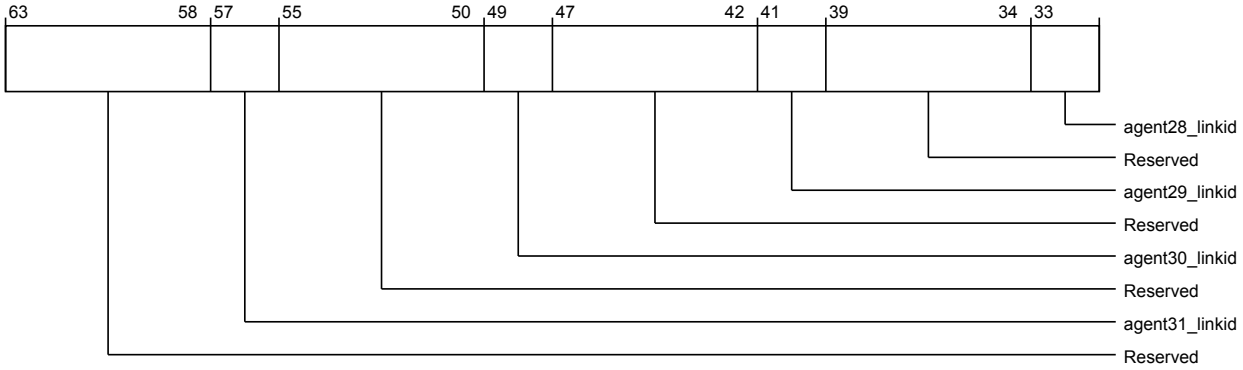


Figure 3-1274 por_cxla_por_cxla_agentid_to_linkid_reg3 (high)

The following table shows the por_cxla_agentid_to_linkid_reg3 higher register bit assignments.

Table 3-1288 por_cxla_por_cxla_agentid_to_linkid_reg3 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent31_linkid	Specifies the Link ID for Agent ID 31	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent30_linkid	Specifies the Link ID for Agent ID 30	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent29_linkid	Specifies the Link ID for Agent ID 29	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent28_linkid	Specifies the Link ID for Agent ID 28	RW	2'h0

The following image shows the lower register bit assignments.

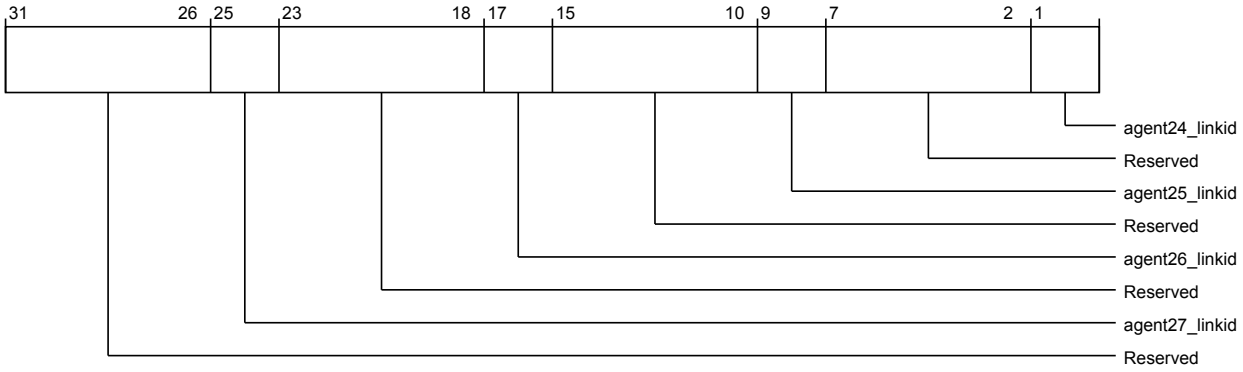


Figure 3-1275 por_cxla_por_cxla_agentid_to_linkid_reg3 (low)

The following table shows the por_cxla_agentid_to_linkid_reg3 lower register bit assignments.

Table 3-1289 por_cxla_por_cxla_agentid_to_linkid_reg3 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent27_linkid	Specifies the Link ID for Agent ID 27	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent26_linkid	Specifies the Link ID for Agent ID 26	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent25_linkid	Specifies the Link ID for Agent ID 25	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent24_linkid	Specifies the Link ID for Agent ID 24	RW	2'h0

por_cxla_agentid_to_linkid_reg4

Specifies the mapping of Agent ID to Link ID for Agent IDs 32 to 39.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC50

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

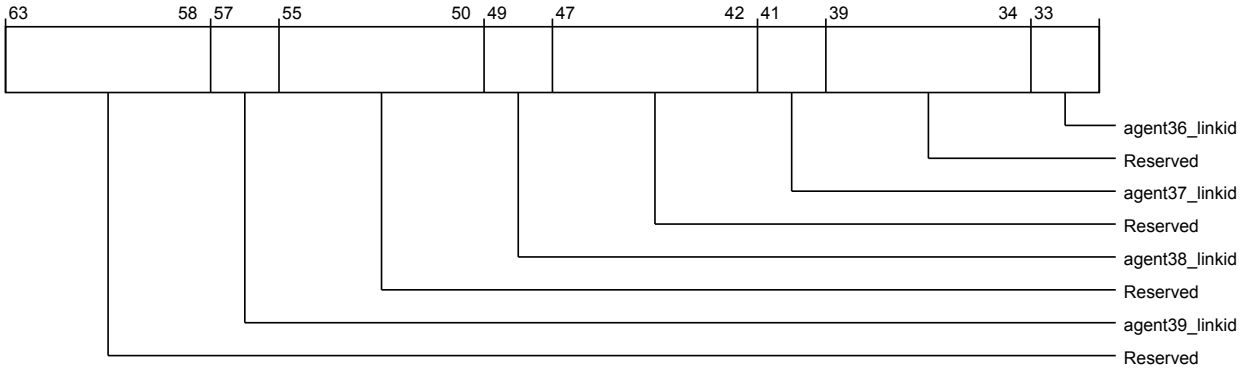


Figure 3-1276 por_cxla_por_cxla_agentid_to_linkid_reg4 (high)

The following table shows the por_cxla_agentid_to_linkid_reg4 higher register bit assignments.

Table 3-1290 por_cxla_por_cxla_agentid_to_linkid_reg4 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent39_linkid	Specifies the Link ID for Agent ID 39	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent38_linkid	Specifies the Link ID for Agent ID 38	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent37_linkid	Specifies the Link ID for Agent ID 37	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent36_linkid	Specifies the Link ID for Agent ID 36	RW	2'h0

The following image shows the lower register bit assignments.

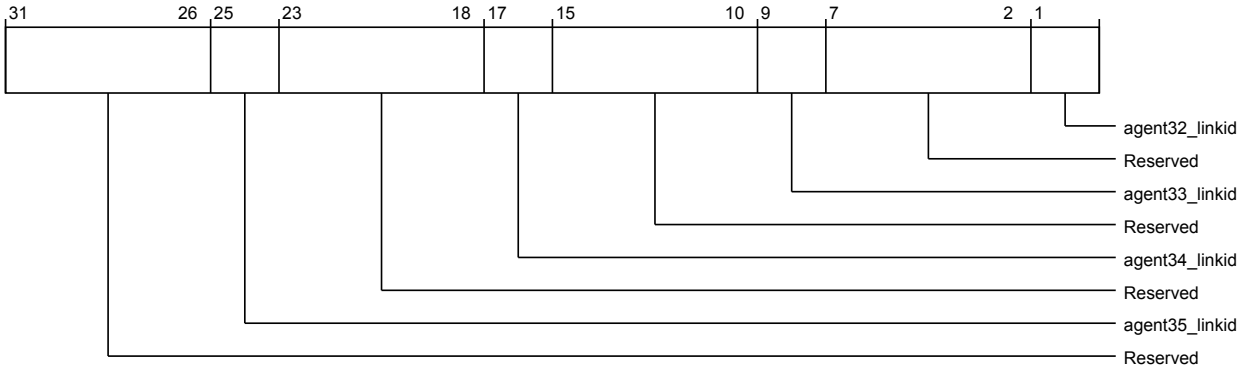


Figure 3-1277 por_cxla_por_cxla_agentid_to_linkid_reg4 (low)

The following table shows the por_cxla_agentid_to_linkid_reg4 lower register bit assignments.

Table 3-1291 por_cxla_por_cxla_agentid_to_linkid_reg4 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent35_linkid	Specifies the Link ID for Agent ID 35	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent34_linkid	Specifies the Link ID for Agent ID 34	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent33_linkid	Specifies the Link ID for Agent ID 33	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent32_linkid	Specifies the Link ID for Agent ID 32	RW	2'h0

por_cxla_agentid_to_linkid_reg5

Specifies the mapping of Agent ID to Link ID for Agent IDs 40 to 47.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC58

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

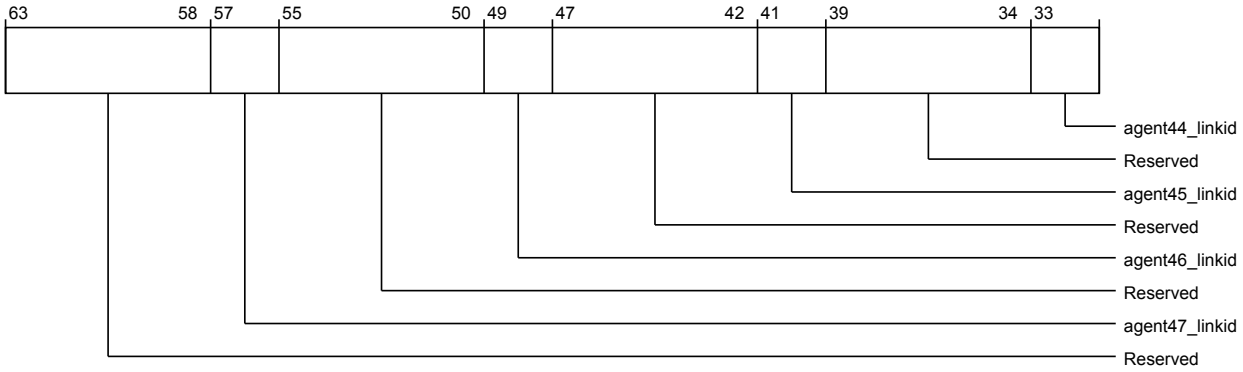


Figure 3-1278 por_cxla_por_cxla_agentid_to_linkid_reg5 (high)

The following table shows the por_cxla_agentid_to_linkid_reg5 higher register bit assignments.

Table 3-1292 por_cxla_por_cxla_agentid_to_linkid_reg5 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent47_linkid	Specifies the Link ID for Agent ID 47	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent46_linkid	Specifies the Link ID for Agent ID 46	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent45_linkid	Specifies the Link ID for Agent ID 45	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent44_linkid	Specifies the Link ID for Agent ID 44	RW	2'h0

The following image shows the lower register bit assignments.

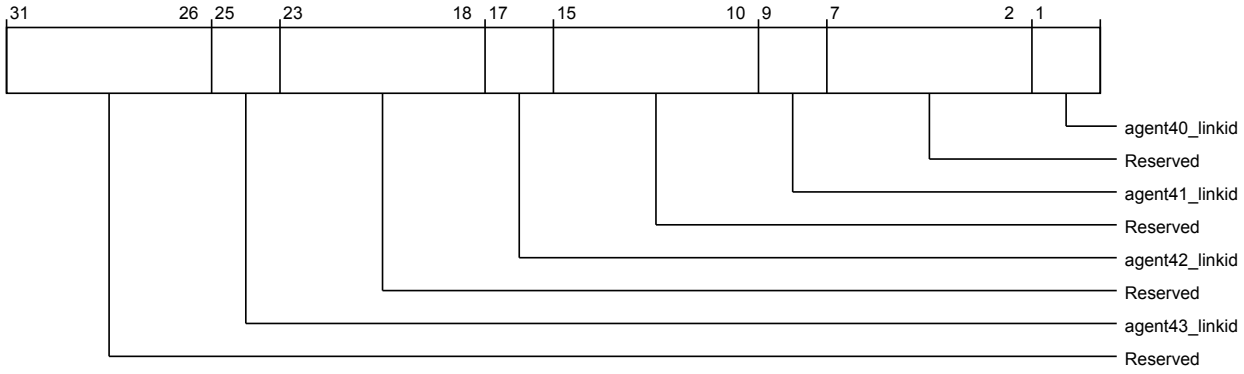


Figure 3-1279 por_cxla_por_cxla_agentid_to_linkid_reg5 (low)

The following table shows the por_cxla_agentid_to_linkid_reg5 lower register bit assignments.

Table 3-1293 por_cxla_por_cxla_agentid_to_linkid_reg5 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent43_linkid	Specifies the Link ID for Agent ID 43	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent42_linkid	Specifies the Link ID for Agent ID 42	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent41_linkid	Specifies the Link ID for Agent ID 41	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent40_linkid	Specifies the Link ID for Agent ID 40	RW	2'h0

por_cxla_agentid_to_linkid_reg6

Specifies the mapping of Agent ID to Link ID for Agent IDs 48 to 55.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC60

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

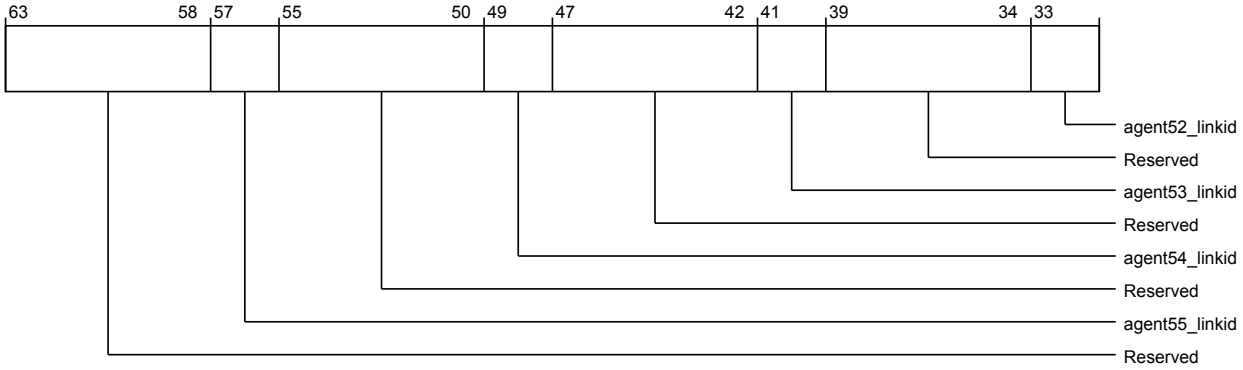


Figure 3-1280 por_cxla_por_cxla_agentid_to_linkid_reg6 (high)

The following table shows the por_cxla_agentid_to_linkid_reg6 higher register bit assignments.

Table 3-1294 por_cxla_por_cxla_agentid_to_linkid_reg6 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent55_linkid	Specifies the Link ID for Agent ID 55	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent54_linkid	Specifies the Link ID for Agent ID 54	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent53_linkid	Specifies the Link ID for Agent ID 53	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent52_linkid	Specifies the Link ID for Agent ID 52	RW	2'h0

The following image shows the lower register bit assignments.

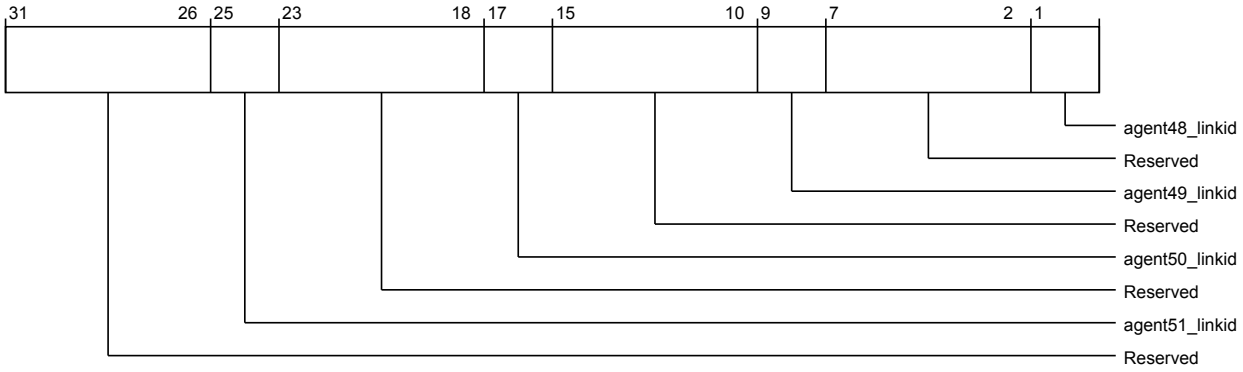


Figure 3-1281 por_cxla_por_cxla_agentid_to_linkid_reg6 (low)

The following table shows the por_cxla_agentid_to_linkid_reg6 lower register bit assignments.

Table 3-1295 por_cxla_por_cxla_agentid_to_linkid_reg6 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent51_linkid	Specifies the Link ID for Agent ID 51	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent50_linkid	Specifies the Link ID for Agent ID 50	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent49_linkid	Specifies the Link ID for Agent ID 49	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent48_linkid	Specifies the Link ID for Agent ID 48	RW	2'h0

por_cxla_agentid_to_linkid_reg7

Specifies the mapping of Agent ID to Link ID for Agent IDs 56 to 63.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC68

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

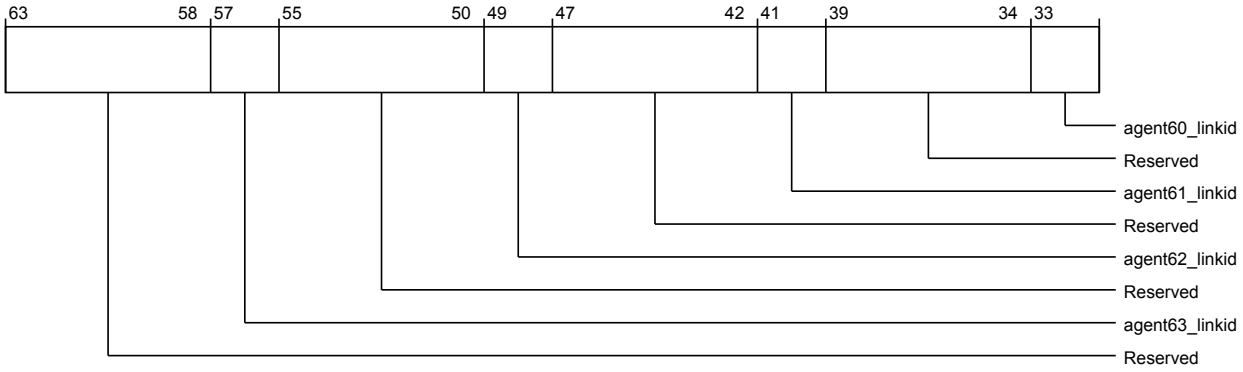


Figure 3-1282 por_cxla_por_cxla_agentid_to_linkid_reg7 (high)

The following table shows the por_cxla_agentid_to_linkid_reg7 higher register bit assignments.

Table 3-1296 por_cxla_por_cxla_agentid_to_linkid_reg7 (high)

Bits	Field name	Description	Type	Reset
63:58	Reserved	Reserved	RO	-
57:56	agent63_linkid	Specifies the Link ID for Agent ID 63	RW	2'h0
55:50	Reserved	Reserved	RO	-
49:48	agent62_linkid	Specifies the Link ID for Agent ID 62	RW	2'h0
47:42	Reserved	Reserved	RO	-
41:40	agent61_linkid	Specifies the Link ID for Agent ID 61	RW	2'h0
39:34	Reserved	Reserved	RO	-
33:32	agent60_linkid	Specifies the Link ID for Agent ID 60	RW	2'h0

The following image shows the lower register bit assignments.

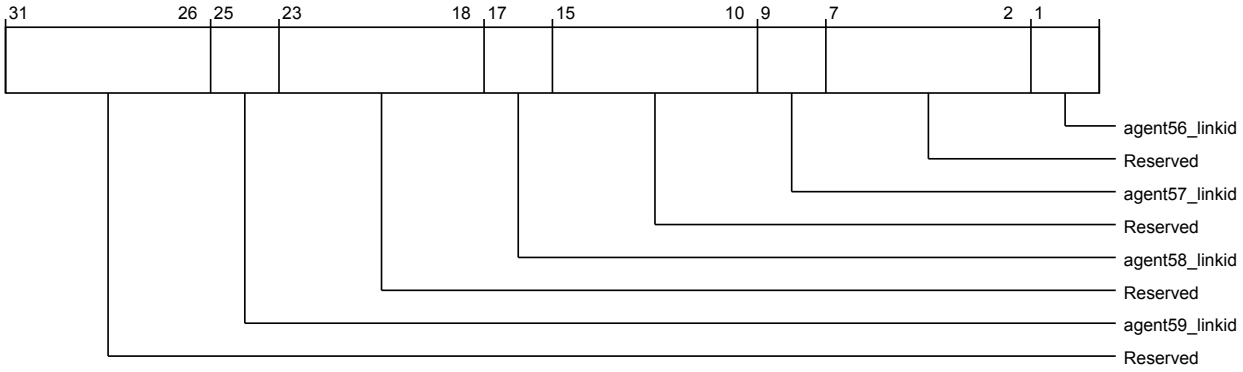


Figure 3-1283 por_cxla_por_cxla_agentid_to_linkid_reg7 (low)

The following table shows the por_cxla_agentid_to_linkid_reg7 lower register bit assignments.

Table 3-1297 por_cxla_por_cxla_agentid_to_linkid_reg7 (low)

Bits	Field name	Description	Type	Reset
31:26	Reserved	Reserved	RO	-
25:24	agent59_linkid	Specifies the Link ID for Agent ID 59	RW	2'h0
23:18	Reserved	Reserved	RO	-
17:16	agent58_linkid	Specifies the Link ID for Agent ID 58	RW	2'h0
15:10	Reserved	Reserved	RO	-
9:8	agent57_linkid	Specifies the Link ID for Agent ID 57	RW	2'h0
7:2	Reserved	Reserved	RO	-
1:0	agent56_linkid	Specifies the Link ID for Agent ID 56	RW	2'h0

por_cxla_agentid_to_linkid_val

Specifies which Agent ID to Link ID mappings are valid.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hC70

Register reset 64'b0

Usage constraints Only accessible by secure accesses.

Secure group override por_cxla_secure_register_groups_override.linkid_ctl

The following image shows the higher register bit assignments.

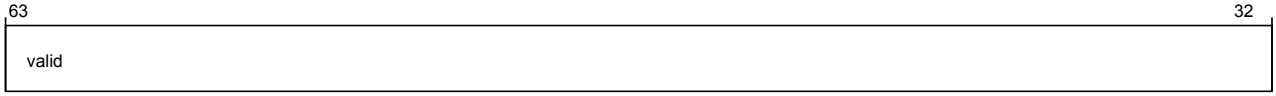


Figure 3-1284 por_cxla_por_cxla_agentid_to_linkid_val (high)

The following table shows the por_cxla_agentid_to_linkid_val higher register bit assignments.

Table 3-1298 por_cxla_por_cxla_agentid_to_linkid_val (high)

Bits	Field name	Description	Type	Reset
63:32	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

The following image shows the lower register bit assignments.

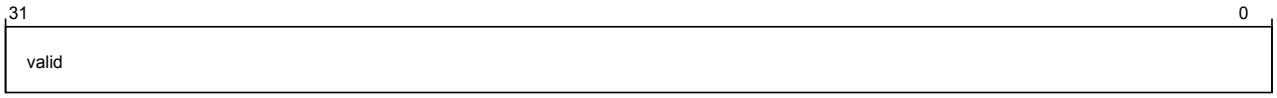


Figure 3-1285 por_cxla_por_cxla_agentid_to_linkid_val (low)

The following table shows the por_cxla_agentid_to_linkid_val lower register bit assignments.

Table 3-1299 por_cxla_por_cxla_agentid_to_linkid_val (low)

Bits	Field name	Description	Type	Reset
31:0	valid	Specifies whether the Link ID is valid; bit number corresponds to logical Agent ID number (from 0 to 63)	RW	63'h0

por_cxla_linkid_to_pcie_bus_num

Specifies the mapping of CCIX Link ID to PCIe bus number.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hC78
Register reset 64'b0
Usage constraints Only accessible by secure accesses.

The following image shows the higher register bit assignments.

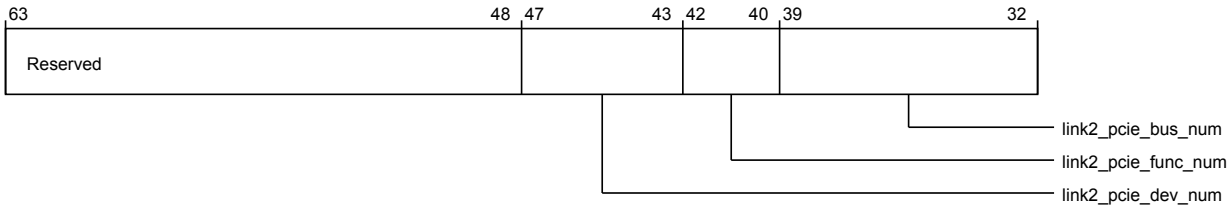


Figure 3-1286 por_cxla_por_cxla_linkid_to_pcie_bus_num (high)

The following table shows the por_cxla_linkid_to_pcie_bus_num higher register bit assignments.

Table 3-1300 por_cxla_por_cxla_linkid_to_pcie_bus_num (high)

Bits	Field name	Description	Type	Reset
63:48	Reserved	Reserved	RO	-
47:43	link2_pcie_dev_num	PCIe Device number for Link ID 2	RW	5'h00
42:40	link2_pcie_func_num	PCIe Function number for Link ID 2	RW	3'h0
39:32	link2_pcie_bus_num	PCIe bus number for Link ID 2	RW	8'h00

The following image shows the lower register bit assignments.

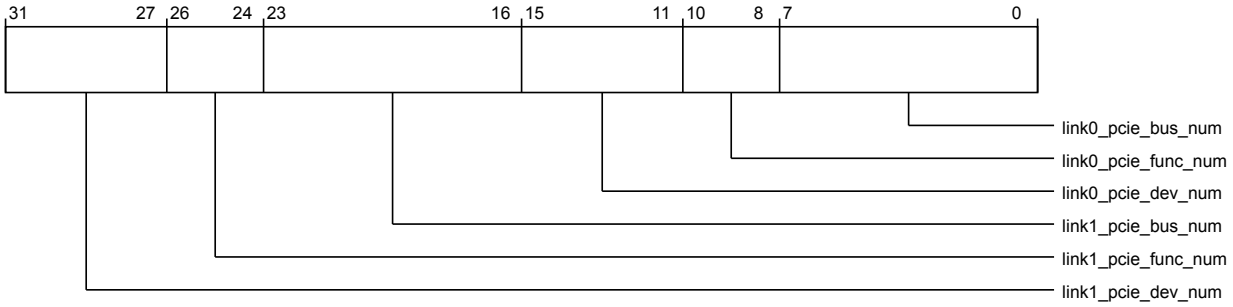


Figure 3-1287 por_cxla_por_cxla_linkid_to_pcie_bus_num (low)

The following table shows the por_cxla_linkid_to_pcie_bus_num lower register bit assignments.

Table 3-1301 por_cxla_por_cxla_linkid_to_pcie_bus_num (low)

Bits	Field name	Description	Type	Reset
31:27	link1_pcie_dev_num	PCIe Device number for Link ID 1	RW	5'h00
26:24	link1_pcie_func_num	PCIe Function number for Link ID 1	RW	3'h0
23:16	link1_pcie_bus_num	PCIe bus number for Link ID 1	RW	8'h00
15:11	link0_pcie_dev_num	PCIe Device number for Link ID 0	RW	5'h00
10:8	link0_pcie_func_num	PCIe Function number for Link ID 0	RW	3'h0
7:0	link0_pcie_bus_num	PCIe bus number for Link ID 0	RW	8'h00

por_cxla_permsg_pyld_0_63

Contains bits[63:0] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD00
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

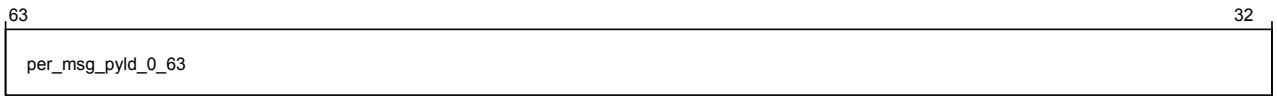


Figure 3-1288 por_cxla_por_cxla_permsg_pyld_0_63 (high)

The following table shows the por_cxla_permsg_pyld_0_63 higher register bit assignments.

Table 3-1302 por_cxla_por_cxla_permsg_pyld_0_63 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_0_63	Protocol Error Msg Payload[63:0]	RW	64'b0

The following image shows the lower register bit assignments.

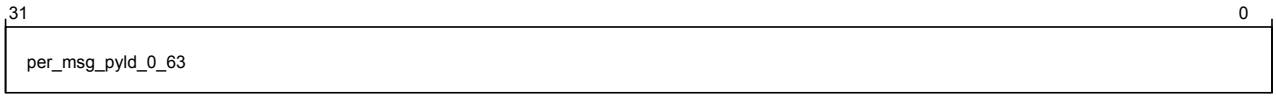


Figure 3-1289 por_cxla_por_cxla_permsg_pyld_0_63 (low)

The following table shows the por_cxla_permsg_pyld_0_63 lower register bit assignments.

Table 3-1303 por_cxla_por_cxla_permsg_pyld_0_63 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_0_63	Protocol Error Msg Payload[63:0]	RW	64'b0

por_cxla_permsg_pyld_64_127

Contains bits[127:64] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD08
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

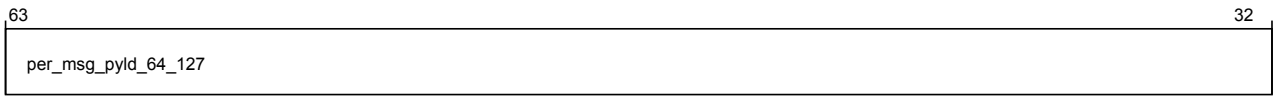


Figure 3-1290 por_cxla_por_cxla_permsg_pyld_64_127 (high)

The following table shows the por_cxla_permsg_pyld_64_127 higher register bit assignments.

Table 3-1304 por_cxla_por_cxla_permsg_pyld_64_127 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_64_127	Protocol Error Msg Payload[127:64]	RW	64'b0

The following image shows the lower register bit assignments.

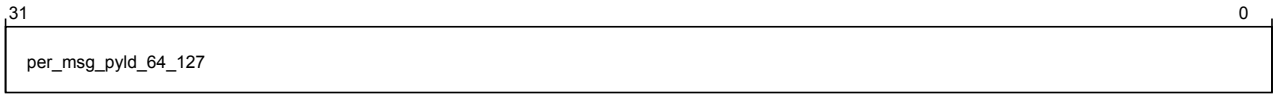


Figure 3-1291 por_cxla_por_cxla_permsg_pyld_64_127 (low)

The following table shows the por_cxla_permsg_pyld_64_127 lower register bit assignments.

Table 3-1305 por_cxla_por_cxla_permsg_pyld_64_127 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_64_127	Protocol Error Msg Payload[127:64]	RW	64'b0

por_cxla_permsg_pyld_128_191

Contains bits[192:128] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD10
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

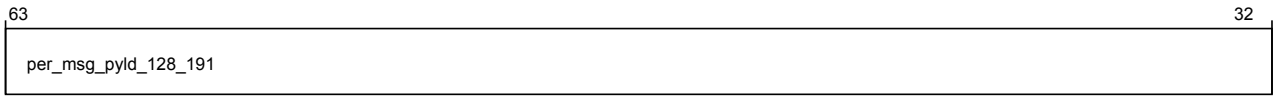


Figure 3-1292 por_cxla_por_cxla_permsg_pyld_128_191 (high)

The following table shows the por_cxla_permsg_pyld_128_191 higher register bit assignments.

Table 3-1306 por_cxla_por_cxla_permsg_pyld_128_191 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_128_191	Protocol Error Msg Payload[191:128]	RW	64'b0

The following image shows the lower register bit assignments.

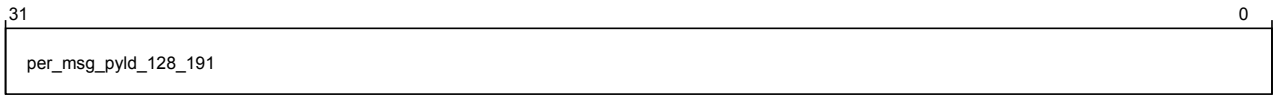


Figure 3-1293 por_cxla_por_cxla_permsg_pyld_128_191 (low)

The following table shows the por_cxla_permsg_pyld_128_191 lower register bit assignments.

Table 3-1307 por_cxla_por_cxla_permsg_pyld_128_191 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_128_191	Protocol Error Msg Payload[191:128]	RW	64'b0

por_cxla_permsg_pyld_192_255

Contains bits[255:192] of CCIX Protocol Error (PER) Message payload.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD18
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

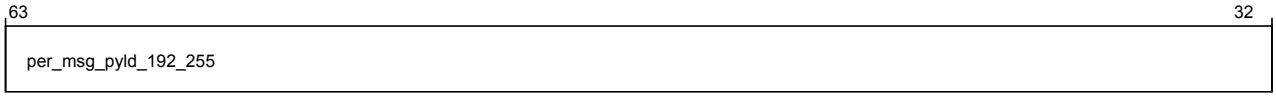


Figure 3-1294 por_cxla_por_cxla_permsg_pyld_192_255 (high)

The following table shows the por_cxla_permsg_pyld_192_255 higher register bit assignments.

Table 3-1308 por_cxla_por_cxla_permsg_pyld_192_255 (high)

Bits	Field name	Description	Type	Reset
63:32	per_msg_pyld_192_255	Protocol Error Msg Payload[255:192]	RW	64'b0

The following image shows the lower register bit assignments.

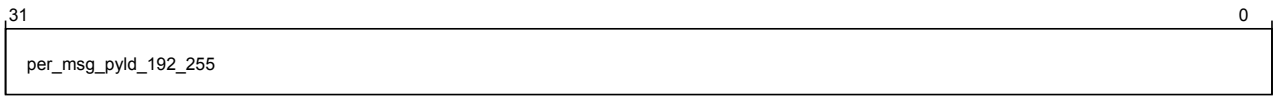


Figure 3-1295 por_cxla_por_cxla_permsg_pyld_192_255 (low)

The following table shows the por_cxla_permsg_pyld_192_255 lower register bit assignments.

Table 3-1309 por_cxla_por_cxla_permsg_pyld_192_255 (low)

Bits	Field name	Description	Type	Reset
31:0	per_msg_pyld_192_255	Protocol Error Msg Payload[255:192]	RW	64'b0

por_cxla_permsg_ctl

Contains Control bits to trigger CCIX Protocol Error (PER) Message.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'hD20
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

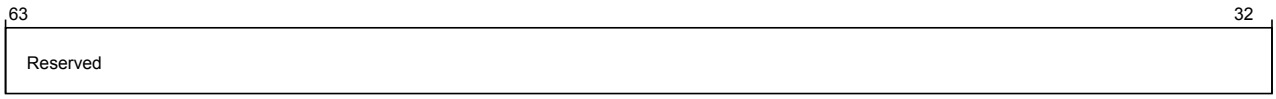


Figure 3-1296 por_cxla_por_cxla_permsg_ctl (high)

The following table shows the por_cxla_permsg_ctl higher register bit assignments.

Table 3-1310 por_cxla_por_cxla_permsg_ctl (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

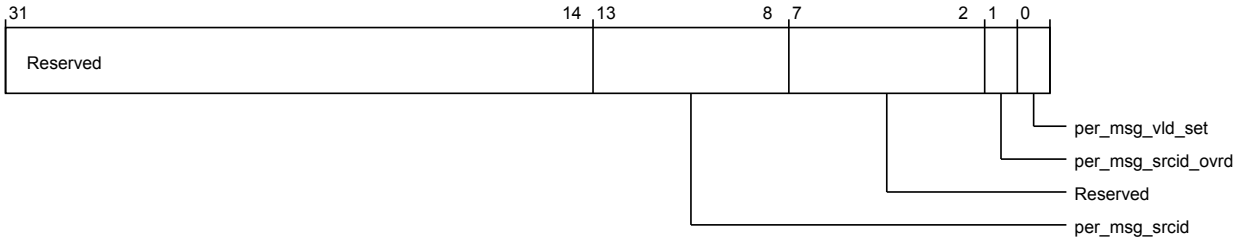


Figure 3-1297 por_cxla_por_cxla_permsg_ctl (low)

The following table shows the por_cxla_permsg_ctl lower register bit assignments.

Table 3-1311 por_cxla_por_cxla_permsg_ctl (low)

Bits	Field name	Description	Type	Reset
31:14	Reserved	Reserved	RO	-
13:8	per_msg_srcid	Contains Source ID used on CCIX Protocol Error Msg. Used when per_msg_srcid_ovrd is set.	RW	6'b0
7:2	Reserved	Reserved	RO	-
1	per_msg_srcid_ovrd	When set, overrides the Source ID on Protocol Error Msg by value specified in this register. Or else the source ID from payload[55:48] is used.	RW	1'b0
0	per_msg_vld_set	When set, sends CCIX Protocol Error Msg. Must be cleared after the current error is processed and before a new error message is triggered	RW	1'b0

por_cxla_err_agent_id

Contains Error Agent ID. Must be programmed by CCIX discovery s/w. Used as TargetID on CCIX Protocol Error (PER) Message.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'hD28

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

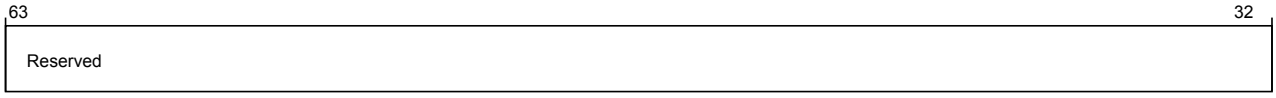


Figure 3-1298 por_cxla_por_cxla_err_agent_id (high)

The following table shows the por_cxla_err_agent_id higher register bit assignments.

Table 3-1312 por_cxla_por_cxla_err_agent_id (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

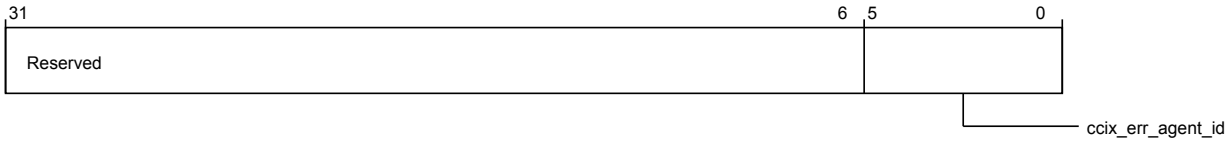


Figure 3-1299 por_cxla_por_cxla_err_agent_id (low)

The following table shows the por_cxla_err_agent_id lower register bit assignments.

Table 3-1313 por_cxla_por_cxla_err_agent_id (low)

Bits	Field name	Description	Type	Reset
31:6	Reserved	Reserved	RO	-
5:0	ccix_err_agent_id	CCIX Error AgentID	RW	6'b0

por_cxla_pmu_event_sel

Specifies the PMU event to be counted.

Its characteristics are:

Type RW

Register width (Bits) 64

Address offset 14'h2000

Register reset 64'b0

Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

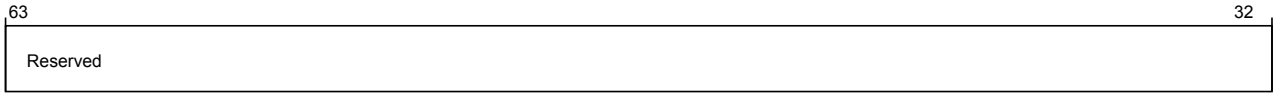


Figure 3-1300 por_cxla_por_cxla_pmu_event_sel (high)

The following table shows the por_cxla_pmu_event_sel higher register bit assignments.

Table 3-1314 por_cxla_por_cxla_pmu_event_sel (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

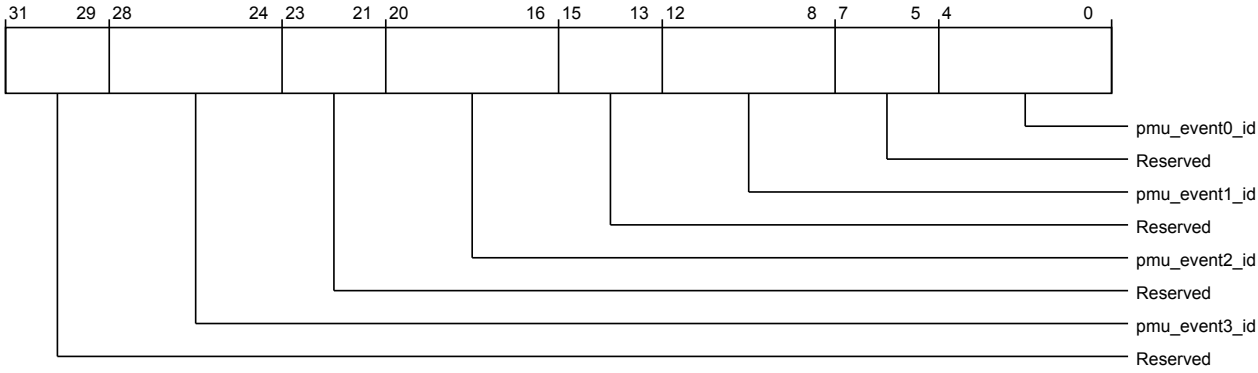


Figure 3-1301 por_cxla_por_cxla_pmu_event_sel (low)

The following table shows the por_cxla_pmu_event_sel lower register bit assignments.

Table 3-1315 por_cxla_por_cxla_pmu_event_sel (low)

Bits	Field name	Description	Type	Reset
31:29	Reserved	Reserved	RO	-
28:24	pmu_event3_id	CXLA PMU Event 3 ID; see pmu_event0_id for encodings	RW	5'b0
23:21	Reserved	Reserved	RO	-
20:16	pmu_event2_id	CXLA PMU Event 2 ID; see pmu_event0_id for encodings	RW	5'b0
15:13	Reserved	Reserved	RO	-
12:8	pmu_event1_id	CXLA PMU Event 1 ID; see pmu_event0_id for encodings	RW	5'b0

Table 3-1315 por_cxla_por_cxla_pmu_event_sel (low) (continued)

Bits	Field name	Description	Type	Reset
7:5	Reserved	Reserved	RO	-
4:0	pmu_event0_id	CXLA PMU Event 0 ID 5'h00: No event 5'h01: RX TLP for Link 0 5'h02: RX TLP for Link 1 5'h03: RX TLP for Link 2 5'h04: TX TLP for Link 0 5'h05: TX TLP for Link 1 5'h06: TX TLP for Link 2 5'h07: RX CXS for Link 0 5'h08: RX CXS for Link 1 5'h09: RX CXS for Link 2 5'h0A: TX CXS for Link 0 5'h0B: TX CXS for Link 1 5'h0B: TX CXS for Link 2 5'h0D: Average RX TLP size in DWs 5'h0E: Average TX TLP size in DWs 5'h0F: Average RX TLP size in CCIX messages 5'h10: Average TX TLP size in CCIX messages 5'h11: Average size of RX CXS in DWs within a beat 5'h12: Average size of TX CXS in DWs within a beat 5'h13: TX CXS link credit backpressure 5'h14: RX TLP buffer full and backpressured 5'h15: TX TLP buffer full and backpressured 5'h16: Average latency to process an RX TLP 5'h17: Average latency to form a TX TLP	RW	5'b0

por_cxla_pmu_config

Configures the CXLA PMU.

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2210
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

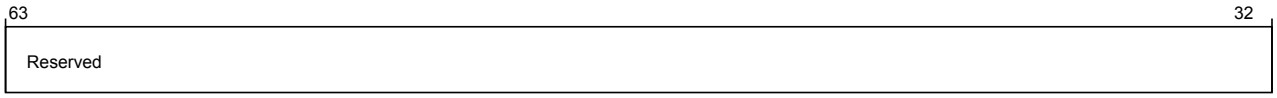


Figure 3-1302 por_cxla_por_cxla_pmu_config (high)

The following table shows the por_cxla_pmu_config higher register bit assignments.

Table 3-1316 por_cxla_por_cxla_pmu_config (high)

Bits	Field name	Description	Type	Reset
63:32	Reserved	Reserved	RO	-

The following image shows the lower register bit assignments.

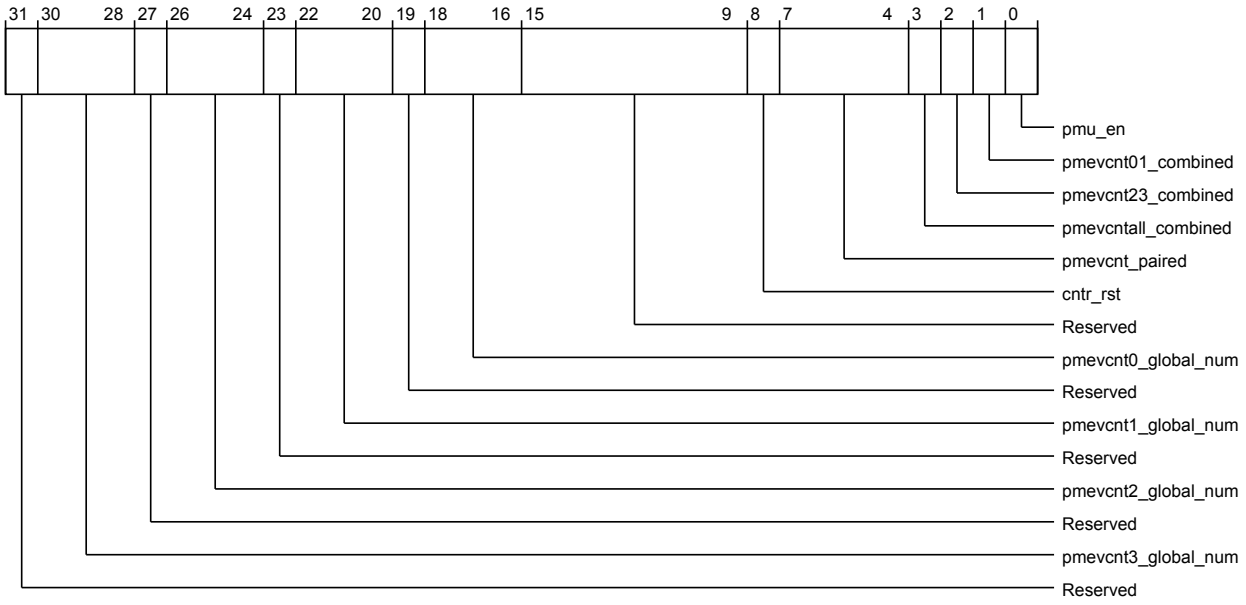


Figure 3-1303 por_cxla_por_cxla_pmu_config (low)

The following table shows the por_cxla_pmu_config lower register bit assignments.

Table 3-1317 por_cxla_por_cxla_pmu_config (low)

Bits	Field name	Description	Type	Reset
31	Reserved	Reserved	RO	-
30:28	pmevcnt3_global_num	Global counter to pair with PMU counter 3; see pmevcnt0_global_num for encodings	RW	3'b0
27	Reserved	Reserved	RO	-
26:24	pmevcnt2_global_num	Global counter to pair with PMU counter 2; see pmevcnt0_global_num for encodings	RW	3'b0
23	Reserved	Reserved	RO	-
22:20	pmevcnt1_global_num	Global counter to pair with PMU counter 1; see pmevcnt0_global_num for encodings	RW	3'b0

Table 3-1317 por_cxla_por_cxla_pmu_config (low) (continued)

Bits	Field name	Description	Type	Reset
19	Reserved	Reserved	RO	-
18:16	pmevcnt0_global_num	Global counter to pair with PMU counter 0 3'b000: Global PMU event counter A 3'b001: Global PMU event counter B 3'b010: Global PMU event counter C 3'b011: Global PMU event counter D 3'b100: Global PMU event counter E 3'b101: Global PMU event counter F 3'b110: Global PMU event counter G 3'b111: Global PMU event counter H	RW	3'b0
15:9	Reserved	Reserved	RO	-
8	cntr_rst	Enables clearing of live counters upon assertion of snapshot	RW	1'b0
7:4	pmevcnt_paired	PMU local counter paired with global counter	RW	4'b0
3	pmevcntall_combined	Enables combination of all PMU counters (0, 1, 2, 3) NOTE: When set, pmevcnt01_combined and pmevcnt23_combined have no effect.	RW	1'b0
2	pmevcnt23_combined	Enables combination of PMU counters 2 and 3	RW	1'b0
1	pmevcnt01_combined	Enables combination of PMU counters 0 and 1	RW	1'b0
0	pmu_en	CXLA PMU enable NOTE: All other fields in this register are valid only if this bit is set.	RW	1'b0

por_cxla_pmevcnt

Contains all PMU event counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2220
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

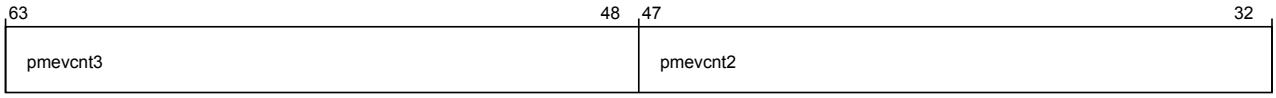


Figure 3-1304 por_cxla_por_cxla_pmevcnt (high)

The following table shows the por_cxla_pmevcnt higher register bit assignments.

Table 3-1318 por_cxla_por_cxla_pmevcnt (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcnt3	PMU event counter 3	RW	16'h0000
47:32	pmevcnt2	PMU event counter 2	RW	16'h0000

The following image shows the lower register bit assignments.

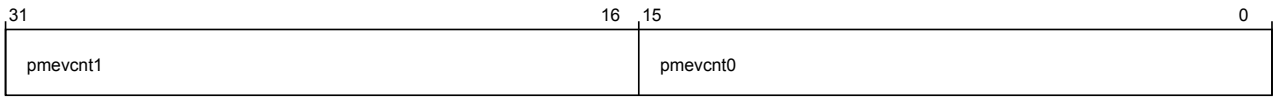


Figure 3-1305 por_cxla_por_cxla_pmevcnt (low)

The following table shows the por_cxla_pmevcnt lower register bit assignments.

Table 3-1319 por_cxla_por_cxla_pmevcnt (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcnt1	PMU event counter 1	RW	16'h0000
15:0	pmevcnt0	PMU event counter 0	RW	16'h0000

por_cxla_pmevcntsr

Functions as the PMU event counter shadow register for all counters (0, 1, 2, 3).

Its characteristics are:

Type RW
Register width (Bits) 64
Address offset 14'h2240
Register reset 64'b0
Usage constraints There are no usage constraints.

The following image shows the higher register bit assignments.

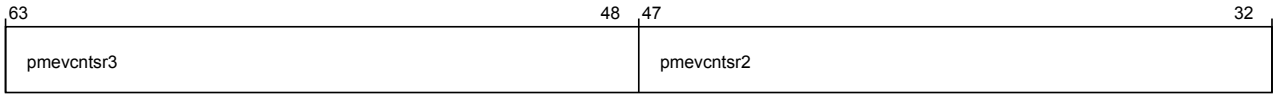


Figure 3-1306 por_cxla_por_cxla_pmevcntsr (high)

The following table shows the por_cxla_pmevcntsr higher register bit assignments.

Table 3-1320 por_cxla_por_cxla_pmevcntsr (high)

Bits	Field name	Description	Type	Reset
63:48	pmevcntsr3	PMU event counter 3 shadow register	RW	16'h0000
47:32	pmevcntsr2	PMU event counter 2 shadow register	RW	16'h0000

The following image shows the lower register bit assignments.

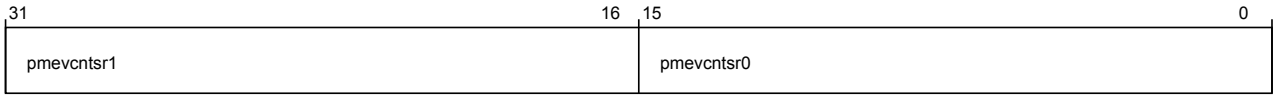


Figure 3-1307 por_cxla_por_cxla_pmevcntsr (low)

The following table shows the por_cxla_pmevcntsr lower register bit assignments.

Table 3-1321 por_cxla_por_cxla_pmevcntsr (low)

Bits	Field name	Description	Type	Reset
31:16	pmevcntsr1	PMU event counter 1 shadow register	RW	16'h0000
15:0	pmevcntsr0	PMU event counter 0 shadow register	RW	16'h0000

3.4 CMN-600 programming

This section contains CMN-600 programming information.

This section contains the following subsections:

3.4.1 Boot-time programming requirements

After reset, CMN-600 uses a default configuration that accesses the HN-D ACE-Lite master interface (to access boot flash) and the configuration registers. An RN-F, or master behind an RN-I, must then access the configuration registers to configure CMN-600 before there is broader access to components such as HN-F or SN.

The following example assumes a system control processor (SCP) is performing the CMN-600 configuration.

- The SCP boots, either from local memory or through CMN-600 memory accesses targeting memory behind the HN-D:
  - All other masters are held in reset or otherwise issue no requests to CMN-600.
  - The HN-D is identified through straps on the RN SAM.
- The SCP discovers the system, if needed.
- The SCP determines the desired address map and corresponding SAM register values.
- The SCP performs a sequence to remap the configuration register space, if needed.
  - Drain all requests in flight by waiting for their responses.
  - Issue a single 64-bit store to a PERIPHBASE register behind the HN-D. This register would be in logic external to CMN-600 and an update would cause the signal values on the CFGM_PERIPHBASE input to change.
  - Wait for the response for that store.
- The SCP uses CMN-600 configuration register writes to program the SAM for all HN-Fs, if needed.
- The SCP uses the CMN-600 configuration registers to program the SAM for all RNs including the one being used by the SCP.

  Note

  RN-F ESAM types are not able to block transactions before RN SAM programming and transactions must be blocked by some external mechanism.

  - The SCP's SAM is then programmed as the rest of the system. The last step is to set a bit that indicates using the programmed address map instead of using the default map.
- At this point, the SCP can make general accesses anywhere in the address space and other masters can begin issuing requests.

3.4.2 Runtime programming requirements

This section describes the requirements for programming during runtime.

The hardware for handling RN membership in the coherence domain or DVM domain has been shifted to the XP to which the RN is attached. A low-level four-phase handshake mechanism (SYSCOREQ/SYSCOACK) has been added to allow quick and local entry to and exit from snoop and DVM domains. No communication with central hardware resources is needed. When a block is removed from the coherence or DVM domain, the XP acts as a protocol agent to give a generic response to any snoop or DVM messages.

For legacy devices that do not support the SYSCOREQ/SYSCOACK mechanism, direct configuration writes to the XP by software can trigger the same mechanism. Refer to *2.30 RN entry to and exit from Snoop and DVM domains* on page 2-163 for more details.

3.5 CML programming

The system must be programmed to enable correct operation with CML.

This section contains the following subsections:

3.5.1 CMN-600 CML (CCIX) Related Programmable Registers

This section contains a list of CML programmable registers.

CXRA:

- RA SAM
  - **por_cxg_ra_sam_addr_region_reg<X>**
- LDID to RAID LUT
  - **por_cxg_ra_rnf_ldid_to_raid_reg<X>**
  - **por_cxg_ra_rnd_ldid_to_raid_reg<X>**
  - **por_cxg_ra_rni_ldid_to_raid_reg<X>**
  - **por_cxg_ra_rnf_ldid_to_raid_val**
  - **por_cxg_ra_rni_ldid_to_raid_val**
  - **por_cxg_ra_rnd_ldid_to_raid_val**
- Remote AgentID (RAID/HAID) to LinkID LUT
  - **por_cxg_ra_agentid_to_linkid_reg<X>**
  - **por_cxg_ra_agentid_to_linkid_val**
- CCIX protocol link control and status
  - **por_cxg_ra_cxprtcl_link<X>_ctl**
  - **por_cxg_ra_cxprtcl_link<X>_status**
- Auxiliary Control Register
  - **por_cxg_ra_aux_ctl**
- Configuration Control Register
  - **por_cxg_ra_cfg_ctl**

CXHA:

- HAID
  - **por_cxg_ha_id**
- RAID to LDID LUT
  - **por_cxg_ha_rnf_raid_to_ldid_reg<X>**
  - **por_cxg_ha_rnf_raid_to_ldid_val**
- Remote AgentID (RAID/HAID) to LinkID LUT
  - **por_cxg_ha_agentid_to_linkid_reg<X>**
  - **por_cxg_ha_agentid_to_linkid_val**
- CCIX protocol link control and status
  - **por_cxg_ha_cxprtcl_link<X>_ctl**
  - **por_cxg_ha_cxprtcl_link<X>_status**
- Auxiliary Control Register
  - **por_cxg_ha_aux_ctl**
- RN SAM

CXLA:

- CCIX capabilities (read only)
  - **por_cxla_ccix_prop_capabilities**
- CCIX configured properties
  - **por_cxla_ccix_prop_configured**
- CXS I/F properties/parameters (read only)
  - **por_cxla_tx_cxs_attr_capabilities**
  - **por_cxla_rx_cxs_attr_capabilities**
- Remote AgentID (RAID/HAID) to LinkID LUT
  - **por_cxla_agentid_to_linkid_reg<X>**
  - **por_cxla_agentid_to_linkid_val**
- LinkID to PCIe Bus Number LUT
  - **por_cxla_linkid_to_pcie_bus_num**
- Auxiliary Control Register
  - **por_cxla_aux_ctl**

HN-F:

- LDID to CHI NodeID register
  - **por_hnf_rn_phys_id<X>**
- CCIX port aggregation mask register
  - **por_hnf_cml_port_aggr_grp0_add_mask**
- CCIX port aggregation control register
  - **por_hnf_cml_port_aggr_grp0_reg**

RN-F/RN-I/RN-D:

- RN SAM
- CCIX port aggregation mode enable and control register
  - **cml_port_aggr_grp0_reg**
  - **cml_port_aggr_mode_ctrl_reg**
- CCIX port aggregation mask register
  - **cml_port_aggr_grp0_add_mask**

3.5.2 CML Bring-up Sequence

Use the following information to bring up a CML sequence.

1. Local system discovery and bring-up.
   a. Use the CMN-600 discovery mechanism, as defined in *2.4 Node ID mapping* on page 2-51, to discover node types, their corresponding locations (node IDs) and logical IDs. Node types that are of interest for CML specific programming are RN-Fs, RN-Is, RN-Ds, HN-Fs and CCIX gateway blocks (CXRA, CXHA and CXLA).
   b. Bring up the local system to allow normal local operations. Complete the CMN-600 boot time programming requirements specified in *3.4.1 Boot-time programming requirements* on page 3-1067 to bring up all local non-CCIX components (HN-F, HN-D, HN-I, RN-I, SN-F and XP) and program RN SAM with the local address map.
2. CCIX device and system discovery.
   a. CCIX system discovery may involve going through the PCIe link activation and device enumeration mechanism. Please follow the standard PCIe device enumeration steps to detect CCIX capable devices.
   b. If CCIX capable device(s) are detected during PCIe device enumeration, proceed to the remaining steps. In addition, program the PCIe RC to enable multiple VCs.
3. CCIX device enumeration.
   a. Discover all CCIX agents (RA and HA) at each CCIX device. These agents must be uniquely identified (ID). If any CCIX device contains CMN-600, follow the CMN-600 discovery

mechanism, as defined in *2.4 Node ID mapping* on page 2-51, to discover node types, corresponding locations (node IDs) and logical IDs.

b. Discover the address map requirements of each CCIX device.
c. Read the CCIX capabilities of each CCIX device.
   - To determine CMN-600 CCIX capabilities, read the CCIX capabilities register (**por_cxla_ccix_prop_capabilities**) present in each CXLA.
d. Determine the common properties and capabilities supported by all CCIX devices and configure them in each CCIX device.
   - Configure these properties in the CCIX configured properties register (**por_cxla_ccix_prop_configured**) present in each CXLA.
e. Follow the programming requirements as specified in *3.5.3 CMN-600 initial programming requirements to enable CCIX communication* on page 3-1070

3.5.3 CMN-600 initial programming requirements to enable CCIX communication

The terms *link*, *CCIX link*, and *CCIX protocol link* used in subsequent sections refer to CCIX logical link as defined in CCIX protocol specification. Please refer to CCIX protocol specification for more details.

Programming the Auxiliary and Configuration control registers:

- SMP mode
  — SMP mode can be enabled by setting smp_mode_en bit in por_{cxg_ra, cxg_ha, cxla}_aux_ctl registers. SMP mode must be the same in all communicating CCIX Gateway pairs.
- CXSA mode
  — CXSA mode can be enabled by setting cxsa_mode_en bit in CXRA's por_cxg_ra_cfg_ctl register. When this mode is enabled, CXRA inside CCIX Gateway is used to communicate with a remote CCIX Slave Agent. In this mode CXRA receives requests from locals HN-Fs.

Programming requirements corresponding to local CCIX agents:

- *Requesting Agent ID* (RAID) assignment.
  — For all Requesting Agents, program the RAIDs in LDID to RAID LUT registers (**por_cxg_ra_rn{f, i, d}_ldid_to_raid_reg<X>**) and set the corresponding valid bit in the **por_cxg_ra_rn{f, i, d}_ldid_to_raid_val** register present in each CXRA.
  — If CXSA mode is enabled, then program the CCIX Source ID (Agent ID) in entry 0 of CXRA's "RN-F LDID to RAID LUT" register **(por_cxg_ra_rnf_ldid_to_raid_reg0)** and set the corresponding valid bit in the **por_cxg_ra_rnf_ldid_to_raid_val** register.
  — *Home Agent ID* (HAID) assignment.
    ◦ Program the HAID in the HAID register (**por_cxg_ha_id**) present in each CXHA.

    Note

    1. Since all CXHAs can communicate with all local HNs (HN-F, HN-I, and HN-D), they can have the same HAID unless uniqueness is required for routing purposes.
    2. According to CCIX specification, HA and RA with the same ID must reside behind the same CCIX protocol link. Please refer to CCIX specification for more details.
    3. This programming is not needed if CXSA mode is enabled.

Programming requirements corresponding to remote CCIX agents:

- LinkID assignment.
  — Assign a unique LinkID to each remote CCIX protocol link with which a CCIX gateway (CXRA, CXHA and CXLA) can communicate. Each CCIX gateway block can communicate with up to three remote CCIX protocol links. These links are marked sequentially as links 0, 1, and 2. Each remote CCIX agent (RA or HA), identified by their RAID or HAID, that the gateway can communicate with must be behind only one link. Determine the LinkID of each remote agent (target) and program it in the AgentID (RAID/HAID) to LinkID LUT register (**por_{cxg_ra,**

cxg_ha, cxla}_agentid_to_linkid_reg<X>) present in each CXRA, CXHA, and CXLA. Set the respective valid bits in **por_{cxg_ra, cxg_ha, cxla}_agentid_to_linkid_val**.

Note

1. LinkID must only be unique within a CCIX gateway block. Each CCIX gateway has a respective LinkID space.
2. Each remote link, identified by its LinkID, has its own CCIX protocol link control and status registers.
3. If CXSA mode is enabled, CXHAs AgentID (RAID/HAID) to LinkID LUT register programming is not needed.CXRAs AgentID (RAID/HAID) to LinkID LUT register must be programmed for CCIX Slave Agent ID.

- PCIe Bus Number assignment.
  - Program the PCIe Bus Number for each remote link in the LinkID to PCIe Bus Number LUT register (**por_cxla_linkid_to_pcie_bus_num**) present in each CXLA.

    Note

    This is only needed if PCIe header is used to route a CCIX TLP.

- LDID assignment.
  - Assign a unique *Logical Device ID* (LDID) for each remote caching agent (RN-F) that can send requests to HNs (HN-F, HN-I and HN-D).
    - Program these unique LDIDs in the RAID to LDID LUT register (**por_cxg_ha_rnf_raid_to_ldid_reg<X>**) present in each CXHA. Set the **ldid<X>_rnf** bit to mark the remote agent as a caching agent. Set the respective valid bit in register **por_cxg_ha_rnf_raid_to_ldid_val**.
    - Program the NodeID of each CXHA in HN-F's LDID to CHI NodeID register (**por_hnf_rn_phys_id<X>**) for each remote RN-F (caching agent) that is proxied through that CXHA.

    Note

    1. Remote LDID values must be greater than those used by the local RN-F nodes.
    2. HN-F uses LDID for Snoop Filter (SF) tracking. LDID assignment is not required for non-caching Requesting Agents (RAs), which do not need to be snooped.
    3. This programming is not needed if CXSA mode is enabled.

- RA SAM.
  - For each remote Home Agent, program the address range and corresponding HAID in RA SAM register (**por_cxg_ra_sam_addr_region_reg<X>**) present in each CXRA.
  - If CXSA mode is enabled, RASAM must be programmed with remote CCIX Slave Agent's address range and Agent ID.
- CXHA RN SAM.
  - Program the RN SAM present in each CXHA with address/memory map of local HNs. Please refer to *2.19 RN and HN-F SAM programming* on page 2-112 for details on RN SAM programming.

    Note

    CXHA RN SAM can be programmed as part of local system bring-up, when programming the RN SAM inside each RN with local HNs address/memory map. This programming is not needed if CXSA mode is enabled.

- Program the CCIX protocol link control register (**por_cxg_{ra, ha}_cxprtcl_link<X>_ctl**) present in each CXRA and CXHA.

——— **Note** ———

There is a CCIX protocol link control register for each CCIX protocol link that a given CCIX gateway block (CXRA, CXHA and CXLA) can communicate with.

———————————

——— **Note** ———

If CXSA mode is enabled: a) CXHA's protocol link control registers need not be programmed, and b) CXRA's "lnk0_num_snpcrds" can be set to `4'hF`.

———————————

— Set the link enable bit (**lnk0_link_en**) for each CCIX protocol link that can be used in the future.

——— **Note** ———

If this bit is not set, credits are not set aside for this link.

———————————

— Program the number of credits (**lnk0_num_{snpcrds, reqdatcrds}**) field with the percentage of protocol credits that must be assigned/granted for a given link.

——— **Note** ———

1. This step is optional. Default credits are equally assigned/granted to each enabled link as determined by the link enable bit (**lnk<X>_link_en**).
2. Please ensure that the total percentage of credits allocated to all links does not exceed 100.

Refer to the following table for the number of links and related allowed credit distribution percentage:

———————————

Table 3-1322 Number of links and allowed credit distribution percentage

Number of links	Allowed Credit Distribution
1	100%
2	50%/50%
2	25%/75%
3	50%/25%/25%
3	33%/33%/33%

After distributing credits based on the programmed percentage across all the links available, any remaining credits are allocated to link0. For example, link0 will be allocated 44 credits while link1 and link2 will be allocated 42 credits each for the 128 credit, 33% credit distribution configuration.

- *CCIX Port Aggregation* (CPA) programming sequence for RN SAM.
  — Set the **region<N>_pag_en bit in cml_port_aggr_mode_ctrl_reg** register to 1'b1 for each remote non-hashed memory region that must use CPA.
  — Set 1'b1 in each bit of **addr_mask field in the cml_port_aggr_grp0_add_mask** register that must be used in hashing to distribute the request traffic between CCIX gateways.
  — Program the number of CCIX gateways and their Node ID's in **cml_port_aggr_grp0_reg register's num_cxg_pag0** and **pag0_tgtid0 and pag0_tgtid1** fields.
- CCIX Port Aggregation programming sequence for HN-F SAM.

— For each valid LDID in the in the **por_hnf_rn_phys_id<X>** registers, set the cpa_en_ra<ldid> to 1'b1 if it must use CPA.
— Set 1'b1 in each bit of addr_mask field in the **por_hnf_cml_port_aggr_grp0_add_mask** register that must be used in hashing to distribute the snoop traffic between CCIX gateways.
— Program the number of CCIX gateways and their Node ID's in **por_hnf_cml_port_aggr_grp0_reg** register's **num_cxg_pag0**, **pag0_tgtid0**, and **pag0_tgtid1** fields.

3.5.4 Runtime programming

Use the following information for runtime programming.

1. Bring up CCIX protocol link. Please refer to *3.5.5 CCIX Protocol Link-up Sequence* on page 3-1073.
2. Add a CCIX protocol link in system coherency and DVM domains. Please refer to *3.5.7 CCIX Protocol Link Coherency and DVM Domain Entry/Exit* on page 3-1074. This programming is not needed if CXSA mode is enabled.
3. Program the remote address range and corresponding CXRA node ID for each remote memory region in RN SAM present in CMN-600 RN-F, RN-I, and RN-D. RNSAM must not be programmed to target CXRA when enabled for CXSA mode.

   ——— **Note** ———

   If the software can guarantee that there is no traffic to the remote address range until CCIX-related initial programming is complete and CCIX protocol links are up, then this programming should be done upfront (i.e. when programming RN SAMs with local address map).

   ———————————

3.5.5 CCIX Protocol Link-up Sequence

Use the following information to link-up.

This section describes the steps to set up a CCIX protocol link between each CMN-600's CCIX gateway block (CXRA, CXHA and CXLA) and corresponding remote CCIX link that it is communicating with. The term *link* used in this section refers to CCIX protocol link. Multiple CCIX links can be setup simultaneously by extending this sequence for each link.

1. Check if the communication on link can be established.
   a. Poll link enable bit (**lnk<X>_link_en**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) in CXRA and CXHA to ensure that the link is enabled.
2. Ensure that the link is down and can accept a new link up request.
   a. Poll link up bit (**lnk<X>_link_up**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) to ensure that it is clear. Poll link down bit (**lnk<X>_link_down**) in CCIX protocol link status register (**por_cxg_<ra/ha>_cxprtcl_link<X>_status**) to ensure that it is set. Poll link ACK bit (**lnk<X>_link_ack**) in CCIX protocol link status register (**por_cxg_<ra/ha>_cxprtcl_link<X>_status**) to ensure that it is clear.
3. Make a request to bring up the link.
   a. Set link request bit (**lnk<X>_link_req**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) in CXRA and CXHA.
4. Ensure that the link up request is accepted.
   a. Link up request is acknowledged by setting link ACK bit (**lnk<X>_link_ack**) and clearing link down bit (**lnk<X>_link_down**) in CCIX protocol link status register (**por_cxg_<ra/ha>_cxprtcl_link<X>_status**) present in CXRA and CXHA. Link up means that both sides are ready to receive and grant CCIX protocol credits.
5. After both sides acknowledge the link up request, instruct both sides to start granting credits.
   a. Set link up bit (**lnk<X>_link_up**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) in CXRA and CXHA.
6. Link<X> is now up. Both sides can now exchange CCIX protocol credits and protocol messages.

3.5.6 CCIX Protocol Link-down Sequence

Use the following information to link down.

This section describes steps to bring down a CCIX protocol link between each CMN-600's CCIX gateway block (CXRA, CXHA and CXLA) and corresponding remote CCIX protocol link that it is communicating with. The term *link* used in this section refers to CCIX protocol link. Multiple CCIX protocol links can be brought down simultaneously by extending this sequence for each link.

Note

Before initiating a link down sequence, software must ensure the following:

1. There are no outstanding transactions that require CCIX message transfers across the link for their completion. This includes GIC-D in SMP mode.
2. The protocol agents on both sides of the link are configured to not initiate new transactions across the link. For CMN-600:
   a. Poll "link OT CopyBack" (**lnk<X>_ot_cbkwr**) bit in CXRA's "CCIX Protocol Link Status" (**por_cxg_ra_cxprtcl_link<X>_status**) register to make sure that it is cleared. This is to ensure that there are no outstanding CopyBack requests targeting that link.
   b. Take the link out of system coherency and DVM domains. Please refer to *3.5.7 CCIX Protocol Link Coherency and DVM Domain Entry/Exit* on page 3-1074
3. If CXSA mode is enabled, CCIX links must not be brought down until all HN-Fs communicating with this CXSA are in OFF state.

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1. Ensure that the link is up and can accept a new link down request.
   a. Poll link up bit (**lnk<X>_link_up**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) in CXRA and CXHA to ensure that the link is up. Poll link request bit (**lnk<X>_link_req**) to ensure that it is set.
2. Make a request to bring down the link.
   a. Clear link request bit (**lnk<X>_link_req**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) in CXRA and CXHA to make a link down request.
3. Ensure that the link down request is accepted.
   a. Poll link ACK bit (**lnk<X>_link_ack**) in CCIX protocol link status register (**por_cxg_<ra/ha>_cxprtcl_link<X>_status**) to ensure that it is cleared. After link down request is accepted, each side must stop granting local CCIX protocol credits and start returning remote CCIX protocol credits.
4. Ensure that each side has received all its protocol credits and is ready to go down.
   a. Link down ready status is conveyed by setting link down bit (**lnk<X>_link_down**) in CCIX protocol link status register (**por_cxg_<ra/ha>_cxprtcl_link<X>_status**) in CXRA and CXHA.
5. After both sides acknowledge that they are ready to take down the link, instruct both sides to shut down the link.
   a. This is done by clearing link up bit (**lnk<X>_link_up**) in CCIX protocol link control register (**por_cxg_<ra/ha>_cxprtcl_link<X>_ctl**) present in CXRA and CXHA.
6. Link<X> is now down. No protocol message or credit transfers should occur across link.

3.5.7 CCIX Protocol Link Coherency and DVM Domain Entry/Exit

Each CCIX Gateway block (CXRA, CXHA and CXLA) includes software bits for entry and exit of a given CCIX protocol link from system coherency and DVM domains.

Snoop coherency domain entry/exit request bit (**lnk<X>_snoopdomain_req**) is present in each CXHA's CCIX protocol link control register (**por_cxg_ha_cxprtcl_link<X>_ctl**) and the corresponding acknowledge bit (**lnk<X>_snoopdomain_ack**) is present in CCIX protocol link status register (**por_cxg_ha_cxprtcl_link<X>_status**).

DVM domain entry/exit request bit (**lnk<X>_dvmdomain_req**) is present in each CXRA's CCIX protocol link control register (**por_cxg_ra_cxprtcl_link<X>_ctl**) and the corresponding acknowledge bit (**lnk<X>_dvmdomain_ack**) is present in CCIX protocol link status register (**por_cxg_ra_cxprtcl_link<X>_status**).

Please refer to *2.30 RN entry to and exit from Snoop and DVM domains* on page 2-163 for additional information.

3.6 Support for RN-Fs compliant with CHI Issue A specification

Although CMN-600 natively supports devices compliant with CHI Issue B specification, it also provides support for connecting RN-Fs based on CHI Issue A specification with some feature restrictions and the corresponding CMN-600 programming requirements.

This section describes these feature restrictions.

This section contains the following subsections:

3.6.1 CHI Issue A device node ID mapping

In a CMN-600 system, all devices are assigned a unique CHI Issue B node ID such as B_NID [n:0], where n = 6, 8, or 10 based on the system node ID width.

CHI Issue A devices, however, have a fixed 7-bit wide node ID such as A_NID[6:0]. For such devices, the A_NID is derived from the CHI Issue B node ID by shifting the LSBs and padding the MSBs with zeros as necessary as shown in the following tables.

Table 3-1323 Mapping CHI Issue A device node ID into CMN-600 device node ID

Node ID width	CMN-600 device node ID	Comments
7 bits	B_NID [6:0] = (A_NID[4:0], `2'b00`)	A_NID[6:5] must be zero
9 bits	B_NID [8:0] = (A_NID[6:0], `2'b00`)	-
11 bits	B_NID [10:0] = (`2'b00`, A_NID[6:0], `2'b00`)	2 MSBs of B_NID are padded with zeros

Table 3-1324 Mapping CMN-600 device node ID into CHI Issue A device node ID

Node ID width	CHI Issue A device node ID	Comments
7 bits	A_NID [6:0] = (`2'b00`, B_NID[6:2])	B_NID[1:0] are zeros and are discarded
9 bits	A_NID [6:0] = B_NID[8:2]	B_NID[1:0] bits are zeros and are discarded
11 bits	A_NID [6:0] = B_NID[8:2]	B_NID[10:9] and B_NID[1:0] bits are zeros and are discarded

3.6.2 Stashing

CHI Issue A RN-Fs do not support stashing.

All HN-F instances are configured to not send snoop stash requests to the CHI Issue A RN-F.

3.6.3 Direct Cache Transfer

CHI Issue A RN-Fs do not support *Direct Cache Transfer* (DCT).

All HN-F instances are configured to disable DCT in snoop requests to the CHI Issue A RN-F.

3.6.4 Data poison

CHI Issue A RN-Fs do not support data poisoning.

All HN-F instances are configured to report and log data poison errors detected on SLC data sent to the CHI Issue A RN-F.

Likewise, DMC must be configured to report and log data poison errors detected on read data.

3.6.5 RN SAM programming

CHI Issue A RN-Fs can be configured as ESAM.

When CHI Issue A RN-F is configured as ESAM, then the SAM in CMN-600 must be programmed following the steps described in *2.16 RN SAM* on page 2-100.

3.6.6 System coherency entry and exit

For system coherency entry or exit, either the hardware or software interface must be enabled.

For system coherency entry or exit, either the hardware or software interface must be enabled as described in *2.30 RN entry to and exit from Snoop and DVM domains* on page 2-163.

Chapter 4
SLC Memory System

This chapter describes the SLC memory system.

It contains the following sections:

4.1 About the SLC memory system

The SLC memory system consists of the HN-F protocol nodes in CMN-600.

There is a configurable number of instances (1-32) of the HN-F, and each HN-F node or slice has the following features:

- 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB of SLC data RAM and tag RAM.
- Combined *Point-of-Coherency* (PoC) and *Point-of-Serialization* (PoS).
- SF size of 512KB, 1MB, 2MB, 4MB, or 8MB.

Each HN-F in CMN-600 is configured to manage a specific portion of the total address space. For each portion of the address, each HN-F:

- Can cache data in SLC.
- Manages PoC and PoS functionality for ordering and coherency.
- Tracks RN-F caching in the SF.

The SLC memory system has the following features:

- *Physically Indexed and Physically Tagged* (PIPT).
- Coherency granule is a fixed length of 64 bytes. SLC line size is a fixed length of 64 bytes.
- Both SLC and SF are 16-way set-associative. 12-way for 3MB SLC configurations.
- The SLC and SF victim selection policy is:
  - Pseudo random if all ways are valid.
  - If there is invalid way, there is no need to victim.
  - Victim selection is needed only if all ways are taken.
- ———— **Note** ————

  For SLC, CMN-600 R2 supports *Enhanced LRU* (eLRU) cache replacement policy as well that can be enabled by setting a bit in config register. eLRU is Dynamic Biased Replacement Policy. Two bits per set/way are used to keep track of and predict how soon a cache line is expected to be used again. This information is dynamically adjusted based on few reference sets.

  ————————————

  SLC and SF arrays:
  - Supports one-, two-, or three-cycle non-pipelined tag array.
  - Supports two- or three-cycle non-pipelined data array.
  - SLC tag, SF tag, and SLC data arrays are single-ported, supporting one read or write access with no concurrency available.
  - SLC tag, SF tag, and SLC data arrays are ECC (SECDED) protected, with inline ECC checking and correction. SECDED means *Single-Error Correction and Double-Error Detection*.
- 32 or 64 entry address and data buffer, known as *PoC Queue* (POCQ), to service:
  - All transactions from the CHI interface.
  - SLC evictions to the memory controller.
  - SF evictions and associated writebacks to the memory controller.
- CMO propagation to SN-F/SBSX:
  - Propagates Persistent CMO requests to a cache line to the memory controller.
  - Conditional CMO propagation to the memory controller to support external DRAM caches.
  - HN-F must be explicitly programmed to allow such propagation using the HN-F SAM's **por_hnf_sam_sn_properties** register to each SN-F.
- Supports QoS-based protocol flow control:
  - PoC and PoS resources (POCQ) are allocated or rejected for protocol retry, based on the QoS class.
  - POCQ resources are watermarked for different QoS classes with user-configurable options.
  - Starvation prevention for lower-priority QoS classes.
  - QoS-based static grantee selection for CHI architecture credit return.
- QoS priority based request selection to the memory controller.

- Supports allocation in the SLC from snoop intervention. This enables data sharing through the SLC for multiple sharers.
- SLC state includes caching *Logical Device IDentifier* (LDID) to detect dynamic read sharing.
- Configurable 34, 44, or 48-bit physical address support.
- PoC and PoS for all snoopable and non-snoopable, and Cacheable and Non-cacheable address space.
- Supports ECC scrubbing for single-bit ECC errors on SF and SLC tag RAMs.
- Software-controlled error injection support to enable testing of software error handler routine.
- Power-management states to support:
  - Full powerdown of the SLC and SF. HN-F only mode when both SLC and SF are powered down.
  - Half the SLC ways powered down.
  - Retention for SLC and SF.
  - SLC full powerdown with SF on, when in SF only mode.
- Arm TrustZone® technology support in SLC and SF.
- Software configurable (1, 2, 4, 8, or 12 ways) Memory Region locking support in the SLC.
- Software configurable (1, 2, 4, 8, or 12 ways) *On Chip Memory* (OCM) support in the SLC:
  - OCM memory does not need any physical memory backing.
- Supports CHI enhancements for:
  - *Direct Cache Transfer* (DCT).
  - *Direct Memory Transfer* (DMT). DMT not supported with 128b SBSX configurations.
  - Cache Stashing.
  - Atomics support.
  - Data Poison.
  - Data Parity (Datacheck).
  - Trace Tag.
- Invisible SLC support:
  - CMN-600 HN-F implements an invisible cache. All accesses (cacheable/non-cacheable/Device types) are checked against the SLC and snoop filter. The SLC cannot be cleaned and invalidated (flushed) by software using ARM architecture set/way operations. Software specific to CMN-600 would instead be required to flush the SLC, as described in this TRM. Invisible SLC support eliminates the need to perform SLC flushes for software context switches from cacheable to non-cacheable.
- Supports up to two memory-region-based SN targets and 1, 3, or 6 SN-F address hashing.

4.2 Configurable options

The HN-F can be configured in several ways.

The HN-F has the following configurable parameters:

- SLC size of 0KB, 128KB, 256KB, 512KB, 1MB, 2MB, 3MB, or 4MB.
- SF size of 512K, 1M, 2MB, 4MB, or 8MB.
- 32 or 64 POCQ entries.
- One-, two-, or three-cycle tag RAM arrays. For a given configuration, both SLC tag and SF tag have the same latency.
- Two- or three-cycle Data RAMs, data, and SF array RAMs. All data RAMs have the same latency.

The HN-F has the following static, or fixed, parameters:

- HN-F CHI interface data-VC (DAT) width of 256 bits.

4.3 Basic operation

CMN-600 system level cache is a distributed, mostly-exclusive last-level cache.

The SLC is optimized to eliminate redundancy for private data lines from the RN-F, and enables redundancy, or pseudo-inclusion, when a sharing pattern is detected between RN-F clusters. CMN-600 SLC also acts as DRAM cache for I/O coherent agents, that is, RN-Is, by enabling RN-Is to allocate or not allocate, based on the usage model.

The SF works in conjunction with the SLC to track coherent lines that are present in the RN-F caches. The SF is fully inclusive of all the lines present in the RN-F caches. SF eviction invalidates the lines from RN-F caches to maintain this inclusion.

Normally, a particular coherent cache line is present only in the system level cache or SF except when the line is shared between RN-F clusters. In the shared case, the line can be present in both the SLC and the SF.

4.4 Cache maintenance operations

The CMN-600 uses a number of CHI *Cache Maintenance Operation*s (CMOs).

The following operations are supported:

- CleanInvalid.
- CleanShared.
- MakeInvalid.
- CleanSharedPersist.

These operations always look up the SLC and the SF, and take the following actions:

- Clean and invalidate the line if present in the SLC.
- If the CMO is snoopable, the HN-F sends a snoop to the RN-F post snoop filter lookup if required.
- If the cache line is modified in the SLC or in the cache of the RN-Fs, the HN-F initiates a memory controller writeback if required.

——— **Note** ———

If the CMO is MakeInvalid, there is no writeback to the memory controller.

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4.5 Cacheable and Non-cacheable exclusives

The HN-F supports PoC monitor functionality for Cacheable and snoopable exclusive operations from the RN-Fs.

The Cacheable and snoopable exclusive transactions are:

- ReadShared.
- ReadClean.
- CleanUnique.

The HN-F also supports system monitor functionality for Non-cacheable exclusive support. See the *Arm® AMBA® 5 CHI Architecture Specification* for more information about exclusives.

Note

Each HN-F in CMN-600 can support tracking of up to 64 logical processors for exclusive operations. The system programmer must ensure that there are no more than 64 logical processors capable of concurrently sending exclusive operations.

4.6 TrustZone technology support

The HN-F supports TrustZone technology by treating the NS bit from a request as part of the address.

TrustZone enables the HN-F to treat Secure and Non-secure as two different areas of the memory space:

- The NS bit is stored in the SLC and SF tags.
- Snoops also propagate the NS bit as part of the message.
- Any request to the memory controller also propagates the NS bit.

4.7 Snoop connectivity and control

Each HN-F can send three types of snoop.

The snoop requests are:

- Directed, to one RN-F.
- Multicast, to more than one but not all.
- Broadcast, to all RN-Fs.

4.8 QoS features

The HN-F protocol queue (POCQ) is a key shared system resource that communicates with the memory controller for external memory access.

The HN-F provides QoS capabilities in support of the following traffic classes:

- Real-time or pseudo-real-time traffic that requires a maximum bounded latency at potentially fixed bandwidth.
- Latency-sensitive traffic, traditionally from a processor device.

CMN-600 uses QoS values to designate these traffic classes. Every request to the HN-F has a 4-bit QoS value that is associated with it, with a higher number indicating a higher priority. The four QoS classes are:

- Highest priority, known as HighHigh.
- High priority.
- Medium priority.
- Low priority.

This section contains the following subsections:

- *4.8.1 QoS decoding* on page 4-1087.
- *4.8.2 QoS class and POCQ resource availability* on page 4-1087.

4.8.1 QoS decoding

QoS decoding takes place inside the HN-F.

The QoS decoding is as follows:

- The CHI interface supports a 4-bit QoS value.
- The 4-bit QoS has 16 possible values. Refer to *Table 2-14 QoS classes in HN-F* on page 2-74 for the QoS ranges and class values in HN-F.
- QoS mapping is fixed, and is shown in the qos_band register.

The POCQ is logically partitioned to service different QoS class traffic. The HN-F also uses the priorities in the table to arbitrate for the following:

- Memory controller request selection in the POCQ control block.
- Data return selection logic, that is, a CompData to a requester.
- Protocol credits sent to an RN-F or RN-I following a protocol-layer retry.

4.8.2 QoS class and POCQ resource availability

The POCQ buffers are shared resources for all QoS classes.

The higher the QoS class, the higher the occupancy availability. For example, the *HighHigh* (HH) QoS class can use all the POCQ entries except for the dedicated SF pool.

The following figure shows the availability of POCQ resources for various QoS levels, using a particular QoS pool that is shared between multiple QoS classes.

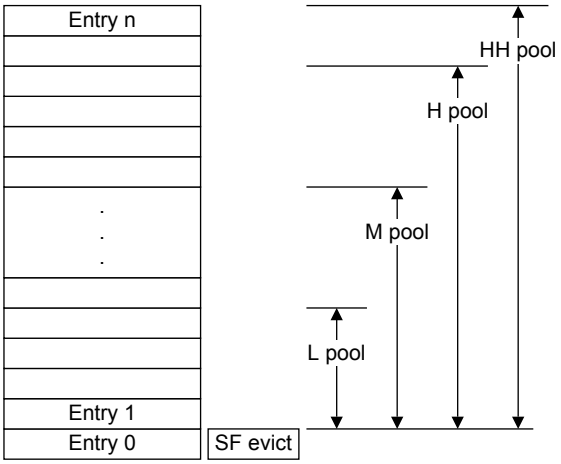

Figure 4-1 POCQ availability and QoS classes

The QoS pools are:

hh_pool Available for HH class.

h_pool Available for H class and HH class.

m_pool Available for M class, H class, and HH class.

l_pool Available for all classes.

seq SF evictions only.

This scheme enables a higher-priority QoS class to have more POCQ resources for transaction processing, and prevents a lower-priority QoS from using all the POCQ. The level of POCQ availability decreases for the lower QoS classes.

QoS pool distribution of the POCQ is software-configurable using the qos_reservation register.

4.9 CMN-600 Hardware-based cache flush engine

This section describes the hardware-based cache flush engine of the CMN-600 product.

Per HNF instance configuration registers:

- POR_HNF_ABF_LO_ADDR: lower range address
- POR_HNF_ABF_HI_ADDR: upper range address
- POR_HNF_ABF_PR: ABF Policy Register. Triggers flush start, indicates flush operation type
- POR_HNF_ABF_SR: ABF Status Register. Indicates flush completion and other status information

The flush engine will ensure that all cache lines in the lower/upper range are flushed from the CMN-600 Snoop Filter and SLC. Once all cache lines within this range are flushed, a status register bit is set indicating Flush engine completed and interrupt (INTREQPPU) is sent, if enabled.

——— **Note** ———

Interrupt indication and complete bit in status registers are set regardless of normal completion or abort condition. Error bits in Status register should be checked to determine if Flush request completed normally or aborted.

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Flush Sequence:

1. Flush CMN-600 Snoop Filters, this will result in flushing the lines in the lower level (L2, etc.) caches, lower-level write-backs go to memory, are not allocated to the CMN-600 SLC.
2. Flush the CMN-600 SLC cache.
3. On completion of the flush:
   a. The HN-F sets status bit when the flush is complete for that HNF. If there are error conditions, those are also set in status register. Status register is cleared when next ABF request starts.
   b. The HN-F sends a completion message to the global Power/Clock/Reset unit, and an optional INTREQPPU is asserted when all HN-F instances have completed the flush.

ABF

ABF requests are processed in parallel to other ongoing requests from RNs. No ordering/ coherency guarantee is provided if same address is targeted by both. Power management transition requests have higher precedence than *Address Based Flush* (ABF) request. ABF request is supported only when Power management state is in FAM, HAM, or SFONLY mode and retention state is IDLE or RETENTION (not transitionary). While ABF is in progress, any update to PWPR (Power Policy Register) will cause ABF state machine to abort and Power management request will proceed.

By default, flush engine will write-back any modified data to memory before invalidating cache line from internal caches. Two additional config modes are provided for user flexibility. In total, three modes are:

- **CleanInvalid:** Write-back and invalidate (default).
- **MakeInvalid:** In this mode, modified data will not be written back to memory. (user programmable).
- **CleanShare:** In this mode, modified data written back to memory but clean data remain in internal caches. (user programmable).

If *On Chip Memory* (OCM) is enabled and address range overlaps with ABF range, OCM behavior will supersede ABF. For SLC, this would mean that for CleanInvalid & CleanShare modes, no action would be taken and for MakeInvalid, there would be no difference in behavior regardless of address in OCM range or not. For SFflush, behavior is same between OCM address match and not.

The following tables provide a summary for SF and SLC caches for all three modes.

Table 4-1 SF Cache operation

SF Cache	Hit		Miss	
ABF Mode	SNP type to RN-F	Change SF state?	SNP to RN-F	Change SF state?
CleanInvalid	CleanInvalid	Yes	n/a	No
MakeInvalid	MakeInvalid	Yes	n/a	No
CleanShared	CleanShared	Yes*	n/a	No

Table 4-2 SLC Cache operation

SLC Cache state		Modified		Exclusive/Shared		Invalid	
ABF Mode	OCM Match	Evict Line?	Change L3 State (Final state)	Evict Line?	Change L3 State (Final state)	Evict Line?	Change L3 State (Final state)
CleanInvalid	No	Yes	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)
MakeInvalid	No	No	Yes (I)	No	Yes (I)	No	No (I)
	Yes	No	Yes (I)	No	Yes (I)	No	No (I)
CleanShared	No	Yes	Yes (E)	No	No (ES)	No	No (I)
	Yes	No	No (M)	No	No (ES)	No	No (I)

Note

The following assumptions are:

- RNs should not access a cache line (within flush range) while ABF is in progress to ensure coherency/ordering is maintained.
- Address ranges and trigger needs to be programmed for each HN-F in the SCG.
- ABF related Config register bits should not be changed once trigger bit (abf_enable) is set until status register indicates flush is done (abf_complete).
- HN-F needs to be in one of the three operational modes (FAM, HAM, SFONLY). Once Flush starts, any update to *Power Policy Register* (PWPR) will cause ABF to abort.
- SF needs to be enabled. If SF is disabled, Flush engine will abort with error status.
- At the completion of ABF, Status register should be checked to ensure *Address Based Flush* (ABF) completed without any errors. If ABF aborted for any reasons, it would be indicated in status register.

4.10 Data Source Handling

CMN-600 populates DataSource field of CompData response to specify source of the data.

DataSource information can be used to:

- Determine usefulness of PrefetchTgt (Memory controller prefetch) transaction.
- Profile and debug software to evaluate and optimize data sharing patterns.

Table 4-3 DataSource encodings

Source of Data	Message	Encoding
HN-I	Default (Non-memory source)	3’b000
RN-F	Peer CPU cache within local Cluster	3’b001
RN-F	Local Cluster cache	3’b010
HN-F	SLC (system level cache)	3’b011
RN-F	Peer cluster cache	3’b100
Remote Chip	Remote chip caches	3’b101
SN-F/SBSX	PrefetchTgt was useful	3’b110
SN-F/SBSX	PrefetchTgt was not useful	3’b111

CMN-600 drives DataSource value only when the source of the data is either HN-F or HN-I. For other data sources, CMN-600 acts as a conduit.

The encoding of DataSource indication used by CMN-600 is same as the suggested value in CHI architecture document. Any deviation from those encoding may result in unexpected behavior.

4.11 Software configurable memory region locking

The HN-F supports variable size memory regions that can be locked in the system level cache with way reservation.

These variable size memory regions ensure that locked lines are not evicted from the SLC, and any access to those lines is guaranteed to hit in the SLC. The variable memory region can be one of the following sizes:

- 0.5MB
- 1MB
- 2MB
- 4MB
- 8MB

Software uses the following mechanism to program the HN-F configuration registers to enable region locking:

- The hnf_slc_lock_ways register specifies the total number of locked HN-F system level cache ways. This can be a value of 1, 2, 4, 8, or 12.
- The following region base registers specify the base address of the region that is using locked ways:
  - hnf_slc_lock_base0 register.
  - hnf_slc_lock_base1 register.
  - hnf_slc_lock_base2 register.
  - hnf_slc_lock_base3 register.
- A combination of the total SLC size, hnf_slc_lock_ways register, and the hnf_slc_lock_base0 register to hnf_slc_lock_base3 register defines the following:
  - The total amount of cache locked, calculated as follows:

$$\frac{\text{Total SLC size x Number of locked ways}}{16}$$

  - Ways are locked beginning with way 0 and then in ascending order.
  - The number of valid regions and exactly which regions, and therefore which of the hnf_slc_lock_base0 to hnf_slc_lock_base3 registers, are valid and included in the HN-F way allocation.
  - The exact location, size, and alignment requirement of each region.
- The region alignment is identical to the region size, for example:
  - A 0.5MB region is aligned to any 0.5MB boundary.
  - A 4MB region is aligned to any 4MB boundary.
- The size and alignment requirement is enforced in hardware, to prevent any errors in software.
- Regions can be disjointed or contiguous, to create a larger single region.
- All valid regions use all locked ways. There is no application-level way segregation.
- No overlocking is allowed. This means it is not possible to have more indices per set than is supported by the number of locked ways, preventing the spilling of locked ways.
- The HN-F must be in the FAM power state. Memory Region Locking is not supported in other CMN-600 power states.

Note

The locked regions do not comprehend Secure as opposed to Non-secure memory regions, so overlocking can occur if aliasing is performed between Secure and Non-secure regions.

The following tables specify various combinations of region size and the number of locked ways that software must program using the hnf_slc_lock_ways register and the hnf_slc_lock_base0 register to hnf_slc_lock_base3 register.

Table 4-4 SLC Region Lock sizes

SLC size	Number of locked ways	Total locked region size	Locked ways	Number of ways per region	Region 0	Region 1	Region 2	Region 3
8MB	1	0.5MB	0	1	0.5MB	-	-	-
8MB	2	1MB	0-1	1, 1	0.5MB	0.5MB	-	-
8MB	4	2MB	0-3	1, 1, 1, 1	0.5MB	0.5MB	0.5MB	0.5MB
8MB	8	4MB	0-7	2, 2, 2, 2	1MB	1MB	1MB	1MB
8MB	12	6MB	0-11	2, 2, 4, 4	1MB	1MB	2MB	2MB

Table 4-5 Settings for hnf_slc_lock_baseX

Region size	Valid bits
0.5MB	[43:18]
1MB	[43:19]
2MB	[43:20]
4MB	[43:21]
8MB	[43:22]

4.12 Software-configurable On-Chip Memory

The CMN-600 HN-F supports software configurable *On-Chip Memory* (OCM) which allows for the creation of systems without physical DDR memory. It also allows a system to use SLC as scratchpad memory.

In OCM mode, the HN-F does not send requests to the SN-F. In order to enable OCM, the following requirements must be met:

- The HN-F must be in the FAM power state. Other CMN-600 power states are not supported in OCM mode.
- All OCM ways must be same across all HN-Fs in a system cache group.
- OCM mode must be enabled before any non-config accesses are sent to HN-F.

In OCM mode, the following CMOs terminate in the SLC:

- CleanInvalid and CleanShared CMOs terminate in the SLC without performing a WriteBack to the SN-F.
- MakeInvalid invalidates the cache line in SLC, and can be used to invalidate the OCM region.

OCM mode can be enabled by programming the **hnf_ocm_en** bit in the **por_hnf_cfg_ctl** register. If the **hnf_ocm_allways_en** bit is set to 1, then all transactions targeting the HN-Fs have OCM behavior. The OCM region must be contiguous and aligned to the total SLC size of the configuration when the **hnf_ocm_allways_en** is set to 1. If the **hnf_ocm_allways_en** bit is 0, the OCM regions are defined by the region locking registers that *4.11 Software configurable memory region locking* on page 4-1092 describes.

Note

Secure and non-secure memory regions are not explicitly controlled by the region locking registers. Hence secure and non-secure memory regions combined should not exceed the total SLC size that is locked for OCM.

4.13 CMO propagation from HN-F to SN-F/SBSX

CMN-600 supports propagation of CMO and PCMO requests for a given cache line to the memory controller.

This feature ensures that the cache line has been written to the memory controller and any copies in the CMN-600 system have been removed. Conditional CMO and PCMO propagation to the memory controller also supports external DRAM caches. This feature can be enabled or disabled in each HN-F's **por_hnf_sam_sn_properties** register bits corresponding to each SN-F.

4.14 Source-based SLC cache partitioning

CMN-600 R2 only. HN-F supports a feature to lock SLC ways for requesting nodes RN-F, RN-I, and RN-D.

This feature is an extension of the address based way locking but the locked ways are based on the requestors instead of the programmed address. CMN-600 supports programming of the number of ways that can be locked, RN devices for which these ways are locked and allocation policies in each HN-F. With this feature enabled, the locked SLC ways are only available to the programmed RNs for any new cache line allocations.

Source based way locking feature can be enabled by programming the **por_hnf_rn_region_lock**.rn_region_lock_en bit to 1'b1 in each HN-F instance. The requesting nodes, for which these ways are to be locked must also be explicitly enabled in the por_hnf_rn*region_vec registers. The requesting nodes are individually identified using the logical IDs. Each requesting node type RN-F, RN-I and RN-D have different registers and are uniquely identified in CMN-600 system using logical IDs. The number of ways that are locked are programmed in **por_hnf_slc_lock_ways** register's "ways" field.

The region locking features has two allocation modes:

- Allocating new cache lines for matching RNs only in the locked ways. By doing so, the matching RNs are restricted to allocate to the locked partition only. This mode can be enabled by setting por_hnf_rn_region_lock.rn_pick_locked_ways_only bit to 1'b1.
- Allocating new cache lines for matching RNs to one of the locked or unlocked ways. This mode is the default behavior. In this mode, the locked ways are restricted only to the matching RNs but the unlocked ways are accessible by all the RNs.

Source-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.

——— **Note** ———

The HN-F must be in the FAM power state. Source-based cache partitioning is not supported in other CMN-600 power states.

———————————

4.15 Way-based SLC cache partitioning

CMN-600 R2 only. Each SLC cache instance can be partitioned into different regions such that each requesting node (RN-F, RN-I, RN-D) can allocate in one or more regions, each consisting of four consecutive ways.

Each region group has config registers that indicate which of the logical RNF/RNI/RND masters can allocate to the corresponding group of SLC ways. By default, all RNs can allocate in all 16 ways as shown in the following tables.

Table 4-6 Logical RNF ID requesting node

Register Name	Addr Offset	Ways Reserved	Default	Logical RNF ID								
				63	62	61	60	----	3	2	1	0
por_hnf_slcway_partition0_rnf_vec	0xc48	[3:0]	{64'{1'b1}}									
por_hnf_slcway_partition1_rnf_vec	0xc50	[7:4]	{64'{1'b1}}									
por_hnf_slcway_partition2_rnf_vec	0xc58	[11:8]	{64'{1'b1}}									
por_hnf_slcway_partition3_rnf_vec	0xc60	[15:12]	{64'{1'b1}}									

Table 4-7 Logical RNI ID requesting node

Register Name	Addr offset	Ways Reserved	Default	Logical RNI ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rni_vec	0xc68	[3:0]	{32'{1'b1}}									
por_hnf_slcway_partition1_rni_vec	0xc70	[7:4]	{32'{1'b1}}									
por_hnf_slcway_partition2_rni_vec	0xc78	[11:8]	{32'{1'b1}}									
por_hnf_slcway_partition3_rni_vec	0xc80	[15:12]	{32'{1'b1}}									

Table 4-8 Logical RND ID requesting node

Register Name	Addr Offset	Ways Reserved	Default	Logical RND ID								
				31	30	29	28	----	3	2	1	0
por_hnf_slcway_partition0_rnd_vec	0xc88	[3:0]	{32'{1'b1}}									
por_hnf_slcway_partition1_rnd_vec	0xc90	[7:4]	{32'{1'b1}}									
por_hnf_slcway_partition2_rnd_vec	0xc98	[11:8]	{32'{1'b1}}									
por_hnf_slcway_partition3_rnd_vec	0xca0	[15:12]	{32'{1'b1}}									

The registers in these tables are used to mask the ways that are available for an RN to allocate to at all times. A value of:

- 1'b1: Indicates the corresponding Logical RN ID can allocate in this region
- 1'b0: Indicates the corresponding Logical RN ID cannot allocate to this region

In order to enable the way reservation only to a subset of RN's, the mask in the above registers must be programmed as shown in the following example:

Example for reserving ways 0-3 for RNF 0,1,2 and 3

1. Write 64'h000000000000000F por_hnf_slcway_partition0_rnf_vec. Enables logical RNF ID's 0,1,2 and 3 to allocate to ways 0 through 3. All other RNFs (ID 4 through 63) cannot allocate to these ways.
2. Write 32'h00000000 por_hnf_slcway_partition0_rni_vec. Disables all 32 RNIs from allocating to ways 0 through 3.
3. Write 32'h00000000 por_hnf_slcway_partition0_rnd_vec. Disables all 32 RNDs from allocating to ways 0 through 3.

——— **Note** ———

Three conditions apply to this example:

- This feature cannot be used if region based locking, source based locking or OCM is enabled.
- The region registers can be changed runtime.
- When the way partitioning scheme is not being used, the above registers must be returned to the default values.
- Each RN should be configured to allocate to at least one partition. Setting the bit for a given RN to 0 in all partition registers will default it to allocating in any partition.
- RN-I and RN-D each support a maximum logical ID of 32 in the partition mask register. In CML configurations, care must be taken to assign LDID to remote RN-I and RN-Ds above the local RN-I and RN-D logical ID's. This ensures SLC partitioning is honored correctly across all RN-I and RN-Ds.

———————————

Way-based SLC cache partitioning is supported only when *Enhanced LRU* (eLRU) mode is used.

——— **Note** ———

The HN-F must be in the FAM power state. Cache partitioning is not supported in other CMN-600 power states.

———————————

4.16 Error reporting and software-configured error injection

HN-F detects and reports errors of several types to the error block.

Below are the errors HN-F supports:

- Correctable Errors: Such as, single-bit ECC error detection and correction in the SLC Tag RAM, SF Tag RAM, and SLC Data RAM.
- Deferred Errors: Such as, double-bit ECC error detection in SLC Data RAM.
- Uncorrectable Errors: Such as, double-bit ECC error detection in SLC Tag RAM and SF Tag RAM.

If the DATACHECK_EN parameter is enabled, HN-F may also support Data parity error detection in the SLC Data RAM. Such errors are logged as Deferred Errors.

HN-F follows the procedures described in *2.14 Error handling* on page 2-82 for logging and reporting all error types.

Refer to **por_hnf_errmisc.errsrc** for information regarding the error source.

4.16.1 Software-configurable error injection

The HN-F supports software-configurable error injection and reporting. This feature enables testing of the software error handler routine for SLC double-bit ECC data errors.

The HN-F configuration register for a particular logical thread enables configurable error injection and reporting. When enabled, any Cacheable read for which the HN-F provides the data, that is, a system cache hit, drives the slave error from the system cache pipe and drives a fault interrupt through the RAS control block for that read. This emulates a double-bit ECC error in the system cache data RAM without polluting the system level cache data RAM through the fill path.

Note

SLC misses do not drive any slave errors or error interrupts. This mechanism is designed to mimic SLC data ECC errors for SLC hits.

To configure error injection, refer to the *por_hnf_por_hnf_err_inj* register for details.

4.16.2 Software-configurable parity error injection

The HN-F supports software-configurable parity error injection.

This feature enables testing of the software error handler routine for parity error. To enable this feature, refer to the **por_hnf_byte_par_err_inj** register. It specifies the byte lane from 0 to 31 in which a parity error is introduced. The memory data is uncorrupted with such injection.

Chapter 5
Debug trace and PMU

This chapter describes the *Debug Trace* (DT) and *Performance Monitoring Unit* (PMU) features.

It contains the following sections:

5.1 DT system overview

CMN-600 provides at-speed self-hosted *Debug Trace* (DT) capabilities.

The DT capabilities include:

- Watch-point- and trace-tag-initiated transaction tracing.
- Globally synchronized cycle counters for precise tracing.
- CHI trace tag generation.
- CoreSight™ ATB trace streaming.
- Configuration register access to trace data.
- Cross trigger support.
- Secure debug support.
- Event-based interrupts.

The CMN-600 DT system consists of a set of *Debug Trace Controllers* (DTCs) and *Debug Trace Monitors* (DTMs) distributed across the interconnect. DTCs are located inside HN-Ds and HN-Ts while DTMs are located inside XPs.

The following interfaces are present in all DTCs:

- ATB.
- **DBGWATCHTRIGREQ**.
- **DBGWATCHTRIGACK**.
- **INTREQPMU**.

The following interfaces are present only in the master DTC:

- **NIDEN**.
- **SPNIDEN**.
- **PMUSNAPSHOTREQ**.
- **PMUSNAPSHOTACK**.

——— **Note** ———

NIDEN and **SPNIDEN** are propagated from master DTC to all DTMs. When asserted, they must remain asserted for at least 72 clock cycles. Likewise, when deasserted, they must remain deasserted for at least 72 clock cycles. This ensures that all internal CMN-600 components transit into their debug and trace states correctly.

———————————

The following figure shows an example DT system with two DTC domains.

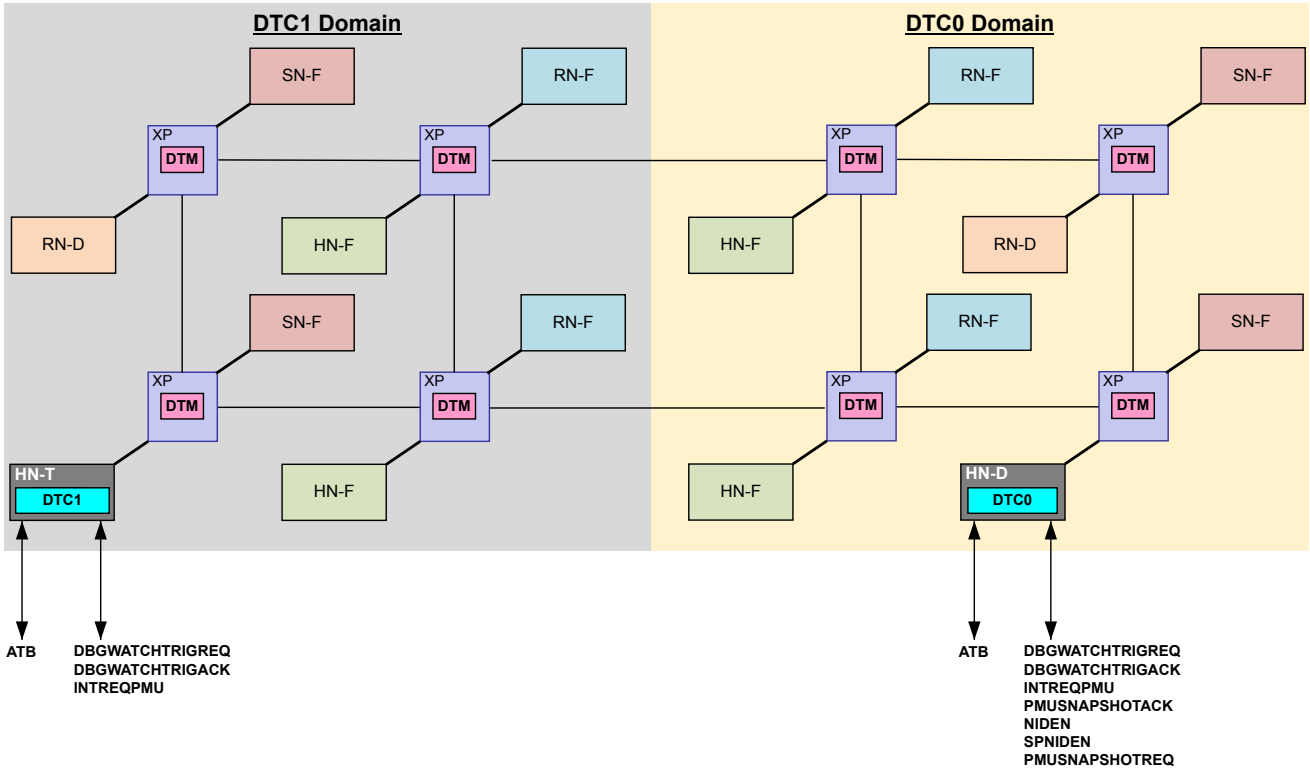

Figure 5-1 Example DT System with two DTC domains

Note

In a DT system comprising multiple DTCs, the one located inside the HN-D is designated as the master DTC or DTC0. DTM assignment to DTCs is achieved via configuring XP parameters within Socrates.

Each DTC is associated with a set of DTMs to form an exclusive DTC domain. When enabled, DTMs within a DTC domain collect trace data and transmit it to the associated DTC. The number of DTC domains is determined by the number of HN-T nodes in the mesh.

In a DT system comprising multiple DTCs, the one located inside the HN-D is designated as the master DTC or DTC0. DTM assignment to DTCs is achieved via configuring XP parameters within Socrates.

Each DTC domain must be built using contiguous XPs.

The DT system implements the following functions:

- CHI flit monitoring at XP device ports using four sets of *WatchPoint*s (WPs) in each DTM.
- Flit trace generation and storage at each DTM with control register access to trace packets.
- Trace tag generation.
- Debug trigger signaling and trace packet streaming over the *Arm Trace Bus* (ATB) at each DTC.
- Internal event-based cross trigger generation and broadcast to all DTMs.
- Globally synchronized cycle counters.

This section contains the following subsections:

- *5.1.1 DTM watchpoint* on page 5-1103.
- *5.1.2 DTM FIFO buffer* on page 5-1106.
- *5.1.3 Read mode* on page 5-1109.
- *5.1.4 DTC* on page 5-1110.
- *5.1.5 ATB packets* on page 5-1110.

5.1.1 DTM watchpoint

A DTM has four *WatchPoints* (WPs) that monitor flit uploads and downloads at XP device ports.

WPs monitor flits by matching on a subset of flit fields that are specified using a pair of val and mask registers as shown in the following figure:

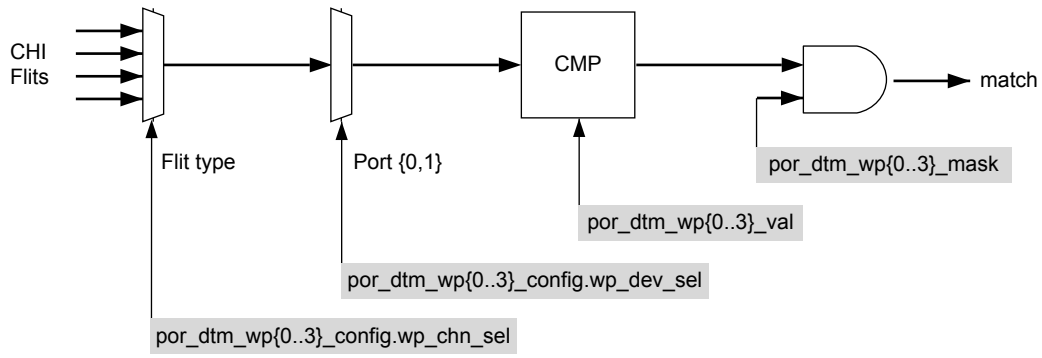

Figure 5-2 CMN-600 DTM WP comparator

A WP can be configured to monitor flits from one of two XP device ports and one of four CHI channels:

- REQ
- RSP
- SNP
- DAT

In addition, the WP can be configured to do one or more of the following tasks on detecting a flit match:

- Set trace tag bit on the flit.
- Generate flit trace.
- Generate cross trigger to DTC.
- Generate debug trigger to DTC.
- Increment PMU counters.

Note

Two WPs within a group can be combined for complex matching. For example, WP0 and WP1 can be combined, just as WP2 and WP3 can be combined.

The four DTM WPs are assigned in groups of two each to flit uploads and downloads as follows:

- WP0 and WP1 are assigned to flit uploads.
- WP2 and WP3 are assigned to flit downloads.

WP match value and mask register

The WP flit matching criterion is specified using a 64b match value register (**dtm_wpN_val**) and a 64b mask register (**dtm_wpN_mask**), where N=0, 1, 2, or 3. These registers allow matching up to 64b of the flit.

The value to be matched is written in `dtm_wpN_val` register. Bits that need to be masked off in the match comparison are specified in the `dtm_wpN_mask` register by writing a 1'b1 in the corresponding bit positions.

The CHI flits fields are divided into two match groups: a primary match group, and a secondary match group. The tables below specify the flits fields that belong to each of the groups for the different CHI

channels. The RSP and DAT channels have only a primary match group while REQ and SNP channels have both primary and secondary match groups.

Flit matching from two different match groups requires two WPs to be combined. For example, if both Opcode and Address fields of flits uploaded on the REQ channel are to be matched, then WP0 and WP1 need to be combined, with Opcode match specified in WP0 and Address match specified in WP1 or vice versa. Likewise, if both Opcode and Address fields of flits downloaded on the REQ channel must match, then WP2 and WP3 must be combined in a similar manner.

REQ channel width and bit ranges for the primary match group are contained in the following table.

Table 5-1 REQ channel: primary match group

Field	Width	Bit range
SRCID/TGTID	11	10:0
STASHNID/RETURNNID	11	21:11
STASHNIDVALID/ENDIAN	1	22:22
RETURNTXNID/{3'b0, STASHLPIDVALID, STASHLPID[3:0]}	8	30:23
OPCODE	6	36:31
SIZE	3	39:37
NS	1	40:40
ALLOWRETRY	1	41:41
ORDER	2	43:42
PCRDTYPE	4	47:44
LPID	5	52:48
EXPCOMPACK	1	53:53
TRACETAG	1	54:54
RSVDC	8	62:55

REQ channel width and bit ranges for the secondary match group are contained in the following table.

Table 5-2 REQ channel: secondary match group

Field	Width	Bit range
QOS	4	3:0
ADDR	48	51:4
LIKELYSHARED	1	52:52
MEMATTR	4	56:53
SNPATTR	1	57:57
EXCL/SNOOPME	1	58:58
TRACETAG	1	59:59

RSP channel width and bit ranges for the primary match group are contained in the following table.

Table 5-3 RSP channel: primary match group

Field	Width	Bit range
QOS	4	3:0
SRCID/TGTID	11	14:4
OPCODE	4	18:15
RESPERR	2	20:19
RESP	3	23:21
FWDSTATE / STASH	3	26:24
DBID	8	34:27
PCRDTYPE	4	38:35
TRACETAG	1	39:35
DEVEVENT	2	41:40

SNP channel width and bit ranges for the primary match group are contained in the following table.

Table 5-4 SNP channel: primary match group

Field	Width	Bit range
SRCID	11	10:0
FWDTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]} / VMIDEXT	8	18:11
OPCODE	5	23:19
NS	1	24:24
DONOTGOTOSD	1	25:25
RETTOSRC	1	26:26
TRACETAG	1	27:27
ADDR[35:0]	36	63:28

SNP channel width and bit ranges for the secondary match group are contained in the following table.

Table 5-5 SNP channel: secondary match group

Field	Width	Bit range
SRCID	11	10:0
FWDTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]} / VMIDEXT	8	18:11
OPCODE	5	23:19
NS	1	24:24
DONOTGOTOSD	1	25:25
RETTOSRC	1	26:26
TRACETAG	1	27:27

Table 5-5 SNP channel: secondary match group (continued)

Field	Width	Bit range
QOS	4	31:28
ADDR[44:13]	32	63:32

DAT channel width and bit ranges for the primary match group are contained in the following table.

Table 5-6 DAT channel: primary match group

Field	Width	Bit range
QOS	4	3:0
SRC/TGTID	11	14:4
HOMENID	11	25:15
OPCODE	3	28:26
RESPERR	2	30:29
RESP	3	33:31
FWDSTATE / STASH	3	36:34
DBID	8	44:37
CCID	2	46:45
DATAID	2	48:47
TRACETAG	1	49:49
POISON	1	50:50
CHUNKV	2	52:51
DEVEVENT	2	54:53
RSVDC	8	62:55

Note

chunkv[1:0] denotes whether the upper or lower 128 bits of data are valid.

5.1.2 DTM FIFO buffer

Traces captured by the DTM are stored in a four-entry DTM FIFO buffer. Each entry is 144-bits wide.

Entries are allocated to all enabled WPs as needed. Trace data from WPs are packed based on the trace data format and stored within each entry to efficiently use the limited buffer storage. Hence an entry may contain trace data from multiple flits captured at different times.

As each FIFO entry fills up, trace data from that entry is sent to the DTC for streaming out via the ATB interface.

Trace data format

CMN-600 supports several trace data formats.

The trace data format is specified by the 3-bit packet type encoding in the DTM WP configuration register **por_dtm_wp{0..3}_config.wp_pkt_type**. The following table provides the supported trace data formats and their packet type encodings.

Table 5-7 Trace data formats

Packet type	Trace data format		Size	Max traces per FIFO entry
000	TXNID[7:0]		8 bits	18
001	{2'b00, OPCODE[5:0],TXNID[7:0]}		16 bits	9
010	{TGTID[10:0], SRCID[10:0], OPCODE[5:0],TXNID[7:0]}		36 bits	4
011	Reserved		-	-
100	Control Flit (see tables below for field descriptions)	REQ	141 bits	1
		RSP	61 bits	
		SNP	96 bits	
		DAT	83 bits	
101	Reserved		-	-
110	Reserved		-	-
111	Reserved		-	-

Trace data is packed into a DTM FIFO buffer entry such that the higher order bytes contain older trace data. For example, if the trace data format is set to TXNID (type 0) and three TXNIDs (trace data) are received in the order 0x01, followed by 0x02, followed by 0x03, then the trace FIFO entry is set to:

- 0000_0000_0000_0000_0000_0000_0000_0001_0203

The following tables describe the control flit formats for various flit channels beginning with REQ control flit information.

Table 5-8 REQ control flit

Field	Width	Bit range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
STASHNID / RETURNNID	11	44:34
STASHNIDVALID /ENDIAN	1	45:45
RETURNTXNID / {3'b0, STASHLPIDVALID, STASHLPID[3:0]}	8	53:46
OPCODE	6	59:54
SIZE	3	62:60
NS	1	63:63
LIKELYSHARED	1	64:64
ALLOWRETRY	1	65:65
ORDER	2	67:66
PCRDTYPE	4	71:68
MEMATTR	4	75:72
SNPATTR	1	76:76
LPID	5	81:77

Table 5-8 REQ control flit (continued)

Field	Width	Bit range
EXCL/SNOOPME	1	82:82
EXPCOMPACK	1	83:83
TRACETAG	1	84:84
ADDR	48	132:85
RSVDC	8	140:133
Total	141	-

The following table contains RSP control flit information.

Table 5-9 RSP control flit

Field	Width	Bit Range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
OPCODE	4	37:34
RESPERR	2	39:38
RESP	3	42:40
FWDSTATE / STASH	3	45:43
DBID	8	53:46
PCRDTYPE	4	57:54
TRACETAG	1	58:58
DEVEVENT	2	60:59
Total	61	-

The following table contains SNP control flit information. See also *6.10 DEVEVENT in CMN-600* on page 6-1148 for more **DEVEVENT** information.

Table 5-10 SNP control flit

Field	Width	Bit Range
QOS	4	3:0
SRCID	11	14:4
TXNID	8	22:15
FWDNID	11	33:23
FWDTXNID / {`3'b0`, STASHLPIDVALID, STASHLPID[3:0]} / VMIDEXT	8	41:34
OPCODE	5	46:42
NS	1	47:47
DONOTGOTOSD	1	48:48
RETTOSRC	1	49:49

Table 5-10 SNP control flit (continued)

Field	Width	Bit Range
TRACETAG	1	50:50
ADDR	45	95:51
Total	96	-

The following table contains DAT control flit information.

Table 5-11 DAT control flit

Field	Width	Bit Range
QOS	4	3:0
TGTID	11	14:4
SRCID	11	25:15
TXNID	8	33:26
HOMENID	11	44:34
OPCODE	3	47:45
RESPERR	2	49:48
RESP	3	52:50
FWDSTATE / STASH	3	55:53
DBID	8	63:56
CCID	2	65:64
DATAID	2	67:66
TRACETAG	1	68:68
POISON	4	72:69
CHUNKV	2	74:73
DEVEVENT	2	76:75
RSVDC	8	84:77
Total	85	-

See also *6.10 DEVEVENT in CMN-600* on page 6-1148 for more **DEVEVENT** information.

Note

chunkv[1:0] denotes whether the upper or lower 128 bits of data are valid.

5.1.3 Read mode

Read mode provides an alternate way to access trace data stored in the DTM trace FIFO buffer, via configuration register access.

Each entry in the FIFO buffer is mapped to three 64-bit configuration registers, **dtm_fifo_entry{0..3}_X**, where X = 0, 1, or 2.

Read mode is enabled by setting the **trace_no_atb** bit in the DTM control register (**por_dtm_control**). Setting this bit causes all FIFO entries to be cleared and the DTM FIFO read status register (**por_dtm_fifo_entry_ready**) to be reset.

In this mode, each FIFO entry is allocated to the corresponding WP. For example, **por_dtm_fifo_entry0_{0..2}** can be allocated to WP0, **por_dtm_fifo_entry1_{0..2}** can be allocated to WP1, and so on.

The read status for each WP trace data is reflected in the corresponding bit in the DTM FIFO entry ready status register (**por_dtm_fifo_entry_ready**). When a FIFO entry is full, the corresponding status bit is set, indicating that the trace data is ready to be read. Subsequent writes into that FIFO entry are disabled until the status bit is cleared. A write of 1 clears the status bit and enables the corresponding FIFO entry to capture subsequent trace data.

5.1.4 DTC

DTCs control DTMs.

The main features of the DTC are:

- Trace packing, generation, and streaming via ATB interface
- Time stamping of traces
- Global synchronized cycle counters in all units (16-bit)
- ATB flush of DTM and DTC
- Watch point trigger event based interrupt
- Eight sets of performance counters (32-bit) with shadow registers, paired with one or more DTM local counters
- PMU snapshot of DTM and DTC
- PMU overflow interrupt

5.1.5 ATB packets

Each DTC aggregates flit trace data from the DTMs into the DTC trace FIFO, packetizes them, and sends them out on its ATB interface.

In addition it sends other control and debug packets. This section describes the different packet formats used on the ATB interface.

Trace data packet format

Trace data packet contains a four-byte header and a payload of variable size (in bytes).

The following figure shows the packet header.

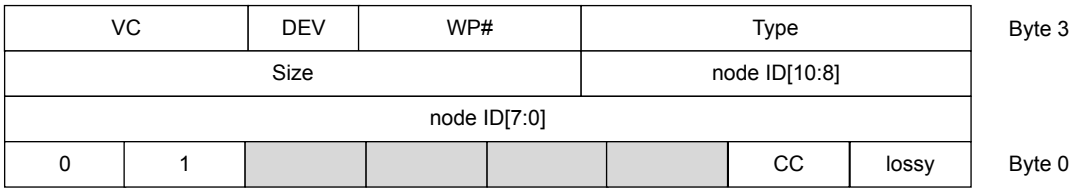

Figure 5-3 Trace data packet header

The packet header contains the following fields:

- **VC** is the CHI channel encoded as:
  - `00` – REQ
  - `01` – RSP
  - `10` – SNP
  - `11` – DAT
- **DEV** is the device port number, 0 or 1.
- **WP#** is the watchpoint number, 0-3, that captured the trace.
- **Type** is the packet format type.
- **Size** is the payload size specified as (number of bytes – 1).

- **NodeID** is the CHI node ID, shifted right by three bits reflecting the (X,Y) coordinates of the XP where the trace was captured.
- **CC** is the cycle counter. When set, this field indicates that a 2-byte cycle count is included in the packet after the payload.

The following key points must be observed:

1. For packet type `100`, the leading zeros in upper-order bytes of the trace data payload are compressed and not transmitted. The payload **Size** field in the trace packet header is adjusted accordingly. For example, trace data = `0000_0000_0000_0000_0000_0000_0000_0001_0203` is sent as `01_0203`, with **Size** = 2 (indicating three bytes transferred).
2. The **WP** field selection for match might be different from the type of payload generated from the matching. When WPs are combined, the lower watchpoint number is specified as the **WP#** in the trace packet header.
3. Trace data is of variable length. The expected number of bytes, not including the header, is (**Size** + 1). And with **CC**, another two bytes are included at the end of the trace data.
4. Any time the previous packets cannot be transmitted in full, a lossy bit is asserted for the immediate next packet. A separate lossy bit is maintained for each of the watchpoints.

Alignment sync packet format

The alignment sync delimits trace start.

The alignment sync packet is 16 bytes long and comprises 15 bytes of zeros followed by 0x80.

The alignment sync packet is the first packet that is sent after tracing is enabled. In addition, the DTC can be configured to send the alignment sync packet periodically by programming the DTC control register, por_dt_trace_control.

Time stamp packet format

The time stamp packet carries the SoC timer information. The time stamp is used to align the sequence of trace events across the SoC.

The time stamp packet is sent opportunistically under the following circumstances when the DTC FIFO has enough space to accommodate the time stamp packet:

- After each alignment sync packet is sent.
- When flush is complete.
- Periodically based on the setting of por_dt_trace_control.timestamp_period register and only when trace packets have been sent following the last time stamp packet.

The time stamp packet format is shown in the following figure.

The time stamp packet contains the following fields:

- TS# 3-bit encoding of the size of time stamp specified as number of bytes - 1
- CC, when set, indicates a 2-byte cycle count is included in the packet after the payload

Figure 5-4 Time stamp packet

Cycle counting packet format

Trace packets include an optional attached cycle counter.

Each watchpoint includes a configuration bit. The logical operator AND is used on the configuration bit and global cycle count enable. The following figure shows a typical cycle counting scenario.

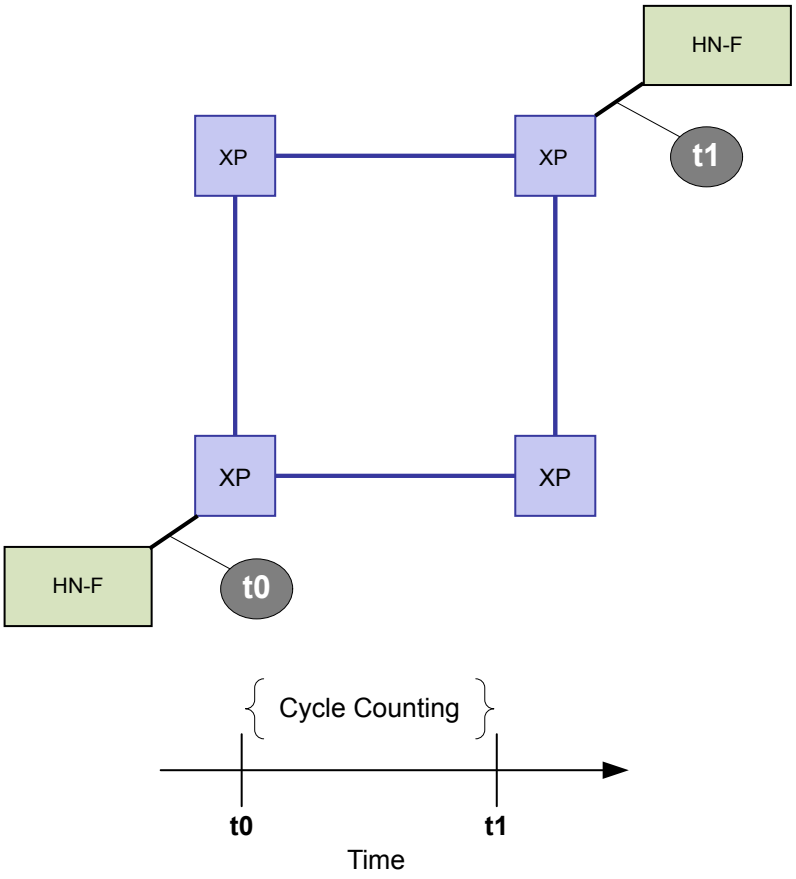

Figure 5-5 Cycle counting

The cycle counter payload is two bytes and is indicated by the **CC** bit in the trace packet header. Cycle counters across the interconnect are turned on and off synchronously. This ensures that all of them have the same time stamp value.

Trace stream example

DTCs send trace data out on the ATB bus as a trace stream.

An example trace stream is shown in the following figure. It consists of:

- 4-byte trace packet header.
- M-byte trace data.
- 2-byte cycle count.
- 1-byte time stamp header.
- N-byte time stamp.
- 2-byte cycle count.

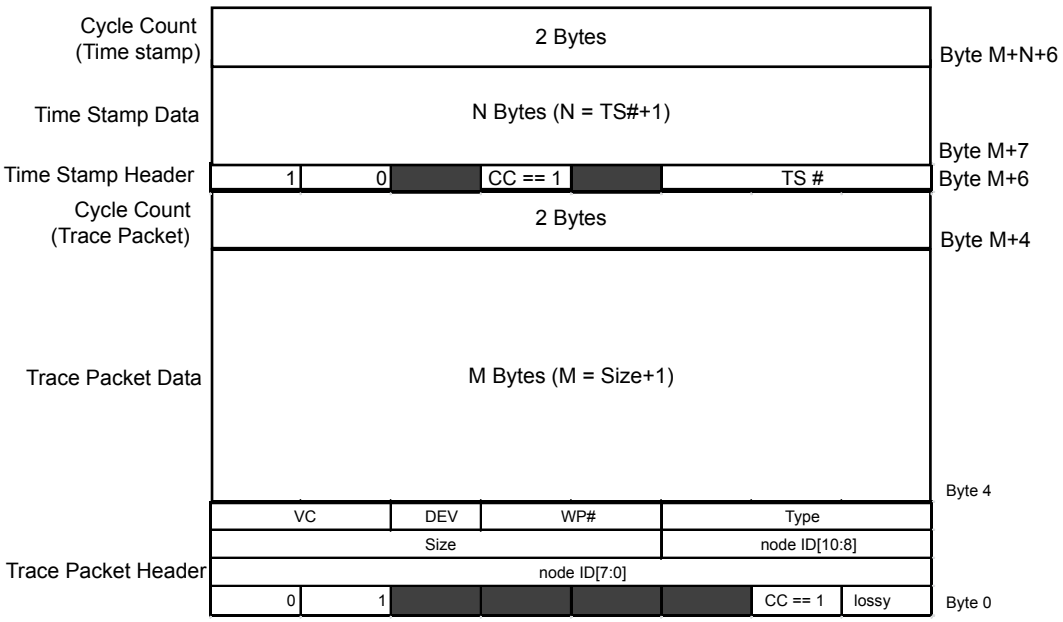

Figure 5-6 Trace stream

5.2 DT programming

This section describes the DTM and DTC programming sequences.

This section contains the following subsections:

5.2.1 DTM watchpoint programming

Use this procedure to program **Watchpoint N, where N=0..3**.

1. Program the intended watchpoint matching fields, such as source ID, target ID and opcode, by writing the appropriate values into the **dtm_wp0_val** and **dtm_wp0_mask** registers.
2. Program the WP settings/function in **dtm_wpN_config.wp_dev_sel** and **dtm_wpN_config.wp_chn_sel** to select the device port and flit CHI channel.
3. Program **dtm_wp0_config.wp_grp** for primary or secondary group of watchpoint value.
4. If two watchpoints need to be combined, write `1'b1` into **dtm_wpN_config.wp_combine**.

   ——— **Note** ———

   The **wp_combine** field is present in WP0 and WP2 only.

   ———————————

5. If trace packets are to be generated from this watchpoint, program **dtm_wp0_config.wp_pkt_type** and write `1'b1` to **dtm_wp0_config.wp_pkt_gen**.
6. If cross trigger needs to be setup from this watchpoint, write `1'b1` into **dtm_wp0_config.wp_ctrig_en**.
7. If debug watchpoint trigger needs to be setup from this watchpoint, program **dtm_wp0_config.wp_dbgtrig_en**.
8. If cycle count is needed in the trace packet, set **dtm_wp0_config.wp_cc_en** = 1.
9. If debug watchpoint trace tag is to be enabled, write `1'b1` to **dtm_control.trace_tag_enable**.
10. The final step is to write `1'b1` to **dtm_control.dtm_enable** to enable the WP.

5.2.2 DTC programming

NIDEN needs to be asserted for any trace and PMU operation. All watchpoint functions must be programmed and enabled in the DTMs first.

1. Write `1'b1` to **por_dt_dtc_ctl.dbgtrigger_en** if DBGWATCHTRIG should be generated for DTM debug watchpoint trigger.
2. Write `1'b1` to **por_dt_dtc_ctl.atbtrigger_en** if ATB trigger should be generated for DTM debug watchpoint trigger.
3. Write `1'b1` to **por_dt_dtc_ctl.cc_en** to enable cycle count.
4. Write `1'b0` to **por_dt_dtc_ctl.dt_wait_for_trigger** if no cross trigger is required.
5. Write `1'b1` to **por_dt_dtc_ctl.dt_en**.

The following register bits are present only in the main DTC (DTC0):

- **por_dt_secure_access**
- **por_dt_dtc_ctl.dt_en**
- **por_dt_dtc_ctl.wait_for_trigger**
- **por_dt_dtc_ctl.cc_start**
- **por_dt_pmcr.pmu_en**
- **por_dt_pmsrr**
- **por_dt_pmssr.ss_cfg_active**
- **por_dt_pmssr.ss_pin_active**

5.3 DT usage examples

This section describes example usage of DT features.

This section contains the following subsections:

5.3.1 Flit tracing

CMN-600 provides support for tracing individual flits at device interfaces at each XP.

DTM WPs can be programmed to monitor flit uploads and downloads at each of the two XP device ports on any of the four CHI channels:

- REQ
- RSP
- SNP
- DAT

Using a set of val/mask registers, the WPs provide flexibility in matching on a user defined subset of flit fields.

On a match, WPs capture and store flit fields, that are most useful for debug, into trace buffers. The generated trace can then be streamed out on the ATB interface or accessed via control register interface.

Details of the format of the value and mask registers, in addition to trace packets can be found in *WP match value and mask register* on page 5-1103 and *Trace data format* on page 5-1106 sections of this manual.

Flit tracing example

CMN-600 provides support for tracing individual flits at device interfaces at each XP.

Refer to section *5.2.1 DTM watchpoint programming* on page 5-1114 for more information.

This section shows an example for setting up a simple trace scenario to trace REQ flits corresponding to a ReadShared transaction to address=X initiated by RNF2 and sending the trace packets out on the ATB bus

1. Setup watchpoints (WPs) inside XP connected to RNF2 to monitor REQ flits uploaded from RNF2. Since Opcode and Address fields are mapped to two different registers: primary and secondary match registers respectively. Two WPs need to be set up: one to monitor the Opcode and the other to monitor the Address.
    a. Program WP0 (upload WP) to monitor REQ.Opcode as follows:
        a. Set dtm_wp0_val/mask registers to match on Opcode=ReadShared
        b. Set dtm_wp0_config to
            a. Select upload device port (wp_dev_sel=RNF2_port)
            b. Flit channel (wp_chn_sel=REQ)
            c. Match format group to primary for Opcode match (wp_grp=0)
            d. Set combined mode to gang-up WP0 and WP1 (wp_combine=1)
            e. Enable REQ flit trace packet generation (set wp_pkt_type, wp_pkt_gen=1)
    b. Program WP1 (upload WP) to monitor REQ.Address as follows:
        a. Set dtm_wp1_val/mask registers to match on Address=X
        b. Set dtm_wp1_config to

a. Select upload device port (wp_dev_sel=RNF2_port)
b. Flit channel (wp_chn_sel=REQ)
c. Match format group to secondary for Address match (wp_grp=1)

Note: In combined mode, WP0 config settings are used for enabling trace generation

1. Enable trace tag generation in the WP
   - Set dtm_control.dtm_enable = 1
     — Program the DTC to start the trace
2. Program por_dt_dtc_ctl as follows:
   - Enable tracing (dt_en=1)

5.3.2 Trace tag

CMN-600 provides support for trace tag generation at the device interfaces and propagation to destination devices.

This feature enables a set of flits corresponding to a specific transaction or a set of transactions matching a specific criterion to be tagged for tracing.

For example, using the trace tag mechanism, flits from all four CHI channels:

- REQ.
- RSP.
- SNP.
- DAT.

These four channels pertain to a Memory Read transaction to a specific address that can be tagged for tracing.

Trace tag generation

A trace tag is generated internally by an XP, or externally by an RN-F or SN-F device and reflected in the **TRACETAG** field of the uploaded flit.

Inside the XP, DTM WPs generate the trace tag by matching on flits uploaded at the corresponding XP device port. The DTM WPs can be programmed to match on a flit on any of the four CHI channels: REQ, RSP, DAT, and SNP.

DTM WPs can be programmed to match on a flit on any CHI channel and on any device port. However, for debug, it is most useful to program WPs to match on REQ flits uploaded at the RN and HN-F device ports. This programming is useful because these are the starting flits that originate new transactions. Once tagged, subsequent RSP, SNP, and DAT flits pertaining to the same transaction carry the trace tag.

If all the following conditions are true, the trace tag is not generated by the XP:

- Flit transfer takes place from one device port to the other device port, within the same XP.
- The flit destination device is not an HN.
- The flit transfer to its destination occurs one cycle after the XP receives it.

Trace tag propagation

All CMN-600 devices forward on the trace tag, when asserted, from a received flit corresponding to a transaction to all subsequent flits associated with that transaction.

In addition, the HN-F propagates the trace tag from the source transaction to spawned transactions such as SLC evictions and snoop filter back invalidations.

Using OR, the trace tag generated inside the XP is combined with the **TRACETAG** field in the flit received from the source device. This result is sent in the **TRACETAG** field of the flit transmitted to the destination device.

Trace tag example

This section contains a Trace Tag scenario based trace generation with synchronized cycle counts.

Refer to section *5.2.1 DTM watchpoint programming* on page 5-1114 for more information.

This section shows an example for setting up a simple trace scenario to trace REQ flits corresponding to a ReadShared transaction to address=X initiated by RNF2 and sending the trace packets out on the ATB bus

1. Setup watchpoints (WPs) inside XP connected to RNF2 to monitor REQ flits uploaded from RNF2. Since Opcode and Address fields are mapped to two different registers - primary and secondary match registers respectively - two WPs need to be set up: one to monitor the Opcode and the other to monitor the Address.
   a. Program WP0 (upload WP) to monitor REQ.Opcode as follows:
      a. Set dtm_wp0_val/mask registers to match on Opcode=ReadShared
      b. Set dtm_wp0_config to
         a. Select upload device port (wp_dev_sel=RNF2_port)
         b. Flit channel (wp_chn_sel=REQ)
         c. Match format group to primary for Opcode match (wp_grp=0)
         d. Set combined mode to gang-up WP0 and WP1 (wp_combine=1)
         e. Enable REQ flit trace packet generation (set wp_pkt_type, wp_pkt_gen=1)
   b. Program WP1 (upload WP) to monitor REQ.Address as follows:
      a. Set dtm_wp1_val/mask registers to match on Address=X
      b. Set dtm_wp1_config to
         a. Select upload device port (wp_dev_sel=RNF2_port)
         b. Flit channel (wp_chn_sel=REQ)
         c. Match format group to secondary for Address match (wp_grp=1)

Note: In combined mode, WP0 config settings are used for enabling trace generation

1. Enable trace tag generation in the WP
   - Set dtm_control.dtm_enable = 1
     — Program the DTC to start the trace
2. Program por_dt_dtc_ctl as follows:
   - Enable tracing (dt_en=1)

5.3.3 Debug watch trigger

DTM WPs can be programmed to match on specific flits and generate a debug watch trigger event to the DTC.

The DTC can be programmed to signal the debug watch trigger event in one of the following ways:

1. Signal a debug watch trigger interrupt on the DBGWATCHTRIGREQ/DBGWATCHTRIGACK interface.

   ——— **Note** ———

   This interface is based on a four-phase handshake protocol.

   ———————————

2. Signal an ATB trace trigger with ATID 0x7D on the ATB interface.
3. Signal both a debug watch trigger interrupt and an ATB trace trigger.

In a system with multiple DTCs, each DTC has its own ATB interface on which it signals ATB trace triggers from DTMs within its DTC domain. Whereas debug watch trace interrupts are signaled on the single DBGWATCHTRIGREQ/ DBGWATCHTRIGACK interface shared between the DTCs.

5.3.4 Cross trigger

CMN-600 provides support for triggering DTMs based on a specific event(s) occurring elsewhere in the system.

By default, DTMs start monitoring and tracing flits without waiting for another event. The cross trigger feature allows flit monitoring and tracing to to be delayed until after the events of interest are observed in the system.

The cross trigger event is setup in two steps as follows:

1. DTM WPs are set up to monitor flits and generate traces.
2. Other DTM WPs (in the same XP or different XPs) are set up to generate a cross trigger on specific event(s) to the DTC which is programmed to trigger the DTMs in Step1.

Cross trigger example

CMN-600 provides support for triggering DTMs based on a specific event(s) occurring elsewhere in the system.

Refer to section *5.2.1 DTM watchpoint programming* on page 5-1114 for more information.

This example illustrates a cross trigger scenario where trace DAT flits corresponding to a ReadShared transaction to address-X that originated at RN-F2 after 10 WriteNoSnoops have been uploaded to the HN-D.

1. Set WP at RN-F2 upload port to monitor REQ flits (refer to step 1 in *5.3.4 Cross trigger* on page 5-1117).
2. Set WP(s) at all DAT download ports to generate DAT flit traces (refer to step 2 in *5.3.4 Cross trigger* on page 5-1117).
3. Setup WP at HN-D upload port to monitor WriteNoSnoop flits.
   a. Program WP0 (upload WP) to monitor and enable cross trigger REQ. Opcode as follows:
      a. Set **dtm_wp0_val/mask** registers to match on Opcode = WriteNoSnoop.
      b. Set **dtm_wp0_config** to:
         a. Select upload device port (wp_dev_sel = HND_port).
         b. Flit channel (wp_chn_sel = REQ).
         c. Match format group to primary for Opcode match (wp_grp = 0).
         d. Enable cross trigger (wp_ctrig_en = 1).
   b. Enable WP.
      - Set dtm_control.dtm_enable = 1.
4. Setup counter in DTC to count 10 trigger events from HN-D WP before.
   - Program **por_dt_dtc_ctl** as follows:
      1. Set cross trigger count (cross_trigger_count = 9).
      2. Enable waiting for HN-D WP trigger event (dt_wait_for_trigger = 1).
      3. Enable DTC (dt_en = 1).

Sample profile

CMN-600 supports ARMv8.2 sample extension.

WPs can be programmed to monitor channel, opcode, and related PM items. A Sample Interval Counter Register (PMSICR) counts down with each of the match. When the counter hits zero, the Trace Tag of the next matched transaction is asserted. At the same time, the counter is reloaded with programmed value from PMSIRR, and the next count down cycle repeats.

There is only one set of PMSCIR/PMSIRR per XP, as only one outstanding transaction is expected. PMSICR is 24 bits, and the lower 8 bits of PMSIRR are zero.

In general, secure transaction are allowed to be tagged and traced with **secure_debug_disable** register. When this bit is set, secure registers are read with non-secure access.

5.4 PMU system overview

CMN-600 includes *Performance Monitoring Unit* (PMU) capabilities.

The PMU offers these features:

- Local and global performance counters with shadow registers.
- PMU snapshot across all internal CMN-600 devices.

The PMU consists of local performance counters in the DTMs and global performance counters in the DTCs as shown in the following figure.

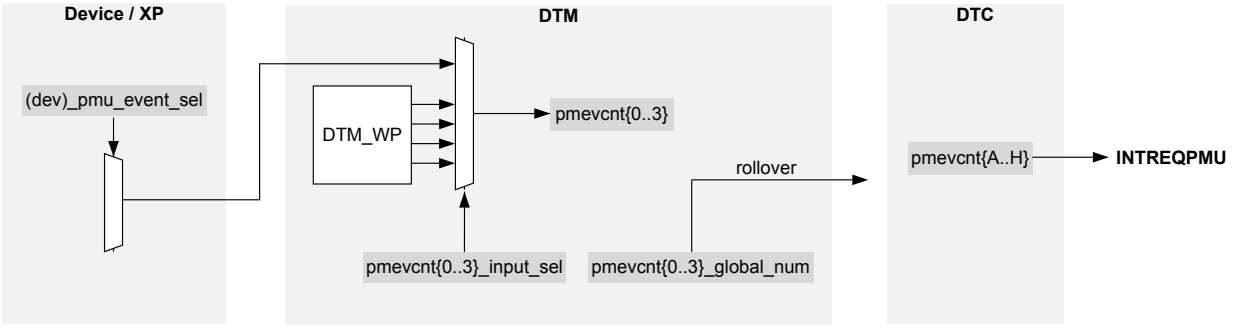

Figure 5-7 CMN-600 PMU local and global performance counters

5.5 PMU feature description

This section describes PMU features.

The PMU system performs the following tasks:

- Select PMU event from XP, the local watchpoint, and the devices on XP ports.
- Operates four local PMU counters (4 × 16b).
- Operates eight global PMU counters (8 × 32b) associated with the local counters.
- Snapshot.
- Overflow interrupt from global PMU counters.

The PMU counter value can be copied over into the shadow registers when:

- A request of snapshot via input pin PMUSNAPSHOTREQ.
- A write into **por_dt_pmsrr.ss_req** within the DTC.

On receiving a snapshot request, DTC sends the snapshot request to all DTMs. Multiple snapshot requests are collapsed into a single request. On receiving PMU snapshot packets from all DTMs, rollover information is updated at the global counters, and the counter value is copied to the shadow registers.

5.6 PMU system programming

This section contains sequences on how to program the PMU, PMU snapshot, and PMU interrupt.

This section contains the following subsections:

5.6.1 PMU counter setup

This section contains programming information for the PMU counter.

Use this procedure to setup the PMU counters.

1. NIDEN input has to be asserted for any trace and PMU operation.

2. Program **(dev)_pmu_event_set** register in the devices or XP.

3. Program **dtm_pmu_config.pmevcnt{0..3}_input_sel** to select PMU event counter inputs. The input can be from watchpoint or from selected events from devices or XP, in the step above.

4. Program **dtm_pmu_config.pmevcnt_paired** and **dtm_pmu_config.pmevcnt{0..3}_global_num** to select the paired top global PMU counters.

5. Program **dtm_pmu_config.pmevcnt{01, 23}_combined** for any combined local PMU counters.

6. Write `1'b1` to **dtm_pmu_config.pmu_en**.

——— **Note** ———

To activate CXLA PMU function, program the associated **por_cxg_ra_cfg_ctl.en_cxla_pmucmd_prop** to 1'b1.

———————————

7. Program **por_dt_pmevcnt_localnum.localnum{A..H}** to be the number of local counters that feed into this global counter.

8. Program **por_dt_pmcr.cntcfg** to pair the 32-bit global counter to make a 64-bit counter.

9. Write `1'b1` to **por_dt_pmcr.ovfl_intr_en** to enable interrupt on INTREQPMU on any global counter overflow.

10. Write `1'b1` to **por_dt_pmcr.pmu_en** to start PMU operation.

5.6.2 PMU snapshot programming

This section contains programming information for the PMU snapshot.

Use this procedure to setup the PMU counters.

1. NIDEN input has to be asserted for any trace and PMU operation.
2. Program PMU counters as described in *5.6.1 PMU counter setup* on page 5-1121.
3. Write `1'b1` to **por_dt_pmsrr.ss_req**. This causes the DTC to send a PMU snapshot instruction. On receiving this instruction, the DTM sends PMU snapshot packets to the DTC.
4. The DTC updates **por_dt_pmssr.ss_status** after receiving PMU snapshot packets.
5. Software can poll **por_dt_pmssr.ss_ss_status** to check if the snapshot process is done.
6. For a multiple-DTC system, sub-DTC maintains snapshot status for the DTM within its own domain.

5.6.3 PMU interrupt programming

This section contains programming information for the PMU interrupt.

Use this procedure to set up the PMU overflow interrupt.

1. NIDEN input must be asserted for any trace and PMU operation.
2. Program PMU counters as described in *5.6.1 PMU counter setup* on page 5-1121.

3. Write `1'b1` to **por_dt_pmcr.ovfl_intr_en**. Any PMU counter overflow asserts INTREQPMU.
4. For multiple DTCs, write `1'b1` to all **por_dt_pmcr.ovfl_intr_en** fields.
5. When observing assertion of INTREQPMU, **por_dt_pmovsr.pmovsr[7:0]** should be polled to see which global counter causes the interrupt. For multiple DTCs, all `por_dt_pmovsr` registers must be polled.
6. To clear INTREQPMU, write 1'b1 into the corresponding **por_dt_pmovsr_clr.pmovsr_clr[7:0]**.

5.7 Secure debug support

Secure debug state is controlled by SPNIDEN input and the **por_dt_por_dt_secure_access.secure_debug_disable** configuration register bit.

Secure debug is enabled when SPNIDEN is asserted, or when the **por_dt_por_dt_secure_access.secure_debug_disable** bit is LOW, which is the default value.

When secure debug is enabled, all events can be counted and all flits can be traced.

When secure debug is disabled, all events with unknown secure state are not counted and all flits with unknown secure state are not traced.

Chapter 6
Performance Optimization and Monitoring

This chapter describes performance optimization techniques for use by system integrators, and the *Performance Monitoring Unit* (PMU).

It contains the following sections:

6.1 Performance optimization guidelines

There are some restrictions when optimizing CMN-600.

To obtain maximum performance from CMN-600, the system integrator must be aware of the following information:

RN-I When request ordering is not required, transaction requests must be dispatched with non-overlapping IDs to ensure optimal bandwidth operation. Large burst transactions, that is, larger than 64B, must be split into 64B or smaller burst transactions. In addition, set **AxSIZE** to the RN-I's AXI bus width to fully utilize the available bandwidth.

For example, set AxSIZE to 4 (16B) if AXI bus width is 128 bits or set AxSIZE to 5 (32B) if AXI bus width is 256 bits.

Read or write requests to different parts of the same cache line must be combined into a single cache line request. For example, multiple (partial) WriteUnique transactions must be combined into a single WriteUnique or a single WriteLineUnique transaction, where all bytes in the cache line are written.

Based on the transaction attributes, RN-I can enforce additional ordering on transactions, targeting device memory downstream of HN-I, affecting the overall achievable bandwidth.

HN-F High temporal locality of address usage in transactions can cause same-address dependencies to occur in the event of transactions with addresses to overlapping cache lines. This results in higher latency because of serialization delays between these transactions. CMN-600 is microarchitected to avoid hot spotting in the HN-F partitions or in the memory controllers, but this is unavoidable in cases of temporally local same-address usage.

HN-I Stream of interleaved reads and writes targeting the same peripheral downstream of HN-I results in higher latencies on these transactions. It also could result in serialization delays between these reads and writes. It is recommended not to interleave read and write transactions when targeting the same peripheral.

6.2 About the Performance Monitoring Unit

CMN-600 provides access to various performance events. Some of these events are unique to and originate in a specific CMN-600 component, and some are available by using watchpoints in the *Debug Watchpoint Module* (DWM) in the XP where the component is located.

This chapter describes the performance events and the relevant use cases for most of those events. See *Chapter 5 Debug trace and PMU* on page 5-1100 for information about the infrastructure and logic that enable general utility of the performance monitor events.

The following table shows the PMU events.

Table 6-1 PMU events

Component	NS [a]	Event	Description
HN-D	Refer to *6.7 DN performance events* on page 6-1145 for event summary details.		
HN-I	No	PMU_HNI_TXDATFLITV	Transmitted data flits. Available through the DWM.
	No	PMU_HNI_RXDATFLITV	Received data flits. Available through the DWM.
	Yes	PMU_HNI_RXREQFLITV	Received requests. Available through the DWM.
	Yes	PMU_HNI_RXREQ_REQORDER	Received ReqOrder requests. Available through the DWM.
SBSX	No	PMU_SBSX_TXDATFLITV	Transmitted data flits. Available through the DWM.
	No	PMU_SBSX_RXDATFLITV	Received data flits. Available through the DWM.
	Yes	PMU_SBSX_RXREQFLITV	Received requests. Available through the DWM.
HN-F	Yes	PMU_HN_CACHE_MISS	Total cache misses
	Yes	PMU_HNL3_SF_CACHE_ACCESS	Total number of cache accesses
	Yes	PMU_HN_CACHE_FILL	Total allocations in HN SLC cache
	Yes	PMU_HN_POCQ_RETRY	Total number of requests that have been retried
	Yes	PMU_HN_POCQ_REQS_RECVD	Total number of requests that the HN received
	Yes	PMU_HN_SF_HIT	Total number of SF hits
	Yes	PMU_HN_SF_EVICTIONS	Total number of SF evictions
	Yes	PMU_HN_L3_EVICTION	Number of SLC evictions
	Yes	PMU_HN_L3_FILL_INVALID_WAY	Number of SLC fills to an invalid way
	Yes	PMU_HN_MC_RETRIES	Number of requests receiving retry response from the memory controller
	Yes	PMU_HN_MC_REQS	Total number of requests that are sent to the memory controller
	Yes	PMU_HN_QOS_HH_RETRY	Number of times HN-F protocol retried a QoS 15 (highest) class request

[a] Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

Table 6-1 PMU events (continued)

Component	NS [a]	Event	Description
RN-I, RN-D	No	PMU_RNI_RDATABEATS_P0	S0 RDataBeats
	No	PMU_RNI_RDATABEATS_P1	S1 RDataBeats
	No	PMU_RNI_RDATABEATS_P2	S2 RDataBeats
	Yes	PMU_RNI_RXDATFLITV	**RXDAT** flits received
	Yes	PMU_RNI_TXDATFLITV	**TXDAT** flits sent
	Yes	PMU_RNI_TXREQFLITV	Total **TXREQ** flits sent
	Yes	PMU_RNI_TXREQFLITV_RETRIED	Retried **TXREQ** flits sent
	No	PMU_RNI_RRTFULL	Read request tracker full
	No	PMU_RNI_WRTFULL	Write request tracker
	Yes	PMU_RNI_TXREQFLITV_REPLAYED	Replayed **TXREQ** flits
CXHA	Yes	HA_REQ_TRK_OCC	Request tracker occupancy
	Yes	HA_RD_DAT_BUFF_OCC	Read data buffer occupancy
	Yes	HA_RSP_DATA_BYPASS_BUF_OCC	CCIX response data bypass buffer occupancy
	Yes	HA_WR_DAT_BUFF_OCC [b]	Write data buffer occupancy
	Yes	HA_SNP_TRK_BUF_OCC	Snoop tracker occupancy
	Yes	HA_SNP_DAT_SINK_BUF_OCC	Snoop data sink buffer occupancy
	Yes	HA_SNP_HZD_BUF_OCC	Snoop hazard buffer occupancy
	Yes	HA_RD_DAT_BYPASS	Read data bypass taken
	Yes	HA_SNP_PCRD_STALLS_LNK0 [b]	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 0
	Yes	HA_SNP_PCRD_STALLS_LNK1 [b]	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 1
	Yes	HA_SNP_PCRD_STALLS_LNK2 [b]	Snoop request available but no SNP Pcrd to send over CCIX per LinkEnd for Link 2
	Yes	HA_CHI_RSP_UPLOAD_STALLS	Local HA upload stalls to CHI because of contention with RA
	Yes	HA_CHI_DAT_UPLOAD_STALLS	Local HA upload stalls to CHI because of contention with RA

[a] Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.
[b] If applications use only Non-secure transactions, then NS counting will be correct. If a mix of S and NS is used, then use Secure Debug such as assert SPNIDEN.

Table 6-1 PMU events (continued)

Component	NS [a]	Event	Description
CXLA	No	LA_RX_TLP_LINK0	RX TLPs on Link 0
	No	LA_RX_TLP_LINK1	RX TLPs on Link 1
	No	LA_RX_TLP_LINK2	RX TLPs on Link 2
	No	LA_TX_TLP_LINK0	TX TLPs on Link 0
	No	LA_TX_TLP_LINK1	TX TLPs on Link 1
	No	LA_TX_TLP_LINK2	TX TLPs on Link 2
	No	LA_RX_CXS_LINK0	RX CXS on Link 0
	No	LA_RX_CXS_LINK1	RX CXS on Link 1
	No	LA_RX_CXS_LINK2	RX CXS on Link 2
	No	LA_TX_CXS_LINK0	TX CXS on Link 0
	No	LA_TX_CXS_LINK1	TX CXS on Link 1
	No	LA_TX_CXS_LINK2	TX CXS on Link 2
	No	LA_RX_TLP_AVG_SIZE	Average RX TLP size in DWs
	No	LA_TX_TLP_AVG_SIZE	Average TX TLP size in DWs
	No	LA_RX_TLP_AVG_CCIX_MSGS	Average RX TLP size in CCIX messages
	No	LA_TX_TLP_AVG_CCIX_MSGS	Average TX TLP size in CCIX messages
	No	LA_RX_CXS_AVG_SIZE	Average size of RX CXS in DWs within a beat
	No	LA_TX_CXS_AVG_SIZE	Average size of TX CXS in DWs within a beat
	No	LA_TX_CXS_LCRD_BACKPRESSURE	TX CXS link credit backpressure from PHY
	No	LA_RX_TLPBUF_FULL_STALL	RX TLP buffer full and backpressured
	No	LA_TX_TLPBUF_FULL_STALL	TX TLP buffer full and backpressured
	No	LA_RX_AVG_TLP_LAT	Average latency to process an RX TLP
	No	LA_TX_AVG_TLP_LAT	Average latency to form a TX TLP

[a] Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

Table 6-1 PMU events (continued)

Component	NS [a]	Event	Description
CXRA	Yes	RA_REQ_TRK_OCC	Request tracker occupancy
	Yes	RA_SNP_TRK_OCC	Snoop tracker occupancy
	Yes	RA_RD_DAT_BUF_OCC	Read data buffer occupancy [b]
	Yes	RA_WR_DAT_BUF_OCC	Write data buffer occupancy [b]
	Yes	RA_SNP_SINK_BUF_OCC	Snoop sink buffer occupancy [b]
	Yes	RA_SNP_BCASTS	Snoop broadcasts
	Yes	RA_REQ_CHAINS	Number of request chains formed larger than one
	Yes	RA_REQ_CHAIN_AVG_LEN	Average size of request chains only for chains size larger than one
	Yes	RA_CHI_RSP_UPLOAD_STALLS	Local RA upload stalls to CHI because of contention with HA [b]
	Yes	RA_CHI_DAT_UPLOAD_STALLS	Local RA upload stalls to CHI because of contention with HA
	Yes	RA_DAT_PCRD_STALLS_LNK0	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 0 [b]
	Yes	RA_DAT_PCRD_STALLS_LNK1	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 1 [b]
	Yes	RA_DAT_PCRD_STALLS_LNK2	Memory Data Request available, but no DAT Pcrd to send over CCIX per LinkEnd 2 [b]
	Yes	RA_REQ_PCRD_STALLS_LNK0	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 0 [b]
	Yes	RA_REQ_PCRD_STALLS_LNK1	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 1 [b]
	Yes	RA_REQ_PCRD_STALLS_LNK2	Memory Data Request available but no Req Pcrd to send over CCIX per LinkEnd 2 [b]

6.2.1 Cycle counter

The cycle counter is used to track time.

You can reset this counter to initiate the time interval over which you want to capture the events.

PMU_CYCLE_COUNTER Cycle counter.

Because the cycle counter is clocked by **GCLK0**, it is not incremented during periods of *High-level Clock Gating* (HCG) when the clocks are stopped.

[a] Can the event be determined to be Secure or Non-secure? If No, the event is considered to be Secure, irrespective of Secure or Non-secure attributes associated with the event.

6.3 HN-F performance events

The HN-F performance analysis counters are used to monitor cache behavior.

For a particular cache, the cache miss or hit rate is used to measure the capacity of the cache, and the location for certain applications. To measure the cache miss rate, the performance monitor counters count the number of instances of cache accesses and cache misses.

This section contains the following subsections:

6.3.1 Cache performance

Cache performance events are required to calculate the cache miss rate and the cache allocation.

The following sections describe the cache performance events.

Cache miss rate

The cache events that are required to calculate the cache miss rate are:

PMU_HN_CACHE_MISS_EVENT	Counts the total cache misses. This is a first-time lookup result, and is high priority.
PMU_HNSLC_SF_CACHE_ACCESS_EVENT	The total number of cache accesses. These are first-time accesses, and are high priority.

Note

The performance counter architecture enables only four HNs to collect the cache miss rate. However, the CMN-600 microarchitecture is such that the cache miss rate that is measured at one HN-F is a good proxy for the cache miss rate of the remaining HN-Fs.

Calculate the cache miss rate as follows:

$$\text{Cache miss rate (\%)} = \frac{\text{Total cache misses}}{\text{Total cache accesses}} \times 100$$

Certain request types can cause multiple cache accesses:

- Lookup.
- Tag update.
- Victim selection.
- Cache fill.

Event counting is therefore limited to first time accesses only. For example, for a ReadUnique transaction that leads to an SLC hit, PMU_HNSLC_SF_CACHE_ACCESS_EVENT is only counted the first time cache lookup is performed. The tag update is not counted as a cache access. Similarly, for WriteBack or Write*Unique transactions with an SLC allocate hint, only the first instance of an SLC lookup is counted as an access and hit or miss. The eventual victim selection and cache fill are not counted as additional accesses.

Cache allocations

The cache allocation event counts the number of times an HN-F SLC cache is allocated. It provides an approximate cache usage for this particular application over a specific time slice. This event does not check whether the application has any hot sets.

PMU_HN_CACHE_FILL_EVENT Counts all cache line allocations to SLC cache.

All cache line writes, that is, Write*Unique, WriteBack, and Evictions that are allocated in SLC cache, are counted towards this event.

6.3.2 HN-F counters

Applications can bottleneck on one or more HN-Fs because they frequently target an address or a stream of addresses.

The following POCQ occupancy and request retry events are used to monitor possible performance loss in the system:

PMU_HN_POCQ_RETRY_EVENT The total number of requests that have been retried.

PMU_HN_POCQ_REQS_RECVD_EVENT The total number of requests that the HN-F receives.

Requests that cannot be queued in the POCQ, because of lack of credits, are retried. The HN-F responds with a RetryAck response, and the request waits for a static credit. This indicates whether the bottlenecks are caused by a lack of credits, and also shows if the latency of requests is very high.

Calculate the message retry rate as follows:

$$\text{HN-F message retry rate (\%)} = \frac{\text{HN-F total messages retried}}{\text{HN-F total messages received}} \times 100$$

6.3.3 SF events

There are three snoop events that can be counted.

The following sections describe the SF performance events.

SF miss rate

This event measures the amount of memory controller traffic that is generated. It can also be used to measure the efficiency of the SF.

PMU_HN_SF_HIT_EVENT Measures the number of SF hits.

Calculate the SF hit rate as follows:

$$\text{Snoop filter hit rate (\%)} = \frac{\text{Total snoop filter hits}}{\text{Total SLC lookups}} \times 100$$

SF accesses are only counted for first-time lookups, and not for the victim selection accesses or SF fills. Because the SLC lookup and SF lookups are parallel, the SLC lookups can be used to calculate the SF hit rate.

SF evictions

This event measures the frequency of SF evictions.

PMU_HN_SF_EVICTIONS_EVENT Measures the number of SF evictions when cache invalidations are initiated.

Snoops sent and received with hit rate

This event measures the amount of shared data across clusters for a specific application, using snoops hits or misses.

PMU_HN_SNOOPS_SENT_EVENT Number of snoops sent. Does not differentiate between broadcast or directed snoops.

PMU_HN_SNOOPS_BROADCAST_EVENT Number of snoop broadcasts sent.

Calculate the snoops sent and received rate as follows:

$$\text{Shared data (\%)} = \frac{\text{Total snoops broadcast}}{\text{Total snoops sent}} \times 100$$

The number of broadcast and total snoops measures the shared data invalidations.

6.3.4 System-wide events

The memory controller request retries determine whether the memory controller is the bottleneck in the system, which can cause higher request latencies.

The following events can be counted:

PMU_HN_MC_RETRIES_EVENT Number of requests that are retried to the memory controller.

PMU_HN_MC_REQS_EVENT Total number of requests that are sent to the memory controller.

Calculate the retry rate for requests to the memory controller as follows:

$$\text{MC message retry rate (\%)} = \frac{\text{MC total messages retried}}{\text{MC total messages received}} \times 100$$

6.3.5 Quality of Service

Requests with a HighHigh QoS must be allocated and processed from the POCQ with the highest priority compared to High, Medium, and Low QoS requests.

If the HighHigh requests are retried too frequently, there could be a bottleneck at a particular HN-F, or the POCQ reservation for HighHigh requests requires adjustment.

PMU_HN_QOS_HH_RETRY How often a HighHigh request is retried.

6.3.6 HN-F PMU event summary

The following table shows a summary of the HN-F PMU events.

Table 6-2 HN-F events

Number	Name	Description
1	PMU_HN_CACHE_MISS_EVENT	Counts total cache misses in first lookup result (high priority)
2	PMU_HNSLC_SF_CACHE_ACCESS_EVENT	Counts number of cache accesses in first access (high priority)
3	PMU_HN_CACHE_FILL_EVENT	Counts total allocations in HN SLC (all cache line allocations to SLC)
4	PMU_HN_POCQ_RETRY_EVENT	Counts number of retried requests
5	PMU_HN_POCQ_REQS_RECVD_EVENT	Counts number of requests received by HN
6	PMU_HN_SF_HIT_EVENT	Counts number of SF hits
7	PMU_HN_SF_EVICTIONS_EVENT	Counts number of SF eviction cache invalidations initiated
8	PMU_HN_DIR_SNOOPS_SENT_EVENT	Counts number of directed snoops sent (not including SF back invalidation)

Table 6-2 HN-F events (continued)

Number	Name	Description
9	PMU_HN_BRD_SNOOPS_SENTEVENT	Counts number of multicast snoops sent (not including SF back invalidation)
10	PMU_HN_SLC_EVICTION_EVENT	Counts number of SLC evictions (dirty only)
11	PMU_HN_SLC_FILL_INVALID_WAY_EVENT	Counts number of SLC fills to an invalid way
12	PMU_HN_MC_RETRIES_EVENT	Counts number of retried transactions by the MC
13	PMU_HN_MC_REQS_EVENT	Counts number of requests sent to MC
14	PMU_HN_QOS_HH_RETRY_EVENT	Counts number of times a HighHigh priority request is protocol-retried at the HN-F
15	PMU_HNF_POCQ_OCCUPANCY_EVENT	Counts the POCQ occupancy in HN-F. Occupancy filtering is programmed in **pmu_occup1_id**.
16	PMU_HN_POCQ_ADDRHAZ_EVENT	Counts number of POCQ address hazards upon allocation
17	PMU_HN_POCQ_ATOMICS_ADDRHAZ_EVENT	Counts number of POCQ address hazards upon allocation for atomic operations
18	PMU_HN_LD_ST_SWP_ADQ_FULL_EVENT	Counts number of times ADQ is full for Ld/St/SWP type atomic operations while POCQ has pending operations
19	PMU_HN_CMP_ADQ_FULL_EVENT	Counts number of times ADQ is full for CMP type atomic operations while POCQ has pending operations
20	PMU_HN_TXDAT_STALL_EVENT	Counts number of times HN-F has a pending TXDAT flit but no credits to upload
21	PMU_HN_TXRSP_STALL_EVENT	Counts number of times HN-F has a pending TXRSP flit but no credits to upload
22	PMU_HN_SEQ_FULL_EVENT	Counts number of times requests are replayed in SLC pipe due to SEQ being full
23	PMU_HN_SEQ_HIT_EVENT	Counts number of times a request in SLC hit a pending SF eviction in SEQ
24	PMU_HN_SNP_SENT_EVENT	Counts number of snoops sent including directed, multicast, and SF back invalidation
25	PMU_HN_SFBI_DIR_SNP_SENT_EVENT	Counts number of times directed snoops were sent due to SF back invalidation
26	PMU_HN_SFBI_BRD_SNP_SENT_EVENT	Counts number of times multicast snoops were sent due to SF back invalidation
27	PMU_HN_SNP_SENT_UNTRK_EVENT	Counts number of times snooped were sent due to untracked RNF's
28	PMU_HN_INTV_DIRTY_EVENT	Counts number of times SF back invalidation resulted in dirty line intervention from the RN
29	PMU_HN_STASH_SNP_SENT_EVENT	Counts number of times stash snoops were sent
30	PMU_HN_STASH_DATA_PULL_EVENT	Counts number of times stash snoops resulted in data pull from the RN
31	PMU_HN_SNP_FWDED_EVENT	Counts number of times data forward snoops were sent

6.4 RN-I performance events

External devices connect at an RN-I bridge.

This section contains the following subsections:

6.4.1 Bandwidth at RN-I bridges

External devices connect at an RN-I bridge.

The following events measure bandwidth at the RN-I bridges:

Requested read bandwidth at RN-I bridges

External devices connect to CMN-600 at an RN-I bridge.

To monitor the behavior of the system, the following events measure the read bandwidth at each RN-I bridge:

RDataBeats_Port0 Number of RData beats, **RVALID** and **RREADY**, dispatched on port 0. This is a measure of the read bandwidth.

RDataBeats_Port1 Number of RData beats, **RVALID** and **RREADY**, dispatched on port 1. This is a measure of the read bandwidth.

RDataBeats_Port2 Number of RData beats, **RVALID** and **RREADY**, dispatched on port 2. This is a measure of the read bandwidth.

Because CMOs are sent through the read channel, their responses are included in these events.

Calculate the read bandwidth as follows:

$$\text{Read bandwidth} = \frac{\text{Number RDataBeats\_Port}n \times \text{AXIDataBeatSize}}{\text{Cycles}} \times \text{Frequency}$$

Where AXIDataBeatSize is the number of bytes for each AXI beat. In most cases, this is the same size as the AXI bus.

Actual read bandwidth on interconnect

RXDATFLITV measures the bandwidth that an RN-I bridge sends to the interconnect.

To measure the actual bandwidth that an RN-I bridge sends to the interconnect, and not the useful bandwidth the external devices can use, this event counts the number of received data flit requests that the bridge receives through the data channel:

RXDATFLITV Number of **RXDAT** flits received. This event is a measure of the true read data bandwidth. It excludes CMOs, because CMO completions return to the RN-I through the response channel, but includes replayed requests.

This event includes the replayed requests because of the read data buffer decoupled scheme.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{RXDATFLITV} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Write bandwidth at RN-I bridges

TXDATFLITV monitors the number of data flits that the RN-I bridge sends out.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the RN-I bridge sends out, to measure the actual write bandwidth that is sent to the interconnect:

TXDATFLITV Number of **TXDAT** flits dispatched. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{TXDATFLITV x DataFlitSize}}{\text{Cycles}} \text{ x Frequency}$$

6.4.2 Bottleneck analysis at RN-I bridges

CMN-600 provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system.

This enables you to monitor the current bottlenecks in the system, and checks multiple events in the RN-Is, HN-Fs, and memory controllers. In the RN-I bridges, the events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times the read and write tracker is full and therefore cannot accept new requests in the system. This can cause delays in the AXI masters.
- The number of read request replays, because of decoupling of the read request buffers and read data buffers in the RN-I system.

Request retry rate at RN-I bridges

TXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system.

It does this by measuring the request retry rate:

TXREQFLITV_RETRIED Number of retried **TXREQ** flits dispatched. This event is a measure of the retry rate.

Calculate the request retry rate as follows:

$$\text{Retry rate} = \frac{\text{TXREQFLITV\_RETRIED}}{\text{TXREQFLITV\_TOTAL}}$$

Read and write delays at RN-I bridges

To monitor the delays for both reads and writes, CMN-600 enables you to monitor how full the read and write trackers are in the RN-I bridges.

When one of the trackers is full, the bridge cannot accept new requests from the AXI master. This delays the I/O devices that connect to the AXI master.

You can use the measure of how full the trackers are, together with the read and write bandwidth from the RN-I bridge to the interconnect, to help isolate the source of bottlenecks in the system. For example:

- If the read tracker of a specific RN-I bridge is full but the effective read bandwidth from the bridge is not close to the maximum expected, the interconnect cannot keep up with the read traffic from the specific device.
- If the bandwidth is close to maximum, the I/O device can send requests to the maximum of its port bandwidth and this is why the tracker is full.

You can also use the measure of how full the trackers are with AXI PMUs to monitor delays to the AXI masters.

The following events monitor the read and write trackers:

RRT_OCCUPANCY All entries in the read request tracker are occupied. This is a measure of oversubscription in the read request tracker.

WRT_OCCUPANCY All entries in the write request tracker are occupied. This is a measure of oversubscription in the write request tracker.

6.4.3 RN-I PMU event summary

There are twenty RN-I PMU events.

The following table shows a summary of the RN-I PMU events.

Table 6-3 RN-I PMU event summary

Number	Name	Description
1	PMU_RNI_RDATABEATS_P0	Number of RData beats, **RVALID** and **RREADY**, dispatched on port 0. This is a measure of the read bandwidth, including CMO responses.
2	PMU_RNI_RDATABEATS_P1	Number of RData beats, **RVALID** and **RREADY**, dispatched on port 1. This is a measure of the read bandwidth, including CMO responses.
3	PMU_RNI_RDATABEATS_P2	Number of RData beats, **RVALID** and **RREADY**, dispatched on port 2. This is a measure of the read bandwidth, including CMO responses.
4	PMU_RNI_RXDATFLITV	Number of **RXDAT** flits received. This is a measure of the true read data bandwidth, excluding CMOs.
5	PMU_RNI_TXDATFLITV	Number of **TXDAT** flits dispatched. This is a measure of the write bandwidth.
6	PMU_RNI_TXREQFLITV	Number of **TXREQ** flits dispatched. This is a measure of the total request bandwidth.
7	PMU_RNI_TXREQFLITV_RETRIED	Number of retried **TXREQ** flits dispatched. This is a measure of the retry rate.
8	PMU_RNI_RRT_OCCUPANCY	All entries in the read request tracker are occupied. This is a measure of oversubscription in the read request tracker.
9	PMU_RNI_WRT_OCCUPANCY	All entries in the write request tracker are occupied. This is a measure of oversubscription in the write request tracker.
10	PMU_RNI_TXREQFLITV_REPLAYED	Number of replayed TXREQ flits. This is the measure of replay rate.
11	PMU_RNI_WRCANCEL_SENT	Number of write data cancels sent. This is the measure of write cancel rate
12	PMU_RNI_WDATABEAT_P0	Number of WData beats, WVALID and WREADY , dispatched on port 0. This is a measure of write bandwidth on AXI port 0.
13	PMU_RNI_WDATABEAT_P1	Number of WData beats, WVALID and WREADY , dispatched on port 1. This is a measure of write bandwidth on AXI port 1.
14	PMU_RNI_WDATABEAT_P2	Number of WData beats, WVALID and WREADY , dispatched on port 2. This is a measure of write bandwidth on AXI port 2.
15	PMU_RNI_RRTALLOC	Number of allocations in the read request tracker. This is a measure of read transaction count
16	PMU_RNI_WRTALLOC	Number of allocations in the write request tracker. This is a measure of write transaction count
17	PMU_RNI_RDB_UNORD	Number of cycles for which Read Data Buffer state machine is in Unordered Mode.
18	PMU_RNI_RDB_REPLAY	Number of cycles for which Read Data Buffer state machine is in Replay mode

Table 6-3 RN-I PMU event summary (continued)

Number	Name	Description
19	PMU_RNI_RDB_HYBRID	Number of cycles for which Read Data Buffer state machine is in hybrid mode. Hybrid mode is where there is mix of ordered/unordered traffic.
20	PMU_RNI_RDB_ORD	Number of cycles for which Read Data Buffer state machine is in ordered Mode.

6.5 SBSX performance events

This section contains SBSX performance event information.

This section contains the following subsections:

6.5.1 Bandwidth at SBSX bridges

This section contains SBSX bridge bandwidth information.

The following events are used to measure bandwidth at the SBSX bridges:

Read bandwidth on interconnect at SBSX bridges

This section contains information on read bandwidth on interconnect at SBSX bridges.

This event counts the number of received data flits at the SBSX and interconnect:

PMU_SBSX_RXDAT Number of RXDAT flits received at XP from SBSX. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{PMU\_SBSX\_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DWM, not in the SBSX, and is defined from the XP's perspective.

Write bandwidth at SBSX bridges

This section contains information on write bandwidth at SBSX bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the SBSX receives, to measure the actual write bandwidth that is received from the interconnect:

PMU_SBSX_TXDAT Number of **TXDAT** flits dispatched from XP to SBSX. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{PMU\_SBSX\_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DWM, not in the SBSX design. The event is defined from XP’s perspective.

Total requested bandwidth at SBSX bridges

This section contains information on total requested bandwidth at SBSX bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event by monitoring the number of request flits that a SBSX bridge receives:

PMU_SBSX_TXREQ_TOTAL: Number of **TXREQ** flits dispatched from XP to SBSX. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

$$\text{Total requested bandwidth} = \frac{\text{PMU\_SBSX\_TXREQ\_TOTAL} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DWM, not in the SBSX design, and is defined from the XP's perspective.

6.5.2 Bottleneck analysis at SBSX bridges

This section contains information on bottleneck analysis at SBSX bridges.

CMN-600 provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system. This enables you to monitor the current bottlenecks in the system, and checks multiple events in all CMN-600 components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of cycles the bridge is forced to stall due to backpressures on AXI/CHI interface.

The following events are used to measure bottlenecks at the SBSX bridges:

- *6.5 SBSX performance events* on page 6-1138.
-

Request retry rate at SBSX bridges

This section contains information on the request retry rate at SBSX bridges.

RXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system. It does this by measuring the request retry rate:

RXREQFLITV_RETRIED
Number of RXREQ flits dispatched. This event is a measure of the retry rate. Calculate the retry rate as follows:
Retry rate = RXREQFLITV_RETRIED / RXREQFLITV_TOTAL

Delays at SBSX bridges due to backpressure

To analyze the delays in SBSX bridges, CMN-600 enables you to monitor the source of backpressure.

When SBSX has requests that are ready to be sent to AXI/ACE-Lite downstream, but cannot send it due to backpressure from AXI/ACE-Lite downstream, it holds the request in the *Receive Request Tracker* (RRT). This results in the RRT getting full and so the SBSX bridge cannot accept any new requests from RNs impacting system performance.

The following table contains events monitor such backpressure from AXI/ACE-Lite downstream:

Table 6-4 AXI/ACE downstream events monitor information

Events	Description
ARVALID_NO_ARREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AR channel.
AWVALID_NO_AWREADY	Number of cycles the SBSX bridge is stalled due to backpressure on AW channel.
WVALID_NO_WREADY	Number of cycles the SBSX bridge is stalled due to backpressure on W channel.

If a mesh is congested with many DAT or RSP flits, it may not give link credits to SBSX in timely manner which results in DAT flits for Reads or RSP flits for Writes getting stalled in SBSX. The following table describes events monitor in such cases where SBSX bridge is not able to upload DAT/RSP flits on the mesh.

Table 6-5 CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the TXDAT flit in SBSX bridge is waiting for link credits.
TXRSPFLITV_NO_LINKCRD	Number of cycles the TXRSP flit in SBSX bridge is waiting for link credits.

Tracker occupancy analysis

To debug performance issues, additional events are provided to measure occupancy of various trackers in SBSX such as *Request Received Tracker* (RRT), *Request Dispatch Tracker* (RDT), and *Write Data Buffers* (WDB).

Note that Read, Write, and CMO transactions occupy RRT before they are dispatched on the AXI interface. Once Read/CMO transactions are dispatched on AXI, they move from RRT to RDT. Writes remain on RRT until the write response is obtained from AXI interface and then deallocated from RRT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker, while RDT is called AXI pending tracker.

The following table contains tracker occupancy information.

Table 6-6 Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RRT
RRT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RRT
RRT_CMO_OCCUPANCY_CNT_OVFL	CMO occupancy count overflow event in RRT
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow event
RDT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RDT
RDT_CMO_OCCUPANCY_CNT_OVFL	CMO occupancy count overflow event in RDT

6.5.3 SBSX PMU event summary

This section contains SBSX PMU event summary information.

Please refer to **por_sbsx_pmu_event_sel** for more information.

6.6 HN-I performance events

This section contains HN-I performance event information.

This section contains the following subsections:

6.6.1 Bandwidth at HN-I bridges

This section contains HN-I bridge bandwidth information.

The following events are used to measure bandwidth at the HN-I bridges:

Read bandwidth on interconnect at HN-I bridges

This section contains information on read bandwidth on interconnect at HN-I bridges.

This event counts the number of received data flits at the HN-I and interconnect:

PMU_HNI_RXDAT Number of *RXDAT* flits received at XP from HN-I. This event is a measure of the read data bandwidth.

Calculate the actual read bandwidth as follows:

$$\text{Actual read bandwidth} = \frac{\text{PMU\_HNI\_RXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

The event is tracked in the DWM, not in the HN-I design. The event is defined from XP's perspective.

Write bandwidth at HN-I bridges

This section contains information on write bandwidth at HN-I bridges.

In a similar way to the read actual bandwidth event, this event monitors the number of data flits that the HN-I receives, to measure the actual write bandwidth that is received from the interconnect:

PMU_HNI_TXDAT Number of **TXDAT** flits dispatched from XP to HN-I. This event is a measure of the write bandwidth.

Calculate the write bandwidth as follows:

$$\text{Actual write bandwidth} = \frac{\text{PMU\_HNI\_TXDAT} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DWM, not in the HN-I design. The event is defined from XP's perspective.

Total requested bandwidth at HN-I bridges

This section contains information on total requested bandwidth at HN-I bridges.

To improve efficiency when using PMU events and signals, this event combines the read and write bandwidth estimation in a single event by monitoring the number of request flits that a HN-I bridge receives:

PMU_HNI_TXREQ_TOTAL: Number of **TXREQ** flits dispatched from XP to HN-I. This event is a measure of the total request bandwidth.

Calculate the total bandwidth as follows:

$$\text{Total requested bandwidth} = \frac{\text{PMU\_HNI\_TXREQ} \times \text{DataFlitSize}}{\text{Cycles}} \times \text{Frequency}$$

Note

This event is tracked in the DWM, not in the HN-I design. The event is defined from the XP's perspective.

6.6.2 Bottleneck analysis at HN-I bridges

This section contains information on bottleneck analysis at HN-I bridges.

CMN-600 provides events that observe the locations where the nodes or bridges are full, which can cause delays in the rest of the system. This enables you to monitor the current bottlenecks in the system, and checks multiple events in all CMN-600 components. The events monitor the following:

- The number of times the bridge is forced to retry because of the lack of dynamic credits.
- The number of times requests are serialized due to ordering requirements.
- The number of cycles the bridge is forced to stall due to backpressures.

The following events are used to measure bottlenecks at the HN-I bridges:

- *6.6 HN-I performance events* on page 6-1141.

Request retry rate at HN-I bridges

This section contains information on the request retry rate at HN-I bridges.

RXREQFLITV_RETRIED monitors the efficiency of using dynamic credits in the system. It does this by measuring the request retry rate:

RXREQFLITV_RETRIED: Number of **RXREQ** flits dispatched. This event is a measure of the retry rate.

Calculate the retry rate as follows:

$$\text{Retry rate} = \frac{\text{RXREQFLITV\_RETRIED}}{\text{RXREQFLITV\_TOTAL}}$$

Delays at HN-I bridges due to ordering requirements

When requests are received at the HN-I, there are different ordering guarantees HN-I bridge needs to maintain based on the source and attributes of the request.

The requests are serialized in some cases indicating a lower than expected bandwidth at HN-I as shown in the following table.

Table 6-7 PCIe and Non-PCIe RN request information

Request	Description
NONPCIE_SERIALIZED	Number of Non-PCIe RN requests that are serialized.
PCIE_SERIALIZED	Number of PCIe RN requests that are serialized.

Delays at HN-I bridges due to backpressure

To analyze the delays in HN-I bridges, CMN-600 enables you to monitor the source of backpressure.

When HN-I has requests that are ready to be sent to AXI/ACE-Lite downstream, but cannot send it due to backpressure from AXI/ACE-Lite downstream, it holds onto the request in the *Receive Request Tracker* (RRT). As a result, the RRT gets full. Therefore, the HN-I bridge cannot accept any new requests from RNs, thereby impacting system performance.

The following table contains events monitor such backpressure from AXI/ACE-Lite downstream:

Table 6-8 AXI/ACE downstream events monitor information

Events	Description
ARVALID_NO_ARREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AR channel
AWVALID_NO_AWREADY	Number of cycles the HN-I bridge is stalled due to backpressure on AW channel
WVALID_NO_WREADY	Number of cycles the HN-I bridge is stalled due to backpressure on W channel

Even if the AXI/ACE-Lite downstream is ready to accept new requests, the HN-I bridge cannot send them downstream while the *Request Dispatch Tracker* (RDT) is full. The lifetime of a request in the RDT depends on response latency from AXI/ACE-Lite downstream and backpressure on TXDAT channel.

The following table describes events monitor in such cases where an HN-I bridge is unable to send new requests to AXI/ACE-Lite downstream:

Table 6-9 AXI/ACE downstream events monitor information (no new requests sent)

Events	Description
ARREADY_NO_ARVALID	Number of cycles the AR channel is waiting for new requests from HN-I bridge
AWREADY_NO_AWVALID	Number of cycles the AW channel is waiting for new requests from HN-I bridge

If the mesh is congested with many DAT Flits, it may not give link credits to HN-I in timely manner. This delay results in the stalling of DAT flits for Reads in HN-I. The following table describes events monitor in such cases where an HN-I bridge is not able to upload a DAT flit on the mesh.

Table 6-10 CHI events monitor information

Events	Description
TXDATFLITV_NO_LINKCRD	Number of cycles the TXDAT flit in HN-I bridge is waiting for link credits

Tracker occupancy analysis in HN-I

To debug performance issues, additional events are provided to measure occupancy of various trackers in SBSX such as *Request Received Tracker* (RRT), *Request Dispatch Tracker* (RDT), and *Write Data Buffers* (WDB).

Note that Read, Write, and CMO transactions occupy RRT before they are dispatched on the AXI interface. Once Read and CMO transactions are dispatched on AXI, they move from RRT to RDT. Writes remain on RRT until the write response is obtained from AXI interface and then deallocated from RRT. Knowing the occupancy of RRT and RDT independently can inform you better about the bottleneck source. In the PMU event register description section, RRT is called request tracker while RDT is called AXI pending tracker.

The following table contains tracker occupancy information:

Table 6-11 Tracker occupancy information

Events	Description
RRT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RRT
RRT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RRT
RDT_RD_OCCUPANCY_CNT_OVFL	Read occupancy count overflow event in RDT
RDT_WR_OCCUPANCY_CNT_OVFL	Write occupancy count overflow event in RDT
WDB_OCCUPANCY_CNT_OVFL	WDB occupancy count overflow event

6.6.3 HN-I PMU event summary

This section contains HN-I PMU event summary information.

Please refer to **por_hni_pmu_event_sel** for more information.

6.7 DN performance events

This section contains DN performance event information.

The following table shows a summary of the DN PMU events.

Table 6-12 DN PMU event summary

Number	Name	Description
1	PMU_DN_RXREQ_DVMOP	Number of DVMOP requests received. This includes all the sub-types include TLB invalidate, Branch predictor invalidate, instruction cache (physical and virtual) invalidate.
2	PMU_DN_RXREQ_DVMSYNC	Number of DVM Sync requests received.
3	PMU_DN_RXREQ_DVMOP_VMID_FILTERED	Number of incoming DVMOP requests that are subject to VMID based filtering. This is a measure of the effectiveness of VMID based filtering and potential reduction in DVM snoops.
4	PMU_DN_RXREQ_RETRIED	Number of incoming requests that are retried. This is a measure of the retry rate.
5	PMU_DN_TRK_OCCUPANCY	Counts the tracker occupancy in DN.

The `pmu_occup1_id` bit field in the `por_dn_pmu_event_sel` register is used to program the occupancy counter for specific operations types. The following table summarizes the options:

Table 6-13 Field values for pmu_occup1_id

pmu_occup1_id field values	Description
4'b0000	All
4'b0001	DVM Ops
4'b0010	DVM Syncs

Note

In HN-D, DN PMU events can be accessed only when the corresponding HN-I PMU select is Zero (NONE).

DN events can be accessed via the HN-D. The **por_dn_pmu_event_sel** register will output on corresponding TXPMU output only if **por_hni_pmu_event_sel** bits 5,13, 21, and 29 are set to 0. Otherwise the value on the HN-I PMU will be available.

6.8 XP PMU event summary

This section contains XP PMU event summary information.

Each of the XP PMU events is associated with:

- one of 6 XP ports - East, West, North, South, device port0 or device port1
- one of 4 CHI channels - REQ, RSP, SNP or DAT

Up to 4 XP PMU Events can be specified using the por_mxp_pmu_event_sel register described in section 3.3.6.

The following table shows a summary of the XP PMU events.

Table 6-14 XP PMU event summary

Number	Name	Description
1	PMU_XP_TXFLIT_VALID	Number of flits transmitted on a specified port and CHI channel. This is a measure of the flit transfer bandwidth from an XP. **Note** On device ports, this event also includes link flit transfers.
2	PMU_XP_TXFLIT_STALL	Number of cycles when a flit is stalled at an XP waiting for link credits at a specified port and CHI channel. This is a measure of the flit traffic congestion on the mesh and at the flit download ports.
3	PMU_XP_PARTIAL_DAT_FLIT_VALID	Number of times when a partial DAT flit is uploaded on to the mesh from a RN-F_CHIA port. Partial DAT flit transmission occurs when XP is not able to combine two 128b DAT flits and send them over the 256b DAT channel. This can happen under 2 circumstances: 1. Only one 128b DAT flit is received within a transmission time window. 2. Two 128b DAT flits are received but they are not two halves of a single 256b word.

6.9 Occupancy and lifetime measurement using PMU events

CMN-600 has PMU events to measure the average occupancy of a tracker and measure the average lifetime of the requests in that tracker.

This event is implemented for many of the trackers in CMN-600 units (HN-F, RN-I/RN-D, HN-I, and others). The following formula measures the average occupancy and lifetime and can be applied to all the trackers where this event is supported:

Occupancy Measurement

The formula to measure the occupancy is:

$$\text{Average Occupancy (entries)} = \frac{\text{PMU\_OCCUPANCY\_EVENT} << 12}{\text{PMU\_CYCLE\_COUNTER}}$$

For example, for RN-I *Read Request Tracker* (RRT) average occupancy, the formula is:

$$\text{Average RRT Occupancy (entries)} = \frac{\text{PMU\_RNI\_RRT\_OCCUPANCY\_EVENT} << 12}{\text{PMU\_CYCLE\_COUNTER}}$$

Lifetime Measurement

If a tracker supports lifetime event, the formula to measure the lifetime is:

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU\_OCCUPANCY\_EVENT} << 12}{\text{PMU\_NUM\_TRACKER\_ALLOCATIONS}}$$

For example, for RN-I *Read Request Tracker* (RRT) average lifetime, the formula is:

$$\text{Average Lifetime (cycles)} = \frac{\text{PMU\_RNI\_RRT\_OCCUPANCY} << 12}{\text{PMU\_RNI\_RRTALLOC}}$$

6.10 DEVEVENT in CMN-600

CMN-600 HN-Fs support device specific events called DEVEVENT that are sent along with the completion of a transaction.

Completion of a transaction can be a data response (DAT) or completion response (RSP). These events contain information regarding the transaction encountering SLC hit or miss. And it also includes information about snoops sent to resolve coherency actions. These events can be measured using watch points on the XP that the RN-F is connected. Refer to *5.1.1 DTM watchpoint* on page 5-1103 for watchpoint usage.

The following table describes the DEVEVENT encodings from HN-F.

Table 6-15 DEVEVENT encodings from HN-F

Encoding	Description
`2'b00`	Line missed in SLC and no snoops sent
`2'b01`	Line missed in SLC and directed snoop sent
`2'b10`	Line missed in SLC and broadcast snoops sent
`2'b11`	Line hit in SLC and no snoops sent

Responses from other CMN-600 devices have the default `2’b00` as the DEVEVENT value.

Appendix A
Signal Descriptions

This section describes the CMN-600 I/O signals.

It contains the following sections:

A.1 About the signal descriptions

CMN-600 signals are composed of a base name along with identifiers that indicate unique product configuration.

Because there are multiple identical interfaces in CMN-600, the signal names described in this appendix are only root names, in many cases. The actual signal name includes a port-specific identifier suffix. The system configuration determines which of the signals described in this appendix are used in a particular system.

A.2 Clock and reset signals

The following table shows the CMN-600 clock and reset signals.

Table A-1 CMN-600 clock and reset signals

Signal	Type	Description	Connection information
GCLK0	Input	Primary CMN-600 clock input	Connect to global clock for CMN-600.
nSRESET	Input	CMN-600 reset, active-LOW	Connect to global reset for CMN-600.

A.3 Clock management signals

The following table shows the clock management Q-Channel signals.

Table A-2 Clock management Q-Channel signals

Signal	Type	Description	Connection information
QACTIVE_CLKCTL	Output	Indication that CMN-600 is active, and that the *External Clock Controller* (ExtCC) must not make a request for CMN-600 to prepare to stop the clocks	Connect to external clock controller.
QREQn_CLKCTL	Input	Request from the ExtCC for the CMN-600 to prepare to stop the clocks	Connect to external clock controller or tie HIGH if unused.
QACCEPTn_CLKCTL	Output	Positive acknowledgment after receiving **QREQn** assertion indicating that CMN-600 has completed preparation to stop the clocks and that the ExtCC can stop the clocks	Connect to external clock controller.
QDENY_CLKCTL	Output	Negative acknowledgment after receiving **QREQn** assertion indicating that CMN-600 has refused the request from the ExtCC to prepare to stop the clocks	

A.4 Power management signals

This section contains information on power management signals.

The following table shows the power management signals for the logic power domain.

Table A-3 Power management signals for logic power domain

Signal	Type	Description	Connection information
PREQ_LOGIC	Input	Indicates a request for a power state transition	Connect to external power management controller or tie LOW if unused.
PSTATE_LOGIC[4:0]	Input	The power state to which a transition is requested [c]	Connect to external power management controller or tie to `5'b01000` if unused.
PACCEPT_LOGIC	Output	Indicates acknowledgment of the power state transition and completion of the power state transition within the CMN-600	Connect to external power management controller.
PDENY_LOGIC	Output	Indicates denial of the power state transition	
PACTIVE_LOGIC	Output	Hint that indicates activity across the CMN-600. When LOW, indicates the possibility of entering static retention or the OFF state.	

Note

The system cannot be powered down if **PACTIVE_LOGIC** is asserted.

[c] If *MultiCycle Path* (MCP), the MCP duration must be ≤8 cycles to the last flop to receive this signal. This is a requirement for implementation.

A.5 Interrupt and event signals

The following table shows the interrupt and event signals.

——— **Note** ———

All signal names in this section are only a root name indicated as **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

CMN-600 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

———————————

Table A-4 Interrupt and event signals

Signal	Type	Description	Connection information
INTREQPPU	Output	Power state transition complete	Connect to external interrupt control logic or Generic Interrupt Controller.
INTREQPMU_NID<x>	Output	PMU count overflow interrupt. NID indicates node ID where <x> represents the NodeID number for that HN-D/DTC or HN-T/DTC.	
INTREQERRNS	Output	Non-secure error handling interrupt	
INTREQERRS	Output	Secure error handling interrupt	
INTREQFAULTNS	Output	Non-secure fault handling interrupt	
INTREQFAULTS	Output	Secure fault handling interrupt	

A.6 Configuration input signals

The following table shows the configuration input signals.

All of these signals must be stable at least ten cycles before deassertion of reset and must remain stable throughout the operation of the CMN-600, until a following reset assertion or power down, if any.

Table A-5 General configuration input signals

Signal	Type	Description	Connection information
CFGM_PERIPHBASE[47:26]	Input	Base address [47:26] of the CMN-600 configuration register space	Tie as required for system memory map.

A.7 Device population signals

The following table shows the RN-D ACE-Lite+DVM device population signals.

These signals are present only when CMN-600 has been configured to include the relevant RN-D bridge.

Table A-6 RN-D ACE-Lite+DVM device population signals

Signal	Type	Description	Connection information
ACCHANNELEN_S0_NID<x>	Input	Indicates that the RN-D bridge at NodeID <x> is populated and AMBA slave port 0 for NodeID <x> is of type ACE-Lite+DVM and includes a device which responds to DVM messages on the AC channel. **0** DVM-capable device is not populated. **1** DVM-capable device is populated.	Tie as required for system configuration.
ACCHANNELEN_S1_NID<x>	Input	Indicates that the RN-D bridge at NodeID <x> is populated and AMBA slave port 1 for NodeID <x> is of type ACE-Lite+DVM and includes a device which responds to DVM messages on the AC channel. **0** DVM-capable device is not populated. **1** DVM-capable device is populated.	
ACCHANNELEN_S2_NID<x>	Input	Indicates that the RN-I bridge at NodeID <x> is populated and AMBA slave port 2 for NodeID <x> is of type ACE-Lite+DVM and includes a device which responds to DVM messages on the AC channel. **0** DVM-capable device is not populated. **1** DVM-capable device is populated.	

A.8 CHI interface signals

CMN-600 uses channels that form an inbound and outbound CHI interface for each device using signals that form each channel in a specific interface.

The *Arm AMBA® 5 CHI Architecture Specification* defines four channels:

- *Request* (REQ).
- *Response* (RSP).
- *Snoop* (SNP).
- *Data* (DAT).

Note

All signal names in this section are only a root name, **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

- CMN-600 interface signal name == **RootName_NID#**, where # is the node ID corresponding to the specific interface.

This section contains the following subsections:

- *A.8.1 Per-device interface definition* on page Appx-A-1157.
- *A.8.2 Per-channel interface signals* on page Appx-A-1158.
- *A.8.3 Non-channel-specific interface signals* on page Appx-A-1161.

A.8.1 Per-device interface definition

Each CHI device included in a CMN-600 system has distinct functionality, and the requirements and configuration of its respective CHI interfaces differ.

The requirements and configuration for the CHI interfaces are as follows:

External RN-F interface

The RN-F interface consists of a request channel, snoop channel, and two response channels, one in each direction, as the following figure shows.

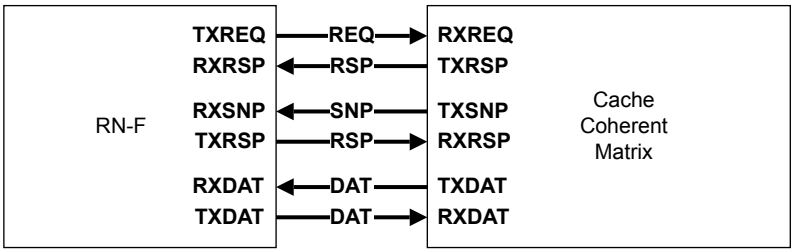

Figure A-1 External RN-F interface

It also has two data channels, one in each direction, for data transfers. CMN-600 receives request messages from the RN-F and sends responses to it. In addition, CMN-600 sends snoop messages to the RN-F and receives snoop response messages.

External SN-F interface

The SN-F interface consists of a request channel and a response channel as the following figure shows.

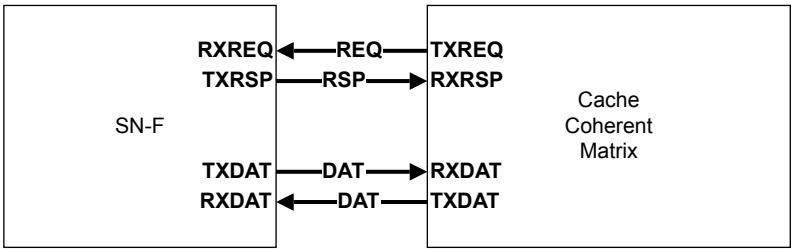

Figure A-2 External SN-F interface

It also has two data channels, one in each direction, for data transfers. The SN-F receives request messages from CMN-600 and returns response messages.

A.8.2 Per-channel interface signals

For communication between devices, each channel includes a *Transmit* (TX) and a *Receive* (RX) port, with various interface signals traveling from TX to RX.

Note

Connection of CHI interfaces between two devices requires cross-coupling of the **TX*** and **RX*** signals between the two devices, as required by the CHI architecture.

The following table shows the Transmit Request channel signals.

Table A-7 Transmit Request channel signals

Signal	Type	Description	Connection information
TXREQFLITPEND	Output	Transmit Request Early Flit Valid hint	Connect to **RXREQFLITPEND** of the corresponding CHI device, if populated.
TXREQFLITV	Output	Transmit Request Flit Valid	Connect to **RXREQFLITV** of the corresponding CHI device, if populated.
TXREQFLIT[n:0][d]	Output	Transmit Request Flit	Connect to **RXREQFLIT** of the corresponding CHI device, if populated.
TXREQLCRDV	Input	Transmit Request channel link layer credit	Connect to **RXREQLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Response channel signals.

Table A-8 Transmit Response channel signals

Signal	Type	Description	Connection information
TXRSPFLITPEND	Output	Transmit Response Early Flit Valid hint	Connect to **RXRSPFLITPEND** of the corresponding CHI device, if populated.
TXRSPFLITV	Output	Transmit Response Flit Valid	Connect to **RXRSPFLITV** of the corresponding CHI device, if populated.

[d] The value of n is configuration-dependent.

Table A-8 Transmit Response channel signals (continued)

Signal	Type	Description	Connection information
TXRSPFLIT[n:0][e]	Output	Transmit Response Flit	Connect to **RXRSPFLIT** of the corresponding CHI device, if populated.
TXRSPLCRDV	Input	Transmit Response channel link layer credit	Connect to **RXRSPLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Snoop channel signals.

Table A-9 Transmit Snoop channel signals

Signal	Type	Description	Connection information
TXSNPFLITPEND	Output	Transmit Snoop Early Flit Valid hint	Connect to **RXSNPFLITPEND** of the corresponding CHI device, if populated.
TXSNPFLITV	Output	Transmit Snoop Flit Valid	Connect to **RXSNPFLITV** of the corresponding CHI device, if populated.
TXSNPFLIT[n:0][f]	Output	Transmit Snoop Flit	Connect to **RXSNPFLIT** of the corresponding CHI device, if populated.
TXSNPLCRDV	Input	Transmit Snoop channel link layer credit	Connect to **RXSNPLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Transmit Data channel signals.

Table A-10 Transmit Data channel signals

Signal	Type	Description	Connection information
TXDATFLITPEND	Output	Transmit Data Early Flit Valid hint	Connect to **RXDATFLITPEND** of the corresponding CHI device, if populated.
TXDATFLITV	Output	Transmit Data Flit Valid	Connect to **RXDATFLITV** of the corresponding CHI device, if populated.
TXDATFLIT[n:0][g]	Output	Transmit Data Flit	Connect to **RXDATFLIT** of the corresponding CHI device, if populated.
TXDATLCRDV	Input	Transmit Data channel link layer credit	Connect to **RXDATLCRDV** of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Receive Request channel signals.

Table A-11 Receive Request channel signals

Signal	Type	Description	Connection information
RXREQFLITPEND	Input	Receive Request Early Flit Valid hint	Connect to **TXREQFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQFLITV	Input	Receive Request Flit Valid	Connect to **TXREQFLITV** of the corresponding processor, if populated, otherwise tie LOW.

[e] The value of n is configuration-dependent.
[f] The value of n is configuration-dependent.
[g] The value of n is configuration-dependent.

Table A-11 Receive Request channel signals (continued)

Signal	Type	Description	Connection information
RXREQFLIT[n:0][h]	Input	Receive Request Flit	Connect to **TXREQFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXREQLCRDV	Output	Receive Request channel link layer credit	Connect to **TXREQLCRDV** of the corresponding CHI device, if populated.

The following table shows the Receive Response channel signals.

Table A-12 Receive Response channel signals

Signal	Type	Description	Connection information
RXRSPFLITPEND	Input	Receive Response Early Flit Valid hint	Connect to **TXRSPFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPFLITV	Input	Receive Response Flit Valid	Connect to **TXRSPFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXRSPFLIT[n:0][i]	Input	Receive Response Flit	Connect to **TXRSPFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXRSPLCRDV	Output	Receive Response channel link layer credit	Connect to **TXRSPLCRDV** of the corresponding CHI device, if populated.

The following table shows the Receive Snoop channel signals.

Table A-13 Receive Snoop channel signals

Signal	Type	Description	Connection information
RXSNPFLITPEND	Input	Receive Snoop Early Flit Valid hint	Connect to **TXSNPFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPFLITV	Input	Receive Snoop Flit Valid	Connect to **TXSNPFLITV** of the corresponding processor, if populated, otherwise tie LOW.
RXSNPFLIT[n:0][j]	Input	Receive Snoop Flit	Connect to **TXSNPFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXSNPLCRDV	Output	Receive Snoop channel link layer credit	Connect to **TXSNPLCRDV** of the corresponding CHI device, if populated.

The following table shows the Receive Data channel signals.

Table A-14 Receive Data channel signals

Signal	Type	Description	Connection information
RXDATFLITPEND	Input	Receive Data Early Flit Valid hint	Connect to **TXDATFLITPEND** of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATFLITV	Input	Receive Data Flit Valid	Connect to **TXDATFLITV** of the corresponding processor, if populated, otherwise tie LOW.

[h] The value of n is configuration-dependent.
[i] The value of n is configuration-dependent.
[j] The value of n is configuration-dependent.

Table A-14 Receive Data channel signals (continued)

Signal	Type	Description	Connection information
RXDATFLIT[n:0][k]	Input	Receive Data Flit	Connect to **TXDATFLIT** of the corresponding CHI device, if populated, otherwise tie LOW.
RXDATLCRDV	Output	Receive Data channel link layer credit	Connect to **TXDATLCRDV** of the corresponding CHI device, if populated.

A.8.3 Non-channel-specific interface signals

Every transmit and receive link layer interface includes additional signals that exist only at the interface level and are not channel specific.

The following table shows the LinkActive interface signals.

Table A-15 Receive LinkActive interface signals

Signal	Type	Description	Connection information
RXLINKACTIVEREQ	Input	Receive channel LinkActive request from adjacent transmitter device	Connect to **TXLINKACTIVEREQ** of the corresponding CHI device, if populated, otherwise tie LOW.
RXLINKACTIVEACK	Output	Receive channel LinkActive acknowledgment to adjacent transmitter device	Connect to **TXLINKACTIVEACK** of the corresponding CHI device, if populated.
TXLINKACTIVEREQ	Output	Transmit channel LinkActive request to adjacent receiver device	Connect to **RXLINKACTIVEREQ** of the corresponding CHI device, if populated.
TXLINKACTIVEACK	Input	Transmit channel LinkActive acknowledgment from adjacent receiver device	Connect to **RXLINKACTIVEACK** of the corresponding CHI device, if populated, otherwise tie LOW.

The following table shows the Sactive interface signals.

Table A-16 Sactive interface signals

Signal	Type	Description	Connection information
RXSACTIVE	Input	Indication from the adjacent CHI device that it has one or more outstanding protocol-layer transactions. **RXSACTIVE** must remain asserted throughout the lifetime of the transaction.	Connect to **TXSACTIVE** of the corresponding CHI device.
TXSACTIVE	Output	Indication to the adjacent CHI device that CMN-600 has one or more outstanding protocol-layer transactions. **TXSACTIVE** remains asserted throughout the lifetime of the transaction.	Connect to **RXSACTIVE** of the corresponding CHI device.

The following table shows the hardware coherency interface signals.

[k] The value of n is configuration-dependent.

Table A-17 Hardware coherency interface signals

Signal	Type	Description	Connection information
SYSCOREQ	Input	Request to enter CHI coherence domain when asserted and to exit the CHI coherence domain when deasserted. **SYSCOREQ** and **SYSCOACK** implement a four-phase handshake protocol.	Connect to **SYSCOREQ** of corresponding CHI device, if populated, otherwise tie LOW.
SYSCOACK	Output	Acknowledge CHI coherence domain entry/exit request	Connect to **SYSCOACK** of corresponding CHI device, if populated.

A.9 ACE-Lite and AXI Interface signals

CMN-600 interfaces use **RootName** signal name within a more fully specified convention.

Note

All signal names in this section consist of a root name, **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

- CMN-600 ACE-Lite and AXI interface signal name == **RootName_[S|M]<#a>_NID#b**, where:

  S|M Defines either a slave or master interface.

  $\#_a$ Defines an optional interface identifier for a node that can support multiple AMBA interfaces.

  $\#_b$ Defines the node ID corresponding to the specific interface.

Multi-bit signals append the bit-range identifier included in the **RootName** to the end of the full signal name.

This section contains the following subsections:

- *A.9.1 ACE-Lite-with-DVM slave interface signals* on page Appx-A-1163.
- *A.9.2 AXI/ACE-Lite master interface signals* on page Appx-A-1168.
- *A.9.3 A4S Signal list* on page Appx-A-1171.

A.9.1 ACE-Lite-with-DVM slave interface signals

This interface is present as the ACE-Lite-with-DVM slave port for an RN-D bridge. The signal descriptions show which signals specific to DVM functionality are not present in an ACE-Lite interface without DVM.

The following table shows the clock and power management signals.

Table A-18 Clock and power management signals

Signal	Type	Description	Connection information
ACLKEN_S	Input	AXI bus clock enable	Connect to clock enable logic. Tie HIGH if RN-I port is unused.
ACWAKEUP_S	Output	Indication that the interconnect is starting a transaction that is being sent to the DVM master (SMMU)	Connect to corresponding master device, if populated.
AWAKEUP_S	Input	Indication that the master is starting a transaction that is being sent to the interconnect	Connect to corresponding master device, if populated, otherwise tie LOW.
RNID_SAM_STALL_DIS	Input	Disables RN SAM programming stall for specified RN	Tie HIGH if boot programming, including RN SAM, is done through this RN-I port. Otherwise, tie LOW.
SYSCOREQ_S	Input	Request to enter DVM domain when asserted and to exit the DVM domain when deasserted. SYSCOREQ and SYSCOACK implement a four-phase handshake protocol.	Connect to corresponding master device. Tie LOW if master is not populated or does have port.
SYSCOACK_S	Output	Acknowledge for DVM domain entry/exit	Connect to corresponding master device, if populated.

The following table shows the Write Address Channel signals.

Table A-19 Write Address Channel signals

Signal	Type	Description	Connection information
AWREADY_S	Output	Write address ready	Connect to corresponding master device, if populated.
AWVALID_S	Input	Write address valid	Connect to corresponding master device, if populated, otherwise tie LOW.
AWID_S[10:0]	Input	Write address ID	
AWADDR_S[n:0][1]	Input	Write address	
AWLEN_S[7:0]	Input	Write burst length	
AWSIZE_S[2:0]	Input	Write burst size	
AWBURST_S[1:0]	Input	Write burst type	
AWLOCK_S	Input	Write lock type	
AWCACHE_S[3:0]	Input	Write memory type	
AWUSER_S[n:0]	Input. Where n = REQ_RSVDC_WIDTH.	User-defined signal	
AWPROT_S[2:0]	Input	Write protection type	
AWQOS_S[3:0]	Input	Write Quality of Service identifier	
AWSNOOP_S[3:0]	Input	Write transaction type	
AWDOMAIN_S[1:0]	Input	Write shareability domain	
AWATOP[5:0]	Input	Atomic Operation	Tie LOW.
AWSTASHNID[10:0]	Input	Indicates the node identifier of the physical interface that is the target interface for the cache stash operation	Connect to corresponding master device, if populated, otherwise tie LOW.
AWSTASHNIDEN	Input	When asserted, indicates that the AWSTASHNID signal is valid and should be used	Connect to corresponding master device, if populated, otherwise tie LOW.
AWSTASHLPID[4:0]	Input	Indicates the logical processor sub-unit associated with the physical interface that is the target for the cache stash operation	Connect to corresponding master device, if populated, otherwise tie LOW.
AWSTASHLPIDEN	Input	When asserted, indicates that the AWSTASHLPID signal is enabled and should be used	Connect to corresponding master device, if populated, otherwise tie LOW.
AWTRACE	Input	Trace signal associated with the AW Write Address channel	Connect to corresponding master device, if populated, otherwise tie LOW.

The following table shows the Write Data Channel signals.

[1] The value of n is configuration-dependent.

Table A-20 Write Data Channel signals

Signal	Type	Description	Connection information
WREADY_S	Output	Write data ready	Connect to corresponding master device, if populated.
WVALID_S	Input	Write data valid	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATA_S[n:0][m]	Input	Write data	Connect to corresponding master device, if populated, otherwise tie LOW.
WSTRB_S[d:0] The value of d = (n/8 -1).	Input	Write byte-lane strobes	Connect to corresponding master device, if populated, otherwise tie LOW.
WLAST_S	Input	Write data last transfer indication	Connect to corresponding master device, if populated, otherwise tie LOW.
WUSER_S[0]	Input	WDATACHK Valid	Connect to corresponding master device, if populated, otherwise tie LOW.
WTRACE	Input	Trace signal associated with the Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.
WPOISON[p:0]	Input	Poison signal associated with the W Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATACHK[d:0] The value of d = (n/8 -1).	Input	Datacheck signal associated with the Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.

The following table shows the Write Response Channel signals.

Table A-21 Write Response Channel signals

Signal	Type	Description	Connection information
BREADY_S	Input	Write response ready	Connect to corresponding master device, if populated, otherwise tie LOW.
BVALID_S	Output	Write response valid	Connect to corresponding master device, if populated.
BID_S[10:0]	Output	Write response ID	
BRESP_S[1:0]	Output	Write response	
BUSER_S[3:0]	Output	User response signal	
BTRACE	Output	Trace signal associated with the Write Response channel	Connect to corresponding master device, if populated.

The following table shows the Read Address Channel signals.

[m] The value of n is configuration-dependent.

Table A-22 Read Address Channel signals

Signal	Type	Description	Connection information
ARREADY_S	Output	Read address ready	Connect to corresponding master device, if populated.
ARVALID_S	Input	Read address valid	Connect to corresponding master device, if populated, otherwise tie LOW.
ARID_S[10:0]	Input	Read address ID	
ARADDR_S[n:0][n]	Input	Read address	
ARLEN_S[7:0]	Input	Read burst length	
ARSIZE_S[2:0]	Input	Read burst size	
ARBURST_S[1:0]	Input	Read burst type	
ARLOCK_S	Input	Read lock type	
ARCACHE_S[3:0]	Input	Read cache type	
ARUSER_S[n:0]	Input. Where n = REQ_RSVDC_WIDTH.	User-defined signal	
ARPROT_S[2:0]	Input	Read protection type	
ARQOS_S[3:0]	Input	Read Quality of Service value	
ARSNOOP_S[3:0]	Input	Read transaction type	
ARDOMAIN_S[1:0]	Input	Read shareability domain	
ARTRACE	Input	Trace signal associated with the Read Address channel	Connect to corresponding master device, if populated, otherwise tie LOW.

The following table shows the Read Data Channel signals.

Table A-23 Read Data Channel signals

Signal	Type	Description	Connection information
RREADY_S	Input	Read data ready	Connect to corresponding master device, if populated, otherwise tie LOW.
RVALID_S	Output	Read data valid	Connect to corresponding master device, if populated.
RID_S[10:0]	Output	Read data ID	Connect to corresponding master device, if populated.
RDATA_S[n:0][o]	Output	Read data	Connect to corresponding master device, if populated.
RRESP_S[1:0]	Output	Read data response	Connect to corresponding master device, if populated.
RLAST_S	Output	Read data last transfer indication	Connect to corresponding master device, if populated.

[n] The value of n is configuration-dependent.
[o] The value of n is configuration-dependent.

Table A-23 Read Data Channel signals (continued)

Signal	Type	Description	Connection information
RUSER_S[0:0]	Output.	RDATACHK valid signal	Connect to corresponding master device, if populated
RTRACE	Output	Trace signal associated with the Read Data channel	Connect to corresponding master device, if populated.
RPOISON[p-1]	Output	Poison signal associated with the Read Data channel	Connect to corresponding master device, if populated.
RDATACHK[d:0] The value of d is d = (n/8 -1).	Output	Datacheck signal associated with the Read Data channel	Connect to corresponding master device, if populated.

The following table shows the Snoop Address Channel signals. These signals are not included in an ACE-Lite interface without DVM.

Table A-24 Snoop Address Channel signals

Signal	Type	Description	Connection information
ACREADY_S	Input	Snoop address ready	Connect to corresponding master device, if populated, otherwise tie LOW.
ACVALID_S	Output	Snoop address valid	Connect to corresponding master device, if populated.
ACADDR_S[n:0][p]	Output	Snoop address	
ACSNOOP_S[3:0]	Output	Snoop transaction type	
ACPROT_S[2:0]	Output	Snoop protection type	
ACVMIDEXT[3:0]	Output	Snoop Address VMID Extension	
ACTRACE	Output	Snoop address trace	

The following table shows the Snoop Response Channel signals. These signals are not included in an ACE-Lite interface without DVM.

Table A-25 Snoop Response Channel signals

Signal	Type	Description	Connection information
CRREADY_S	Output	Snoop response ready	Connect to corresponding master device, if populated.
CRVALID_S	Input	Snoop response valid	Connect to corresponding master device, if populated, otherwise tie LOW.
CRRESP_S[4:0]	Input	Snoop response	
CRTRACE	Input	Snoop response trace	

Note

WUSER_S[0] acts as a WDATACHK valid signal when DATACHECK_EN parameter is enabled.

- If WUSER_S[0]=0, RNI/RND synthesizes the correct WDATACHK value before sending it on CHI write request.
- If WUSER_S[0]=1, RNI/RND uses WDATACHK pin value to drive on CHI write request.

[p] The value of n is configuration-dependent.

WUSER_S[0] input is ignored if DATACHECK_EN parameter is not enabled.

Note

RUSER_S[0] acts as a RDATACHK valid signal. Since RNI/RND always drives RDATACHK value , RUSER_S[0] is set to 1 when DATACHECK_EN parameter is enabled.

RUSER_S[0] output is set to 0 if DATACHECK_EN parameter is not enabled.

A.9.2 AXI/ACE-Lite master interface signals

HN-I and SBSX have an AXI/ACE-Lite master interface.

The following table shows the clock enable signal.

Table A-26 Clock enable signal

Signal	Type	Description	Connection information
ACLKEN_M	Input	AXI Master bus clock enable	Connect to clock-enable logic.
AWAKEUP_M	Output	Indication that CMN-600 is starting an AXI transaction	Connect to corresponding slave device, if populated.

The following table shows the Write Address Channel signals.

Table A-27 Write Address Channel signals

Signal	Type	Description	Connection information
AWREADY_M	Input	Write address ready	Connect to corresponding slave device, if populated, otherwise tie LOW.
AWVALID_M	Output	Write address valid	Connect to corresponding slave device, if populated.
AWID_M[10:0]	Output	Write address ID	
AWADDR_M[n:0][q]	Output	Write address	
AWLEN_M[7:0]	Output	Write burst length	
AWSIZE_M[2:0]	Output	Write burst size	
AWBURST_M[1:0]	Output	Write burst type	
AWLOCK_M	Output	Write lock type	
AWCACHE_M[3:0]	Output	Write cache type	
AWUSER_M[n:0]	Output. Where n = REQ_RSVDC_WIDTH.	User signal	
AWPROT_M[2:0]	Output	Write protection type	
AWQOS_M[3:0]	Output	Write Quality of Service value	
AWSNOOP_M[3:0]	Output	Shareable write transaction type	
AWDOMAIN_M[1:0]	Output	Write shareability domain	
AWTRACE_M	Output	-	

[q] The value of n is configuration-dependent.

The following table shows the Write Data Channel signals.

Table A-28 Write Data Channel signals

Signal	Type	Description	Connection information
WREADY_M	Input	Write data ready	Connect to corresponding slave device, if populated, otherwise tie LOW.
WVALID_M	Output	Write data valid	Connect to corresponding slave device, if populated.
WDATA_M[n:0][sr]	Output	Write data	Connect to corresponding slave device, if populated.
WSTRB_M[n:0] [tr]	Output	Write byte-lane strobes	Connect to corresponding slave device, if populated.
WLAST_M	Output	Write data last transfer indication	Connect to corresponding slave device, if populated.
WUSER_M[0:0]	Output	WDATACHK valid signal	Connect to corresponding slave device, if populated.
WPOISONM[p:0] The value of p = (n/64) - 1.	Output	Poison signal associated with the Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.
WDATACHKM[d:0] The value of d = (n/8 -1).	Output	Datacheck signal associated with the Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.
WTRACEM	Output	Trace signal associated with the Write Data channel	Connect to corresponding master device, if populated, otherwise tie LOW.

The following table shows the Write Response Channel signals.

Table A-29 Write Response Channel signals

Signal	Type	Description	Connection information
BREADY_M	Output	Write response ready	Connect to corresponding slave device, if populated.
BVALID_M	Input	Write response valid	Connect to corresponding slave device, if populated, otherwise tie LOW.
BID_M[10:0]	Input	Write response ID	
BRESP_M[1:0]	Input	Write response	
BUSER_M[3:0]	Input	User signal	
BTRACEM	Input	-	

The following table shows the Read Address Channel signals.

[r] **WDATA** is configurable to 128 bits or 256 bits. **WSTRB** scales accordingly.
[s] The value of n is configuration-dependent.
[t] The value of n is configuration-dependent.

Table A-30 Read Address Channel signals

Signal	Type	Description	Connection information
ARREADY_M	Input	Read address ready	Connect to corresponding slave device, if populated, otherwise tie LOW.
ARVALID_M	Output	Read address valid	Connect to corresponding slave device, if populated.
ARID_M[10:0]	Output	Read address ID	
ARADDR_M[n:0][u]	Output	Read address	
ARLEN_M[7:0]	Output	Read burst length	
ARSIZE_M[2:0]	Output	Read burst size	
ARBURST_M[1:0]	Output	Read burst type	
ARLOCK_M	Output	Read lock type	
ARCACHE_M[3:0]	Output	Read cache type	
ARUSER_M[n:0]	Output, where n = `REQ_RSVDC_WIDTH`.	User signal	
ARPROT_M[2:0]	Output	Read protection type	
ARQOS_M[3:0]	Output	Read Quality of Service value	
ARSNOOP_M[3:0]	Output	Shareable read transaction type	
ARDOMAIN_M[1:0]	Output	Read shareability domain	
ARTRACEM	Output	-	

The following table shows the Read Data Channel signals.

Table A-31 Read Data Channel signals

Signal	Type	Description	Connection information
RREADY_M	Output	Read data ready	Connect to corresponding slave device, if populated.
RVALID_M	Input	Read data valid	Connect to corresponding slave device, if populated, otherwise tie LOW.
RID_M[10:0]	Input	Read data ID	Connect to corresponding slave device, if populated, otherwise tie LOW.
RDATA_M[127:0]/[255:0]	Input	Read data	Connect to corresponding slave device, if populated, otherwise tie LOW.
RRESP_M[1:0]	Input	Read data response	Connect to corresponding slave device, if populated, otherwise tie LOW.
RLAST_M	Input	Read data last transfer indication	Connect to corresponding slave device, if populated, otherwise tie LOW.
RUSER_M[0:0]	Input	RDATACHK valid signal	Connect to corresponding slave device, if populated, otherwise tie LOW.

[u] The value of n is configuration-dependent.

Table A-31 Read Data Channel signals (continued)

Signal	Type	Description	Connection information
RPOISONM[p:0] The value of p = (n/64) - 1.	Input	Poison signal associated with the Read Data channel	Connect to corresponding master device, if populated.
RDATACHKM[d:0] The value of d = (n/8 -1).	Input	Datacheck signal associated with the Read Data channel	Connect to corresponding master device, if populated.
RTRACEM	Input	Trace signal associated with the Read Data channel	Connect to corresponding master device, if populated.

Note

RUSER_M[0] acts as a RDATACHK valid signal when DATACHECK_EN parameter is enabled.

- If RUSER_M[0]=0, SBSX/HNI synthesizes the correct RDATACHK value before sending it on CHI read data response.
- If RUSER_M[0]=1, SBSX/HNI uses RDATACHK pin value to drive on CHI read data response.

RUSER_M[0] input is ignored if DATACHECK_EN parameter is not enabled.

Note

WUSER_M[0] acts as a WDATACHK valid signal. Since SBSX/HNI always drives WDATACHK value , WUSER_M[0] is set to 1 when DATACHECK_EN parameter is enabled.

WUSER_M[0] output is driven to 0 if DATACHECK_EN parameter is not enabled.

A.9.3 A4S Signal list

The A4S interface signals are listed in the following tables.

Table A-32 A4S Transmit signals

Signal	Type	Description	Connection information
TXA4STREADY	Input	TXA4STREADY indicates that the slave can accept a transfer in the current cycle.	Connect from RXA4STREADY of the A4S slave, if populated, otherwise tie LOW.
TXA4STVALID	Output	TXA4STVALID indicates that the master is driving a valid transfer. A transfer takes place when both TXA4STVALID and TXA4STREADY are asserted.	Connect to RXA4STVALID of the A4S slave, if populated.
TXA4STDEST[7:0]	Output	8'b0	TXA4STDEST is always zero.
TXA4STID[7:0]	Output	TXA4STID is the data stream identifier that indicates different streams of data.	Connect to RXA4STID of the A4S slave, if populated.
TXA4STDATA[63:0]	Output	TXA4STDATA is the primary payload that is used to provide the data that is passing across the interface.	Connect to RXA4STDATA of the A4S slave, if populated.
TXA4STSTRB[7:0]	Output	TXA4STSTRB is the byte qualifier that indicates whether the content of the associated byte of TXA4STDATA is processed as a data byte or a position byte.	Connect to RXA4STSTRB of the A4S slave, if populated.

Table A-32 A4S Transmit signals (continued)

Signal	Type	Description	Connection information
TXA4STKEEP[7:0]	Output	TXA4STKEEP is the byte qualifier that indicates whether the content of the associated byte of TDATA is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier deasserted are null bytes and can be removed from the data stream.	Connect to RXA4STKEEP of the A4S slave, if populated.
TXA4STLAST	Output	TXA4STLAST indicates the boundary of a packet.	Connect to RXA4STLAST of the A4S slave, if populated.

Table A-33 A4S Receive signals

Signal	Type	Description	Connection information
RXA4STREADY	Output	RXA4STREADY indicates that the slave can accept a transfer in the current cycle.	Connect to TXA4STREADY of the A4S master, if populated.
RXA4STVALID	Input	RXA4STVALID indicates that the master is driving a valid transfer. A transfer takes place when both RXA4STVALID and RXA4STREADY are asserted.	Connect from TXA4STVALID of the A4S master, if populated, otherwise tie LOW.
RXA4STDEST[7:0]	Input	RXA4STDEST provides routing information for the data stream.	Connect from TXA4STDEST of the A4S master, if populated, otherwise tie LOW.
RXA4STID[7:0]	Input	RXA4STID is the data stream identifier that indicates different streams of data.	Connect from TXA4STID of the A4S master, if populated, otherwise tie LOW.
RXA4STRI[7:0]	Input	RXA4STID is the chip to chip routing information that indicates RA ID of the other chip.	Connect from TXA4STRI of the A4S master, if populated, otherwise tie LOW.
RXA4STDATA[63:0]	Input	RXA4STDATA is the primary payload that is used to provide the data that is passing across the interface.	Connect from TXA4STDATA of the A4S master, if populated, otherwise tie LOW.
RXA4STSTRB[7:0]	Input	RXA4STSTRB is the byte qualifier that indicates whether the content of the associated byte of RXA4STDATA is processed as a data byte or a position byte.	Connect from TXA4STSTRB of the A4S master, if populated, otherwise tie LOW.
RXA4STKEEP[7:0]	Input	RXA4STKEEP is the byte qualifier that indicates whether the content of the associated byte of TDATA is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier deasserted are null bytes and will be removed from the data stream.	Connect from TXA4STKEEP of the A4S master, if populated, otherwise tie LOW.
RXA4STLAST	Input	RXA4STLAST indicates the boundary of a packet.	Connect from TXA4STLAST of the A4S master, if populated, otherwise tie LOW.

A.10 CXLA interface signals

The following tables describe CMN-600 CXLA interface signals.

The following table contains global signals.

Table A-34 Global signals

Signal	Type	Description	Connection information
CLK_CGL	Input	CML CGL clock input.	Connect to CGL clock for CXLA.
nRESET_CGL	Input	CML CGL reset, active LOW.	Connect to CGL reset for CXLA.
CLK_CXS	Input	CML CXS clock input.	Connect to CXS clock for CXLA.
nRESET_CXS	Input	CML CXS reset, active LOW.	Connect to CXS reset for CXLA.
DFTCLKBYPASS	Input	See *A.12 DFT and MBIST interface signals* on page Appx-A-1183 for more DFT information.	See *A.12 DFT and MBIST interface signals* on page Appx-A-1183 for more DFT information.
DFTCLKDISABLE	Input		
DFTRSTDISABLE	Input		
DFTCGEN	Input		
DFTRAMHOLD	Input		
DFTMCPHOLD	Input		
QACTIVE_CGLCLKCTL	Output (CMN-600)	Indication that the CGL side of the CMN-600 is active and that the External Clock Controller (ExtCC) must not make a request for the CMN-600 and corresponding CXLA to prepare to stop the clock CLK_CGL.	OR with QACTIVE_CGLCLKCTL (CXLA) and connect to external clock controller.
QACTIVE_CGLCLKCTL	Output (CXLA)	Indication that the CGL side of the CXRH is active and that the External Clock Controller (ExtCC) must not make a request for the CMN-600 and corresponding CXLA to prepare to stop the clock CLK_CGL.	OR with QACTIVE_CGLCLKCTL (CMN-600) and connect to external clock controller.
QACTIVE_CXSCLKCTL	Output	Indication that the CXS side of CXLA is active and that the External Clock Controller (ExtCC) must not make a request for the corresponding CXLA to prepare to stop the clock CLK_CXS.	Connect to external clock controller.
QREQn_CXSCLKCTL	Input	Request from the ExtCC for the CXLA to prepare to stop the clock CLK_CXS	Connect to external clock controller or tie HIGH if unused.
QACCEPTn_CXSCLKCTL	Output	Positive acknowledgment after receiving QREQn assertion indicating that the CXLA has completed preparation to stop the clock CLK_CXS and that the ExtCC can stop the clock CLK_CXS.	Connect to external clock controller.
QDENY_CXSCLKCTL	Output	Negative acknowledgment after receiving QREQn assertion indicating that the CXLA has refused the request from the ExtCC to prepare to stop the clock CLK_CXS.	Connect to external clock controller.

Table A-34 Global signals (continued)

Signal	Type	Description	Connection information
PWR_QREQn_CXLA	Input	Indicates a request for a power state transition in CXLA.	Connect to external power management controller or tie HIGH if unused.
PWR_QACCEPTn_CXLA	Output	Indicates acknowledgment of the power state transition and completion of the power state transition within the CXLA.	Connect to external power management controller.
PWR_QDENY_CXLA	Output	Indicates denial of the power state transition.	Connect to external power management controller.
PWR_QACTIVE_CXLA	Output	Hint that indicates activity across the CXLA. When LOW, indicates the possibility of entering the OFF state.	Connect to external power management controller.
PCIE_BUS_NUM	Input	Requester ID of the corresponding PCIe IP.	-

CCIX Gateway Link (CGL) interface (Credited Micro-Architecture interface between RA, HA, and LA components)

The following tables contain *CCIX Gateway Link* (CGL) interface signals.

The following table contains Transmit Memory Request interface signals.

Table A-35 Transmit Memory Request interface signals

Signal	Type	Description	Connection information
TXCGLREQDATFLITPEND	Output	Transmit Memory Request Early Flit Valid hint.	Connect to RXCGLREQDATFLITPEND of the corresponding CXLA.
TXCGLREQDATFLITV	Output	Transmit Memory Request Flit Valid.	Connect to RXCGLREQDATFLITV of the corresponding CXLA.
TXCGLREQDATFLIT[n:0]	Output	Transmit Memory Request Flit.	Connect to RXCGLREQDATFLIT of the corresponding CXLA.
TXCGLREQDATLCRDV	Input	Transmit Memory Request channel link layer credit.	Connect to RXCGLREQDATLCRDV of the corresponding CXLA.

The following table contains Transmit Snoop Request interface signals.

Table A-36 Transmit Snoop Request interface signals

Signal	Type	Description	Connection information
TXCGLSNPFLITPEND	Output	Transmit Snoop Request Early Flit Valid hint.	Connect to RXCGLSNPFLITPEND of the corresponding CXLA.
TXCGLSNPFLITV	Output	Transmit Snoop Request Flit Valid.	Connect to RXCGLSNPFLITV of the corresponding CXLA.
TXCGLSNPFLIT[n:0]	Output	Transmit Snoop Request Flit.	Connect to RXCGLSNPFLIT of the corresponding CXLA.
TXCGLSNPLCRDV	Input	Transmit Snoop Request channel link layer credit.	Connect to RXCGLSNPLCRDV of the corresponding CXLA.

The following table contains Transmit Memory Response interface signals.

Table A-37 Transmit Memory Response interface signals

Signal	Type	Description	Connection information
TXCGLREQRSPFLITPEND	Output	Transmit Memory Response Early Flit Valid hint.	Connect to RXCGLREQRSPFLITPEND of the corresponding CXLA.
TXCGLREQRSPFLITV	Output	Transmit Memory Response Flit Valid.	Connect to RXCGLREQRSPFLITV of the corresponding CXLA.
TXCGLREQRSPFLIT[n:0]	Output	Transmit Memory Response Flit.	Connect to RXCGLREQRSPFLIT of the corresponding CXLA.
TXCGLREQRSPLCRDV	Input	Transmit Memory Response channel link layer credit.	Connect to RXCGLREQRSPLCRDV of the corresponding CXLA.

The following table contains Transmit Snoop Response interface signals.

Table A-38 Transmit Snoop Response interface signals

Signal	Type	Description	Connection information
TXCGLSNPRSPFLITPEND	Output	Transmit Snoop Response Early Flit Valid hint.	Connect to RXCGLSNPRSPFLITPEND of the corresponding CXLA.
TXCGLSNPRSPFLITV	Output	Transmit Snoop Response Flit Valid.	Connect to RXCGLSNPRSPFLITV of the corresponding CXLA.
TXCGLSNPRSPFLIT[n:0]	Output	Transmit Snoop Response Flit.	Connect to RXCGLSNPRSPFLIT of the corresponding CXLA.
TXCGLSNPRSPLCRDV	Input	Transmit Snoop Response channel link layer credit.	Connect to RXCGLSNPRSPLCRDV of the corresponding CXLA.

The following table contains Transmit Snoop Data interface signals.

Table A-39 Transmit Snoop Data interface signals

Signal	Type	Description	Connection information
TXCGLSNPDATFLITPEND	Output	Transmit Snoop Data Early Flit Valid hint.	Connect to RXCGLSNPDATFLITPEND of the corresponding CXLA.
TXCGLSNPDATFLITV	Output	Transmit Snoop Data Flit Valid.	Connect to RXCGLSNPDATFLITV of the corresponding CXLA.
TXCGLSNPDATFLIT[n:0]	Output	Transmit Snoop Data Flit.	Connect to RXCGLSNPDATFLIT of the corresponding CXLA.
TXCGLSNPDATLCRDV	Input	Transmit Snoop Data channel link layer credit.	Connect to RXCGLSNPDATLCRDV of the corresponding CXLA.

The following table contains Transmit Memory Response interface signals.

Table A-40 Transmit Memory Response interface signals

Signal	Type	Description	Connection information
TXCGLRSPDATFLITPEND	Output	Transmit Memory Response Data Early Flit Valid hint.	Connect to RXCGLRSPDATFLITPEND of the corresponding CXLA.
TXCGLRSPDATFLITV	Output	Transmit Memory Response Data Flit Valid.	Connect to RXCGLRSPDATFLITV of the corresponding CXLA.

Table A-40 Transmit Memory Response interface signals (continued)

Signal	Type	Description	Connection information
TXCGLRSPDATFLIT[n:0]	Output	Transmit Memory Response Data Flit.	Connect to RXCGLRSPDATFLIT of the corresponding CXLA.
TXCGLRSPDATLCRDV	Input	Transmit Memory Response Data channel link layer credit.	Connect to RXCGLRSPDATLCRDV of the corresponding CXLA.

The following table contains Transmit Protocol Credit interface signals.

Table A-41 Transmit Protocol Credit interface signals

Signal	Type	Description	Connection information
TXCGLPCRDFLITPEND	Output	Transmit Protocol Credit Early Flit Valid hint.	Connect to RXCGLPCRDFLITPEND of the corresponding CXLA.
TXCGLPCRDFLITV	Output	Transmit Protocol Credit Flit Valid.	Connect to RXCGLPCRDFLITV of the corresponding CXLA.
TXCGLPCRDFLIT[n:0]	Output	Transmit Protocol Credit Flit.	Connect to RXCGLPCRDFLIT of the corresponding CXLA.
TXCGLPCRDLCRDV	Input	Transmit Protocol Credit channel link layer credit.	Connect to RXCGLPCRDLCRDV of the corresponding CXLA.

The following table contains Receive Memory Request interface signals.

Table A-42 Receive Memory Request interface signals

Signal	Type	Description	Connection information
RXCGLREQDATFLITPEND	Input	Receive Memory Request Early Flit Valid hint.	Connect to TXCGLREQDATFLITPEND of the corresponding CXLA.
RXCGLREQDATFLITV	Input	Receive Memory Request Flit Valid.	Connect to TXCGLREQDATFLITV of the corresponding CXLA.
RXCGLREQDATFLIT[n:0]	Input	Receive Memory Request Flit.	Connect to TXCGLREQDATFLIT of the corresponding CXLA.
RXCGLREQDATLCRDV	Output	Receive Memory Request channel link layer credit.	Connect to TXCGLREQDATLCRDV of the corresponding CXLA.

The following table contains Receive Snoop Request interface signals.

Table A-43 Receive Snoop Request interface signals

Signal	Type	Description	Connection information
RXCGLSNPFLITPEND	Input	Receive Snoop Request Early Flit Valid hint.	Connect to TXCGLSNPFLITPEND of the corresponding CXLA.
RXCGLSNPFLITV	Input	Receive Snoop Request Flit Valid.	Connect to TXCGLSNPFLITV of the corresponding CXLA.

Table A-43 Receive Snoop Request interface signals (continued)

Signal	Type	Description	Connection information
RXCGLSNPFLIT[n:0]	Input	Receive Snoop Request Flit.	Connect to TXCGLSNPFLIT of the corresponding CXLA.
RXCGLSNPLCRDV	Output	Receive Snoop Request channel link layer credit.	Connect to TXCGLSNPLCRDV of the corresponding CXLA.

The following table contains Receive Memory Response interface signals.

Table A-44 Receive Memory Response interface signals

Signal	Type	Description	Connection information
RXCGLREQRSPFLITPEND	Input	Receive Memory Response Early Flit Valid hint.	Connect to TXCGLREQRSPFLITPEND of the corresponding CXLA.
RXCGLREQRSPFLITV	Input	Receive Memory Response Flit Valid.	Connect to TXCGLREQRSPFLITV of the corresponding CXLA.
RXCGLREQRSPFLIT[n:0]	Input	Receive Memory Response Flit.	Connect to TXCGLREQRSPFLIT of the corresponding CXLA.
RXCGLREQRSPLCRDV	Output	Receive Memory Response channel link layer credit.	Connect to TXCGLREQRSPLCRDV of the corresponding CXLA.

The following table contains Receive Snoop Response interface signals.

Table A-45 Receive Snoop Response interface signals

Signal	Type	Description	Connection information
RXCGLSNPRSPFLITPEND	Input	Receive Snoop Response Early Flit Valid hint.	Connect to TXCGLSNPRSPFLITPEND of the corresponding CXLA.
RXCGLSNPRSPFLITV	Input	Receive Snoop Response Flit Valid.	Connect to TXCGLSNPRSPFLITV of the corresponding CXLA.
RXCGLSNPRSPFLIT[n:0]	Input	Receive Snoop Response Flit.	Connect to TXCGLSNPRSPFLIT of the corresponding CXLA.
RXCGLSNPRSPLCRDV	Output	Receive Snoop Response channel link layer credit.	Connect to TXCGLSNPRSPLCRDV of the corresponding CXLA.

The following table contains Receive Snoop Data interface signals.

Table A-46 Receive Snoop Data interface signals

Signal	Type	Description	Connection information
RXCGLSNPDATFLITPEND	Input	Receive Snoop Data Early Flit Valid hint.	Connect to TXCGLSNPDATFLITPEND of the corresponding CXLA.
RXCGLSNPDATFLITV	Input	Receive Snoop Data Flit Valid.	Connect to TXCGLSNPDATFLITV of the corresponding CXLA.

Table A-46 Receive Snoop Data interface signals (continued)

Signal	Type	Description	Connection information
RXCGLSNPDATFLIT[n:0]	Input	Receive Snoop Data Flit.	Connect to TXCGLSNPDATFLIT of the corresponding CXLA.
RXCGLSNPDATLCRDV	Output	Receive Snoop Data channel link layer credit.	Connect to TXCGLSNPDATLCRDV of the corresponding CXLA.

The following table contains Receive Memory Response interface signals.

Table A-47 Receive Memory Response interface signals

Signal	Type	Description	Connection information
RXCGLRSPDATFLITPEND	Input	Receive Memory Response Data Early Flit Valid hint.	Connect to TXCGLRSPDATFLITPEND of the corresponding CXLA.
RXCGLRSPDATFLITV	Input	Receive Memory Response Data Flit Valid.	Connect to TXCGLRSPDATFLITV of the corresponding CXLA.
RXCGLRSPDATFLIT[n:0]	Input	Receive Memory Response Data Flit.	Connect to TXCGLRSPDATFLIT of the corresponding CXLA.
RXCGLRSPDATLCRDV	Output	Receive Memory Response Data channel link layer credit.	Connect to TXCGLRSPDATLCRDV of the corresponding CXLA.

The following table contains Receive Protocol Credit interface signals.

Table A-48 Receive Protocol Credit interface signals

Signal	Type	Description	Connection information
RXCGLPCRDFLITPEND	Input	Receive Protocol Credit Early Flit Valid hint.	Connect to TXCGLPCRDFLITPEND of the corresponding CXLA
RXCGLPCRDFLITV	Input	Receive Protocol Credit Flit Valid.	Connect to TXCGLPCRDFLITV of the corresponding CXLA.
RXCGLPCRDFLIT[n:0]	Input	Receive Protocol Credit Flit.	Connect to TXCGLPCRDFLIT of the corresponding CXLA.
RXCGLPCRDLCRDV	Output	Receive Protocol Credit channel link layer credit.	Connect to TXCGLPCRDLCRDV of the corresponding CXLA.

The following table contains Receive and Transmit channel LinkActive interface signals.

Table A-49 Receive and Transmit channel LinkActive interface signals

Signal	Type	Description	Connection information
RXCGLLINKACTIVEREQ	Input	Receive channel LinkActive request from CXLA.	Connect to TXCGLLINKACTIVEREQ of the corresponding CXLA.
RXCGLLINKACTIVEACK	Output	Receive channel LinkActive acknowledgement to CXLA.	Connect to TXCGLLINKACTIVEACK of the corresponding CXLA.

Table A-49 Receive and Transmit channel LinkActive interface signals (continued)

Signal	Type	Description	Connection information
TXCGLLINKACTIVEREQ	Output	Transmit channel LinkActive request to CXLA.	Connect to RXCGLLINKACTIVEREQ of the corresponding CXLA.
TXCGLLINKACTIVEACK	Input	Transmit channel LinkActive acknowledgement from CXLA.	Connect to RXCGLLINKACTIVEACK of the corresponding CXLA.

The following table contains RXCGLSACTIVE and TXCGLSACTIVE interface signals.

Table A-50 RXCGLSACTIVE and TXCGLSACTIVE interface signals

Signal	Type	Description	Connection information
RXCGLSACTIVE	Input	Indication from CXLA that it has one or more outstanding protocol-layer transactions. RXSACTIVE must remain asserted throughout the lifetime of the transaction.	Connect to TXCGLSACTIVE of the corresponding CXLA.
TXCGLSACTIVE	Output	Indication to CXLA that CXRH has one or more outstanding protocol-layer transactions. TXSACTIVE remains asserted throughout the lifetime of the transaction.	Connect to RXCGLSACTIVE of the corresponding CXLA.

The following table contains CXLA configuration interface signals.

Table A-51 CXLA configuration interface signals

Signal	Type	Description	Connection information
TXPUBFLITPEND	Output	Transmit Utility Bus Early Flit Valid hint	Connect to RXPUBFLITPEND of the corresponding CXLA.
TXPUBFLITV	Output	Transmit Utility Bus Flit Valid	Connect to RXPUBFLITV of the corresponding CXLA.
TXPUBFLIT [34:0]	Output	Transmit Utility Bus Flit	Connect to RXPUBFLIT of the corresponding CXLA.
TXPUBLCRDV[1:0]	Input	Transmit Utility Bus channel link layer credit	Connect to RXPUBLCRDV of the corresponding CXLA.
RXPUBFLITPEND	Input	Receive Utility Bus Early Flit Valid hint	Connect to TXPUBFLITPEND of the corresponding CXLA.
RXPUBFLITV	Input	Receive Utility Bus Flit Valid	Connect to TXPUBFLITV of the corresponding CXLA.
RXPUBFLIT [34:0]	Input	Receive Utility Bus Flit	Connect to TXPUBFLIT of the corresponding CXLA.
RXPUBLCRDV[1:0]	Output	Receive Utility Bus channel link layer credit	Connect to TXPUBLCRDV of the corresponding CXLA.
RXPUBLINKACTIVEREQ	Input	Receive channel LinkActive request from CXLA	Connect to TXPUBLINKACTIVEREQ of the corresponding CXLA.
RXPUBLINKACTIVEACK	Output	Receive channel LinkActive acknowledgement to CXLA	Connect to TXPUBLINKACTIVEACK of the corresponding CXLA.
RXPUBLINKFLIT	Input	Receive channel Link Flit valid from CXLA. Indicates that RXPUBFLITV is a link flit	Connect to TXPUBLINKFLIT of the corresponding CXLA.

Table A-51 CXLA configuration interface signals (continued)

Signal	Type	Description	Connection information
TXPUBLINKACTIVEREQ	Output	Transmit channel LinkActive request to CXLA	Connect to RXPUBLINKACTIVEREQ of the corresponding CXLA.
TXPUBLINKACTIVEACK	Input	Transmit channel LinkActive acknowledgement from CXLA	Connect to RXPUBLINKACTIVEACK of the corresponding CXLA.
TXPUBLINKFLIT	Output	Transmit channel Link Flit valid to CXLA. Indicates that TXPUBFLITV is a link flit	Connect to RXPUBLINKFLIT of the corresponding CXLA.

A.11 Debug, trace, and PMU interface signals

Signals that aid debugging are included in CMN-600.

The following table shows the debug, trace, and PMU interface signals.

——— **Note** ———

All signal names in this section are only a root name indicated as **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

CMN-600 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

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Table A-52 Debug, trace, and PMU interface signals

Signal	Type	Description	Connection information
ATCLKEN_NID<x>	Input	ATB clock enable, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATREADY_NID<x>	Input	ATB device ready: 0 = not ready, 1 = ready. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
AFVALID_NID<x>	Input	FIFO flush request, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATDATA[63:0]_NID<x>	Output	ATB data bus, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATVALID_NID<x>	Output	ATB valid data: 0 = no valid data, 1 = valid data. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATBYTES[1:0]_NID<x>	Output	CoreSight ATB device data size: 0b00 = 1 byte, 0b01 = 2 bytes, 0b10 = 3 bytes, 0b11 = 4 bytes. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
AFREADY_NID<x>	Output	FIFO flush acknowledge: 0 = FIFO flush not complete, 1 = FIFO flush complete. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
ATID[6:0]_NID<x>	Output	ATB trace source identification, where <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	-
DBGWATCHTRIGREQ_NID<x>	Output	Trigger output from DEM indicating assertion of a DT event. **DBGWATCHTRIGREQ** is asynchronous-safe, and operates in a four-phase handshake with **DBGWATCHTRIGACK**. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	Connect to external debug and trace control logic.
DBGWATCHTRIGACK_NID<x>	Input	External acknowledgment of receipt of **DBGWATCHTRIGREQ**. **DBGWATCHTRIGACK** must be asynchronous-safe, and operates in a four-phase handshake with **DBGWATCHTRIGREQ**. <x> is the NodeID number for that HN-D/DTC or HN-T/DTC.	Connect to external debug and trace control logic, or tie LOW if **DBGWATCHTRIGREQ** is unused.

Table A-52 Debug, trace, and PMU interface signals (continued)

Signal	Type	Description	Connection information
PMUSNAPSHOTREQ	Input	External request that the live PMU counters are snapshot to the shadow registers.**PMUSNAPSHOTREQ** must be asynchronous-safe, and operates in a four-phase handshake with **PMUSNAPSHOTACK**.	Connect to external debug and trace control logic, or tie LOW if unused.
PMUSNAPSHOTACK	Output	Indication that all live PMU counters have been copied to shadow registers and the contents can be read. **PMUSNAPSHOTACK** is asynchronous-safe, and operates in a four-phase handshake with **PMUSNAPSHOTREQ**.	Connect to external debug and trace control logic.
NIDEN	Input	Global enable for all debug, trace, and PMU functionality. **0** Disabled. **1** Enabled.	Tie or drive as appropriate to meet system security requirements.
SPNIDEN	Input	Global enable for secure debug, trace, and PMU capability. Only applicable when **NIDEN** is enabled. **0** Disabled. **1** Enabled.	
TSVALUEB[63:0]	Input	Global system timestamp value in binary format.	Connect to external system timestamp counter output.

A.12 DFT and MBIST interface signals

Signals that support DFT and MBIST capabilities are included in CMN-600.

The following table shows the DFT signals.

Table A-53 DFT signals

Signal	Type	Description	Connection information
DFTCLKBYPASS	Input	Select the SLC RAM clock to follow the CMN-600 input clock, as applicable for each clock region.	Tie LOW if unused.
DFTCLKDISABLE[3:0]	Input	Disable clock regions during scan shift.	
DFTRAMHOLD	Input	Disable the RAM chip select during scan shift.	
DFTMCPHOLD	Input	Assert to prevent HN-F multicycle RAMs from clocking during capture cycles.	
DFTRSTDISABLE	Input	Disable internal synchronized reset during scan shift.	
DFTCGEN	Input	Scan shift enable. Forces on the clock grids during scan shift.	
DFTSCANMODE	Input	During functional mode, the HN-F SLC and SF RAM set address and write data inputs satisfy RAM hold timing constraints using pipeline behavior. The set address and write data are only clocked and enabled the cycle before the RAMs are accessed, and are held the cycle that the RAM clock asserts. The RAM hold constraints are not guaranteed during ATPG test, because random data is shifted into the flops that control the set address and write data flop enables. This allows the set address and write data to change in the same cycle as a RAM access, violating the RAM hold constraints. This signal addresses the hold constraints during ATPG test. It is used to force the RAM set address and write data flop enables LOW in the cycle that RAM clocks are enabled during ATPG test. The combination of the functional pipeline behavior and this override logic enable holds MCPs to be used on the RAM set address and write data inputs in the implementation flow and during static timing analysis.	

The following table shows the MBIST signals.

Table A-54 MBIST signals

Signal	Type	Description	Connection information
nMBISTRESET	Input	Primary reset to enter MBIST. Must be HIGH during functional non-MBIST operation.	Tie HIGH if unused.
MBISTREQ	Input	SLC MBIST mode request	Tie LOW if unused.

A.13 RN SAM configuration interface signals

Signals that support RN SAM configuration are included in CMN-600.

The following table shows the RN SAM configuration interface signals.

——— **Note** ———

All signal names in this section are only a root name indicated as **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

CMN-600 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

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Table A-55 RN SAM configuration interface signals

Signal	Type	Description	Connection information
RXPUBFLITPEND	Input	Receive channel early flit valid hint	Connect to **TXPUBFLITPEND** of the corresponding CHI device, if populated. Otherwise, tie LOW.
RXPUBFLITV	Input	Receive channel flit valid	Connect to **TXPUBFLITV** of the corresponding CHI device, if populated. Otherwise, tie LOW.
RXPUBFLIT[34:0]	Input	Receive channel flit	Connect to **TXPUBFLIT[n:0]** of the corresponding CHI device, if populated. Otherwise, tie LOW.
RXPUBLINKFLIT	Input	Receive channel link flit	Connect to **TXPUBLINKFLIT** of the corresponding CHI device, if populated. Otherwise, tie LOW.
RXPUBLCRDV_RP1	Output	Receive channel link layer credit	Connect to **TXPUBLCRDV_RP1** of the corresponding CHI device, if populated.
RXPUBLINKACTIVEREQ	Input	Receive channel LinkActive request	Connect to **TXPUBLINKACTIVEREQ** of the corresponding CHI device, if populated. Otherwise, tie LOW.
RXPUBLINKACTIVEACK	Output	Receive channel LinkActive acknowledge	Connect to **TXPUBLINKACTIVEACK** of the corresponding CHI device, if populated.
TXPUBFLITPEND	Output	Transmit channel flit valid	Connect to **RXPUBFLITPEND** of the corresponding CHI device, if populated.
TXPUBFLITV	Output	Transmit channel early flit valid hint	Connect to **RXPUBFLITV** of the corresponding CHI device, if populated.
TXPUBFLIT[34:0]	Output	Transmit channel flit	Connect to **RXPUBFLIT[34:0]** of the corresponding CHI device, if populated.
TXPUBLINKFLIT	Output	Transmit channel link flit	Connect to **RXPUBLINKFLIT** of the corresponding CHI device, if populated.
TXPUBLCRDV_RP1	Input	Transmit channel link layer credit	Connect to **RXPUBLCRDV_RP1** of the corresponding CHI device, if populated, otherwise tie LOW.
TXPUBLINKACTIVEREQ	Output	Transmit channel LinkActive request	Connect to **RXPUBLINKACTIVEREQ** of the corresponding CHI device, if populated.
TXPUBLINKACTIVEACK	Input	Transmit channel LinkActive acknowledge	Connect to **RXPUBLINKACTIVEACK** of the corresponding CHI device, if populated, otherwise tie LOW.
TXPUBCFGACTIVE	Output	Transmit channel Configuration Active	Connect to **RXPUBCFGACTIVE** of the corresponding CHI device, if populated.

A.14 Processor event interface signals

Signals that support processor event interface capabilities are included in CMN-600.

The following table shows the processor event interface signals.

——— **Note** ———

All signal names in this section are only a root name indicated as **RootName**. CMN-600 interfaces use **RootName** within a more fully specified signal name as follows:

CMN-600 interface signal name == **RootName_NID#**, where # represents the node ID corresponding to the specific interface.

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Table A-56 Processor event interface signals

Signal	Type	Description	Connection information
EVENTIREQ	Output	Event input request for processor wake up from WFE state. Remains asserted until EVENTIACK is asserted, and is not reasserted until EVENTIACK is LOW.	Connect to EVENTIREQ input of processor.
EVENTIACK	Input	Event input request acknowledge. Must not be asserted until EVENTIREQ is HIGH, and then must remain asserted until after EVENTIREQ goes LOW.	Connect to EVENTIACK output of processor, or tie to EVENTIREQ output of CMN-600 if unused.
EVENTOREQ	Input	Event output request for processor wake up, triggered by SEV instruction. Must only be asserted when EVENTOACK is LOW, and then must remain HIGH until after EVENTOACK goes HIGH.	Connect to EVENTOREQ output of processor, or tie LOW if unused.
EVENTOACK	Output	Event output request acknowledge. Is not asserted until EVENTOREQ is HIGH, and then remains asserted until after EVENTOREQ goes LOW.	Connect to EVENTOACK input of processor.

The following table shows the CHI Issue A processor event interface signals.

Table A-57 CHI Issue A processor event interface signals

Signal	Type	Description	Connection information
EVENTIREQ	Output	Event input request for processor wake up from WFE state. Remains asserted until EVENTIACK is asserted, and is not reasserted until EVENTIACK is LOW.	Connect to CLREXMON_REQ input of processor.
EVENTIACK	Input	Event input request acknowledge. Must not be asserted until EVENTIREQ is HIGH, and then must remain asserted until after EVENTIREQ goes LOW.	Connect to CLREXMON_ACK output of processor, or tie to EVENTIREQ output of CMN-600 if unused.
EVENTOREQ	Input	Event output request for processor wake up, triggered by SEV instruction. Must only be asserted when EVENTOACK is LOW, and then must remain HIGH until after EVENTOACK goes high.	Refer to first note below, otherwise tie LOW.
EVENTOACK	Output	Event output request acknowledge. Is not asserted until EVENTOREQ is HIGH, and then remains asserted until after EVENTOREQ goes LOW.	Refer to note below.

Note

1. EVENT_OUT from CHI Issue A processor must be handled by the event handling logic external to CMN-600. If system integration wants to connect the EVENT_OUT to CMN-600 EVENTOREQ/ACK, it is the responsibility of the integrator to design the necessary logic to stitch EVENT_OUT which is a multicycle pulse to the four-phase handshake pair taking into account the asynchronous domain crossing.
2. EVENT_IN of CHI Issue A processor may be driven by event handling logic external to CMN-600.

Appendix B
CXS Specification

This appendix describes the Coherent Multichip Link product.

It contains the following sections:

B.1 CCIX interfaces

The CCIX protocol specifies messages that are conveyed between the participating chips. It supports packing one or more messages into a packet.

While CCIX is designed to work over PCIe, the protocol is agnostic to the transport used and other transport mechanism are possible. Examples could include wide direct interfaces over a silicon interposer, optical connections, or encapsulated transport over any number of network technologies.

CML is agnostic to the specific transport used in a system while ensuring that PCIe implementations are efficient and easy to implement by using a lightweight interface designed to efficiently issue CCIX protocol messages to transport logic outside of CMN-600-CML. It is the responsibility of this transport logic to convey the messages to the specified CCIX agents.

CCIX protocol communication consists of a series of messages that are sent between agents in the system. The size of a CCIX message varies from 4 bytes to more than 100 bytes, in 4-byte increments.

Multiple CCIX messages that target the same destination can be assembled into a CCIX packet. For inbound and outbound messages, this packing occurs inside CML. The minimum size for a CCIX packet is 8 bytes, and the maximum is 512 bytes. Smaller maximum sizes are specified by some components.

The CXS interface efficiently passes CCIX packets from one block to another. For a given instance of the interface, all CCIX packet transport occurs in one direction, for example, from block A to block B. In CCIX systems, packets move in both directions by sending messages to and receiving messages from other agents. Because of this packet transport, it is typical for a given pair of blocks to have two instances of this interface, one for each direction, as the following figure shows.

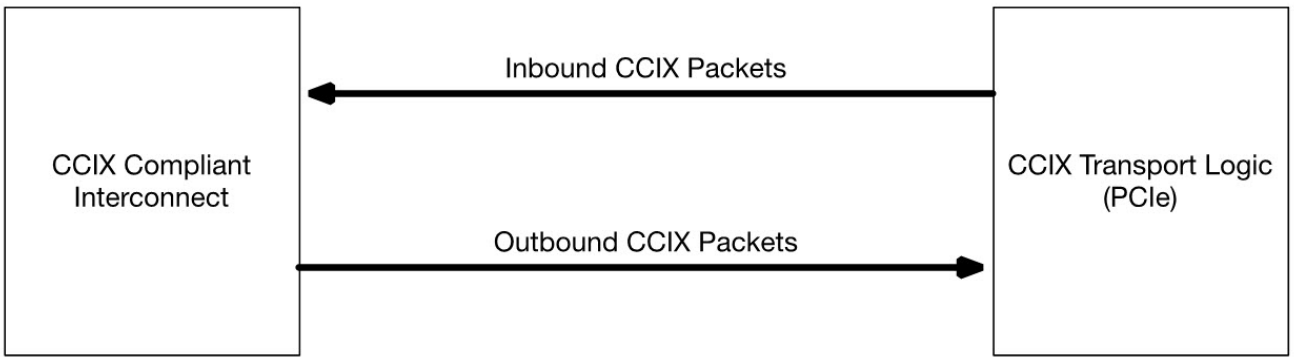

Figure B-1 Basic CXS connectivity

This section contains the following subsections:

- *B.1.1 CXS basic operation* on page Appx-B-1188.
- *B.1.2 CXS interface attributes* on page Appx-B-1189.

B.1.1 CXS basic operation

A single instance of the interface, or one transmitter that is connected to one receiver, sends data in one direction.

If the transmitter has at least one credit from the receiver, and has valid data to send to the receiver, the transmitter:

1. Asserts the **CXSTXVALID** signal.
2. Places the data to be transmitted in **CXSTXDATA**.
3. Sends the required packet control information in **CXSTXCNTL**.
4. Decrements its credit counter by one.

A single cycle of data (data and control) is referred to as a flit.

The receiver does not stall or delay a flit if the transmitter has received a credit. If the receiver is not guaranteed to be ready to accept any flit, no credit is granted to the transmitter.

When the receiver is capable to receive additional flits, it returns credits to the transmitter by asserting **CXSRXCRDGNT**. When the transmitter sees **CXSTXCRDGNT** asserted, it increments its credit counter by one. If it receives a credit during the same cycle that it is returning or using a credit, the counter does not change. The receiver generally has sufficient storage to issue multiple credits to the transmitter. The number of credits that are needed to keep the interface flowing at full bandwidth is dependent on the credit return latency. The credit return latency is the number of cycles in the full loop of **CXSRXCRDGNT**, **CXSTXCRDGNT**, **CXSTXVALID**, **CXSRX VALID**, and **CXSCRDGNT**. If the available storage in the receiver (and therefore the number of credits the receiver can issue) is greater than or equal to the credit return latency, the interface can sustain one flit per cycle.

The following table shows the main signals of the interface.

Table B-1 CXS signal names

Name	Direction	Description
CXSVALID	Sender to receiver	Indicates that valid information is being passed this cycle
CXSDATA	Sender to receiver	The flit data containing the packet bytes being transmitted. Ignore if **CXSVALID** is not asserted.
CXSCNTL	Sender to receiver	Control information for identifying the start and end of packets within the data field. Ignore if **CXSVALID** is not asserted.
CXSCRDGNT	Receiver to sender	Flow control information indicating that the receiver can accept one flit of data
CXSCRDRTN	Sender to receiver	Flow control information indicating that the sender is returning a previously granted credit without using it. Can only be asserted if **CXSVALID** is not asserted.

In a typical connection between an interconnect block and a transport block, each block has two ports: a CXS TX port and a CXS RX port. The TX port of one block is generally connected to the RX port of the other block in pairs as the following figure shows. In this configuration, there are two independent instances of the CXS interface.

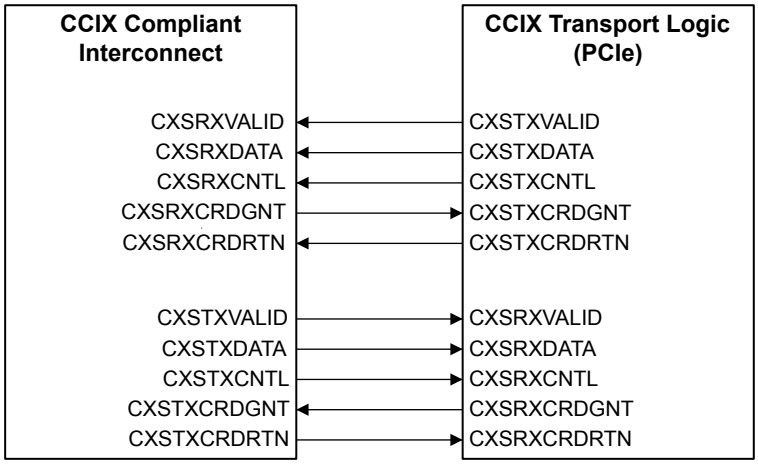

Figure B-2 CXS interface example connection example

B.1.2 CXS interface attributes

The CXS interface has options to meet the needs for CCIX transport in various systems.

These attributes are set independently for the transmitter and the receiver as the following table shows.

Table B-2 Interface attributes

Attribute	Options	Description
CXSDATAFLITWIDTH	256, 512, 1024	Width (in bits) of the **CXSDATA** signal
CXSMAXPKTPERFLIT	2, 3, 4	Maximum number of packets that can be present in a single flit of data
CXSCONTINUOUSDATA	True, False	Receiver (RX): If set to True, this receiver requires that after a packet is started, it is completed in consecutive cycles if enough credits are available. Transmitter (TX): If set to True, this transmitter does not begin a packet until it can deliver the complete packet in consecutive cycles as long as credits are available.
CXSERRORFULLPKT	True, False	RX: If set to True, this receiver requires that the length of every packet (including packets ending with EndError) match the packet length specified in the packet header. TX: If set to True, if this transmitter is unable to complete a packet and must end the packet with an EndError indication, the transmitter sends the number of bytes specified in the packet header before ending the packet. NOTE: The encoding of the packet length within the packet is outside of the scope of the CXS document. For use of this interface for CCIX packet transmission, see the CCIX specification for packet length encoding.
CXSDATACHECK	None, Parity, *Single Error Correct, Double Error Detect* (SECDED)	Datacheck support on **CXSDATA**, **CXSCNTL**. Parity: Odd parity • 1 bit per byte on **CXSDATA**. • 1 bit for **CXSCNTL**. SECDED: ECC on a 64-bit granularity • 8 bits per 64 bits of data. • 8 bits for **CXSCNTL** (zero extended to 64 bits). NOTE: 1. The SECDED ECC algorithm is not yet specified. 2. **CXSDATA** and **CXSCNTL** is the same level of Datacheck support.
CXSREPLICATION	None, Duplicate, Triplicate	Signal replication on **CXSVALID**, **CXSCRDGNT**, **CXSCRDRTN**. Duplicate: **CXSVALIDCHK**, **CXSCRDGNTCHK**, and **CXSCRDRTNCHK** are each single bit signals duplicating the value of the corresponding control signal. Triplicate: **CXSVALIDCHK**, **CXSCRDGNTCHK**, and **CXSCRDRTNCHK** are each two-bit signals with each of the two bits having the same value as the corresponding control signal.

When assembling a system, the attributes of the connected CXS TX and CXS RX interfaces must be compatible. The following table shows the compatibility requirements for each of the defined attributes.

Table B-3 CXS attribute compatibility

Attribute	Compatibility requirement
CXSDATAFLITWIDTH	TX and RX must match
CXSMAXPKTPERFLIT	TX must be less than or equal to RX

Table B-3 CXS attribute compatibility (continued)

Attribute	Compatibility requirement
CXSCONTINUOUSDATA	If RX **CXSCONTINUOUSDATA** = True, then TX **CXSCONTINUOUSDATA** must be True
CXSERRORFULLDATA	If RX **CXSERRORFULDATA** = True, then TX **CXSERRORFULLDATA** must be True
CXSDATACHECK	If RX **CXSDATACHECK** = None: • TX **CXSDATACHECK** can be any value. • Associated TX signals can be disconnected. If RX **CXSDATACHECK** = Parity or SECDED: • TX **CXSDATACHECK** must have the same value.
CXSREPLICATION	If RX **CXSREPLICATION** = None: • TX **CXSREPLICATION** can be any value. • Associated TX signals can be left disconnected. If RX **CXSREPLICATION** = Duplicate or Triplicate: • TX **CXSREPLICATION** must have the same value.

B.2 Signal descriptions

The CMN-600 product includes transmit, receive, and width signals for the CXS and CHI interfaces.

CXS interface

The following table contains the transmit signals.

Table B-4 TX signals

Signal	Type	Description	Connection information
CXSTXDATA	Output	Transmit channel data flit.	Connect to CXSRXDATA of the corresponding PCIe IP.
CXSTXCNTL	Output	Transmit channel control information.	Connect to CXSRXCNTL of the corresponding PCIe IP.
CXSTXVALID	Output	Transmit channel data flit valid.	Connect to CXSRXVALID of the corresponding PCIe IP.
CXSTXCRDGNT	Input	Transmit channel link layer credit grant.	Connect to CXSRXCRDGNT of the corresponding PCIe IP.
CXSTXCRDRTN	Output	Transmit channel link layer credit return.	Connect to CXSRXCRDRTN of the corresponding PCIe IP.
CXSTXDATACHK	Output	Transmit channel Parity or ECC for DATA field.	Connect to CXSRXDATACHK of the corresponding PCIe IP.
CXSTXCNTLCHK	Output	Transmit channel Parity or ECC for CNTL field.	Connect to CXSRXCNTLCHK of the corresponding PCIe IP.
CXSTXVALIDCHK	Output	Transmit channel Duplication or Triplication for VALID bit.	Connect to CXSRXVALIDCHK of the corresponding PCIe IP.
CXSTXCRDGNTCHK	Input	Transmit channel Duplication or Triplication for CRDGNT bit.	Connect to CXSRXCRDGNTCHK of the corresponding PCIe IP.
CXSTXCRDRTNCHK	Output	Transmit channel Duplication or Triplication for CRDRTN bit.	Connect to CXSRXCRDRTNCHK of the corresponding PCIe IP.
CXSTXACTIVEREQ	Output	Transmit channel link activation/ deactivation request.	Connect to CXSRXACTIVEREQ of the corresponding PCIe IP.
CXSTXACTIVEACK	Input	Transmit channel link activation/ deactivation acknowledge.	Connect to CXSRXACTIVEACK of the corresponding PCIe IP.
CXSTXDEACTHINT	Input	Transmit channel hint for link deactivation.	Connect to CXSRXDEACTHINT of the corresponding PCIe IP.

The following table contains the receive signals.

Table B-5 RX signals

Signal	I/O	Description	Connection information
CXSRXDATA	Input	Receive channel data flit.	Connect to CXSTXDATA of the corresponding PCIe IP.
CXSRXCNTL	Input	Receive channel control information.	Connect to CXSTXCNTL of the corresponding PCIe IP.
CXSRXVALID	Input	Receive channel data flit valid.	Connect to CXSTXVALID of the corresponding PCIe IP.
CXSRXCRDGNT	Output	Receive channel link layer credit grant.	Connect to CXSTXCRDGNT of the corresponding PCIe IP.

Table B-5 RX signals (continued)

Signal	I/O	Description	Connection information
CXSRXCRDRTN	Input	Receive channel link layer credit return.	Connect to CXSTXCRDRTN of the corresponding PCIe IP.
CXSRXDATACHK	Input	Receive channel Parity or ECC for DATA field.	Connect to CXSTXDATACHK of the corresponding PCIe IP.
CXSRXCNTLCHK	Input	Receive channel Parity or ECC for CNTL field.	Connect to CXSTXCNTLCHK of the corresponding PCIe IP.
CXSRXVALIDCHK	Input	Receive channel Duplication or Triplication for VALID bit.	Connect to CXSTXVALIDCHK of the corresponding PCIe IP.
CXSRXCRDGNTCHK	Output	Receive channel Duplication or Triplication for CRDGNT bit.	Connect to CXSTXCRDGNTCHK of the corresponding PCIe IP.
CXSRXCRDRTNCHK	Input	Receive channel Duplication or Triplication for CRDRTN bit.	Connect to CXSTXCRDRTNCHK of the corresponding PCIe IP.
CXSRXACTIVEREQ	Input	Receive channel link activation/ deactivation request.	Connect to CXSTXACTIVEREQ of the corresponding PCIe IP.
CXSRXACTIVEACK	Output	Receive channel link activation/ deactivation acknowledge.	Connect to CXSTXACTIVEACK of the corresponding PCIe IP.
CXSRXDEACTHINT	Output	Receive channel hint for link deactivation.	Connect to CXSTXDEACTHINT of the corresponding PCIe IP.

The following table contains the width signals.

Table B-6 Signal widths

Signal	Width
CXS[TX/RX]DATA	CXSDATAFLITWIDTH (256, 512, 1024 bits)
CXS[TX/RX]CNTL	See the Control Field Widths and Placement portion of this manual for more information.
CXS[TX/RX]VALID	1 bit
CXS[TX/RX]CRDGNT	1 bit
CXS[TX/RX]CRDRTN	1 bit
CXS[TX/RX]DATACHK	CXSDATACHECK = 'Parity': CXSDATAFLITWIDTH/8 bits CXSDATACHECK = 'SECDED': (CXSDATAFLITWIDTH/64) * 8 bits
CXS[TX/RX]CNTLCHK	CXSDATACHECK = 'Parity': 1 bit CXSATACHECK = 'SECDED': 8 bits
CXS[TX/RX]VALIDCHK	CXSREPLICATION = 'Duplicate': 1 bit CXSREPLICATION = 'Triplicate': 2 bit
CXS[TX/RX]CRDGNTCHK	CXSREPLICATION = 'Duplicate': 1 bit CXSREPLICATION = 'Triplicate': 2 bit

Table B-6 Signal widths (continued)

Signal	Width
CXS[TX/RX]CRDRTNCHK	CXSREPLICATION = 'Duplicate': 1 bit CXSREPLICATION = 'Triplicate': 2 bit
CXS[TX/RX]ACTIVEREQ	1 bit
CXS[TX/RX]ACTIVEACK	1 bit
CXS[TX/RX]DEACTHINT	1 bit

B.3 Packet control fields

The **CXSCNTL** signal contains five fields.

The widths of each field, and therefore the bit position of each field, within **CXSCNTL** vary with the attributes of the interface as the following table shows.

Table B-7 Packet control fields

Field	Description
START	Each bit in START indicates a packet is starting in this flit. START[0] = 1: At least one packet is starting in this flit. START[1] = 1: At least two packets are starting in this flit. … The number of bits in START is the number of packets that can be present in a flit of data (**CXSMAXPKTPERFLIT**). If any bit in START is 1, all lower bits of START must be 1.
START[N:0]PTR	This field is an array of pointers to the starting location of packets in this flit. • There is one pointer for each START bit, valid only if that START bit is set. • If the corresponding START bit is 0, the pointer can have any value and should be ignored. • All packet starts are 16-byte aligned. • The width of each pointer is $\log_2$(**CXSDATAFLITWIDTH**/128) bits. • The first byte of the Xth starting packet is (START[X]PTR << 4).
END	Each bit in END indicates a packet is ending in this flit. END[0] = 1: At least one packet is ending in this flit. END[1] = 1: At least two packets are ending in this flit. … The number of bits in END is the number of packets that can be present in a flit of data (**CXSMAXPKTPERFLIT**). If any bit of END is 1, all lower bits of END must be 1.
ENDERROR	Each bit in ENDERROR indicates that a packet is ending with an error condition this flit. ENDERROR[0] = 1: The first packet ending this cycle has an error. ENDERROR[1] = 1: The second packet ending this cycle has an error. … The number of bits in ENDERROR is the number of bits in END. If ENDERROR[N] is asserted, END[N] must be asserted.
END[N:0]PTR	This field is an array of pointers to the last four bytes of packets ending in this flit. • There is one pointer for each END bit, valid only if that END bit is set. • If the corresponding END bit is 0, the pointer can have any value and should be ignored. • All packet ends are four-byte aligned. • The width of each pointer is $\log_2$(**CXSDATAFLITWIDTH**/32) bits. • Each end pointer points to the first byte of the last aligned four bytes of the packet. — The last byte of the Xth ending packet is therefore [(END[X]PTR << 2) + 3].

The following table shows packet control field widths and placement information.

Table B-8 Packet control field widths and placement

CXSMAXPKTPERFLIT	CXSDATAFLITWIDTH	Width of CXSCNTL	Bit positions in field	Bit positions in CXSCNTL
2	256	14	START[1:0]	CXSCNTL[1:0]
			START0PTR[0]	CXSCNTL[2]
			START1PTR[0]	CXSCNTL[3]
			END[1:0]	CXSCNTL[5:4]
			ENDERROR[1:0]	CXSCNTL[7:6]
			END0PTR[2:0]	CXSCNTL[10:8]
			END1PTR[2:0]	CXSCNTL[13:11]
2	512	18	START[1:0]	CXSCNTL[1:0]
			START0PTR[1:0]	CXSCNTL[3:2]
			START1PTR[1:0]	CXSCNTL[5:4]
			END[1:0]	CXSCNTL[7:6]
			ENDERROR[1:0]	CXSCNTL[9:8]
			END0PTR[3:0]	CXSCNTL[13:10]
			END1PTR[3:0]	CXSCNTL[17:14]
2	1024	22	START[1:0]	CXSCNTL[1:0]
			START0PTR[2:0]	CXSCNTL[4:2]
			START1PTR[2:0]	CXSCNTL[7:5]
			END[1:0]	CXSCNTL[9:8]
			ENDERROR[1:0]	CXSCNTL[11:10]
			END0PTR[4:0]	CXSCNTL[16:12]
			END1PTR[4:0]	CXSCNTL[21:17]
3	256	-	(Not legal: 256 bit interface has maximum of 2 packets)	
3	512	27	START[2:0]	CXSCNTL[2:0]
			START0PTR[1:0]	CXSCNTL[4:3]
			START1PTR[1:0]	CXSCNTL[6:5]
			START2PTR[1:0]	CXSCNTL[8:7]
			END[2:0]	CXSCNTL[11:9]
			ENDERROR[2:0]	CXSCNTL[14:12]
			END0PTR[3:0]	CXSCNTL[18:15]
			END1PTR[3:0]	CXSCNTL[22:19]
			END2PTR[3:0]	CXSCNTL[26:23]

Table B-8 Packet control field widths and placement (continued)

CXSMAXPKTPERFLIT	CXSDATAFLITWIDTH	Width of CXSCNTL	Bit positions in field	Bit positions in CXSCNTL
3	1024	33	START[2:0]	CXSCNTL[2:0]
			START0PTR[2:0]	CXSCNTL[5:3]
			START1PTR[2:0]	CXSCNTL[8:6]
			START2PTR[2:0]	CXSCNTL[11:9]
			END[2:0]	CXSCNTL[14:12]
			ENDERROR[2:0]	CXSCNTL[17:15]
			END0PTR[4:0]	CXSCNTL[22:18]
			END1PTR[4:0]	CXSCNTL[27:23]
			END2PTR[4:0]	CXSCNTL[32:28]
4	256	-	(Not legal: 256 bit interface has maximum of 2 packets)	
4	512	36	START[3:0]	CXSCNTL[3:0]
			START0PTR[1:0]	CXSCNTL[5:4]
			START1PTR[1:0]	CXSCNTL[7:6]
			START2PTR[1:0]	CXSCNTL[9:8]
			START3PTR[1:0]	CXSCNTL[11:10]
			END[3:0]	CXSCNTL[15:12]
			ENDERROR[3:0]	CXSCNTL[19:16]
			END0PTR[3:0]	CXSCNTL[23:20]
			END1PTR[3:0]	CXSCNTL[27:24]
			END2PTR[3:0]	CXSCNTL[31:28]
			END3PTR[3:0]	CXSCNTL[35:32]
4	1024	44	START[3:0]	CXSCNTL[3:0]
			START0PTR[2:0]	CXSCNTL[6:4]
			START1PTR[2:0]	CXSCNTL[9:7]
			START2PTR[2:0]	CXSCNTL[12:10]
			START3PTR[2:0]	CXSCNTL[15:13]
			END[3:0]	CXSCNTL[19:16]
			ENDERROR[3:0]	CXSCNTL[23:20]
			END0PTR[4:0]	CXSCNTL[28:24]
			END1PTR[4:0]	CXSCNTL[33:29]
			END2PTR[4:0]	CXSCNTL[38:34]
			END3PTR[4:0]	CXSCNTL[43:39]

B.4 Packet size constraints

The CXS interface transmits a very specific payload.

The CXS interface transmits packets of data that meet the following requirements:

- At least 4 bytes in size
- A multiple of 4 bytes in size
- No limit on packet size.

The CCIX places further constraints on packet size:

- At least 8 bytes in size.
- No more than 512 bytes in size.

When used for CCIX packet transfer, CXS packets must meet these constraints.

B.5 Packet position constraints

The CXS interface transmits a very specific payload.

To simplify datapath implementation, CXS places restrictions on the placement of packets within each flit of data.

- The first byte of a packet must be placed on an aligned 16-byte boundary (byte 0, 16, 32, 48, 64, 80, 96, or 112).
- Subsequent bytes of the packet occupy subsequent bytes of the flit.
- Packets can end on any four-byte aligned boundary.
- Once a packet has been started at a byte position in the current flit, that packet occupies every subsequent byte in that flit until the packet ends or the flit ends.
- If there are remaining bytes in the packet when the flit ends, that packet starts at byte 0 of the next flit and occupies every subsequent byte position until the packet ends or the flit ends.
- When a packet ends within a flit, the remaining bytes in the flit may be unused. These unused bytes are not part of any packet.
- Any packet in a flit must begin at the first available 16-byte boundary relative to the start of the flit or the ending of a previous packet.

CXSMAXPKTPERFLIT specifies the maximum number of packets that can have bytes in the current flit. There can be up to **CXSMAXPKTPERFLIT** new packets starting in a flit, and up to **CXSMAXPKTPERFLIT** packets ending in a flit.

If a packet started on a previous flit and is continuing on the current flit, that continuing packet counts towards the packet limit. That packet could therefore only have one less than **CXSMAXPKTPERFLIT** new packets starting.

B.6 CCIX Packet Details

This section contains CCIX packet details.

CMN supports:

- Both PCIe and optimized header formats.
- Both single message per packet, No Message Packing, and multiple messages per packet: Message packing.
- Maximum TLP size of 512B which is the maximum permitted by CCIX specification.

All of these CMN supported properties are found in the por_cxla_ccix_prop_capabilities register.

Based on the system requirements/support, these properties can be programmed in configuration register por_cxla_ccix_prop_configured during system discovery. CMN generates a TLP-based on the configured properties in por_cxla_ccix_prop_configured register.

B.7 Packet examples

These following examples illustrate packet placement rules as well as the CXSCNTL field usage.

Examples in the following two tables both have CXSCONTINUOUSDATA = TRUE and CXSDATACHECK = None. Each data packet in the figures is shaded and has a unique identifier. Unused packet slots have dashes instead of identifiers.

The following table shows an example with 256-bit data, CXSDATAFLITWIDTH = 256. It has up to two packets per flit, CXSMAXPKTPERFLIT = 2.

		Cycle											
Signal	**Field**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
CXSVALID		0	1	1	0	1	1	1	1	1	1	1	1
CXSDATA[31:0]		-	TLPA	TLPB	-	TLPD	TLPD	TLPE	TLPE	TLPF	TLPH	TLPI	TLPK
CXSDATA[63:32]		-	TLPA	TLPB	-	TLPD	-	TLPE	TLPE	-	TLPH	TLPI	TLPK
CXSDATA[95:64]		-	TLPA	TLPB	-	TLPD	-	TLPE	TLPE	-	TLPH	TLPI	TLPK
CXSDATA[127:96]		-	TLPA	-	-	TLPD	-	TLPE	TLPE	-	TLPH	TLPI	TLPK
CXSDATA[159:128]		-	TLPA	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPG	TLPI	TLPJ	TLPL
CXSDATA[191:160]		-	TLPA	TLPC	-	TLPD	TLPE	TLPE	-	TLPG	TLPI	TLPJ	TLPL
CXSDATA[223:192]		-	TLPA	TLPC	-	TLPD	TLPE	TLPE	-	TLPG	TLPI	TLPJ	TLPL
CXSDATA[255:224]		-	-	TLPC	-	TLPD	TLPE	TLPE	-	TLPG	TLPI	TLPJ	TLPL
CXSCNTL[1:0]	START[1:0]	-	0x1	0x3	-	0x1	0x1	0x0	-	0x3	0x3	0x1	0x3
CXSCNTL[2]	START0PTR[0]	-	0x0	0x0	-	0x0	0x1	-	-	0x0	0x0	0x0	0x0
CXSCNTL[3]	START1PTR[0]	-	-	0x1	-	-	-	-	-	0x1	0x1	-	0x1
CXSCNTL[5:4]	END[1:0]	-	0x1	0x3	-	0x0	0x1	0x0	0x1	0x3	0x1	0x3	0x3
CXSCNTL[7:6]	ENDERROR[1:0]	-	0x0	0x0	-	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
CXSCNTL[10:8]	END0PTR[2:0]	-	0x6	0x2	-	-	0x0	-	0x4	0x0	0x3	0x3	0x3
CXSCNTL[13:11]	END1PTR[2:0]	-	-	0x7	-	-	-	-	-	0x7	-	0x7	0x7

Figure B-3 Example 256-bit wide interface with maximum of two packets per flit.

The following table shows an example with 512-bit data, CXSDATAFLITWIDTH = 512. It has up to four packets per flit, CXSMAXPKTPERFLIT = 4.

		Cycle											
Signal	**Field**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
CXSVALID		0	1	1	0	1	1	1	1	1	1	1	0
CXSDATA[31:0]		-	TLPA	TLPB	-	TLPD	TLPD	TLPE	TLPE	TLPF	TLPI	TLPM	-
CXSDATA[63:32]		-	TLPA	TLPB	-	TLPD	-	TLPE	TLPE	-	TLPI	TLPM	-
CXSDATA[95:64]		-	TLPA	TLPB	-	TLPD	-	TLPE	TLPE	-	TLPI	TLPM	-
CXSDATA[127:96]		-	TLPA	TLPB	-	TLPD	-	TLPE	TLPE	-	TLPI	TLPM	-
CXSDATA[159128]		-	TLPA	TLPB	-	TLPD	TLPE	TLPE	TLPE	TLPG	TLPJ	TLPN	-
CXSDATA[191:160]		-	TLPA	TLPB	-	TLPD	TLPE	TLPE	TLPE	TLPG	TLPJ	TLPN	-
CXSDATA[223:192]		-	TLPA	-	-	TLPD	TLPE	TLPE	TLPE	TLPG	TLPJ	TLPN	-
CXSDATA[255:224]		-	TLPA	-	-	TLPD	TLPE	TLPE	TLPE	TLPG	TLPJ	TLPN	-
CXSDATA[287:256]		-	TLPA	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPH	TLPK	TLPO	-
CXSDATA[319:288]		-	-	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPH	TLPK	TLPO	-
CXSDATA[351:320]		-	-	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPH	TLPK	TLPO	-
CXSDATA[383:352]		-	-	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPH	TLPK	TLPO	-
CXSDATA[415:384]		-	-	TLPC	-	TLPD	TLPE	TLPE	TLPE	TLPI	TLPL	TLPP	-
CXSDATA[447:416]		-	-	TLPC	-	TLPD	TLPE	TLPE	-	TLPI	TLPL	TLPP	-
CXSDATA[479:448]		-	-	TLPC	-	TLPD	TLPE	TLPE	-	TLPI	TLPL	TLPP	-
CXSDATA[511:480]		-	-	TLPC	-	TLPD	TLPE	TLPE	-	TLPI	TLPL	TLPP	-
CXSCNTL[3:0]	START[3:0]	-	0x1	0x3	-	0x1	0x1	0x0	0x0	0xF	0x7	0xF	-
CXSCNTL[5:4]	START0PTR[1:0]	-	0x0	0x0	-	0x0	0x1	-	-	0x0	0x1	0x0	-
CXSCNTL[7:6]	START1PTR[1:0]	-	-	0x2	-	-	-	-	-	0x1	0x2	0x1	-
CXSCNTL[8:9]	START2PTR[1:0]	-	-	-	-	-	-	-	-	0x2	0x3	0x2	-
CXSCNTL[11:10]	START3PTR[1:0]	-	-	-	-	-	-	-	-	0x3	-	0x3	-
CXSCNTL[15:12]	END[3:0]	-	0x1	0x3	-	0x0	0x1	0x0	0x1	0x7	0xF	0xF	-
CXSCNTL[19:16]	ENDERROR[3:0]	-	0x0	0x0	-	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
CXSCNTL[23:20]	END0PTR[3:0]	-	0x8	0x5	-	-	0x0	-	0xC	0x0	0x3	0x3	-
CXSCNTL[27:24]	END1PTR[3:0]	-	-	0xF	-	-	-	-	-	0x7	0x7	0x7	-
CXSCNTL[31:28]	END2PTR[3:0]	-	-	-	-	-	-	-	-	0xB	0xB	0xB	-
CXSCNTL[35:32]	END3PTR[3:0]	-	-	-	-	-	-	-	-	0xF	0xF	0xF	-

Figure B-4 Packet examples 512 bit four packets per flit

B.8 CXS flow control

Flow control on the CXS interface is implemented through a credit exchange mechanism.

When the CXS interface is reset or activated, the transmitter has no credits. Therefore, the transmitter can send no data across the interface. The receiver grants credits to the transmitter by asserting the **CXSRXCRDGNT** signal. A credit allows the transmitter to send a single flit across the interface. Each cycle in which **CXSRXCRDGNT** is asserted grants a single credit to the transmitter. Each cycle in which **CXSTXVALID** is asserted sends one valid flit of data and implicitly returns one credit to the receiver. In cycles where **CXSTXVALID** is not asserted, the transmitter can explicitly return one credit by asserting **CXSTXCRDRTN**. The **CXSTXCRDRTN** mechanism is typically used to return credits before deactivating the link.

The maximum number of credits that a receiver grants a transmitter is implementation-defined, with a limit of 15 credits. The transmitter must be able to track up to 15 credits at a time. The receiver must guarantee that it can receive one flit of data for each credit that it grants.

A transmitter cannot use a credit to send a flit until the cycle after the **CXSTXCRDGNT** signal is asserted. This means there must be at least one flop between **CXSTXCRDGNT** and the **CXSTXVALID** signal. A pure combinational path between **CXSTXCRDGNT** and **CXSTXVALID** is not allowed.

The following figure shows a basic credit exchange as seen on the transmitter's pins. The receiver sends a single credit and gets a single flit in return. The receiver then sends four credits and receives four flits.

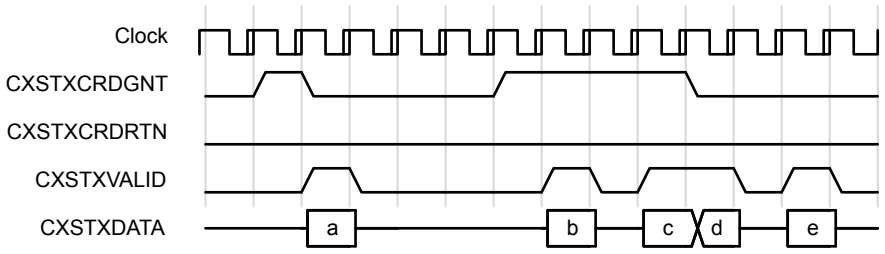

Figure B-5 Basic credit mechanism

The following figure shows a steady state credit exchange example. In this example system, the credit loop is three cycles:

1. The steady state delay between sending a valid flit.
2. Receiving back the credit that flit consumes.
3. Sending another flit targeting the same buffer resource.

In this case:

1. Flit A is transmitted.
2. The credit is returned two cycles later.
3. Flit D is sent one cycle later using the returned credit.

Because this is a three-cycle loop, the receiver on this interface must have storage to grant at least three credits in order to keep the interface flowing at full bandwidth.

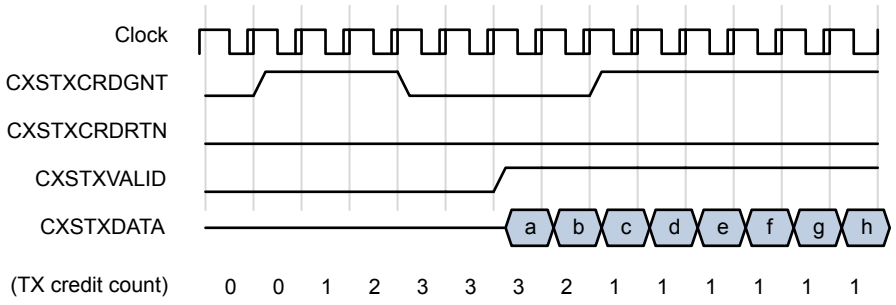

Figure B-6 Steady state credit example

In the same system, if the receiver only had two buffers available, the performance would be lower, as the following figure shows.

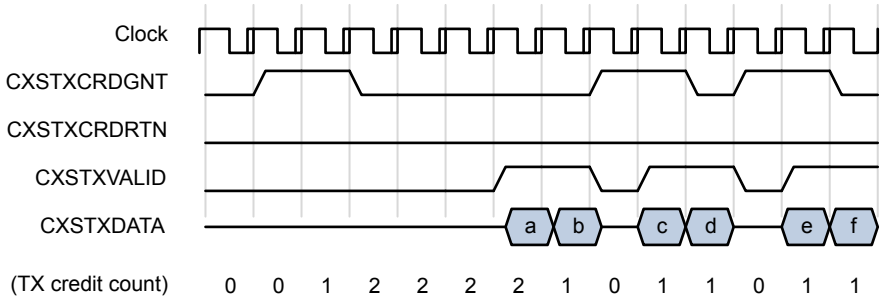

Figure B-7 Too few credits example

B.9 CXS interface activation and deactivation

A mechanism is provided for a CXS interface to move between a full running operational state and a low power state.

When moving between operational states, including when exiting from reset, it is important that the exchange of credits is carefully controlled to avoid the loss of flits or credits.

On exit from reset, or when moving to a full running operational state, the interface starts in an idle state and the transfer of flits can only commence when credits have been exchanged. Credits can only be exchanged when the sender of the credits knows the receiver is ready to receive them.

A two-signal, four-phase handshake mechanism is used. This mechanism synchronizes the state of the link between the transmitter and receiver, initiated by the transmitter. In addition, a deactivation request hint is available for the receiver to request that the link be brought down.

In a typical connection with two CXS interfaces (one outbound, one inbound), there are two independent instances of the handshake mechanism.

This section contains the following subsections:

B.9.1 Request and acknowledge handshaking

Request and acknowledge handshaking uses **CXSACTIVEREQ** and **CXSACTIVEACK** as primary signals.

The following figure shows the relationship between the payload, credit, **CXSACTIVEREQ**, and **CXSACTIVEACK** signals.

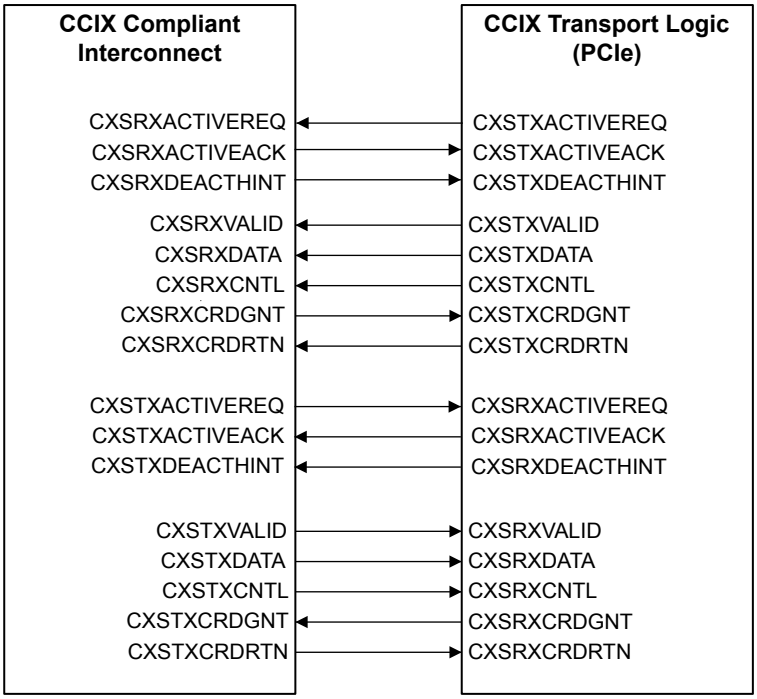

Figure B-8 CXS link activation

The transmitter, which sends the payload flits, requires a credit before it can send a flit. The receiver passes a credit when it has the resources available to accept a flit.

- On exit from reset, all credits are held by the receiver and at least one must be passed to the transmitter before flit transfer can begin.
- During normal operation, there is an ongoing exchange of flits and credits between the two sides of the interface.
- Before entering a low-power state, the sending of payload flits must be stopped and all credits must be returned to the receiver. These requirements effectively return the interface to the same state as immediately after reset.

Four states are defined for the interface operation:

RUN
There is an ongoing exchange of flits and credits between the two components.

STOP
The interface is in a low-power state and is not operational. All credits are held by the receiver and the transmitter is not permitted to send any flits.

ACTIVATE
This state is used when moving from the STOP state to the RUN state.

DEACTIVATE
This state is used when moving from the RUN state to the STOP state.

RUN and STOP are stable states. When one of these states is entered, a channel can remain in this state indefinitely.

DEACTIVATE and ACTIVATE are transient states. It is expected that when one of these states is entered, a channel moves to the next stable state relatively quickly.

——— **Note** ———

The specification does not define a maximum period of time in a transient state, but it is expected that it is deterministic for any given implementation.

———————————

The **CXSACTIVEREQ** and **CXSACTIVEACK** signals determine the state. The following figure shows the relationship between the four states.

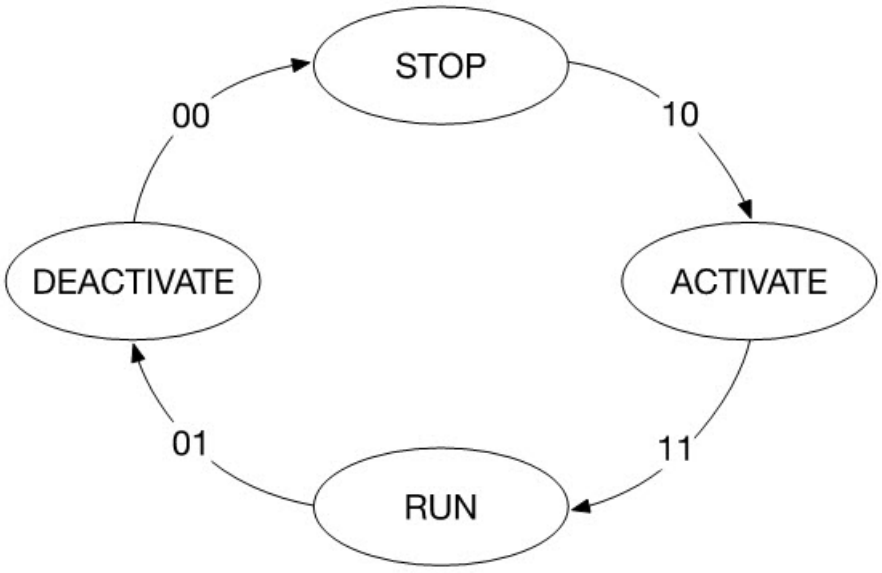

Figure B-9 Request and acknowledge handshake states

The following table provides the mapping of the states to the **CXSACTIVEREQ** and **CXSACTIVEACK** signals.

Table B-9 Mapping of states to the ACTIVE signals

State	CXSACTIVEREQ	CXSACTIVEACK
STOP	0	0
ACTIVATE	1	0
RUN	1	1
DEACTIVATE	0	1

The following table describes the transmitter's and receiver's behavior within a single link for each state.

Table B-10 Behavior for request and acknowledge states

State	Transmitter	Receiver
STOP	Has no credits. Must not send any flits or credit returns. Is guaranteed not to receive any credits. Must assert **CXSTXACTIVEREQ** to move to the ACTIVATE state if it has flits to send.	Is guaranteed not to receive any flits or credit returns. Must not send any credits.
ACTIVATE	Must not send any flits. Must be prepared to receive credits in this state, although it must not use them until in RUN state. Remains in the ACTIVATE state while waiting for the receiver to acknowledge the move to RUN state. NOTE: The transmitter only receives credits in the ACTIVATE state when there is a race between the receiver sending credits and asserting **CXSACTIVEACK** to move to the RUN state.	Is guaranteed not to receive any flits. Must not send any credits. The ACTIVATE state is a transient state and the receiver controls the move to the RUN state by asserting **CXSACTIVEACK**. Must assert **CXSACTIVEACK** and move to the RUN state before sending credits. Is permitted to assert **CXSACTIVEACK** and send a credit in the same cycle. NOTE: It may appear that a receiver has sent credits in the ACTIVATE state if there is a race between the receiver sending credits and asserting **CXSACTIVEACK** to move to the RUN state.
RUN	Can receive credits. Can send flits when it has credits available. Deasserts **CXSTXACTIVEREQ** to exit from this state if it wants to move to a low-power state.	Can receive flits corresponding to the credits it has sent. Sends credits when it has resources available to accept further flits. Must remain in the RUN state until it observes the deassertion of **CXSRXACTIVEREQ**.
DEACTIVATE	Must return credits using flits or **CXSTXCRDRTN**. It is recommended that the transmitter enters the DEACTIVATE state only when it has no more flits to send. Therefore, it is expected that the transmitter returns credits using only **CXSTXCRDRTN**. Must be prepared to continue receiving credits. For each additional credit received, it must return the credit by sending a valid flit or asserting **CXSTXCRDRTN**. Remains in the DEACTIVATE state while waiting for the receiver to acknowledge the move to the STOP state. At this point, it is guaranteed to receive no more credits.	Stops sending credits and collects all returned credits. Must be prepared to receive flits in this state. This is not expected, but can occur. Is permitted to send credits when first entering this state. However, it must have stopped sending credits and had all credits returned before exiting this state. Receives flits or explicit credit returns until all credits are returned. Must wait for all credits to be returned before deasserting **CXSACTIVEACK** and entering STOP state.

The following table describes the behavior for each request and acknowledge state.

Table B-11 Request and acknowledge states summary

State	Transmitter	Receiver
STOP	Must not send flits. Will not receive credits.	Must not send credits. Will not receive flits.
ACTIVATE	Must not send flits. Must accept credits.	Must not send credits. Will not receive flits.
RUN	Can send flits. Must accept credits.	Must accept flits. Can send credits.
DEACTIVATE	Must not send flits, except for credit return flits. Must accept credits. Must return credit.	Must accept flits. Must stop sending credits.

CXSDEACTHINT is not part of the four-phase handshake. The receiver can assert this signal HIGH to indicate to the transmitter that it wants to go to a lower power state, therefore deactivating the link. It is implementation-defined whether the transmitter ignores the hint or uses it to influence link deactivation. The receiver can change the value of **CXSDEACTHINT** at any time regardless of link state.

If the transmitter has flits to send, it is expected, but not required, that it ignores **CXSDEACTHINT** and keeps the link in RUN state. If the transmitter has no flits to send, it can keep the link in RUN state or transition to STOP state. In this case, the transmitter can use **CXSDEACTHINT** to affect that decision.

One usage example in a CCIX system is an interconnect transitioning to a low-power state. The interconnect can directly transition the outbound channel to STOP state. The inbound channel is under control of the CCIX transport logic, however. The interconnect asserts **CXSDEACTHINT** on the inbound channel. If the transport logic has no flits to send, it can transition the inbound interface to STOP state allowing the interconnect to go to a low-power state.

B.9.2 Race conditions

A race condition exists when one side of the interface performs two actions at or around the same time.

There are two situations where one side of the interface performs two actions at or around the same time:

1. Changing the **CXSACTIVEREQ** or **CXSACTIVEACK** signal to change the state of the interface.
2. Sending an associated credit, flit, or credit return around the time of the state change.

This occurs in the following situations:

- When the receiver is asserting **CXSACTIVEACK**, to move from ACTIVATE to RUN, it is also permitted to start sending credits:
  - A race can occur between the sending of a credit, which is expected in the new state, and the assertion of the **CXSACTIVEACK** signal indicating the state change.
  - This is acceptable because the transmitter is required to be able to accept the credit in the previous state as well as in the new state.
  - For the receiver, it is permitted to send a credit in the same cycle that **CXSACTIVEACK** is asserted.
  - For the transmitter, it is required to accept a credit both before and after the assertion of **CXSACTIVEACK**.
- When the transmitter is deasserting **CXSACTIVEREQ**, to move from RUN to DEACTIVATE, it must stop sending flits:

— A race can occur between the last flit sent, which is expected in the previous state, and the deassertion of the **CXSACTIVE_REQ** signal indicating the state change.
— This is acceptable because the receiver is required to be able to accept the flit in the next state, as well as in the previous state.
— For the transmitter, it is permitted to send a flit in the last cycle that **CXSACTIVEACK** is asserted.
— For the receiver, it is required to accept flits both before and after the deassertion of **CXSACTIVEACK**.

These race conditions are possible because the **CXSACTIVEREQ** and **CXSACTIVEACK** need not have the same delay between transmitter and receiver as the other signals. In order for the interface to work correctly, the following signals from TX to RX must have exactly the same cycle delay between transmitter and receiver, and are expected to be synchronous:

- CXSVALID
- CXSDATA
- CXSCNTL
- CXSVALIDCHK
- CXSDATACHK
- CXSCNTLCHK
- CXSCRDRTN
- CXSCRDRTNCHK

Also, these two signals from RX to TX must have the same delay between receiver and transmitter, and are expected to be synchronous:

- CXSCRDGNT
- CXSCRDGNTCHK

The delay on the TX->RX signals can be different than the delay on the RX->TX signals.

These signals can have any delay, and need not have the same delay as each other or the other signals. They are expected to be synchronous:
- CXSACTIVEACK
- CXSDEACTHINT

The signal **CXSACTIVEREQ** can have any delay, and need not have the same delay as the other signals. This signal can be asynchronous and must be synchronized by the receiver.

Generally, the physical distance between the transmitter and receiver determines the number of flop stages required to achieve the desired frequency. That number of flop stages is most likely applied to all of the signals on the interface.

The exception is **CXSACTIVEREQ**. It is common for the receiver's clock to stop during the STOP state due to clock gating. **CXSTXACTIVEREQ** assertion may be used to restart that clock. It is possible that the flops between transmitter and receiver are in the receiver clock domain and are also clock gated during STOP state. Because of this, **CXSACTIVEREQ** may need to have a purely combinational path (no flops) between transmitter and receiver, and may be a multicycle path due to distance and required frequency of the interface. This is acceptable because **CXSACTIVEREQ** and **CXSACTIVEACK** form a four-phase handshake and can run asynchronously.

CXSACTIVEREQ should therefore be treated by the receiver as an asynchronous signal and run through appropriate synchronization logic to avoid metastability before use. **CXSACTIVEACK** and **CXSDEACTHINT** are only sent when clocks are running in both TX and RX, and therefore should be treated as synchronous signals. This means that **CXSACTIVEACK** and **CXSDEACTHINT** should not be multicycle path between RX and TX, although they can have multiple flops as needed.

B.9.3 Response to a new state

When moving to a new state, where the state change has been initiated by the other-side of the interface, a component might be required to change its behavior.

If the state change requires a component to start sending flits or credits, then there is no defined limit on the time taken for the component to start the new behavior. This new behavior only occurs in the new state.

If the state change requires a component to stop sending flits or credits, then the component is permitted to take some time to respond. In this scenario, it is possible to see behavior when first entering a new state which is not expected within that state.

The state change from RUN to DEACTIVATE is the point at which flits, credits, and credit returns stop being sent.

Flits are sent by the transmitter, which is also the component that determines the state change, and therefore the transmitter can ensure flits are not sent after the state change. However, a race condition might still occur as described previously.

Credits are sent by the receiver, but that component does not determine the state change. The receiver might take some time to react to the state change and therefore it is possible for credits to be sent when first entering the DEACTIVATE state.

The protocol requires that the receiver has stopped sending credits and has had all credits returned before it signals the change from DEACTIVATE to STOP.

Determining when to move to ACTIVATE or DEACTIVATE

The transmitter is always responsible for initiating the state change from RUN to STOP, or from STOP to RUN.

The transmitter itself can determine that a state change is needed. This can happen through a number of mechanisms.

The following examples are not exhaustive:

- The transmitter can determine that it has flits to send, so must move from STOP to RUN.
- The transmitter can determine that it has no activity to perform for a significant period of time, so can move from RUN to STOP.
- The transmitter can observe an independent sideband signal that indicates it should move either from RUN to STOP, or from STOP to RUN.
- The transmitter can observe the **CXSDEACTHINT** signal from the receiver and decide to move from RUN to STOP.

B.9.4 Interface activation and deactivation examples

This section provides interface activation and deactivation examples.

An activation of an interface is shown in the following figure. At time zero, the interface is in STOP state. The receiver could be clock-gated or powered down at this time. The transmitter asserted **CXSTXACTIVEREQ** and shifts to ACTIVATE state. It then waits for the receiver to wake up. The transmitter sees that the receiver is ready when **CXSTXACTIVEACK** is asserted. This indicates that the interface has moved to RUN state. In this case, **CXSTXCRDGNT** is asserted the same cycle, which allows the transmitter to begin sending flits. In this example, the transmitter receives a credit in the same cycle that the interface shifts to RUN state.

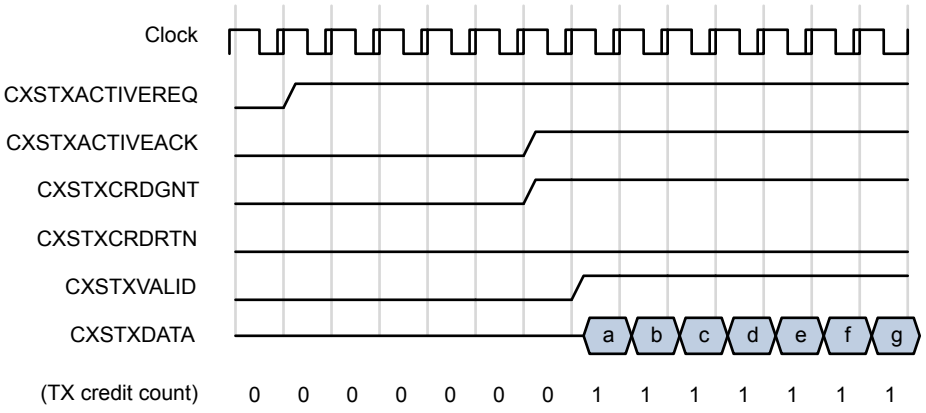

Figure B-10 Interface activation example

The following figure shows the same example with one modification: there is more delay between the receiver and transmitter on the **CXSTXACTIVEACK** path than there is on the **CXSTXCRDGNT** path. Because of this, the transmitter receives a credit while the interface is still in ACTIVATE state. However, the transmitter must wait to send a flit until the interface is in RUN state.

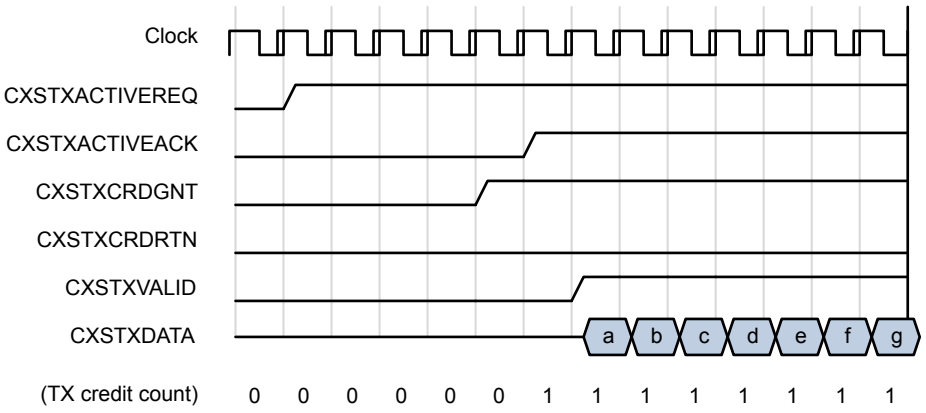

Figure B-11 Interface activation example with race

The following figure shows an interface deactivation example. The interface starts in RUN state. The transmitter runs out of flits to send and decides to deactivate the interface. The transmitter deasserts **CXSTXACTIVEREQ** taking the interface into DEACTIVATE state. Because the transmitter still has a non-zero credit count, the transmitter begins returning credits by asserting **CXSTXCRDRTN**.

The receiver continues to grant credits to the transmitter for a number of cycles until the receiver recognizes that the link is being deactivated. The transmitter must return the additional credits as well, asserting **CXSTXCRDRTN** until its credit count is zero and it sees **CXSTXACTIVEACK** deasserted, signaling the entry into STOP state. Because the receiver can't assert **CXSRXACTIVEACK** until it has all of the credits and there are no credit grants in flight, the transmitter never sees **CXSTXACTIVEACK** deasserted while the transmitter still has credits.

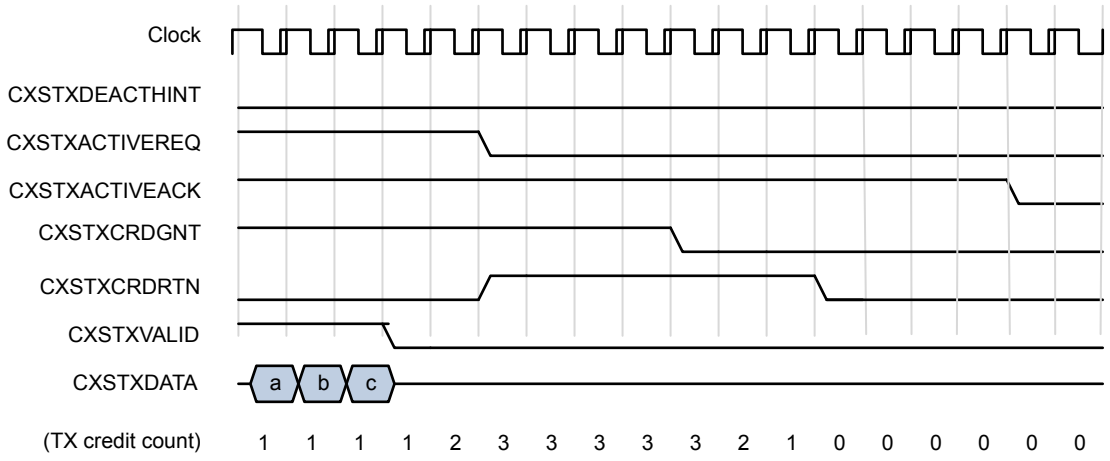

Figure B-12 Interface deactivation example

B.10 CXS packet continuous delivery guarantees

A receiver on a CXS interface can be built with a store-and-forward approach, in which each packet is fully received before it is used or sent out on another interface. Any receiver built in this way does not need to assert the **CXSCONTINUOUSDATA** attribute and can ignore this section.

However, if lowest latency is desired, a receiver can be built to begin transmission of a packet on another interface before the full packet has been received on the CXS interface. This results in lower latency, but if the downstream interface can't tolerate interruptions in the data flow (e.g. PCIe), this imposes a requirement on the CXS interface to deliver data at a rate high enough to ensure uninterrupted transmission of the full packet on the other interface.

The **CXSCONTINUOUSDATA** attribute is set by a transmitter if the transmitter can guarantee that a packet is not started on the CXS interface until transmitter can deliver all the data of that packet in subsequent cycles with no interruptions if it is given enough credits on the CXS interface. If a transmitter does not assert the **CXSCONTINUOUSDATA** attribute the receiver can't rely on the continuous delivery of data.

A transmitter that guarantees continuous delivery is generally designed such that a packet is not started on the interface until:

- The full packet is available in the transmitter.
- The packet is stored in the same clock domain or a higher frequency clock domain than the CXS interface.
- The datapath, clocking, and arbitration logic can guarantee delivery of the packet at full interface bandwidth.

One further implication is that the transmitter should not attempt to deactivate the link if that deactivation could occur at a time when some but not all packet data has been issued.

For continuous delivery to be effective and avoid the need for store-and-forward, the receiver must grant enough credits (and therefore have sufficient buffering) to keep the packet flowing at the required bandwidth. Specifying the buffering required is outside the scope of this specification, but in general the number of credits needed is a function of:

- The latency on **CXSCRDGNT** between receiver and transmitter.
- The maximum internal transmitter delay between **CXSTXCRDGNT** and **CXSTXVALID** when the transmitter has a packet stalled waiting for credits.
- The latency on **CXSVALID** between the transmitter and receiver.
- The microarchitecture of the receiver.
- The bandwidth of the downstream interface.

B.11 CXS Error signaling

This section describes how the CXS interface handles errors.

There are three error types:

- Transport errors between transmitter and receiver on CXS
- Packet errors on CXS
- Errors outside of the scope of the CXS interface

This section contains the following subsections:

B.11.1 Transport errors

Information on the CXS signals may be corrupted between the transmitter and receiver. One potential corruption source is a bit flipped from an alpha particle or voltage drop.

No *Single Error Detect* (SED), *Double Error Detect* (DED), or *Single Error Correct, Double Error Detect* (SECDED) protection on the corrupted interface signals leads to a silent error. This can cause unpredictable effects on the receiver or transmitter, including possible corrupt data, performance degradation (if a credit is lost), or the interface hanging.

For interface signals with data checking, there are four types of errors:

1. Single-bit error on signal protected by parity.
2. Duplicated or triplicated signals that are not all identical.
3. Double-bit error on signal protected by SECDED or ECC.
4. Single-bit error on signal protected by SECDED or ECC.

The first three cases are uncorrectable errors. The receiver of the signal (the transmitter for **CXSCRDGNT**, the receiver for all other signals) is responsible for detecting the error. The response to the error is implementation-defined, but should generally include recording information about the error and notifying the system that an unrecoverable error has occurred.

The last case is a correctable error. The receiver is expected to correct the error and proceed as if the error had not occurred. If the receiver asserts the attribute **CXSCONTINUOUSDATA**, any extra delay required to correct single-bit errors must not cause the continuous data guarantee to be violated.

In an uncorrectable error case, the receiver should generally attempt to continue operation after the error, if possible.

B.11.2 Packet errors

There are conditions which the transmitter may not be able to complete a packet which has been started on the CXS.

1. Uncorrectable Error:
   a. The transmitter has started a packet, but is permanently unable to send the full contents of the packet.
   b. For example, there is an uncorrectable error reading the later bytes of the packet from a RAM.
2. Error Correctable through Retry:
   a. The transmitter has started a packet and detected an error on that packet. The transmitter may have a mechanism to reissue that packet in the future.
   b. For example, a PCIe controller that passes through a packet coming from PCIe and later discovers a CRC error. The PCIe logic can request a retransmission of that packet.

In both of these cases, the transmitter must end the packet with the ENDERROR indicator in the control field. The receiver should then drop that packet and generally behave as if the packet was never sent. It

is, of course, permissible for the receiver to record the fact that the packet was dropped as part of performance monitoring logic, but the receiver should not treat the dropped packet as an error condition.

The transmitter has responsibility for retransmitting the packet, if possible, or logging/reporting the error through implementation-defined means.

If the receiver and transmitter both assert the **CXSERRORFULLDATA** attribute, the transmitter should send the number of bytes of data specified in the packet header before ending the packet with END and ENDERROR, even if the error is detected somewhere in the middle of the packet. This may mean padding the packet out with zeroes or invalid data to achieve the correct length. The encoding of the packet size within the packet is outside the scope of the CXS specification.

If **CXSERRORFULLDATA** is not an attribute of the transmitter the packet can be terminated on the next flit regardless of the original planned length of the packet.

B.11.3 Errors outside of CXS scope

If an error is detected by the transmitter logic early enough that the packet is not sent across the CXS interface, the CXS interface does not define a method for the transmitter to inform the receiver that an error has occurred.

In general, this should be considered an error in the transmitter and logged/reported to the system through implementation specific means.

Any bad data or errors that are reported inside the CCIX messages, such as poison data, or an error response on a memory request to an invalid address, is communicated through the CCIX protocol messages within the CXS packets. These errors are outside of the scope of CXS.

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

C.1 Revisions

Differences between released versions of the document are listed in this appendix.

Table C-1 Differences between issue 0000-00 and issue 0000-01

Change	Location	Affects
CMN-600 product name update.	Various locations in manual.	r0p0
Various product overview changes.	*Chapter 1 Introduction* on page 1-13.	
Various product feature changes.	*Chapter 2 Functional Description* on page 2-36.	
Register content update.	*3.3 Register descriptions* on page 3-194.	
System Level Cache content changes.	*Chapter 4 SLC Memory System* on page 4-1078.	
Updated Debug Trace and PMU section.	*Chapter 5 Debug trace and PMU* on page 5-1100.	
Updated signal descriptions.	*Chapter 6 Performance Optimization and Monitoring* on page 6-1124.	

Table C-2 Differences between issue 0000-01 and issue 0101-00

Change	Location	Affects
Addition of CML product information.	*1.1 About CMN-600* on page 1-14 Optional CML product overview in Section 1.1.	r1p1
Addition of CML product information.	*1.3 Features* on page 1-17 introducing the Optional CML features in Section 1.3.	
Addition of CML product information.	*1.4 Interfaces* on page 1-21 updated Figure 1-1 including CML interfaces in Section 1.4.	
New configuration information.	Configurable components new Section 1.5.1 added.	
CML interfaces content added.	*1.5.1 System component selection* on page 1-22 Section 1.5.2 updated.	
Configuration tables 1-1, 1-2, and 1-3 updated with CMN clarifications and new CML content..	*1.5.2 Mesh sizing and top-level configuration* on page 1-23 Section 1.5.2 updated.	
CXG content added.	*2.1.6 CXG* on page 2-41 Section 2.1.6 updated.	
Cross chip routing an ID mapping information added/updated.	*2.23 Cross chip routing and ID mapping* on page 2-134 Section 2.3 updated including several flow diagrams.	
Updated flow diagrams.	CCIX ID management and mapping Section 2.5 updated including several flow diagrams.	
New CML discovery information.	*2.5 Discovery* on page 2-54 Section 2.7 updated.	
Table 2-7 updated with XID values.	*2.5.1 Configuration address space organization* on page 2-54 Section 2.7 updated.	
Table 2-8 added with new CML node ID information.	*2.5.2 Configuration register node structure* on page 2-57 Section 2.7.2 updated.	
Table 2-10 updated: removed invalid values.	*2.5.3 Child pointers* on page 2-60 Section 2.7.2.	
Atomics clarification for RN-I interfaces added.	*2.7 Atomics* on page 2-67 Section 2.9.	
Global address map topic added.	Global address map Section 2.17.1.	
RN-SAM clarification regarding GIC support. Also, RN-SAM target ID selection priorities clarified.	*2.16 RN SAM* on page 2-100 Section 2.17.2.	
RA-SAM information added for CXG.	*2.17 CXRA SAM* on page 2-105 Section 2.17.3.	
HN-F clarification regarding system implementation.	*2.18 HN-F SAM* on page 2-106 Section 2.18.	
Addition of CCIX port aggregation.	*2.19.4 Support for CCIX Port Aggregation* on page 2-117 topic.	
Clock domain diagrams updated to include CX-LA functionality: Figures 2-54 and 2-55.	*2.27.1 Clock domains* on page 2-145 section.	
Global clock information updated to include CML support: Table 2-48.	*2.27.5 Clock enable inputs* on page 2-148 section.	
Section 2.21.1 added to include CML information.	*2.28.1 CML reset* on page 2-151 section.	
Addition of CML register content.	*3.3.11 CXHA configuration registers* on page 3-881, *3.3.12 CXRA configuration registers* on page 3-945, and *3.3.13 CXLA configuration registers* on page 3-1025 register sections.	
Various updated signal descriptions to include CML support.	*Appendix A Signal Descriptions* on page Appx-A-1149 section.	
CXS specification added including all Appendix B subsections.	*Appendix B CXS Specification* on page Appx-B-1187 section.	

Table C-3 Differences between LAC issue 0101-00 and EAC issue 0100-00

Change	Location	Affects
Configurable option addition to Table 1-2. Global parameters section.	*1.5.2 Mesh sizing and top-level configuration* on page 1-23.	r1p0
Configurable option addition to Table 1-3. HN-I and SBSX sections.	*1.5.3 Device placement and configuration* on page 1-26.	
Various text edits for clarification and technical accuracy.	*2.14 Error handling* on page 2-82.	
Various text edits for technical accuracy.	*2.14.1 Error types* on page 2-85.	
Updated tables contain a new bit 58: physical_mem_en	*2.22 HN-I SAM* on page 2-124.	
Added programming sequence.	*2.19 RN and HN-F SAM programming* on page 2-112.	
Tables 1-2 and 1-3 updated; default values added.	*1.5.2 Mesh sizing and top-level configuration* on page 1-23 and *1.5.3 Device placement and configuration* on page 1-26.	
Table 2-8, updated CXHA and CXLA values.	*2.5.2 Configuration register node structure* on page 2-57.	
Added new topic.	*4.10 Data Source Handling* on page 4-1091.	
Added new topic.	*6.9 Occupancy and lifetime measurement using PMU events* on page 6-1147.	
Register content update.	*3.3 Register descriptions* on page 3-194.	
Added new topic.	*Delays at SBSX bridges due to backpressure* on page 6-1139.	
Added new topics.	*Tracker occupancy analysis* on page 6-1140 and *Tracker occupancy analysis in HN-I* on page 6-1143.	
NIDEN and SPNIDEN note added.	*5.1 DT system overview* on page 5-1101.	
BRESP values updated.	*A.9.1 ACE-Lite-with-DVM slave interface signals* on page Appx-A-1163 and *A.9.2 AXI/ACE-Lite master interface signals* on page Appx-A-1168.	

Table C-4 Differences between EAC issue 0100-00 and EAC issue 0100-01

Change	Location	Affects
Added new topic.	*2.14.10 CXHA error handling* on page 2-97.	r1p0
Added new section including seven sub-topics.	*3.5 CML programming* on page 3-1068.	
Text edits for technical clarifications.	*2.6 Addressing capabilities* on page 2-66.	
Text edits for technical clarifications.	*2.7 Atomics* on page 2-67.	
Added new topic.	*1.3.4 CCIX and CXS property support* on page 1-19.	

Table C-5 Differences between EAC issue 0100-00 and EAC issue 0101-01

Change	Location	Affects
Updated figure RN SAM target ID selection policy.	*2.16.1 Target IDs* on page 2-100.	r1p1
Text edits for technical accuracy.	*2.18 HN-F SAM* on page 2-106.	
GIC Memory partition sizes updated.	*2.19.2 Region size configuration* on page 2-113.	
Content updated.	*2.27.2 CML clock inputs* on page 2-145.	
Updated signal names.	*2.29.4 P-Channel on device reset* on page 2-156.	
Updated register reset values.	**por_dt_dbg_id** and **por_rnsam_unit_info**.	
Text edits for technical accuracy.	*3.4.1 Boot-time programming requirements* on page 3-1067.	
Updated parameters for technical accuracy.	*4.1 About the SLC memory system* on page 4-1079.	
Updated event names.	*Read and write delays at RN-I bridges* on page 6-1135.	
Updated endpoint references.	*2.22 HN-I SAM* on page 2-124.	

Table C-6 Differences between EAC issue 0101-01 and EAC issue 0102-00

Change	Location	Affects
Updated RN-F LDID assignment and new bullet added for LDIDs.	*2.23 Cross chip routing and ID mapping* on page 2-134.	r1p2
Figures 2-32, 2-33, and 2-34 updated to include CXHA blocks.	*2.14 Error handling* on page 2-82.	
Updated Table 2-22 for ERRMISC fields.	*2.14.3 Error detection, signaling, and reporting* on page 2-87.	
New HN-F bullet.	*2.19.1 SAM programming sequence* on page 2-112.	
Updated figure 2-57 to include NOSFLC references and Logic=ON transition states.	*2.29.7 HN-F power domains* on page 2-157.	
Updated CMO propagation bullet and corrections to OCM support bullets.	*4.1 About the SLC memory system* on page 4-1079.	
Updated descriptions for WUSER_S, RUSER_S, WUSER_M, and RUSER_M. Also, new notes added for these channel signals.	*A.9.1 ACE-Lite-with-DVM slave interface signals* on page Appx-A-1163.	
Updated descriptions for WUSER_M and RUSER_M. Also, new notes added for these channel signals.	*A.9.2 AXI/ACE-Lite master interface signals* on page Appx-A-1168.	
Various register descriptions and content updates.	Register description section.	
Added new section for CHI support for CML.	*1.3.3 CML Properties, Support, and Requirements* on page 1-18.	

Table C-7 Differences between EAC issue 0102-00 and EAC issue 0103-00

Change	Location	Affects
New RA SAM configuration register table.	*2.19.2 Region size configuration* on page 2-113.	r1p3
CCIX port aggregation content added.	*3.5.1 CMN-600 CML (CCIX) Related Programmable Registers* on page 3-1068.	
Various register descriptions and content updates.	*3.3 Register descriptions* on page 3-194.	
Updated MCSX, MCSY, and DCS count values.	*1.5.2 Mesh sizing and top-level configuration* on page 1-23.	
Updated NUM_WR_REQ, NUM_RD_REQ, NUM_RD_BUF, and NUM_AXI_REQS values.	*1.5.3 Device placement and configuration* on page 1-26.	

Table C-8 Differences between EAC issue 0103-00 and EAC issue 0103-01

Change	Location	Affects
Updated **maxpacketsize** field.	por_cxla_ccix_prop_configured	r1p3-01
CCIX architecture update.	*1.2 Compliance* on page 1-16.	
Revision bits register update.	por_cfgm_periph_id_2_periph_id_3	
Section rewrite.	*2.29.10 HN-F power domain completion interrupt* on page 2-162.	

Table C-9 Differences between EAC issue 0103-01 and EAC issue 0200-00

Change	Location	Affects
CACTIVE_S signal no longer supported.	*A.9.1 ACE-Lite-with-DVM slave interface signals* on page Appx-A-1163.	r2p0-00
New information on HN-D access of DN events.	*6.7 DN performance events* on page 6-1145.	
New information on R2 supported features.	*4.9 CMN-600 Hardware-based cache flush engine* on page 4-1089, *2.20 RN and HN-F SAM R2 Support* on page 2-120, *4.14 Source-based SLC cache partitioning* on page 4-1096, and *4.14 Source-based SLC cache partitioning* on page 4-1096.	
External child operation clarified.	*2.5.3 Child pointers* on page 2-60.	
Table 1-5, Updated Global parameter, Processor resources, and System cache values.	*1.5.2 Mesh sizing and top-level configuration* on page 1-23.	
Programming sequence clarification.	*2.19.4 Support for CCIX Port Aggregation* on page 2-117.	
New information on PMU event updates for CXRA in Table 6-1.	*6.2 About the Performance Monitoring Unit* on page 6-1126.	
New registers for R2.	*3.3 Register descriptions* on page 3-194.	
New information on CML properties in Table 1-1.	*1.3.3 CML Properties, Support, and Requirements* on page 1-18.	
New information on A4S features and signal list.	*2.26 GIC communication over AXI4 Stream ports* on page 2-144and *A.9.3 A4S Signal list* on page Appx-A-1171.	
New information on CAL topic.	*2.1.13 Component Aggregation Layer* on page 2-43.	
New information on R2 VMID filter.	*2.12 DVM messages* on page 2-79.	
New information on SBSX errors.	*2.14.7 SBSX error handling* on page 2-95.	

Table C-10 Differences between EAC issue 0200-00 and EAC issue 0300-00

Change	Location	Affects
New information on R3 supported features.	*1.3.2 R3 Features* on page 1-18.	r3p0-00
New registers for R3.	*3.3 Register descriptions* on page 3-194.	
New information on 128 RN-F support.	*2.24 CMN-600 R3 128 RN-F support* on page 2-140.	
New information on CPAGs.	*2.25 CCIX Port Aggregation groups* on page 2-143.	
New CCS parameters and example configuration (CMN-600 R2).	*1.5.2 Mesh sizing and top-level configuration* on page 1-23 and *1.5.3 Device placement and configuration* on page 1-26.	