ARM Corelink™ CCN-508 (PL-508)

Software Developers Errata Notice

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- the document title
- the document number, ARM-ECM-0410995
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Release Information

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text in Chapter 2. Fixed errata are not shown as updated unless the erratum text has changed. The summary table in section 2.2 identifies errata that have been fixed in each product revision.

09 Apr 2015: Changes in Document v1

Page	Status	ID	Cat	Rare	Summary of Erratum
7	New	843871	CatB	Rare	HAM->FAM power domain transition can cause unpredictable behavior
8	New	843869	CatC		Potential starvation for Low or Medium QOS Non-cacheable transactions to a CHI DMC in a heavily-loaded system
9	New	843870	CatC		L3 and Snoop Filter single-bit ECC error count overflows do not generate INTREQ

Contents

Chapter 1.
Introduction

This chapter introduces the errata notice for the ARM Corelink^{TM} CCN-508 interconnect.

1.1. Scope of this document

This document describes errata categorized by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

This document describes errata that may impact anyone who is developing software that will run on implementations of this ARM product.

1.2. Categorization of errata

Errata recorded in this document are split into the following levels of severity:

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Table 1   **Categorization of errata**

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Errata Type	Definition
Category A	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
Category A(rare)	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category B	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
Category B(rare)	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
Category C	A minor error.

Chapter 2.
Errata Descriptions

2.1. Product Revision Status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n*   Identifies the major revision of the product.

p*n*   Identifies the minor revision or modification status of the product.

2.2. Revisions Affected

Table 2 below lists the product revisions affected by each erratum. A cell marked with $\boxed{\textbf{X}}$ indicates that the erratum affects the revision shown at the top of that column.

Refer to the reference material supplied with your product to identify the revision of the IP.

Table 2   **Revisions Affected**

ID	Cat	Rare	Summary of Erratum	r0p0	r0p1
843871	CatB	Rare	HAM->FAM power domain transition can cause unpredictable behavior	X	
843870	CatC		L3 and Snoop Filter single-bit ECC error count overflows do not generate INTREQ	X	
843869	CatC		Potential starvation for Low or Medium QOS Non-cacheable transactions to a CHI DMC in a heavily-loaded system	X	

2.3. Category A

There are no errata in this category

2.4. Category A (Rare)

There are no errata in this category

2.5. Category B

There are no errata in this category

2.6. Category B (Rare)

843871: HAM->FAM power domain transition can cause unpredictable behavior

Category B Rare
Products Affected: CCN-508 Cache Coherent Network.
Present in: r0p0

Description

The CCN-508 HN-F (L3) can re-execute memory transactions if there are Cacheable transactions present in the HN-F in the 0 to 4K address range, when an HAM->FAM power state transition (half L3 to full L3 transition) occurs.

The issue occurs when the set address for the L3 initialization op falsely hazards against an L3 victim in the 0 to 4K physical address range, which results in a pipeline replay of an un-associated transaction in the HN-F tracker.

Configurations Affected

Any CCN-508 configuration with 3-cycle HN-F RAMs that uses the HN-F HAM power state feature.

Implications

CCN-508 HN-F can re-execute memory transactions during the HAM->FAM power state transition, which results in unpredictable behavior.

Workaround

If you can modify the hardware, then you can implement any one of the following workarounds

- Configure CCN-508 to use 2-cycle HN-F RAMs.

- Remap the P-Channel HAM->FAM power state transition to HAM->NOL3 followed by NOL3->FAM.

- Disable the P-Channel HAM power state.

Alternatively, in software you can implement any one of the following workarounds:

- Set the lowest 4K of the physical address space as L3 Non-cacheable.

- Remap the software-initiated HAM->FAM power state transition to HAM->NOL3 followed by NOL3->FAM.

- Disable the software-initiated HAM power state.

2.7. Category C

843869: Potential starvation for Low or Medium QOS Non-cacheable transactions to a CHI DMC in a heavily-loaded system

Category C
Products Affected: CCN-508 Cache Coherent Network.
Present in: r0p0

Description

The CCN-508 receives CHI protocol retry responses when a CHI DMC cannot accept read or write requests due to trackers being full or other lack of resource scenarios. When the DMC is able to accept a retried transaction, it sends a credit response to CCN-508 which can be associated with a QOS level from the PCRED type field.

Under conditions where all transactions are non-cacheable, are retried by the DMC, and are issued to CCN-508 in a repetitive/periodic sequence, Low or Medium QOS transactions can be starved while HighHigh and High QOS transactions make forward progress. The Low or Medium QOS transactions make progress if any of the necessary conditions are removed, such as a reduction in DMC protocol retries, reduction in overall Non-cacheable traffic, or the removal of the repetitive/periodic nature of the non-cacheable traffic.

Configurations Effected

Any CCN-508 configuration using a CHI DMC that uses PCRED type to manage Low, Medium, High, and HighHigh QOS traffic.

Conditions

Low QOS transactions can be starved under the following conditions:

1) All transactions issued to CCN-508 are non-cacheable AND

2) The CHI DMC retries all non-HighHigh QOS transactions AND

3) Transactions are issued to CCN-508 in a repetitive/periodic sequence AND

4) High-bandwidth, HighHigh transactions occur

Implications

Non-cacheable Low or Medium QOS transactions can be starved by High and HighHigh QOS transactions in a heavily loaded system where all DMC transactions are retried.

Workaround

1) Do not use high-bandwidth HighHigh traffic, HighHigh QOS is intended for low-bandwidth, low-latency traffic.

2) If using a DMC-520 then program the DMC-520 credit_control register with a prescaler value of 8 and credit_count value of 1. This results in a relatively equal distribution of credits for the H/M/L QOS retried transactions, and greatly reduces and removes the occurrence of this starvation scenario.

3) Do not use a combination of Low/Medium/High QOS traffic by configuring the CCN-508 QOS regulators.

843870: L3 and Snoop Filter single-bit ECC error count overflows do not generate INTREQ

Category C
Products Affected: CCN-508 Cache Coherent Network.
Present in: r0p0

Description

CCN-508 has a single-bit ECC error counter that is intended to assert the INTREQ output pin when the counter overflows. The counter functions correctly, but the INTREQ is not asserted when the counter overflows.

Configurations Affected

All CCN-508 configurations that require INTREQ assertion on single-bit ECC error count overflows.

Conditions

The CCN-508 INTREQ is not generated for any single-bit ECC error overflow conditions.

Implications

CCN-508 will not assert INTREQ for single-bit ECC error overflow conditions.

Workaround

Periodically read the CCN-508 HN-F err_syndrome_reg0 registers to observe the single-bit error count.