Application Note

Additional DSTREAM TCK Filtering for heavily branched JTAG chains

Version 4.0

Non-Confidential - Published

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Release Information

The following changes have been made to this Application Note.

Document History

Date	Issue	Confidentiality	Change
10/10/2019	**A**	Non-Confidential - Published	First release

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Confidentiality Status

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Product Status

The information in this document is Final, that is for a developed product.

Web Address

http://www.arm.com

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1 Conventions and Feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

monospace denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

mono**space** denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

monospace italic
: denotes arguments to commands and functions where the argument is to be replaced by a specific value.

monospace bold
: denotes language keywords when used outside example code.

italic highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold highlights interface elements, such as menu names. Also used for emphasis in descriptive lists, where appropriate, and for ARM® processor signal names.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

- Your name and company.
- The serial number of the product.
- Details of the release you are using.
- Details of the platform you are using, such as the hardware platform, operating system type and version.
- A small standalone sample of code that reproduces the problem.
- A clear explanation of what you expected to happen, and what actually happened.
- The commands you used, including any command-line options.
- Sample output illustrating the problem.
- The version string of the tools, including the version number and build numbers.

Feedback on documentation

If you have comments on the documentation, e-mail errata@arm.com. Give:

- The title.

- The number, ARM-ECM-0725988, A.
- If viewing online, the topic names to which your comments apply.
- If viewing a PDF version of a document, the page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

ARM periodically provides updates and corrections to its documentation on the ARM Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- ARM Information Center, http://infocenter.arm.com/help/index.jsp.
- ARM Technical Support Knowledge Articles, http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html.
- ARM Support and Maintenance, http://www.arm.com/support/services/support-maintenance.php.
- ARM Glossary, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

2 Preface

This Application Note is intended for users of the Arm DSTREAM debug unit who are debugging a target system with multiple JTAG branches.

3 Introduction

This Application Note addresses a problem which might occur when using DSTREAM with a multi-branch JTAG chain, particularly one which contains physically long and uneven branches.

4 Problem Description

The JTAG interface is a synchronous interface which relies on a clock signal (TCK) to tell the target devices in the scan-chain when to sample the TDI and TMS signals.

When using a JTAG chain with only one end-point, this is a simple matter. The TCK signal is series-terminated within the debug unit, in this case DSTREAM. This way the signal reaches full rail-to-rail logic levels when it is received by the high-impedance TCK input of the target device. This provides good signal integrity and a monotonic clock signal.

When a target system contains multiple JTAG devices on a single JTAG chain, things become more complicated. The TCK signal must be split into two branches of some physical length, causing signal reflection issues, and usually with an impedance mis-match, causing problems with signal amplitudes.

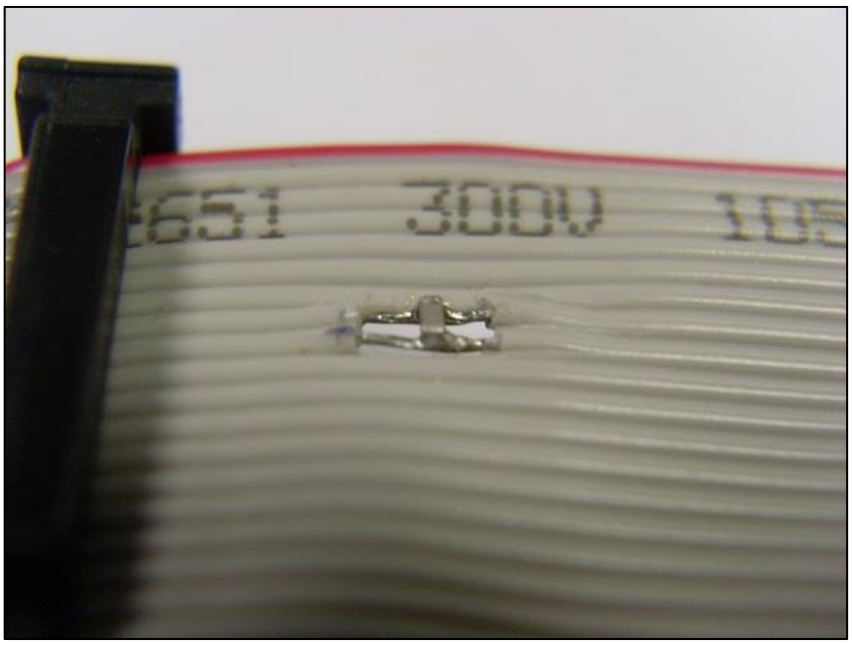
The target system's JTAG chain might perform perfectly when being driven by slow output drivers (like boundary-scan tools or low-cost debug units) but might experience problems when being driven by fast output drivers (like the DSTREAM or ULINK Pro range of debug units). These debug units use fast output drivers with high slew-rates to achieve high bandwidth communication with the target system.

Ideally, any target system that is required to work with high-speed JTAG tools should be designed to overcome these issues by using buffers to 'fan-out' the TCK signal into the various JTAG branches. This is good practice in digital electronics and should be done wherever any clock signal is split into multiple branches.

5 Workarounds

While the DSTREAM-ST and later units have a switchable slew-rate filter to overcome this issue, the DSTREAM and earlier units do not. If a DSTREAM unit needs to work with a heavily branched JTAG chain, there are a number of ways to achieve this.

- Modify the target system to include signal buffers on the TCK signal – this might not always be possible but would allow the best bandwidth of the JTAG connection.
- Modify the target system to include resistors where the TCK signal is split – this works by decoupling the branches from each other and reducing the slew rate slightly. This has been known to work with some target systems using 100R resistors on each branch of the TCK signal, but it reduces the JTAG bandwidth slightly.
- Modify the debug cable to introduce a TCK capacitor close to the debug unit – this effectively combines the 33R series resistor within DSTREAM with an external capacitor to form an RC filter. The recommended value of this capacitor is 220pF and, ideally, should be as small as possible. This capacitor would connect between the TCK signal and one of the adjacent GND signals. See the picture below for an example of the capacitor modification.



The red stripe on one edge of the cable indicates signal 1 (connected to pin 1) and the capacitor is connected between signals 8 and 9 (using 9 and 10 would also work). The capacitor shown is a 220pF 50V capacitor in an 0603 package. Insulation using PVC tape or heat-shrink sleeving might be required if there is a possibility of this device shorting on a metal surface or voltage source.

Next, connect this cable so that the capacitor is close to the DSTREAM unit. If it is used the other way around, the inductance of the cable could cause the TCK signal to ‘ring’ and might induce false clock edges.

If pre-modified cables are required, these will be issued for free by Arm upon request.