Application Note AN539

Arm® SSE-123 Example Subsystem for MPS2+

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Release Information

The following changes have been made to this Application Note.

Contents

SSE-123 Example Subsystem for MPS2+

1 Conventions and Feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

`monospace`   denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space   denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
denotes arguments to commands and functions where the argument is to be replaced by a specific value.

`monospace bold`
denotes language keywords when used outside example code.

italic   highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold   highlights interface elements, such as menu names. Denotes signal names. Also used for emphasis in descriptive lists, where appropriate.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

- Your name and company.

- The serial number of the product.

- Details of the release you are using.

- Details of the platform you are using, such as the hardware platform, operating system type and version.

- A small standalone sample of code that reproduces the problem.

- A clear explanation of what you expected to happen, and what actually happened.

- The commands you used, including any command-line options.

- Sample output illustrating the problem.

- The version string of the tools, including the version number and build numbers.

Feedback on documentation

If you have comments on the documentation, e-mail `errata@arm.com`. Give:

- The title.

- The number, Arm DAI 0539A.

- If viewing online, the topic names to which your comments apply.

- If viewing a PDF version of a document, the page numbers to which your comments apply.

- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Arm periodically provides updates and corrections to its documentation on the Arm Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- Arm Information Center, `http://infocenter.arm.com/help/index.jsp`

- Arm Technical Support Knowledge Articles,
  `http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html`

- Arm Support and Maintenance,
  `http://www.arm.com/support/services/support-maintenance.php`

- Arm Glossary, `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014g/index.html`

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

2 Preface

2.1 Purpose of this application note

This document discusses the operation of Arm Application Note AN539. This is a Soft Macro Model (SMM) implementation of the SSE-123 Integration with SIE-200 and CMSDK components targeting the MPS2+ FPGA Prototyping board.

2.2 References

- *Arm DDI 0218 – PrimeCell® SingleMaster DMA Controller (PL081) Technical Reference Manual.*

- *Arm 100112_0200_07_en– Arm® MPS2 and MPS2+ FPGA Prototyping Boards Technical Reference Manual*

- *MCBQVGA-TS-Display-v12 – Keil MCBSTM32F200 display board schematic.*

- *Arm 101370 – Arm® SSE-123 Example Subsystem Technical Reference Manual.*

- *Arm DDI 0479C – Cortex™-M System Design Kit Technical Reference Manual*

- *Arm DDI 0571F – Arm® SIE-200 System IP for Embedded Technical Reference Manual*

The following books are only available to licensees or require registration with Arm.

- *Arm DIT0062C – Cortex™-M23 Processor Integration and Implementation Manual*

- *Arm 101372 - Arm® SSE-123 Example Subsystem Configuration and Integration Manual.*

2.3 Terms and abbreviations

CMSDK	*Cortex-M* System Design Kit.
DMA	Direct Memory Access.
MCC	Motherboard Configuration Controller.
RAM	Random Access Memory.
FPGA	Field Programmable Gate Array.
SCC	Serial Configuration Controller.
TRM	Technical Reference Manual.
APB	Advanced Peripheral Bus.
AHB	Advanced High-performance Bus.
RTL	Register Transfer Level.
SMM	Soft Macrocell Model.
MSC	Master Security Controller
PPC	Peripheral Protection Controller
EAM	Exclusive Access Controller

MPC	Memory Protection Controller
IDAU	Implementation Defined Attribution Unit
MPS2+	MPS2+ FPGA Prototyping board
R/W	Read/Write
MTB	Micro Trace Buffer

2.4   Subsystem version details

This SMM is generated using various packages. These are detailed below.

Version	Descriptions
BP210 r1p0	**Arm ® Cortex®-M System Design Kit** Full version of the design kit supporting Cortex-M0, Cortex-M0 DesignStart®, Cortex-M0+, Cortex-M3 and Cortex-M4. Also contains the AHB Bus Matrix and advanced AHB components.
BP300 r3p1	**Arm ® SIE-200** SIE-200 is a system IP library to enable ARMv8-M and TrustZone® for v8-M ecosystem. All SIE-200 components have AHB5 interfaces to support Armv8-M processors.
CG065 r0p0-00eac0	**Arm ® SSE-123**
AT621 r1p0	**Arm® Cortex®-M23**
PL081 r1p2	**PrimeCell® Single Master DMA Controller**
PL022 r1p4	**Arm PrimeCell® Synchronous Serial Port**

Table 2-1 : Module versions

2.5   Encryption key

Arm programs the MPS2+ motherboard with a decryption key. This key is required to decrypt prebuilt images.

Caution

A battery supplies power to the key storage area of the FPGA. Any keys stored in the FPGA might be lost when battery power is lost. If this happens you must return the board to Arm for reprogramming of the key.

3 Overview

3.1 System block diagram

Figure 3-1 : System Overview, shows the high-level diagram of the full SMM-SSE-123 MPS2+ FPGA System.
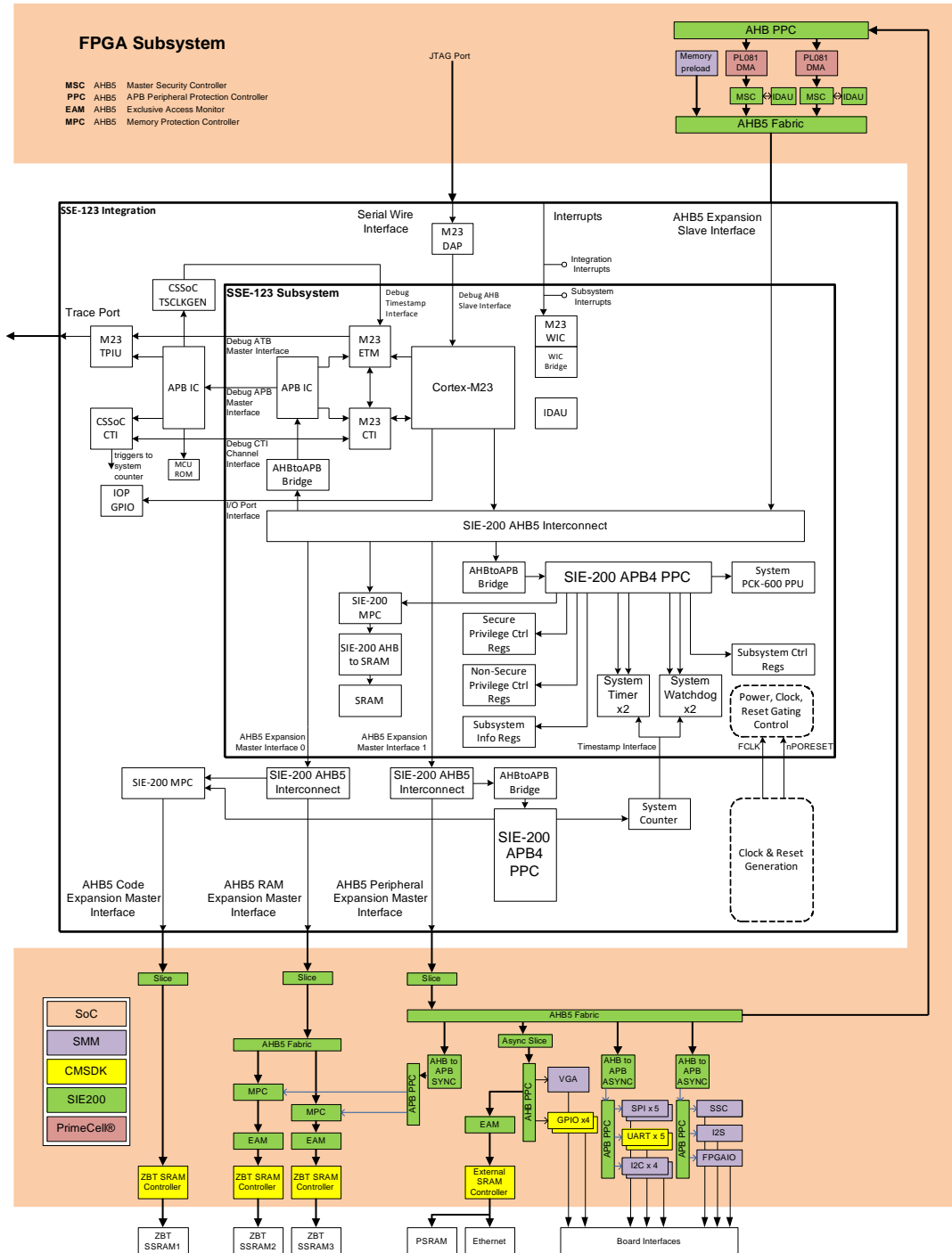
Figure 3-1 : System Overview

Note how the FPGA Subsystem extends the SSE-123 Integration by adding to its expansion interfaces.

3.2   SIE-200 components

The following SIE-200 components are used in the FPGA wrapper for the SSE-123 Integration:

- TrustZone AHB5 peripheral protection controller.

- AHB5 bus matrix.

- AHB5 to AHB5 asynchronous bridge.

- AHB5 to AHB5 synchronous bridge.

- AHB5 to APB asynchronous bridge.

- AHB5 to APB synchronous bridge.

- TrustZone APB4 peripheral protection controller.

- TrustZone AHB5 memory protection controller.

- AHB5 exclusive access monitor.

- AHB5 default slave.

3.3   Memory and peripheral protection note

The SIE-200 MPC and PPC components can affect memory and IO security management and must be configured as required for your application. See *Arm® SIE-200 System IP for Embedded Technical Reference Manual* for further details.

3.4   SSE-123 Integration Memory Map Overview

This memory map includes information regarding IDAU security information for memory regions defined by SSE-123 Integration. It does not define what is implemented in those regions. Please see the following pages for further details of this FPGA implementation and the *Arm® SSE-123 Example Subsystem Configuration and Integration Manual* for more details.

ROW ID	Address From	Address To	Size	Region Name	Description	Alias with Row ID	IDAU Region Values Security	IDAU Region Values ID AUID	IDAU Region Values NSC
1	0x0000_0000	0x0DFF_FFFF	224MB	Code Memory	Maps to AHB5 Master Expansion Code Interface	4	NS	0	0
2	0x0E00_0000	0x0E00_1FFF	8KB	Reserved	Reserved				
3	0x0E00_2000	0x0FFF_FFFF	-	Reserved	Reserved				
4	0x1000_0000	0x1DFF_FFFF	224MB	Code Memory	Maps to AHB5 Master Expansion Code Interface	1	S	1	CODE NSC
5	0x1E00_0000	0x1E00_1FFF	8KB	Reserved	Reserved				
6	0x1E00_2000	0x1FFF_FFFF	-	Reserved	Reserved				
7	0x2000_0000	0x20FF_FFFF	16MB	Internal SRAM	Internal SRAM Code Area Note: Full 16MB is not fully decoded. SSE-123 FPGA SRAM maps 256KB	10	NS	2	0
8	0x2100_0000	0x27FF_FFFF	112MB	Reserved	Reserved				
9	0x2800_0000	0x2FFF_FFFF	128MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface for external SRAM Note: Full 128MB is not fully decoded. Refer to Table 3-3 : SSRAM2 and SSRAM3 address mapping for more details	12			
10	0x3000_0000	0x30FF_FFFF	16MB	Internal SRAM	Internal SRAM Code Area Note: Full 16MB is not fully decoded. SSE-123 FPGA SRAM maps 256KB	7	S	3	RAMNSC
11	0x3100_0000	0x37FF_FFFF	112MB	Reserved	Reserved				
12	0x3800_0000	0x3FFF_FFFF	128MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface for external SRAM Note: Full 128MB is not fully decoded. Refer to Table 3-3 : SSRAM2 and SSRAM3 address mapping for more details	9			
13	0x4000_0000	0x4000_0FFF	4KB	Base Peripheral	Subsystem Timer 0	25	NS	4	0
14	0x4000_1000	0x4000_1FFF	4KB	Base Peripheral	Subsystem Timer 1	26			

#	Start	End	Size	Block	Description				
15	0x4000_2000	0x4001_FFFF	120KB	Reserved	Reserved				
16	0x4002_0000	0x4002_0FFF	4KB	System Control	Subsystem information registers	22			
17	0x4002_1000	0x4007_FFFF	380KB	Reserved	Reserved				
18	0x4008_0000	0x4008_0FFF	4KB	System Control	Non-Secure Privilege Control Registers				
19	0x4008_1000	0x4008_2FFF	8KB	System Control	Non-Secure Subsystem Watchdog				
20	0x4003_0000	0x4008_7FFF	20KB	Reserved	Reserved				
21	0x4008_8000	0x4008_BFFF	16KB	System Control	Reserved				
22	0x4008_C000	0x400E_FFFF	464KB	Reserved	Reserved				
23	0x400F_0000	0x400F_FFFF	64KB	Reserved	Reserved				
24	0x4010_0000	0x4FFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface				
25	0x5000_0000	0x5000_0FFF	4KB	Base Peripheral	Subsystem Timer 0	13			
26	0x5000_1000	0x5000_1FFF	4KB	Base Peripheral	Subsystem Timer 1	14			
27	0x5000_2000	0x5001_FFFF	120KB	Reserved	Reserved				
28	0x5002_0000	0x5002_0FFF	4KB	System Control	Subsystem information registers	17			
29	0x5002_1000	0x5002_1FFF	4KB	System Control	Subsystem control registers				
30	0x5002_2000	0x5002_2FFF	4KB	System Control	System PPU				
31	0x5002_3000	0x5002_6FFF	16KB	Reserved	Reserved				
32	0x5002_7000	0x5002_7FFF	4KB	System Control	Reserved				
33	0x5002_8000	0x5007_FFFF	352KB	Reserved	Reserved		S	5	0
34	0x5008_0000	0x5008_0FFF	4KB	System Control	Secure Privilege Control Registers				
35	0x5008_1000	0x5008_2FFF	8KB	System Control	Secure Subsystem Watchdog				
36	0x5008_3000	0x5008_3FFF	4KB	System Control	SRAM Memory Protection Control				
37	0x5008_4000	0x5008_7FFF	16KB	Reserved	Reserved				
38	0x5008_8000	0x5008_BFFF	16KB	System Control	Reserved				
39	0x5008_C000	0x500E_FFFF	400KB	Reserved	Reserved				
40	0x500F_0000	0x500F_FFFF	64KB	Reserved	Reserved				
41	0x5010_0000	0x5FFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface				

42	0x6000_0000	0x6FFF_FFFF	256MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	NS	6	0
43	0x7000_0000	0x7FFF_FFFF	256MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	S	7	0
44	0x8000_0000	0x8FFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	NS	8	0
45	0x9000_0000	0x9FFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	S	9	0
46	0xA000_0000	0xAFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	NS	A	0
47	0xB000_0000	0xBFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	S	B	0
48	0xC000_0000	0xCFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	NS	C	0
49	0xD000_0000	0xDFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	S	D	0
50	0xE000_0000	0xE003_FFFF	256KB	PPB	Private Peripheral Bus. Local to CPU			
51	0xE004_0000	0xE004_0FFF	4KB	System Debug	M23 TPIU			
52	0xE004_1000	0xE004_1FFF	4KB	System Debug	M23 ETM			
53	0xE004_2000	0xE004_2FFF	4KB	System Debug	M23 CTI	Exempt		
54	0xE004_3000	0xE00F_DFFF	748KB	Reserved	Reserved			
55	0xE00F_E000	0xE00F_EFFF	4KB	System Debug	MCU Debug ROM			
56	0xE00F_F000	0xE00F_FFFF	4KB	System Debug	M23 Debug ROM			
57	0xE010_0000	0xEFFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	NS	E	0
58	0xF000_0000	0xF00F_FFFF	1MB	System Debug	System Debug Region – System Debug ROM, CTI & TSCLKGEN.	Exempt		
59	0xF010_0000	0xFFFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	S	F	0

Table 3-1 : Memory map overview

3.4.1 External ZBT SRAMs Synchronous SRAM for Code (SSRAM1)

4MB of ZBT memory is available in the code region of the memory map. The memory is named SSRAM1 and is mapped both to the Non-secure and secure code memory region as shown in Table 3-2. To provide security gating, there is an MPC in the SSE-123 Integration.

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	**0x0000_0000**	**0x003F_FFFF**	**4MB**	Code Memory	**ZBT SRAM (SSRAM1)**	5	NS	0	0
2	**0x0040_0000**	**0x007F_FFFF**	**4MB**		**SSRAM1 alias**	6			
3	0x0080_0000	0x0DFF_FFFF	116MB		Not used. Returns Bus Errors when accessed.	-			
4	0x0E00_0000	0x0FFF_FFFF	32MB	Reserved	Reserved	8			
5	**0x1000_0000**	**0x103F_FFFF**	**4MB**	Code Memory	**ZBT SRAM (SSRAM1)**	1	S	1	CODE NSC
6	**0x1040_0000**	**0x107F_FFFF**	**4MB**		**SSRAM1 alias**	2			
7	0x1080_0000	0x1DFF_FFFF	116MB		Not used. Returns Bus Errors when accessed.	-			
8	0x1E00_0000	0x1FFF_FFFF	32MB	Reserved	Reserved	4			

Table 3-2 : External SSRAM1 mapping to Code Memory

Because 4MB of memory exists in an 8MB window, the top 4MB of that window is aliased with the lower 4MB. As a result, both will share the same security setting. This ensures that there are no security holes that allow secure and non-secure access to the same physical location on the ZBT SSRAM at the same time.

3.4.2 External ZBT SRAMs Synchronous SRAM (SSRAM2 and SSRAM3)

4MB of ZBT memory is available in the expansion 0 region of the memory map. The memory is formed by the combination of memories SSRAM2 and SSRAM3. All unused regions shown in the table return bus error responses when accessed.

ROW ID	Address		Size	Region Name	Description	Alias With Row ID	IDAU Region Values		
	From	To					Security	IDAUID	NSC
1	**0x2800_0000**	**0x281F_FFFF**	**2MB**		**ZBT SRAM (SSRAM2)**	4			
2	**0x2820_0000**	**0x283F_FFFF**	**2MB**	Expansion 0	**ZBT SRAM (SSRAM3)**	5			
3	0x2840_0000	0x2FFF_FFFF	124MB		Not used. Returns Bus Errors when accessed.				
4	**0x3800_0000**	**0x381F_FFFF**	**2MB**		**ZBT SRAM (SSRAM2)**	1			
5	**0x3820_0000**	**0x383F_FFFF**	**2MB**	Expansion 0	**ZBT SRAM (SSRAM3)**	2			
6	0x3840_0000	0x3FFF_FFFF	124MB		Maps to AHB5 Master Expansion 0 Interface				

Table 3-3 : SSRAM2 and SSRAM3 address mapping

An Exclusive Access Monitor and a Memory Protection Controller exist on the path of each ZBT SRAM. They support exclusive access and security gating so that blocks of aliased memory can be assigned individually to Secure or Non-secure regions. The two MPCs are as follows:

- SSRAM2MPC is the MPC for SSRAM2. Its APB interface is mapped to address 0x5800_8000 and its interrupt signal is connected to S_MPCEXP_STATUS[1].
- SSRAM3MPC is the MPC for SSRAM3. Its APB interface is mapped to address 0x5800_9000 and its interrupt signal is connected to S_MPCEXP_STATUS[2].

Both SSRAM1MPC and SSRAM2MPC have the same configuration settings as listed in Table 3-4.

Parameter	Configuration	Description
DATA_WIDTH	32bits	Data Width: 32bits
ADDR_WIDTH	22	Address Width. Set at 22bits to support 4 Mbyte of memory space.
MASTER_WIDTH	5	HMASTER signal width. 5-bit for 32 masters
USER_WIDTH	0	User signal width parameter, default: 1, ports tied if 0
BLK_SIZE	11	Block size: (1 << BLK_SIZE) bytes, min. value: 5, max. value: 20. Set at 8 for 256 byte blocks.
GATE_RESP	0	Response on data AHB when accessed during programming lock: 0 – Add wait states until lock is released (default) 1 – Drive bus error

Table 3-4 : SSRAM2MPC and SSRAM3MPC Configuration settings.

PSRAM

The MPS2+ FPGA prototyping board provides a 16-bit PSRAM interface supporting two banks of Parallel SRAMs each up to 8MB, totaling 16MB of SRAM. These memories are currently mapped only to non-secure SRAM space as follows:

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	0x8000_0000	0x80FF_FFFF	16MB	AHB Master Expansion 1 Interface Area	PSRAM		NS	8	0
2	0x8100_0001	0x8FFF_FFFF	246MB		Not used. Returns Bus Errors when accessed.				

Table 3-5 : External PSRAM mapping to Code Memory

3.4.4 **Expansion System peripherals**

Other than the SSRAMs, PSRAMs and the Ethernet MAC and PHY, all FPGA peripherals that are extensions to the SSE-123 Integration are mapped into two key areas of the memory map:

- 0x4010_0000 to 0x4FFF_FFFF Non-Secure region which maps to AHB Master Expansion 1 interface.

- 0x5010_0000 to 0x5FFF_FFFF Secure region which maps to AHB Master Expansion 1 interface.

Table 3-6 : FPGA Expansion Peripheral Map shows how these peripherals are mapped.

To support TrustZone-Armv8-M and allow Software to map these peripherals to secure or non-secure address space, many peripherals are mapped twice and either APB PPC or AHB PPC is then used to gate access to these peripherals. An FPGA Secure Privilege Control block and a non-secure Privilege Control block then provide controls to these PPC.

For expansion AHB Masters within the system, there is a Master Security Controller (MSC) added to each master with an associated IDAU. Masters that have IDAU are:

- PL081 DMA Engine. All DMAs can be mapped as Secure or Non-Secure Masters. The intention is to support the use-case where for each pair of DMAs that shared a single AHB expansion interface, one is mapped as a secure and another is mapped as non-secure.

ROW ID	Address From	To	Size	Description	Alias With Row ID	IDAU Region Values Security	ID
1	0x4010_0000	0x4010_0FFF	4K	GPIO 0	40		
2	0x4010_1000	0x4010_1FFF	4K	GPIO 1	41		
3	0x4010_2000	0x4010_2FFF	4K	GPIO 2	42		
4	0x4010_3000	0x4010_3FFF	4K	GPIO 3	43		
5	0x4010_4000	0x4010_FFFF		Not used. Returns Bus Errors when accessed.		NS	4
6	0x4011_0000	0x4011_0FFF	4K	DMA 0	45		
7	0x4011_1000	0x4011_1FFF	4K	DMA 1	46		
8	0x4011_2000	0x4011_2FFF	4K	Reserved	47		
9	0x4011_3000	0x4011_3FFF	4K	Reserved	48		

ROW ID	Address From	To	Size	Description	Alias With Row ID	Security	ID
10	0x4011_4000	0x401F_FFFF		Not used. Returns Bus Errors when accessed.			
11	0x4020_0000	0x4020_0FFF	4K	UART 0 – J20	50		
12	0x4020_1000	0x4020_1FFF	4K	UART 1 - XBEE	51		
13	0x4020_2000	0x4020_2FFF	4K	UART 2 - Reserved	52		
14	0x4020_3000	0x4020_3FFF	4K	UART 3 - Shield 0	53		
15	0x4020_4000	0x4020_4FFF	4K	UART 4 - Shield 1	54		
16	0x4020_5000	0x4020_5FFF	4K	FPGA - PL022 (SPI – J21)	55		
17	0x4020_6000	0x4020_6FFF	4K	FPGA - PL022 (SPI for LCD)	56		
18	0x4020_7000	0x4020_7FFF	4K	FPGA - SBCon I2C (Touch)	57		
19	0x4020_8000	0x4020_8FFF	4K	FPGA - SBCon I2C (Audio Conf)	58		
20	0x4020_9000	0x4020_9FFF	4K	FPGA - PL022 (SPI ADC)	59		
21	0x4020_A000	0x4020_AFFF	4K	FPGA - PL022 (SPI Shield0)	60		
22	0x4020_B000	0x4020_BFFF	4K	FPGA - PL022 (SPI Shield1)	61		
23	0x4020_C000	0x4020_CFFF	4K	SBCon (I^2C - Shield0)	62		
24	0x4020_D000	0x4020_DFFF	4K	SBCon (I^2C - Shield1)	63		
25	0x4020_E000	0x402F_FFFF		Not used. Returns Bus Errors when accessed.			
26	0x4030_0000	0x4030_0FFF	4K	FPGA - SCC registers	65		
27	0x4030_1000	0x4030_1FFF	4K	FPGA - I2S (Audio)	66		
28	0x4030_2000	0x4030_2FFF	4K	FPGA - IO (System Ctrl + I/O)	67		
29	0x4030_3000	0x40FF_FFFF		Not used. Returns Bus Errors when accessed.			
30	0x4100_0000	0x4100_FFFF	64K	VGA Console	69		
31	0x4110_0000	0x4113_FFFF	256K	VGA Image	70		
32	0x4114_0000	0x41FF_FFFF		Not used. Returns Bus Errors when accessed.			
33	0x4200_0000	0x420F_FFFF	1M	Ethernet	72		
34	0x4210_0000	0x4800_6FFF		Not used. Returns Bus Errors when accessed.			
35	0x4800_7000	0x4800_7FFF	4K	FPGA Non-Secure Privilege Control			
36	0x4800_8000	0x4810_3FFF		Not used. Returns Bus Errors when accessed.			
37	0x4810_4000	0x4810_4FFF	4K	System Counter Read.	80		
38	0x4810_5000	0x481F_FFFF	1004K	Reserved.			
39	0x4820_0000	0x4FFF_FFFF		Not used. Returns Bus Errors when accessed.			
40	0x5010_0000	0x5010_0FFF	4K	GPIO 0	1		
41	0x5010_1000	0x5010_1FFF	4K	GPIO 1	2		
42	0x5010_2000	0x5010_2FFF	4K	GPIO 2	3		
43	0x5010_3000	0x5010_3FFF	4K	GPIO 3	4		
44	0x5010_4000	0x5010_FFFF		Not used. Returns Bus Errors when accessed.		S	5
45	0x5011_0000	0x5011_0FFF	4K	DMA 0	6		
46	0x5011_1000	0x5011_1FFF	4K	DMA 1	7		
47	0x5011_2000	0x5011_2FFF	4K	Reserved	8		
48	0x5011_3000	0x5011_3FFF	4K	Reserved	9		

ROW ID	Address From	To	Size	Description	Alias With Row ID	IDAU Region Values Security ID
49	0x5011_4000	0x501F_FFFF		Not used. Returns Bus Errors when accessed.		
50	0x5020_0000	0x5020_0FFF	4K	UART 0 – J20	11	
51	0x5020_1000	0x5020_1FFF	4K	UART 1 - XBEE	12	
52	0x5020_2000	0x5020_2FFF	4K	UART 2 - Reserved	13	
53	0x5020_3000	0x5020_3FFF	4K	UART 3 - Shield 0	14	
54	0x5020_4000	0x5020_4FFF	4K	UART 4 - Shield 1	15	
55	0x5020_5000	0x5020_5FFF	4K	FPGA - PL022 (SPI)	16	
56	0x5020_6000	0x5020_6FFF	4K	FPGA - PL022 (SPI for LCD)	17	
57	0x5020_7000	0x5020_7FFF	4K	FPGA - SBCon I2C (Touch)	18	
58	0x5020_8000	0x5020_8FFF	4K	FPGA - SBCon I2C (Audio Conf)	19	
59	0x5020_9000	0x5020_9FFF	4K	FPGA - PL022 (SPI ADC)	20	
60	0x5020_A000	0x5020_AFFF	4K	FPGA - PL022 (SPI Shield0)	21	
61	0x5020_B000	0x5020_BFFF	4K	FPGA - PL022 (SPI Shield1)	22	
62	0x5020_C000	0x5020_CFFF	4K	SBCon (Shield0)	23	
63	0x5020_D000	0x5020_DFFF	4K	SBCon (Shield1)	24	
64	0x5020_E000	0x502F_FFFF		Not used. Returns Bus Errors when accessed.		
65	0x5030_0000	0x5030_0FFF	4K	FPGA - SCC registers	26	
66	0x5030_1000	0x5030_1FFF	4K	FPGA - I2S (Audio)	27	
67	0x5030_2000	0x5030_2FFF	4K	FPGA - IO (System Ctrl + I/O)	28	
68	0x5030_3000	0x50FF_FFFF		Not used. Returns Bus Errors when accessed.		
69	0x5100_0000	0x5100_FFFF	64K	VGA Console	30	
70	0x5110_0000	0x5113_FFFF	256K	VGA Image	31	
71	0x5114_0000	0x51FF_FFFF		Not used. Returns Bus Errors when accessed.		
72	0x5200_0000	0x520F_FFFF	1M	Ethernet	33	
73	0x5210_0000	0x5800_6FFF		Not used. Returns Bus Errors when accessed.		
74	0x5800_7000	0x5800_7FFF	4K	Reserved		
75	0x5800_8000	0x5800_8FFF	4K	SSRAM2 Memory Protection Controller (MPC)		
76	0x5800_9000	0x5800_9FFF	4K	SSRAM3 Memory Protection Controller (MPC)		
77	0x5800_A000	0x580F_FFFF		Not used. Returns Bus Errors when accessed.		
78	0x5810_0000	0x5810_0FFF	4K	Code Expansion MPC		
79	0x5810_1000	0x5810_3FFF	12K	Reserved		
80	0x5810_4000	0x5810_4FFF	4K	System Counter Read.	37	
81	0x5810_5000	0x5810_5FFF	4K	System Counter Control		
82	0x5810_6000	0x581F_FFFF	1000K	Reserved.		
83	0x5820_0000	0x5FFF_FFFF		Not used. Returns Bus Errors when accessed.		

Table 3-6 : FPGA Expansion Peripheral Map

4 Programmers Model

4.1 CMSDK, SSE-123 Integration and SIE-200 components

This programmer's model is supplemental to the CMSDK, SSE-123 Integration, and SIE-200 documentation, which covers many of the included components in more detail. Figure 3-1 : System Overview shows the connectivity of the system.

4.2 External ZBT Synchronous SRAM (SSRAM1)

SSRAM1 is ZBT RAM in the CODE region. This is interfaced to two external 32-bit ZBT SSRAM devices in parallel, forming a 64-bit ZBT SSRAM. 8MB of memory space is allocated, but only 4MB is used (each ZBT SSRAM is 2MB).

4.3 External ZBT Synchronous SRAM (SSRAM2 & SSRAM3)

The ZBT SSRAM is set up as two external ZBT SSRAMs, connected to two independent ZBT interfaces. 8MB of memory space is allocated, but only 4MB is used (each ZBT SSRAM is 2MB).

Note: SSRAM2 and SSRAM3 are in the SRAM region. Running code from SRAM region is slower than from CODE region because the internal bus structure is not optimized for running programs from this region.

4.4 External PSRAM

A 16MB 16-bit PSRAM area is available and the memory map allocates the address range 0x8000_0000 - 0x80FF_FFFF. This enables large test programs to be used, for example *uClinux*, in the External RAM region of the Cortex-M memory space.

Note: PSRAM is in the SRAM region. Running code from SRAM region is slower than from CODE region because the internal bus structure is not optimized for running programs from this region.

4.5 AHB GPIO

The SMM uses four CMSDK AHB GPIO blocks, each providing 16 bits of IO. These are connected to the EXP port as follows.

EXP Port	GPIO
EXP[15:0]	GPIO0[15:0]
EXP[31:16]	GPIO1[31:16]
EXP[47:32]	GPIO2[47:32]
EXP[51:48]	GPIO3[51:48]
EXP[63:49]	Not used. Read as 0.

Table 4-1 : GPIO Mapping

The GPIO alternative function lines select if peripherals or GPIOs are available for each pin. See section 9 - Shield Support for mappings.

4.6 SPI (Serial Peripheral Interface)

The SMM implements five PL022 SPI modules:

- One general-purpose SPI module that connects to the general-purpose SPI connector, J21.

- Three general-purpose SPI modules that connect to the Expansion headers J7 and J8. Intended for use with the V2C-Shield1 which provide an interface with the ADC and provide SPI on the headers. These are alt-functions on the EXP ports. See section 9 - Shield Support for mappings.

- One Color LCD module control.

The Self-test program provided with the MPS2+ includes example code for the color LCD module control interface.

The SPI ports connected to J21 can be configured as a master or a slave. The chip select line is configured as an input in slave mode to be used as frame/slave select.

Chip Selects are controlled by SCC register `fpga_misc` rather than the PL022 chip select output. See *Table 4-4 : System Control and I/O Memory* Map for more details.

4.7 SBCon (I²C)

The SMM implements four SBCon serial modules:

- One SBCon module for use by the Color LCD touch interface.

- One SBCon module to configure the audio controller.

- Two general purpose SBCon modules, that connect to the Expansion headers J7 and J8, are intended for use with the V2C-Shield1 which provide an I²C interface on the headers. See section 9 - Shield Support for mappings.

  The Self-test program provided with the MPS2+ includes example code for the color LCD module control and Audio interfaces.

4.8 UART

The SMM implements five CMSDK UARTs:

- UART 0 – J20.

- UART 1 – XBEE on shield adaptor board.

- UART 2 – Reserved.

- UART 3 - Shield 0 on shield adaptor board.

- UART 4 - Shield 1 on shield adaptor board.

UART 1, 3 and 4 are alt-functions on the EXP ports. See section 9 - Shield Support for mappings.

4.9 Color LCD serial interface

The color LCD module has two interfaces:

- SPI for sending image data to the LCD.

- I^{2}C to transfer data input from the touch screen.

These interfaces are connected to a STMicroelectronics STMPE811QTR Port Expander with Advanced Touch Screen Controller on the Keil MCBSTM32C display board (schematic listed in the reference section). The Keil display board contains an AM240320LG display panel and uses a Himax HX8347-D LCD controller. The display panel jumpers, J0-J3 are configured as "0010" selecting the SPI MPU mode.

Self-test provided with the MPS2+ includes example code for both interfaces.

4.10 Ethernet

The SMM design connects to an SMSC LAN9220 device through a static memory interface.

The self-test program includes example code for a simple loopback operation.

4.11 VGA

The VGA output is split into two areas as below:

Output Type	Address From	To	Description
Console text area	0x4100_0000	0x4100_FFFF	Writes ASCII characters to the current location of the cursor.
	0x5100_0000	0x5100_FFFF	
Graphical image area	0x4110_0000	0x4113_FFFF	512x128 image area at the bottom of the screen. 0x4110_0000 is the top left of the area and 0x4113_FFFF is the bottom right. HADDR[16:2] = YYYYYYYXXXXXXXX where X and Y are the horizontal and vertical pixel offset respectively.
	0x5110_0000	0x5113_FFFF	

Table 4-2 : VGA Memory Map

Console text area:

The console text area displays ASCII characters. The cursor moves when a character is written. Standard ASCII control codes 0x8 for backspace, 0xA and 0xD for newline are supported, but no other control codes are implemented. The cursor wraps at end of line and can't be moved

arbitrarily, only as described above. The characters are 16 pixels tall x 8 pixels wide. The text scrolls when the bottom is reached. The text area is 80 characters wide * 21 characters tall.

Graphical image area:

To write to the graphical image output, each pixel requires one 32-bit word, therefore, a total of 256KB are needed. The values in the data buffer are packed as 4 bits per channel in the format 0x00000RGB. The pixel in the top left-hand corner of the display occupies address 0x4110_0000 with each successive row using an offset of 0x0000_0400 from the previous row. For example, the leftmost pixel (LMP) of the 2nd row is at 0x4110_0400 and the LMP of the 3rd row is at 0x4110_0800.

4.12 Audio I²S

A simple FIFO interface generates and receives I²S audio.

Address	Name	Information
0x4030_1000 0x5030_1000	CONTROL	Control Register [31:18] : Reserved [17] : Audio CODEC reset control (output pin) [16] : FIFO reset [15] : Reserved [14:12] : RX Buffer IRQ Water Level - Default 2 (IRQ triggers when less than 2 word spaces available) [11] : Reserved [10: 8] : TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than 2 word spaces available) [7: 4] : Reserved [3] : RX Interrupt Enable [2] : RX Enable [1] : TX Interrupt Enable [0] : TX Enable
0x4030_1004 0x5030_1004	STATUS	Status register [31:6] : Reserved [5] : RX Buffer Full [4] : RX Buffer Empty [3] : TX Buffer Full [2] : TX Buffer Empty [1] : RX Buffer Alert (Depends on Water level) [0] : TX Buffer Alert (Depends on Water level)
0x4030_1008 0x5030_1008	ERROR	Error status register [31:2] : Reserved [1] : RX overrun - write 1 to clear [0] : TX overrun/underrun - write 1 to clear

Address	Name	Information
0x4030_100C 0x5030_100C	DIVIDE	Divide ratio register (for Left/Right clock) [31:10] : Reserved [9: 0] LRDIV (Left/Right) Default = 0x80 12.288MHz / 48KHz / 2 (L+R) = 128
0x4030_1010 0x5030_1010	TXBUF	Transmit Buffer FIFO Data Register (WO) [31:16] : Left Channel [15: 0] : Right Channel
0x4030_1014 0x5030_1014	RXBUF	Receive Buffer FIFO Data Register (RO) [31:16] Left Channel [15: 0] Right Channel
0x4030_1018 – 0x4030_12FC 0x5030_1018 – 0x5030_12FC	RESERVED	-
0x4030_1300 0x5030_1300	ITCR	Integration Test Control Register [31:1] : Reserved [0] : ITCR
0x4030_1304 0x5030_1304	ITIP1	Integration Test Input Register 1 [31:1] : Reserved [0] : SDIN
0x4030_1308 0x5030_1308	ITOP1	Integration Test Output Register 1 [31:4] : Reserved [3] : IRQOUT [2] : LRCK [1] : SCLK [0] : SDOUT

Table 4-3 : Audio I^{2}S Memory Map

4.13 Audio Configuration

The SMM implements a simple SBCon interface based on I^{2}C. It is used to configure the Cirrus Logic Low Power Codec with Class D Speaker Driver, CS42L52 part on the MPS2+ board.

4.14 FPGA system control and I/O

The SMM implements an FPGA system control block.

Address	Name	Information
0x4030_2000 0x5030_2000	FPGAIO->LED0	LED connections [31:2] : Reserved [1:0] : LED R/W Default reset value : 0x0000_0000
0x4030_2004 0x5030_2004	RESERVED	
0x4030_2008 0x5030_2008	FPGAIO->BUTTON	Buttons [31:2] : Reserved [1:0] : Buttons R/W Default reset value : 0x0000_0000
0x4030_200C 0x5030_200C	RESERVED	
0x4030_2010 0x5030_2010	FPGAIO->CLK1HZ	1Hz up counter R/W Default reset value : 0x0000_0000
0x4030_2014 0x5030_2014	FPGAIO->CLK100HZ	100Hz up counter R/W Default reset value : 0x0000_0000
0x4030_2018 0x5030_2018	FPGAIO->COUNTER	Cycle Up Counter, Sourced from MAINCLK. Increments when 32-bit prescale counter equals zero and automatically reloads. FPGAIO->COUNTER wraps around when it reaches its terminal value. R/W Default reset value : 0x0000_0000
0x4030_201C 0x5030_201C	FPGAIO->PRESCALE	Bit[31:0] – reload value for prescale counter. Counts down, and automatically reloads when it reaches zero. R/W Default reset value : 0x0000_0000

Address	Name	Information
0x4030_2020 0x5030_2020	FPGAIO->PSCNTR	32-bit Prescale counter – current value of the pre-scaler counter. The Cycle Up Counter increments when the prescale down counter reaches 0. The pre-scaler counter is reloaded with PRESCALE after reaching 0. Counts down at speed of MAINCLK R/W Default reset value : 0x0000_0000
0x4030_2024 0x5030_2024	RESERVED	
0x4030_204C 0x5030_204C	FPGAIO->MISC	Misc control [31:10] : Reserved [9] : SHIELD1_SPI_nCS [8] : SHIELD0_SPI_nCS [7] : ADC_SPI_nCS [6] : CLCD_BL_CTRL [5] : CLCD_RD [4] : CLCD_RS [3] : CLCD_RESET [2] : RESERVED [1] : SPI_nSS [0] : CLCD_CS R/W Default reset value : 0x1111_1111

Table 4-4 : System Control and I/O Memory Map

4.15 Serial Configuration Controller (SCC)

The SMM implements communication between the microcontroller and the FPGA system through an SCC interface.
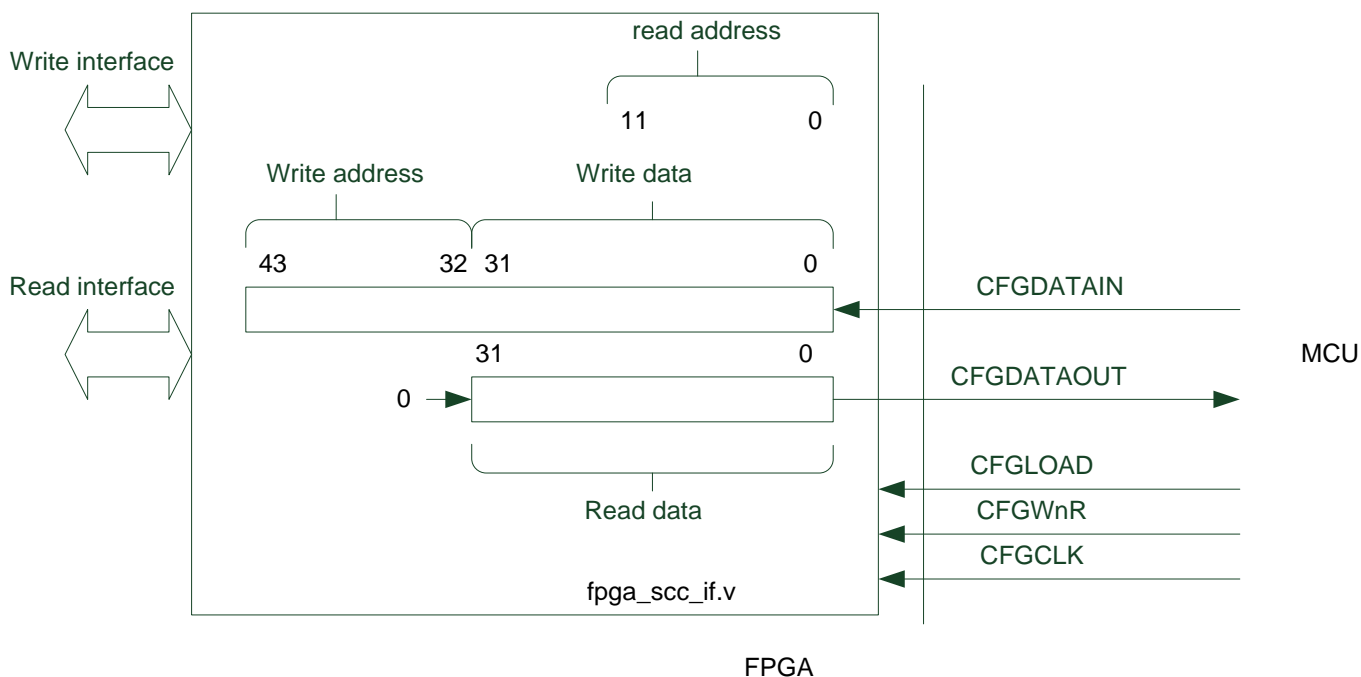
Figure 4-1 : Diagram of the SCC Interface

The read-addresses and write-addresses of the SCC interface do not use bits[1:0].
All address words are word-aligned.

Address	Name	Information
0x000	CFG_REG0	Bits[31:0] - Reserved
0x004	CFG_REG1	Bits [31:8] - Reserved Bits [7:0] - MCC LEDs: 0 = OFF 1 = ON
0x008	CFG_REG2	Reserved
0x00C	CFG_REG3	Bits [31:8] - Reserved Bits [7:0] - MCC switches: 0 = OFF 1 = ON
0x010	CFG_REG4	Bits [31:4] - Reserved Bits [3:0] - Board Revision
0x014	RESERVED	-
0x018	RESERVED	-
0x01C	RESERVED	-
0x020 – 0x09C	RESERVED	-
0x0A0	SYS_CFGDATA_RTN	32bit DATA [r/w]
0x0A4	SYS_CFGDATA_OUT	32bit DATA [r/w]

Address	Name	Information
0x0A8	SYS_CFGCTRL	Bit[31] - Start (generates interrupt on write to this bit)
		Bit[30] - R/W access
		Bits[29:26] - Reserved
		Bits[25:20] - Function value
		Bits[19:12] - Reserved
		Bits[11:0] - Device (value of 0/1/2 for supported clocks)
0x0AC	SYS_CFGSTAT	Bits[31:2] - Reserved
		Bit[1] - Error
		Bit[0] - Complete
0x0AD – 0x0FC	RESERVED	-
0x100	SCC_DLL	DLL lock register
		Bits [31:24] - DLL LOCK MASK[7:0] - These bits indicate if the DLL locked is masked.
		Bits [23:16] - DLL LOCK MASK[7:0] - These bits indicate if the DLLs are locked or unlocked
		Bits [15:1] - Reserved
		Bit[0] - This bit indicates if all enabled DLLs are locked
0x104 – 0xFF4	RESERVED	-
0xFF8	SCC_AID	SCC AID register is read only
		Bits[31:24] - FPGA build number
		Bits[23:20] - MPS2+ target board revision
		(A = 0, B = 1, C = 2)
		Bits[19:8] - Reserved
		Bits[7:0] - Number of SCC configuration register
0xFFC	SCC_ID	SCC ID register is read only
		Bits[31:24] - Implementer ID: 0x41 = Arm
		Bits[23:20] - Reserved
		Bits[19:16] - IP Architecture: 0x4 =AHB
		Bits[15:4] - Primary part number: 539 = AN539
		Bits[3:0] - Reserved

Table 4-5 : SCC Register memory map

5 Clock architecture

The following tables list clocks entering and generated by the SMM.

5.1 Clocks

5.1.1 Source clocks

The following clocks are inputs to the system.

Clock	Input Pin	Frequency	Note
OSC0	OSCCLK[0]	40MHz	Core clock (x2)
OSC1	OSCCLK[1]	24.58MHz	Reference clock
OSC2	OSCCLK[2]	25MHz	Peripheral clock
DBGCLK	CS_TCK	Set by debugger	JTAG input
CFGCLK	CLCD_PDH[13]	Set by MCC	SCC register clock from MCC
SPICFGCLK	CLCD_PDL[6]	Set by MCC	SPI clock for memory access

Table 5-1 : Source clocks

5.1.2 Internal clocks

The following clocks are generated internally from the source clocks.

Clock	Source	Frequency	Note
MAINCLK	OSC0	20MHz	
AUDMCLK	OSC1	12.29MHz	
AUDSCLK	OSC1	3.07MHz	
DBGCLK	OSC0	20MHz	
SPICLCD	OSC2	25MHz	
SPICON	OSC2	25MHz	
I2CCLCD	OSC2	25MHz	
I2CAUD	OSC2	25MHz	
S32KCLK	OSC1	32kHz	
clk_100hz	OSC1	100Hz	
clk_zbtout	OSC0	20MHz	Phase shifted MAINCLK
traceclk	OSC0	20MHz	

Table 5-2 : Generated internal clocks

5.1.3 Clock outputs

The following clocks are generated internally and are output from the FPGA.

Clock	Output Port	Frequency	Note
spiclcd	CLCD_T_SCK	kHz	Software Configured
spicon	SPI_SCK	kHz	Software Configured
i2cclcd	CLCD_T_SCL	kHz	Software Generated
i2caud	AUD_SCL	kHz	Software Generated
i2c_shield0	EXP[5]	kHz	Software Generated
i2c_shield1	EXP[31]	kHz	Software Generated
spi_shield0	EXP[11]	kHz	Software Configured
spi_shield1	EXP[44]	kHz	Software Configured
spi_adc	EXP[19]	kHz	Software Configured
traceclk	CS_TRACECLK	20MHz	
clk_zbtout	SSRAM1_CLK[0]	20MHz	
clk_zbtout	SSRAM1_CLK[1]	20MHz	
clk_zbtout	SSRAM2_CLK	20MHz	
clk_zbtout	SSRAM3_CLK	20MHz	

Table 5-3 : Generated external clocks

5.1.4 Clocks connecting to the SSE-123 Integration

The following clocks connect to the SSE-123 Integration. This includes both clocks provided to the SSE-123 Integration and clocks generated by it.

Full details of each of these clocks is given in the *Arm® SSE-123 Example Subsystem Configuration and Integration Manual*

SIE-123 Clock	Driven by / Driving	Source	Frequency	Note
FASTCLK	MAINCLK	Wrapper	20MHz	Main Clock Input
HCLK	SYSCLK	SIE-123	20MHz	Main System Clock
REFCLK	S32KCLK	Wrapper	32kHz	Asynchronous 32KHz clock input
SWCLKTCK	DBGCLK	Wrapper	20MHz	SW/JTAG DP clock
TRACECLKIN	traceclk	Wrapper	20MHz	TPIU trace port clock input

Table 5-4 : SSE-123 Integration clocks

6 FPGA Secure Privilege Control

The SSE-123 Integration's Secure Privilege Control and Non-secure Privilege Block provide expansion security control signals that control the various security gating units within the subsystem. The following table lists the connectivity of system security extension signal. More details are available in *Arm® SSE-123 Example Subsystem Technical Reference Manual.*

Components Name	Components signals	Security Expansion Signals
DMA 0 MSC	msc_irq	S_MSCEXP_STATUS[0]
	msc_irq_clear	S_MSCEXP_CLEAR[0]
	cfg_nonsec	NS_MSCEXP[0]
DMA 1 MSC	msc_irq	S_MSCEXP_STATUS[1]
	msc_irq_clear	S_MSCEXP_CLEAR[1]
	cfg_nonsec	NS_MSCEXP[1]
Reserved	msc_irq	S_MSCEXP_STATUS[2]
	msc_irq_clear	S_MSCEXP_CLEAR[2]
	cfg_nonsec	NS_MSCEXP[2
Reserved	msc_irq	S_MSCEXP_STATUS[3]
	msc_irq_clear	S_MSCEXP_CLEAR[3]
	cfg_nonsec	NS_MSCEXP[3]
APB PPC EXP 1	apb_ppc_irq	S_APBPPCEXP_STATUS[1]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[1]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP1[15:0]
	cfg_ap	APB_P_PPCEXP1[15:0]
APB PPC EXP 2	apb_ppc_irq	S_APBPPCEXP_STATUS[2]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[2]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP2[15:0]
	cfg_ap	APB_P_PPCEXP2[15:0]
APB PPC EXP 3	apb_ppc_irq	S_APBPPCEXP_STATUS[3]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[3]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP3[15:0]
	cfg_ap	APB_P_PPCEXP3[15:0]
AHB PPC EXP	ahb_ppc_irq	S_AHBPPCEXP_STATUS[0]
	ahb_ppc_clear	S_AHBPPCEXP_CLEAR[0]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	AHB_NS_PPCEXP[15:0]
	chg_ap	AHB_P_PPCEXP[15:0]

Components Name	Components signals	Security Expansion Signals
Reserved		S_MPCEXP_STATUS[0]
MPC SSRAM1	secure_error_irq	S_MPCEXP_STATUS[1]
MPC SSRAM2	secure_error_irq	S_MPCEXP_STATUS[2]

Table 6-1 : Security Expansion signals connectivity.

The following table lists the peripherals that are controlled by APB PPC EXP 1. Each APB <n> interface is controlled by APB_NS_PPCEXP1[n] and APB_P_PPCEXP1[n].

APB PPC EXP 1 Interface Number <n>	Name
0	Reserved
1	SSRAM2 Memory Protection Controller (MPC)
2	SSRAM3 Memory Protection Controller (MPC)
15:3	Reserved

Table 6-2 : Peripherals Mapping of APB PPC EXP 1

The following table lists the peripherals that are controlled by APB PPC EXP 2. Each APB <n> interface is controlled by APB_NS_PPCEXP2[n] and APB_P_PPCEXP2[n].

APB PPC EXP 2 Interface Number <n>	Name
0	SPI_0
1	SPI_1
2	SPI_2
3	SPI_3
4	SPI_4
5	UART_0
6	UART_1
7	UART_2
8	UART_3
9	UART_4
10	I2C_0
11	I2C_1
12	I2C_2
13	I2C_3
15:14	Reserved

Table 6-3 : Peripherals Mapping of APB PPC EXP 2

The following table lists the peripherals that are controlled by APB PPC EXP 3. Each APB <n> interface is controlled by APB_NS_PPCEXP3[n] and APB_P_PPCEXP3[n].

APB PPC EXP 3 Interface Number <n>	Name
0	SCC
1	AUDIO
2	FPGAIO
15:3	Reserved

Table 6-4 : Peripherals Mapping of APB PPC EXP 3

The following table lists the peripherals that are controlled by AHB PPC EXP. Each AHB <n> interface is controlled by AHB_NS_PPCEXP[n] and AHB_P_PPCEXP[n].

AHB PPC EXP Interface Number <n>	Name
0	VGA
1	GPIO_0
2	GPIO_1
3	GPIO_2
4	GPIO_3
5	PSRAM / ETHERNET
7:6	Reserved
8	DMA_0
9	DMA_1
15:10	Reserved

Table 6-5 : Peripherals Mapping of AHB PPC EXP

The following table lists the Master Security Controllers (MSCs) that are controlled by NS_MSCEXP signals. These control signals are used to map each peripheral connected to their associated MSCs as Secure or Non-Secure Masters.

NS_MSCEXP bits	Name
0	MSC cfg_nonsec for DMA0
1	MSC cfg_nonsec for DMA1
15:2	Reserved

Table 6-6 : Peripherals Mapping of AHB PPC EXP1

7 Interrupt Map

The Interrupts in the FPGA subsystem extend the SSE-123 Integration Interrupt map by adding to the expansion area as follows:

Interrupt Input	Interrupt Source
NMI	Combined Secure Watchdog and NMI_Expansion
IRQ[0]	Non-Secure Watchdog Reset Request
IRQ[1]	Non-Secure Watchdog Interrupt
IRQ[2]	Reserved
IRQ[3]	Integration System Timer 0
IRQ[4]	Integration System Timer 1
IRQ[5]	Reserved
IRQ[6]	CTI IRQ request 0
IRQ[7]	CTI IRQ request 1
IRQ[8]	Reserved
IRQ[9]	MPC Combined (Secure)
IRQ[10]	PPC Combined (Secure)
IRQ[11]	MSC Combined (Secure)
IRQ[12]	Bridge Error Combined Interrupt (Secure)
IRQ[13:14]	Reserved
IRQ[15]	PD_SYS PPU
IRQ[31:16]	Reserved by configuration of SSE-123 Integration
IRQ[32]	UART 0 Receive Interrupt
IRQ[33]	UART 0 Transmit Interrupt
IRQ[34]	UART 1 Receive Interrupt
IRQ[35]	UART 1 Transmit Interrupt
IRQ[36]	UART 2 Receive Interrupt
IRQ[37]	UART 2 Transmit Interrupt
IRQ[38]	UART 3 Receive Interrupt
IRQ[39]	UART 3 Transmit Interrupt
IRQ[40]	UART 4 Receive Interrupt
IRQ[41]	UART 4 Transmit Interrupt
IRQ[42]	UART 0 Combined Interrupt
IRQ[43]	UART 1 Combined Interrupt
IRQ[44]	UART 2 Combined Interrupt
IRQ[45]	UART 3 Combined Interrupt
IRQ[46]	UART 4 Combined Interrupt
IRQ[47]	UART Overflow (0, 1, 2, 3 & 4)
IRQ[48]	Ethernet
IRQ[49]	Audio I2S
IRQ[50]	Touch Screen

IRQ[51]	SPI #0 (SPI Header)
IRQ[52]	SPI #1 (CLCD)
IRQ[53]	SPI #2 (Shield ADC)
IRQ[54]	SPI #3 (Shield 0 SPI)
IRQ[55]	SPI #4 (Shield 1 SPI)
IRQ[56]	DMA #0 Error Interrupt Request
IRQ[57]	DMA #0 Terminal Count Interrupt Request
IRQ[58]	DMA #0 Combined Interrupt Request
IRQ[59]	DMA #1 Error Interrupt Request
IRQ[60]	DMA #1 Terminal Count Interrupt Request
IRQ[61]	DMA #1 Combined Interrupt Request
IRQ[62]	DMA #2 Error Interrupt Request
IRQ[63]	DMA #2 Terminal Count Interrupt Request
IRQ[64]	DMA #2 Combined Interrupt Request
IRQ[65]	DMA #3 Error Interrupt Request
IRQ[66]	DMA #3 Terminal Count Interrupt Request
IRQ[67]	DMA #3 Combined Interrupt Request
IRQ[68]	GPIO 0 Combined Interrupt
IRQ[69]	GPIO 1 Combined Interrupt
IRQ[70]	GPIO 2 Combined Interrupt
IRQ[71]	GPIO 3 Combined Interrupt
IRQ[87:72]	GPIO 0 individual interrupts
IRQ[103:88]	GPIO 1 individual interrupts
IRQ[119:104]	GPIO 2 individual interrupts
IRQ[123:120]	GPIO 3 individual interrupts

Table 7-1 : FPGA Expansion Interrupt Map.

7.1 UARTS Interrupts

There are five CMSDK UARTs in the system, and each has the following interrupt pins:

- TXINT

- RXINT

- TXOVRINT

- EXOVRINT

- UARTINT

The TXINT, RXINT and UARTINT interrupt signal of each UART drive a single interrupt input of the M23 CPU. In addition, The TXOVERINT and EXOVRINT interrupt signals of all five UARTs, ten signals in all, are logically ORed together to drive IRQ[47].

8 Debug configuration

8.1 Supported debug and trace interfaces

P-JTAG Processor debug is not supported. Use SWD.

8.2 ICache with software breakpoint debug

There is a known issue when using ICache with software breakpoint debug. The debugger software breakpoint assumes system memory coherence behavior, which is not a default feature of an enabled ICache (in an SSE-123 default configuration).

Conditions where this occurs are defined as:

- Debugger does not perform cache maintenance operations
- The requested breakpoint in the cached memory range of ICache
- The address of the requested breakpoint is in writable memory

Implications of the issue on debug:

- The exact implications vary depending on the properties of the debug access used to insert the breakpoint and the cache status at the time of breakpoint insertion.
- The common implications are that a debug session becomes unstable, the inserted breakpoints malfunction and may remain in the code memory after debug session ended.

To work around the known issue, the debugger must either:

- Not use a software breakpoint (on cacheable instructions).
- Use the software breakpoint only when the cache is disabled.
- Ensure invalidation tasks are completed (which can only be applied to the contents of a full cache).

9 Shield Support

This SMM can support up to two external shield devices with the addition of the Arm V2C-SHIELD (HBI-0289) expansion board to the MPS2+ FPGA Prototyping board (V2M-MPS2+). To enable the Shield support, three SPI, three UART and two I^{2}C interfaces are multiplexed with GPIO over the Expansion Headers.
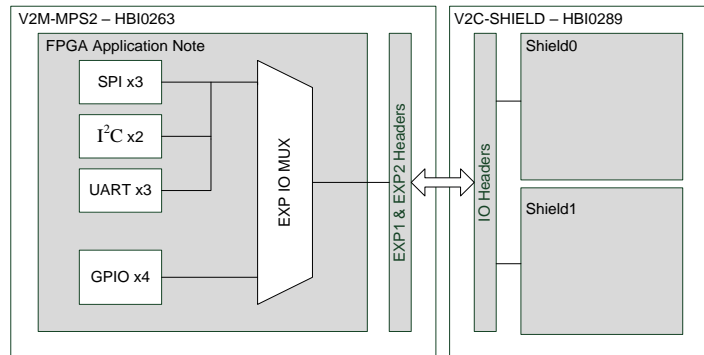

Figure 9-1 : Shield Device Expansion

Multiplexing is controlled by the alternative function output from the associated GPIO Register.

EXP Signal	GPIO Source Port	Alternative Function	Description
EXP[0]	GPIO0 [0]	UART3 RXD	Shield0 UART Receive
EXP[4]	GPIO0 [4]	UART3 TXD	Shield0 UART Transmit
EXP[5]	GPIO0 [5]	SBCON2 SCL	Shield0 I^{2}C Clock
EXP[15]	GPIO0 [15]	SBCON2 SDA	Shield0 I^{2}C Data
EXP[11]	GPIO0 [11]	SPI3 SCK	Shield0 SPI Clock
EXP[12]	GPIO0 [12]	SPI3 SS	Shield0 SPI Chip Select
EXP[13]	GPIO0 [13]	SPI3 MOSI	Shield0 SPI Data Out
EXP[14]	GPIO0 [14]	SPI3 MISO	Shield0 SPI Data In
EXP[26]	GPIO1 [10]	UART4 RXD	Shield1 UART Receive
EXP[30]	GPIO1 [14]	UART4 TXD	Shield1 UART Transmit
EXP[31]	GPIO1 [15]	SBCON3 SCL	Shield1 I^{2}C Clock
EXP[41]	AHB GPIO2 [9]	SBCON3 SDA	Shield1 I^{2}C Data
EXP[38]	AHB GPIO2 [6]	SPI4 SS	Shield1 SPI Chip Select
EXP[39]	AHB GPIO2 7]	SPI4 MOSI	Shield1 SPI Data Out
EXP[40]	AHB GPIO2 [8]	SPI4 MISO	Shield1 SPI Data In
EXP[44]	AHB GPIO2 [12]	SPI4 SCK	Shield1 SPI Clock
EXP[16]	GPIO1 [0]	SPI2 SS	ADC SPI Chip Select
EXP[17]	GPIO1 [1]	SPI2 MISO	ADC SPI Data In
EXP[18]	GPIO1 [2]	SPI2 MOSI	ADC SPI Data Out
EXP[19]	GPIO1 [3]	SPI2 SCK	ADC SPI Clock
EXP[21]	GPIO1 [5]	-	User button 0
EXP[22]	GPIO1 [6]	-	User button 1

Table 9-1 : Shield Alternative Function Pinout

10 Configurations

10.1 SSE-123 Integration and Subsystem

The following options are detailed *Arm® SSE-123 Example Subsystem Configuration and Integration Manual*. These options control the inclusion of presence of components in both the SSE-123 Integration and Subsystem.

Parameter	Implemented Values	Default Values	Description
FLASH_ENABLED	0	0,1	Include Flash Cache and Flash Controller in the Integration layer
IO_PORT_ENABLED	0	0,1	Enable Cortex-M23 single cycle IO port
DEBUG_MODE	2	0,1,2	Define debug functionality

Table 10-1 : SSE-123 Subsystem major configuration options

10.2 SSE-123 Integration

The SSE-123 Integration has several configurable options. For full details of each configuration option, refer to *Arm® SSE-123 Example Subsystem Configuration and Integration Manual*

Parameter	Implemented Values	Default Values	Description
CODEEXP_ADDR_WIDTH	22, (4MB)	13 to 28	Memory size of the code expansion in the Integration layer
CODEEXP_BLK_SIZE	10, (32KB)	0-15	Defines the CODEEXP MPC block size for memory protection
IK_NUMIRQ	16	3-16	Number of Integration layer internal IRQ lines
WAKE_NUMIRQ	92	1-96	Number of Integration layer external IRQ lines

Table 10-2 : SSE-123 Integration configuration options

10.3 SSE-123 Subsystem

The SSE-123 Subsystem is contained within the SSE-123 Integration. It has several configurable options. The specific configuration settings used by this example build are detailed in the table below.

The following options are detailed *Arm® SSE-123 Example Subsystem Configuration and Integration Manual*.

Parameter	Implemented Values	Supported Values	Description
SRAM_ADDR_WIDTH	16 (64KB)	13 to 24	Defines the SRAM size included
SRAM_BLK_SIZE	5 (1KB)	0-15	Defines SRAM MPC block size used for memory protection
EXP_NUMIRQ	108	0-224	Number of expansion IRQ lines. Overridden by Integration layer
EXP_IRQDIS[EXP_NUMIRQ:0]	0x0	0,1 per bit	EXPIRQ line disable mask. Overridden by Integration layer
WICLINES	0x7E	2-242	Number of IRQ lines used as wakeup sources. Overridden by Integration layer
INITVTORNS_RST	0x00000000	Any address [31:8]	Default Non-Secure Vector table offset at reset.
ACC_WAITN_RST	1	0,1	Value of Bus access wait at reset.
MPCEXP_DIS[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the SMPCEXPSTATUS bus. Overridden by Integration layer
MSCEXP_DIS[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the SMSCEXPSTATUS, SMSCEXPCLEAR and NS_MSCEXP buses.
BRGEXP_DIS[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the BRGEXPSTATUS and BRGEXPCLEAR buses
APBPPCEXP_DIS0[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the APBNSPPCEXP and APBPPPCEXP buses. Overridden by Integration layer
APBPPCEXP_DIS1[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the APBNSPPCEXP and APBPPPCEXP buses. Overridden by Integration layer
APBPPCEXP_DIS2[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the APBNSPPCEXP and APBPPPCEXP buses. Overridden by Integration layer
APBPPCEXP_DIS0[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the APBNSPPCEXP and APBPPPCEXP buses. Overridden by Integration layer
AHBPPCEXP_DIS[15:0]	0x0000	0x0000 to 0xFFFF	Disable support for individual bits on the AHBNSPPCEXP and AHBPPPCEXP buses
IRQLATENCY[7:0]	0x15 (minimum)	0x15 to 0xFF	Cortex-M23 supports zero jitter interrupt latency for zero wait-state memory

Table 10-3 : SSE-123 configuration option

10.4 Cortex-M23

Refer to document *Arm® SSE-123 Example Subsystem Technical Reference Manual*, *Processor Configuration Options* for parameters used in SSE-123 Subsystem to configure the Cortex-M23 CPU core.

For the specific configuration settings used by this example build, refer to the tables below.

For full details of each configuration option, refer to *Arm® Cortex™-M23 Processor Integration and Implementation Manual*

Parameter	Implemented Values	Default Values	Description
ACG	YES	YES	Specifies if architectural clock gates are included to minimize dynamic power dissipation
BE	NO	NO	Specifies the endianness for data transfers: NO = Little-endian. YES = Byte-invariant big-endian.
BKPT	4	4	Specifies the number of breakpoint unit comparators implemented.
DBG	YES	YES	Specifies whether the debug extensions are implemented:
HWF	NO	NO	Halfword fetching only:
IOP	NO	NO	Include I/O port functionality
IRQDIS_0	0x00000000	0x00000000	
IRQDIS_1	0x00000000	0x00000000	
IRQDIS_2	0x00000000	0x00000000	IRQ line disable mask. Bit m of this 32-bit parameter disables IRQ[32n+m] and WICLINES[32n+m+2].
IRQDIS_3	0x00000000	0x00000000	For each bit:
IRQDIS_4	0x00000000	0x00000000	0 = IRQ enabled.
IRQDIS_5	0x00000000	0x00000000	1 = IRQ disabled.
IRQDIS_6	0x00000000	0x00000000	
IRQDIS_7	0x0000	0x0000	
MPU_NS	8	8	Specifies the number of implemented Non-secure Memory Protection Unit (MPU_NS) regions:
MPU_S	8	8	Specifies the number of implemented Secure Memory Protection Unit (MPU_S) regions: Note: If you exclude Security Extension, (MPU_S = 0), the Secure MPU is also excluded.
NUMIRQ	0x7C	32	Specifies the highest interrupt number (NUMIRQ-1) of implemented user interrupts
RAR	YES	NO	Specifies whether all synchronous states or only architecturally required states are reset
SAU	8	4	Specifies the number of implemented Security Attribute Unit (SAU) regions
SDIV	NO	NO	Specifies the implemented divider: NO = Include the fast, 17-cycle divider. YES = Include the small, 34-cycle divider.
SECEXT	YES	YES	Specifies whether the ARMv8-M security extensions are included

SMUL	NO	NO	Specifies the implemented multiplier: NO = Include the fast, single-cycle multiplier. YES = Include the small, 32-cycle multiplier.
SYST	2	2	Specifies whether the SysTick timer functionality is included
VTOR	YES	YES	Specifies whether the Vector Table Offset Register is included
WPT	2	2	Specifies the number of watchpoint unit comparators implemented.

Table 10-4 : Cortex-M23 configuration settings

Parameter	Implemented Values	Default Values	Description
ACG	YES	YES	Specifies if architectural clock gates are included to minimize dynamic power dissipation
CTI	YES	YES	Specifies whether the Cortex-M23 CTI is included
ETM	YES	NO	Specifies whether the Cortex-M23 ETM is included
MTB	NO	NO	Specifies whether the Cortex-M23 MTB is included
MTBWIDTH	0xC	12	Address width of MTB SRAM.
WIC	YES	YES	Specifies whether the WIC interface is implemented
WICLINES	0x7E	130	Specifies the lines supported by the WIC interface

Table 10-5 : Cortex-M23 integration configuration settings

Parameter	Implemented Values	Default Values	Description
AHBSLV	YES	YES	Specifies the bus protocol implemented on the SLV port
BASEADDR	0xE00FE003	0xE00FF003	Specifies the value of the DAP MEM-AP base register that is read by debug tools to locate the first debug component in the system
HALTEV	YES	NO	Specifies if the DAP includes halt event signaling support:
JTAGnSW	NO	NO	Specifies the external debug protocol implemented by the Cortex-M23 DAP: NO = Implement Serial Wire. YES = Implement JTAG.
SWMD	NO	NO	Cortex-M23 DAP Serial Wire Multi-drop Support:
TARGETID	0x07480477	0x00000001	Defines the contents of the Target Identification register in the Cortex-M23 DAP

Table 10-6 : Cortex-M23 integration MCU configuration settings