AMBA University Kit

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Technical Reference Manual

ARM®

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AMBA University Kit
Technical Reference Manual

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Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidentiality	Change
September 2001	A	Non-Confidential	First issue

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Preface

This preface introduces the ARM *AMBA University Kit* (AUK) and its reference documentation. It contains the following sections:

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About this document

This document is the technical reference manual for the AUK. It gives detailed information about:

- the function of the whole system
- each module in the system
- how to design a new system module.

Intended audience

This document has been written for *System-on-Chip* (SoC) designers and system architects, and provides a description of components within the AUK architecture.

Using this manual

This book is organized into the following chapters:

Chapter 1 ***Introduction***

Read this chapter for an overview of the AUK.

Chapter 2 ***The AUK Microcontroller***

Read this chapter for a description of the modules of the AHB EASY microcontroller.

Chapter 3 ***ARM7TDMI AHB Wrapper***

Read this chapter for a description of the ARM7TDMI AHB wrapper module.

Chapter 4 ***AHB Modules***

Read this chapter for details of the AHB modules that are used in the AUK.

Chapter 5 ***APB Modules***

Read this chapter for details of the APB modules that are used in the AUK.

Chapter 6 ***Behavioral Modules***

Read this chapter for details of how to use the behavioral modules, including memory modules and the external AMBA Test Interface Driver module (the *TICBOX*). This chapter contains a description of the *TICTalk* command language.

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Chapter 7 *Designer's Guide*

Read this chapter for details of how to add new bus master, slave and peripheral modules to the AHB EASY microcontroller.

Product revision status

The r*n*p*n*v*n* identifier indicates the revision status of the product described in this document, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

v*n* Identifies a version that does not affect the external functionality of the product.

Typographical conventions

The following typographical conventions are used in this book:

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names. Denotes ARM processor signal names. Also used for terms in descriptive lists, where appropriate.

`monospace` Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

`mono`space Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

`monospace italic` Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

`monospace bold` Denotes language keywords when used outside example code.

Timing diagram conventions

This manual contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labeled when they occur. Therefore, no additional meaning must be attached unless specifically stated.

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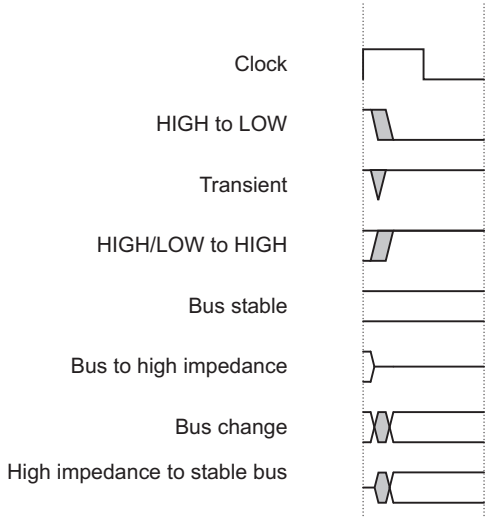

Key to timing diagram conventions

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

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Further reading

This section lists publications from both ARM Limited and third parties that provide additional information on developing code for the ARM family of processors.

ARM periodically provides updates and corrections to its documentation. See `http://www.arm.com` for current errata sheets, addenda, and the ARM Frequently Asked Questions list.

ARM publications

This document contains information that is specific to the AUK. Refer to the following documents for other relevant information:

- *AMBA Specification (Rev 2.0)* (ARM IHI 0011)
- *ARM Architecture Reference Manual* (ARM DUI 0100)
- *ARM7TDMI data Sheet* (ARM DDI 0029)
- *AUK User Guide* (ARM DUI 0167)
- *Micropack AHB CPU Wrappers Technical Reference Manual* (ARM DUI 0169).

Other publications

- *IEEE 1149.1 JTAG standard*.

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- the page number(s) to which your comments apply
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

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Chapter 1
Introduction

This chapter introduces the ARM *AMBA University Kit* (AUK). It contains the following section:

- *Overview of the AUK* on page 1-2.

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1.1 Overview of the AUK

The AUK comprises the building blocks needed to create an example system based on the low-power, generic design methodology of the *Advanced Microcontroller Bus Architecture* (AMBA).

The AUK:

- enables custom devices to be developed in very short design cycles
- enables the resulting subcomponents to be easily reused in future designs.

1.1.1 AUK system blocks

The example design provides all the system modules needed to manage an AMBA system:

- reset controller
- arbiter
- decoder.

These system modules control various aspects of the *Advanced High Performance Bus* (AHB).

1.1.2 AUK components

The example design comprises:

- Two buses:
  - the AHB
  - the *Advanced Peripheral Bus* (APB).
- The ARM processor AHB wrapper, to enable execution of ARM code in an AHB system.
- The *Test Interface Controller* (TIC), to enable external control of the AHB during system test.
- A minimum set of basic microcontroller peripherals. These are supported, and are implemented as low-power designs on the APB. They include:
  - an interrupt controller
  - a remap and pause controller
  - a 16-bit timer module.
- The example *Static Memory Interface* (SMI). This demonstrates the minimum requirements for an *External Bus Interface* (EBI).

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- A 1KB block of internal memory.

The AUK consists of a microcontroller with some external memory as shown in Figure 1-1.

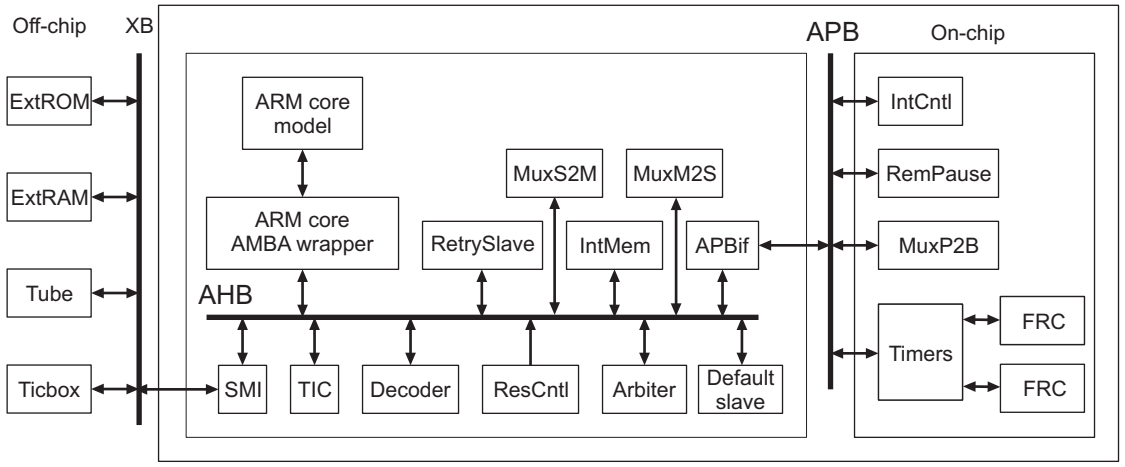

Figure 1-1 AUK system diagram

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Chapter 2
The AUK Microcontroller

This chapter describes the microcontroller which is the main unit of the ARM *AMBA University Kit* (AUK). It contains the following sections:

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2.1 Functional overview

The modules of the EASY microcontroller are grouped in five classes:

AMBA system components

Used to control the general operation of the system.

Peripherals Low-power peripherals, which are connected to the peripheral bus.

Example components

Demonstration modules that are only simulation models.

System test methodology

Modules used for testing the system.

Processor core

The ARM processor core that is built into the EASY microcontroller.

With the exception of the processor core the above modules are fully described in this chapter. For details of the processor core see Chapter 3 *ARM7TDMI AHB Wrapper*.

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2.2 The AMBA system components

The *Advanced Microcontroller Bus Architecture* (AMBA) system comprises:

- *Reset controller*
- *Arbiter*
- *Decoder*
- *AHB to APB bridge*.

2.2.1 Reset controller

The reset controller consists of a state machine which generates the **HRESETn** signal. This signal indicates the current reset state of the AMBA bus and is used by all the other elements in the EASY microcontroller, primarily for power-on initialization.

Note

All other reset modes, such as standby or warm reset, must be implemented separately.

2.2.2 Arbiter

The arbiter provides arbitration between bus masters competing for access to the AHB. Although there are only two bus masters in the EASY microcontroller, the ARM and the TIC, the arbiter has provision for up to four masters. To extend the number of masters, see Chapter 7 *Designer's Guide*. The arbitration is currently assigned with a simple priority system, with the TIC as the highest priority, and the processor as the lowest (also the reset default). The arbitration scheme is not defined in the *AMBA Specification* and can be dependent on implementation.

2.2.3 Decoder

The decoder consists of a simple address decoding logic, which is used to select the system bus slaves based on the address of the current transfer. This module controls the configurable memory map for the system.

2.2.4 AHB to APB bridge

The AHB to APB bridge interface is an AHB slave. When accessed (in normal operation or system test) it initiates an access to the APB. APB accesses are of different duration (three **HCLK** cycles in the EASY for a read, and two cycles for a write). They also have their width fixed to one word, which means it is not possible to write only an 8-bit section of a 32-bit APB register. APB peripherals do not require a **PCLK** input,

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because the APB access is timed with an enable signal generated by the AHB to APB bridge interface. This makes APB peripherals low power consumption parts, because they are only strobed when accessed.

For more information on the APB bus, see the *AMBA Specification*.

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2.3 Reference peripherals

Figure 2-1 shows how the reference peripherals are interconnected within the *Reference Peripherals Specification* (RPS) block, and how they are connected to the bridge.

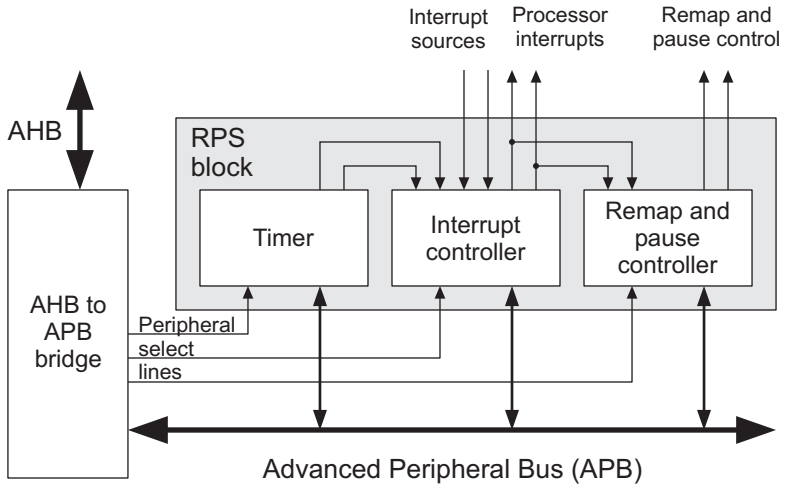

Figure 2-1 Block diagram of the RPS block and bridge

The base addresses of each of the peripherals (timer, interrupt controller, and remap and pause controller) are defined in the AHB to APB bridge interface, which selects the peripheral according to its base address. The whole APB address range is also defined in the bridge.

These base addresses can be implementation-specific. The peripherals standard specifies only the register offsets (from an unspecified base address), register bit meaning, and minimum supported function.

Table 2-1 shows the three bases and their current addresses in the EASY microcontroller.

Table 2-1 Peripherals base addresses

Peripheral	EASY base address
Interrupt controller	`0x8000 0000`
Timer	`0x8400 0000`
Remap and pause controller	`0x8800 0000`

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Note

When writing software or test patterns to run on the system, the absolute hex addresses must not be used within the code. Instead, define the base addresses in a header and then use the offset to this base address.

The APB data bus is split into two separate directions:

- read (**PRDATA**), where data travels from the peripherals to the bridge
- write (**PWDATA**), where data travels from the bridge to the peripherals.

This simplifies driving the buses because turnaround time between the peripherals and bridge is avoided.

In the default system, because the bridge is the only master on the bus, **PWDATA** is driven continuously. **PRDATA** is a multiplexed connection of all peripheral **PRDATA** outputs on the bus, and is only driven when the slaves are selected by the bridge during APB read transfers.

It is possible to combine these two buses into a single bidirectional bus, but precautions must be taken to ensure that there is no bus clash between the bridge and the peripherals.

2.3.1 Timer

The timer comprises:

- two 16-bit periodic/free running down counters
- a clock prescaler (divide by 1, 16, or 256)
- a test veneer.

When the counters underflow (passing zero value and reloading) they can generate interrupt requests which are passed to the interrupt controller. Both counter values can be loaded, read, and controlled through addressable registers.

2.3.2 Interrupt controller

The interrupt controller contains a set of registers for controlling eight *interrupt request* (IRQ) sources and one *fast interrupt request* (FIQ) source. These have the following functions:

- enable or disable specific interrupt sources from triggering the ARM **nIRQ** or **nFIQ** interrupt lines
- read the status of all interrupt sources at the inputs of the interrupt controller
- read the status of the interrupt sources enabled to trigger the ARM interrupt lines
- generate a software-triggered **nIRQ** signal to the ARM processor
- isolate the interrupt controller for test.

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The number of IRQ sources can easily be extended by increasing the number of IRQ registers.

2.3.3 Remap and pause controller

The remap and pause controller has three functions:

Reset status This enables software to determine whether the last reset was a *Power-On Reset* (POR) or a soft reset. The latter function is redundant in the EASY microcontroller, since it does not have a soft reset. It is implemented only as an example for systems that might provide a soft reset state.

Remap memory On reset the internal RAM is mapped out and bank 4 of the external memory is mapped into location `0x0000 0000` which is the boot location for the ARM processor. The reset memory map is cancelled by writing to a register in this peripheral.

Pause mode The EASY microcontroller only supports one simple power-saving mode, called Pause. This halts all bus activity (but not the system clock) and waits for an interrupt signal from the interrupt controller before restarting the system.

The remap and pause controller also contains an ID register which is currently only a single bit. This block can be extended in many ways including support for software-generated resets, more sophisticated power-saving modes and more detailed ID information.

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2.4 Example components

The example components include:

- *Internal memory*
- *Static memory interface*
- *Retry slave*
- *Default slave*.

Typically these blocks must be re-implemented according to the specific system requirements of the microcontroller being developed.

2.4.1 Internal memory

The internal memory is a very basic behavioral model of 1KB of zero wait state static memory, which is not synthesizable. The size of the memory can be extended by altering a setting in the HDL file.

2.4.2 Static memory interface

The SMI is a 32-bit *External Bus Interface* (EBI) that can connect up to four 256MB banks of zero to four wait state memory to the EASY microcontroller. However, the number of wait states is set as a constant in the HDL (before synthesis), and is set for all four banks. The example SMI also supports test signals from the TIC. These override the normal operation of the SMI during system test, and directly control the tristate drivers on the **XD** bus.

2.4.3 Retry slave

The retry slave is an example of how to implement an AHB slave that generates retry responses and wait states for read or write accesses. It is used as a template for building slaves that require the use of a retry response.

2.4.4 Default slave

The default slave is used to fill holes in the memory map, so that the system still functions if an invalid area of memory is accessed. This must be modified to suit the memory map of the system, so that all areas of memory access a system slave.

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2.5 System test methodology

Each AHB slave, AHB master, and APB peripheral must be tested in complete isolation. This means that components must be designed with test veneers that enable non-bus signals to be controlled and observed.

When a component is tested, a special test bit is set. This test bit switches these multiplexed signals to test registers (accessible through the AHB or APB), which effectively isolates each component from the rest of the system.

Test vectors must be written to test the component in isolation, making as few assumptions about the rest of the system as possible.

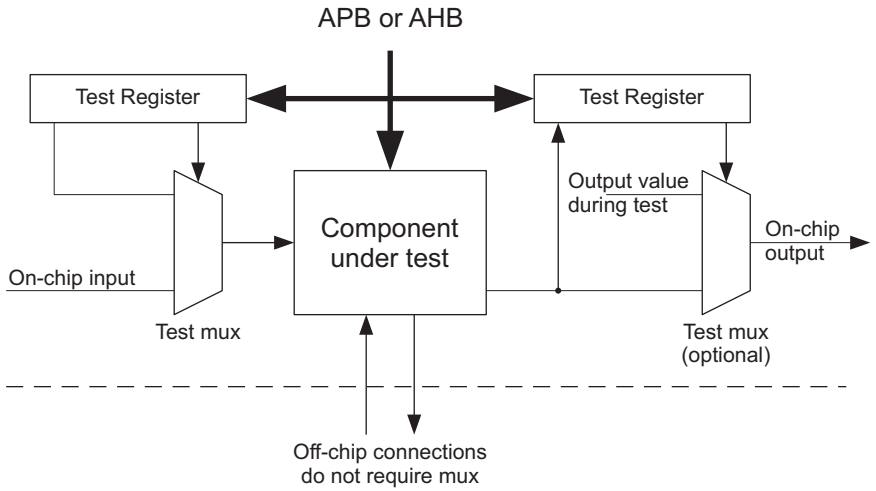

Figure 2-2 Simple test veneer example

A good example of this approach is provided by the test veneer for the ARM processor, which is described in the *AMBA ARM7TDMI Interface Data Sheet*. This approach is also used to test the peripherals on the APB bus.

Under normal conditions, when the TIC is not in use, the current bus master performs transfers to and from any one of the following slaves:

- internal memory
- AHB to APB bridge interface (to access the peripherals)
- example retry slave
- EBI.

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However, when test mode is entered, and the TIC is the current master, the following slaves can be accessed:

- internal memory
- AHB to APB bridge interface (to access the peripherals)
- example retry slave
- ARM bus master (test veneer).

Note

Bus masters can become slaves during test mode. The EBI cannot be tested using the TIC because of the way test access is provided to the AHB bus. The TIC is a state machine driven by the test request inputs (**TESTREQA** and **TESTREQB**). It also contains a register that enables it to read address information from the test bus (**TESTBUS**) and drive it onto the AHB address bus (**HADDR**). However, it cannot drive the test bus. Instead, it overrides the normal function of the EBI, forcing it to provide a 32-bit channel between **HRDATA** and **TESTBUS**, passing out read data during a read test vector. Therefore, in test mode, the EBI cannot function as a slave.

TESTBUS must be a 32-bit channel. In a system which only supports a 16-bit or 8-bit external data bus, additional external pins such as address lines must be forced into a special test mode to supply the full 32-bit bidirectional channel required.

For more information about:

- the test interface, see the *AMBA Specification*
- applying test vectors to an EASY-based microcontroller, see the *AUK User Guide*.

Note

The **TESTREQA**, **TESTREQB** and **TESTBUS** signals are the same as the **TREQA**, **TREQB**, and **TBUS** signals described in the *AMBA Specification (Rev 2.0)*.

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Chapter 3
ARM7TDMI AHB Wrapper

This chapter describes the ARM7TDMI processor core wrapper that you can use with an AHB-based EASY system. It contains the following sections:

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3.1 About the ARM7TDMI AHB wrapper

The ARM7TDMI AHB wrapper interfaces between the ARM7TDMI core and the AHB bus. The modules that translate access from the core to AHB accesses when the core is the current master are common to both cores. The wrapper itself sits alongside the core, intercepting the memory bus. An example higher-level module is also included for each core. This shows how the core and wrapper can be connected, and is used by the synthesis scripts provided to enable the wrapper to be synthesized alongside a timing file for the core.

The wrapper also enables testing of the ARM7TDMI core when the *Test Interface Controller* (TIC) is the current AHB master, allowing the TIF-format production test vectors supplied by ARM to be used with AHB-based designs. Figure 3-1 on page 3-3 shows a top-level block diagram of the ARM7TDMI AHB wrapper.

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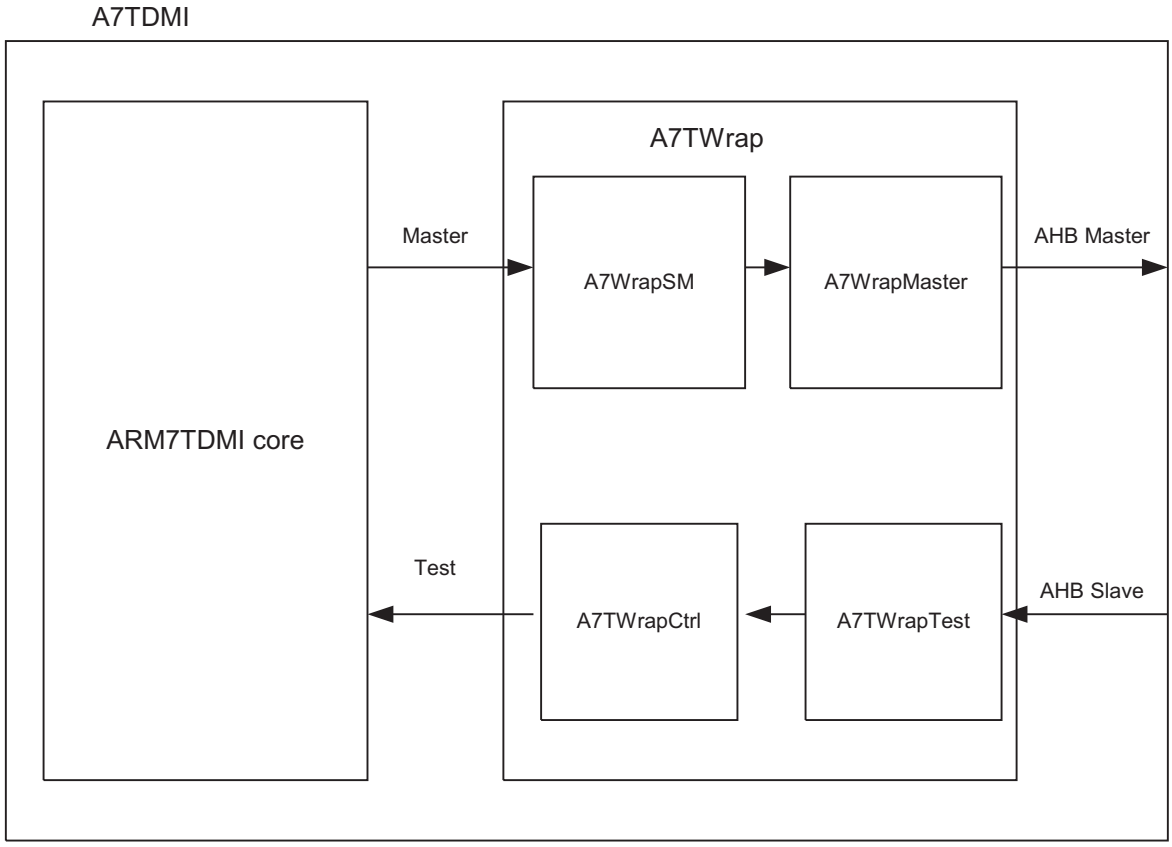

Figure 3-1 ARM7TDMI AHB wrapper block diagram

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3.2 Signal interface

This section describes the signal interface of A7TWrap. It does not describe the ARM7TDMI. Only those signals from the ARM7TDMI core that are used by the AHB wrapper are described. All other core signals must be connected to the external system in the same way as for a native core design. See the *ARM7TDMI Datasheet* for the relevant information.

Note

The exception is **DOUT[31:0]**, which must be connected directly to the **HWDATA[31:0]** AHB bus and the **DOUT[31:0]** input on A7TWrap.

Table 3-1 describes the signals used by the ARM7TDMI AHB wrapper.

Table 3-1 ARM7TDMI AHB signal descriptions

Signal	Direction	Description
System inputs		
HCLK	Input	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of **HCLK**.
HRESETn	Input	Reset. The bus reset signal is active LOW and is used to reset the system and the bus. This is the only active LOW AHB signal.
Master inputs		
HRDATAM[31:0]	Input	Read data bus. Used to transfer data to the ARM7TDMI in master mode.
HREADYM	Input	Transfer done. When HIGH, the **HREADYM** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESPM[1:0]	Input	Transfer response. Indicates an OKAY, ERROR, RETRY, or SPLIT response.
HGRANTM	Input	Bus grant. Indicates that the ARM7TDMI is currently the highest priority master. Ownership of the address/control signals changes at the end of a transfer when **HREADYM** is HIGH, so a master gains access to the bus when both **HREADYM** and **HGRANTM** are HIGH.
Master outputs		
HADDRM[31:0]	Output	This is the 32-bit system address bus.
HTRANSM[1:0]	Output	Transfer type. Indicates the type of the current transfer, that can be NONSEQUENTIAL, SEQUENTIAL, or IDLE.

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Table 3-1 ARM7TDMI AHB signal descriptions (continued)

Signal	Direction	Description
HWRITEM	Output	Transfer direction. When HIGH, this signal indicates a write transfer and when LOW a read transfer.
HSIZEM[2:0]	Output	Transfer size. Indicates the size of the transfer, that can be byte (8-bit), halfword (16-bit), or word (32-bit).
HBURSTM[2:0]	Output	Burst type. This signal indicates if the transfer forms part of a burst. The **ARM7TDMI** performs incrementing bursts of type INCR.
HPROTM[3:0]	Output	Protection control. These signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a Supervisor mode access or User mode access.
HBUSREQM	Output	Bus request. A signal from the wrapper to the bus arbiter that indicates that it requires the bus.
HLOCKM	Output	Locked transfer. When HIGH, this signal indicates that the master requires locked access to the bus and no other master must be granted the bus until this signal is LOW.
Slave inputs		
HTRANS1S	Input	Transfer type. This is attached to bit 1 of the AHB **HTRANS[1:0]** bus. It indicates an active (NONSEQ or SEQ) or inactive (IDLE or BUSY) transfer.
HWRITES	Input	Transfer direction. When HIGH, this signal indicates a write transfer and when LOW a read transfer.
HWDATAS[31:0]	Input	Write data bus. Used to transfer data to the **ARM7TDMI** in slave mode.
HSELS	Input	Slave select. Selects the **ARM7TDMI** as slave.
HREADYS	Input	Transfer done. When HIGH, this signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
Slave outputs		
HRDATAS[31:0]	Output	Read data bus. Used to transfer data from the ARM7TDMI in slave mode.
HREADYOUTS	Output	Transfer done. When HIGH, this signal indicates that a transfer to the ARM7TDMI has finished. This signal can be driven LOW to extend a transfer.
HRESPS[1:0]	Output	Transfer response. Indicates an OKAY, ERROR, RETRY, or SPLIT response. The ARM7TDMI always responds with OKAY.

Table 3-2 on page 3-6 describes the signals to the ARM7TDMI core.

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Table 3-2 Signals to ARM7TDMI core

Signal	Direction	Description
Shared master/slave signals		
nRESET	Output	Active LOW reset to core.
MCLK	Output	Core clock for ARM7TDMI.
DIN[31:0]	Output	Data bus. For master mode this is connected to **HRDATAM**, for test mode it is connected to **HWDATAS**.
DOUT[31:0]	Input	Data bus. For master mode this is connected to **HWDATAM**, for test mode it is connected to **HRDATAS**.
Master inputs		
A[31:0]	Input	Address bus
LOCK	Input	Indicates a locked transfer (such as SWP).
MAS[1:0]	Input	Transfer size. Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit).
nMREQ	Input	Not memory access.
nOPC	Input	Not opcode access.
nRW	Input	Not read/write.
nTRANS	Input	Not memory translate. When LOW, this signal indicates that the processor is in user mode.
SEQ	Input	Sequential access.
Master outputs		
ABORT	Output	Indicates that an access has aborted (that is, received an ERROR response on the AHB).
nFIQ	Output	Fast interrupt request.
nIRQ	Output	Standard interrupt request.
nWAIT	Output	Indicates that current access is waited.
Test inputs		
BUSDIS	Input	Bus disable. When INTEST is selected on scan chain 0, 4, or 8 this is HIGH. It can be used to disable external logic driving onto the bidirectional data bus during scan testing. This signal changes after the falling edge of **TCK**.

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Table 3-2 Signals to ARM7TDMI core (continued)

Signal	Direction	Description
COMMRX	Input	When the communications channel receive buffer is full this is HIGH. This signal changes after the rising edge of **MCLK**.
COMMTX	Input	When the communications channel transmit buffer is empty this is HIGH. This signal changes after the rising edge of **MCLK**.
DBGACK	Input	Debug acknowledge. When the processor is in a debug state this is HIGH.
DBRQI	Input	Internal debug request. This is the logical OR of **DBGRQ** and bit 1 of the debug control register.
HIGHZ	Input	When the **HIGHZ** instruction has been loaded into the TAP controller this signal is HIGH.
RANGEOUT0	Input	EmbeddedICE macrocell. When the EmbeddedICE watchpoint unit 0 has matched the conditions currently present on the address, data, and control buses, this is HIGH. This signal is independent of the state of the watchpoint enable control bit.
RANGEOUT1	Input	EmbeddedICE macrocell. The same as **RANGEOUT0** but corresponds to the EmbeddedICE watchpoint unit 1.
nCPI	Input	Not coprocessor instruction. LOW when a coprocessor instruction is processed. The processor then waits for a response from the coprocessor on the **CPA** and **CPB** lines. If **CPA** is HIGH when **MCLK** rises after a request has been initiated by the processor, the coprocessor handshake is aborted, and the processor enters the undefined instruction trap. If **CPA** is LOW at this time, the processor enters a busy-wait period until **CPB** goes LOW before completing the coprocessor handshake.
nENOUT	Input	Not enable output. During a write cycle, this signal is driven LOW before the rising edge of **MCLK**, and remains LOW for the entire cycle. This can be used to aid arbitration in shared bus applications.
nENOUTI	Input	Not enable output. During a write cycle, this signal is driven LOW before the rising edge of **MCLK**, and remains LOW for the entire cycle. This can be used to aid arbitration in shared bus applications.
nEXEC	Input	Not executed. This is HIGH when the instruction in the execution unit is not being executed because, for example, it has failed its condition code check.
nM[4:0]	Input	Not processor mode. These are the inverse of the internal status bits indicating the current processor mode.

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Table 3-2 Signals to ARM7TDMI core (continued)

Signal	Direction	Description
nTDOEN	Input	Not **TDO** enable. When serial data is being driven out on **TDO** this is LOW. Usually used as an output enable for a **TDO** pin in a packaged part.
SCREG[3:0]	Input	Scan chain register. These reflect the ID number of the scan chain currently selected by the TAP controller. These change on the falling edge of **TCK** when the TAP state machine is in the UPDATE-DR state.
TBIT	Input	Thumb state. When the processor is executing the THUMB instruction set, this is HIGH. It is LOW when executing the ARM instruction set. This signal changes in phase two in the first execute cycle of a BX instruction.
xnTRST	Input	JTAG reset input from external tester.
xTCK	Input	JTAG clock input from external tester.
xTDI	Input	JTAG data input from external tester.
xTMS	Input	JTAG mode select input from external tester.
xTDO	Input	JTAG data input from core.
Slave outputs		
ABE	Output	Address bus enable. The address bus drivers are disabled when this is LOW, putting the address bus into a high impedance state. This also controls the LOCK, **MAS[1:0]**, **nRW**, **nOPC**, and **nTRANS** signals in the same way. **ABE** must be tied HIGH if there is no system requirement to disable the address drivers.
ALE	Output	Address latch enable. This signal is provided for backwards compatibility with older ARM processors. For new designs, if address retiming is required, ARM Limited recommends the use of **APE**, and for **ALE** to be connected HIGH. The address bus, **LOCK**, **MAS[1:0]**, **nRW**, **nOPC**, and **nTRANS** signals are latched when this is held LOW. This enables these address signals to be held valid for the complete duration of a memory access cycle. For example, when interfacing to ROM, the address must be valid until after the data has been read.
APE	Output	Address pipeline enable. Selects whether the address bus, **LOCK**, **MAS[1:0]**, **nRW**, **nTRANS**, and **nOPC** signals operate in pipelined (**APE** is HIGH) or depipelined mode (**APE** is LOW). Pipelined mode is particularly useful for DRAM systems, where it is desirable to provide the address to the memory as early as possible, to enable longer periods for address decoding and the generation of DRAM control signals. In this mode, the address bus does not remain valid to the end of the memory cycle. Depipelined mode can be useful for SRAM and ROM access. Here the address bus, **LOCK**, **MAS[1:0]**, **nRW**, **nTRANS**, and **nOPC** signals must be kept stable throughout the complete memory cycle. However, this does not provide optimum performance.

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Table 3-2 Signals to ARM7TDMI core (continued)

Signal	Direction	Description
BIGEND	Output	Big-endian configuration. Selects how the processor treats bytes in memory: • HIGH for big-endian format • LOW for little-endian format.
BL[3:0]	Output	Byte latch control. The values on the data bus are latched on the falling edge of **MCLK** when these signals are HIGH. For most designs these signals must be tied HIGH.
BREAKPT	Output	Breakpoint. A conditional request for the processor to enter debug state is made by placing this signal HIGH. If the memory access at that time is an instruction fetch, the processor enters debug state only if the instruction reaches the execution stage of the pipeline. If the memory access is for data, the processor enters debug state after the current instruction completes execution. This allows extension of the internal breakpoints provided by the EmbeddedICE Logic.
BUSEN	Output	Bus enable. A static configuration signal that selects whether the bidirectional data bus (**D[31:0]**) or the unidirectional data buses (**DIN[31:0]** and **DOUT[31:0]**) are used for transfer of data between the processor and memory. When **BUSEN** is LOW, **D[31:0]** is used. **DOUT[31:0]** is driven to a value of zero, and **DIN[31:0]** is ignored, and must be tied LOW. When **BUSEN** is HIGH, **DIN[31:0]** and **DOUT[31:0]** are used. **D[31:0]** is ignored and must be left unconnected.
CPA	Output	Coprocessor absent. Placed LOW by the coprocessor if it is capable of performing the operation requested by the processor.
CPB	Output	Coprocessor busy. Placed LOW by the coprocessor when it is ready to start the operation requested by the processor. It is sampled by the processor when **MCLK** goes HIGH in each cycle in which **nCPI** is LOW.
DBE	Output	Data bus enable. Must be HIGH for data to appear on either the bidirectional or unidirectional data output bus. When LOW the bidirectional data bus is placed into a high impedance state and data output is prevented on the unidirectional data output bus. It can be used for test purposes or in shared bus systems.
DBGEN	Output	Debug enable. A static configuration signal that disables the debug features of the processor when held LOW. This signal must be HIGH to allow the EmbeddedICE Logic to function.
DBGRQ	Output	Debug request. This is a level-sensitive input, that when HIGH causes ARM7TDMI core to enter debug state after executing the current instruction. This enables external hardware to force the ARM7TDMI core into debug state, in addition to the debugging features provided by the EmbeddedICE Logic.

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Table 3-2 Signals to ARM7TDMI core (continued)

Signal	Direction	Description
EXTERN0	Output	External input 0. This is connected to the EmbeddedICE Logic and allows breakpoints and watchpoints to be dependent on an external condition.
EXTERN1	Output	External input 1. This is connected to the EmbeddedICE Logic and allows breakpoints and watchpoints to be dependent on an external condition.
ISYNC	Output	Synchronous interrupts. Set this HIGH if **nIRQ** and **nFIQ** are synchronous to the processor clock, LOW for asynchronous interrupts.
nENIN	Output	Not enable input. This must be LOW for the data bus to be driven during write cycles. Can be used in conjunction with **nENOUT** to control the data bus during write cycles.
nTRST	Output	Not test reset. Reset signal for the boundary-scan logic. This pin must be pulsed or driven LOW to achieve normal device operation, in addition to the normal device reset, **nRESET**.
SDOUTBS	Output	Boundary scan serial output data. Accepts serial data from an external boundary-scan chain output, synchronized to the rising edge of **TCK**. This must be tied LOW, if an external boundary-scan chain is not connected.
TBE	Output	Test bus enable. When LOW, **D[31:0]**, **A[31:0]**, **LOCK**, **MAS[1:0]**, **nRW**, **nTRANS**, and **nOPC** are set to high impedance. Similar in effect as if both **ABE** and **DBE** had been driven LOW. However**, TBE** does not have an associated scan cell and so enables external signals to be driven high impedance during scan testing. Under normal operating conditions **TBE** must be HIGH.
TCK	Output	Test clock. Clock signal for all test circuitry. When in debug state, this is used to generate **DCLK**, **TCK1**, and **TCK2**.
TDI	Output	Test data in. Serial data for the scan chains.
TMS	Output	Test mode select. Mode select for scan chains.

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3.3 Description of the ARM7TDMI wrapper blocks

This section contains descriptions of the following blocks:

- *A7TDMI*
- *A7TWrap*
- *A7WrapSM*
- *A7WrapMaster* on page 3-14
- *A7TWrapTest* on page 3-15
- *A7TWrapCtrl* on page 3-21.

3.3.1 A7TDMI

This is an example top level containing instantiations of both the ARM7TDMI core and the AHB wrapper. It is used by the provided synthesis scripts to enable synthesis of the wrapper alongside a characterized timing file of the core. All core signals not connected to the AHB wrapper are shown with example connections only. You can change these, or use a completely new top-level in the design.

3.3.2 A7TWrap

This instantiates the master and slave components of the ARM7TDMI AHB wrapper. It includes:

- multiplexor on **DIN**
- combinational creation of TRANS from **nMREQ** and **SEQ**
- creation of **MCLK** from inverted **HCLK**
- delayed **CLKEN**.

3.3.3 A7WrapSM

In master mode, this block converts the memory accesses from the core into pseudo-AHB accesses. The following sections of the code are explained:

- *Main state machine* on page 3-12
- *Address generation* on page 3-13
- *Wait states* on page 3-14
- *Error support* on page 3-14
- *Control signaling (HTRANS, HSIZE, HBURST, HPROT)* on page 3-14.

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Main state machine

The main state machine uses the state variable AddrState (which is registered to create LastAddrState). This can take the following enumerated values:

IDLE Default state. Indicates that no transfer is taking place on the AHB.

IS Indicates that the current IDLE cycle can be part of a merged I-S access.

NON Indicates that the current access is a non-sequential transfer.

SEQ Indicates that the current access is a sequential transfer.

LOKI Pause state to enable **HLOCK** to be asserted on the AHB for one cycle prior to the read access of a SWP instruction.

LOKR Read access of a SWP instruction.

LOKW Read access of a SWP instruction.

Figure 3-2 on page 3-13 shows the possible state transitions. State transitions occur on the rising edge of **HCLK**. Transitions back to the same state can occur either when the access on the pseudo-AHB is waited, or during sequential accesses in a burst (SEQ only).

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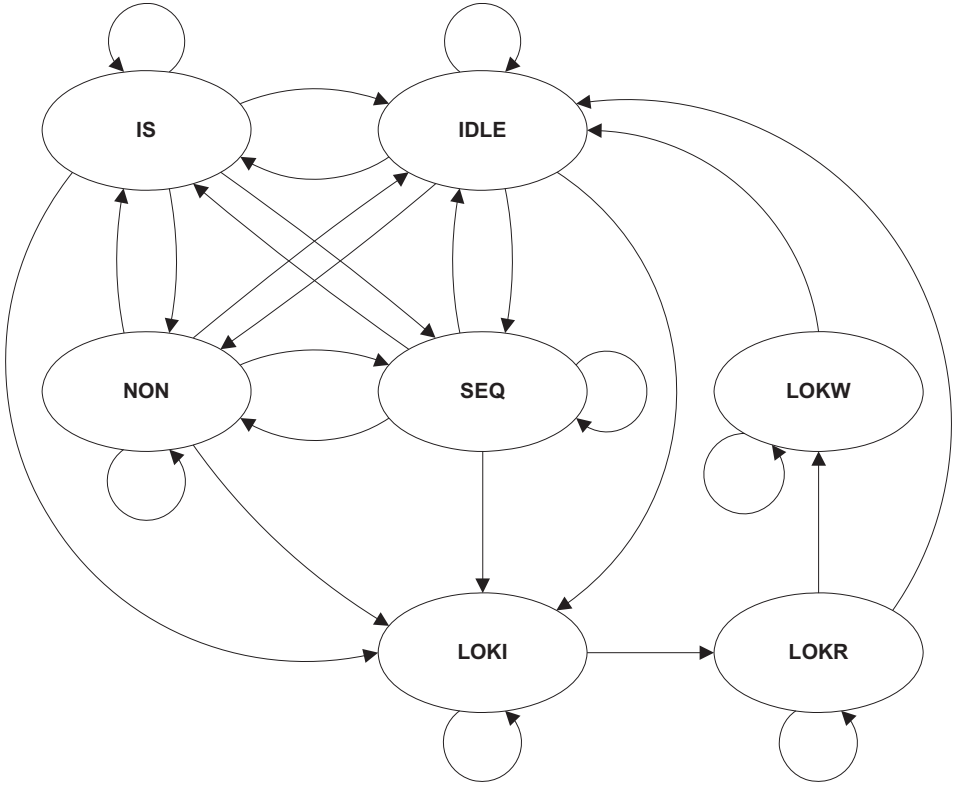

Figure 3-2 ARM7 AHB wrapper main state machine

Address generation

There are two internal sources of address:

- a registered version of the core address
- a locally incremented address created within A7WrapSM.

Normally the registered version of the address is used, but the registered version is required when performing sequential accesses to prevent a combinational path from the core to **HADDR**.

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Wait states

Wait states on the AHB (indicated by **HREADY** being LOW) are propagated to the ARM7 only when the core is attempting to access the bus. A string of IDLE cycles are not waited. Additional wait states (where one wait state equates to a single cycle of **HCLK**) are added as follows:

- +1 wait state for each NONSEQ access from the core (except SWP accesses). These are masked by wait states from the previous access, if any are received. Instruction fetches from the ARM7 cores are always initiated as merged I-S cycles, and so do not see this extra wait state.
- +2 wait states on the read at the start of a SWP instruction. This enables **HLOCK** to be asserted for a cycle before the AHB access commences.

Error support

The ARM7 AHB wrappers include support for the ERROR response on **HRESP**.

Control signaling (HTRANS, HSIZE, HBURST, HPROT)

Table 3-3 shows the control signal values used by the ARM7 AHB wrapper.

Table 3-3 Control signal values

Signal	Value
HTRANS	00: IDLE 10: NONSEQUENTIAL 11: SEQUENTIAL
HSIZE	00: BYTE 01: HALFWORD 10: WORD
HBURST	001: INCR
HPROT	bit 3: (cacheable) 0 for all accesses bit 2: (bufferable) 0 for all accesses bit 1: 1 = privileged access, 0 = user access bit 0: 1 = data access, 0 = opcode fetch

3.3.4 A7WrapMaster

In master mode, this block converts the pseudo-AHB accesses from A7WrapSM into true AHB by adding support for split and retry responses, and also for **HGRANT**. A SPLIT or RETRY response, or loss of **HGRANT**, causes the affected access to be placed into a holding register for reconstruction when the access can recommence on the AHB. During this time, the pseudo-AHB access is simply waited using **MREADY**.

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The holding registers store the current transfer on the pseudo-AHB on each valid cycle (qualified by **MREADY**). The AHB outputs are multiplexed based on the signal **HoldSel**. This is a registered signal, which is synchronously set and cleared by **HoldSet** and **HoldClr** respectively:

- **HoldSet** is activated when a SPLIT or RETRY response is received during the data phase of an access to the core, or when ownership of the AHB bus is lost whilst attempting an active transfer (that is, NONSEQ or SEQ).
- **HoldClr** is activated when **HoldSel** is active, the AHB wrapper has ownership of the bus and any SPLIT or RETRY response has completed.

3.3.5 A7TWrapTest

The test interface block is used to enable the wrapper module to act as an AHB slave during TIC testing of the core. The main parts of this block are:

- the test state machine, that controls the application of the test vectors
- the 28-bit test register, that stores the value of the control inputs during test

The test state machine uses the state variable NextTest (which is registered to create CurrentTest). This can take the following enumerated values:

ST_INACTIVE

Default state. This state is used when the wrapper is not in test mode, and all test outputs are driven to their default levels. The core is clocked as normal in this state.

ST_CTRL_IN

This state is used to load the test register with the control data that is currently on the write data bus. This then determines the values of the control signals that is applied to the core when it is clocked. The core is not clocked during this state.

ST_DATA_IN

In this state write data is being applied to the core (the core is performing a read transfer). The core is clocked in this state.

ST_DATA_OUT

In this state read data is being loaded from the core (the core is performing a write transfer). The core is clocked in this state.

ST_STAT_OUT

This state is used to read the output status signals from the core. The core is not clocked in this state.

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ST_ADDR_OUT

This state is used to read the address output from the core. The core is not clocked in this state.

ST_TURNAROUND

This state is used to enable the external data bus time to turnaround between the address read cycle and the control vector write cycle. The core is not clocked in this state.

The state diagram for the test state machine is shown in Figure 3-3.

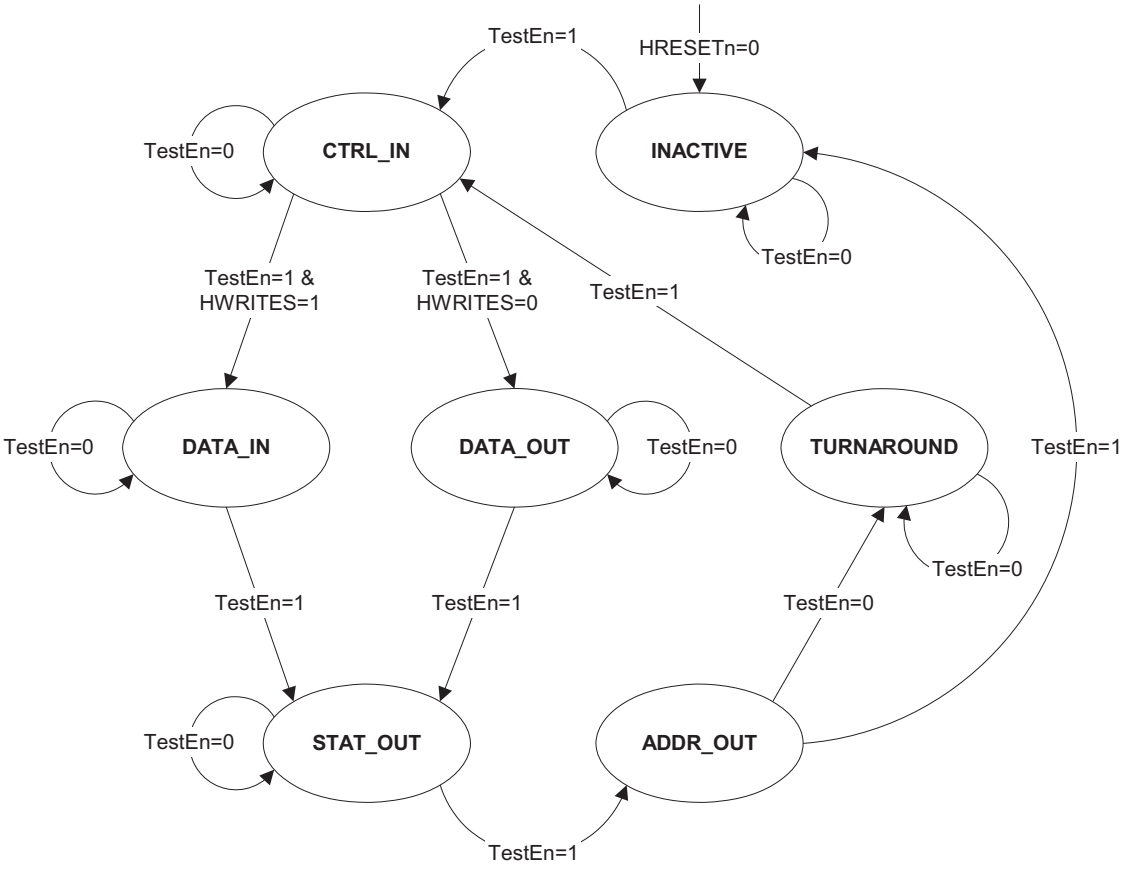

Figure 3-3 ARM7 AHB wrapper test state machine

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The **TestEn** signal is used to control when test vectors are applied to the core, and controls the transitions through the test state machine. **TestEn** is set HIGH when the core is addressed during a valid transfer, when the **HTRANS** input indicates a NONSEQUENTIAL or a SEQUENTIAL transfer.

The 28-bit test register that is loaded during the ST_CTRL_IN state determines the control inputs to the core when it is clocked during the ST_DATA_IN or ST_DATA_OUT states. Table 3-4 shows the control input bit positions.

Table 3-4 ARM7TDMI control input bit position

Signal	Description	Bit position	Comments
SDOUTBS	Boundary scan serial output data	27	-
TBE	Test bus enable	26	-
APE	Address pipeline enable	25	-
BL[3:0]	Byte latch control	24:21	ANDed with **TestClk**, and must only be valid during data access cycle.
TMS	Test mode select	20	-
TDI	Test data in	19	-
TCK	Test clock	18	ANDed with **TestClk.**
nTRST	Not test reset	17	-
EXTERN1	External input 1	16	-
EXTERN0	External input 0	15	-
DBGRQ	Debug request	14	-
BREAKPT	Breakpoint	13	-
DBGEN	Debug enable	12	-
ISYNC	Synchronous interrupts	11	-
BIGEND	Big-endian configuration	10	-
CPA	Coprocessor absent	9	-

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Table 3-4 ARM7TDMI control input bit position (continued)

Signal	Description	Bit position	Comments
CPB	Coprocessor busy	8	-
ABE	Address bus enable	7	This must normally be set HIGH, because if the address bus is tristated (**ABE** LOW), it is not possible to read address values.
ALE	Address latch enable	6	-
DBE	Data bus enable	5	
nFIQ	Not fast interrupt request	4	-
nIRQ	Not interrupt request	3	-
ABORT	Memory abort	2	This must normally be driven when **HRESP** indicates ERROR, and the wrapper has control of the AHB data bus.
nWAIT	Not wait	1	ANDed with **TestClk**, so that the core state can only change during the data access cycle.
nRESET	Not reset	0	-

The test data output multiplexor is found in the A7TWrapCtrl block, but is controlled by the test outputs of this block. It is used to select between:

- core data output during ST_DATA_OUT
- core address output during ST_ADDR_OUT
- core status outputs during ST_STAT_OUT.

The selected output is driven onto the **HRDATAS** output data bus.

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Table 3-5 shows the bit positions of the status output signals when driven on the data bus.

Table 3-5 ARM7TDMI status bit positions

Signal	Description	Bit position	Comment
BUSDIS	Bus disable	31	-
SCREG[3:0]	Scan chain register	30:27	These signals are not important to the normal functioning of the core, but are included in this test vector to give a slight improvement in fault coverage during scan and debug testing.
HIGHZ	HIGHZ instruction in TAP controller	26	-
nTDOEN	Not **TDO** enable	25	-
DBGRQ1	Internal debug request	24	-
RANGEOUT0	ICEbreaker Rangeout0	23	-
RANGEOUT1	ICEbreaker Rangeout1	22	-
COMMRX	Communications channel receive	21	-
COMMTX	Communications channel transmit	20	-
DBGACK	Debug acknowledge	19	-
TDO	Test data out	18	This value is often tristate (as indicated by **nTDOEN**), so is usually masked out.
nENOUT	Not enable output	17	**nENOUT** is only valid during the data access cycle, so **TestClk** is used to clock a register that captures the correct state.

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Table 3-5 ARM7TDMI status bit positions (continued)

Signal	Description	Bit position	Comment
nENOUTI	Not enable output	16	**nENOUTI** is only valid during the data access cycle, so **TestClk** is used to clock a register that captures the correct state.
TBIT	Thumb state	15	-
nCPI	Not coprocessor instruction	14	-
nM[4:0]	Not processor mode	13:9	-
nTRANS	Not memory translate	8	-
nEXEC	Not executed	7	-
LOCK	Locked operation	6	-
MAS[1:0]	Memory access size	5:4	-
nOPC	Not opcode fetch	3	-
nRW	Not read/write	2	-
nMREQ	Not memory request	1	-
SEQ	Sequential address	0	-

This test interface block can be removed if not required, by removing the A7TWrapTest block from the A7TWrap top level wrapper HDL file. It is then necessary to tie the outputs that were originally generated from this block to fixed values, and these are described in the A7TWrap HDL code.

Removing this block means that the test inputs to the A7TWrapCtrl block is static, allowing the test multiplexors to be removed during synthesis, or manually removed from the HDL code.

The AHB slave outputs are only used during TIC testing mode. **HREADYOUTS** is always driven HIGH, because the wrapper never generates wait states. **HRESPS** is always driven to OKAY, because the wrapper never asserts split, retry or error responses.

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HRDATAS is generated according to the current test control signal outputs, and is driven to either **DOUT** from the core, **TestData** from the test block (which is comprised of the core control outputs), or LOW.

3.3.6 A7TWrapCtrl

This block contains the test wrapper control multiplexor used during TIC testing of the core. A simplified diagram of the A7TWrapCtrl block is shown in Figure 3-4.

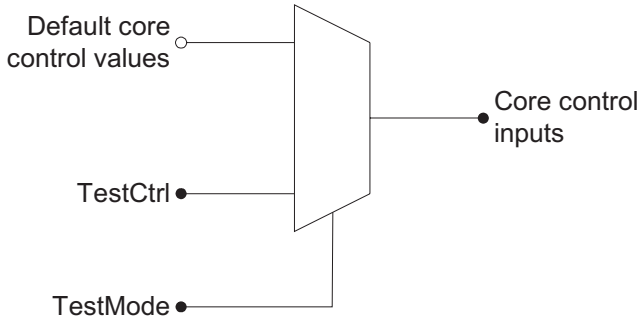

Figure 3-4 A7TWrapCtrl block system diagram

This block is only used during test mode when the wrapper is acting as an AHB slave, and drives the control inputs of the core with the TIC test data. It is separated from the main test block (A7TWrapTest) to enable easier removal of the test wrapper.

When not in test mode the control inputs are driven to their default values (either HIGH or LOW), or are driven with wrapper inputs, such as the two interrupt lines and the JTAG pins. The **AbortInt** signal is generated in the A7WrapMaster block.

If the test wrapper is removed, this multiplexor is optimized out during synthesis, and the outputs driven with their default values. It is also possible to remove this block if the test wrapper is not used. The default connections that the outputs must be tied to are shown in the A7TWrap HDL file.

BUSEN, **DBE**, and **nENIN** are all set to constant values, because they do not have to be controlled during normal system use, or during core TIC testing.

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3.4 Non-standard design practices

The following non-standard design practices are described:

- *Clock gating*
- *Transparent latches*.

3.4.1 Clock gating

A clock inverter is instantiated within A7TWrap (instance name *nHCLKgen*) to provide **nHCLK** (inverted **HCLK**). This signal is used in the following places:

A7TWrap Creation of **dCLKEN**, one of the enable terms for **MCLK**.

A7TWrapTest Creation of **TestModeF**, the other enable term for **MCLK**.

An inverted version of the clock is used so that all HDL code describes only rising-edge sequential logic. This is done because some cell libraries do not contain falling-edge registers, and also to avoid possible insertion of unwanted clock gating during synthesis.

A clock NAND gate is used within A7TWrap (instance name *MCLKgen*) to create **MCLK**, the clock for the memory interface of the ARM7TDMI.

The clock gates are described in the design block ClockInv and ClockNand. The methodology chosen within the supplied synthesis scripts synthesizes these blocks first, sets them as *dont_touch*, and then links them in when synthesizing the wrapper. This ensures that the clock gate instances have known references, and also prevents the optimization routines during later synthesis from altering the gates.

3.4.2 Transparent latches

A transparent latch is instantiated within A7TWrap (instance name *DelCLKEN*). This is use to create **dCLKEN**, one of the enable terms for **MCLK**. The latch operation is described in the design block LATS (transparent latch with asynchronous set). The synthesis methodology for this block is the same as for the clock gates described above.

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Chapter 4
AHB Modules

This chapter describes the data sheets for the modules that are connected to the *Advanced High Performance Bus* (AHB). It contains the following sections:

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4.1 APB bridge

The AHB to APB bridge is an AHB slave, providing an interface between the high-speed AHB and the low-power APB. Read and write transfers on the AHB are converted into equivalent transfers on the APB. Because the APB is not pipelined, wait states are added during transfers to and from the APB when the AHB is required to wait for the APB. Figure 4-1 shows the block diagram of the APB bridge module.

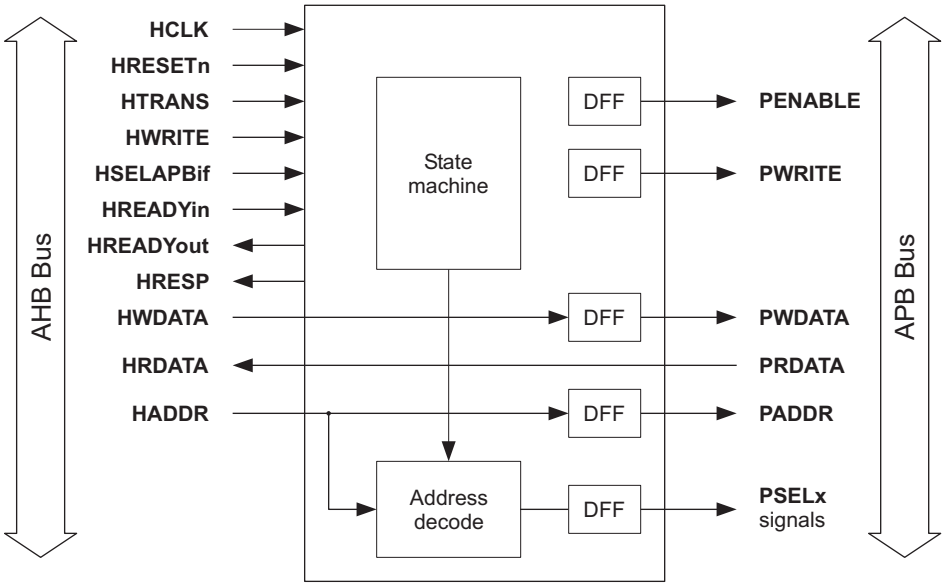

Figure 4-1 Block diagram of bridge module

The main sections of this module are:

- AHB slave bus interface
- APB transfer state machine, which is independent of the device memory map
- APB output signal generation.

To add new APB peripherals, or alter the system memory map, only the address decode sections have to be modified.

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4.1.1 Signal descriptions

The APB bridge module signals are described in Table 4-1 on page 4-2.

Table 4-1 Signal descriptions for bridge module

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.
HTRANS[1:0]	Transfer type	Input	This indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	Transfer direction	Input	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.
HWDATA[31:0]	Write data bus	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this can easily be extended to allow for higher bandwidth operation.
HSELAPBif	Slave select	Input	Each APB slave has its own slave select signal, and this signal indicates that the current transfer is intended for the selected slave. This signal is a combinatorial decode of the address bus.
HRDATA[31:0]	Read data bus	Output	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this can easily be extended to allow for higher bandwidth operation.
HREADYin HREADYout	Transfer done	Input/ output	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module always generates the OKAY response.
PRDATA[31:0]	Peripheral read data bus	Input	The peripheral read data bus is driven by the selected peripheral bus slave during read cycles (when **PWRITE** is LOW).
PWDATA[31:0]	Peripheral write data bus	Output	The peripheral write data bus is continuously driven by this module, changing during write cycles (when **PWRITE** is HIGH).

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Table 4-1 Signal descriptions for bridge module (continued)

Signal	Type	Direction	Description
PENABLE	Peripheral enable	Output	This enable signal is used to time all accesses on the peripheral bus. **PENABLE** goes HIGH on the second clock rising edge of the transfer, and LOW on the third (last) rising clock edge of the transfer.
PSELx	Peripheral slave select	Output	There is one of these signals for each APB peripheral present in the system. The signal indicates that the slave device is selected, and that a data transfer is required. It has the same timing as the peripheral address bus. It becomes HIGH at the same time as **PADDR**, but is set LOW at the end of the transfer.
PADDR[31:0]	Peripheral address bus	Output	This is the APB address bus, which can be up to 32 bits wide and is used by individual peripherals for decoding register accesses to that peripheral. The address becomes valid after the first rising edge of the clock at the start of the transfer. If there is a following APB transfer, the address changes to the new value, otherwise it holds its current value until the start of the next APB transfer.
PWRITE	Peripheral transfer direction	Output	This signal indicates a write to a peripheral when HIGH, and a read from a peripheral when LOW. It has the same timing as the peripheral address bus.

Timing diagrams showing the relationship between AHB and APB transfers can be found in the *APB Specification*.

4.1.2 Peripheral memory map

The APB bridge controls the memory map for the peripherals, and generates a select signal for each peripheral. The default system memory map is shown in Figure 4-2 on page 4-5.

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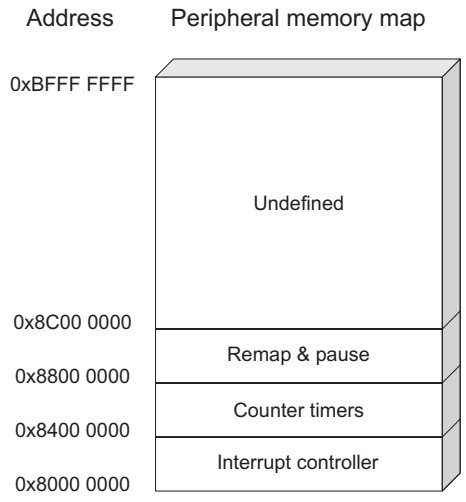

Figure 4-2 Peripheral memory map

4.1.3 Function and operation of module

The APB bridge responds to transaction requests from the currently granted AHB master. The AHB transactions are then converted into APB transactions. The state machine, shown in Figure 4-3 on page 4-6, controls:

- the AHB transactions with the **HREADYout** signal
- the generation of all APB output signals.

The individual **PSELx** signals are decoded from **HADDR**, using the state machine to enable the outputs while the APB transaction is being performed.

If an undefined location is accessed, operation of the system continues as normal, but no peripherals are selected.

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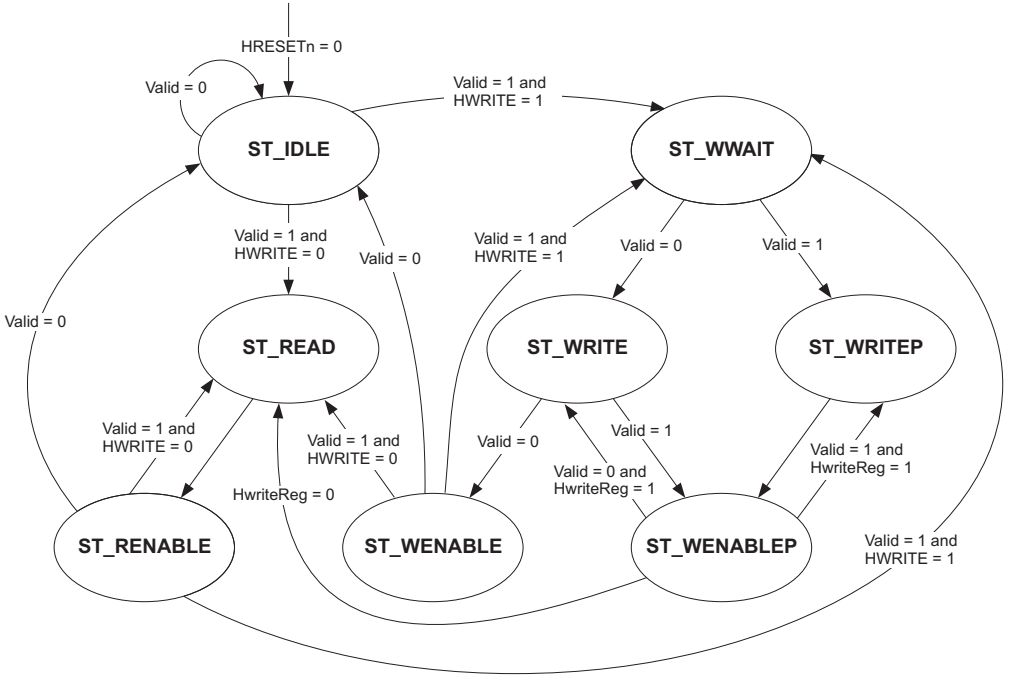

Figure 4-3 State machine for AHB to APB interface

The individual states of the state machine operation are described in the following sections:

- *ST_IDLE*
- *ST_READ* on page 4-7
- *ST_WWAIT* on page 4-7
- *ST_WRITE* on page 4-7
- *ST_WRITEP* on page 4-8
- *ST_RENABLE* on page 4-8
- *ST_WENABLE* on page 4-8
- *ST_WENABLEP* on page 4-9.

ST_IDLE

During this state the APB buses and **PWRITE** are driven with the last values they had, and **PSEL** and **PENABLE** lines are driven LOW.

The ST_IDLE state is entered from:

- reset, when the system is initialized

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- ST_RENABLE, ST_WENABLE, or ST_IDLE, when there are no peripheral transfers to perform.

The next state is:

- ST_READ, for a read transfer, when the AHB contains a valid APB read transfer
- ST_WWAIT, for a write transfer, when the AHB contains a valid APB write transfer.

ST_READ

During this state the address is decoded and driven onto **PADDR**, the relevant **PSEL** line is driven HIGH, and **PWRITE** is driven LOW. A wait state is always inserted to ensure that the data phase of the current AHB transfer does not complete until the APB read data has been driven onto **HRDATA**.

The ST_READ state is entered from ST_IDLE, ST_RENABLE, ST_WENABLE, or ST_WENABLEP during a valid read transfer.

The next state is always ST_RENABLE.

ST_WWAIT

This state is needed because of the pipelined structure of AHB transfers, to allow the AHB side of the write transfer to complete so that the write data becomes available on **HWDATA**. The APB write transfer is then started in the next clock cycle.

The ST_WWAIT state is entered from ST_IDLE, ST_RENABLE, or ST_WENABLE, during a valid write transfer.

The next state is always ST_WRITE.

ST_WRITE

During this state the address is decoded and driven onto **PADDR**, the relevant **PSEL** line is driven HIGH, and **PWRITE** is driven HIGH.

A wait state is not inserted, because a single write transfer can complete without affecting the AHB.

The ST_WRITE state is entered from:

- ST_WWAIT, when there are no more peripheral transfers to perform
- ST_WENABLEP, when the currently pending peripheral transfer is a write, and there are no more transfers to perform.

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The next state is:
- ST_WENABLE, when there are no more peripheral transfers to perform
- ST_WENABLEP, when there is one more peripheral write transfer to perform.

ST_WRITEP

During this state the address is decoded and driven onto **PADDR**, the relevant **PSEL** line is driven HIGH, and **PWRITE** is driven HIGH. A wait state is always inserted, because there must only ever be one pending transfer between the currently performed APB transfer and the currently driven AHB transfer. See the write transfer timing diagrams in the *AMBA Specification (Rev 2.0)* for more details.

The ST_WRITEP state is entered from:

- ST_WWAIT, when there is a further peripheral transfer to perform.
- ST_WENABLEP, when the currently pending peripheral transfer is a write, and there is a further transfer to perform.

The next state is always ST_WENABLEP.

ST_RENABLE

During this state the PENABLE output is driven HIGH, enabling the current APB transfer. All other APB outputs remain the same as the previous cycle.

The ST_RENABLE state is always entered from ST_READ.

The next state is:
- ST_READ, when there is a further peripheral read transfer to perform
- ST_WWAIT, when there is a further peripheral write transfer to perform
- ST_IDLE, when there are no more peripheral transfers to perform.

ST_WENABLE

During this state the PENABLE output is driven HIGH, enabling the current APB transfer. All other APB outputs remain the same as the previous cycle.

The ST_WENABLE state is always entered from ST_WRITE.

The next state is:
- ST_READ, when there is a further peripheral read transfer to perform
- ST_WWAIT, when there is a further peripheral write transfer to perform
- ST_IDLE, when there are no more peripheral transfers to perform.

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ST_WENABLEP

A wait state is inserted if the pending transfer is a read because, when a read follows a write, an extra wait state must be inserted to allow the write transfer to complete on the APB before the read is started.

The ST_WENABLEP state is entered from:

- ST_WRITE, when the currently driven AHB transfer is a peripheral transfer
- ST_WRITEP, when there is a pending peripheral transfer following the current write.

The next state is:

- ST_READ, when the pending transfer is a read
- ST_WRITE, when the pending transfer is a write, and there are no more transfers to perform
- ST_WRITEP, when the pending transfer is a write, and there is a further transfer to perform.

4.1.4 System description

This section describes how the HDL code for the APB bridge is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This should be read in conjunction with the HDL code.

Figure 4-4 on page 4-10 shows the APB bridge module block diagram.

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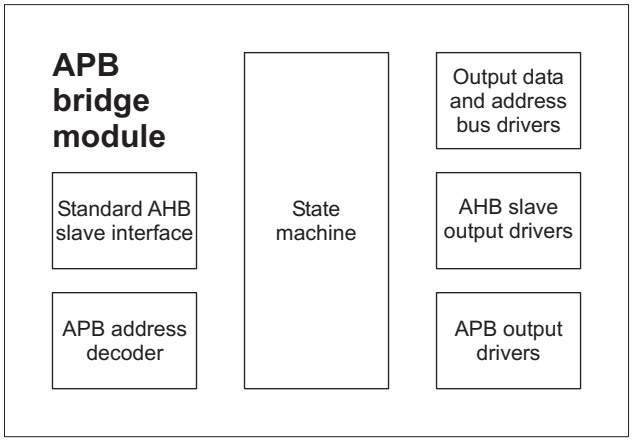

Figure 4-4 APB bridge module block diagram

The AHB to APB bridge comprises a state machine, which is used to control the generation of the APB and AHB output signals, and the address decoding logic which is used to generate the APB peripheral select lines.

All registers used in the system are clocked from the rising edge of the system clock **HCLK**, and use the asynchronous reset **HRESETn**.

Figure 4-5 on page 4-11 shows the APB bridge HDL file.

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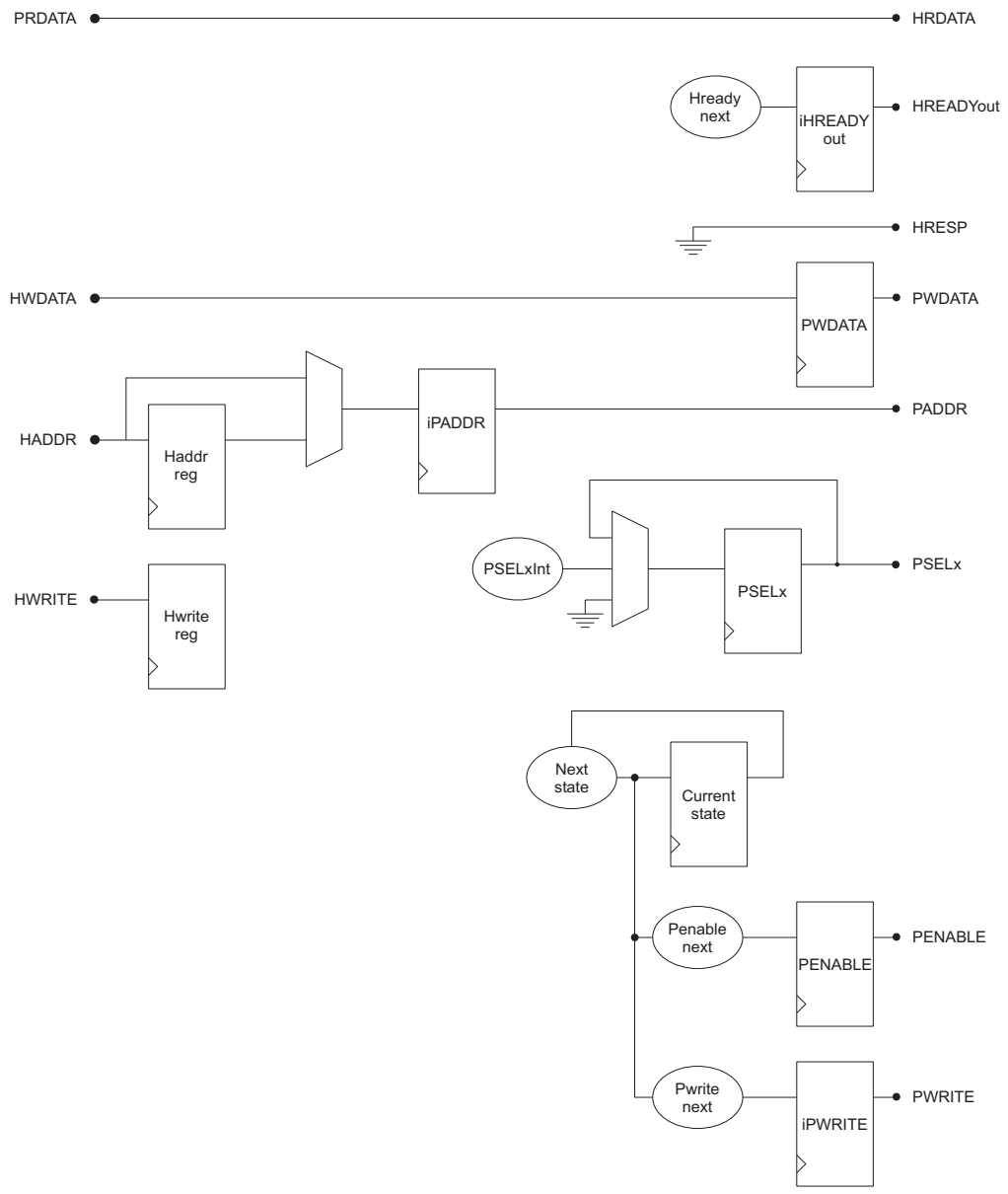

Figure 4-5 APB bridge module system diagram

The main sections in this module are explained in the following paragraphs:

- *Constant definitions* on page 4-12
- *AHB slave bus interface* on page 4-12

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- *APB transfer state machine*
- *APB output signal generation*
- *AHB output signal generation* on page 4-13.

Constant definitions

The constant PADDRWIDTH sets the width of the peripheral address bus that is used, up to a maximum of 32 bits. This size depends on the size of address that is needed by the peripherals in the system. The default value is a 16-bit address bus.

The next two constants define the state machine states, and the top four address bits that are used to decode the peripheral select outputs. If the peripheral address map is changed from the default, these constants must be modified to match the changes.

AHB slave bus interface

This module uses the standard AHB slave bus interface, which comprises:

- the valid transfer detection logic which is used to determine when a valid transfer is accessing the slave
- the address and control registers, which are used to store the information from the address phase of the transfer for use in the data phase.

Because of the different AHB to APB timing of read and write transfers, either the current or the previous address input value is needed to correctly generate the APB transfer. A multiplexor is therefore used to select between the current address input or the registered address, for read and write transfers respectively.

APB transfer state machine

The transfer state machine is used to control the application of APB transfers based on the AHB inputs. The state diagram in Figure 4-3 on page 4-6 shows the operation of the state machine, which is controlled by its current state and the AHB slave interface signals.

APB output signal generation

The generation of all APB output signals is based on the status of the transfer state machine:

- **PWDATA** is a registered version of the **HWDATA** input, which is only enabled during a write transfer. Because the bridge is the only bus master on the APB, it can drive **PWDATA** continuously.

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- **PENABLE** is only set HIGH during one of three enable states, in the last cycle of an APB transfer. A register is used to generate this output from the next state of the transfer state machine.
- The **PSELx** outputs are decoded from the current transfer address. They are only valid during the read, write and enable states, and are all driven LOW at all other times so that no peripherals are selected when no transfers are being performed.
- **PADDR** is a registered version of the currently selected address input (**HADDR** or the address register) and only changes when the read and write states are entered at the start of the APB transfer.
- **PWRITE** is set HIGH during a write transfer, and only changes when a new APB transfer is started. A register is used to generate this output from the next state of the transfer state machine.
- The **APBen** signal is used as an enable on the **PSEL**, **PWRITE** and **PADDR** output registers, ensuring that these signals only change when a new APB transfer is started, when the next state is **ST_READ**, **ST_WRITE**, or **ST_WRITEP**.

AHB output signal generation

A standard AHB slave interface consists of the following three outputs:

- **HRDATA** is directly driven with the current value of PRDATA. APB slaves only drive read data during the enable phase of the APB transfer, with PRDATA set LOW at all other times, so bus clash is avoided on HRDATA (assuming OR bus connections for both the AHB and APB read data buses).
- **HREADYout** is driven with a registered signal to improve the output timing. Wait states are inserted by the APB bridge during the ST_READ and ST_WRITEP states, and during the ST_WENABLEP state when the next transfer to be performed is a read.
- **HRESP** is continuously held LOW, because the APB bridge does not generate SPLIT, RETRY or ERROR responses.

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4.2 Arbiter

The AHB arbiter is responsible for determining which master is given access to the bus. At any time, only one master can perform transfers on the bus. The arbiter ensures this by sampling the request signals from the various masters in the system and then, using an arbitration priority scheme, determines which master is currently the highest priority.

4.2.1 Description

The arbiter is described in the following sections:

- *Arbitration process*
- *Burst operation* on page 4-15
- *Locked operation* on page 4-15
- *Split responses* on page 4-15
- *Default bus master* on page 4-15
- *Dummy bus master* on page 4-16
- *Locked operation and split responses* on page 4-16
- *Additional information* on page 4-16.

Arbitration process

The arbitration process consists of four stages, as shown in Figure 4-6:

1. The master requests access to the bus using **HBUSREQx**.
2. The **HGRANTx** signal is asserted, showing that the master is granted the bus when the current transfer completes.
3. The master owns the address/control signals.
4. The master owns the data bus.

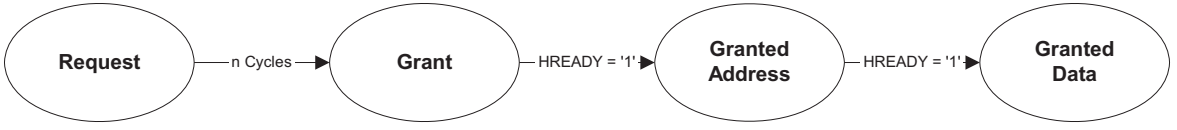

Figure 4-6 Arbitration process

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Burst operation

When a master is performing a fixed length burst (WRAP4, INCR4, WRAP8, INCR8, WRAP16, or INCR16), the master can lower its request signal when the burst has started. Therefore, the arbiter must include a counter which counts the transfer in the burst, enabling it to efficiently hand over ownership of the bus when the burst completes.

Locked operation

A master can assert the **HLOCK** signal so that the next transfers it performs on the bus is considered as a part of a locked sequence of transfers. This means that no other bus master is given access to the bus until the locked sequence has completed.

The master must deassert the **HLOCK** signal when the address phase of the last transfer in the locked sequence has started.

The arbiter asserts the **HMASTLOCK** signal during the address phase of all the transfers in the locked sequence. It is important that any slave which can issue either a SPLIT or RETRY response deals with a locked transfer as soon as possible, because no other master is given access to the bus until the locked transfer has completed.

At the end of a locked sequence of transfers the arbiter keeps the master granted on the bus until the data phase of the final locked transfer has completed. The arbiter can assert the **HGRANT** signal to another master when the final data phase is in progress. However, if the arbiter detects that the final data phase is going to complete with either a SPLIT or RETRY response, it must change **HGRANT** back to ensure that either the dummy master (in the case of a SPLIT) or the locked master (in the case of a RETRY) remains granted the bus.

Split responses

The arbiter has a special function that it must perform for transfers which receive a SPLIT response. The arbiter must ensure that the master which received the SPLIT response is not granted again until the slave has indicated that it is ready to complete the transfer (using the **HSPLITx** signals).

Default bus master

When no masters are requesting the bus, it can be granted to a default bus master. The default master has the advantage that, when it is granted the bus by default, it does not have to go through the Request/Grant stages before it can access the bus. It is recommended that the master which is most likely to use the bus is made the default master.

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Dummy bus master

The dummy bus master is a concept which enables the bus to remain synchronized when no real masters are granted the bus. The dummy master, when granted, simply drives the transfer type to IDLE, ensuring that the bus continues to operate. By convention, the dummy master is master number 0.

Locked operation and split responses

The desired operation of the arbiter when a locked bus master receives a SPLIT response is to grant the dummy bus master (which only performs IDLE transfers) until the master is unsplit and can return to the bus to complete the locked transfer. A dedicated section of the arbiter is used to detect a SPLIT response on a locked bus master. This forces the **HGRANT** and **HMASTER** outputs to grant the dummy bus master until the master is unsplit.

Additional information

The following is applicable during the arbitration process:

- It is possible to be granted the bus without requesting it. This occurs if the master is the default master, which is granted the bus when no other master is requesting.
- The above point also means that it is possible to be granted the bus in the same cycle that it is requested. This can occur if the master is coincidentally granted the bus in the same cycle that it asserts its request signal.
- It is possible that the **Grant** signal is asserted and then removed before the current transfer completes. This can happen during a transfer with a large number of wait states, where only a low priority master is requesting the bus during the early stages of the transfer, but a higher priority master then asserts its request before the current transfer has completed. This process is acceptable because the **Grant** signal is only sampled by masters when **HREADY** is HIGH.
- At the end of an undefined length burst, the master can drop its request signal when it has been granted the bus to start the last transfer in the burst. If the penultimate transfer in the burst is zero wait state, the master remains granted the bus for an additional transfer at the end of the sequence.

4.2.2 Arbiter signal interface

Figure 4-7 on page 4-17 shows the signal interface of the arbiter.

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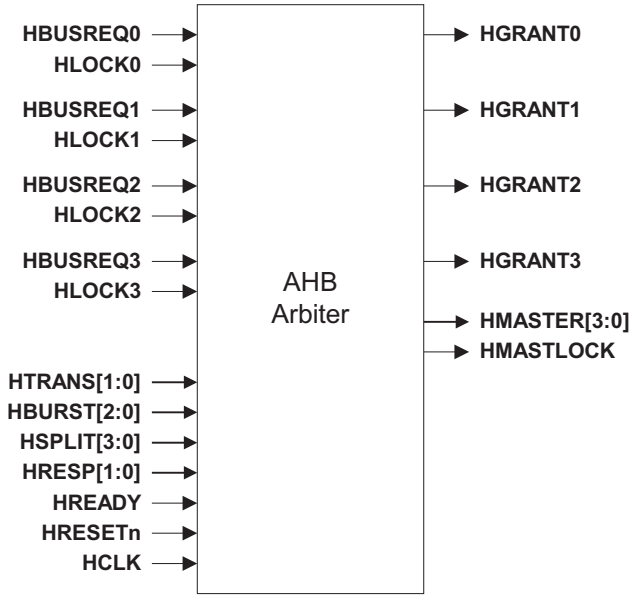

Figure 4-7 Signal interface

Table 4-2 describes the signals used in the arbiter.

Table 4-2 Signal descriptions for arbiter

Signal	Direction	Description
HCLK	Input	Bus clock.
HRESETn	Input	Bus reset.
HREADY	Input	Transfer done. When HIGH, indicates that the current transfer on the bus is complete.
HRESP[1:0]	Input	The transfer response provides additional information on the status of a transfer. Four different responses are available, OKAY, ERROR, RETRY, and SPLIT.
HSPLIT[3:0]	Input	The split bus is used by a slave to indicate to the arbiter which bus masters are allowed to reattempt a split transaction. Each bit of this split bus corresponds to a single bus master.
HBURST[2:0]	Input	Indicates if the transfer forms part of a burst. Four, eight, and sixteen beat bursts are supported. The burst can be either incrementing or wrapping.
HTRANS[1:0]	Input	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE, or BUSY.

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Table 4-2 Signal descriptions for arbiter (continued)

Signal	Direction	Description
HBUSREQx	Input	Request from bus master x to the arbiter which indicates that the bus master requires the bus masters.
HLOCKx	Input	When HIGH, this signal indicates that a master requires locked access to the bus and no other master must be granted the bus until this signal is LOW.
HGRANTx	Output	This signal indicates that bus master x is currently the highest priority master. Ownership of the address/control signals changes at the end of a transfer when **HREADY** is HIGH, so a master gets access to the bus when both **HREADY** and **HGRANTx** are HIGH.
HMASTER[3:0]	Output	These signals from the arbiter indicate which bus master is currently performing a transfer and is used by slaves which support split transfers to determine which master is attempting an access. The timing of **HMASTER** is aligned with the timing of the address and control signals.
HMASTLOCK	Output	Indicates that the current master is performing a locked sequence of transfers. This signal has the same timing as the **HMASTER** signals.

4.2.3 Operation

The basic operation of the arbiter is to sample the **HBUSREQ** inputs from each of the masters in the system and determine which is currently the highest priority master requesting the bus. The output of the priority logic is a 4-bit encoding, which represents the master number of the highest priority master requesting the bus.

If no other master is actively using the bus, the output of the priority logic is decoded and used to generate the **HGRANT** outputs. The **HGRANT** outputs indicate which master drives the address and control signals after the current transfer has completed, as indicated by **HREADY** being HIGH.

The usual process for determining which master is granted is to use the output from the priority logic. However, under the following circumstances the arbiter keeps the current bus master granted irrespective of the **HBUSREQ** inputs:

- when the current master is in the middle of a fixed length burst.
- when the current master is performing a locked transfer.

Figure 4-8 on page 4-19 shows the generation of the **HGRANT** and **HMASTER** signals.

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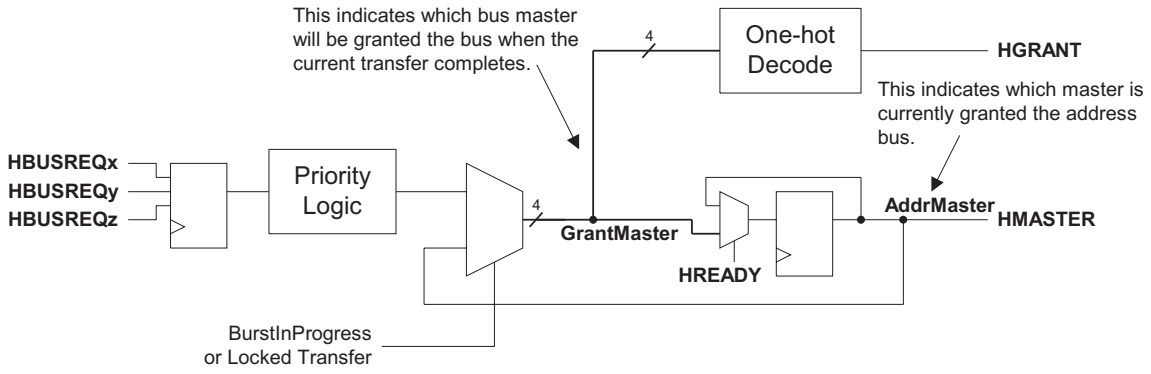

Figure 4-8 HGRANT and HMASTER generation

The following signals are used in the arbiter:

GrantMaster Indicates the number of the master whose **HGRANT** signal is currently asserted.

AddrMaster Gives the number of the master that is currently driving the address/control signals. This is the same as the **HMASTER** output.

DataMaster Gives the number of the master that currently owns the data bus and is either driving the write data bus or is reading from the read data bus.

The relationship between these signals is shown in Figure 4-9. This diagram represents the pipelined nature of the bus, and shows how the pipeline is advanced when the **HREADY** signal is HIGH.

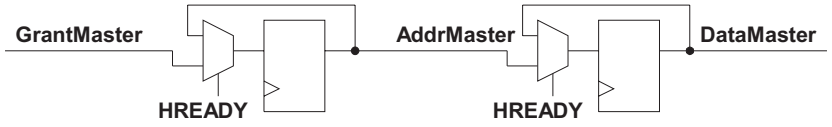

Figure 4-9 Signal relationships

Arbitration priority scheme

The arbiter is supplied with a fixed priority scheme:

- **HBUSREQ(3)** is the highest priority.

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- **HBUSREQ(0)** is the second highest priority. This must only be connected to a **Pause** input.
- **HBUSREQ(2)** is the middle priority.
- **HBUSREQ(1)** is the lowest priority and default bus master. This is usually used for an uncached ARM core.

Bus master 0 is reserved for the dummy bus master, which never performs real transfers. This master is granted either when the **Pause** input is asserted, or when the current master is performing a locked transfer which has received a split response.

If required, this priority scheme can be updated by changing the logic which takes the masked version of the **HBUSREQ** signals, called Request, and generates the 4-bit encoded master number, called TopRequest.

Locked operation

The arbiter also has to deal with locked operations. A bus master is considered to have locked access to the bus if the master has its **HLOCK** signal asserted to the arbiter at the point when it is granted access. The master must then remain the only granted master until its **HLOCK** signal is deasserted.

The logic required to implement locked operation is added to Figure 4-10 on page 4-21. A single output, called **HMASTLOCK**, is used to indicate when a master has locked access to the bus. This output is generated by selecting the appropriate **HLOCK** input, depending on which master is granted the bus in the next cycle.

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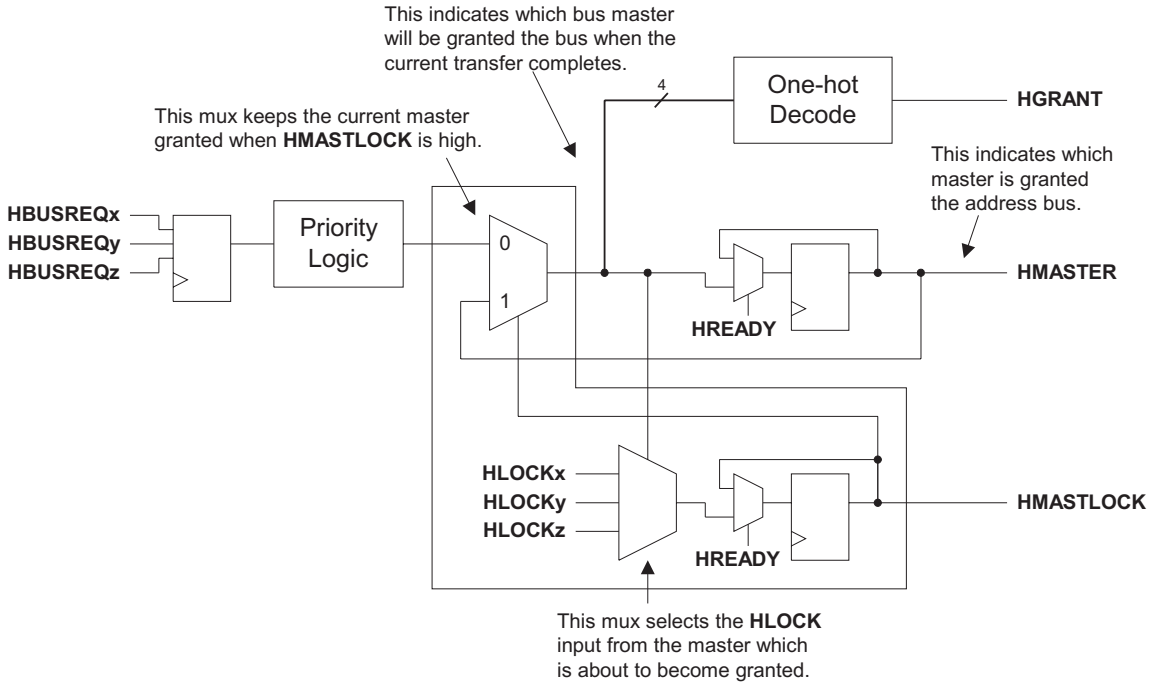

Figure 4-10 Locked transfers

The **HMASTLOCK** output is then used within the arbiter to force the next granted master to be the same as the currently granted master, effectively locking the master on the bus. The master then remains granted until it deasserts the lock.

Split responses

The arbiter performs a special function for transfers which receive a SPLIT response. The arbiter must ensure that the master which received the SPLIT response is not granted again until the slave has indicated that it is ready to complete the transfer (using the **HSPLITx** signals). To implement the split response function, the arbiter requires a mask register with one bit in the register for each bus master in the system.

Whenever a master receives a SPLIT response, the appropriate bit in the SplitMask register is set and, when the slave indicates that the particular master is able to complete, the appropriate bit in the SplitMask register is cleared. Figure 4-11 on page 4-22 shows the split logic.

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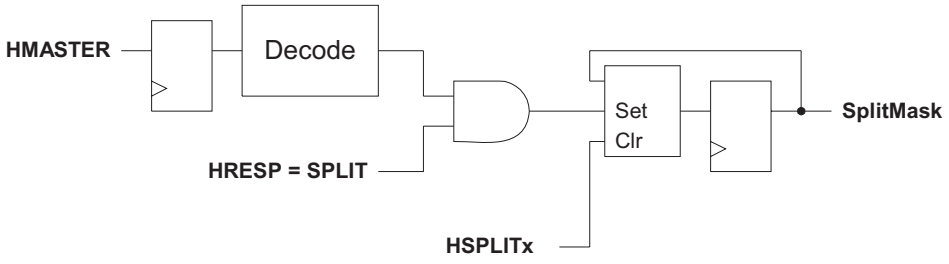

Figure 4-11 Split logic

On the input to the arbiter, the SplitMask register is used to mask out any incoming request signals from masters which have received a SPLIT response.

The required operation of the arbiter when a locked bus master receives a SPLIT response is to grant a dummy bus master (which only performs IDLE transfers) until the master is unsplit and can return to the bus to complete the locked transfer. A dedicated section of the arbiter is used to detect a SPLIT response on a locked bus master. This forces the **HGRANT** and **HMASTER** outputs to grant the dummy bus master until the master is unsplit.

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4.3 Decoder

The system decoder is used to decode the address bus and generate select lines to each of the system bus slaves, indicating that a read or write access to that slave is required. Figure 4-12 shows the decoder module interface block diagram.

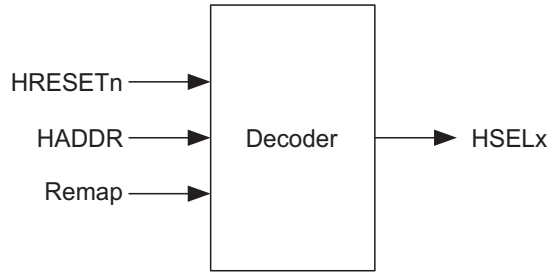

Figure 4-12 Decoder module interface diagram

This module only contains a combinatorial decode of the system address bus, using the **Remap** input to control the selection of the internal and external memory.

4.3.1 Signal description

Table 4-3 shows the signal descriptions for the decoder module

Table 4-3 Decoder module signal descriptions

Signal	Type	Direction	Description
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.
Remap	Reset memory map	Input	When LOW, the internal memory is not part of the system memory map, and external memory is mapped from address `0x00000000` which normally contains the system startup code. In normal operation this signal is HIGH, allowing use of the internal memory.
HSELx	Slave select	Output	Slave select to each system bus slave.

4.3.2 System memory map

The decoder controls the memory map of the system, and generates a slave select signal for each memory region.

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The **Remap** signal is used to provide a different memory map at reset, when ROM is required at address `0x00000000`, and during normal operation, when internal RAM can be used at address `0x00000000`.

The **Remap** signal is typically provided by a remap and pause peripheral, which drives **Remap** LOW at reset. The signal is driven HIGH only after a particular address in the remap and pause peripheral is accessed.

Figure 4-13 shows both the normal and reset memory maps.

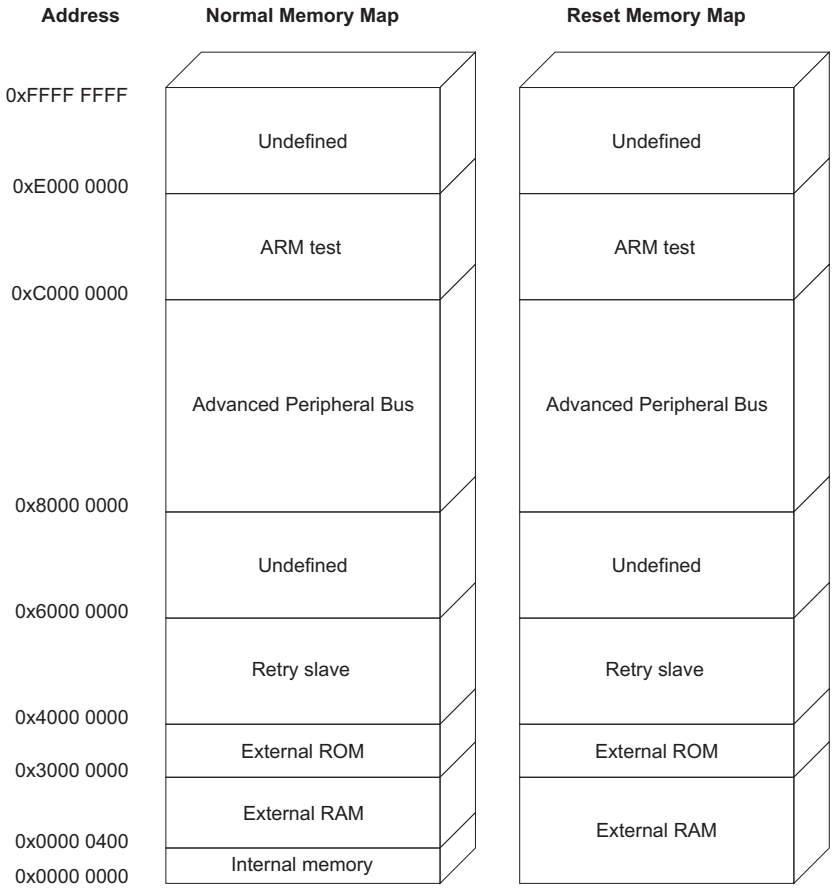

Figure 4-13 System memory map

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4.3.3 Function and operation of the decoder module

The decoder continuously performs a combinatorial decode of the system address bus, updating the slave select outputs whenever the address or system **Remap** inputs change value. The default slave is used to control the operation of the system when a transfer is made to an undefined area of memory, and is selected when an invalid address is generated.

4.3.4 System description

The following paragraphs give a description of how the HDL code for the decoder is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the inputs, and outputs used in the module. This part should be read together with the HDL code. Figure 4-14 shows the decoder module block diagram.

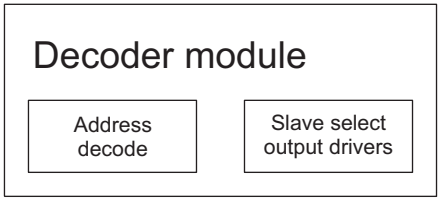

Figure 4-14 Decoder module block diagram

The decoder comprises a simple block of combinational logic, which is used to decode the address and system remap inputs to directly generate the slave select outputs. Figure 4-15 shows the decoder HDL file.

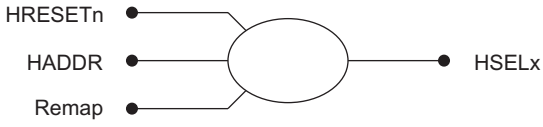

Figure 4-15 Decoder module system diagram

The whole of the decode logic is contained in one `if` statement. During reset, the default slave is selected, and at all other times, the **HADDR** and **Remap** inputs are decoded and used to generate the **HSELx** outputs.

The minimum number of address bits needed to select a slave are used, keeping the combinational logic as small as possible.

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This section of code is used to define the memory map for the whole system. If modules are added, removed, or moved to new locations, the code must be modified to match these system changes, ensuring that the correct slave is selected for each address used.

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4.4 Default slave

The default slave is used to respond to transfers that are made to undefined regions of memory, where no AHB system slaves are mapped. A zero wait OKAY response is made to IDLE or BUSY transfers, with an ERROR response being generated if a NONSEQUENTIAL or SEQUENTIAL transfer is performed. Figure 4-16 shows the default slave module interface diagram.

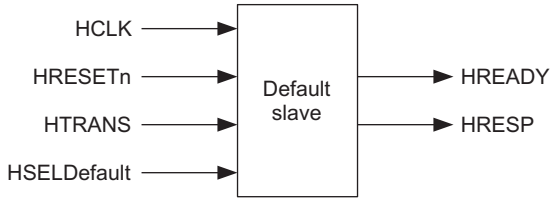

Figure 4-16 Default slave module interface diagram

This module contains a standard AHB slave response interface, using the **HREADY** and **HRESP** outputs to respond to transfers.

4.4.1 Signal descriptions

Table 4-4 shows the signal descriptions for the default slave module

Table 4-4 Default slave module signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HTRANS[1:0]	Transfer type	Input	Indicated the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HSEL	Default slave select	Input	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave. This signal is simply a combinatorial decode of the address bus.
HREADYout	Transfer done	Output	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal is only driven LOW to generate a two cycle error response.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module only generates the OKAY and ERROR responses.

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4.4.2 Function and operation of module

The default slave only responds to transfers when it is selected by the decoder with the **HSEL** input when an undefined region of memory is accessed. The response generated depends on the type of transfer that is performed.

If an IDLE or BUSY transfer is performed, the default slave must provide a zero wait OKAY response because the master does not expect to receive any data back from these transfers.

If a NONSEQUENTIAL or SEQUENTIAL transfer is performed, an ERROR response is generated, because there is nothing at the current location that can be written to or read from. The standard two-cycle ERROR response is provided with one wait state.

4.4.3 System description

This section describes how the HDL code for the default slave is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This should be read together with the HDL code.

Figure 4-17 shows the default slave module block diagram.

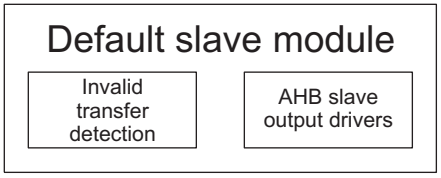

Figure 4-17 Default slave module block diagram

The default slave comprises the invalid transfer detection logic and two simple sets of combinational logic and registers, which are used to generate the **HREADY** and **HRESP** outputs.

Figure 4-18 on page 4-29 shows the decoder HDL file.

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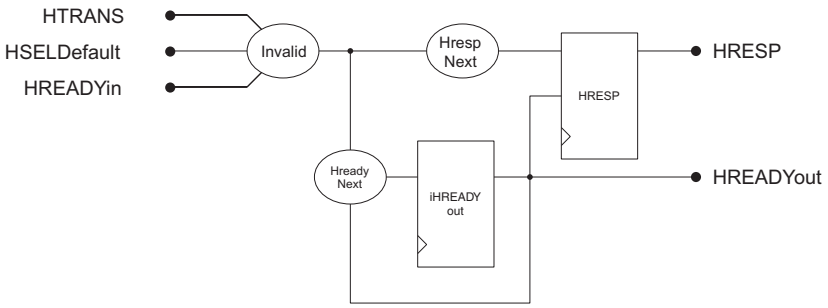

Figure 4-18 Default slave module system diagram

The internal signal Invalid is set HIGH during the final cycle of the address phase of an invalid transfer (when **HREADYin** is set HIGH, a NONSEQUENTIAL or SEQUENTIAL transfer is performed, and the default slave is selected), and is set LOW at all other times.

This signal is then passed to the response generation logic, which is split into two sections for the **HREADYout** and **HRESP** outputs. This logic generates the response values for the output registers. **HREADYout** is set LOW during the first cycle of the data phase, as is required for the two cycle ERROR response, and **HRESP** is set to ERROR for the two-cycles of the data phase.

At all other times, the default slave generates a zero wait OKAY response.

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4.5 Master to slave multiplexor

The master to slave multiplexor is used to connect all of the system bus masters to the bus slaves, using the current **HMASTER** number to select the bus master outputs to use. It is also used to generate the default master outputs when no other masters are selected. Figure 4-19 shows an interface diagram of the master to slave multiplexor module.

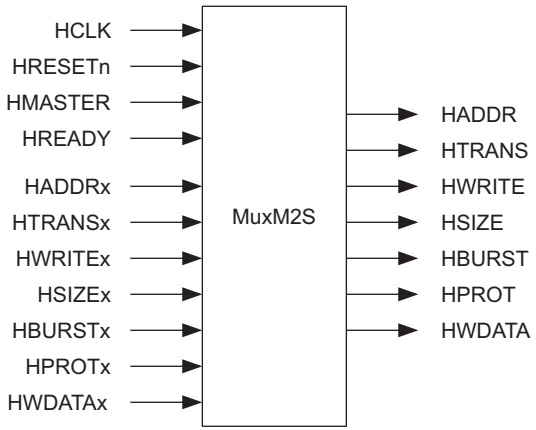

Figure 4-19 Master to slave multiplexor module interface diagram

The module has the address, control and data outputs of all system bus masters as its inputs, and has a single set of these signals as its outputs, which are connected to the inputs of all system slaves. When masters are added to, or removed from the system, the input connections to this module must be altered to account for the changes.

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4.5.1 Signal descriptions

Table 4-5 lists signal descriptions for the master to slave multiplexor module

Table 4-5 Master to slave multiplexor signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HMASTER[3:0]	Master number	Input	These signals from the arbiter indicate which bus master is currently performing a transfer, and is used by slaves which support split transfers to determine which master is attempting an access.
HREADY	Transfer done	Input	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HADDRx[31:0] **HADDR[31:0]**	Address bus	Input/ output	The 32-bit system address bus.
HTRANSx[1:0] **HTRANS[1:0]**	Transfer type	Input/ output	These signals indicate the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITEx **HWRITE**	Transfer direction	Input/ output	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.
HSIZEx[2:0] **HSIZE[2:0]**	Transfer size	Input/ output	These signals indicate the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
HBURSTx[2:0] **HBURST[2:0]**	Burst type	Input/ output	These signals indicate if the transfer forms part of a burst. Both four beat and eight beat bursts are supported and the burst can be either incrementing or wrapping.
HPROTx[3:0] **HPROT[3:0]**	Protection control	Input/ output	The protection control signals provide additional information about a bus access and are primarily intended for use by any module that wishes to implement some level of protection.
HWDATAx[31:0] **HWDATA[31:0]**	Write data bus	Input/ output	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended, however this can easily be extended to allow for higher bandwidth operation.

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4.5.2 Function and operation of module

The master to slave multiplexor controls the routing of address, control and data signals from the system bus masters to the bus slaves. The arbiter determines which master currently has control of the bus, and the multiplexor is used to connect the outputs of the selected master to the inputs of the bus slaves.

The address and control signals are switched during the address phase of a transfer using the **HMASTER** arbiter output.

The write data signals are switched during the data phase of a transfer using a registered version of **HMASTER**.

When no masters are selected, the default master signals are selected and the module drives all outputs LOW, performing IDLE transfers until another master is granted control of the bus.

4.5.3 System description

This section describes how the HDL code for the master to slave multiplexor is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This should be read together with the HDL code.

Figure 4-20 shows the master to slave module block diagram.

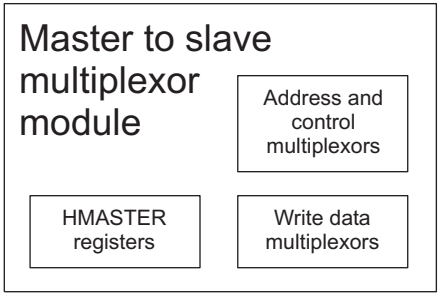

Figure 4-20 Master to slave multiplexor module block diagram

The master to slave multiplexor module comprises a set of multiplexors for each address, control and data output from the system bus masters. A set of registers is also used to hold the previous value of the **HMASTER** input.

Figure 4-21 on page 4-33 shows the master to slave multiplexor HDL file.

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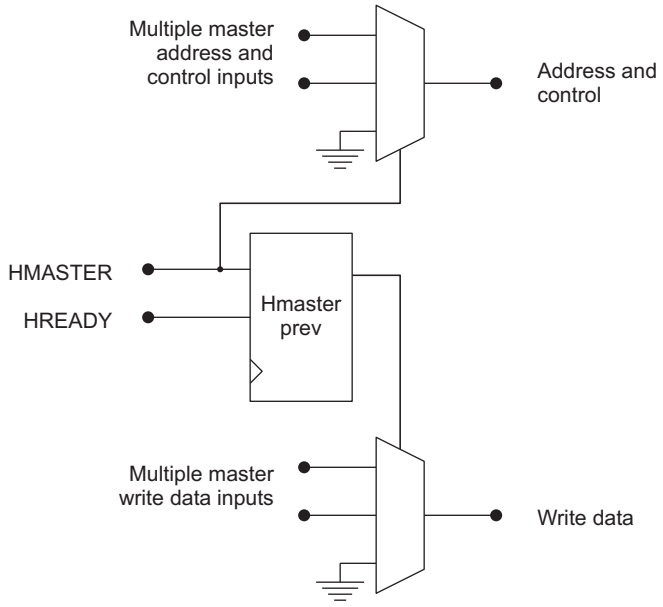

Figure 4-21 Master to slave multiplexor module system diagram

The multiplexor for each master signal has an input for each system bus master, and a ground connection for the default master signal values. The master number is decoded, and used to select the correct input signal.

The multiplexors are constructed using case statements, ensuring that there is no priority to the master selection logic.

An **HREADY** enabled register is used to hold the previous value of **HMASTER**, because the **HWDATA** master outputs are always running one cycle behind the other address and control signals, because of the pipelined bus. The enable is used to ensure that the value is only updated when the previous transfer has completed.

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4.6 Slave to master multiplexor

The slave to master multiplexor is used to connect the read data and response signals of the system bus slaves to the bus masters, using the current decoder **HSELx** outputs to select the bus slave outputs to use. Figure 4-22 shows the slave to master multiplexor module.

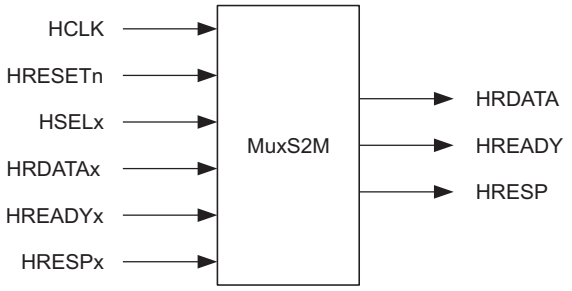

Figure 4-22 Slave to master multiplexor module interface diagram

This module has the read data and response outputs of all system bus slaves as its inputs, and has a single set of these signals as its outputs, which are connected to the inputs of all system masters. When slaves are added to the system or removed, the input connections to this module must be altered to account for the changes.

4.6.1 Signal descriptions

Table 4-6 shows the signal descriptions for the slave to master multiplexor module.

Table 4-6 Slave to master multiplexor signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HSELx	Slave select	Input	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave.

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Table 4-6 Slave to master multiplexor signal descriptions (continued)

Signal	Type	Direction	Description
HRDATAx[31:0] **HRDATA[31:0]**	Read data bus	Input/ output	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
HREADYx **HREADY**	Transfer done	Input/ output	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESPx[1:0] **HRESP[1:0]**	Transfer response	Input/ output	The transfer response provides additional information on the status of a transfer.

4.6.2 Function and operation of module

The slave to master multiplexor controls the routing of read data and response signals from the system bus slaves to the bus masters. The decoder determines which is the currently selected slave, and the multiplexor is used to connect the outputs of the selected slave to the inputs of the bus masters.

The read data and response signals are switched during the data phase of a transfer, so a registered version of the slave select signals is used.

The default slave inputs are used when no other slaves are selected.

4.6.3 System description

This section describes how the HDL code for the slave to master multiplexor is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This part should be read together with the HDL code.

Figure 4-23 on page 4-36 shows the slave to master module block diagram.

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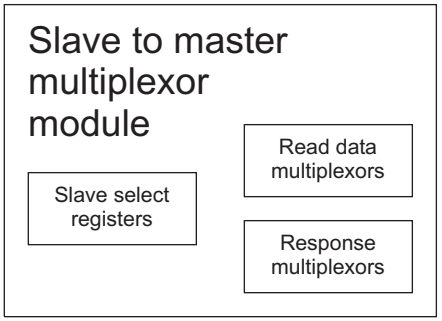

Figure 4-23 Slave to master multiplexor module block diagram

The slave to master multiplexor module comprises a set of registers to store the previous slave select values, and a set of multiplexors for the read data and slave response signals.

Figure 4-24 shows the slave to master multiplexor HDL file.

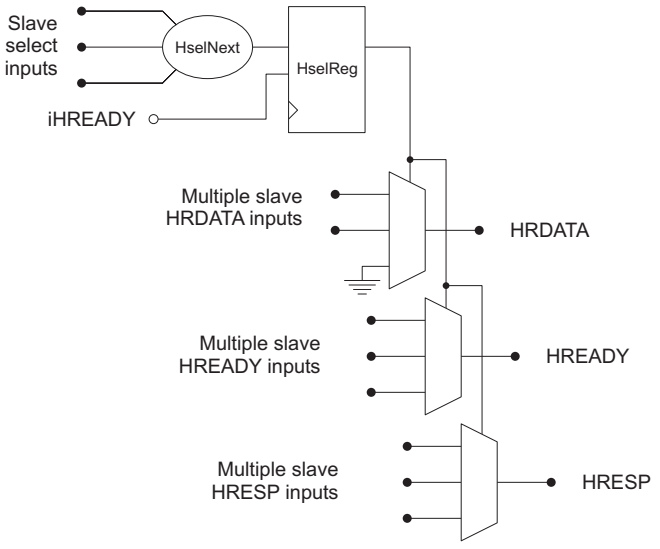

Figure 4-24 Slave to master multiplexor module system diagram

To allow the use of case statements for the multiplexors, the **HSEL** slave select inputs are combined to create a multi-bit bus signal. This bus is then registered, and used as the select control on the three multiplexors, one each for the read data and two response signals. The select register is enabled with the internal **HREADY** signal, ensuring that the outputs only change when the previous transfer has finished.

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Because the default slave does not generate any read data, one input to the **HRDATA** multiplexor is tied LOW, so that when the default slave is selected, no read data appears on **HRDATA**.

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4.7 Reset controller

The reset controller is used to generate the system reset signal from an external reset input as shown in Figure 4-25.

Figure 4-25 Reset controller module interface diagram

This module is based around a state machine, which is used to detect the external reset being asserted, and is used to generate the system reset output.

4.7.1 Signal descriptions

Table 4-7 shows the signal descriptions for the reset controller.

Table 4-7 Reset controller signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
POReset	Power-on reset	Input	Power-on reset input. This active LOW signal causes a cold reset when LOW. Can be asserted asynchronously to **HCLK**.
HRESETn	Reset	Output	The bus reset signal is active LOW, and is used to reset the system and the bus.

The source of the **POReset** signal is implementation-dependent.

4.7.2 Function and operation of module

HRESETn is asserted LOW, and is used to indicate a reset condition where all bus and system states must be initialized. This signal is suitable as an asynchronous clear into state machine flip-flops, and for resetting any peripheral registers that require initialization.

During reset, the arbiter grants the bus to the default reset bus master, and the decoder selects the default slave.

Assertion (the falling edge) of **HRESETn** is asynchronous to **HCLK**. De-assertion (the rising edge) of **HRESETn** is synchronous to the rising edge of **HCLK**. **HRESETn** is only asserted during a power-on reset condition, caused by the assertion of the **POReset** signal. The **POReset** input is an asynchronous input, so a synchronizing register is

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required to eliminate propagation of metastable values. Figure 4-26 shows the operation of the **HRESETn** signal with respect to an example **POReset** input signal and the system clock.

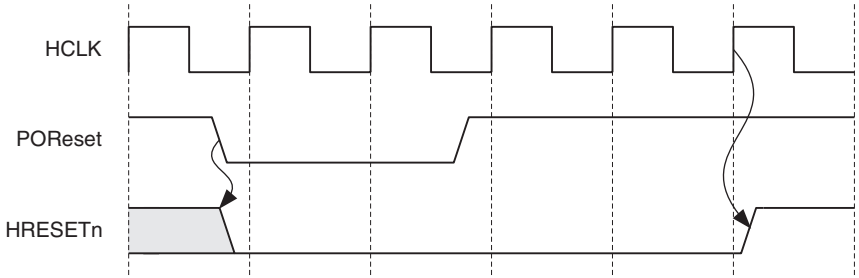

Figure 4-26 Reset signal timing

The reset controller contains a state machine running from the rising edge of **HCLK**. The **HRESETn** signal directly reflects a single bit of the current state, minimizing the combinational logic applied to the reset output.

Figure 4-27 on page 4-40 shows the state machine for the reset controller.

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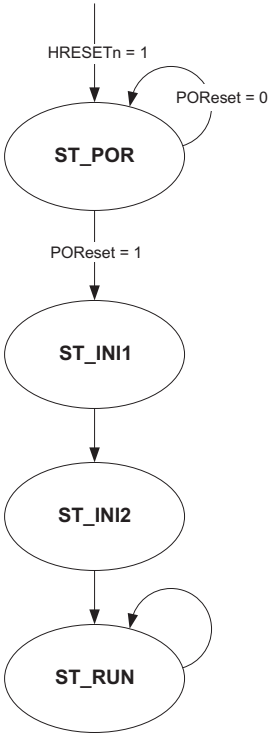

Figure 4-27 State machine for reset controller

The four states are described in:

- *ST_POR*
- *ST_INI1* on page 4-41
- *ST_INI2* on page 4-41
- *ST_RUN* on page 4-41.

ST_POR

During this state, the system is initialized when the reset line is asserted. This state must be preserved by a power on reset cell or controller, until the system bus clock is running and stable, and the system power supply has reached its correct operating voltage (within its allowed limits).

The ST_POR state is entered from:

- reset, when the external reset input is first asserted LOW
- ST_POR when the external reset input is still asserted and the system clock is running.

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The next state is:

- ST_INI1 when the external reset input is deasserted
- ST_POR when the external reset input is still asserted and the system clock is running.

If there is a clock valid signal in the system, this must be used to prevent the ST_POR state from being exited until the clock is valid.

ST_INI1

This state is used to hold the **HRESETn** output LOW for an extra cycle after the external reset is deasserted.

This state is always entered from ST_POR on the first rising edge of the clock that the external reset is HIGH.

The next state is always ST_INI2.

ST_INI2

This state is used in the same way as ST_INI1.

This state is always entered from ST_INI1.

The next state is always ST_RUN.

ST_RUN

This state is used during normal system operation when the **HRESETn** output is set HIGH.

This state is held until the external reset is re-asserted.

The default reset controller implementation asserts **HRESETn** for two cycles after the external reset is deasserted, but this can be altered by adding extra ST_INI states to the state machine, so that it takes more cycles to reach the final ST_RUN state.

4.7.3 System description

The following paragraphs give a description of how the HDL code for the reset controller is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This part should be read together with the HDL code.

Figure 4-28 on page 4-42 shows the reset controller module block diagram.

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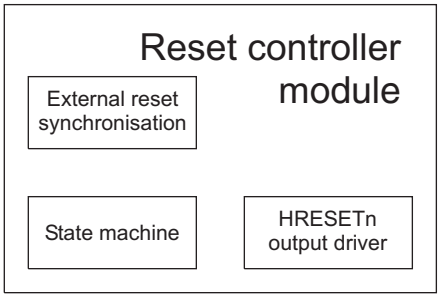

Figure 4-28 Reset controller module block diagram

The reset controller is comprised of a register used to synchronize the external reset input, and a state machine used to control the generation of the system reset output.

All registers used in the system are clocked from the rising edge of the system clock **HCLK**.

Figure 4-29 shows the reset controller HDL file.

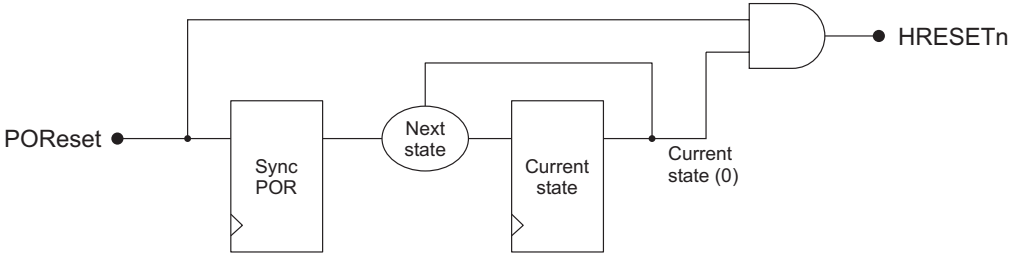

Figure 4-29 Reset controller module system diagram

The main sections in this module are explained in the following paragraphs:

- *Asynchronous reset input synchronization*
- *Reset state machine* on page 4-43
- *Reset output generation* on page 4-43.

Asynchronous reset input synchronization

The asynchronous external reset is first passed through a rising-edge-triggered register. This is to avoid metastability, because of the arrival time of the input relative to the system clock when used in the state machine.

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Reset state machine

The state machine shown in Figure 4-27 on page 4-40 is used to control the generation of the system reset output, based on the status of the synchronized external reset input and the system clock.

The number of cycles the module holds **HRESETn** asserted after the de-assertion of the external reset can be changed by altering the number of initialization states between the first and last states.

Reset output generation

The reset output is generated directly from bit 0 of the state machine registers, gated with the external reset input. This allows asynchronous assertion of the reset output when the external reset input is set LOW and the system clock is not running, but ensures that de-assertion is synchronous to the rising edge of the clock.

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4.8 Retry slave

The retry slave is a rudimentary module that is used to demonstrate how to build an AHB slave. The example contains very little functionality and consists of four 32-bit wide registers. The slave generates various logic functions of these registers, which can be read from different locations.

One of the most important features of the slave is that the response that it gives can be varied according to the high order address lines. Figure 4-30 shows the retry slave block diagram.

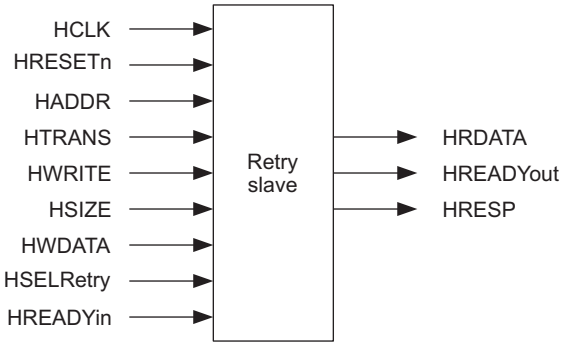

Figure 4-30 Retry slave block diagram

The main sections of this module are:

- the AHB slave bus interface
- the internal read/write registers
- the wait state and retry cycle generation logic
- the read data value generation.

4.8.1 Signal descriptions

Table 4-8 contains a list of signals used by the retry slave.

Table 4-8 Signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.

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Table 4-8 Signal descriptions (continued)

Signal	Type	Direction	Description
HTRANS[1:0]	Transfer type	Input	Indicated the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	Transfer direction	Input	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.
HWDATA[31:0]	Write data bus	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this can easily be extended to allow for higher bandwidth operation.
HSELRetry	Slave select	Input	Each AHB slave has its own slave select signal, and this signal indicates that the current transfer is intended for the selected slave. This signal is a combinatorial decode of the address bus.
HRDATA[31:0]	Read data bus	Output	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However this can easily be extended to allow for higher bandwidth operation.
HREADYin **HREADYout**	Transfer done	Input/output	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module only generates OKAY and RETRY responses.

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4.8.2 Function and operation of module

This example module contains four 32-bit wide registers, which can be accessed using byte, halfword or word, read or write transfers. Extra read only locations are provided that generate logical combinations of these four registers. The module memory map in Table 4-9 shows the logical functions that the slave can provide, and the addresses at which the functions and four read/write registers are accessed.

Table 4-9 Memory map of the example AHB retry slave

Address	Read location	Write location
0x00	R0	R0
0x04	R1	R1
0x08	R2	R2
0x0C	R3	R3
0x10	Not R0	-
0x14	R0 and R1	-
0x18	R1 or R2	-
0x1C	R2 xor R3	-
0x20	R0 and R1 and R2 and R3	-
0x24	R0 or R1 or R2 or R3	-
0x28	R0 xor R1 xor R2 xor R3	-

All addresses shown in the memory map are offsets from the module base address. In the default system the retry slave module occupies memory locations 0x40000000 to 0x5FFFFFFF.

When any of the memory locations are accessed, the high order address lines are used to determine the response that the slave provides, inserting wait states or retry cycles.

The address lines that are used are:

- **HADDR[11:8]**, number of wait states to be inserted
- **HADDR[13:12]**, number of times a retry response is generated.

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The number of wait states inserted for each read or write module access can be varied from 0 to 15, and the number of times the slave provides a retry response can be varied from 0 to 3.

When the slave is programmed to provide a retry response, the number of wait states to insert must be set to a value greater than zero, because all retry responses require two cycles, with a wait state inserted during the first cycle.

4.8.3 System description

The following paragraphs give a description of how the HDL code for the example retry slave is set out. A basic block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs and outputs used in the system. This part should be read together with the HDL code.

Figure 4-31 shows a basic block diagram of the retry slave module system.

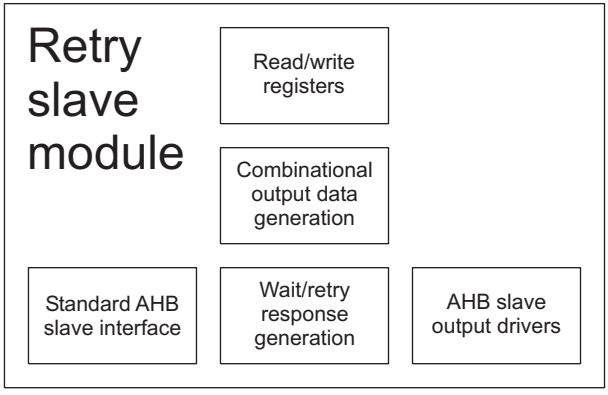

Figure 4-31 Retry slave module block diagram

The retry slave comprises a set of read/write registers, and programmable wait/retry generation logic.

All registers used in the system are clocked from the rising edge of the system clock **HCLK**, and use the asynchronous reset **HRESETn**.

Figure 4-32 on page 4-48 shows the retry slave HDL file.

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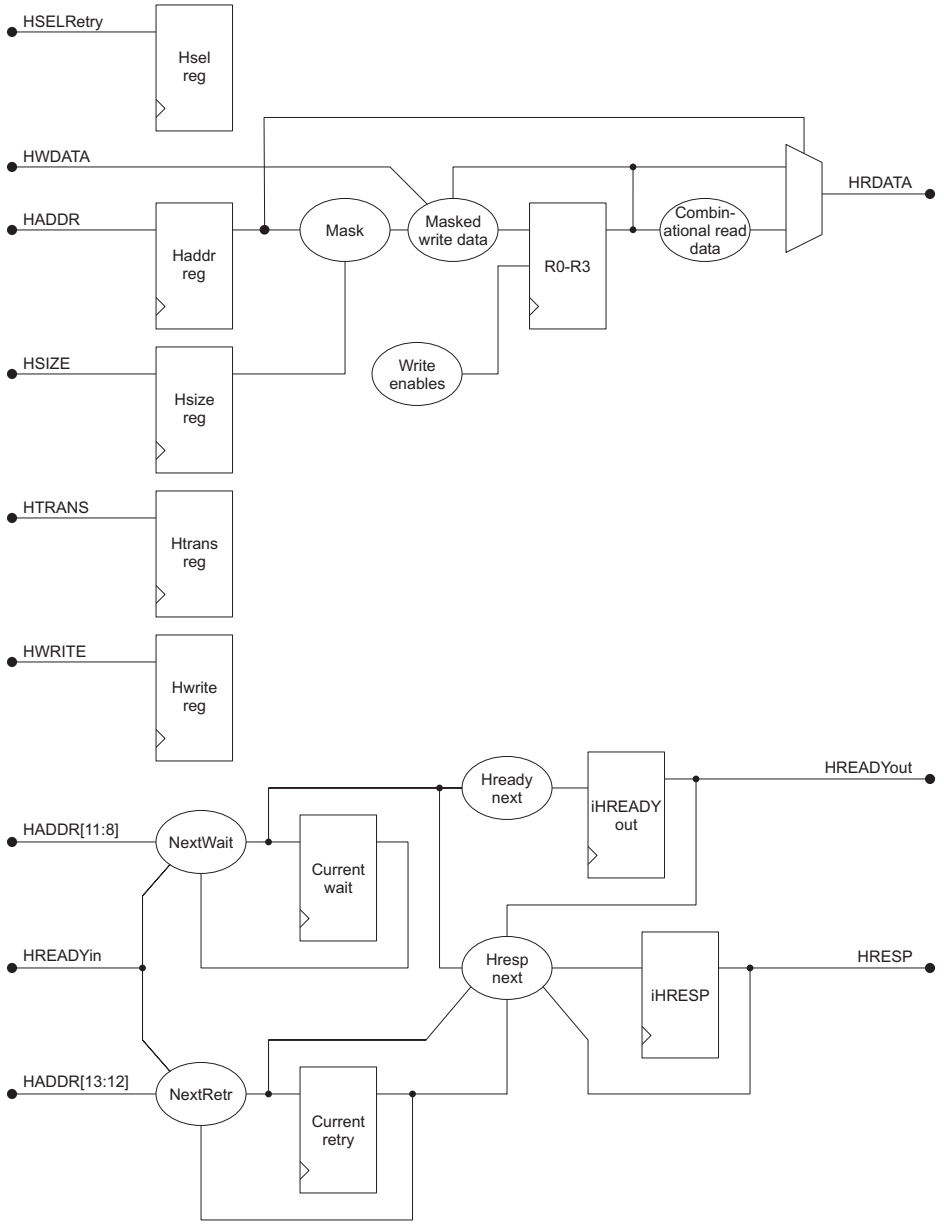

Figure 4-32 Retry slave module system diagram

The main sections in this module are explained in the following paragraphs:

- *AHB slave bus interface* on page 4-49

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- *Write data mask*
- *Read/write registers*
- *Response generation logic*
- *Read data generation* on page 4-50.

AHB slave bus interface

This module uses the standard AHB slave bus interface, which comprises the valid transfer detection logic, and the address and control registers, which are used to store the information from the address phase of the transfer for use in the data phase.

Write data mask

The amount of data written to the four internal registers depends on the transfer size setting. The mask is used to control which bytes of data are written to the 32-bit registers, and which bytes are left unchanged. A single mask value is used to allow one set of size decoding logic to be used for all registers in the module, rather than having a set of decoding logic for each register.

The bytes of data that change are set LOW in the mask, and all other bits are set HIGH.

Read/write registers

Four 32-bit registers are used to store user data, all initializing to zero. They are only enabled when addressed during a write transfer, and when any wait states or retry cycles have ended. The data mask is used to control writes of byte, halfword and word, by masking out the bits of the current write data that are not needed, and ORing it with a masked version of the current register data. This ensures that only the required bytes of the read data are used, and the unchanged register bytes are reloaded with the previous register value.

Response generation logic

This logic is used to control the generation of wait states and retry cycles.

Wait states are inserted when the address of the current transfer has a nonzero value in bits [11:8]. This value, from zero to fifteen, is loaded into the CurrentWait register, and then decremented each clock cycle until zero is reached. This counter value is used to hold the **HREADYout** output LOW until zero is reached, when **HREADYout** is set HIGH and the transfer can complete.

Retry cycles are inserted when the address of the current transfer has a nonzero value in bits [13:12] and [11:8], because all retry cycles require at least one wait state. This value is loaded into the CurrentRetry register, and is decremented each time the transfer is

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retried until zero is reached. The input to the iHRESP register is set according to the state of the retry logic and the wait logic, so that if more than one wait state is inserted, the **HRESP** output only changes during the last **HREADY** LOW cycle. Retry responses are generated until the counter reaches zero, when the **HRESP** output indicates that the transfer can complete normally.

Read data generation

Different read data values must be generated according to the address of the current transfer, selecting output data from one of the four registers or one of the seven combinational outputs. This section of the code selects a data source during the data phase of a valid transfer, and then directly drives the output data bus **HRDATA** with this selected data value.

This combinational output path allows a zero wait state response to be possible, because data written to a register can be read the following cycle with a zero wait state transfer. If a registered output data path is used, reads from registers that were written to in the previous cycle must have at least one wait state inserted, to allow for the internal data register to sample the write data, and then for the data register output to be sampled by the output read data register, before being driven onto the output read data bus.

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4.9 Static memory interface

The AMBA *Static Memory Interface* (SMI) is an example design which shows the basic requirements of an *External Bus Interface* (EBI) in an AMBA system. It is not intended to be a ready-made EBI for a real system. Such an EBI design would have to take process, package, and varying external delays into account.

The SMI connects the AMBA AHB to the external memory bus of an AMBA microcontroller. This allows the connection of up to three 256MB banks of 32-bit wide static memory (for example, SRAM and ROM) and also provides 32-bit test access to the AMBA system in conjunction with the TIC. Figure 4-33 shows the block diagram of the SMI.

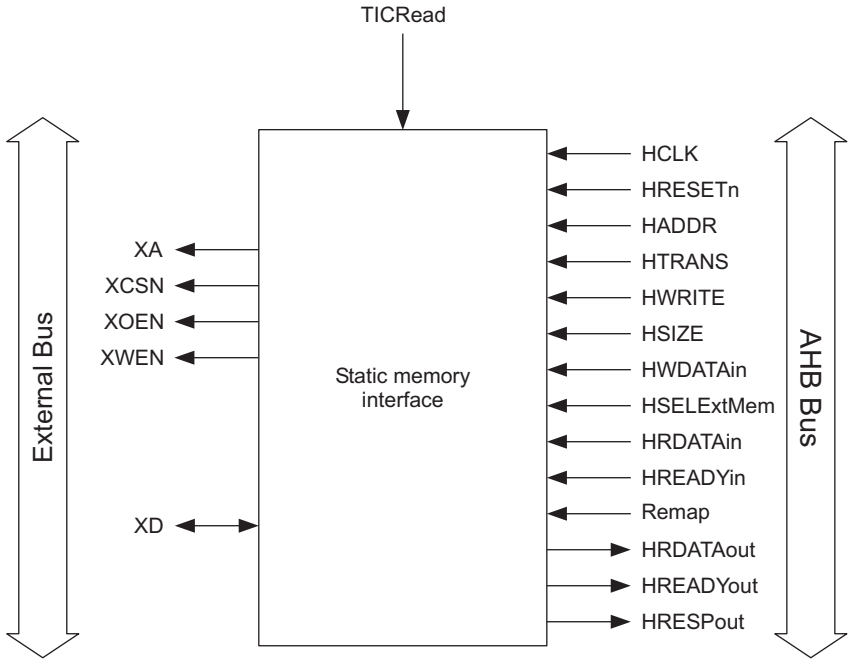

Figure 4-33 Static memory interface block diagram

The main sections of this module are:

- the AHB slave bus interface
- the data and address bus registers and drivers
- the external memory access control logic.

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4.9.1 Signal descriptions

Table 4-7 describes the signals used by the SMI.

Table 4-10 Signal descriptions

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.
HTRANS[1:0]	Transfer type	Input	This indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	Transfer direction	Input	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.
HSIZE[2:0]	Transfer size	Input	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
HWDATAin[31:0	Write data bus	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended, however, this can easily be extended to allow for higher bandwidth operation.
HSELExtMem	Slave select	Input	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave. This signal is a combinatorial decode of the address bus.
HRDATAin[31:0] **HRDATAout[31:0]**	Read data bus	Input/output	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended, however this can easily be extended to allow for higher bandwidth operation.
HREADYin **HREADYout**	Transfer done	Input/output	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module always generates the OKAY response.

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Table 4-10 Signal descriptions (continued)

Signal	Type	Direction	Description
Remap	Reset memory map	Input	When LOW, the internal memory is not part of the system memory map, and external memory is mapped from address `0x00000000`, which normally contains the system startup code. In normal operation this signal is HIGH, allowing use of the internal memory.
TicRead	Drive out read data	Input	This signal controls the SMI to drive the current read data from **HRDATA** to **XD**.
XD[31:0]	External data bus	Input/output	This is the bidirectional external data bus. In normal operation it is driven by the external bus when **XOEN** is LOW, and by this module when **XOEN** is HIGH. During system test this becomes the test bus **TESTBUS** and its direction is controlled by the TIC control signals.
XA[30:0]	External address bus	Output	The external address bus becomes valid during the **HCLK** LOW phase of the transfer and remains valid throughout the rest of the transfer.
XCSN[3:0]	External chip select	Output	These signals are active LOW chip enables for each of the three banks (0-1, 3) of static memory. **XCSN[3]** must be connected to the memory containing the startup program (boot ROM/BIOS) for the system.
XOEN	External output enable	Output	This is the output enable for devices on the external bus. This is LOW during reads from external memory, during which time the selected bank must drive the **XD** bus.
XWEN[3:0]	External write enable	Output	This is the active LOW memory write enable. For little-endian systems, **XWEN[0]** controls writes to the least significant byte and **XWEN[3]**, the most significant. The example system is configured to be little-endian. The SMI is configured to have a minimum of two wait states when writing to memory. **XWEN** is only valid during the second cycle of the write transfer.

4.9.2 Functional description of the SMI

The SMI has five functions in the example system described in the following paragraphs:

- *External bus control* on page 4-54
- *Memory bank select* on page 4-55
- *Memory write control* on page 4-56

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- *Configurable memory access wait states* on page 4-57
- *System test access* on page 4-57.

External bus control

To perform a read from external memory, **XOEN** must be LOW and the **XD** output is tristated, allowing it to be driven with read data by the external memory.

Figure 4-34 shows the timing of a read from memory with zero wait states.

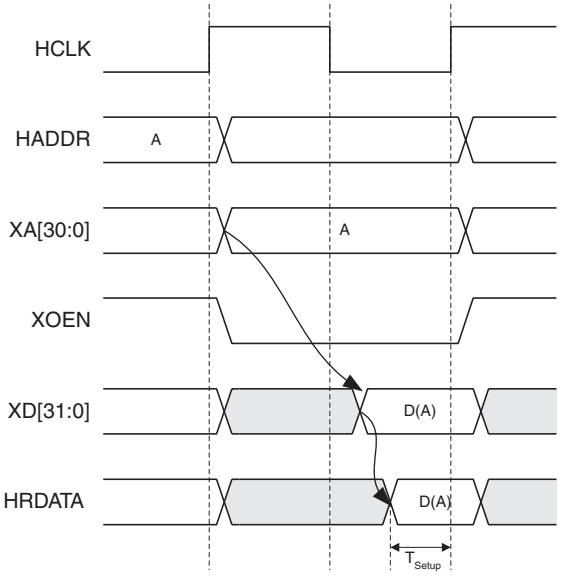

Figure 4-34 Zero wait memory read

Note

The data must be valid on the **XD** bus in time for the signal to propagate on-chip so that the **HRDATA** bus becomes valid before the next rising edge of **HCLK**. If this setup time cannot be achieved, the access requires wait states.

To perform a write to the external memory, **XOEN** must be HIGH, to allow **XD** to be driven by the SMI with a registered version of **HWDATA**.

The SMI requires at least two wait states to be added for a write to memory, to allow for the timing of the **XWEN** write enable signal relative to the **XA** and **XD** buses. When **XWEN** is LOW **XA** must be stable and, on the rising edge of **XWEN**, **XD** must be valid.

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Figure 4-35 shows the timing of a write to memory with two wait states.

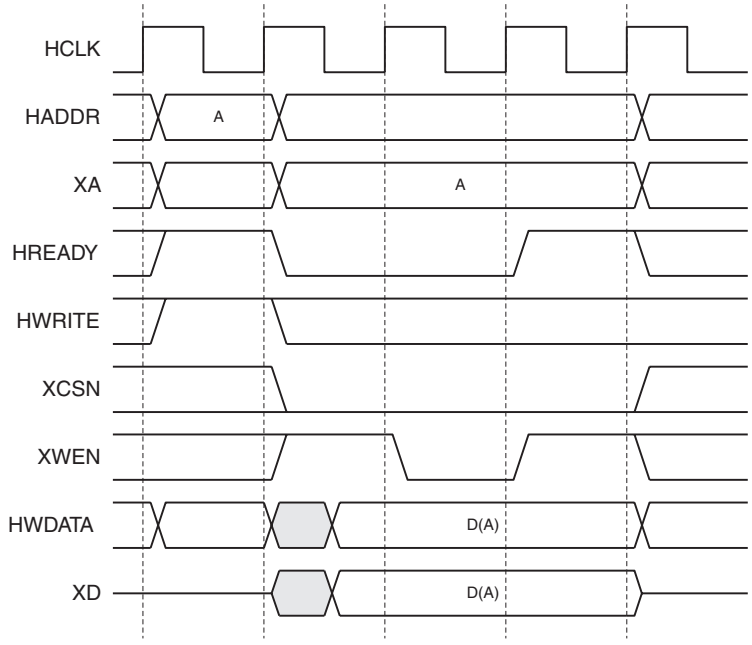

Figure 4-35 Memory write with two wait states

Memory bank select

The **XCSN** chip select lines are controlled by the address of a valid transfer, and the system memory map mode. Before the system memory is remapped, the boot ROM at `0x30000000` is also mapped to the base address of `0x00000000`.

Table 4-11shows the relationship between the inputs and the generated value of XCSN.

Table 4-11 XCSN coding

Input HSELExtMem	Input Remap	Input HADDR[29:28]	Output XCSN[3:0]
0	X	XX	1111
1	0	00	0111
1	0	01	1101
1	0	10	1011

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Table 4-11 XCSN coding (continued)

Input HSELExtMem	Input Remap	Input HADDR[29:28]	Output XCSN[3:0]
1	0	11	0111
1	1	00	1110
1	1	01	1101
1	1	10	1011
1	1	11	0111

XCSN is also held in the 1111 state asynchronously during reset.

Memory write control

The 4-bit **XWEN** write enable signal allows the four bytes in the 32-bit wide word to be written independently. The byte assignments are:

- **XWEN[0]** controls **XD[7:0]**
- **XWEN[1]** controls **XD[15:8]**
- **XWEN[2]** controls **XD[23:16]**
- **XWEN[3]** controls **XD[31:24]**.

The SMI controls **XWEN** for writes in word (32-bit), halfword (16-bit) and byte (8-bit) quantities. The SMI uses **HSIZE[1:0]** and **HADDR[1:0]** to select the width and order of each write to memory. This information must be valid before **XWEN** is asserted.

Table 4-12 shows the bytes selected according to the HSIZE and HADDR[1:0] inputs.

Table 4-12 XWEN coding

HSIZE[1:0]	HADDR[1:0]	XWEN[3:0]
10 (word)	XX	0000
01 (half word)	0X	1100
01 (half word)	1X	0011
00 (byte)	00	1110

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Table 4-12 XWEN coding (continued)

HSIZE[1:0]	HADDR[1:0]	XWEN[3:0]
00 (byte)	01	1101
00 (byte)	10	1011
00 (byte)	11	0111

Configurable memory access wait states

The SMI only supports global (the same for every bank) wait states for read and write accesses. This is configurable (in the HDL model, not in synthesized hardware) between zero and three waits for reads, and between two and three for writes. Figure 4-35 on page 4-55 shows a memory transfer with two wait states. A transfer with more wait states causes more wait cycles to be added. The external address and data information remains valid until the memory access cycle is completed. For writes, the **XWEN** signal is extended, going LOW during the first wait, and not going HIGH until the final cycle of the transfer. Before synthesis, the wait states can be configured by altering the 2-bit wide constants READWAIT and WRITEWAIT. WRITEWAIT must be value 2 or greater.

System test access

During system TIC testing, the external bus output of the SMI is controlled by the active HIGH **TicRead** signal from the TIC. This is used to pass read data from the **HRDATAin** bus onto the external test bus **XD**. During normal operation this signal is held LOW.

4.9.3 System description

The following paragraphs give a description of how the HDL code for the module is set out. A basic system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs and outputs used in the module. This part should be read together with the HDL code.

A basic block diagram of the static memory interface system is shown in Figure 4-36 on page 4-58.

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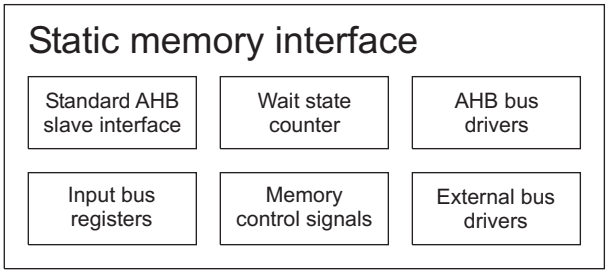

Figure 4-36 Static memory interface module block diagram

The static memory interface module comprises the input bus registers, the wait state counter used to insert wait states, and the external memory control signal generation.

All registers used in the system are clocked from the rising edge of the system clock **HCLK**, and use the asynchronous reset **HRESETn**.

Figure 4-36 shows the static memory interface HDL file.

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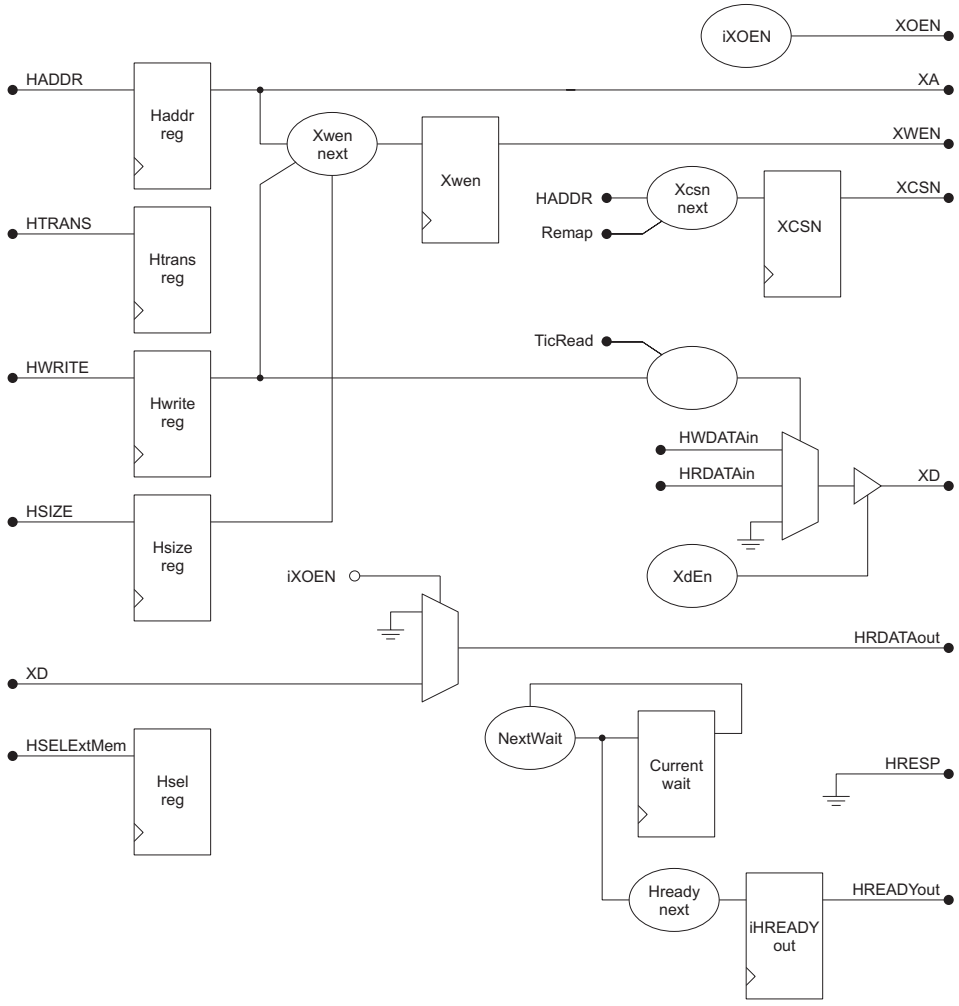

Figure 4-37 Static memory interface module system diagram

The main sections in the SMI module are explained in more detail in the following paragraphs:

- *Constant definitions* on page 4-60
- *AHB slave bus interface* on page 4-60
- *Wait state generation* on page 4-60
- *AHB output data bus generation* on page 4-60
- *External bus output generation* on page 4-61.

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Constant definitions

The constants READWAIT and WRITEWAIT are used to set the number of wait states that are inserted when a read and write transfer is performed. The value of zero to three for reads, and two to three for writes, is set for all transfers to all memory banks, and although configurable in the HDL code, it is permanently set when synthesized.

AHB slave bus interface

This module uses the standard AHB slave bus interface, which comprises:

- the valid transfer detection logic
- the address and control registers, which are used to store the information from the address phase of the transfer for use in the data phase.

The default address setting of the module is external RAM from `0x00000000` to `0x1FFFFFFF`, and external boot ROM from `0x30000000` to `0x3FFFFFFF`. When the **Remap** signal is HIGH, indicating that remapped memory is in use, external RAM is mapped from `0x00000400` to `0x1FFFFFFF`, with internal memory being mapped in the first `0x000` to `0x400` region.

Wait state generation

The counter register is used to insert wait states according to the values set in the READWAIT and WRITEWAIT constants. The counter is loaded with the relevant value when a read or write transfer begins, and decrements the value until no more wait states have to be added. The counter value is used to generate the input to the **HREADYout** register, which is set LOW while the counter is not zero.

AHB output data bus generation

The **HRDATAout** output is driven to **XD** during a normal external memory read transfer, to propagate the read data value from the external bus onto the AHB. **HRDATAout** is driven LOW at all other times.

The registered **HREADYout** output is driven LOW while the current value of the wait state counter is not zero.

The **HRESP** output is held LOW, because the SMI always generates an OKAY response to all transfers.

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External bus output generation

This section contains the signals that are driven onto the external bus:

- **XD** is generated from either the AHB read or write data buses, depending on the current system mode of operation. **HWDATAin** is used during a normal external memory write transfer, and **HRDATAin** is used during a TIC testing read cycle. Because **XD** is a tristate bus, it is only driven by the SMI when the current transfer is a standard write or a TIC testing read, allowing **XD** to be driven by any external modules at all other times.
- **XA** is driven with a registered version of bits [30:0] of **HADDR**, because the full system address range is not required on the external bus.
- **XCSN** is generated from the input address during a valid read or write transfer. Bits [29:28] of the address are decoded as shown in Table 4-8 on page -54. When **Remap** is LOW, the boot ROM is mapped at the base address, in addition to its standard address. External RAM access is not dependant on the **Remap** input. During reset, or when the memory is not addressed, all **XCSN** output bits are set HIGH to deselect all banks of external memory.
- **XOEN** is set LOW during a valid read transfer, and is set HIGH at all other times.
- **XWEN** is generated from the size and address settings for a write transfer, selecting the transfer size and byte lane to use, as shown in Table 4-9 on page -55. A registered output is used to avoid the generation of glitches, which can cause incorrect values to be written to the external ROM.

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4.10 Test interface controller

The *Test Interface Controller* (TIC) is a state machine that provides an AMBA AHB bus master for system test. It reads test write and address data from the external data bus **TESTBUS** (**XD**), and uses the *External Bus Interface* (EBI) to drive the external bus with test read data, allowing the use of only one set of output tristate buffers onto **TESTBUS**.

The TIC is used to convert externally applied test vectors into internal transfers on the AHB bus. A three-wire external handshake protocol is used, with two inputs controlling the type of vector that is applied and a single output that indicates when the next vector can be applied.

Typically the TIC is the highest priority AMBA bus master, which ensures test access under all conditions.

The TIC model supports address incrementing and control vectors. This means that the address for burst transfers can automatically be generated by the TIC.

Figure 4-38 shows the TIC module interface diagram.

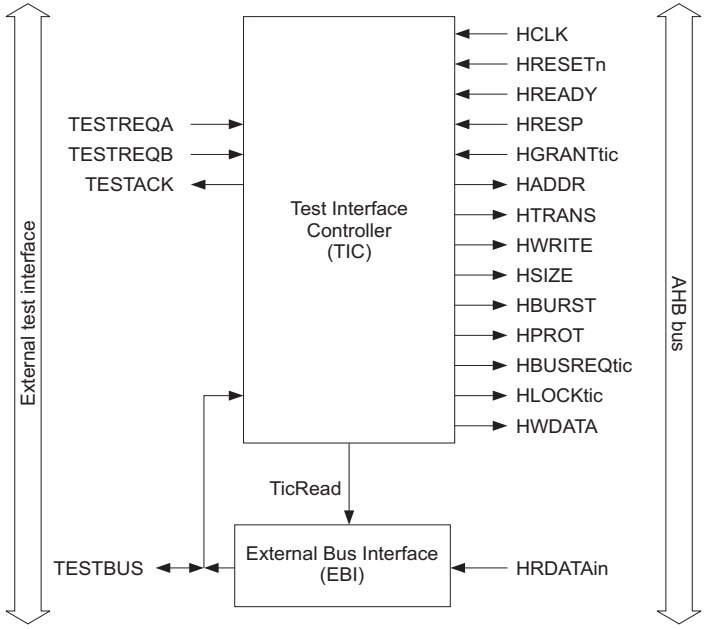

Figure 4-38 TIC module interface diagram

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Figure 4-38 on page 4-62 represents a TIC module in a system where the external data bus becomes the test bus when performing test mode accesses. 16-bit and 8-bit data bus systems require, for example, 16 or 24 address lines to be reconfigured as bidirectional test port signals for the test mode access.

4.10.1 Signal descriptions

The TIC has three primary interfaces:

- the AHB bus master interface, to control the operation of the system during test
- the external test interface, to read the type of vector being applied and control the application of new vectors
- the datapath interface, to control the operation of the EBI to drive the external data bus.

Table 4-13 shows the TIC module signal descriptions for an AHB-based system.

Table 4-13 TIC signal descriptions for AHB

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers. All signal timings are related to the rising edge of **HCLK**.
HRESETn	Reset	Input	The bus reset signal is active LOW and is used to reset the system and the bus. This is the only active LOW signal.
HADDR[31:0]	Address bus	Output	The 32-bit system address bus.
HTRANS[1:0]	Transfer type	Output	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL or IDLE. The TIC does not use the BUSY transfer type.
HWRITE	Transfer direction	Output	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HSIZE[2:0]	Transfer size	Output	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit). The TIC does not support larger transfer sizes.
HBURST[2:0]	Burst type	Output	Indicates if the transfer forms part of a burst. The TIC always performs incrementing bursts of unspecified length.
HPROT[3:0]	Protection control	Output	The protection control signals indicate if the transfer is an opcode fetch or data access, as well as if the transfer is a supervisor mode access or user mode access. These signals can also indicate whether the current access is cacheable or bufferable.

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Table 4-13 TIC signal descriptions for AHB (continued)

Signal	Type	Direction	Description
HWDATA[31:0]	Write data bus	Output	The write data bus is used to transfer data from the master to bus slaves during write operations. A minimum data bus width of 32 bits is recommended, however this can easily be extended to allow for higher bandwidth operation.
HREADY	Transfer done	Input	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Input	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.
HBUSREQtic	Bus request	Output	A signal from the TIC to the bus arbiter which indicates that it requires the bus.
HLOCKtic	Locked transfers	Output	When HIGH this signal indicates that the master requires locked access to the bus and no other master must be granted the bus until this signal is LOW.
HGRANTtic	Bus grant	Input	This signal indicates that the TIC is currently the highest priority master. Ownership of the address and control signals changes at the end of a transfer when **HREADY** is HIGH, so a master gains access to the bus when both **HREADY** and **HGRANTx** are HIGH.
TESTBUS	Test data bus	Input	This is the bidirectional external data bus. In normal operation it is driven by the external bus interface. During system test it becomes the test data bus and its direction is controlled by the test bus request A and B signals.
TESTREQA	Test bus request A	Input	This is the test bus request A input signal and is required as a dedicated device pin. During normal system operation the **TESTREQA** signal is used to request entry into the test mode. During test **TESTREQA** is used, in combination with **TESTREQB**, to indicate the type of test vector that is to be applied in the following cycle.

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Table 4-13 TIC signal descriptions for AHB (continued)

Signal	Type	Direction	Description
TESTREQB	Test bus request B	Input	During test this signal is used, in combination with **TESTREQA**, to indicate the type of test vector that is to be applied in the following cycle.
TESTACK	Test acknowledge	Output	The test bus acknowledge signal gives external indication that the test bus has been granted and also indicates when a test access has completed. When **TESTACK** is LOW the current test vector must be extended until **TESTACK** becomes HIGH.
TicRead	Drive out read data	Output	This signal controls the EBI to drive the current read data from **HRDATA** to **TESTBUS**.

4.10.2 Function and operation of module

The TIC operates as a standard AHB bus master during system test when the external test pins show that the system is required to enter test mode. In this mode, the TIC requests control of the AHB, and when granted uses the AHB to perform system tests.

Table 4-14 shows the operation of the external test pins to change the TIC mode from normal operation into test mode.

Table 4-14 Test control signals during normal operation

TESTREQA	TESTREQB	TESTACK	Description
0	-	0	Normal operation
1	-	0	Enter test mode request
-	-	1	Test mode entered

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During system test the external test pins are used to control the operation of the TIC. The operation of these pins is shown in Table 4-15.

Table 4-15 Test control signals during test mode

TESTREQA	TESTREQB	TESTACK	Description
-	-	0	Current access incomplete
1	1	1	Address vector or control vector or turnaround vector
1	0	1	Write vector
0	1	1	Read vector
0	0	1	Exit test mode

In test mode, the internal **HCLK** is driven from the external **TESTCLK** source. This pin can be the normal clock oscillator source input or a port replacement signal. The system bus clock must not glitch when switching between normal and test mode.

On entry into test mode the TIC indicates that it has switched to the test clock input by asserting the **TESTACK** signal.

Test vector types

There are five types of test vector associated with the test interface:

Address vector The address for all subsequent read and write transfers is sampled by the TIC.

Write vector The TIC performs an AHB write cycle, using the write data currently driven onto the external data bus.

Read vector The TIC performs an AHB read cycle, driving the read data onto the external data bus when it becomes valid.

Control vector **I**nternal TIC registers are set, which control the types of read and write transfers that are performed.

Turnaround vector Used between a read cycle and a write cycle to avoid clashes on the external data bus.

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The address, control and turnaround vectors are all indicated by the same value on the **TESTREQA** and **TESTREQB** signals. The following rules can be used to determine which type of vector is being applied:

- a read vector, or burst of read vectors, is followed by two turnaround vectors
- when a single address or control vector is applied it is an address vector
- when multiple address and control vectors are applied they are all address vectors, apart from the last which is a control vector.

Control vectors

The control vector is used to determine the types of transfer the TIC can perform, by setting the values of the **HSIZE**, **HPROT** and **HLOCK** AHB master outputs.

The default TIC bus master transfer type is:

- 32-bit transfer width, **HSIZE[2:0]** signifies word transfer
- privileged system access, **HPROT[3:0]** signifies supervisor data access, uncacheable and unbufferable.

Bit 0 of the control vector is used to indicate if the control vector is valid. Therefore, if a control vector is applied with bit 0 LOW, the vector is ignored and does not update the control information. This mechanism allows address vectors which have bit 0 LOW to be applied for many cycles without updating the control information.

Although the default settings are sufficient for testing many embedded system designs, the control vector can be used to change the control signals of the transfer, and can also be used to determine whether the TIC must generate fixed addresses or incrementing addresses.

Table 4-16 defines the bit positions of the control vector. The control vector bit definitions are designed to be backwards compatible with earlier versions of the TIC and therefore not all of the control bits are in obvious positions.

Table 4-16 Control vector bit definitions

Bit position	Description
0	Control vector valid
1	Reserved
2	**HSIZE[0]**
3	**HSIZE[1]**

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Table 4-16 Control vector bit definitions (continued)

Bit position	Description
4	**HLOCK**
5	**HPROT[0]**
6	**HPROT[1]**
7	Address increment enable
8	Reserved
9	**HPROT[2]**
10	**HPROT[3]**

There is no mechanism to control the types of burst that the TIC can perform and only incrementing bursts of an undefined length are supported. The TIC only supports 8-bit, 16-bit and 32-bit transfers and therefore **HSIZE[2]** cannot be altered and is always LOW.

To support burst accesses using the test interface, the TIC can support incrementing of the bus address. The TIC increments eight address bits and the address range that can be covered by this incrementer is dependent on the size of the transfers being performed.

The control vector provides a mechanism to enable and disable the address incrementer within the TIC. This allows burst accesses to incremental addresses, as would be used for testing internal RAM. Alternatively the address increment can be disabled, such that successive accesses of a burst occur to the same address, as would be required to continually read from a single peripheral register.

The address incrementer is disabled by default and must be enabled using a control vector prior to use.

Note

The control vector is primarily used to change signals which have the same timing as the address bus. However the control vector also allows the lock signal to be changed, which is actually required before the locked transfer commences. If the **HLOCK** signal is used during testing it must be set a transfer before it is required. This difference in timing on the **HLOCK** signal can in some cases cause an additional transfer to be locked both before and after the sequence intended to be locked.

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4.10.3 Test vector sequences

The following test vector sequences are described:

- *Entering test mode*
- *Write vectors* on page 4-70
- *Read vectors* on page 4-71
- *Control vector* on page 4-72
- *Burst vector* on page 4-73
- *Read-to-write and write-to-read transfers* on page 4-74
- *Exiting test mode* on page 4-75.

Entering test mode

In normal operating mode **TESTREQA** is LOW, indicating that test access is not required and the test bus is used as required for normal operation, which is usually part of the external bus interface. Entering test mode allows test vectors to be applied externally that causes transfers on the internal bus.

The following sequence, required to enter test mode, is illustrated in Figure 4-39 on page 4-70:

1. **TESTREQA** is asserted to request test bus access.
2. Test mode is entered when the TIC has been granted the internal bus and this is indicated by the assertion of the **TESTACK** signal.
3. At this point **TESTCLK** becomes the source of the internal **HCLK** signal.
4. When test mode has been entered **TESTREQB** is asserted to initiate an address vector.
5. The TIC does not perform any internal transfers until a valid address vector has been applied.

A synchronous tester would not be expected to poll **TESTACK** for the bus. Normally the **TESTREQA** signal would be asserted for a minimum number of cycles guaranteed to gain access to the bus (completion of the longest wait-state peripheral access or the maximum number of cycles for all bus masters to have completed their current instruction).

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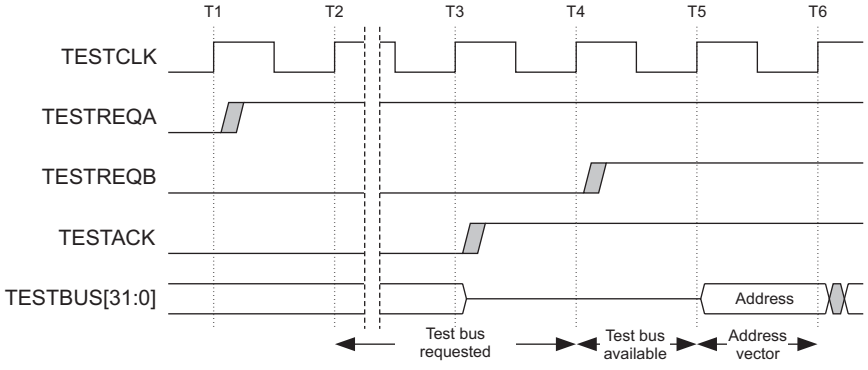

Figure 4-39 Test start sequence

Write vectors

Figure 4-40 shows the sequence of events when applying a set of write test vectors. Initially an address vector is applied and this is followed by a write test vector.

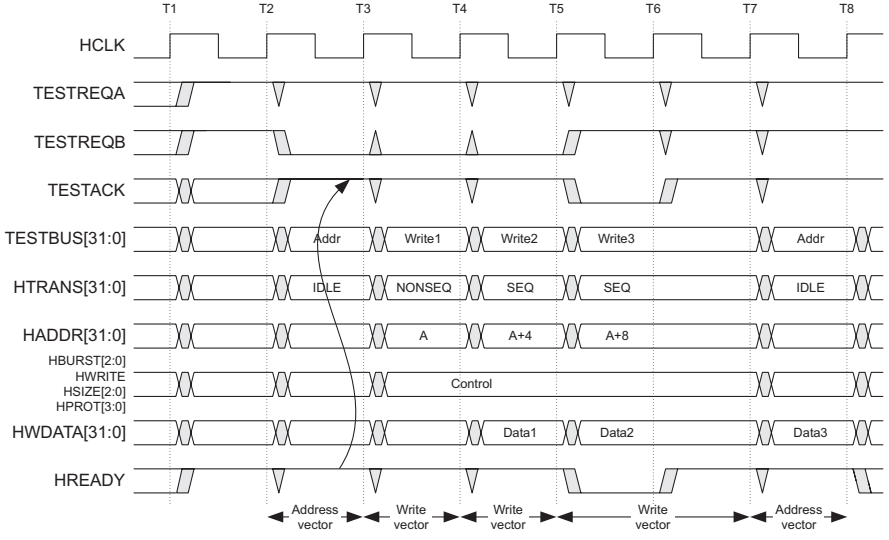

Figure 4-40 Write test vectors

The **TESTREQA** and **TESTREQB** signals are pipelined and are used to indicate what type of vector is applied in the following cycle.

Figure 4-40 shows an example of a number of write transfers being performed.

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The TIC samples the address, **TESTREQA**, and **TESTREQB** signals at time T3, and following this it can initiate the appropriate transfer on the AHB. In the following cycle the write data is driven onto **TESTBUS** and it is then sampled on the following clock edge, T4, and driven onto the internal bus.

If the internal transfer is not able to complete, the **TESTACK** signal is driven LOW and this indicates that the external test vector must be applied for another cycle.

Read vectors

Read transfers are more complex because they require **TESTBUS** to be driven in the opposite direction, and therefore additional cycles are required to prevent bus clash when changing between different drivers of **TESTBUS**. Figure 4-41 shows a typical test sequence for reads.

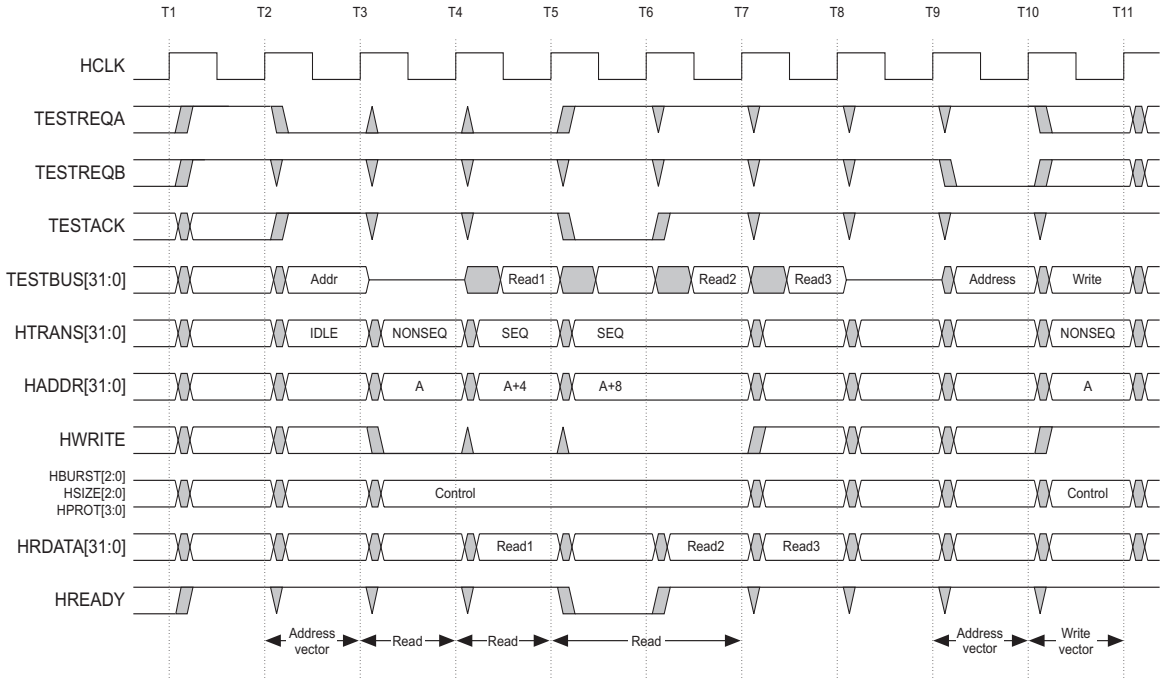

Figure 4-41 Read test vectors

The **TESTREQA** and **TESTREQB** signals are used in the same way as for write transfer. Initially **TESTREQA** and **TESTREQB** are used to apply an address vector and then in the following cycle they are used to indicate that a read transfer is required.

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For the first cycle of a read **TESTBUS** must be tristated, which ensures that the external equipment driving **TESTBUS** has an entire cycle to tristate its buffers before the TIC enables the on-chip buffers to drive out the read data.

At the end of a burst of reads it is also necessary to allow time for bus turnaround. In this case the TIC must turn off the internal buffers and an entire cycle is allowed before the external test equipment starts to drive **TESTBUS**.

The end of a burst of reads is indicated by both **TESTREQA** and **TESTREQB** being HIGH, as for an address vector. In fact they must indicate an address vector for two cycles, which allows for the turnaround cycle at the start of the burst and also the turnaround cycle at the end of the burst.

Control vector

The operation of the TIC can be modified by the use of a control vector. Whenever more than one address vector is applied in succession, the last vector is considered to be a control vector and is not latched as the address. Bit 0 of the control vector is used to determine whether or not the control vector must be considered valid, which allows multiple address vectors to be applied without changing the control information.

Figure 4-42 on page 4-73 shows the process of inserting a control vector.

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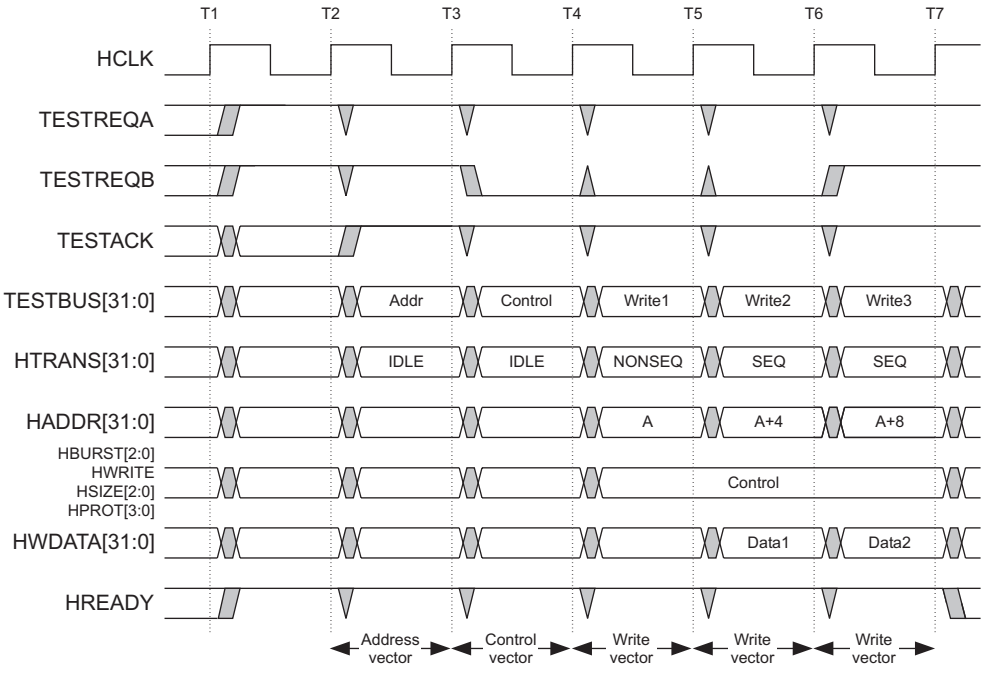

Figure 4-42 Control vector

At time T4 the TIC can determine that **TESTBUS** contains a control vector. This is because the previous cycle was an address vector, and **TESTREQA** and **TESTREQB** are indicating that the following cycle is either a read or a write and therefore the current cycle must be a control vector.

Burst vector

The examples of read and write transfers shown in Figure 4-42 also show how additional transfers can be used to form burst transfers on the bus. The TIC has limited capabilities for burst transfers and can only perform undefined length incrementing bursts.

The TIC contains an 8-bit incrementer and, if an attempt is made to perform a burst which crosses the incrementer boundary, the address simply wraps and the TIC signals the transfer as NONSEQUENTIAL. The exact boundary at which this occurs is dependent on the size of the transfer. For word transfers the incrementer overflows at 1KB boundaries, for halfword transfers it overflows at 512-byte boundaries, and for byte transfers the overflow occurs at 256-byte boundaries.

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Read-to-write and write-to-read transfers

It is possible to switch between read transfers and write transfers without applying a new address vector. Usually this is done with the address incrementer disabled, so that both the read transfers and the write transfers are to the same address. It is also possible to do this with the incrementer enabled if the test circumstances require it.

When moving from a read transfer to a write transfer it is also necessary to allow two cycles for bus handover and therefore **TESTREQA** and **TESTREQB** must signal an address vector for two cycles after the read. This does not cause the address to be changed unless it is followed by a third address vector.

Figure 4-43 illustrates the sequence of events.

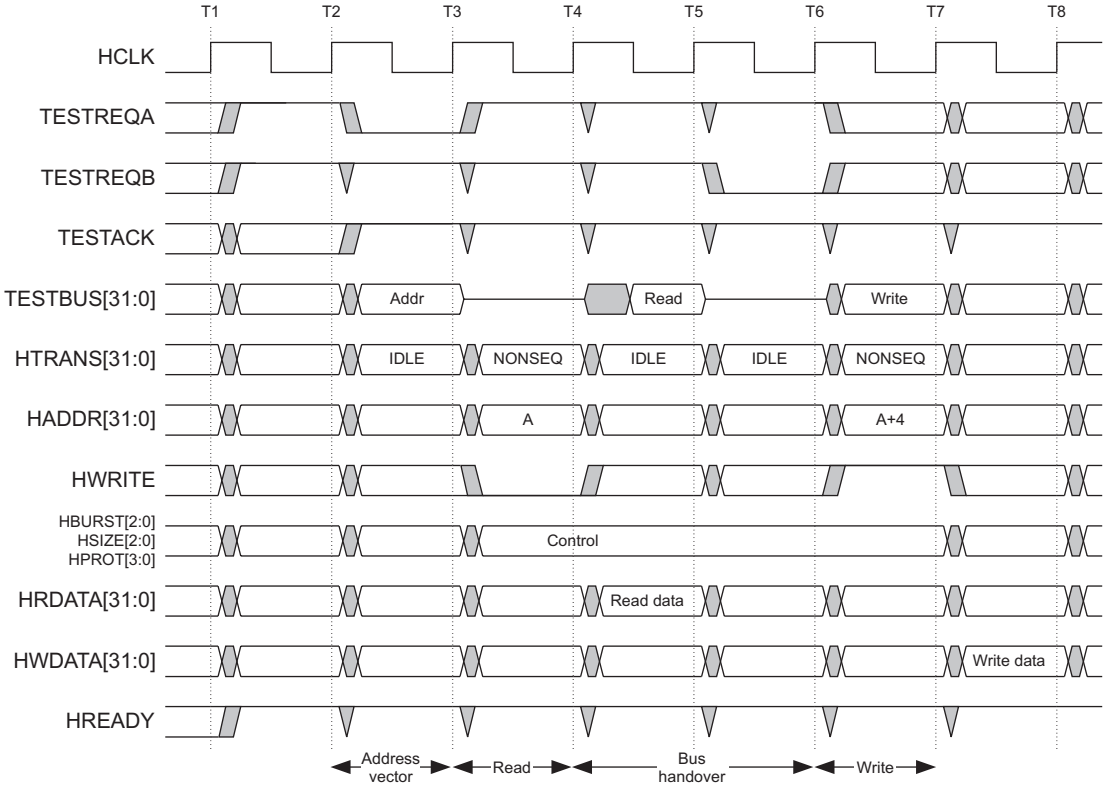

Figure 4-43 Read vector followed by write vector

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Exiting test mode

Test mode is exited using the following sequence:

1. Apply a single cycle of address vector, which causes an IDLE cycle internally. This ensures any internal transfers have been completed and an ADDRESS-ONLY transfer is performed on the internal bus.
2. **TESTREQA** and **TESTREQB** are both driven LOW to indicate that test mode is to be exited.
3. When the test interface has been configured for normal system operation, **TESTACK** goes LOW to indicate that test mode has been exited.

It is important that test mode can be entered and exited cleanly so that the TIC can be used for diagnostic test during system operation, as well as during production testing.

4.10.4 System description

This describes how the HDL code for the TIC is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This should be read together with the HDL code.

Figure 4-44 shows the TIC module block diagram.

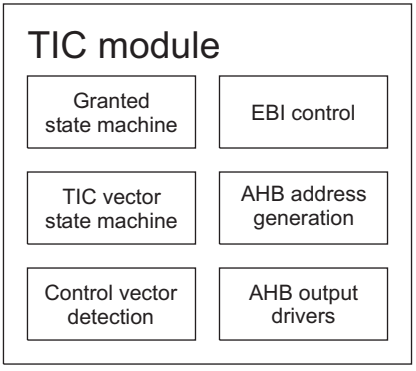

Figure 4-44 TIC module block diagram

The TIC comprises two state machines, which are used to control the access to the AHB of the master interface, and the application of test vectors from the external bus to the system.

All registers in the system are clocked from the rising edge of the system clock **HCLK**, and use the asynchronous reset **HRESETn**.

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A diagram of the TIC HDL file is shown in Figure 4-45.

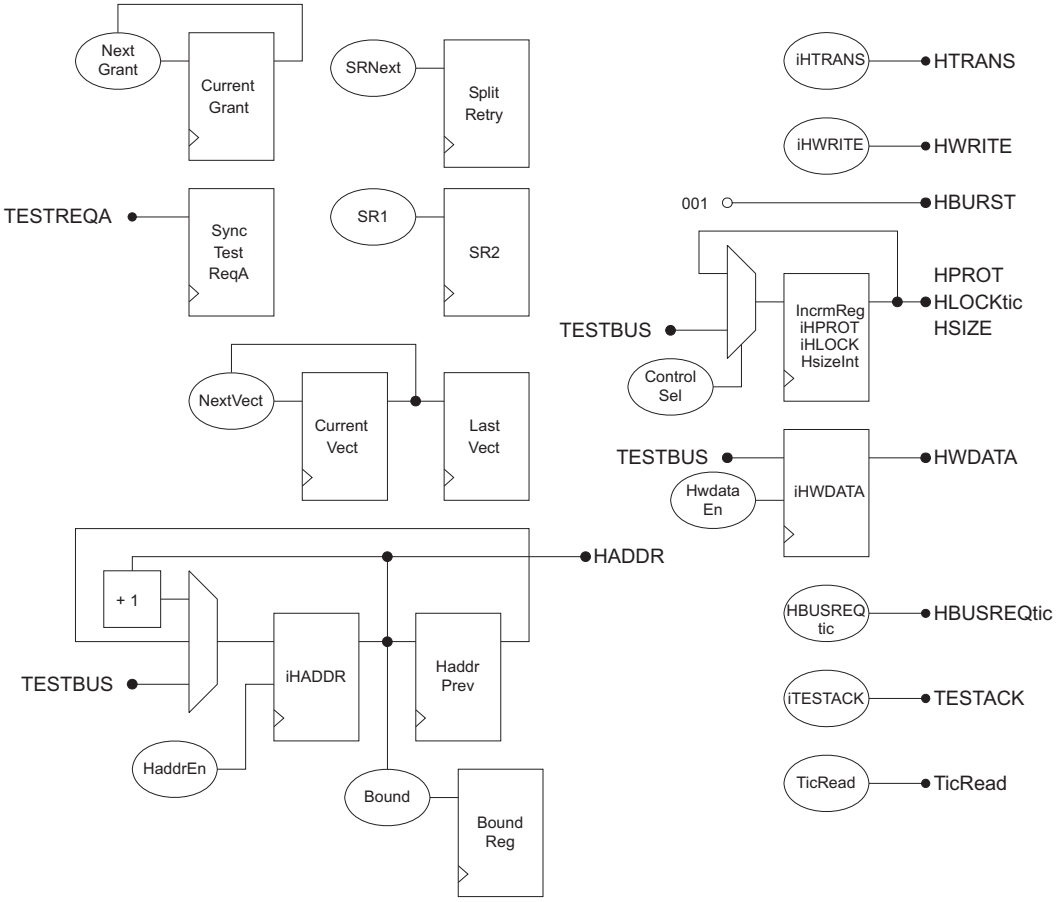

Figure 4-45 TIC module system diagram

The main sections of the code are explained in the following paragraphs:

- *Granted state machine* on page 4-77
- *TIC vector state machine* on page 4-77
- *AHB address generation* on page 4-80
- *Control vector detection* on page 4-81
- *Read data control* on page 4-81
- *Split or retry detection* on page 4-81
- *AHB bus master output signal generation* on page 4-82.

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Granted state machine

This is part of the standard AHB bus master interface, and is used to determine when the TIC is granted the bus, and when it can drive the address, control and data outputs.

The state machine is shown in Figure 4-46, and only advances when the **HREADY** input is set HIGH.

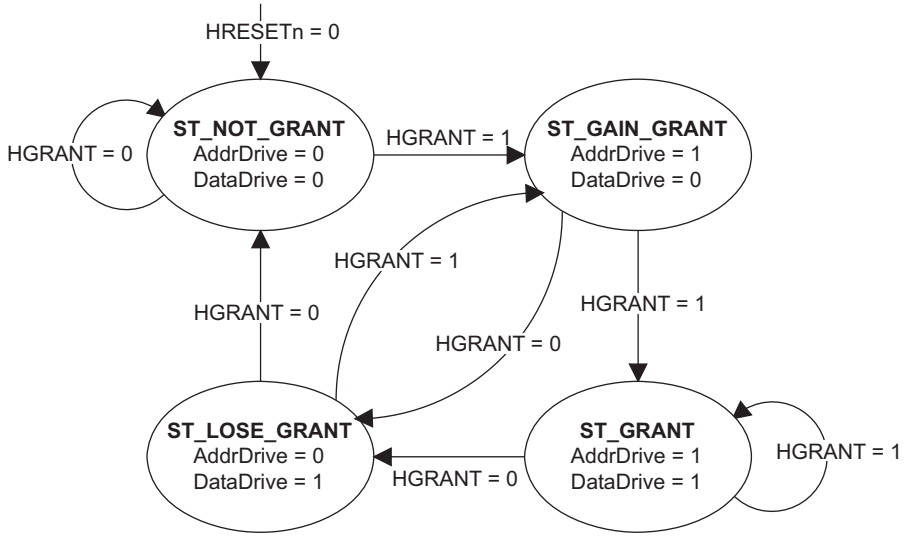

Figure 4-46 TIC module granted state machine

TIC vector state machine

This section of the code is used to control the application of test vectors from the external tester onto the AHB.

Figure 4-47 on page 4-78 illustrates the operation of the TIC vector state machine.

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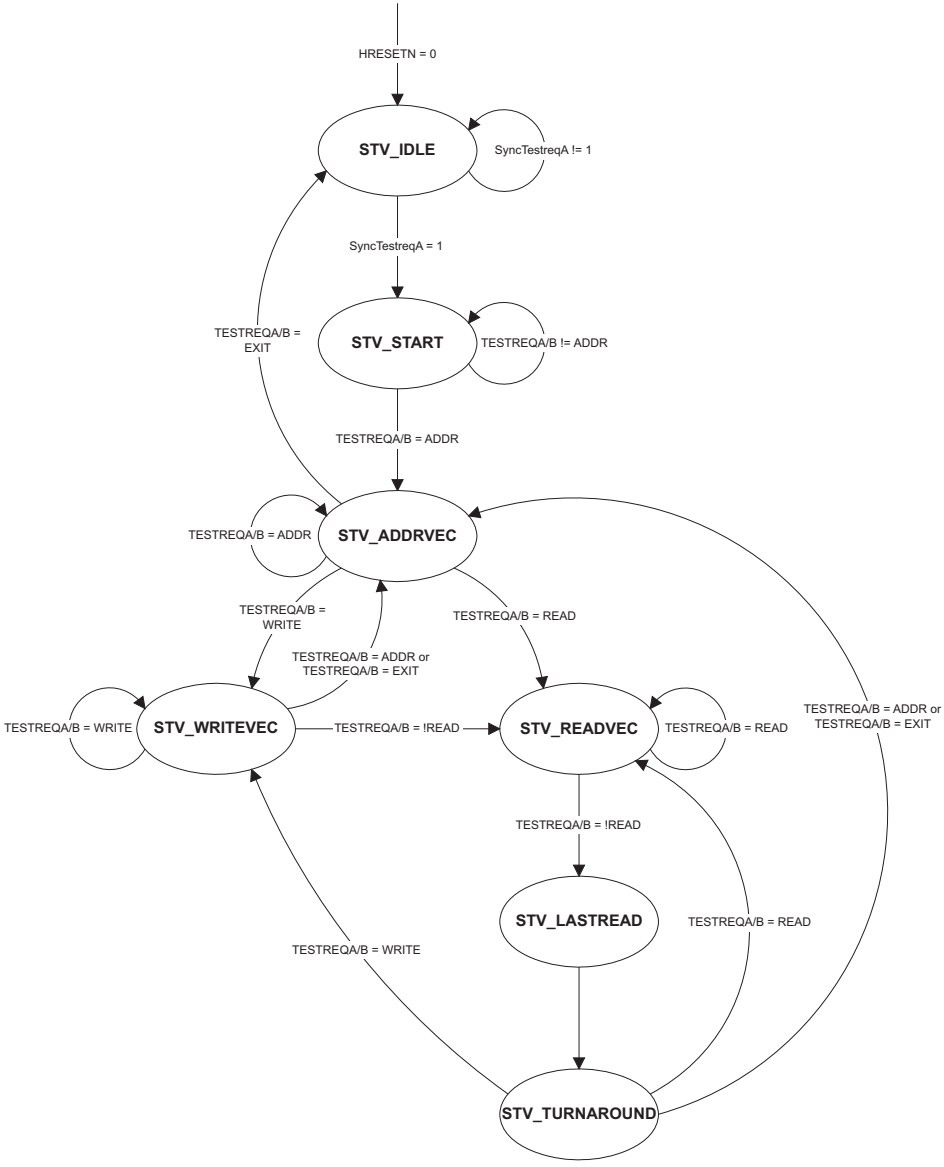

Figure 4-47 TIC vector state machine

At reset the TIC is in the IDLE state and does not request use of the AHB. When in the IDLE state **TESTACK** is driven LOW to indicate that the test interface cannot be used.

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The **TESTACK** signal controls all transactions around the state machine, except for the transition from IDLE to START. In all other cases the state machine remains in the same state if the **TESTACK** signal is low.

The **TESTREQA** signal moves from the IDLE state to the START state. The state of **TESTREQB** is not checked when moving from normal operation to test mode.

In some system implementations it is necessary to switch from an internal clock source to an external clock **TESTCLK** which is used during test mode. When **TESTREQA** first goes HIGH this can be used as an indication that the clock source must be changed. A return signal that indicates when the clock switch has occurred successfully can be used to prevent the move into the START state until the test clock is in use.

If clock switching is being used, it is possible that **TESTREQA** is asynchronous to the on-chip clock before test mode is entered. Therefore a synchronizer is used to generate a synchronized version of **TESTREQA** to control the movement from the IDLE state to the START state.

The START state ensures that the first vector applied is an address vector to prevent read and write vectors occurring before the address has been initialized. The START state is only exited when **TESTREQA** and **TESTREQB** indicate an address vector and the following state is ADDRVEC.

In the ADDRVEC state the TIC registers the address on the **TESTBUS**. The ADDRVEC state is used for both address and control vectors, so additional logic is required to determine whether the value on **TESTBUS** must be considered as an address or as a control vector. If the previous cycle was an address vector and the following cycle (as indicated by **TESTREQA** and **TESTREQB**) is not an address vector, the current cycle is a control vector.

It is possible to stay in the ADDRVEC state for a number of cycles, but usually an address vector is followed by either read or write transfers.

If a write transfer is being performed, the TIC moves into the WRITEVEC state at the same time that it initiates the transfer on the bus. Multiple write transfers can be performed by remaining in the WRITEVEC state. Usually the WRITEVEC is followed by an address vector. However, it is also possible to move directly to a read transfer by moving to the READVEC state.

When a read, or a burst of reads is performed, the TIC enters the READVEC state. This state indicates that the TIC is starting a read transfer on the bus and it is not until the following cycle that the read data appears. When the READVEC state is first entered the **TESTBUS** is tristated, but becomes driven during additional cycles in the READVEC state.

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All read vectors must be followed by two turnaround vectors. For the first of these cycles the TIC moves into the LASTREAD state, during which the last read of the transfer completes and is driven out on to the external **TESTBUS**. During the LASTREAD state no internal transfers are started and the TIC performs IDLE transfers on the bus.

Following the LASTREAD state the TIC moves into the TURNAROUND state, during which time the external **TESTBUS** is tristated. The TURNAROUND state is usually followed by an address vector, but it is also possible to go immediately to a write vector or another read.

The usual method to exit from test is to return to the ADDRVEC state and then set both **TESTREQA** and **TESTREQB** LOW to return to IDLE and effectively exit from test. In fact, at any point the test mode can be exited by setting both **TESTREQA** and **TESTREQB** LOW, and eventually this causes the TIC to exit from test.

Note

When applying TIC vectors it is theoretically possible to assert the **HLOCK** output and then exit from the test. If this happens and then the TIC is granted the bus under normal operation, it effectively locks up the bus. No protection is provided within the TIC to prevent this occurrence.

AHB address generation

There are four main sources of the **HADDR** output in the TIC:

- current address registers
- previous address registers
- external data bus
- incrementer.

The current address is held during a standard read or write cycle, because the address loaded during the previous address vector is used for all subsequent read and write transfers.

The previous address is only used when a split or retry response has been generated by the currently selected slave, and the TIC is set in incrementing mode. When the transfer is regenerated, the incremented address has moved on for the next transfer, so the previous address must be stored for use.

When an address vector is applied, the TIC must read in the new address from the external data bus **TESTBUS**. This new value is stored in the iHADDR registers, and used for the following read and write transfers.

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If address incrementing is enabled, sequential read and write vectors increments the address according to the transfer size that has been set. The first read or write transfer after an address vector is to that address, subsequent transfers have their address incremented. This continues until a control vector is used to disable address incrementing.

Sequential incrementing read and write vectors are signalled as SEQUENTIAL transfers on the AHB, but a NONSEQUENTIAL transfer is added when the address incrementer crosses an 8-bit boundary, set by the current transfer size.

Control vector detection

This part is used to detect a control vector, and contains the control registers. A control vector is the last address vector in a burst of addresses, so is only detected when **TESTREQA** and **TESTREQB** indicate that the next transfer is a read or write vector, and there have been two or more address vectors. The TIC vector state machine is used to detect this, when LastVect and CurrentVect are set to address vector, and NextVect is either a read or a write vector. Also, bit 0 of the control vector (on **TESTBUS**) must be set HIGH for it to be valid, allowing for bursts of addresses.

When it has been detected, the control vector is written to the registers used to hold the transfer settings for **HSIZE**, **HLOCK**, **HPROT,** and if address incrementing is enabled. These values are then held until the next control vector is detected and stored.

Read data control

TicRead is used to enable the EBI to drive the current read data value from **HRDATA** onto **TESTBUS**. It is set HIGH when the last vector was a read, allowing time for the read data to be driven onto the AHB. This output is disabled when the TIC is not granted control of the bus, allowing the EBI to function normally.

Split or retry detection

The TIC must know when the currently selected slave has generated a split or retry, and this section is used to detect that response. If the TIC loses grant before the transfer has been regenerated, the value of the **SplitRetry** signal is held until the TIC has gained control of the bus again.

SR1 and SR2 are also used to indicate the first and second cycles of a SPLIT/RETRY response. SR2 is registered to remove a combinational path from **HRESP** to **HTRANS**.

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AHB bus master output signal generation

Because the TIC is an AHB bus master, it must drive all of the output signals needed to control the operation of AHB slaves on the bus, and also the bus grant request output. This section generates these outputs, and controls when they can be driven out.

HTRANS is generated according to the granted state machine, the TIC vector state machine, the split or retry status, and the incrementer boundary condition.

NONSEQUENTIAL transfers are generated:

- during a read or write following an address
- during a read or write when the TIC has just gained control of the bus
- during a regenerated read or write that has been split or retried
- when the address incrementer has crossed an 8-bit boundary during a sequential read or write.

SEQUENTIAL transfers are generated in incrementing mode:

- when a read follows a read or a write
- when a write follows a write.

IDLE transfers are generated at all other times, because no bus transfers have to be performed.

HWRITE is set HIGH when the current transfer is a write, and is set LOW at all other times. During a regenerated split/retry transfer, the last vector is used.

HBUSREQtic is set LOW when the TIC vector state machine is in the IDLE state, and is set HIGH at all other times, because the bus is only requested when test mode has been entered.

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Chapter 5
APB Modules

This chapter describes the modules that comprise the *Advanced Peripheral Bus* (APB). It contains the following sections:

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5.1 Interrupt controller

The interrupt controller is an APB slave, providing a simple software interface to the interrupt system. It consists of:

- source status and interrupt request status
- separate enable set and enable clear registers to allow independent bit enable control of interrupt sources
- level-sensitive interrupts
- programmable interrupt source.

Figure 5-1 shows the interrupt controller module block diagram.

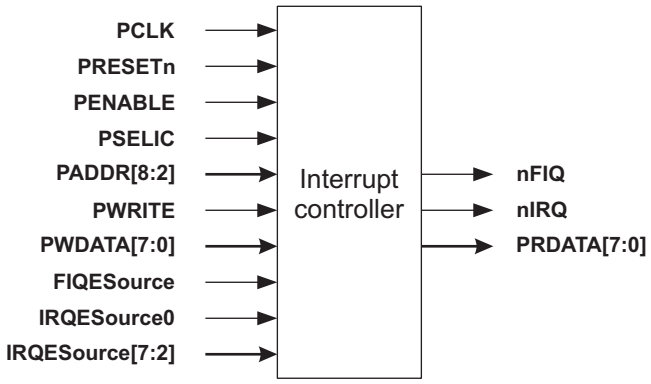

Figure 5-1 Interrupt controller module block diagram

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5.1.1 Hardware interface and signal description

The interrupt controller module is connected to the APB bus. Table 5-1 shows the signal descriptions for the interrupt controller.

Table 5-1 APB signal descriptions for interrupt controller

Signal	Type	Direction	Description
PCLK	Peripheral clock	Input	This clock times all bus transfers. Both the LOW phase and HIGH phase of **PCLK** are used to control transfers.
PRESETn	Peripheral reset	Input	The bus reset signal is active LOW and is used to reset the system.
PENABLE	Peripheral enable	Input	This enable signal is used to time all accesses on the peripheral bus.
PSELIC	Peripheral slave select	Input	When HIGH, this signal indicates that this module has been selected by the APB bridge. This selection is a decode of the system address bus.
PADDR[8:2]	Peripheral address	Input	This is the peripheral address bus, which is used for decoding register accesses. The addresses become valid before **PENABLE** goes HIGH and remains valid after **PENABLE** goes LOW.
PWRITE	Peripheral transfer direction	Input	This signal indicates a write when HIGH and a read when LOW. It has the same timing as the peripheral address bus.
PWDATA[5:0]	Peripheral write data bus	Input	The write peripheral data bus is driven by the bridge at all times.
PRDATA[7:0]	Peripheral read data bus	Output	The read peripheral data bus is driven by this block during read cycles (when **PWRITE** is LOW and **PSELIC** is HIGH).
FIQESource	FIQ interrupt source	Input	**FIQ** interrupt signal into the interrupt module. This active HIGH signal indicates that a fast interrupt request has been generated.
IRQESource[0] **IRQESource[7:2]**	IRQ interrupt sources	Input	**IRQ** interrupt signals into the interrupt module. These active HIGH signals indicate that interrupt requests have been generated. (**IRQESource[1]** is internally generated in the interrupt controller module and is used to provide a software triggered **IRQ**.)
nFIQ	FIQ output	Output	Active LOW fast interrupt request input to the ARM core.
nIRQ	IRQ output	Output	Active LOW interrupt request input to the ARM core.

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5.1.2 Function and operation of the interrupt controller module

The interrupt controller provides a simple software interface to the interrupt system. Certain interrupt bits are defined for the basic functionality required in any system. The remaining bits are available for use by other devices in any particular implementation. In an ARM system, two levels of interrupt are available:

- *fast interrupt request* (FIQ) for fast, low latency interrupt handling
- *interrupt request* (IRQ) for more general interrupts.

Ideally, in an ARM system, only a single FIQ source is in use at any particular time. This provides a true low-latency interrupt, because a single source ensures that the interrupt service routine can be executed directly without the requirement to determine the source of the interrupt. It also reduces the interrupt latency because the extra banked registers, which are available for FIQ interrupts, can be used to maximum efficiency by preventing the requirement for a context save.

Separate interrupt controllers are used for FIQ and IRQ. Only a single bit position is defined for FIQ, which is intended for use by a single interrupt source, while up to 32 bits are available in the IRQ controller. The standard configuration only makes eight interrupt request lines available. This can be extended to up to 32 sources by altering the IRQSize constant setting and increasing the width of the **PWDATA** and **PRDATA** lines to the interrupt controller.

The IRQ interrupt controller uses a bit position for each different interrupt source. Bit positions are defined for a software-programmed interrupt, a communications channel, and counter-timers. Bit 0 is unassigned in the IRQ controller so that it can share the same interrupt source as the FIQ controller.

All interrupt source inputs must be active HIGH and level-sensitive. Any inversion or latching required to provide edge sensitivity must be provided at the generating source of the interrupt.

No hardware priority scheme nor any form of interrupt vectoring is provided, because these functions can be provided in software.

A programmed interrupt register is also provided to generate an interrupt under software control. Typically this can be used to downgrade an FIQ interrupt to an IRQ interrupt.

Interrupt control

The interrupt controller provides:

- interrupt status
- raw interrupt status
- an enable register.

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The enable register is used to determine whether or not an active interrupt source must generate an interrupt request to the processor.

The raw interrupt status indicates whether or not the appropriate interrupt source is active prior to masking and the interrupt status indicates whether or not the interrupt source is causing a processor interrupt.

The enable register has a dual mechanism for setting and clearing the enable bits. This allows enable bits to be set or cleared independently, with no knowledge of the other bits in the enable register.

When writing to the enable set location, each data bit that is HIGH sets the corresponding bit in the enable register. All other bits of the enable register are unaffected. Conversely, the enable clear location is used to clear bits in the enable register while leaving other bits unaffected.

Figure 5-2 shows the structure for a single segment of the interrupt controller.

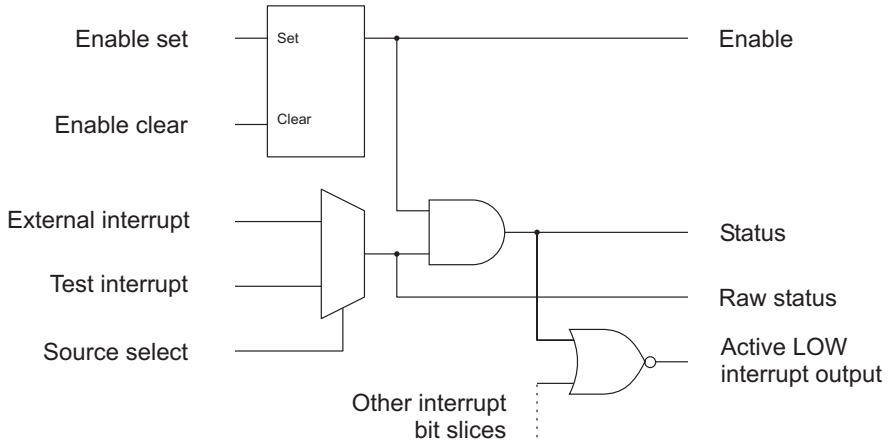

Figure 5-2 Single bit slice of the interrupt controller

The IRQ controller usually has a larger number of bit slices, where the exact size is dependent on the system implementation.

The FIQ interrupt controller consists of a single bit slice, located on bit 0.

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5.1.3 Register memory map

The base address of the interrupt controller is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed. Table 5-2 shows the register memory map.

Table 5-2 Register memory map of the interrupt controller APB peripheral

Address	Read location	Write location
IntBase + 0x000	IRQStatus	-
IntBase + 0x004	IRQRawStatus	-
IntBase + 0x008	IRQEnable	IRQEnableSet
IntBase + 0x00C	-	IRQEnableClear
IntBase + 0x010	-	IRQSoft
IntBase + 0x100	FIQStatus	-
IntBase + 0x104	FIQRawStatus	-
IntBase + 0x108	FIQEnable	FIQEnableSet
IntBase + 0x10C	-	FIQEnableClear
IntBase + 0x014	IRQTestSource	IRQTestSource
IntBase + 0x018	IRQSourceSel	IRQSourceSel
IntBase + 0x114	FIQTestSource	FIQTestSource
IntBase + 0x118	FIQSourceSel	FIQSourceSel

5.1.4 Register descriptions

The following registers are provided for both FIQ and IRQ interrupt controllers:

Enable Read-only. The enable register is used to mask the interrupt input sources and defines which active sources generate an interrupt request to the processor. This register is read-only, and its value can only be changed by the enable set and enable clear locations. If certain bits within the interrupt controller are not implemented, the corresponding bits in the enable register must be read as undefined.

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An enable bit value of 1 indicates that the interrupt is enabled and allows an interrupt request to reach the processor. An enable bit value of 0 indicates that the interrupt is disabled. On reset, all interrupts are disabled.

EnableSet Write-only. This location is used to set bits in the interrupt enable register. When writing to this location, each data bit that is HIGH causes the corresponding bit in the enable register to be set. Data bits that are LOW have no effect on the corresponding bit in the enable register.

EnableClear Write-only. This location is used to clear bits in the interrupt enable register. When writing to this register, each data bit that is HIGH causes the corresponding bit in the enable register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the interrupt enable register.

RawStatus Read-only. This location provides the status of the interrupt sources to the interrupt controller. A HIGH bit indicates that the appropriate interrupt request is active prior to masking.

Status Read-only. This location provides the status of the interrupt sources after masking. A HIGH bit indicates that the interrupt is active and generates an interrupt to the processor.

Soft Write only. A write to bit 1 of this register sets or clears a programmed interrupt. Writing to this register with bit 1 set HIGH generates a programmed interrupt, while writing to it with bit 1 set LOW clears the programmed interrupt. The value of this register can be determined by reading bit 1 of the source Status register. Bit 0 of this register is not used.

Two extra read/write registers are defined for both FIQ and IRQ to allow testing of the interrupt controller module using the AMBA test methodology. They must not be accessed during normal operation.

TestSource Same size as RawStatus, and used to load RawStatus with test data.

SourceSel 1-bit wide (bit 0). When set, the value in TestSource is multiplexed into RawStatus.

5.1.5 Standard configuration of registers

The FIQ interrupt controller is one bit wide and is located on bit 0. The source of this interrupt is implementation-dependent.

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The interrupt controller is customized to fit into each application. The following is an example minimum set of interrupt bits assigned in a system:

- Bits 1 to 5 in the IRQ interrupt controller are defined in the standard EASY world.
- Bit 0 and Bits 6 up to 31 are available for use as required. Bit 0 is left available so that the FIQ source can also be routed to the IRQ controller in an identical bit position.

Table 5-3 gives a typical example allocation of IRQ sources.

Table 5-3 Example of IRQ sources

Bit	Interrupt source
0	Undefined
1	Programmed Interrupt
2	Comms Rx
3	Comms Tx
4	Timer 1
5	Timer 2

5.1.6 System description

This section describes how the HDL code for the interrupt controller is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of all the registers, inputs and outputs used in the system. This section should be read together with the HDL code.

Figure 5-3 on page 5-9 shows the interrupt controller module block diagram.

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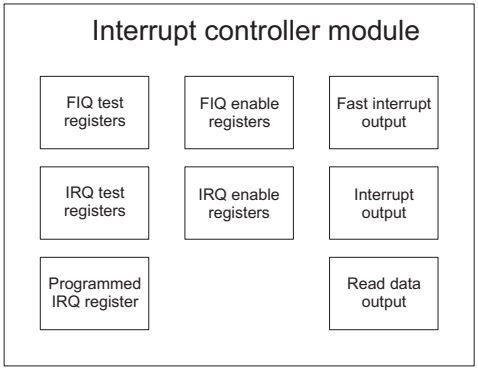

Figure 5-3 Interrupt controller module block diagram

The interrupt controller comprises sets of interrupt registers and test registers that are used to control the generation of the two interrupt outputs to the ARM core, based on the interrupt inputs.

All registers used in the system are clocked from the rising edge of the system clock **PCLK,** and use the asynchronous reset **PRESETn**.

Two diagrams are used to show the interrupt controller HDL file. Figure 5-4 shows the layout of the bit slices that are used for bit 0 of the FIQ and bits 0 and [5:2] of the IRQ.

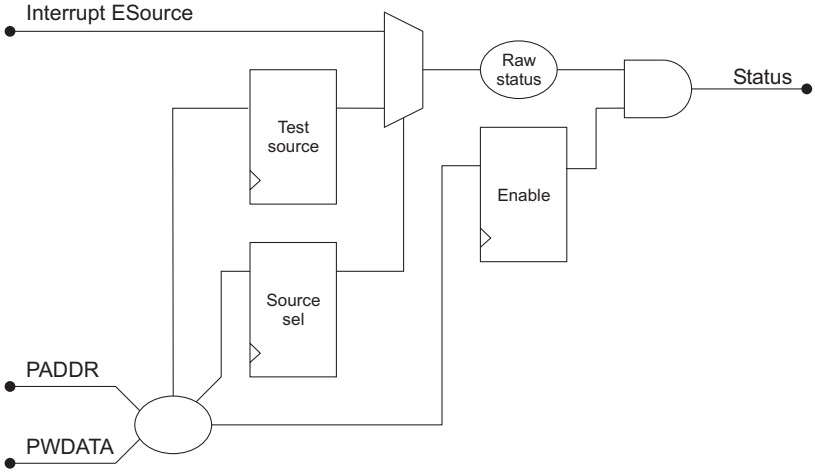

Figure 5-4 Interrupt controller slice system diagram

Figure 5-5 on page 5-10 shows the layout of the whole system.

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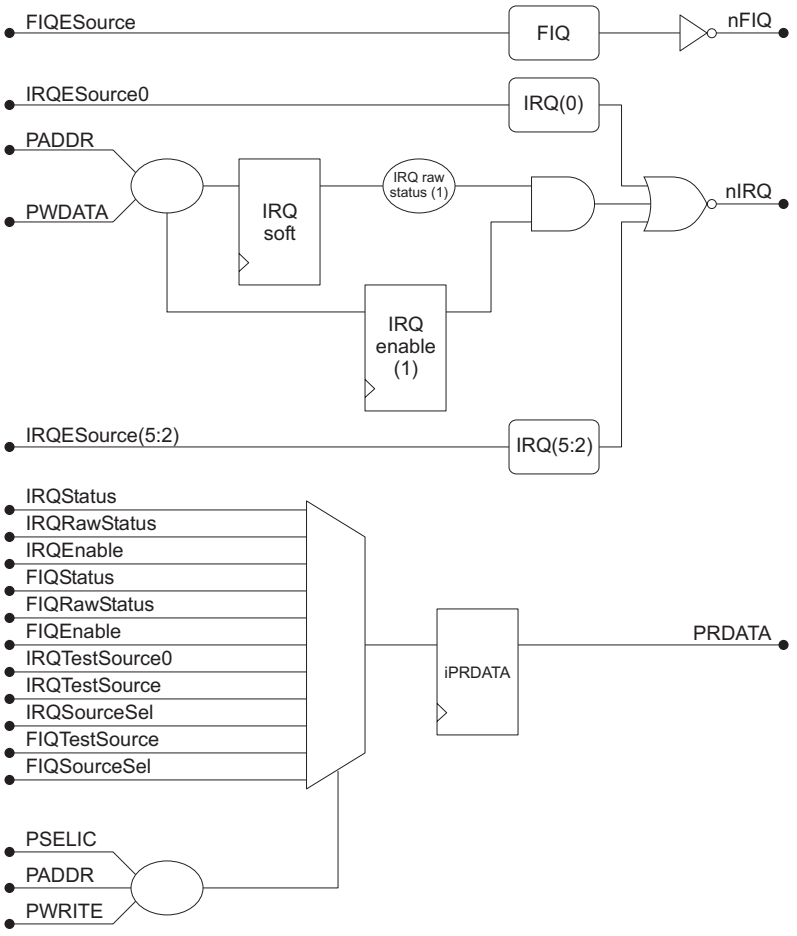

Figure 5-5 Interrupt controller module system diagram

The main sections in this module are explained in more detail in the following paragraphs:

- *Constant definitions* on page 5-11
- *IRQ generation* on page 5-11
- *FIQ generation* on page 5-11
- *Output data generation* on page 5-11.

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Constant definitions

The first two constants that are specified (IRQSIZE and FIQSIZE), are used to set the number of IRQ and FIQ lines that are used in the system. The defaults are for eight IRQ lines and one FIQ line. These constants must only be changed when the number of interrupt input sources are changed.

The other constants are used to set the relative addresses of the interrupt controller registers from the base address.

IRQ generation

Figure 5-4 on page 5-9 shows the structure of the IRQ generation logic from the external interrupt sources.

The read/write TestSource register is used to hold the test value. This is passed through a multiplexor, and then used to switch between the external and internal test interrupt sources. This is the read-only RawStatus value, which is gated with the output of the enable register, and used to generate the Status output.

All of the IRQ sources are then combined to generate the active LOW **nIRQ** output, which is set LOW when any of the IRQ lines are set HIGH.

FIQ generation

The FIQ logic is similar to the IRQ logic, but in the default system is only one bit wide, and does not have a software programmable source. The nFIQ output is directly generated from the single interrupt source bit, using an inverter.

Output data generation

This section is used to decode the current address during a read, and generate the correct data to be driven onto the APB data bus. The address is compared with all of the register addresses, and the value of PRDATANext is set accordingly. This is then stored in the iPRDATA register to help decrease the output propagation time by using a registered output, rather than an output with the combinational delay of the large multiplexor. This register also synchronizes the reading of all raw interrupt inputs to the rising edge of the clock. The **PRDATA** output is then driven by the register.

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5.2 Remap and pause controller

The remap and pause controller is an APB slave, providing control of the system boot behavior and low-power *wait for interrupt* mode.

The main sections of this module are:

- defined boot behavior with power-on reset detection
- a wait for interrupt pause mode
- an identification register.

A block diagram of the remap and pause module is shown in Figure 5-6.

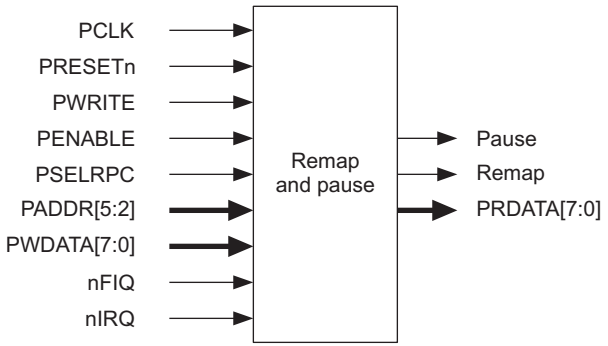

Figure 5-6 Remap and pause module block diagram

5.2.1 Signal descriptions

on page 5-9Table 5-4 describes the APB signals used and produced by the remap and pause controller.

Table 5-4 APB signal descriptions for remap and pause controller

Signal	Type	Direction	Description
PCLK	Peripheral clock	Input	This clock times all bus transfers. Both the LOW phase and HIGH phase of **PCLK** are used to control transfers.
PRESETn	Peripheral reset	Input	The bus reset signal is active LOW and is used to reset the system.
PENABLE	Peripheral enable	Input	This enable signal is used to time all accesses on the peripheral bus.
PSELRPC	Peripheral slave select	Input	When HIGH, this signal indicates that this module has been selected by the APB bridge. This selection is a decode of the system address bus.

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Table 5-4 APB signal descriptions for remap and pause controller (continued)

Signal	Type	Direction	Description
PADDR[5:2]	Peripheral address bus	Input	This is the peripheral address bus, which is used for decoding register accesses. The addresses become valid before **PENABLE** goes HIGH and remains valid after **PENABLE** goes LOW.
PWRITE	Peripheral transfer direction	Input	This signal indicates a write when HIGH and a read when LOW. It has the same timing as the peripheral address bus.
PWDATA[7:0]	Peripheral write data bus	Input	The write peripheral data bus is driven by the bridge at all times.
PRDATA[7:0]	Peripheral read data bus	Output	The read peripheral data bus is driven by this block during read cycles (when **PWRITE** is LOW and **PSELRPC** is HIGH).
nFIQ	FIQ output	Input	FIQ interrupt input from the interrupt controller.
nIRQ	IRQ output	Input	IRQ interrupt input from the interrupt controller.
Pause	Pause mode	Output	HIGH when in the *wait for interrupt* pause mode, and LOW at all other times.
Remap	Reset memory map	Output	LOW when the reset memory map is in use, and HIGH when the normal memory map is in use.

5.2.2 Functions and operations of the remap and pause module

The remap and pause control is the combination of four separate functions:

Pause Defines a method of allowing the processor system to enter a low-power, *wait for interrupt* state, when the system does not require the processor to be active.

Identification Provides an indication of the system configuration.

Reset memory map Provides a method of overlaying the system base memory at reset.

Reset status Provides an indication of the cause of the most recent reset condition. A minimum implementation is defined.

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5.2.3 Register memory map

The base address of the remap and pause controller memory is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed. Table 5-5 shows the remap and pause controller memory map.

Table 5-5 Memory map of the remap and pause controller APB peripheral

Address	Read location	Write location
`RemapBase + 0x00`	-	Pause
`RemapBase + 0x10`	Identification	-
`RemapBase + 0x20`	-	ClearResetMap
`RemapBase + 0x30`	ResetStatus	ResetStatusSet
`RemapBase + 0x34`	-	ResetStatusClear

5.2.4 Remap and pause register descriptions

Pause Write-only. Writing to the pause location causes the system to enter a wait for interrupt state, by setting the **Pause** output HIGH.

The exact effect of writing to this location is not defined, but typically this would prevent the processor from fetching more instructions until the receipt of an interrupt or a power-on reset. More registers can be added to provide more sophisticated power-saving modes.

Identification Read-only. The identification location provides identification information about the system. Only a single-bit implementation (bit 0) is required, which is used to indicate if there is more ID information:

0 = no more ID information 1 = more ID information is available.

If bit zero of the identification register is set, more bits are required to provide more detailed system identification information.

ClearResetMap Write-only. Writing to the clear reset memory map location changes the system memory map. It changes from that required during boot-up to that required during normal operation. This is done by setting the **Remap** output to HIGH. When the reset memory map has been cleared and the normal memory map is in

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use, there is no method of resuming the reset memory map, other than undergoing a power-on reset condition. A typical system implementation is to map the system ROM to location `0x00000000` at reset, but to change the memory map after reset, such that RAM is located at location `0x00000000` for normal operation. In a system where such remapping does not occur, writing to this register has no effect.

ResetStatus Read-only. The reset status location provides the reset status. Only one bit of this register is defined in this specification and this is bit 0, which provides the power-on reset status. Further bits in the ResetStatus register can be implemented to provide more detailed reset information. The ResetStatus register has a dual mechanism for setting and clearing bits, allowing independent bits to be altered with no knowledge of the other bits in the register. This is done by using the ResetStatusClear and the ResetStatusSet registers.

The single bit defined in this specification is the power-on reset bit, which can be used to determine if the most recent reset was caused by initial power-on, or if a warm reset has occurred:

0 = no POR since flag was last cleared 1 = POR.

ResetStatusClear Write-only. This location is used to clear reset status flags. When writing to this register each data bit that is HIGH causes the corresponding bit in the ResetStatus register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the ResetStatus register.

ResetStatusSet Write-only. This location is used to set reset status flags. When writing to this register each data bit that is HIGH causes the corresponding bit in the ResetStatus register to be set. Data bits that are LOW have no effect on the corresponding bit in the ResetStatus register. The power-on reset status bit (bit 0) cannot be set by software, because it can only be set during a system reset. The extra bits of the register are included in the specification to ensure the reset status functionality can easily be expanded.

5.2.5 System description

The following paragraphs describe how the HDL code for the remap and pause controller module is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of all the registers, inputs and outputs used in the system. This section should be read together with the HDL code.

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A basic block diagram of the remap and pause controller module is shown in Figure 5-7.

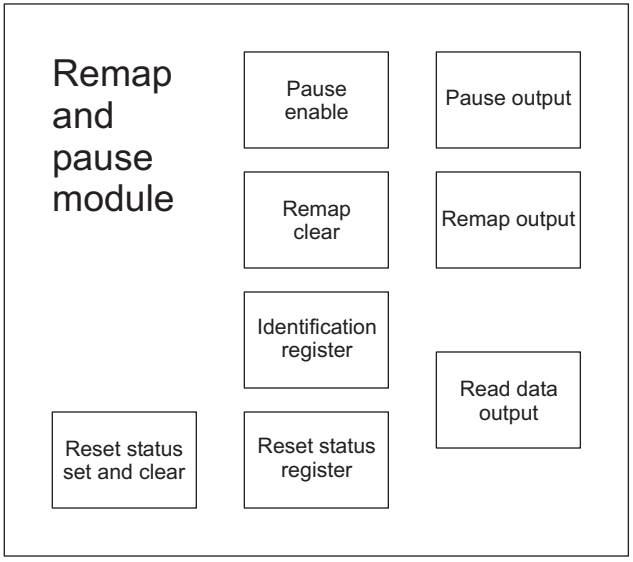

Figure 5-7 Remap and pause module block diagram

The remap and pause controller comprises registers to generate the **Remap** and **Pause** outputs, and logic to allow the reading of the identification and reset status values.

All registers used in the system are clocked from the rising edge of the system clock **PCLK**, and use the asynchronous reset **PRESETn**. The Pause register also uses the two interrupt inputs as asynchronous resets, allowing the value to be cleared while the system is not clocked.

A diagram of the remap and pause HDL file is shown in Figure 5-8 on page 5-17.

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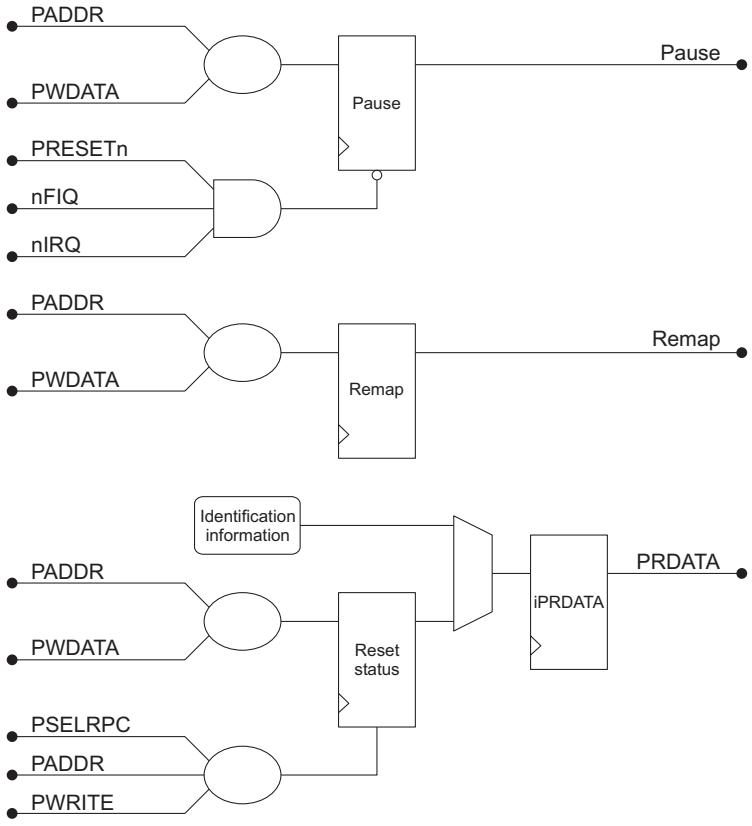

Figure 5-8 Remap and pause module system diagram

The main sections in this module are explained in more detail in the following sections:

- *Constant definitions*
- *ResetStatus value generation* on page 5-18
- *Pause output generation* on page 5-18
- *Remap output generation* on page 5-19
- *Output data generation* on page 5-19.

Constant definitions

The constant IDENTIFICATION holds the identification information about the system. The default setting for this value is all zero. The maximum size for this value is the width of the read and write data buses of the module.

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ResetStatus value generation

This register is modified through the ResetStatusSet and ResetStatusClear addresses. When writing to the set location, each data bit that is HIGH sets the corresponding bit in the ResetStatus register. All other bits of the register are unaffected. Each data bit that is set HIGH when writing to the clear location clears the corresponding bit in the ResetStatus register, leaving all other bits unaffected.

The power-on-reset bit (bit 0) cannot be set by writing to the set location, because it is only set HIGH during system reset. It can be cleared in the same way as the other register bits.

Pause output generation

A register is used to hold the *wait for interrupt* state value. The **Pause** output is synchronously set HIGH (on the rising edge of **PCLK**) when the Pause location is written to, with any value, and is asynchronously set LOW by **PRESETn**, **nFIQ** or **nIRQ**. When set HIGH, it can only be set LOW with a reset or an interrupt.

Figure 5-9 shows the operation of setting and clearing the Pause registered output.

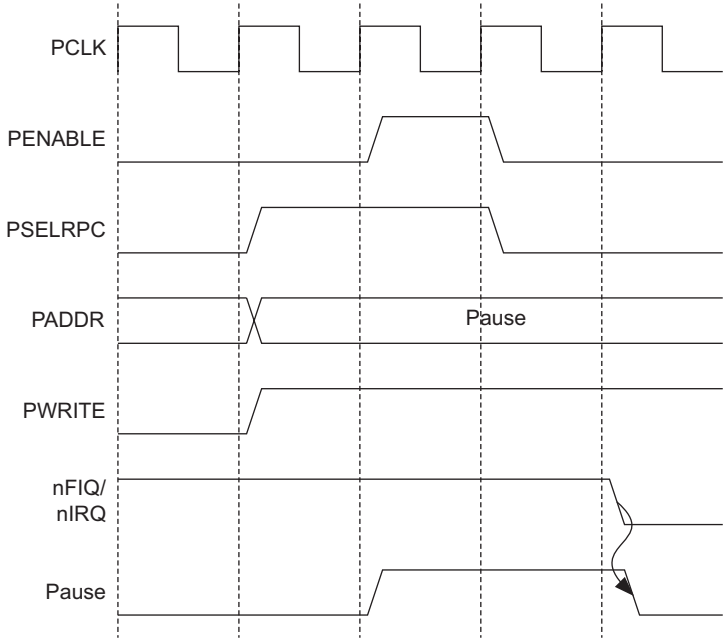

Figure 5-9 Pause signal timing

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Remap output generation

This register is used to hold the system memory map state value. The **Remap** output is set LOW on reset, indicating that the reset memory map is in use. It is set HIGH when the ClearResetMap location is written to with any value, indicating that the normal system memory map is in use. When set HIGH, it can only be set LOW by a system reset.

Output data generation

This section is used to decode the current address during a read, and generate the correct data to be driven onto the APB read data bus. The address is compared with all of the register addresses, and the value of PRDATANext is set accordingly. This is then stored in the iPRDATA register to help decrease the output propagation time by using a registered output, rather than an output with the combinational delay of the large multiplexor. The **PRDATA** output is then driven by the register.

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5.3 Timers

The timers module is an APB slave, providing access to two interrupt generating programmable 16-bit *Free-Running decrementing Counters* (FRCs).

The main sections of the timers module are:

- two identical instantiations of a programmable 16-bit free-running counter
- prescale for each counter clock
- interrupt generation based on counter value.

The timers module is shown in Figure 5-10.

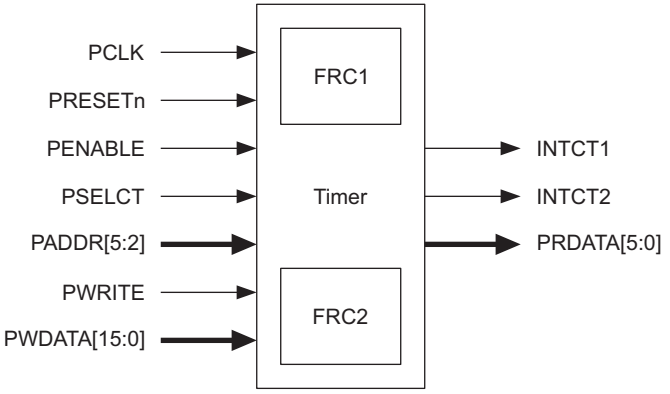

Figure 5-10 Timer module block diagram

5.3.1 Signal descriptions

The two sets of signals associated with the timers module are:

- the external connections to the rest of the EASY world
- the internal connections between the timers module and the two FRC modules.

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The signal descriptions for the timers module are listed in Table 5-6.

Table 5-6 APB signal descriptions for timer

Signal	Type	Direction	Description
PCLK	Peripheral clock	Input	This clock times all bus transfers. Both the LOW phase and HIGH phase of **PCLK** are used to control transfers.
PRESETn	Peripheral reset	Input	The bus reset signal is active LOW and is used to reset the system.
PENABLE	Peripheral enable	Input	This enable signal is used to time all accesses on the peripheral bus.
PSELCT	Peripheral slave select	Input	When HIGH, this signal indicates that this module has been selected by the APB bridge. This selection is a decode of the system address bus.
PADDR[5:2]	Peripheral address bus	Input	This is the peripheral address bus, which is used for decoding register accesses. The addresses become valid before **PENABLE** goes HIGH and remains valid after **PENABLE** goes LOW.
PWRITE	Peripheral transfer direction	Input	This signal indicates a write when HIGH and a read when LOW. It has the same timing as the peripheral address bus.
PWDATA[15:0]	Peripheral write data bus	Input	The write peripheral data bus is driven by the bridge at all times.
PRDATA[15:0]	Peripheral read data bus	Output	The read peripheral data bus is driven by this block during read cycles (when **PWRITE** is LOW and **PSELCT** is HIGH).
INTCT	Counter 1 interrupt	Output	Active HIGH interrupt signal to the interrupt controller module. This signal indicates an interrupt has been generated by counter 1 having been decremented to zero.
INTCT2	Counter 2 interrupt	Output	Active HIGH interrupt signal to the interrupt controller module. This signal indicates an interrupt has been generated by counter 2 having been decremented to zero.

5.3.2 Function and operation of module

Two counters are defined as the minimum provided within a system, although this can easily be expanded. The same principle of simple expansion has been applied to the register configuration, allowing more complex counters to be used.

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Two modes of operation are available:

Free-running mode The counter wraps after reaching its zero value, and continues to count down from the maximum value. This is the default mode.

Periodic timer mode The counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero.

5.3.3 Timer operation

The timer is loaded by writing to the Load register and, if enabled, counts down to zero. When zero is reached, an interrupt is generated. The interrupt can be cleared by writing to the **Clear** register.

After reaching a zero count, if the timer is operating in free-running mode it continues to decrement from its maximum value. If periodic timer mode is selected, the timer reloads the count value from the Load register and continues to decrement. In this mode the counter effectively generates a periodic interrupt. The mode is selected by a bit in the Control register.

At any point, the current counter value can be read from the Value register.

The counter is enabled by a bit in the Control register. At reset, the counter is disabled, the interrupt is cleared, and the Load register is set to zero. The mode and prescale values are set to free-running, and clock divide of one respectively.

Figure 5-11 is a block diagram showing timer operation.

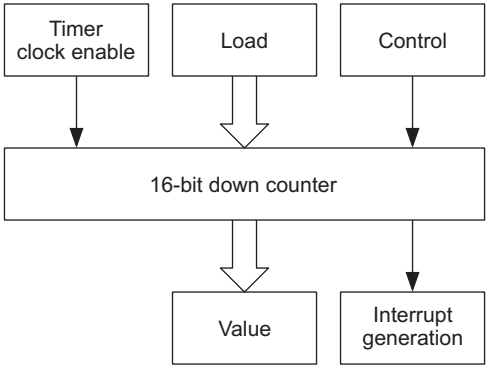

Figure 5-11 Timer operation

The timer clock enable is generated by a prescale unit. The enable is then used by the counter to create a clock with a timing of one of the following:

- the system clock

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- the system clock divided by 16, generated by 4 bits of prescale
- the system clock divided by 256, generated by a total of 8 bits of prescale.

Figure 5-12 shows how the timer clock frequency is selected in the prescale unit.

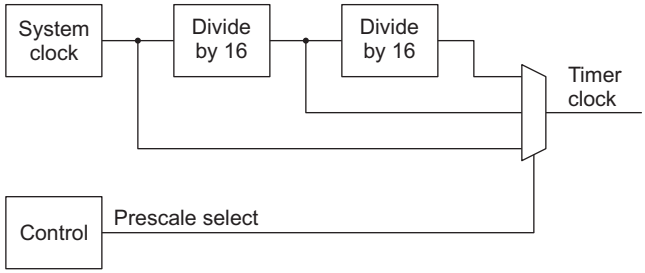

Figure 5-12 Prescale clock enable generation

5.3.4 Register memory map

The base address of the timers module is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

Table 5-7 Memory map of the time APB peripheral

Address	Read location	Write location
`TimerBase + 0x00`	Timer1Load	Timer1Load
`TimerBase + 0x04`	Timer1Value	-
`TimerBase + 0x08`	Timer1Control	Timer1Control
`TimerBase + 0x0C`	-	Timer1Clear
`TimerBase + 0x20`	Timer2Load	Timer2Load
`TimerBase + 0x24`	Timer2Value	-
`TimerBase + 0x28`	Timer2Control	Timer2Control
`TimerBase + 0x2C`	-	Timer2Clear
`TimerBase + 0x10`	Timer1Test	Timer1Test
`TimerBase + 0x30`	Timer2Test	Timer2Test

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5.3.5 Timer register descriptions

TimerXLoad Read/write. This register contains the initial value to be loaded into the counter and is also used as the reload value in periodic mode. This register is the same width as the counter (default is 16 bits).

TimerXValue Read-only. This location gives the current value of the counter.

TimerXClear Write-only. Writing to this location clears an interrupt generated by the counter.

TimerXControl Read/write. This register provides enable/disable, mode and prescale configurations for the counter.

Figure 5-13 shows the control register.

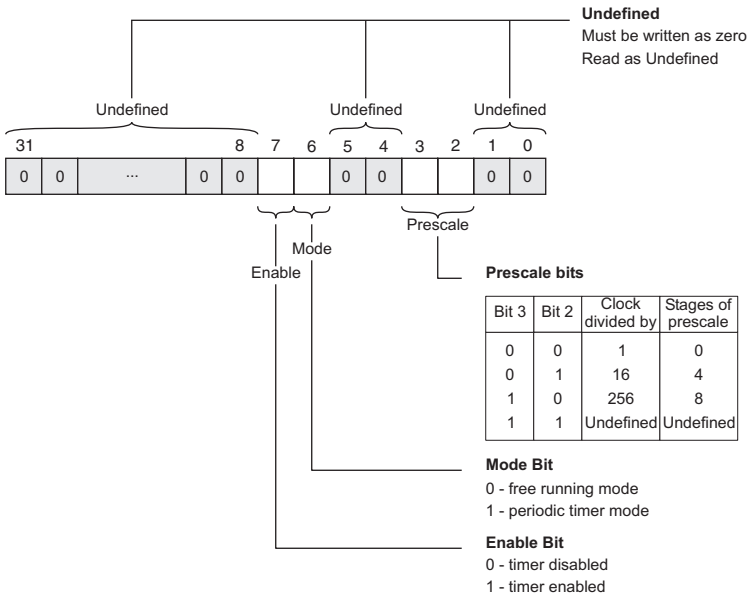

Figure 5-13 The control register

TimerXTest Two special registers are provided for validation purposes, Timer1Test and Timer2Test. These locations must not be accessed during normal system operation.

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Both registers are read/write and are 2 bits wide, as shown in Table 5-8.

Table 5-8 Test register bit functions

Bit	Name	Function
0	Test	Counter test mode
1	TestClkSel	Test clock select

The counter test mode bit is stored in a register in both FRCs. The test clock select bit is stored in a single register in the top-level timers module, but can be accessed from either test address.

When the counter test mode bit is set, the selected 16-bit counter is divided into four separate 4-bit counters that continually loop round from 15 to 0. This reduces the testing time needed to ensure that the correct counting sequence is performed. Clearing this bit (default) brings the selected timer back to normal operation.

When the test clock select bit is set in either of the two test registers, a special test clock (NOT **PENABLE** ANDed with **PSELCT**) is fed into the prescale unit instead of the system clock (therefore both counters have to be using the same clock source, either normal or test). Clearing this bit (default) selects the system clock as the prescale clock input (normal operation).

5.3.6 System description

This section describes how the HDL code for the timers module is set out. A basic system block diagram, with information about the main parts of the HDL code, is followed by details of all the registers, inputs and outputs used in this module. This should be read together with the HDL code.

A basic block diagram of the timers module is shown in Figure 5-14 on page 5-26.

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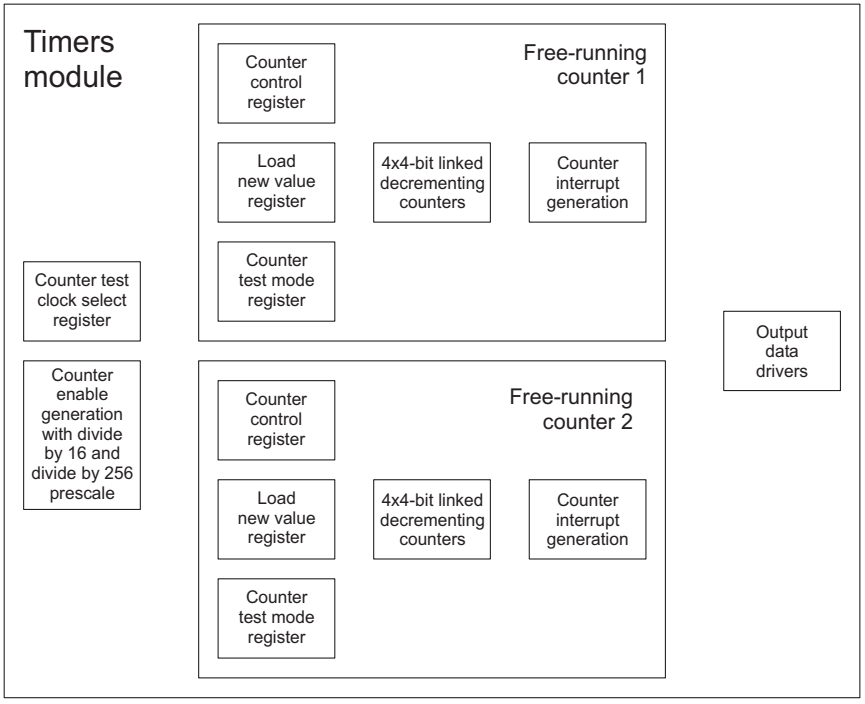

Figure 5-14 Timers module block diagram

The timers module comprises two 16-bit programmable free-running counters, and clock prescale enable generation logic. The free-running counters comprise four linked 4-bit counters, interrupt generation logic and counter control registers.

All registers used in the system are clocked from the rising edge of the system clock **PCLK** and use the asynchronous reset **PRESETN**.

5.3.7 Timer system description

A diagram of the timers module HDL file is shown in Figure 5-15 on page 5-27.

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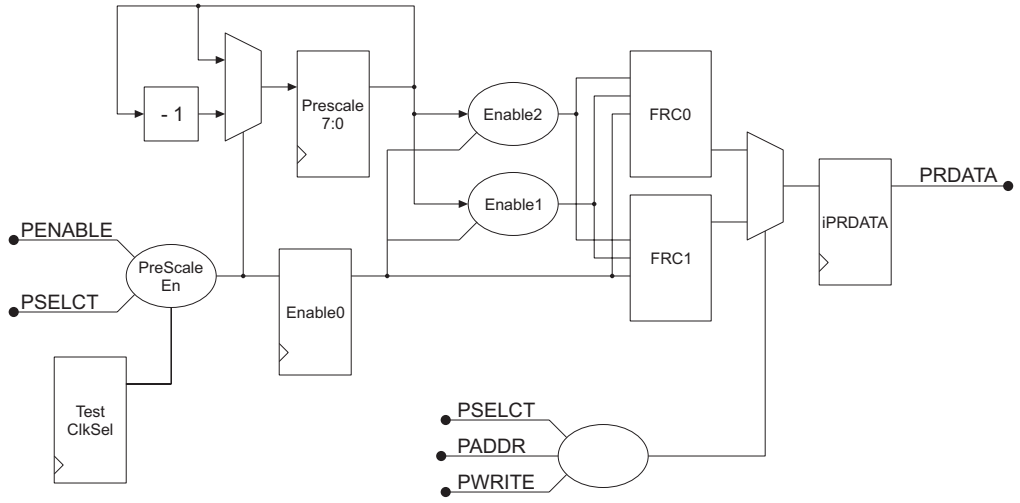

Figure 5-15 Timers module system diagram

The main sections in this module are explained in the following paragraphs:

- *Address decoder*
- *Test clock select generation*
- *Clock prescaler* on page 5-28
- *Output clock enable generation* on page 5-28
- *Output data generation* on page 5-28.

Address decoder

This section is used to generate the **TestSel** signal, which is used to indicate an access to either of the test registers, and the **Frcsel** select lines to the FRCs based on the current address. Because there are two instantiations (in the default system) of an identical FRC module, part of the address decoding must be done at the previous system level.

Test clock select generation

This register is used to store the current value of bit 1 of all counter test registers. A read or write to any of the test register addresses access this single register.

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Clock prescaler

The 8-bit prescale registers are used to generate the two prescale signals of divide by 16 and divide by 256, by decrementing the current value of the registers. The enable signal PreScaleEn is used to control the operation of the registers, which by default is always set, but in test clock mode is a combination of **PENABLE** and **PSELCT**, allowing an output clock pulse to be generated for each read or write access to the timers module.

Output clock enable generation

The three different clock enable signals (equivalent to the system clock, the system clock divided by 16, and the system clock divided by 256) enable the timer clocks in the two FRC modules, based on the amount of prescale that is required.

Figure 5-16 and Figure 5-17 show the timing of these enable signals.

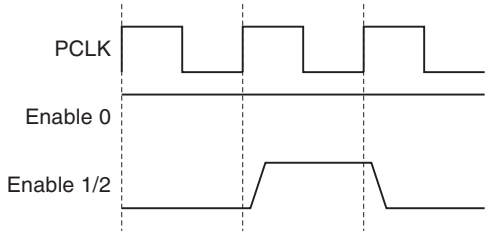

Figure 5-16 Timer module counter enable timing - system clock selected

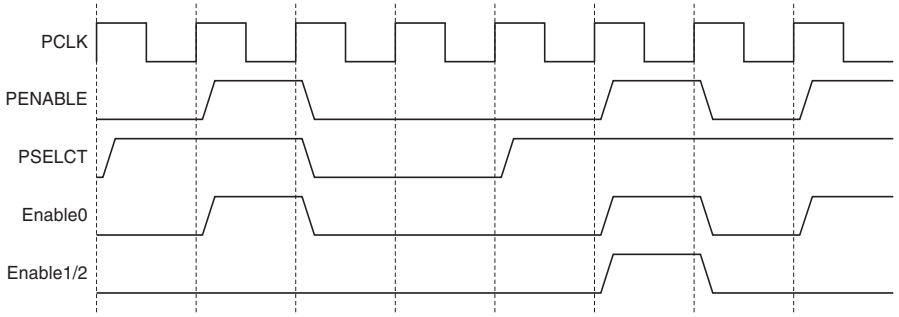

Figure 5-17 Timer module counter enable timing - test clock selected

Output data generation

This section is used to decode the current address during a read, and generate the correct data to be driven onto the APB read data bus. The address is compared with all of the register addresses, and the value of PRDATANext is set accordingly. This is then stored

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in the iPRDATA register to help decrease the output propagation time by using a registered output, rather than an output with the combinational delay of the large multiplexor. The **PRDATA** output is then driven by the register.

The read data is based on the FRC data outputs, with the local Test Clock Select register output also used when reading from a test location.

5.3.8 FRC system description

Two identical instances of the free-running counter block are included in the timers module.

The basic block diagram of the free-running counter block is shown in Figure 5-18.

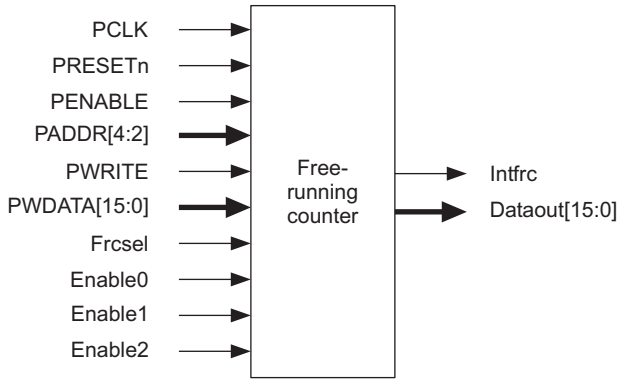

Figure 5-18 FRC module block diagram

5.3.9 FRC signal descriptions

Table 5-9 shows descriptions for the FRC signals.

Table 5-9 Signal descriptions for FRC

Signal	Type	Direction	Description
PCLK	Peripheral clock	Input	Direct connection from timers module.
PRESETn	Peripheral reset	Input	Direct connection from timers module.
PENABLE	Peripheral enable	Input	Direct connection from timers module.
PADDR[4:2]	Peripheral address	Input	Direct connection from timers module.

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Table 5-9 Signal descriptions for FRC (continued)

Signal	Type	Direction	Description
PWRITE	Peripheral transfer direction	Input	Direct connection from timers module.
PWDATA[15:0]	Peripheral write data bus	Input	Direct connection from timers module.
Frcsel	FRC register select	Input	FRC register select, driven HIGH when a register in this FRC is addressed. There is a select line for each counter in the timers module.
Enable0	Enable prescale 0	Input	Counter clock enable, divide by 1.
Enable1	Enable prescale 4	Input	Counter clock enable, divide by 16.
Enable2	Enable prescale 8	Output	Counter clock enable, divide by 256.
Intfrc	Interrupt output	Output	Interrupt output from the counter, generated when 16-bit counter reaches zero. There is an interrupt output for each counter in the timers module.
Dataout	Read data output	Output	Read data output used to generate **PRDATA** for register reads. There is a read data output for each counter in the timers module.

Figure 5-19 on page 5-31 shows the FRC HDL file.

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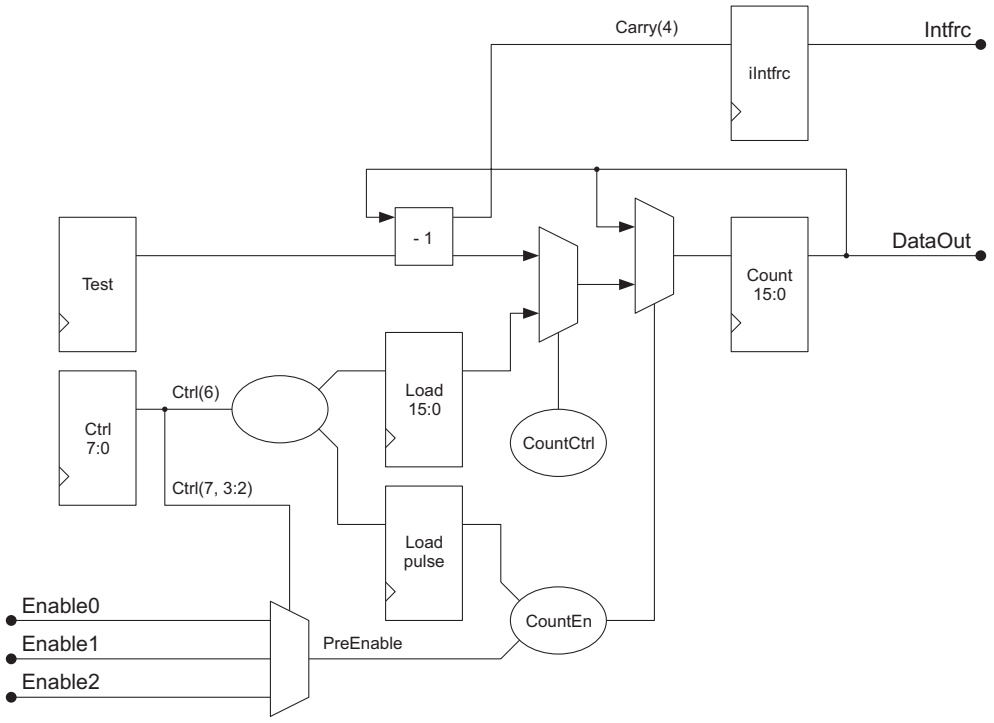

Figure 5-19 FRC module system diagram

The main sections in this module are described in:

- *Control, Test and Load registers*
- *Counter enable selection* on page 5-32
- *16-bit counter* on page 5-32
- *Interrupt generation* on page 5-33
- *Output data generation* on page 5-34.

Control, Test and Load registers

The Control, Test (bit zero only) and Load registers only change when written to, and hold their values at all other times.

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Counter enable selection

The enable input to use is selected according to the prescale mode setting in the control registers. The selected input is then used to generate an internal enable, which is also gated with the enable bit of the control registers. An additional signal ensures that the load data value is clocked into the counters when a load operation is performed.

16-bit counter

The counter is split up into four 4-bit parts (nibbles) to allow efficient testing. Each nibble is used to generate a carry signal (when the 4-bit counter overflows), which is passed to the next nibble as an enable. When Counter Test Mode is selected, all carry enable signals are set HIGH, forcing all four nibbles to count at the same time.

The 16-bit counter value is stored in registers, which are enabled using the externally generated counter enable. The input to the registers is normally the output from the four 4-bit decrementers, but when a new value is written to the Load registers, or when the counter reaches zero and periodic mode is set, the current value of the Load registers is stored in the counter registers.

The operation of the counter is shown in Figure 5-20 on page 5-33.

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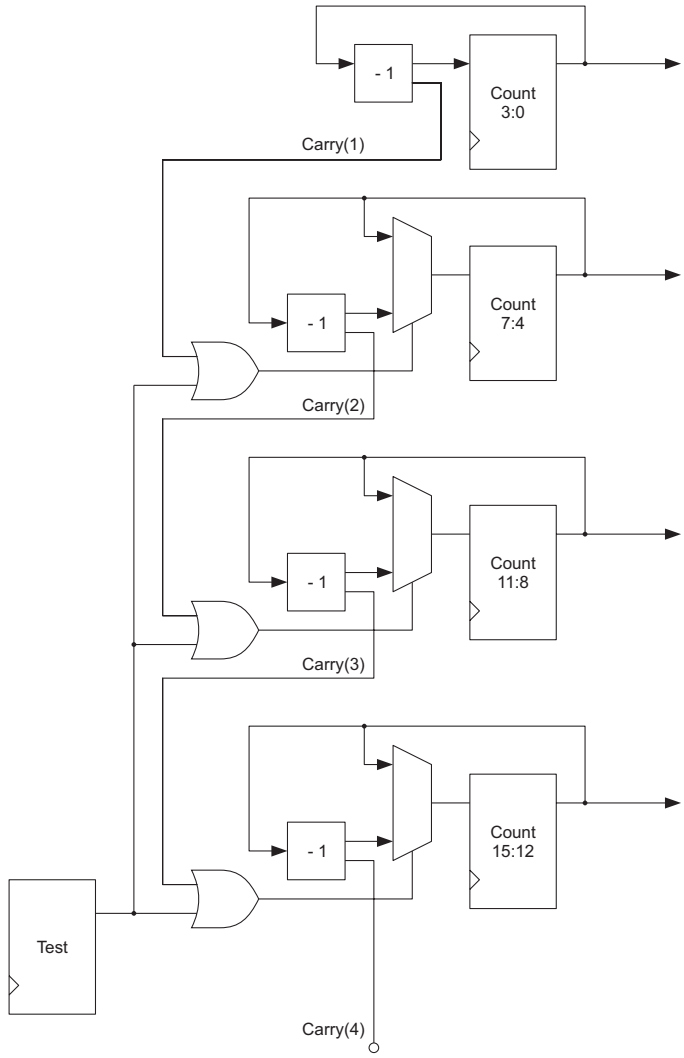

Figure 5-20 FRC module count down diagram

Interrupt generation

An interrupt is generated when the full 16-bit counter reaches zero, and is only cleared when the TimerClear location is written to. A register is used to hold the value until the interrupt is cleared. The most significant carry bit of the counter is used to detect the counter reaching zero.

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Output data generation

The current address is used to generate the internal read data value for the Test, Load, Value and Control locations. Because the Test and Control registers are not 16-bits, the read values are padded out with the Load register value, minimizing the number of output changes when different registers are read.

This read data value is then passed to the timers module, and then driven onto the APB read data bus.

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5.4 Peripheral to bridge multiplexor

The peripheral to bridge multiplexor module is used to connect the read data outputs of the peripheral bus slaves to the peripheral bus bridge module, using the **PSELx** select signals to select the bus slave outputs to use. Figure 5-21 shows an interface diagram for the peripheral to bridge multiplexor module.

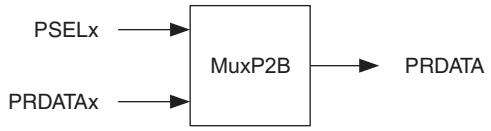

Figure 5-21 Peripheral to bridge multiplexor module interface diagram

This module is a simple multiplexor, with the read data buses from all peripheral bus slaves as the inputs, using the slave select bridge outputs as the select inputs, with a single read data bus as the output to the bridge module. When slaves are added to the system or removed, the input connections to this module must be altered to account for the changes.

5.4.1 Signal descriptions

Table 5-10 shows the signal descriptions for the peripheral to bridge multiplexor module.

Table 5-10 Signal descriptions for peripheral to bridge multiplexor module

Signal	Type	Direction	Description
PSELx	Slave select	Input	Each APB slave has its own slave select signal, and this signal indicates that the current transfer is intended for the selected slave.
PRDATAx[31:0] **PRDATA[31:0]**	Read data bus	Input/ output	The read data bus is used to transfer data from bus slaves to the bridge during read operations.

5.4.2 Function and operation of module

The peripheral to bridge multiplexor controls the routing of read data from the peripheral bus slaves to the bridge. The bridge determines which is the currently selected slave, and the multiplexor is used to connect the output of the selected slave to the input of the bridge.

The read data is switched for the duration of an APB transfer, when the **PSELx** signal is valid.

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A default value of zero is used when no slaves are selected.

5.4.3 System description

The following paragraphs give a description of how the HDL code for the peripheral to bridge multiplexor is set out. A simple system block diagram, with information about the main parts of the HDL code, is followed by details of the registers, inputs, and outputs used in the module. This part should be read together with the HDL code.

Figure 5-22 shows the peripheral to bridge module block diagram.

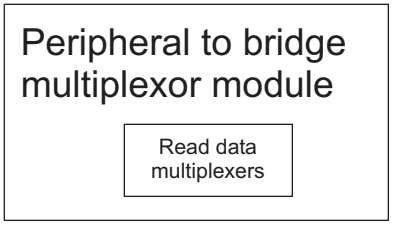

Figure 5-22 Peripheral to bridge multiplexor module block diagram

The peripheral to bridge multiplexor module is comprised of a set of multiplexors for the slave read data.

A diagram of the peripheral to bridge multiplexor HDL file is shown in Figure 5-23.

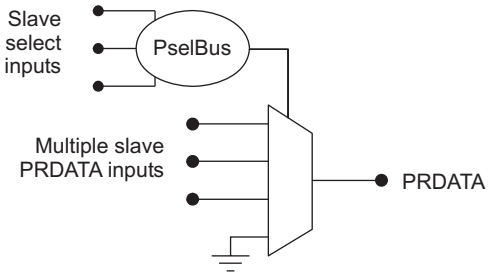

Figure 5-23 Peripheral to bridge multiplexor module system diagram

To allow the use of case statements for the multiplexors, the **PSEL** slave select inputs are combined to create a multi-bit bus signal. This bus is then used as the select control on the read data multiplexor.

One input to the PRDATA multiplexor is tied LOW, so that when no peripheral slaves are selected, no read data appears on **PRDATA**.

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Chapter 6
Behavioral Modules

This chapter describes the behavioral modules found in the *AMBA University Kit* (AUK). The behavioral modules are only available for use during system simulation, because they all read in or generate locally stored data files. This chapter contains the following sections:

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6.1 External RAM

The external RAM module is a simple model of a 32K x 8 off-chip SRAM, which can be initialized with data from a local file.

Figure 6-1 shows the external RAM module interface.

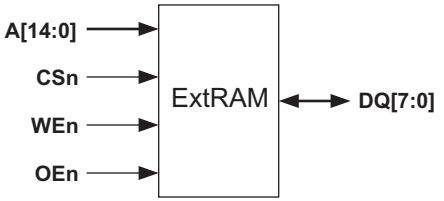

Figure 6-1 External RAM module interface diagram

The main sections of this module are:

- memory initialization from local data file
- memory read and write from external bus.

6.1.1 Signal descriptions

Table 6-1 shows the signal descriptions for the external RAM module.

Table 6-1 Signal descriptions for the external RAM module

Signal	Type	Direction	Description
A[14:0]	External address	Input	The external address input.
DQ[7:0]	External data I/O	Input/ output	The external data bus, sampled during write transfers and driven during read transfers.
CSn	Chip enable	Input	When LOW this signal indicates that the chip has been selected and must respond to the current transfer.
WEn	Write enable	Input	When LOW this signal indicates a write transfer.
OEn	Output enable	Input	When LOW this signal indicates a read transfer, and enables the module to drive data onto DQ.

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6.1.2 User-defined settings

Table 6-2 shows the user-defined settings for the external RAM module.

Table 6-2 User-defined settings for the external RAM module

Signal	Type	Default setting	Description
RAMDEPTH	Memory depth	32	This sets the memory depth in KB. If the value is increased from the default setting, the address input bus A must also be increased to allow all memory to be addressed.

6.1.3 Function and operation of module

Operations described are:

- *Memory initialization from local data file*
- *Memory read and write from external bus*.

Memory initialization from local data file

On simulation initialization, the external RAM module loads in data from the file specified in the instantiating top-level memory module. This must be stored as a two-hex character per line data file, which cannot contain more data than the model supports. An example file `ram.dat` is shown in Example 6-1.

Example 6-1

```
00
01
0F
F7
```

The default configuration for the external RAM modules is in groups of four, which are used to allow memory accesses of full 32-bit words, with a byte stored in each memory module.

Memory read and write from external bus

The external RAM is accessed by transfers through the static memory interface module, allowing both reads from memory and writes to memory. These are performed as 32-bit word transfers, with each byte connected to one of the four memory models.

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See *Static memory interface* on page 4-51 for timing diagrams showing read and write transfers to external memory.

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6.2 External ROM

The external ROM module is a simple model of a 16K x 8 off-chip EPROM, which can be initialized with data from a local file.

Figure 6-2 shows the external ROM module interface.

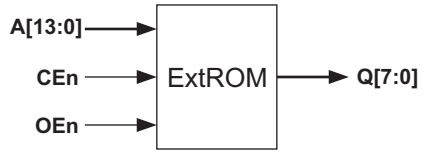

Figure 6-2 External ROM module interface diagram

The main sections of this module are:

- memory initialization from local data file
- memory read from external bus.

6.2.1 Signal descriptions

on page 6-8Table 6-3 shows signal descriptions for the external ROM module.

Table 6-3 Signal descriptions for the external ROM module

Signal	Type	Direction	Description
A[13:0]	External address	Input	The external address input.
Q[7:0]	External data out	Output	The external data bus, driven during read transfers.
CEn	Chip enable	Input	When LOW this signal indicates that the chip has been selected and must respond to the current transfer.
OEn	Output enable	Input	When LOW this signal indicates a read transfer, and enables the module to drive data onto **Q**.

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6.2.2 User-defined settings

Table 6-4 shows user-defined settings for the external ROM module

Table 6-4 User-defined settings for the external ROM module

Signal	Type	Default setting	Description
ROMDEPTH	Memory depth	16	This sets the memory depth in KB. If the value is increased from the default setting, the address input bus A must also be increased to allow all memory to be addressed.

6.2.3 Function and operation of module

Operations described are:

- *Memory initialization from local data file*
- *Memory read from external bus*.

Memory initialization from local data file

On simulation initialization, the external ROM module loads in data from the file specified in the instantiating top-level memory module. This must be stored as a two-hex character per line data file, which cannot contain more data than the model supports. An example file `rom.dat` is shown in Example 6-2.

Example 6-2

```
00
01
0F
F7
```

The default configuration for the external ROM modules is in groups of four, which are used to allow memory accesses of full 32-bit words, with a byte stored in each memory module.

Memory read from external bus

The external ROM is accessed by transfers through the static memory interface module, allowing reads from memory. These are performed as 32-bit word transfers, with each byte connected to one of the four memory models.

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See *Static memory interface* on page 4-51 in AHB Modules, for timing diagrams showing read and write transfers from external memory.

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6.3 Internal RAM

The internal RAM is a simple little-endian model of a 1KB x 32 on-chip SRAM, which can be initialized with data from a local file. The AHB internal RAM is shown in Figure 6-3.

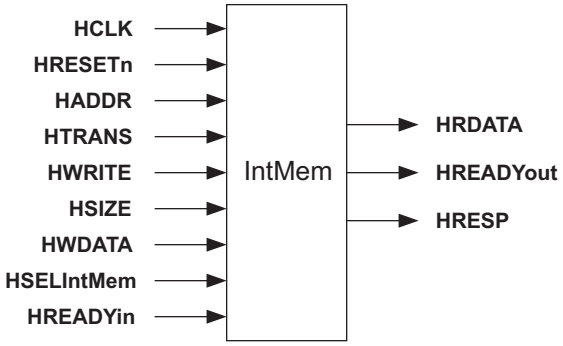

Figure 6-3 AHB internal RAM module interface diagram

The main sections of this module are:

- memory initialization from local data file
- memory read and write from system bus.

6.3.1 AHB signal descriptions

Table 6-5 shows signal descriptions for the AHB internal RAM module

Table 6-5 Signal descriptions for the AHB internal RAM module

Signal	Type	Direction	Description
HCLK	Bus clock	Input	This clock times all bus transfers.
HRESETn	Reset	Input	The bus reset signal is active LOW, and is used to reset the system and the bus.
HADDR[31:0]	Address bus	Input	The 32-bit system address bus.
HTRANS[1:0]	Transfer type	Input	Indicated the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	Transfer direction	Input	When HIGH this signal indicates a write transfer, and when LOW, a read transfer.

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Table 6-5 Signal descriptions for the AHB internal RAM module (continued)

Signal	Type	Direction	Description
HSIZE[2:0]	Transfer size	Input	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit). The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
HWDATA[31:0]	Write data bus	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this can easily be extended to allow for higher bandwidth operation.
HSELIntMem	Slave select	Input	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave. This signal is simply a combinatorial decode of the address bus.
HRDATA[31:0]	Read data bus	Output	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this can easily be extended to allow for higher bandwidth operation.
HREADYin HREADYout	Transfer done	Input / output	When HIGH the **HREADY** signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP[1:0]	Transfer response	Output	The transfer response provides additional information on the status of a transfer. This module always generates the OKAY response.

6.3.2 User-defined settings

Table 6-6 shows user-defined settings for the external RAM module

Table 6-6 User-defined settings for the external RAM module

Signal	Type	Default setting	Description
MemSize	Memory size	1	This sets the memory size in KB.
FileName	Input filename	`intram.dat`	This points to the local input data file that is read in after reset.

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6.3.3 Function and operation of module

Operations described are:

- *Memory initialization from local data file*
- *Memory read and write from system bus*.

Memory initialization from local data file

On simulation initialization, the internal RAM module loads in data from the file specified in the `FileName` setting. This must be stored as an 8-character Verilog `$readmemh` format data file (for both VHDL and Verilog format models), which cannot contain more data than the model supports. Address lines (starting with `@`) and single line comments (starting with `//`) are valid, but all other non-value characters are not allowed. Loading starts from address zero, and continues incrementing on word boundaries until an address line is found in the file. Loading then continues from that address. All values are initialized to zero before loading is started. An example `intram.dat` file is shown in Example 6-3.

Example 6-3

```
ea00000b
ea000005
// Data values stored at 0x00000200
@00000200
01234567
89ABCDEF
```

The internal RAM module stores data as 32-bit words, and in default configuration is 256 words deep, which is equivalent to 1KB. This is only accessible when the normal memory map is in use (**Remap** set HIGH), and occupies the address range from `0x00000000` to `0x000003FF`. If the size of the internal memory is modified, the address range that it occupies also changes. This requires the system decoder to be updated so that it only selects the internal RAM module over the correct address range.

Memory read and write from system bus

The internal RAM module is accessed by standard system bus transfers, allowing both reads from memory and writes to memory. These can be performed as 32-bit word, 16-bit halfword or 8-bit byte transfers. Each byte lane of the transfer is treated separately, so a byte write to byte zero does not alter the values stored in the other three bytes at that word address. Data reads are all treated the same, and the full 32-bit word at the selected word address is driven out onto the system data bus.

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All transfers are performed with zero wait states. An ERROR response is never generated.

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6.4 Test interface driver

The test interface driver (Ticbox) is an external module which drives the test interface lines to gain access to the AHB bus, and then applies test vectors from a test input file. This test input file is the output from a C program written with the TICTalk command language.

Before reading this section, you should be familiar with AMBA and its test interface protocol. If not, see the *AMBA Specification* for more information. Figure 6-4 shows an interface diagram of the ticbox module.

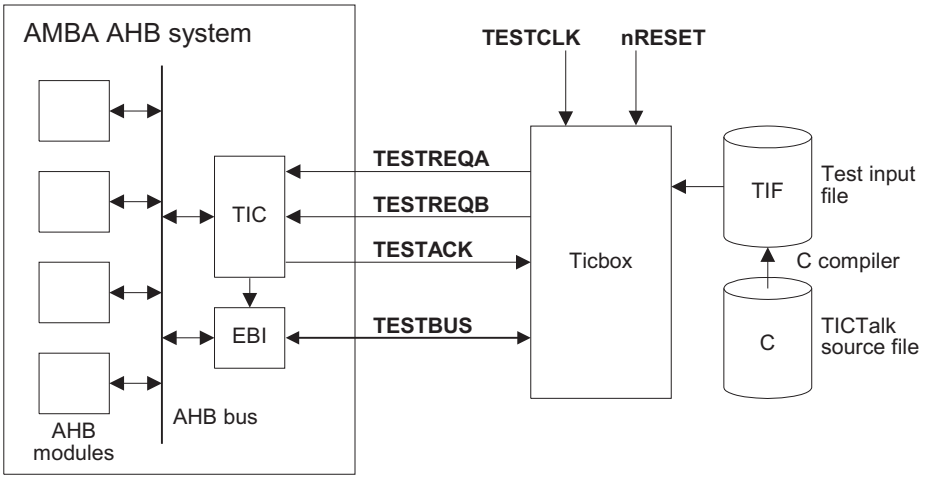

Figure 6-4 Ticbox module interface diagram

The main sections of this module are:

- the input file reader
- output vector generation
- read data expected value checking.

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6.4.1 Signal descriptions

Table 6-7 shows signal descriptions for the Ticbox module

Table 6-7 Signal descriptions for the Ticbox module

Signal	Type	Direction	Description
TESTCLK	Test mode clock	Input	This is the system clock **HCLK** in test mode. All the test interface transactions are timed using this signal.
nReset	External reset	Input	Active LOW external reset input. Used to control the operation of the Ticbox module.
TESTREQA	Test request A	Output	Indicates test vector mode. See the test interface chapter in the *AMBA Specification* for more information about the test protocol. It is driven early in the LOW phase of **TESTCLK** and held to the falling edge of **TESTCLK**.
TESTREQB	Test request B	Output	Indicates test vector mode. See the test interface chapter of the *AMBA Specification* for more information about the test protocol. It is driven early in the LOW phase of **TESTCLK** and held to the falling edge of **TESTCLK**.
TESTACK	Test acknowledge	Input	Indicates that the test bus has been granted and also that a test access has been completed.
TESTBUS[31:0]	Test data bus	Input/ output	32-bit bidirectional test port.

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6.4.2 User-defined settings

Table 6-8 shows user-defined settings for the Ticbox module

Table 6-8 User-defined settings for the Ticbox module

Name	Type	Default setting	Description
FileName	Input filename	`infile.tif` (VHDL) `infile.sim` (Verilog)	This points to the local input vector file that is read in a line at a time as each vector is performed.
HaltOnMismatch	Read error setting	FALSE	This is used to control the operation of the module when a read error is detected. When set FALSE, a warning message is displayed showing the read error, and if set TRUE, the simulation is halted when a read error is detected.
Verbosity	Comment display	TRUE	Controls the displaying of input vector file comments. When set TRUE, comments are displayed, and when set FALSE, comments are not displayed. This does not affect the displaying of other system messages.

6.4.3 Function and operation of module

When the external system reset input has been deasserted, the Ticbox requests access to the system. This is done by asserting **TESTREQA** HIGH and **TESTREQB** LOW. The *Test Interface Controller* (TIC) then indicates when test mode has been entered by asserting **TESTACK** HIGH. When in test mode, the test input file is then read and translated by the Ticbox into AMBA test interface transactions, using the **TESTREQA** and **TESTREQB** signals.

The Ticbox applies test vectors to the system every time the **TESTACK** line indicates the system is ready. On read cycles the value is masked and then compared with the masked expected value given in the test vector file. An error message is given if the comparison fails. System testing ends when the end of the input vector file is reached, and the Ticbox indicates this by asserting both **TESTREQA** and **TESTREQB** LOW to end the simulation.

A typical simulation output display while running a TIC program is shown in Example 6-4.

Example 6-4

```
#    Time: 2603 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Addressing location 80000614
```


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```
#    Time: 2703 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Writing data 00000005

#    Time: 3003 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Addressing location 80000618

#    Time: 3103 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Reading. Expected: 00000010. Mask 0000003F

#    Time: 3403 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Addressing location 8000061c

#    Time: 3703 ns Iteration: 0 Instance:/u_ticbox
# ** Warning: Error on vector read. Expected: 00000010 Actual: 00000011 Mask:
0000003F
#    Time: 3753 ns Iteration: 0 Instance:/u_ticbox

#    Time: 4003 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Addressing location 80000584

#    Time: 4303 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Writing data 00000000

#    Time: 4603 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Addressing cycle at end

#    Time: 4903 ns Iteration: 0 Instance:/u_ticbox
# ** Note: ; Exiting Test Mode

#    Time: 5203 ns Iteration: 0 Instance:/u_ticbox
# ** Failure: Vector run completed: halting simulation
#    Time: 77703 ns Iteration: 0 Instance:/u_ticbox
# Break at ticbox.vhd line 288
```

In Example 6-4 on page 6-14, a read error has occurred, but the error message is broadcast later in the simulation. This is because there are a number of clock cycles between when the read is requested, and when the information is sampled by the Ticbox to be compared with the expected value. The example simulation has been run without HaltOnMismatch set, and therefore the program does not stop after the error has been detected. Verbosity is set, because all TIF vector comments have been displayed in the simulation output.

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6.4.4 TICTalk command language

TICTalk is a very simple set of commands that allows the development of validation programs for the AMBA blocks. The TICTalk language is a small library of C functions. When a TICTalk program is compiled and run, it produces a test input file in what is called the *TIC Interface Format* (TIF) which can be applied using the Ticbox module to test the desired block.

The AMBA test interface is able to perform the following actions:

- address vector
- write vector
- burst of write vectors
- read vector
- burst of read vectors
- change from write to read and read to write.

The TICTalk language performs these actions by combining together a number of basic commands. These commands are described in the following sections.

6.4.5 TICTalk commands

The basic TICTalk commands are described in the following sections:

- *Write address vector (A)*
- *Write test vector (W)*
- *Read test vector (R)* on page 6-17
- *Burst read test vector (B)* on page 6-17
- *Repeat last command (L)* on page 6-17
- *Include the string message into the TIF (C)* on page 6-17
- *Exit test mode (E)* on page 6-17.

Write address vector (A)

The `A(int32 address_vector)` command is used to address a new location in the system. It is always followed by a write test vector, or a read test vector command to perform the required action (write or read data) at that location.

Write test vector (W)

The `W(int32 write_vector)` command generates a data vector write. It can be used after an address vector (single write), another write test vector (burst write) or a read test vector (change from reads to writes).

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Read test vector (R)

The `R(int32 expected_value, int32 mask_value)` command generates a data vector read. The read value is masked with the specified `mask_value` and compared with the `expected_value`. If the comparison is false, an error message is broadcast. It can be used after an address vector (single read), or a write test vector (change from writes to reads), and to indicate the last read on a burst, but it cannot be used after another read test vector. To signal a burst sequence of reads, the burst read vector command must be used instead.

Burst read test vector (B)

The `B(int32 expected_value, int32 mask_value)` command is similar to the read test vector. The only difference is that it can only be used if the next action is another read. This is because, in this case, a change of bus direction is not needed. Otherwise the function performed is the same.

Repeat last command (L)

The `L(int32 number_of_loops)` command signals that the last action must be repeated the specified number of times. This is useful when, for example, a burst of reads or writes from the same address location needs to be performed.

Include the string message into the TIF (C)

The `C(char * message)` command is used to add extra simulation comments.

Exit test mode (E)

The `E()` command must always be used at the end of a program so the Ticbox can signal the end of the test.

6.4.6 Programming with TICTalk commands

The possible combinations that are available when using the TICTalk commands are:

Single writes The command sequence is: `A-W A-W A-W`, and so on.

Single reads The command sequence is: `A-R A-R A-R`, and so on.

Burst of writes The command sequence is: `A-W-W-W`, and so on.

If the value to be written is always the same, the command sequence could also be `A-W-L`, specifying on the `L` command the number of writes required.

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Burst of reads This is a special case. After the A command, B (burst read vector) should be used on consecutive reads, and only on the last read of the burst do we apply the R command. Therefore the sequence is: A-B-B-B-R A-B-B-....-B-R, and so on.

If the value to be read is expected always to be the same, or there is no requirement to check it against an expected value, the sequence could also be A-B-L-R, with the L command specifying the number of reads required.

Change from read to write

This change can only be made after a R command (R-W), and not after a B command.

Change from write to read

If the change is for a single read, the sequence W-R is used. On the other hand if the change is for a read burst, the W-B sequence is used (W-B-B-...-B-R).

6.4.7 The TICTalk file

An example C program using the TICTalk commands is shown in Example 6-5.

Example 6-5

```
#define CT1Load     Counter_Base + 0x00
#define CT1Value    Counter_Base + 0x04
#define CT1Control  Counter_Base + 0x08
#define CT1Clear    Counter_Base + 0x0C
#define CT1Test     Counter_Base + 0x10

#define MaskAll     0x00000000
#define NoMask      0xFFFFFFFF
#define MaskControl 0x000000CC
#define MaskValue   0x0000FFFF
#define DUMMY       0x12345678

#include “header.h”
#include “ticmacros.h”

int main()
{
  A(CT1Load)
  W(0x55555555)
  A(CT1Control)
  W(0x000000C0) /* Counter Enabled, Periodic Mode, Prescale 0 */
```

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```
  A(CT1Value)
  R(0x55555547, MaskValue)
  A(CT1Load)
  W(0xDADADADA)
  B(0xDADADADA, MaskValue)    /* Read CT1Value */
  R(0x000000C0, MaskControl)  /* Read CT1Control */
  A(CT1Value)
  R(0xAAAAAAB8, MaskAll)
  W(0x000000C4)          /* Write to CT1Control */
  W(DUMMY)               /* Write to CT1Clear   */
  L(5)                   /* Repeat last write 5 times */
  E()
}
```

Example 6-5 on page 6-18 shows the TICTalk commands accept 32-bit integers as arguments. These can be specified using the `#define` directive, immediate values or normal C variables. This C-like approach provides the flexibility to develop more elaborate tests and new extended functions. For example, the basic commands could be used to build a pair of functions for reading and writing vectors that automatically take care of bus turnaround and address vectors.

The `ticmacros.h` file includes all the macro definitions for each command. These macros are expanded to generate a test input file in a format that can be read by the Ticbox.

The `header.h` file contains the base address definitions for the different blocks in the system. This is where the `Counter_Base` constant should be defined. This ensures portability of the test program to other systems with different peripheral address mapping.

6.4.8 Generating a test input format file

To generate a TIF file, the TICTalk program must be C compiled (using `gcc` for example) in the following way:

```
gcc -ansi source_file ticmacros.c -o object_file
```

Afterwards the object_file must be run and its output redirected to a file with the same name as the generic variable *FileName* defined in the Ticbox, for example:

```
object_file > infile.tif
```

This output file must then be copied or linked to the directory where the Ticbox simulation model exists.

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6.4.9 TIF format file

The TIF file is very similar to the TICTalk file as shown in Example 6-6, with the difference that all the constant definitions have been substituted with their hexadecimal values and each line reflects a single test cycle. The previous example compiled and executed outputs the following TIF. Lines preceded with a semicolon (;) are comments that the simulator prints on the screen while the test is being executed.

Example 6-6

```
; Addressing location 84000000
A 84000000
; Writing data 55555555
W 55555555
; Addressing location 84000008
A 84000008
; Writing data 000000C0
W 000000C0
; Addressing location 84000004
A 84000004
; Reading. Expected: 55555547. Mask: 0000FFFF
R 55555547 0000FFFF
A ZZZZZZZZ
; Addressing location 84000000
A 84000000
; Writing data DADADADA
W DADADADA
; Reading. Expected: DADADADA. Mask: 0000FFFF
R DADADADA 0000FFFF
; Reading. Expected: 000000C0. Mask: 000000CC
R 000000C0 000000CC
A ZZZZZZZZ
; Addressing location 84000004
A 84000004
; Reading. Expected: AAAAAAB8. Mask: 00000000
R AAAAAAB8 00000000
A ZZZZZZZZ
; Writing data 000000C4
W 000000C4
; Writing data 12345678
W 12345678
; Looping for 5 cycles
L 5
; Addressing cycle at end
A 00000000
; Exiting Test Mode
```


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```
E ZZZZZZZZ
```

6.4.10 SIM format file

The Verilog Ticbox requires the input file to be in the SIM format, which is formatted as a Verilog `include input file, with each test vector calling a task in the Verilog Ticbox behavioural module.

A SIM file is generated from a TIF file using the conversion script tif2sim in the following way:

```
tif2sim infile.tif > infile.sim
```

Comments use the Verilog style double slash (//) and, because of the properties of Verilog `include files, are not displayed in the simulation output. The Verilog Ticbox directly generates the simulation comments based on the test vector that is being run.

The TIF file above is shown in Example 6-7 in SIM format:

Example 6-7

```
// Addressing location 84000000
A(32'h84000000);

// Writing data 55555555
W(32'h55555555);

// Addressing location 84000008
A(32'h84000008);

// Writing data 000000C0
W(32'h000000C0);

// Addressing location 84000004
A(32'h84000004);

// Reading. Expected: 55555547. Mask: 0000FFFF
R(32'h55555547, 32'h0000FFFF);
A(32'hZZZZZZZZ);

// Addressing location 84000000
A(32'h84000000);

// Writing data DADADADA
W(32'hDADADADA);
```


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```
// Reading. Expected: DADADADA. Mask: 0000FFFF
R(32'hDADADADA, 32'h0000FFFF);

// Reading. Expected: 000000C0. Mask: 000000CC
R(32'h000000C0, 32'h000000CC);
A(32'hZZZZZZZZ);

// Addressing location 84000004
A(32'h84000004);

// Reading. Expected: AAAAAAB8. Mask: 00000000
R(32'hAAAAAAB8, 32'h00000000);
A(32'hZZZZZZZZ);

// Writing data 000000C4
W(32'h000000C4);

// Writing data 12345678
W(32'h12345678);

// Looping for 5 cycles
L(32'd5);

// Addressing cycle at end
A(32'h00000000);

// Exiting Test Mode
E(32'hZZZZZZZZ);
```

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6.5 Tube

The tube is a simple method of passing system messages from a test program to the display, and allows a test program to stop the simulation.

Figure 6-5 shows the tube module interface.

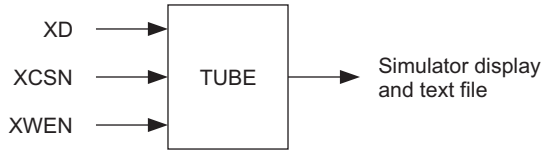

Figure 6-5 Tube module interface diagram

The main sections of this module are:

- message output to simulator
- message output to file
- simulation termination control.

6.5.1 Signal descriptions

Table 6-9 shows signal descriptions for the tube module.

Table 6-9 Signal descriptions for the tube module

Signal	Type	Direction	Description
XD[31:0]	External data	Input	This is the external data bus, which is sampled by this module during write transfers.
XCSN[3:0]	External chip select	Input	These signals are active LOW chip enables.
XWEN[3:0]	External write enable	Input	This is the active LOW memory write enable. For little-endian systems, **XWEN[0]** controls writes to the least significant byte and **XWEN[3]**, the most significant. The example system is configured to be little-endian.

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6.5.2 User-defined settings

Table 6-10 shows user-defined settings for the tube module

Table 6-10 User-defined settings for the tube module

Signal	Type	Default setting	Description
OutFile	Output filename	`Tube.txt`	This points to the local output data file that is written to during simulation when messages are passed to the tube.

6.5.3 Function and operation of module

The tube module is used to perform program message and simulation termination control. It acts as a one-way communications port through which ASCII information can be passed.

Messages are written, one byte at a time, to the tube model location. In the default system this is address range `0x20000000` to `0x2FFFFFFF`, detected by the model using the external enable **XCSN[2]**. These bytes are buffered until a terminating control character is written to the tube, or the buffer overflows (default buffer length is 80 characters). The message is then printed by the simulator, and written to the output text file. An example message is:

```
# ** Note: TUBE: Hard Reset
```

In this example the message `Hard Reset` has been passed to the tube. The program running on the microcontroller can also terminate simulation by writing a control character to the tube with no message to produce the following assertion:

```
# ** Failure: TUBE: Program exit
```

All user messages sent to the simulator display are also recorded in the output text file.

The tube module only accepts the ASCII control characters shown in Table 6-11.

Table 6-11 Valid tube ASCII control characters

ASCII character	Decimal value	Tube function
Control D (^D)	04	Exit test
Linefeed	10	Print output
Carriage return	13	Print output

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Other standard alphanumeric characters are stored in the buffer until displayed. The values for commonly used display characters are shown in Table 6-12.

Table 6-12 Commonly used ASCII alphanumeric characters

ASCII character	Decimal value
0-9	48-57
a-z	97-122
A-Z	65-90
space	32
_	95
#	35

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Chapter 7
Designer's Guide

This chapter briefly describes adding new modules to the EASY microcontroller. Since AMBA has been designed specifically to be modular, little change needs to be made to other elements when a component is added or removed. The chapter contains the following sections:

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7.1 Adding bus masters

For bus masters, the arbiter is the only block that requires changes.

The arbiter currently has facilities for up to two more masters without any modification. A new master needs to be connected to the appropriate **HBUSREQx** and **HGRANTx** signals. This can be done by altering the top-level HDL file, which connects all AHB modules together.

Note

If a system requires more than four masters, the arbiter HDL file also has to be modified.

7.1.1 Arbiter modifications

When modifying the arbiter the following rules must be followed:

- The ARM core must be the default master (granted on reset), and granted when no masters are requesting the bus.
- The *Test Interface Controller* (TIC) must have the highest priority (to allow test access under all conditions).
- Only one master should tie its **HBUSREQx** permanently HIGH.
- Currently the ARM bus master always asserts **HBUSREQx**, therefore no other bus master should constantly request the bus. Consequently the ARM must be the lowest priority master, because masters of lower priority than the ARM are never granted.

If more sophisticated *round-robin* type arbitration schemes are used, the latter point is no longer valid. Alternative arbitration schemes are not considered further in this document.

7.1.2 Bus master requirements

New designs of bus master must drive all the relevant signals at appropriate times. For more information consult the *AMBA Specification*.

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7.2 Adding AHB slaves

When a slave is added, the decoder needs to be modified. This adds an **HSELx** signal for the new slave. The central slave to master multiplexor must also have extra connections added for the new slave.

7.2.1 AHB slave modifications

When adding new AHB slaves, care must be taken to:

- plan the slave position in the memory map
- consider any issues concerning the remapping of memory to allow the external boot ROM to appear at location zero
- decode as few address lines as possible, to keep the slave address decode section gate count low
- ensure that all areas of address space have one, and only one, slave selected.

The default slave must be set so that all holes in the memory map are filled. If any holes are left without a slave to drive the **HREADY** line, any accesses to this area cause the system to lock, with **HREADY** staying LOW until a system reset.

7.2.2 Slave requirements

These vary according to the function of the slave. Special cases like external bus interfaces (which must also consider the requirements of the TIC), or the AHB to APB bridge interface have more complex requirements. For more information consult the *AMBA Specification*.

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7.3 Adding APB peripherals

When adding a peripheral, the APB bridge needs to be modified. This adds a new **PSELx** signal for the new peripheral. The central peripheral to bridge multiplexor must also have extra connections added for the new peripheral.

7.3.1 APB bridge modifications

When adding new **PSELx** lines, similar steps must be taken to those outlined in *AHB slave modifications* on page 7-3, although reset memory map is not an issue for APB peripherals.

7.3.2 Peripheral requirements

When designing APB peripherals, ensure that the resulting hardware has a low power consumption. The following guidelines must be followed where possible:

- Do not use **PCLK** in peripherals unless absolutely necessary because its use dramatically increases power consumption.
- Ensure that peripherals cannot drive **PRDATA[31:0]** during reset (by including a **PRESETn** term on the output enable control).

Designers familiar with conventional circuits connected to free-running clocks might find this design approach difficult. However, it results in small circuits with low power consumption.

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