ARM PrimeCell
AMBA 3 HP Matrix (PL301)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r1p2 of PL301 AMBA 3 HP Matrix

Proprietary notice

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM Limited in the EU and other countries, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM Limited in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM Limited shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Document confidentiality status

This document is Non Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Web address

http://www.arm.com/

Feedback on the product

If you have any comments or suggestions about this product, contact your supplier giving:

- The product name
- A concise explanation of your comments.

Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1   Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2   Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3   Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

08 Oct 2009: Changes in Document v12

Page	Status	ID	Cat	Summary
26	New	690568	Cat 2	QoS becomes active later than expected
27	New	722106	Cat 2	Slave interface transaction tracking logic can malfunction when attempting to exceed write acceptance capability
28	New	723115	Cat 2	WLAST before AW handshake on a single_active_slave interface deadlocks
51	New	671217	Cat 3	Pin specification in timing constraint exceptions does not capture all pins
52	New	701718	Cat 3	Automatic exceptions not rendered correctly when a sync down bridge is found between the core interconnect and a slave
54	New	720607	Doc	DDI0397E HPM (PL301) r1p2 TRM - TRM description of write issuing capability does not match RTL behaviour in all cases

19 Sep 2008: Changes in Document v11

Page	Status	ID	Cat	Summary
14	Updated	393332	Cat 2	Expander read re-order depth can be exceeded
15	Updated	395354	Cat 2	Possible deadlock condition with AHB bridges and downsizers
25	New	577318	Cat 2	Single slave per ID + single active write settings on a slave interface cause the read channel to lock up
48	New	561818	Cat 3	Incorrect stimulus addresses generated for APB configuration port
49	New	570866	Cat 3	Slave interface arbiter priorities changed between releases, resulting in extra latency
50	New	587269	Cat 3	IP-XACT XSL errors cause AMBA Designer stitch failures

01 May 2008: Changes in Document v10

Page	Status	ID	Cat	Summary
24	Updated	510518	Cat 2	RegdSyncUpAxi bridge deadlocks if first transaction arrives before the first CLKEN
34	Updated	423021	Cat 3	RTL generation issue when a Slave I/F sees the full 32-bit address range

03 Apr 2008: Changes in Document v9

Page	Status	ID	Cat	Summary
16	Updated	404614	Cat 2	HxUSER signals not registered by the optimised AHB to AXI bridge
20	Updated	456568	Cat 2	Transaction counter underflow when B handshake precedes AW handshake
33	Updated	422820	Cat 3	AXI-AHB bridge IDLE address unaligned

25 Mar 2008: Changes in Document v8

Page	Status	ID	Cat	Summary
24	New	510518	Cat 2	RegdSyncDnAxi bridge deadlocks if first transaction arrives before the first CLKEN
23	New	466785	Cat 2	Undriven inputs in configurations with a single slave interface and no ID bits

| 46 | New | 493515 | Cat 3 | Multiple instances connected in some mesh arrangements can deadlock |
| 43 | New | 471415 | Cat 3 | Inconsistency between documentation and RTL for arbitration programming through APB configuration port |

05 Dec 2007: Changes in Document v7

Page	Status	ID	Cat	Summary
22	New	460064	Cat 2	Unsynthesizable Verilog
21	New	460061	Cat 2	Slave interfaces being starved when master interface write FIFO fills up
45	New	481763	Cat 3	IP-XACT description does not match v1.2 bus definitions
39	Updated	446841	Cat 3	Configurations with 32 slave interfaces give Verilog compile warnings
32	Updated	422422	Cat 3	RTL uses undefined macros
31	Updated	421416	Cat 3	Master interfaces with AHB protocol and 0 USER bits may give synthesis warnings

03 Oct 2007: Changes in Document v6

Page	Status	ID	Cat	Summary
20	New	456568	Cat 2	Transaction counter underflow when B handshake precedes AW handshake

24 Jul 2007: Changes in Document v5

Page	Status	ID	Cat	Summary
31	New	421416	Cat 3	Master interfaces with AHB protocol and 0 USER bits may give synthesis warnings
32	New	422422	Cat 3	RTL uses undefined macros
33	New	422820	Cat 3	AXI-AHB bridge IDLE address unaligned
34	New	423021	Cat 3	RTL generation issue when a Slave I/F sees the full 32-bit address range
35	New	424365	Cat 3	Combinatorial path from RID/BID to RREADY/BREADY
37	New	436785	Cat 3	IP-XACT description issues with signal directions and naming
38	New	446839	Cat 3	AHB-Lite-Slave master interfaces cannot meet out-of-box timing
39	New	446841	Cat 3	Configurations with 32 slave interfaces give Verilog compile warnings
40	New	447585	Cat 3	Incorrect OVL assertions in axibm_decode_scheme_<design>.v for certain configurations
41	New	449412	Cat 3	Incorrect timing constraints on interfaces with unregistered Expander or Downsizer
42	New	450012	Cat 3	Missing -library option for set_driving_cell statement

30 Mar 2007: Changes in Document v4

Page	Status	ID	Cat	Summary
36	New	430627	Cat 3	QoS permanently active in some master interfaces

24 Jan 2007: Changes in Document v3

Page	Status	ID	Cat	Summary
19	New	419842	Cat 2	AxiToAhbSWrapper generates EXOKAY

| 18 | New | 415042 | Cat 2 | DownsizerAxi (4 to1) RRESP generation incorrect |
| 17 | New | 414732 | Cat 2 | Unlocking write issue when using the optimised AHB to AXI bridge |

19 Sep 2006: Changes in Document v2

Page	Status	ID	Cat	Summary
14	Updated	393332	Cat 2	Expander read re-order depth can be exceeded
15	Updated	395354	Cat 2	Possible deadlock condition with axibm core, ahb bridges and expander
16	New	404614	Cat 3	HxUSER signals not registered by the optimised AHB to AXI bridge
30	New	404615	Cat 3	Formality may report spurious warnings when optimised AHB to AXI bridge is used

11 Jul 2006: Changes in Document v1

Page	Status	ID	Cat	Summary
14	New	393332	Cat 2	Expander read re-order depth can be exceeded
15	New	395354	Cat 2	Possible deadlock condition with axibm core, ahb bridges and expander

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus $\boxed{\textbf{X}}$ indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p2-00rel0
720607	Doc	DDI0397E HPM (PL301) r1p2 TRM - TRM description of write issuing capability does not match RTL behaviour in all cases					X
393332	Cat 2	Expander read re-order depth can be exceeded	X				
395354	Cat 2	Possible deadlock condition with AHB bridges and downsizers	X				
404614	Cat 2	HxUSER signals not registered by the optimised AHB to AXI bridge		X	X	X	
414732	Cat 2	Unlocking write issue when using the optimised AHB to AXI bridge		X			
415042	Cat 2	DownsizerAxi (4 to1) RRESP generation incorrect		X			
419842	Cat 2	AxiToAhbSWrapper generates EXOKAY		X			
456568	Cat 2	Transaction counter underflow when B handshake precedes AW handshake		X	X	X	X
460061	Cat 2	Slave interfaces being starved when master interface write FIFO fills up			X	X	
460064	Cat 2	Unsynthesizable Verilog			X	X	
466785	Cat 2	Undriven inputs in configurations with a single slave interface and no ID bits			X	X	
510518	Cat 2	RegdSyncUpAxi bridge deadlocks if first transaction arrives before the first CLKEN		X	X	X	X
577318	Cat 2	Single slave per ID + single active write settings on a slave interface cause the read channel to lock up					X
690568	Cat 2	QoS becomes active later than expected			X	X	X
722106	Cat 2	Slave interface transaction tracking logic can malfunction when attempting to exceed write acceptance capability					X
723115	Cat 2	WLAST before AW handshake on a single_active_slave interface deadlocks					X

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p2-00rel0
404615	Cat 3	Formality may report spurious warnings when optimised AHB to AXI bridge is used		X	X	X	
421416	Cat 3	Master interfaces with AHB protocol and 0 USER bits may give synthesis warnings		X	X	X	
422422	Cat 3	RTL uses undefined macros		X			
422820	Cat 3	AXI-AHB bridge IDLE address unaligned		X	X	X	
423021	Cat 3	RTL generation issue when a Slave I/F sees the full 32-bit address range		X			
424365	Cat 3	Combinatorial path from RID/BID to RREADY/BREADY		X	X	X	X
430627	Cat 3	QoS permanently active in some master interfaces	X	X			
436785	Cat 3	IP-XACT description issues with signal directions and naming		X			
446839	Cat 3	AHB-Lite-Slave master interfaces cannot meet out-of-box timing		X			
446841	Cat 3	Configurations with 32 slave interfaces give Verilog compile warnings			X	X	
447585	Cat 3	Incorrect OVL assertions in axibm_decode_scheme_<design>.v for certain configurations		X			
449412	Cat 3	Incorrect timing constraints on interfaces with unregistered Expander or Downsizer			X	X	
450012	Cat 3	Missing -library option for set_driving_cell statement			X	X	
471415	Cat 3	Inconsistency between documentation and RTL for arbitration programming through APB configuration port			X	X	
481763	Cat 3	IP-XACT description does not match v1.2 bus definitions			X		
493515	Cat 3	Multiple instances connected in some mesh arrangements can deadlock	X	X	X	X	X
561818	Cat 3	Incorrect stimulus addresses generated for APB configuration port					X
570866	Cat 3	Slave interface arbiter priorities changed between releases, resulting in extra latency					X
587269	Cat 3	IP-XACT XSL errors cause AMBA Designer stitch failures					X

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p2-00rel0
671217	Cat 3	Pin specification in timing constraint exceptions does not capture all pins					X
701718	Cat 3	Automatic exceptions not rendered correctly when a sync down bridge is found between the core interconnect and a slave					X

Errata - Category 1

There are no Errata in this Category

Errata - Category 2

393332:   Expander read re-order depth can be exceeded

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r0p0-00rel0, Fixed in r1p0-00rel0.

Description

When PL301 is configured to use the ExpanderAxi on either the Master or Slave interface the "read data re-order depth" of the Expander Master interface could be exceeded.

Under certain combinations of AXI transaction this can lead to deadlock in the interconnect.

Implications

The interconnect can be deadlocked.

Workaround

When the expander is instantiated on the Slave Interface of the axi_bm_core, set the SlaveInterface read_acceptance_capability parameter to 2. This corresponds to setting the read_issuing_capability of the Master Params component in AMBA Designer to 2.

If the expander is instantiated on the Master Interface, there is no safe workaround, therefore it is recommended that the expander is NOT used on the Master Interface. The user can ensure that the expander is not instantiated on the MasterInterface by ensuring that PL301 is configured so that the MasterInterface data_width is less than or equal to the routing_data_width.

395354: Possible deadlock condition with AHB bridges and downsizers

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r0p0-00rel0, Fixed in r1p0-00rel0.

Description

A possible deadlock condition exists for any PL301 interconnect configuration that has: -

[1] a routing width of 32

[2] a slave interface with AHB protocol, data_width of 64 and register_io of 0

[3] a master interface with AHB protocol

This implies the following sequence of Interconnect Components: -

  AhbToAxi Bridge : DownsizerAxi ... AXI Bus Matrix ... AxiToAhb Bridge

If the AHB master attached to this slave interface attempts a SIZE64 write transaction to the AHB master interface that requires more than one transaction in the 32-bit domain (e.g. AWLEN of 15) it will deadlock.

The deadlock occurs because of a circular dependency between the 3 interconnect components: -

* the AhbToAxi bridge waits for an AXI address handshake before progressing the AHB data transfers of the transaction

* the DownsizerAxi cannot handshake this address until all the outgoing addresses have been handshaked.

* the AxiToAhb bridge accepts the first address but cannot accept any more addresses until the transaction of the first address completes.

* this transaction cannot complete because the AHB data transfers are stalled waiting for the address handshake that cannot happen until it completes.

Implications

The interconnect can be deadlocked

Workaround

Set the register_io for the AHB slave interface to 2. This will cause a register slice to be inserted after the AhbToAxi bridge, decoupling it from the DownsizerAxi and breaking the deadlock loop. It is important that the value is 2 rather than 1, as only a value of 2 will ensure a register slice is instantiated in the correct location to break the deadlock.

As this register is not necessarily required to achieve timing closure with the design, in some design flows a tool could automatically remove it. If your synthesis process or post-synthesis flow could remove this register in any manner you must ensure that is does not do so.

404614: HxUSER signals not registered by the optimised AHB to AXI bridge

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

The **HAUSER**, **HWUSER** and **HRUSER** signals are not registered by the AHB-Lite to AXI bridge optimised for memory and so their stability during the AXI transactions from the master interface of the bridge is not ensured. As the AHB master connected to the AHB slave interface cannot determine the state of the AXI interface from the state of the AHB interface, it is not possible to ensure that the AXI **xUSER** signals are held stable or change at the correct times by enforcing behaviour of the **HxUSER** signals.

Implications

As a result the **HxUSER** signals should not be used. The signals remain on the interface when a memory optimised bridge is instantiated by the configuration, but the signals should be tied to a constant value in the case of inputs and left unconnected in the case of outputs.

Workaround

There is no workaround for this issue. The **HxUSER** signals should not be used on any interface for which the AHB-Lite to AXI bridge optimised for memory is selected.

414732: Unlocking write issue when using the optimised AHB to AXI bridge

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

This defect relates to a slave interface that has been configured to use the AHB-lite to AXI bridge optimised for memory controllers. This is the case when AMBA Designer is used to configure the `interface_protocol` parameter for the master parameters configuration component to be `ahb_lite_mem`.

An unlocking transfer can be missed if the following sequence occurs:

1) A locked sequence to the bridge

2) One or more unlocked transfers to another slave

3) An individual locked transfer to the bridge (preceded by zero or more locked idles)

If the non-sequential address of the individual locked transfer (point 3) is received before the unlocking AXI transaction from the first sequence has completed, the unlocking transaction for the second sequence can be missed leaving the interconnect locked. If the interconnect is left locked, accesses to the locked slave from other masters may wait indefinitely.

Implications

The defect may lead to the interconnect not being unlocked at the end of the AHB locked sequence. This would prevent other masters from accessing the 'locked' slave and could result in deadlock.

Workaround

This problem can be avoided by not using locked transfers in situations where the bridge can be deselected.

The problem will only arise if a master (or arbiter) allows individual locked transfers to occur to the bridge.

415042: DownsizerAxi (4 to1) RRESP generation incorrect

Status

Affects:　　　　　Product PL301 AMBA 3 HP Matrix .

Fault status:　　　Cat 2, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

This defect relates to the generation of the RRESP on the slave interface when downsizing 128-bit or 64-bit READ transactions. When downsizing, multiple read data transfers on the master interface are combined to generate one read data transfer on the slave interface. The RRESPs of the multiple transfers on the master interface are collated to determine the RRESP on the slave interface.

In a sequence of read data transfers, this collation of RRESPs is failing once a SLVERR or DECERR has been received from the slave. The failure results in RESPs on the slave interface which should be OKAY being reported as SLVERR or DECERR. The defect only affects responses to transfers within the same originating transaction.

Implications

This defect will result in the Downsizer indicating to a master that the result of a READ transaction has not completed successfully (RRESP is DECERR or SLVERR), when in fact the READ was completed successfully (RESP is OKAY).

Workaround

None known at this time other than to prevent the slave from issuing DECERR or SLVERR RESPs.

419842: **AxiToAhbSWrapper generates EXOKAY**

Status

Affects:　　　　　　Product PL301 AMBA 3 HP Matrix .

Fault status:　　　　Cat 2, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

This defect can cause an incorrect response to be given to an attempted exclusive access to an AHB slave. Non-exclusive and LOCKed transactions are unaffected.

The AXI-to-AHB bridges which provide access to AHB slaves do not include exclusive access monitor functionality, so cannot correctly report whether exclusivity has been maintained.

If an exclusive access is attempted through one of these bridges, the exclusivity will be ignored and the transaction performed on the AHB side of the bridge as the documentation correctly states. If the slave reports an error, this will be correctly turned into a 'SLVERR' response. If the slave reports that the transaction completed successfully then an 'EXOKAY' response will be returned by the AXI side of the bridge. This is incorrect as the exclusivity was not checked, and the 'OKAY' response should have been generated.

The 'EXOKAY' response may be correct, as exclusivity may, in fact, have been maintained, but this cannot be guaranteed.

Implications

This defect could cause software to behave incorrectly if its behaviour depends on using the response values for exclusive accesses to memory areas located on AHB slaves.

Workaround

Avoid the use of exclusive accesses to AHB slaves. LOCKed accesses should be used where exclusivity is required.

456568: Transaction counter underflow when B handshake precedes AW handshake

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

The AXI specification requires that, within a given transaction, all W channel transfers be completed before the B channel transfer occurs. It does not require, however, that the AW channel transfer has occurred before the B channel transfer. If the B channel handshake occurs before the AW channel handshake, a transaction counter underflow can occur and incorrect behaviour will result. PL301 prevents any W channel transfers, and hence the B channel handshake before the AW channel is VALID, but the B channel handshake can still occur before the AW channel handshake.

Implications

If the AW channel handshake for a transaction does not occur before the B channel handshake, transaction counters in the master interface can underflow causing incorrect operation that would require a reset to correct.

Workaround

Ensure that an AW channel handshake occurs before a B channel handshake for each transaction. This can be achieved by specifying a register slice on the AW channel of master interfaces that could be affected. The register slice must ensure that the handshake occurs on the PL301 side before a VALID can occur on the slave side to enforce this, so a full register slice or a forward register slice (if available in the version of PL301 being used).If a register slice is not acceptable then slaves must be designed to ensure they do not do exhibit this behaviour.

460061: Slave interfaces being starved when master interface write FIFO fills up

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

When the write issuing capability of a master interface is reached, no further transactions are issued, but the arbitration state update mechanism does not account for this and continues to update.

Implications

If a master interface reaches its write issuing capability limit, the arbitration state may continue updating so it will not be possible to predict the arbitration decision for the next transaction that is allowed to proceed. Under certain circumstances, if the arbitration state updates a number of times and returns to the state that granted the last time a transaction was allowed to proceed it could result in starvation of access for one or more masters.

Workaround

Increasing the write issuing capability of the master interface will require more outstanding transactions before the tracking structure fills, which increases the number of outstanding transactions required before this issue can occur. If the write issuing capability is set to one greater than the write acceptance capability of the slave interface that is connected to it then it can never occur. This will incur a small additional area and possibly a small timing penalty.

460064: **Unsynthesizable Verilog**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

When a master interface with the fixed round-robin arbiter is sparsely connected to only a single slave interface in a system that has multiple slave interfaces, incorrect Verilog is generated.

Implications

Configurations with the specified property may either fail to simulate, simulate incorrectly, or fail to synthesize.

Workaround

Use of a programmable least-recently-granted arbiter mechanism on the affected interface will prevent this problem. It may be replaced by a simulator warning regarding use of a zero length replication multiplier (warning of a Verilog construct like: `{0{1'b0}}`), depending on the version of simulator being used.

466785: Undriven inputs in configurations with a single slave interface and no ID bits

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

When an interconnect is specified with a single slave interface which has zero ID bits some signals are undriven.

Implications

The RTL will not behave correctly in simulation and should not be synthesised.

Workaround

Specify that the slave interface has a single ID bit and tie off input pins that are created as a result. If the pins are tied off, the synthesis process should optimise them away and no additional logic should result.

510518: **RegdSyncUpAxi bridge deadlocks if first transaction arrives before the first CLKEN**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

The SyncUpRegd module, which is instantiated in the RegdSyncUpAxi bridge can deadlock if its ACLKEN input is not being generated when a transaction arrives at the slow side of the module (specifically on the slave interface of the AW, W and AR channels).

This could occur for instance if an automatic ACLKEN generator is being used that stabilises a number of slow clock cycles after exiting the reset state and only generates an ACLKEN signal after stabilisation.

The RegdSyncDnAxi bridge also contains this module, but the affected channels are in the reverse direction (B and R) and in order for these channels to be making transfers, there must previously have been transfers on the AW or AR channels, which which would themselves have required ACLKEN to have been active. Therefore this defect will not affect the RegdSyncDnAxi bridge despite it using the affected sub-component.

Implications

If the ACLKEN is not being generated before the first transfer is requested on the AW, W or AR channels, then that channel will deadlock. A reset would be required to restore functionality.

Workaround

Ensure that either ACLKEN is generated before leaving the reset state or that transactions are not presented until the ACLKEN is being generated.

The latter requirement may be enforced by implementing a gating signal which does not allow transactions to pass until a negative edge of the ACLKEN signal has occurred. This gating signal is logically ANDed with the VALID and READY signal of the three affected AXI channels (AW, W and AR) and the output of that function used instead of the bare VALID or READY signal.

The gating signal is derived from the behaviour of the ACLKEN signal, which is generated in the fast clock domain, and is used in the slow clock domain. In order to satisfy the timing requirements of both fast and clock domains, it must change when they have a coincident clock edge. This will happen at the end of the cycle in which ACLKEN is high. Thus a register that resets to 0, has a 1 input and is clocked by ACLKM (the fast clock) but only enabled by ACLKEN will behave correctly. As this register need make only one transition between resets, the enable may be combined with the register's state (D) as a power saving measure - an enable input driven by (ACLKEN & ~D) is enabled by the presence of ACLKEN, but disabled once the register has made the transition.

577318: Single slave per ID + single active write settings on a slave interface cause the read channel to lock up

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p2-00rel0, Open.

Description

Selecting slave-per-ID CDAS for both read and write and also selecting the single-active-write option results in a read deadlock.

Implications

A slave interface cannot have both the slave-per-ID CDAS for reads and the slave-per-ID CDAS with the single-active-write option for writes.

Workaround

The slave-per-ID CDAS with the single-active-write option is in most practical cases more restrictive than the single-slave CDAS, so if the slave-per-ID CDAS is required for reads and that scheme cannot be used without the single-active-write option for writes, it is recommended that the single-slave scheme be used for writes instead. If the slave-per-ID scheme with single-active-write is required for writes then the single-slave, unique-ID or hybrid scheme should be used for reads.

In all cases, if the slave-per-ID scheme is not being used for writes, the single-active-write option should not be set.

690568: **QoS becomes active later than expected**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

When the QoS mechanism becomes active due to the tidemark being exceeded, the masters that won the arbitration decision in the previous cycle will, due to AXI's sticky VALID requirement, be permitted to make a single additional transfer even if they would not be expected to due to not being flagged in the QoS mask value.

Implications

As the cycle in which the QoS tidemark is exceeded could permit two transfers to occur, and the following cycle could also permit two transfers to occur, the QoS tidemark may be exceeded by three non-QoS-privileged transactions.

Workaround

The tidemark may be set lower to ensure the number of transactions that can be issued by QoS-privileged masters is maintained.

722106: Slave interface transaction tracking logic can malfunction when attempting to exceed write acceptance capability

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p2-00rel0, Open.

Description

This defect can affect a slave interface that has the slave-per-id CDAS configured for writes and the single-active-write option selected under the following circumstances:

- the number of outstanding write transactions configured for the slave interface is already reached

- the previous write transaction has not had a W transfer with WLAST asserted, so the single-active-write control would prevent a further AW transfer

- the master asserts AWVALID with transaction properties (AWADDR, etc.) that mean that the CDAS would allow the transaction to proceed if the capacity were greater

- a B transfer for an earlier write transaction is returned before the W transfer with WLAST asserted occurs

In these circumstances the write data ordering transaction tracker can have an erroneous entry added which will result in deadlock when a transaction that is routed to a different slave is received.

Implications

Affected slave interfaces can deadlock.

Workaround

If the master interface driving the affected slave interface has an enforced outstanding write transaction limit (either by design, or by an additional block), then making the write acceptance capability of the slave interface at least as large as that value will prevent the attempted overfilling of the transaction tracker and hence prevent the occurrence of this problem.

It is important to note that the term 'outstanding' means having an AW transfer but not a B transfer, rather than having an AW transfer but not a W transfer with WLAST asserted.

723115: WLAST before AW handshake on a single_active_slave interface deadlocks

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 2, Present in: r1p2-00rel0, Open.

Description

If a slave interface configured to use the slave_per_id CDAS mechansism for write transactions and with the single active slave option also selected is driven such that the AW channel handshake occurs only after the last W handshake associated with it, then that slave interface can deadlock.

Implications

The single active slave mechanism cannot be used if the problematic behaviour cannot be avoided. This in turn may mean that the slave_per_id cyclic scheme cannot be used for write transactions.

Workaround

Please contact Support for assistance with a workaround for this issue.

Errata - Category 3

404615: Formality may report spurious warnings when optimised AHB to AXI bridge is used

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

When a memory optimised AHB to AXI bridge is used (`interface_protocol=ahb_lite_mem` is specified in the Master Params component in AMBA Designer), in some cases a register slice is automatically inserted in the generated RTL to avoid a possible deadlock situation. This register slice is configured to register only the forward path of the AXI AW channel. The design of the register slice is such that static optimisation by the synthesis tool optimises away the pass-through paths on the other channels. However, Formality has an incompatibility with this code and reports some warnings. These warnings are detected by the PL301 log file checking process which causes the PL301 script to report a failure when both synthesis and LEC have in fact completed successfully.

Implications

The synthesis and LEC process appears to have been unsuccessful but has in fact succeeded. The following warnings may be reported:

```
Warning: The port range and the net range of the net 'AxIDS' differ.  (FMR_VLOG-179)
Warning: The port range and the net range of the net 'AxUSERS' differ.  (FMR_VLOG-179)
Warning: The port range and the net range of the net 'AxIDM' differ.  (FMR_VLOG-179)
Warning: The port range and the net range of the net 'AxUSERM' differ.  (FMR_VLOG-179)
```

Workaround

If failure is indicated, check the Formality log file and if the warnings are as shown in the "Implications" section, they may be ignored. The LEC process can be disabled in the AMBA Designer RTL flow manager "Preferences" dialog once it is confirmed that these are the only warnings present.

421416: Master interfaces with AHB protocol and 0 USER bits may give synthesis warnings

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

When a master interface is specified as using the AHB protocol and the configuration also uses 0 user signal bits then some synthesis or LEC warnings can occur.

In these circumstances, on master interfaces the **HRUSER** AHB signal is not provided externally and is unused internally, but still exists as a module input port which is unconnected. Some synthesis or LEC tools may issue warnings about this undriven input port.

In these circumstances, on slave interfaces the **HAUSER** and **HWUSER** AHB signals are not provided externally and are unused internally, but still exist as module input ports and are internally tied to Verilog value `{0(1'b0)}`. Some synthesis or LEC tools may issue warnings about this.

Implications

The signals are unused, so when 0 USER bits are specified, these warnings may be ignored.

Workaround

None

422422: **RTL uses undefined macros**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

The files `DownsizerAxi_128to32Wrapper.v` and

`DownsizerAxiWrapper.v` use Verilog `` `define ``

macros that are defined in the file `Axi.v`, however they are missing a

`` `include statement to include these definitions when reading the `` files.

If compiling all the PL301 Verilog files, the Axi.v file is included by another module before the downsizers are compiled. With some tools/versions, the definitions are persistent across multiple files within the same compilation run and therefore this does not cause a problem. However where these files are compiled separately or with some tool versions this is not the case and undefined macros are therefore found.

Implications

When the PL301 Verilog files are compiled separately, or with some tool versions, undefined macros may be reported.

Workaround

Include the following line immediately before the module declaration in both the affected Verilog files:

`` `include "Axi.v" ``

422820: AXI-AHB bridge IDLE address unaligned

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

In some circumstances during AHB IDLE cycles, the **HADDR** value is not aligned with the **HSIZE** value. This behavior is prohibited in the AHB-Lite specification.

Implications

The defect is not expected to cause a problem in synthesizable code as AHB slave interfaces do not generally sample **HADDR** during IDLE cycles. A protocol checker that is strictly implementing the AHB-Lite specification may report errors.

Workaround

Disable AHB protocol checks for **HADDR** alignment during IDLE cycles.

423021: **RTL generation issue when a Slave I/F sees the full 32-bit address range**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

A code generation error occurs for a configuration which has any slave interface whose entire addressable space is occupied by master interfaces which are configured to use the AHB protocol.

This error does not generate any incorrect code, but causes an infinite loop in the software that generates test vectors for the configuration. As a result the generation stalls.

Implications

Affected configurations cannot be generated.

Workaround

As the defect only manifests itself when AHB interfaces occupy all of the addressable space of a slave interface, this problem can be worked around in most cases by reducing the space the connected slaves occupy in the address map.

424365: Combinatorial path from RID/BID to RREADY/BREADY

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

The core AXI interconnect within PL301 implements combinatorial paths from **BID** to **BREADY** and from **RID** to **RREADY** on master interfaces ("output ports").

When PL301 is configured with no registered component (e.g. an AXI register slice) between the master interfaces of the core interconnect and the master interfaces of the complete PL301 sub-system, then these combinatorial paths are exposed on the external AXI interface.

This contravenes the AXI specification (ARM IHI 0022) which bans combinatorial paths from inputs to outputs on an AXI interface because they can cause problems with timing closure when integrating an AXI-based system.

Note that there are no functional issues due to this erratum.

Implications

The presence of unexpected combinatorial paths on the AXI master interfaces might cause problems when trying to achieve timing closure of the AXI system into which PL301 is integrated.

If user-generated synthesis scripts have assumed that no such paths will exist then it is possible that the user has included `set_false_path` or `set_multicycle_path` commands to hide such paths. These would prevent the paths from being optimised during synthesis which could lead to failures in-silicon. Note that the synthesis scripts provided by ARM with PL301 do not include any such commands.

Workaround

For all AXI master interfaces on PL301, ensure that no false or multicycle paths are declared which would hide paths from **RID** to **RREADY** or from **BID** to **BREADY**. This will ensure that any timing violations are found.

If the user-generated PL301 configuration implements these combinatorial paths, there are two options:

1. If there are no timing violations when PL301 is integrated into the larger system, the paths can be allowed to remain: there are no functional errors associated with these paths.

2. If the affected paths must be registered in order to integrate PL301 into the larger system, re-configure PL301 so that the relevant master interfaces are registered by setting the `registered_io` parameter to 1 or 2.

430627: QoS permanently active in some master interfaces

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0, Fixed in r1p1-00rel0.

Description

If the sum of all read_acceptance_capbilility and write_acceptance_capability values on all slave interfaces can be represented in fewer bits than the value of combined_issuing_capability on a master interface then the Quality-of-Service mechanism for that master interface will not have the expected behaviour. In particular if that condition is true and the combined_acceptance_capability is also a power of two then the QoS scheme will prevent any transactions being transferred by that master interface.

Implications

In some circumstances the values of read_acceptance_capbility and write_acceptance_capability for all slave interfaces and combined_issuing_capability for a master interface can result in no transactions being passed by that master interface unless that interface has been programmed to give QoS privileges to at least one slave interface.

Workaround

During configuration, ensure that the combined_issuing_capability of each master interface is no larger than the sum of all slave interfaces' read_acceptance_capability and write_acceptance_capability values. This will not affect performance as such a restriction will not prevent the maximum possible number of transactions from existing in the system.

In an already configured system, if no transactions are being passed and the Quality-of-Service mechanism is always on, transactions can be enabled by granting QoS privileges to all slave interfaces.

436785: **IP-XACT description issues with signal directions and naming**

Status

Affects:　　　　　Product PL301 AMBA 3 HP Matrix .

Fault status:　　　Cat 3, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

The IP-XACT component description generated when the PL301 RTL is rendered contains some incorrect definitions of signal directions for master or slave interfaces that are configured for AHB protocol and some signal naming mismatches compared to the Verilog.

Implications

When the IP-XACT description is used by AMBA Designer for RTL stitching the generated PL301 with other components, there are errors in the resulting stitched RTL due to signal direction and signal naming mismatches.

Workaround

None.

446839: AHB-Lite-Slave master interfaces cannot meet out-of-box timing

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

A PL301 instance with a master interface using the AHB-Lite-slave protocol cannot be synthesised to meet timing constraints out of the box. The **HREADY** output on such an interface is directly connected to the **HREADYOUT** input. The default constraints for such an interface are such that the input delay of the input combined with the output delay of the output are greater than a clock cycle and thus cannot be met.

Implications

Synthesis cannot meet timing constraints.

Workaround

Adjust the timing constraints in the rendered scripts to values that are achievable.

446841: Configurations with 32 slave interfaces give Verilog compile warnings

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

If a configuration has 32 slave interfaces, a value that is used to pad a one-bit-per-slave-interface value up to 32 bits is 0 bits in width. This padding value is created using the Verilog repeat operator and if the number of repeats is 0 some versions of some simulators issue a warning message.

Implications

Verilog compile warnings may be issued.

Workaround

No functionality is affected, so no workaround is required. Ignore this particular warning.

447585: Incorrect OVL assertions in axibm_decode_scheme_<design>.v for certain configurations

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

For configurations where there are multiple remap ranges on a master interface using the same remap bit, the OVL assertions that are rendered in the Verilog file `axibm_decode_scheme_<design>.v` (where `<design>` is the configuration name) are generated incorrectly and cause simulation errors of the form:

```
identifier 'm0_remap_range_0' previously declared
```

Implications

Simulations fail due to syntax errors with incorrectly formed OVL assertions.

Workaround

As only OVLs are involved, disabling OVLs for this file will avoid the problem.

449412: Incorrect timing constraints on interfaces with unregistered Expander or Downsizer

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

The synthesis timing constraints are incorrectly generated for master or slave interfaces that have an Expander or Downsizer instantiated without being registered. The timing constraints do not account for the combinatorial paths that exist through the Expander and Downsizer, and so this can lead to over-constrained paths.

Implications

Timing on over-constrained paths cannot be met.

Workaround

Adjust the timing constraints in the rendered scripts to values that are achievable.

450012: Missing -library option for set_driving_cell statement

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

The set_driving_cell statement in the synthesis scripts does not have a -library option with it to specify which technology library to draw the driving cell from. Some versions of Design Compiler issue a warning when this is the case. The warning is of the form:

```
Warning: Driving cell was specified without the -library option. Using
library_cell BUFX2HS from library ss_1v08_125c.db:ss_1v08_125c. (UID-1003)
```

Implications

The tool infers which library to draw the cell from and the warning indicates the identity of that library. If multiple libraries are configured, it is possible the inferred library may be incorrect.

Even though the warning does not cause a problem with the end synthesis result, the IP generation scripts will report the synthesis run as FAILED.

Workaround

If the inferred cell library is correct, no action is required and the warning may be ignored. If the cell library is incorrect, a -library option should be added to the control script line that executes the command set_driving_cell.

471415: Inconsistency between documentation and RTL for arbitration programming through APB configuration port

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p1-00rel0,r1p1-00rel1, Fixed in r1p2-00rel0.

Description

The description of access to arbitration registers via the APB programming interface is not consistent with the RTL.

Implications

If the documentation is followed, unexpected programming of, or interrogation of, the arbitration mechanisms may result which could result in unexpected behaviour.

Workaround

The documentation indicates the following:

```
==============================================
Write = 0 x XX 00 XX 00
             |       |- New priority level
             |
             |- Slave interface number
==============================================
Read = A special write, followed by read
Write = 0 x FF 00 00 XX
                      |- Slave interface number
      ----------------------------------------
Read  = 0 x 00 00 XX XX
                   | |- Slave interface number
                   |
                   |- Priority
==============================================
```

but this is inconsistent with the RTL. The RTL requires the following use mechanism:

```
==============================================
Write = 0 x XX 00 XX 00
             |       |- New priority level
             |
             |- Slot number
==============================================
Read = A special write, followed by read
Write = 0 x FF 00 00 XX
                      |- Slot number
```

```
         ---------------------------------------
Read  = 0 x 00 00 XX XX
                  |  |- Slave interface number
                  |
                  |- Priority
==============================================
```

The "slot number" is the index of the slave interface in the list of slave interfaces in the arbitration specification in the XML configuration file regardless of the slave interface number they describe, so slot 0 relates to the first arbitration specification line, slot 1 to the second, etc.

481763: IP-XACT description does not match v1.2 bus definitions

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p1-00rel0, Fixed in r1p1-00rel1.

Description

The APB IP-XACT bus definition has been corrected and means that the PL301 APB description is not compatible with IP-XACT v1.2.

Implications

PL301 instances cannot be stitched by AMBA Designer

Workaround

Update to PL301 version r1p1-00rel1; the APB description is the only change from r1p1-00rel0.

493515: **Multiple instances connected in some mesh arrangements can deadlock**

Status

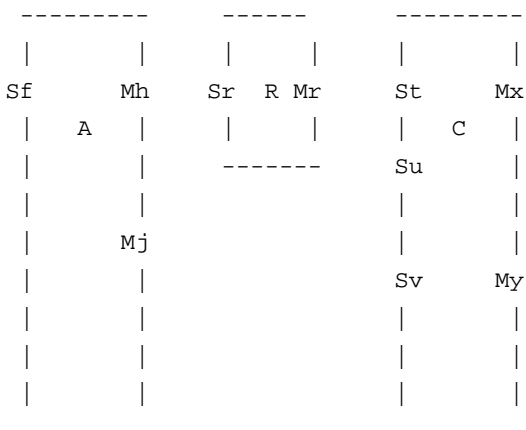Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p2-00rel0, Open.

Description

When connecting multiple instances of PL301 in non-trivial ways, it is possible to create a system that can deadlock. This issue is not due to a defect in the PL301 product, but inherent in the flexibility allowed by the AXI protocol.

If there are multiple AXI connections between instances of PL301 and the upstream instance has slave interfaces which allow transactions to more than one master interface at a time then that system could be liable to deadlock due to the relative ordering of AW or AR transfers at their origin and destination.

The following system can exhibit this issue. All slave interfaces use the slave-per-id cyclic scheme:

```
 ---------     ------     ---------
 |       |     |    |     |       |
Sf      Mh    Sr  R Mr    St      Mx
 |   A   |     |    |     |   C   |
 |       |      -------   Su      |
 |       |               |       |
 |      Mj               |       |
 |       |               Sv      My
 |       |               |       |
 |       |               |       |
 |       |               |       |
 ---------               ---------
```

The following routes for transactions are possible:

(1) Sf->Mh->Sr->Mr->St->Mx

(2) Sf->Mj->Su->My

(3) Sv->My

(4) Sv->Mx

If the system is quiescent and then these transactions handshake in the following places in the following order:

(1) AW handshakes in Mr

(2) AW handshakes in My

(3) AW handshakes in My

(4) AW handshakes in Mx

(1) AW handshakes in Mx

Because of the AXI requirement that the first beat of W must be transferred in the same order as the AW transfers, each of the master and slave interfaces involved in those four transactions may only perform a W transfer with one specific party:

Sf will only handshake with Mx, which will only handshake with Sv, which will only handshake with My, which will only handshake with Sf.

Thus the system deadlocks for writes.

Implications

If a system is configured that is subject to this problem then under some sequences of transactions, the system can become deadlocked. A reset would be required to recover.

Workaround

Affected instances of PL301 are those that have more then one route along which **some** transaction can pass (via any number of register slices, other PL301 instances, or any other component) to another PL301 instance and also have one or more slave interfaces that have both a cyclic scheme other than single-slave and write acceptance capability greater than 1 (for writes) or the higher rank cyclic scheme (for reads). So if instance A has a route to instance C via instance B and another route to instance C via a register slice, then it is affected.

If a PL301 instance is affected, the deadlock issue can be avoided by setting appropriate slave interface parameters. For reads, the selected cyclic dependency avoidance scheme must be anything except higher-rank. The choice of cyclic dependency avoidance scheme can be made independently for each slave interface. For writes, the selected cyclic dependency avoidance scheme must be either single-slave or slave-per-id and if the slave-per-id scheme is selected then the write acceptance capability of the slave interface must be set to 1, or an external mechanism must be used to prevent more than 1 data-active write transaction from being in progress. An data-active write transaction is different from an active write transaction - the latter is one which has had an AW or W channel handshake but not a B channel handshake whereas the former is one that has had an AW channel handshake but not a W handshake with WLAST asserted.

Prior to version r1p2, there is only a single parameter to select cyclic scheme, and the selected scheme applies to both reads and writes. From version r1p2 onwards, the cyclic schemes for reads and write can be selected separately.

561818: Incorrect stimulus addresses generated for APB configuration port

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p2-00rel0, Open.

Description

The out-of-box test vectors use incorrect offsets for querying the arbitration registers of master interfaces when one or more master interfaces lack the arbitration registers. The vectors correctly do not attempt to access the registers of master interfaces that lack them, but use incorrect addresses for subsequent master interfaces.

Implications

One phase of the out-of-box test mechanism will not pass if master interfaces are configured that lack the arbitration registers.

Workaround

Contact Support for assistance resolving this defect if required.

570866: **Slave interface arbiter priorities changed between releases, resulting in extra latency**

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p2-00rel0, Open.

Description

The priorities of master interfaces at the arbitration of the R and B channels in slave interfaces changed between versions of the product. In earlier versions, the priority was determined by the order of the master interfaces in the configuration file. In version r1p2 the order is determined by the cyclic_rank attribute of the master interfaces.

The master interface that the default slave is connected to does not have a cyclic_rank attribute, so a value of 0 is inferred for it, and this results in the default slave being the highest priority. The highest priority master interface is used as a default arbitration choice when no VALID signals are asserted by master interfaces so that one master interface will have a fast path as soon as activity resumes, as it will not need to win the arbitration. With the changed priorities, the master interface with the fast path becomes the default slave rather than the first master interface declared in the configuration file.

Implications

The fast path from one master interface will not exist after a default arbitration.

Workaround

The default slave's master interface can be given a cyclic_rank attribute which will cause its priority to be the lowest, which will result in another master interface having the highest priority and thus being the default arbitration decision.

The default slave's master interface parameters are created by the amba_build.tcl script. Support can provide guidance on changes needed to this script to achieve this result.

587269: IP-XACT XSL errors cause AMBA Designer stitch failures

Status

Affects:　　　　　　Product PL301 AMBA 3 HP Matrix .

Fault status:　　　　Cat 3, Present in: r1p2-00rel0, Open.

Description

The IP-XACT description of the generated PL301 design omits clock domain specific reset signals for AXI interfaces that do not specify an outer register slice and have an external interface faster than the PL301 core.

Implications

The IP-XACT file cannot be used for any purpose which requires correct declaration of RESET signals when affected interfaces are present.

Workaround

A modified stylesheet for the IP-XACT description is required. Support can provide this on request.

671217: Pin specification in timing constraint exceptions does not capture all pins

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p2-00rel0, Open.

Description

The file pl301_a3bm_exceptions.tcl, generated in the rendering process, that documents timing exceptions for the pl301 instance does not correctly capture all required pins in the slow clock domain of a clock crossing bridge.

Implications

Multi-cycle paths across the clock domain crossing bridge are defined as single cycle paths, and hence the design is over constrained.

Workaround

The file is generated by the rendering process and is specific to each pl301 configuration. Contact support for a corrected template from which to generate this file.

701718: Automatic exceptions not rendered correctly when a sync down bridge is found between the core interconnect and a slave

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Cat 3, Present in: r1p2-00rel0, Open.

Description

Multi-cycle paths through a RegdSyncDn clock bridge on a master interface (between the PL301 core and a slave) are specified in the wrong sense.

Implications

Some of the specified multicycle paths do not exist and so will have no effect. Other paths do exist and as a result, some single cycle paths are defined as multicycle which could lead to incorrect timing paths in the final synthesised design.

Workaround

The affected file is generated and is unique to a configuration. Contact support for a corrected template that the file is generated from.

Errata - Documentation

720607: DDI0397E HPM (PL301) r1p2 TRM - TRM description of write issuing capability does not match RTL behaviour in all cases

Status

Affects: Product PL301 AMBA 3 HP Matrix .

Fault status: Doc, Present in: r1p2-00rel0, Open.

Description

In a configuration with a single slave interface, a master interface's write issuing capability parameter will not be enforced.

The write issuing capability's presence was to allow a transaction tracking structure to be correctly sized. When there is only a single slave interface, this tracking structure is not required and thus removed. The size of the tracking structure imposed a limit on the number of outstanding write transactions that could exist through that master interface, so its removal removes the restriction on the number of outstanding transactions.

Implications

The write issuing capability of a master interface cannot be used to restrict the number of outstanding write transactions through a master interface.

Workaround

If the ability to restrict write issuing capability on a master interface is required, a second slave interface can be added with all inputs tied low and outputs ignored. This will cause the transaction tracking structure (and hence the outstanding transaction limit) to be present.

Errata – Driver Software

There are no Errata in this Category