ARM PrimeCell®
SRAM NOR + NAND Flash Memory Controller (PL353)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r2p1 of SRAM NOR + NAND Flash Memory Ctlr -3YT

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- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Related Products

This document only captures defects specific to the ZA815 product. The current release is r0p0-00dev0 and has been based on PL301-r1p1-00bet2. All defects on that apply to this PL301 revision will apply to ZA815 too and details can be found in the latest PL301-DC-11001 Errata document. If instantiating the DMP then all declared erratum relating to PL368 will also apply and document PL368-DC-11001 should be consulted.

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

12 Aug 2009: Changes in Document v12

Page	Status	ID	Cat	Summary
31	New	721059	Cat 2	SLC ECC misses single error to bit0 byte0 and fails to detect some double error cases

04 Nov 2008: Changes in Document v11

Page	Status	ID	Cat	Summary
30	New	534963	Cat 2	Potential data error when writing to SRAM with ACLK async to MCLK
27	Updated	456826	Cat 2	PREADY not returned early for APB writes to direct_cmd register when PCLKEN is not tied high
44	Updated	583618	Cat 3	Explicit Perl paths causing RTL rendering issues on certain machines
43	New	533517	Cat 3	FIFO depths chosen in AMBA Designer may be inconsistent

29 Feb 2008: Changes in Document v10

Page	Status	ID	Cat	Summary
28	New	501623	Cat 2	CS not deasserted in accesses to NAND in certain modes of operation
41	Updated	447567	Cat 3	READY not returned when zero's written to memc_cfg_set & memc_cfg_clr
55	Updated	445215	Doc	Use of ClearCS or nand_csl with the EBI can result in deadlock

23 Oct 2007: Changes in Document v8

Page	Status	ID	Cat	Summary
24	New	445912	Cat 2	PL35x uses invalid signals in the NAND fsm
17	Updated	372884	Cat 2	Mode updates not holding off subsequent transactions
18	Updated	393151	Cat 2	Following a period with nand_booten asserted, interrupt not always cleared
25	Updated	455815	Cat 2	tRHW is not programmable and can be violated (by software or the ECC block)
26	Updated	456580	Cat 2	Async mux_mode behaviour is not supported by some flash devices.
27	Updated	456826	Cat 2	PREADY not returned early for APB writes to direct_cmd register when PCLKEN is not tied high
41	New	447567	Cat 3	PREADY not returned when zero's written to memc_cfg_set & memc_cfg_clr
34	Updated	381382	Cat 3	Memory FSM incorrectly coded for use with NAND boot enable
35	Updated	404770	Cat 3	NAND boot mode problem for some NAND memory device protocols
36	Updated	408515	Cat 3	Memory Configuration Register does not indicate mux_mode correctly
39	Updated	418214	Cat 3	Register update mechanism mismatching manager commands
42	Updated	456825	Cat 3	Command phase time may be one cycle short during ECC if aclk synchronously greater than mclk
46	Updated	381891	Doc	Row boundary behaviour not documented
47	Updated	404182	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, incorrect reset value for sram_cycles register

48	Updated	404184	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, incorrect waveform in Fig 2-16
49	Updated	404865	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, Figure 3-5 has incorrect address mapping
54	Updated	442865	Doc	DDI0380E SMC (PL350) TRM, incorrect ecc_value field width in ecc_value register
55	Updated	445215	Doc	Use of ClearCS or nand_csl with the EBI can result in deadlock

20 Sep 2007: Changes in Document v7

Page	Status	ID	Cat	Summary
27	New	456826	Cat 2	PREADY not returned early for APB writes to direct_cmd register when PCLKEN is not tied high
26	New	456580	Cat 2	Async mux_mode behaviour is not supported by some flash devices.
25	New	455815	Cat 2	tRHW is not programmable and can be violated (by software or the ECC block)
23	New	443976	Cat 2	ECC does not detect 2-bit errors
22	New	415513	Cat 2	CS remaining asserted between transactions is not supported by CRAM 1.0
21	New	415054	Cat 2	Error when asynchronous write follows a synchronous write and is to a different chip-select
42	New	456825	Cat 3	Command phase time may be one cycle short during ECC if aclk synchronously greater than mclk
40	New	445213	Cat 3	Remap functionality can be wrong
37	Updated	409123	Cat 3	Setting tWP to 1 in async mux_mode gives a tWP value of 0.
35	Updated	404770	Cat 3	NAND boot mode problem for some NAND memory device protocols
55	New	445215	Doc	Use of ClearCS or nand_csl with the ebi can result in deadlock
54	New	442865	Doc	DDI0380E SMC (PL350) TRM, incorrect ecc_value field width in ecc_value register

22 Dec 2006: Changes in Document v6

Page	Status	ID	Cat	Summary
39	New	418214	Cat 3	Register update mechanism mismatching manager commands

21 Nov 2006: Changes in Document v5

Page	Status	ID	Cat	Summary
38	New	412923	Cat 3	Can enter low_power mode while transactions are still outstanding
53	New	411811	Doc	TRM error on set_cycles_val
20	New	410564	Cat 2	Updating BCR while command fifo is full and during an AXI write with ID 0x00 results in deadlock
15	New	410562	Cat 1	Memory interface locks up when EBIBACKOFF asserted during turnaround time of burst finishing at boundary
19	New	410561	Cat 2	tAVH violation on reads in mux-mode operation
37	New	409123	Cat 3	Setting tWP to 1 in async mux_mode gives a tWP value of 0.

52	New	408962	Doc	Lack of documentation on connecting EBI to memory controllers that run at different frequencies
36	New	408515	Cat 3	Memory Configuration Register does not indicate mux_mode correctly
51	New	408513	Doc	Memory configuration register description incorrect in TRM
49	New	404865	Doc	TRM Figure 3-5 has incorrect address mapping
48	New	404184	Doc	Incorrect waveform in Fig 2-16 of TRM
17	New	372884	Cat 2	Mode updates not holding off subsequent transactions
50	Updated	405861	Doc	Incorrect version of documentation in release
35	Updated	404770	Cat 3	NAND boot mode problem for some NAND memory device protocols
47	Updated	404182	Doc	Incorrect reset value for sram_cycles register
18	Updated	393151	Cat 2	Following a period with nand_booten asserted, interrupt not always cleared
34	Updated	381382	Cat 3	Memory FSM incorrectly coded for use with NAND boot enable

27 Sep 2006: Changes in Document v4

Page	Status	ID	Cat	Summary
35	New	404770	Cat 3	NAND boot mode problem for some NAND memory device protocols
50	New	405861	Doc	Incorrect version of documentation in release
47	New	404182	Doc	Incorrect reset value for sram_cycles register in TRM

14 Aug 2006: Changes in Document v3

Page	Status	ID	Cat	Summary
46	New	381891	Doc	Row boundary behaviour not documented

10 Jul 2006: Changes in Document v2

Page	Status	ID	Cat	Summary
18	New	393151	Cat 2	Following a period with nand_booten asserted, interrupt not always cleared
34	New	381382	Cat 3	Memory FSM incorrectly coded for use with NAND boot enable

18 Apr 2006: Changes in Document v1

No Errata in this document revision

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

NOTE: Some documentation errata are not directly applicable to the PL353 but are included in this table as the documentation is common across the PL351, PL352, PL353, PL354 products. This may result in certain product revisions appearing in the table for which no corresponding PL353 release actually exists.

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p1-01rel0	r1p1-01rel1	r1p2-00rel0	r2p0-00rel0	r2p0-02rel0	r2p1-00rel0
381891	Doc	Row boundary behaviour not documented		X								
404182	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, incorrect reset value for sram_cycles register	X	X	X	X	X	X				
404184	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, incorrect waveform in Fig 2-16			X	X	X	X	X			
404865	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, Figure 3-5 has incorrect address mapping			X	X	X	X	X			
405861	Doc	Incorrect version of documentation in release				X						
408513	Doc	DDI0380D SMC (PL350 series) r1p2 TRM, memory configuration register description is incorrect			X	X	X	X	X			

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p1-01rel0	r1p1-01rel1	r1p2-00rel0	r2p0-00rel0	r2p0-02rel0	r2p1-00rel0
408962	Doc	DII0137C SMC (PL350 series) r1p1 IM, how to connect EBI to SMC when the interfaces run at different frequencies			X	X	X	X	X			
411811	Doc	DDI0380C SMC (PL350 series) r1p1 TRM, Fig 5-1 shows incorrect values for set_cycles_val			X	X	X	X	X			
442865	Doc	DDI0380E SMC (PL350) TRM, incorrect ecc_value field width in ecc_value register								X		
445215	Doc	Use of ClearCS or nand_csl with the EBI can result in deadlock	X	X	X	X	X	X	X	X	X	X
410562	Cat 1	Memory interface locks up when EBIBACKOFF asserted during turnaround time of burst finishing at boundary	X	X	X	X	X	X				
372884	Cat 2	Mode updates not holding off subsequent transactions	X	X	X	X	X	X				
393151	Cat 2	Following a period with nand_booten asserted, interrupt not always cleared		X	X							
410561	Cat 2	tAVH violation on reads in mux-mode operation	X	X	X	X	X	X				
410564	Cat 2	Updating BCR while command fifo is full and during an AXI write with ID 0x00 results in deadlock	X	X	X	X	X	X				

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p1-01rel0	r1p1-01rel1	r1p2-00rel0	r2p0-00rel0	r2p0-02rel0	r2p1-00rel0
415054	Cat 2	Error when asynchronous write follows a synchronous write and is to a different chip-select	X	X	X	X	X	X				
415513	Cat 2	CS remaining asserted between transactions is not supported by CRAM 1.0	X	X	X	X	X	X				
443976	Cat 2	ECC does not detect 2-bit errors								X		
445912	Cat 2	Invalid signals in the NAND fsm	X	X	X	X	X	X	X			
455815	Cat 2	tRHW is not programmable and can be violated (by software or the ECC block)								X	X	
456580	Cat 2	Async mux_mode behaviour is not supported by some flash devices.	X	X	X	X	X	X	X	X	X	
456826	Cat 2	PREADY not returned early for APB writes to direct_cmd register when PCLKEN is not tied high	X	X	X	X	X	X	X	X	X	
501623	Cat 2	CS not deasserted in accesses to NAND in certain modes of operation								X	X	X
534963	Cat 2	Potential data error when writing to SRAM with ACLK async to MCLK	X	X	X	X	X	X	X	X	X	X
721059	Cat 2	SLC ECC misses single error to bit0 byte0 and fails to detect some double error cases										X
381382	Cat 3	Memory FSM incorrectly coded for use with NAND boot enable		X	X							

ID	Cat	Summary of Erratum	r0p0-00rel0	r1p0-00rel0	r1p1-00rel0	r1p1-00rel1	r1p1-01rel0	r1p1-01rel1	r1p2-00rel0	r2p0-00rel0	r2p0-02rel0	r2p1-00rel0
404770	Cat 3	NAND boot mode problem for some NAND memory device protocols	X	X	X	X						
408515	Cat 3	Memory Configuration Register does not indicate mux_mode correctly		X	X	X	X	X				
409123	Cat 3	Setting tWP to 1 in async mux_mode gives a tWP value of 0.		X	X	X	X	X				
412923	Cat 3	Can enter low_power mode while transactions are still outstanding	X	X	X	X	X	X				
418214	Cat 3	Register update mechanism mismatching manager commands		X	X	X	X	X				
445213	Cat 3	Remap functionality can be wrong	X	X	X	X	X	X	X	X	X	X
447567	Cat 3	READY not returned when zero's written to memc_cfg_set & memc_cfg_clr	X	X	X	X	X	X	X			
456825	Cat 3	Command phase time may be one cycle short during ECC if aclk synchronously greater than mclk								X	X	
533517	Cat 3	FIFO depths chosen in AMBA Designer may be inconsistent						X	X	X	X	X
583618	Cat 3	Explicit Perl paths causing RTL rendering issues on certain machines	X	X	X	X	X	X	X	X	X	X

Errata - Category 1

410562: Memory interface locks up when EBIBACKOFF asserted during turnaround time of burst finishing at boundary

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 1, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

PSRAM devices deassert the wait signal at the end of a burst that finishes at or about to cross a page boundary.

The wait signal is sampled on the fedback clock which is only driven during memory transactions. If the last rising edge of the fedback clock does not sample wait high after the transaction then the wait signal will remain low internally until the next memory access starts. The last value sampled on the wait signal depends on a combination of clock speed, fedback clock delay and the time between chip-select deassertion and the wait signal returning to its high impedence state.

If the sampled wait signal remains low and a turnaround time is required i.e. between a read and write then if EBIBACKOFF is asserted during that turnaround time the memory interface will lock-up.

This problem can occur with all PSRAM devices.

Implications

Under the above described conditions, the memory interface will lock up and will never release the EBI.

Workaround

none

Errata - Category 2

372884: Mode updates not holding off subsequent transactions

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

The PL350 provides a mechanism for synchronising the update of a memory configuration register with its own internal configuration registers.

Following an update, subsequent commands should be formatted using the new settings. However, because the command fifo in the memory interface can be populated immediately prior to the update occuring, the commands already in the fifo when the update occurs will be incorrectly formatted for the new settings.

Commands during an update should be throttled in the format block such that the final command that performs the update is the only command active in the memory interface at that time.

Implications

This defect will affect a system which is accessing a chip whilst performing an update which, for example, changes burst length to a smaller value.

Typically it is expected that the change would be from default (smaller) burst lengths to longer, in which case the resulting behaviour should not cause any issues.

Workaround

There is no workaround for this issue.

393151: Following a period with nand_booten asserted, interrupt not always cleared

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r1p0-00rel0,r1p1-00rel0, Fixed in r1p1-00rel1.

Description

The signal nand_booten is asserted when the controller is used to boot from NAND memory devices. The controller will suspend operation during busy periods by internally waiting for the interrupt before continuing.

When nand_booten is de-asserted, it is possible for an interrupt to be outstanding. If this interrupt is not cleared before the next read, software may try to access the nand chip whilst it is busy.

Implications

If the interrupt is not cleared when exiting boot mode, on the first read to NAND software may incorrectly assume the busy period has expired and access the memory whilst it is busy.

Workaround

The fix for this involves updating the fsm to clear the interrupt when entering the data state, and ensuring that the boot_busy flag is only set when moving out of command to idle state.

A software fix would be to always manually clear the interrupt upon exit of nand_booten mode.

410561: tAVH violation on reads in mux-mode operation

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

When reads are made to mux-mode memory devices, the timing between the deassertion of ADV and the address changing (tAVH) is violated.

This is because the address is changed on the same clock edge as ADV is deasserted.

tAVH is a mux-mode parameter and hence this violation does not occur with non-mux-mode memory devices.

Implications

This tAVH violation would cause protocol errors on the memory interface and could result in data corruption.

Workaround

This problem can be avoided by not performing async mux-mode reads. Synchronous mux-mode reads are not affected by this defect.

410564: Updating BCR while command fifo is full and during an AXI write with ID 0x00 results in deadlock

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

If the memory configuration registers are updated when the command fifo is full and then an AXI write with ID 0x00 is received to the other interface, a WAW hazard is incorrectly flagged. As there is no bresp to the manager operation, the hazard is never cleared and it will lock up both the AXI and memory interface.

The RTL change for this issue is in files pl35x_entry0_xxxx.v and pl35x_entry1_xxxx.v circa line 276:

FROM

assign hazard_valid_out = ~format_ready;

TO

assign hazard_valid_out = ~format_ready && ~mgr_cmd;

Implications

This results in a deadlock on the AXI and memory interface.

Workaround

To avoid this problem, either the memory configuration registers should be updated when the command fifo is not full or by preventing master 0 from issuing a write when the memory registers are being updated.

415054: Error when asynchronous write follows a synchronous write and is to a different chip-select

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

When an asynchronous write immediately follows a synchronous write and is therefore to a different chip-select, then the asynchronous write is treated as a synchronous read.

Implications

This erratum results in the asynchronous write being treated as a synchronous read by the memory device.

Workaround

Program all chip selects to run in the same mode of operation.

415513: CS remaining asserted between transactions is not supported by CRAM 1.0

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

The SMC does not deassert chip-select between immediately consecutive transfers to memory. This behaviour is not supported by CRAM 1.0

Implications

Not deasserting CS between transactions could cause undefined behaviour from the memory. One of the results could be the memory returning incorrect data for back to back read

transfers.

Workaround

None.

443976: ECC does not detect 2-bit errors

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r2p0-00rel0, Fixed in r2p0-02rel0.

Description

When the PL351 is configured with the ECC block enabled, the ECC is generated correctly but there is an issue in the detection algorithm resulting in 2-bit errors not being detected.

There are no issues with the PL351 with ECC disabled.

Implications

2-bit errors are not detected correctly.

Workaround

There is no workaround. If ECC is required please use a later release.

445912: Invalid signals in the NAND fsm

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

The NAND fsm has a term that references two signals (**rfifo_space_ok** and **next_read_n_write**) from the command FIFO. These signals are used without checking they are valid from the command fifo.

Using these signals when they are not valid can lead to a requested end command being omitted.

This can occur if one of the following rare sequences of events arises:

1) A read is followed by a program operation containing fewer AXI transactions than the cfifo depth and the read data has not been accepted by the master,

or,

2) A program operation (write data phase) is immediately followed by a read operation (without a command phase in between).

Implications

It is possible for a write sequence that is programmed to generate an end command to omit that end command.

Workaround

Case 1) can be avoided by ensuring that all reads have completed before starting a program operation or by ensuring that all program operations contain more AXI transactions than the command fifo depth.

Case 2) should never happen during NAND operation. If software is going to poll the NAND memory to detect the completion of a write, it should issue a status read command phase access before starting to poll.

455815: tRHW is not programmable and can be violated (by software or the ECC block)

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r2p0-00rel0,r2p0-02rel0, Fixed in r2p1-00rel0.

Description

No timing parameter is enforced between the read and write enable signals on the nand interface.

However, some memories do require this timing delay.

The controller only does this when using column change commands during ECC reads.

Implications

If tRHW gets violated it might result in data corruption in the memory

Workaround

1) If using ecc use the full jump mode

2) Running the controller in async mode will increase the delay by 2 mclk cycles.

456580: Async mux_mode behaviour is not supported by some flash devices.

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0, Fixed in r2p1-00rel0.

Description

In async mux mode, WE is asserted at the same time as CS. However, for some flash devices, WE must be asserted after the address phase of the transfer.

Implications

Some mux_mode flash devices may not be supported.

Workaround

None.

456826: PREADY not returned early for APB writes to direct_cmd register when PCLKEN is not tied high

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0, Fixed in r2p1-00rel0.

Description

If the APB is clocked at a slower frequency than ACLK (i.e. PCLKEN is not tied high) then PREADY may not be returned until the completion of the access. For APB direct_command accesses this can involve a sequence of the current APB access and one or more AXI accesses. In this instance PREADY will not be retuned until the data match occurs.

Implications

In some systems it may not be possible to write to the AXI channel until the APB channel has completed. This could cause a system deadlock. Please note that the NAND flash memory controller is not affected by this problem.

Workaround

When executing AXI direct_command sequences ensure PCLKEN is tied high.

501623: CS not deasserted in accesses to NAND in certain modes of operation

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

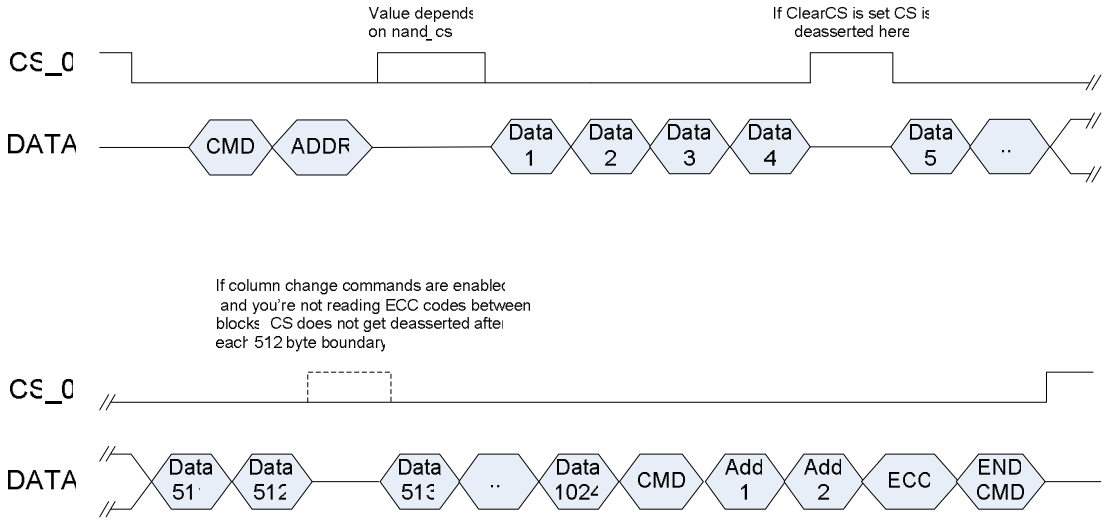
Fault status: Cat 2, Present in: r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

PL351/353 is designed to support NAND devices that require **CS** to be held low between data-phase accesses, as well as devices that do not have this requirement. To satisfy both types of memory the ECC block will not de-assert **CS** after a block has been completed if it is about to issue a command.

However, in certain modes of operation (specifically when column-change commands are enabled and you are not reading ECC codes between blocks), PL351/353 incorrectly assumes that it is about to perform an operation and cancels the request to ClearCS.

This results in **CS** not being deasserted after the last transfer in a 512 byte block and while **CS** is deasserted the EBI will not be released. The following timing diagram illustrates the **CS** behaviour.



Implications

Under the above mentioned conditions, **CS** will not be deasserted. This could result in a deadlock situation if data or code required to create the next transaction is stored through the same EBI.

Workaround

If ECC is disabled, this problem will not occur.

When using ECC, there are two possible work arounds:

1. Use the ECC block in full command mode for writes, and read ECC codes between blocks for reads.

2. If you are reading or writing more than one 512 byte block, ensure that the data crosses the 512 byte boundary in a single un-interrupted transaction.

534963: Potential data error when writing to SRAM with ACLK async to MCLK

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

When writes are performed by the memory controller, write data and command are pushed into the respective FIFOs in the same cycle. When running with ACLK asynchronous to MCLK, there is no guarantee that the two sets of data will arrive in the MCLK domain in the same cycle. The write data may be one cycle later.

The memory FSM only checks that the write data has arrived when it is in the IDLE state.

A problem can occur if the FSM is not idle when a new write command is popped from the command FIFO. This new command can be started back to back with a previous command but there is no check to see that the write data has arrived.

This problem can only occur when ACLK/MCLK are asynchronous doing non mux mode writes to SRAM where all the write data for the memory burst is contained in a single AXI beat.

The NAND interface is unaffected.

Implications

If this occurs then data written to memory will be corrupted.

Workaround

The following work arounds exist

1) For async non-muxmode writes use a memory burst length that is long enough to contain more than one AXI beat (normally memory burst length of 4 will do this).

This workaround has least impact on performance because AXI bursts of data (greater than 1 beat) are treated optimally on the memory interface.

This workaround can be used provided the memory device supports back to back transactions without chip select being deasserted.

2) If the memory device requires chip select to be deasserted between bursts, then the best workaround is to set the refresh_period register to 1. This ensures the FSM returns to idle between every transaction. This adds tTR idle cycles between each transaction of a burst that would otherwise have completed back to back.

721059: SLC ECC misses single error to bit0 byte0 and fails to detect some double error cases

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 2, Present in: r2p1-00rel0, Open.

Description

There is a defect in the coding of the SLC ECC algorithm.

Only the odd half of the parity calculation is being tested to check for pass / fail.

When reading the data from NAND with the SLC ECC enabled, in some specifc cases, the results indicated in the registers will be incorrect.

The rendered file

pl35x_ecc_reg_<xmlcfg>.v will contain multiple instances of a line such as

assign next_ecc1_data_0_pass_fail = |ecc1_data_0_ecc_odd & next_ecc1_data_0_read;

Only the "_ecc_odd" vector is being tested to determine pass fail.

Both the odd and even halves should be tested.

assign next_ecc1_data_0_pass_fail = ((|ecc1_data_0_ecc_odd) || (|ecc1_data_0_ecc_even)) & next_ecc1_data_0_read;

Implications

There are three implications of this errata.

1. A single bit error in data byte 0, bit 0 will not be detected.

This error case will result in a false positive that the data has passed the error check.

2. A single bit error in second 12 bits of the 3 parity bytes read from the spare area, will incorrectly be identified as having passed the error check.

The algorithm intent is that errors occurring in the spare area, will be flagged as uncorrectable fail.

3. Some double error cases are not correctly identified as uncorrectable fail.

90 double errors out of the 8485140 possible double error combinations are not correctly identified as uncorrectable fail.

- All double errors in the data (8386560 possible errors) will be correctly identified as uncorrectable fail.

- 66 of the 276 possible double errors in the parity bytes are not identified as uncorrectable fail

- 24 of the 98304 possible 1 error in data 1 error in parity, will not be identified as uncorrectable fail

These 90 cases will result in a false positive that the data has passed the error check.

Workaround

There is a software workaround to the first implication of this defect.

If a single bit error occurs to byte 0, bit 0, the ECC register values return ecc_fail = 1'b0

ecc_correct = 1'b1

This result uniquely identifies a single bit error to byte 0, bit 0 in the current implementation.

The register values can be read to identify this case, and the bit error can be corrected.

A more complex software workaround is to manually read the ECC parity data stored in the spare area and then use software to calulate the ECC result independently of the hardware mechanism.

Errata - Category 3

381382: Memory FSM incorrectly coded for use with NAND boot enable

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0, Fixed in r1p1-00rel1.

Description

When in NAND boot mode, the controller uses the interrupt to pause operation during busy periods.

At the end of each command access the interrupt is cleared, so that it can be set again after the busy period has elapsed.

The controller will resume operation when the interrupt is set again (on the rising edge of the NAND busy signal).

An error in the FSM causes the interrupt to be cleared before the data read can start, and therefore the controller gets stalled indefinitely.

Implications

The NAND boot feature cannot be guaranteed to work as expected.

Workaround

None

404770: NAND boot mode problem for some NAND memory device protocols

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1, Fixed in r1p1-01rel0.

Description

In NAND boot mode, the static memory controller stalls operation during the NAND busy period following the command phase of a read access.

The flag that controls this stall internally is currently set when moving from command state to idle state, for example when finishing the second command of a page read program.

For memories that do not require this second command, this flag is not being set and hence the controller does not stall operation during the NAND busy period.

Implications

When using the NAND boot feature, if the PL350 controller does not issue a second command in a read program, then it will not stall during the memory device's busy period.

Therefore, if the memory device cannot accept a second command and the data access is attempted before the busy period elapses a violation will occur.

Workaround

Some NAND devices automatically power-on in page-read mode.

Memories which cannot support a second command as part of a page read program, but power-on in read mode could be booted from by only issuing read data accesses without the command phase.

The necessary code for booting and loading the driver would need to fit into the first page of memory as other pages could not be accessed without a read command.

408515: Memory Configuration Register does not indicate mux_mode correctly

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

The Memory Configuration Register does not correctly report if an interface is in mux_mode as stated in the TRM.

Implications

none

Workaround

none

409123: Setting tWP to 1 in async mux_mode gives a tWP value of 0.

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

Setting tWP to 1 in async mux_mode gives a write pulse width of 0.

Implications

none

Workaround

To work around the problem set tWP = 2 which will give a longer but valid write pulse width.

412923: Can enter low_power mode while transactions are still outstanding

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

If the SMC is idle and receives a power down request followed by an AXI transaction in the same or subsequent cycle the transaction will get registered into the AXI interface but the SMC will still enter low-power mode.

If all the necessary data has been been received (or the transaction is a read) it will be completed by the SMC. However, if the there is still data outstanding the transaction will not complete until a power-up request is received.

If this occurs, resetting the SMC while in low-power mode, before all the transactions have been completed, would result in AXI protocol violations.

Implications

AXI protocol violations could result from this activity.

Workaround

There are no registers in the SMC that cannot be accessed while not in low-power mode. Therefore, low-power mode should not be entered unless all masters have completed accessing the SMC.

418214: Register update mechanism mismatching manager commands

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

The PL350 controller series implement a mechanism to synchronise updates to format and timing configuration registers with updates to memory devices' internal registers.

If a "ModeReg And UpdateRegs" direct command is applied whilst a "ModeReg" direct command to the same chip is being processed in the controller's pipeline then the update logic incorrectly updates the controller's internal registers when the first ModeReg command completes on the memory interface.

For example, a PSRAM device has a Bus Configuration Register (BCR) that dictates parameters such as burst length. A use case for programming the controller and memory to a new burst length is to issue a "ModeReg and UpdateRegs" direct command.

PSRAM devices also contain a Refresh Configuration Register (RCR) to control its self-refresh function. A use case for programming the memory to a new setting is to isse a "ModeReg" direct command.

If the RCR update is performed immediately prior to the BCR, the described error condition could occur.

Implications

If an AXI access is accepted into the format stage of the pipeline after the internal registers have updated, but before the second ModeReg command, then it will be formatted with the new settings. This will result in unpredictable behaviour.

Workaround

The recommended workaround is to always perform "ModeReg and UpdateRegs" commands before "ModeReg" commands.

For example, in the case described above involving PSRAM, perform the BCR then the RCR.

445213: Remap functionality can be wrong

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

The remap pins on PL35x can be used to map chip 0 of a memory interface to address 0x00000000.

However, it aliases chip 0 but does not hide other chips out of the way.

For example if PL35x is set up so that chip 1 is at 0x00000000 and chip 0 is at 0x0100000 then when remap is asserted PL35x would try to map an incoming AXI command to both chips.

The other chip can be on either interface on dual interface configurations

There are three possible (pre-silicon) workarounds

1) Do not place any memory chip selects at base address 0x00000000

2) Configure chip select 0 at address 0x00000000 therefore removing the need for a remap.

3) Tie the address match and mask pins to programmble registers to allow the chip select addresses to be programmable.

Implications

PL350 does not support accesses to two chips at the same time. The behaviour is undefined.

Workaround

None

447567: READY not returned when zero's written to memc_cfg_set & memc_cfg_clr

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

The memc_cfg_set and memc_cfg_clear registers are write-only registers in which each bit enables or disables a particular function.

Writing 32'h00000000 to these registers should have no functional effect. However,

pready is never returned if such a write does occur.

(This will prevent **hready** being returned in an AHB based system)

Implications

The APB (or connected AHB) transaction will never complete.

Workaround

Do not write zero to either the memc_cfg_clear or memc_cfg_set registers.

456825: Command phase time may be one cycle short during ECC if aclk synchronously greater than mclk

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r2p0-00rel0,r2p0-02rel0, Fixed in r2p1-00rel0.

Description

If aclk and mclk are synchronous to each other and aclk is greater than mclk and the ecc column jump function is enabled, then it may be possible for the command phase to be

one cycle short.

Implications

Undefined behaviour may be observed from the memory device as timing paramters may be violated.

Workaround

If using the column jump functionality of the ecc block ensure that t_wc and t_wp are both one cycle longer than required.

533517: FIFO depths chosen in AMBA Designer may be inconsistent

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

When configuring the memory controller in AMBA Designer there is a potential case that choosing Read FIFO depths may cause confusion.

In the configuration window, the desired Read FIFO depth can be selected for each memory interface (for example "12").

If the desired memory width is then chosen, the Read FIFO depth is reset to the default for that memory width (eg "2"). This is because the valid options change for different memory widths.

If the "OK" button is pressed, the memory controller is generated with the default Read FIFO depth (eg "2").

If the right click AMBA Designer -> "reconfigure" option is now selected, the configuration window is opened. The value in the Read FIFO depth is the "12" input above, not that of the rendered memory controller (which was the default "2").

If the "OK" button is pressed the memory controller will be generated with the Read FIFO depth from the configuration window (here "12"). This would lead to changing the Read FIFO depth, without specifically choosing to.

The values in the configuration window, when "OK" is pressed are always those used for RTL generation.

Implications

Confusion may arise when selecting FIFO depths.

The options in the configuration window are those used in the RTL generation process.

Workaround

Check all the values in the configuration window, before pressing the "OK" button.

The values in the configuration window are those used in the RTL generation process.

583618: Explicit Perl paths causing RTL rendering issues on certain machines

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Cat 3, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

The Perl script used to render the desired configuration of the RTL has a hard coded path to where it expects Perl to be installed.

shared/bin/render.pl

contains:

#!/usr/local/bin/perl -w

If a suitable Perl version is not installed here, an error can occur.

The cause of the error can be hard to trace.

Implications

During the render process an error may occur.

The RTL will not be rendered successfully.

Workaround

The simplest workaround is to create a unix soft link so that the installed version of Perl is found in /usr/local/bin/perl.

Alternatively the render.pl script can be modified to replace

#!/usr/local/bin/perl -w

with

eval "exec perl -w -S $0 $@" # -*- Perl -*-

if ($running_under_some_sh);

undef ($running_under_some_sh);

This ensures the script uses the installed version of Perl.

Errata - Documentation

381891: Row boundary behaviour not documented

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p0-00rel0, Fixed in r1p1-00rel0.

Description

The documentation does not specify the behaviour of the controller with respect to memory row boundaries.

The controller has no knowledge of row boundary information so cannot prevent memory bursts crossing such boundaries. However, the burst alignment functionality of the controller allows bursts to always be aligned, and not cross, memory burst address boundaries. Since memory burst boundaries are smaller than row boundaries, in this mode row boundaries will not be crossed.

Implications

Some memories, for example Cellular RAM, do not support row boundary crossing. The burst_align bit of the set_opmode register must be left at 1'b0 so that bursts are aligned to memory burst address boundaries. This will ensure that memory row boundaries are never crossed.

Workaround

none

404182: DDI0380C SMC (PL350 series) r1p1 TRM, incorrect reset value for sram_cycles register

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1, Fixed in r1p2-00rel0.

Description

In Table 3-1 of the TRM DDI0380C, the reset value of register sram_cycles<x>_<n> is given as 0x0000AAFF.

This is incorrect. The reset value should be set to 0x0002B3CC.

Implications

none

Workaround

none

404184: DDI0380C SMC (PL350 series) r1p1 TRM, incorrect waveform in Fig 2-16

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

In Fig 2-16 of the TRM DDI0380C, the WE waveform is incorrect. It is shown as being asserted many cycles after CS gets asserted.

WE should be shown to go low, that is get asserted on the same cycle as CS.

WE in this figure should also be shown to be asserted for twp+2 cycles instead of twp, since in asynchronous mux-mode WE is asserted for twp+2 cycles.

The following restriction on timing parameters should also be mentioned:

For writes in mux mode, tWC should be set to a value >= tWP + 2.

Implications

none

Workaround

none

404865: DDI0380C SMC (PL350 series) r1p1 TRM, Figure 3-5 has incorrect address mapping

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

The top four registers

Comp_id_3, Comp_id_2, Comp_id_1, Comp_id_0

should be replaced by

pcell_id_3, pcell_id_2, pcell_id_1 and pcell_id_0 respectively.

The addresses shown on the right hand side of the figure are not correct.

From bottom to top, they should be

0xFE0 (corresponding to Periph_id_0), 0xFE4, 0xFE8, 0xFEC, 0xFF0, 0xFF4, 0xFF8 and 0xFFC.

Implications

none

Workaround

none

405861: Incorrect version of documentation in release

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel1, Fixed in r1p1-01rel0.

Description

Incorrect documentation versions relating to product revision r1p0 were delivered in error with the release of product r1p1-00rel1.

Implications

None

Workaround

Documentation from the previous (r1p1-00rel0) or subsequent (r1p1-01rel0) releases can be used.

408513: DDI0380D SMC (PL350 series) r1p2 TRM, memory configuration register description is incorrect

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

In the Memory Interface Configuration Register description on page 3-8 of TRM DDI0380C

bits[9:8] memory_type1 should read

```
Returns the memory interface 1 type:
b00 = Configuration does not include this memory interface
b01 = SRAM non-muxed
b10 = NAND
b11 = SRAM muxed
If b00, the remaining bit slices for memory interface 1 are always read as 0.
```

(not SRAM mixed as it currently states)

similarly bits[1:0] memory_type0 should read

```
Returns the memory interface 0 type:
b00 = Reserved
b01 = SRAM non-muxed
b10 = NAND
b11 = SRAM muxed.
```

However due to an rtl defect the register will never read b11. If the rtl defect is not fixed both the above descriptions should be:

```
b01 = SRAM
b10 = NAND
b11 = Reserved.
```

Implications

none

Workaround

none

408962: DII0137C SMC (PL350 series) r1p1 IM, how to connect EBI to SMC when the interfaces run at different frequencies

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

On page 2-9 of the IM, the following note should be added for better clarification of system connectivity:

If the EBI were used to interface between two memory controllers (for instance SMC0 and SMC1), and SMC0 and the EBI were running faster than SMC1, then the EBIGRANT signal from EBI to SMC1 must be synchronised to the slow clock domain of SMC1.

Since EBICLOCK is synchronous to the memory controller clock domain, one flip-flop is enough to match the EBIGRANT signal from the EBICLK domain to the memory controller clock domain.

This logic is applicable even if the two different memory interfaces of PL350 are running at different frequencies, or if one of the memory controllers were a DMC.

Implications

none

Workaround

none

411811: DDI0380C SMC (PL350 series) r1p1 TRM, Fig 5-1 shows incorrect values for set_cycles_val

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0, Fixed in r2p0-00rel0.

Description

In the TRM DDI0380C, Figure 5-1 says:

```
set_cycles_val = (t6<<18) | (t5<<15) | (t4<<12) | (t3<<9) | (t2<<6) | (t1<<3) | (t0);
```

This should be changed to

```
set_cycles_val = (t6<<20) | (t5<<17) | (t4<<14) | (t3<<11) | (t2<<8) | (t1<<4) | (t0);
```

Implications

none

Workaround

none

442865: DDI0380E SMC (PL350) TRM, incorrect ecc_value field width in ecc_value register

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r2p0-00rel0, Fixed in r2p0-02rel0.

Description

In PL350 r2p0 TRM, in table 3-22

Field ecc_value is given as bits [24:0]. This should be [23:0].

The reserved bits are given as bits [26:25]. This should be [26:24].

Implications

None

Workaround

None

445215: Use of ClearCS or nand_csl with the EBI can result in deadlock

Status

Affects: product AXI Static Memory Controller, SRAM NOR + NAND Flash Memory Ctlr -3YT.

Fault status: Doc, Present in: r0p0-00rel0,r1p0-00rel0,r1p1-00rel0,r1p1-00rel1,r1p1-01rel0,r1p1-01rel1,r1p2-00rel0,r2p0-00rel0,r2p0-02rel0,r2p1-00rel0, Open.

Description

Both the ClearCS bit in a NAND data phase command and the nand_csl tie-off cause the SMC to hold CS low after completing a transaction.

This is intended behaviour that is required by certain NAND memory devices.

In systems that share the NAND memory interface using an EBI it must be noted that while the SMC holds CS low it also keeps requesting the EBI.

This means that there are a number of conditions that may create a deadlock:

1. A master controlling the NAND command sequence interleaves transactions with another memory interface connected to another port on the EBI.

2. An independant master(s) accesses another memory interface in the same memory controller as the NAND memory interface and prevents the next NAND command reaching the NAND memory interface.

It is therefore a system design requirement to ensure these conditions cannot occur.

Implications

The system can deadlock

Workaround

Don't use NAND memory devices that requires chip select to be held low between transactions.

Errata – Driver Software

There are no Errata in this Category