ARM

ARM Core
ARM9E-S (AT170)
Errata Notice

This document contains all errata known at the date of issue in Rev.2 ARM9E-S product releases up to and including revision.r2p1. Refer to the Errata Summary Table on page 7 for information about which of the errata affect each revision.

Proprietary notice

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM Limited in the EU and other countries, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM Limited in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM Limited shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Document confidentiality status

This document is Non Confidential.

Web address

http://www.arm.com/

Feedback on the product

If you have any comments or suggestions about this product, contact your supplier giving:

- The product name
- A concise explanation of your comments.

Feedback on this document

If you have any comments on about this document, please send email to mailto:support-cores@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Contents

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- a unique defect tracking identifier
- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

22 Jul 2004: Changes in Document v1.0

Page	Status	ID	Cat	Summary
9	New	326713	Cat 2	Real monitor breakpoint missed in Thumb state

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus | X | indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r2p0	r2p1
326713	Cat 2	Real monitor breakpoint missed in Thumb state	X	

Errata - Category 1

There are no Errata in this Category.

Errata - Category 2

326713: Real monitor breakpoint missed in Thumb state

Status

Affects: product AT170_ARM9E-S.

Fault status: Cat 2, Present in: r2p0, Open. New in this Errata document.

Description

Under certain circumstances, a breakpoint on a Thumb instruction is not taken if Monitor mode debug is enabled.

In Monitor mode debug, if the core is configured for 32 bit Thumb instruction fetches, and a breakpoint is set on an odd half word address, the breakpoint is not taken if the instruction at the preceding even half word address is stalled due to an interlock.

Conditions

1. Debug is enabled (DBGEN is HIGH and Debug control register bit[5] is LOW)

2. 32-bit fetches in Thumb state are enabled (CFGTHUMB32 is HIGH)

3. Monitor mode debug is enabled (Debug control register bit[4] is HIGH)

4. A breakpoint is set on an odd halfword address (Address bit[1] = 1)

5. The instruction at the preceding even half word address is stalled due to an interlock

An example code sequence that causes this behavior is:

```
ADD R2, #4   ; Address = 0x100
LDR R0, [R1] ; Address = 0x102
ADD R0, #1   ; Address = 0x104, Interlock due to data dependency on LDR
STR R0, [R2] ; Address = 0x106, Breakpoint address
```

Implications

This errata only affects Monitor mode debug operations. The normal function of the core is not affected.

Workaround

To workaround this errata, use the BKPT instruction instead of setting breakpoints.

Errata - Category 3

There are no Errata in this Category.