

ARM® High Performance Physical IP Platform

Optimized for TSMC® 40nm G Process

The ARM® 40nm High Performance Physical IP Platform delivers process optimized IP, for best-in-class processor implementations.

ARM Physical IP, optimized specifically for the TSMC® CLN40G process, offers a suite of memory, logic, and interface products to jump start SoC designs. The base set of IP, enabling faster time-to-market, is available free to designers. An enhanced IP set, containing high speed and high density libraries, is available for purchase to further accelerate processor performance or minimize power consumption. All products are available for evaluation from the ARM website.



Memory Highlights

- Two family optimizations: High Density and High Speed
- Aspect ratio control for efficient floor planning
- Low active power and leakage only standby power
- Support for multiple retention and power down modes through fine-grain power gating
- Integrated BIST MUX

ARM Memory IP Family

ARM Memories provide SoC designers with a comprehensive platform of memory compilers to meet target performance, power and area needs. The High Speed compilers deliver memory instances of over 1GHz to maximize ARM processor performance. The High Density compilers, in contrast, generate dense SRAM arrays to meet stringent die size and cost constraints. In order to satisfy SoC design power-saving demands, ARM Memories also enable various degrees of partial and full shut down, resulting in leakage power reductions of 40-75%.

Logic Highlights

- High performance Multi-channel cell architecture, enabling power and area optimization
 - High Speed 12 track cells
 - High Density 9 track cells
- Advanced Power Management Kit
- Comprehensive cell library of greater than 1400 cells for each family

ARM Logic IP Family

ARM Logic IP provides designers over 10,000 cell options, enabling implementation of all logic functions for SoC development in consumer and enterprise applications. High Density libraries provide an optimal performance, area and power combination for power sensitive applications. High performance libraries are optimized for speed, delivering 15-25% better performance over competing products.

To address the leakage power challenges of sub-micron designs, the ARM Logic IP family includes Multi-channel length libraries. These libraries allow significant

DDR Highlights

- Drop-in PHY Macro (x32 or x16)
- DDR3/2 1600/1066Mbps capable
- DFI 2.0 Compliant interface

GPIO Highlights

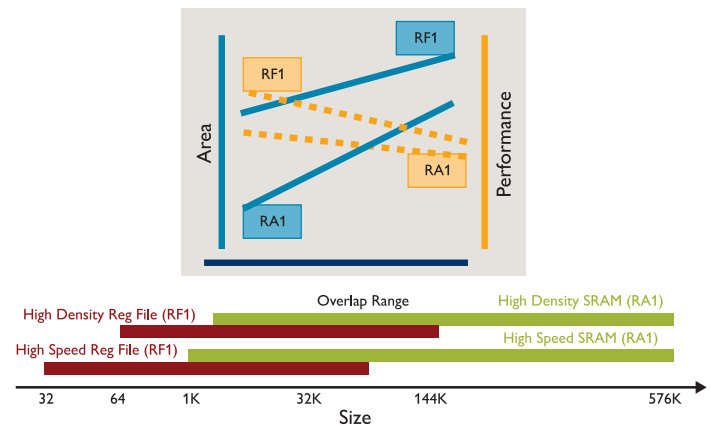
- Digitally programmable architecture
 - Bi-directional, 3-state, CMOS and Schmitt inputs
 - Drive strengths, voltage levels, and slew rates

ARM Interface IP Family

ARM DDR High Speed Interface (HSI) IP is a fully integrated hard macro that ensures robust operation between a DDR memory controller and the off-chip SDRAM. Delivered with full timing closure, this DFI-compliant drop-in solution achieves reliable high speed transfers of up to 1600Mbps for DDR3 and 1066Mbps for DDR2. Coupled with ARM PrimeCell™ Memory Controllers, this silicon-proven DDR PHY provides a complete interface solution for high speed memory interfaces.

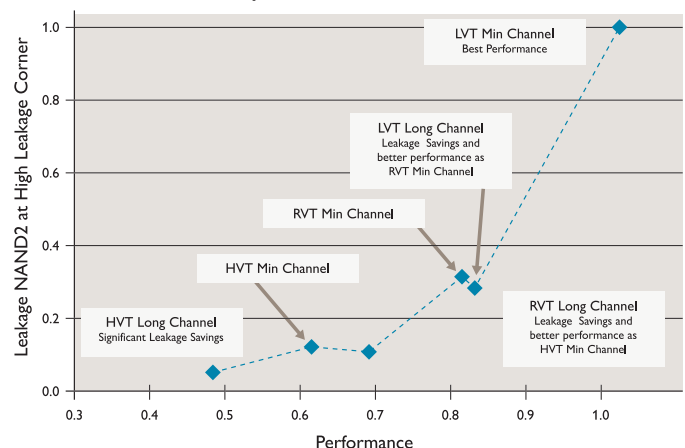
ARM advanced DFM techniques and tools also optimize yield without sacrificing performance. emBISTRx, a complete, high performance BIST/BISR subsystem offers yield and test strategy optimization. The ARM Physical IP development flow offers comprehensive QA and validation, resulting in accurate designs with high manufacturing yields. With increasing performance, as well as stringent power, area and DFM requirements, ARM Memories and tools deliver the most effective solution for processor optimization.

Performance/Area Tradeoffs in Memory Compilers

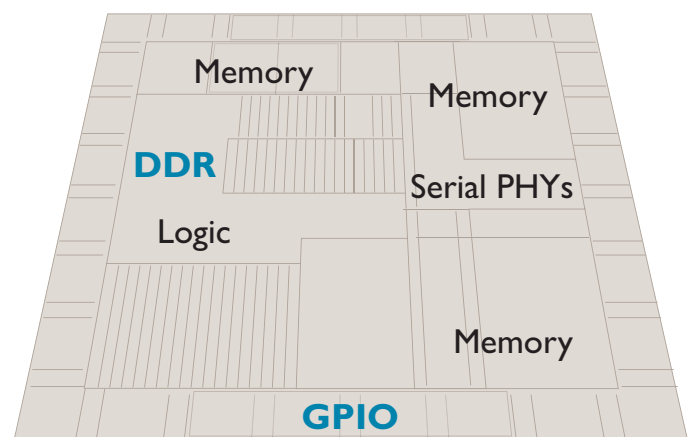


leakage power savings by replacing or complementing the HVt implant layer with long channel length devices, providing better performance, lower leakage and reduced manufacturing costs. Multi-channel libraries are footprint compatible, enabling effortless cell swapping for leakage optimization within standard design flows. ARM logic cell libraries optionally include a Power Management Kit (PMK) for advanced power savings and an Engineering Change Order (ECO) kit for design flexibility.

Multi-Channel Libraries: Big Power Savings for Comparable Performance



ARM GPIO provides a robust interface for off-chip connectivity. The comprehensive set of programmable features allows designers significant flexibility, without compromising die size. At 25um, the ARM GPIO have the smallest pitch in the industry. ARM GPIO leverage an advanced, low capacitance ESD structures consistent with ARM DDR. These structures ensure high SoC reliability and are silicon validated to reduce risk.



Support of Leading EDA Design Flows

Each ARM product is delivered with an extensive and accurate set of models, supporting industry-leading formats, validated with tools provided by ARM Connected Community™ EDA partners including Cadence, Magma, Mentor Graphics and Synopsys. The products are designed to support leading EDA solutions, such as those featured in TSMC Reference Flows.

EDA Deliverables Highlights

- Simulation models (Verilog)
- Timing models (non-linear and current source)
- Advanced power management modeling
- Signal integrity and IR drop analysis models
- Place-and-route abstracts
- LVS netlists and GDSII files



ARM Physical IP Platform Overview



ARM Memories are optimized to deliver fast processor performance while minimizing power consumption and die size. The Memories include advanced power management features, providing dynamic and leakage power savings, resulting in reduced packaging costs. High Density memories maximize the performance/area tradeoff for dense SRAM arrays with small real estate requirements. This innovative high-speed architecture, combined with processor-specific power management modes, enables superior ARM processor implementations, not available in generic solutions.



ARM Logic libraries deliver next-generation standard cells for high performance, mainstream and power-optimized configurations. Performance libraries unleash the frequency of high speed ARM processors, while the High Density libraries offer a balance between speed and area targets. Used in the combination, these libraries allow for independent

performance, area and power optimization across all regions of the SoC. The PMK and ECO kit reduce power consumption and lower overall design risk.



ARM DDR HSI IP enables high performance processor operation via low latency off-chip memory accesses. This IP is a drop-in ready, hard macro that is silicon proven and extensively tested across a wide range of process, voltage and temperature ranges. With wide operating margins and a history of volume production over several geometries and foundries, the ARM DDR HSI IP reduces overall memory interface design risk.

ARM GPIO IP provides SoC designers with a programmable interface designed to connect the ARM processor to the outside world. These tight pitch GPIO reduce pad ring area and provide design flexibility without compromising reliability.



ARM Contacts
www.arm.com

email contact:
sales-leads@arm.com

CHINA
+86 21 62351296

FRANCE
+33 1 39 30 47 89

GERMANY
+49 89 928 615 0

INDIA
+91 80 5138 4000

ISRAEL
+972 9 7632000

JAPAN
+81 45 477 5260

KOREA
+82 31 712 8234

NORWAY
+47 4000 5757

SINGAPORE
+65 6728 0950

TAIWAN
+886 2 2627 1681

UK
+44 1223 400400

USA
+1 408.576 1500

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