ARM® Performance Mobile Physical IP Platform

Optimized for Common Platform™ 32/28nm LP Process

The ARM® 32/28nm Performance Mobile Physical IP Platform delivers process-optimized IP, for best-in-class processor implementations.

The 32/28nm platform is comprised of logic libraries, memory compilers and interface IP. Collectively, they provide a powerful suite of design alternatives, offering System-on-Chip (SoC) designers the ability to balance performance, power, area and manufacturability throughout the design process. ARM leadership in microprocessor architectures, coupled with its Physical IP Platform, delivers optimal SoC designs and reduces time-to-market.

common platform solution provider™

ARM®

The Architecture for the Digital World®

Memory

Memory Highlights

- The industry's most comprehensive set of compilers on a single process technology
- Rich power management features
  - Low active and leakage power
  - Selective power management across various banks of memories
  - Multiple power domain support
- Advanced emBISTRx™ test and repair solutions, including support for ARM Cortex processors

ARM Memory IP Family

ARM Memory IP provides SoC designers with high quality memories to meet a wide range of performance, power and area requirements. The 32/28nm Memory family has been defined to specifically target Cortex™ ARM processors in key applications, ranging from ultra-low power wireless applications, supporting very low standby power, to optimum power/performance MID applications, that need performance and long battery life. The ARM Memory IP family also increases the speed of high performance, low active power applications such as high speed consumer netbooks. With an

Logic

Logic Highlights

- Multiple track heights and channel lengths offering a range of power and area design points
- Libraries offering more than 1,000 cells and 100 functions each
- Power Management Kit for active dynamic and leakage power reduction
- ECO Kit enabling cost and schedule-effective modifications
- Robust silicon validation and design practices ensuring successful designs

ARM Logic IP Family

The ARM 32/28nm Logic family consists of high performance and high density libraries with an enhanced cell set. They generate superior RTL-to-GDSII results through integration with state-of-the-art EDA tools and flows. The ARM development flow has the industry's most comprehensive QA and validation procedures, resulting in accurate designs with high manufacturing yields.

ARM Logic libraries contain an extensive selection of combinatorial and sequential cells. Library functions are available in multiple drive strengths to facilitate fast, dense and power-efficient designs. The Logic product line

Interface

DDR Highlights

- Drop-in, DFI compliant, hard macro PHY
- Programmable architecture enabling multiple configurations & power options
- Comprehensive DFT & PVT compensation

GPIO Highlights

- 2.5V Tolerant architecture with built-in hysterisis support
- Dynamically programmable slew rates, drive strengths, termination and retention
- Multiple package options, including: Flip Chip, Wire Bond, in-line, staggered and dual row

ARM Interface IP Family

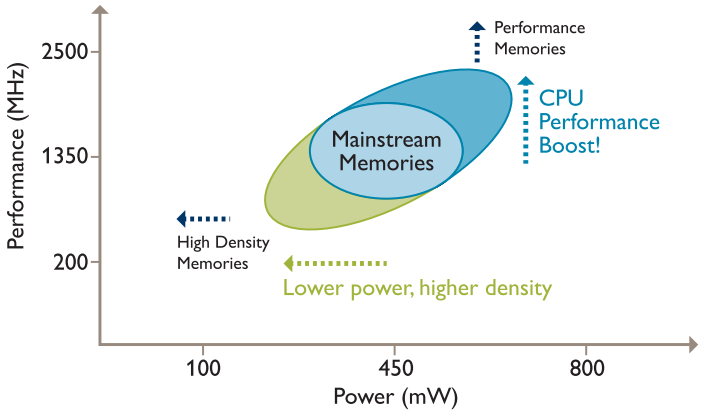
ARM Interface IP includes both the General Purpose and High Speed Interfaces (HSI) required to build a 32/28nm SoC pad ring. The High Speed Interface product family covers a broad range of applications for off-chip memory interfaces (DDR) while the programmable interface family covers various generic applications needing multi-voltage and voltage tolerant support.

The hard macro HSI DDR IP is designed to be fully compliant with DDR3/2 and LPDDR/2 SDRAM for simplified SoC integration. The DFI compliant DDR Interface IP enables seamless integration with ARM PrimeCell™ memory controllers for quick RTL-to-GDSII generation

advanced memory architecture combined with an extensive set of bit cells, the 32/28nm memories support multi-core requirements and enable fast memory accesses.

The Memory libraries for the Common Platform 32/28nm LP process will be fully characterized and delivered with a complete set of views and models supporting up to date industry-standard EDA tools.

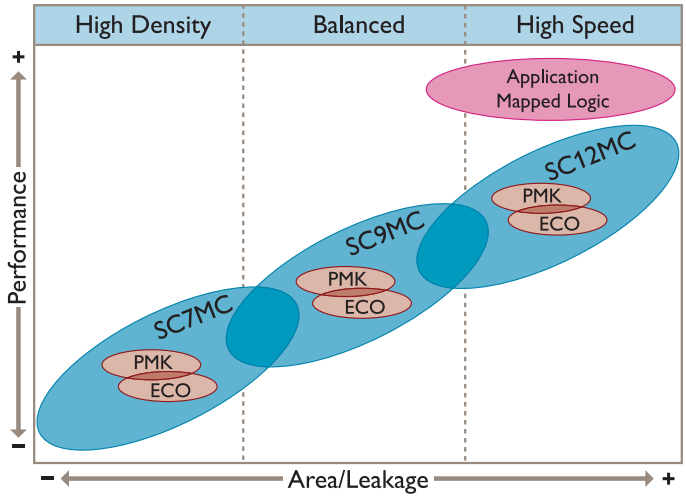
ARM Memory IP Family



has been synergistically developed with ARM Cortex processors, customer design benchmarks and EDA partners.

To address the challenges of sub-micron dynamic leakage power, the ARM Logic IP family includes Multi-Channel length cells. These Multi-Channel length libraries allow significant leakage power savings by replacing the HVt implant layer with long channel length devices, providing better performance, lower voltage and reduced manufacturing costs. Multi-channel libraries are footprint compatible, enabling effortless cell swapping for leakage/power optimization within standard design flows.

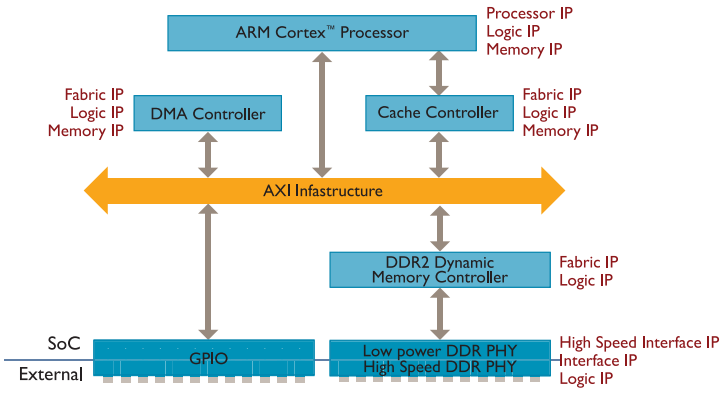
ARM Multi-Channel Logic IP



without compromising the power/performance trade-off.

The fully programmable general purpose Interface IP (GPIO) consists of a comprehensive set of building blocks for optimized pad ring development, supporting a wide range of form factors and package options. The flexible GPIO allows the designer to reconfigure the IO pads in order to achieve the best throughput and signal quality. All ARM Interface IP is designed to ensure high SoC reliability meeting industry-standard ESD and latch-up protection levels. The ARM development flow has the industry's most comprehensive QA and validation procedures.

ARM DDR Processor to Pads Solution



Support of Leading EDA Design Flows

Each ARM product is delivered with an extensive and accurate set of models, supporting industry-leading formats, validated with tools provided by ARM Connected Community™ EDA partners including Cadence, Magma, Mentor Graphics and Synopsys. The products are designed to support leading EDA solutions, such as those featured in Common Platform Reference Flows.

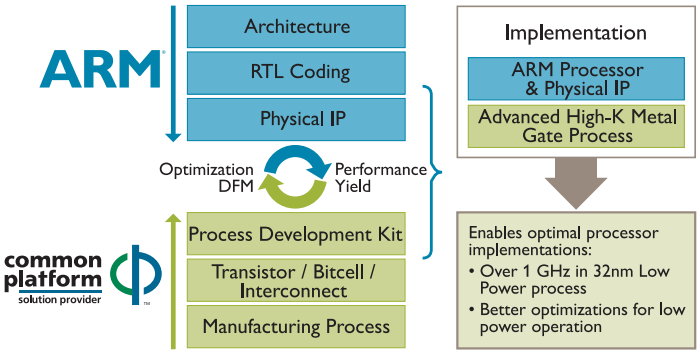
EDA Deliverables Highlights

- Simulation models (Verilog)
- Timing models (non-linear and current source)
- Advanced power management modeling
- Signal integrity and IR drop analysis models
- Place-and-route abstracts
- LVS netlists and GDSII files

cadence™ MAGMA Mentor Graphics SYNOPSYS®

ARM / Common Platform Partnership

The Common Platform has teamed with ARM to develop leadership silicon proven IP for the CMOS 32/28nm platform. This collaboration results in the highest performance, most power efficient ARM SoC implementations and facilitates broad industry adoption, all strengthened by the ARM global support infrastructure. ARM continues to work closely with the Common Platform to ensure early engagement on advanced nodes, full integration of ARM processor IP and comprehensive EDA support.



Common Platform

IBM, Chartered Semiconductor Manufacturing and Samsung Electronics have forged a unique manufacturing collaboration to implement bulk CMOS 32/28nm, 45nm, 65nm and 90nm process technologies. By combining the expertise and research resources of all three companies and leveraging advances such as High-k Metal Gate Technology (HKMG), 193nm immersion lithography and ultra low-k dielectrics, the Common Platform technology collaboration is able to accelerate the availability of leading-edge technology to foundry customers. The Common Platform model is supported by a comprehensive design-enablement ecosystem, enabling foundry customers to easily source their chip designs to multiple 300-mm foundries with minimal design work and with unprecedented flexibility and choice. In addition, the Common Platform solution consists of a complete range of design support from leading EDA, IP, and design services providers.

Innovation and industry leadership through collaboration

ARM

ARM Contacts

www.arm.com

email contact:

sales-leads@arm.com

CHINA +86 21 62351296	INDIA +91 80 5138 4000	KOREA +82 31 712 8234	TAIWAN +886 2 2627 1681
FRANCE +33 1 39 30 47 89	ISRAEL +972 9 7632000	NORWAY +47 4000 5757	UK +44 1223 400400
GERMANY +49 89 928 615 0	JAPAN +81 45 477 5260	SINGAPORE +65 6728 0950	USA +1 408 576 1500