Application Note AN505

Example IoT Subsystem design for V2M-MPS2+

Non-Confidential

Example IoT Subsystem design for V2M-MPS2+

Copyright © 2017 ARM. All rights reserved.

Release Information

The following changes have been made to this Application Note.

Product Status

The information in this document is Final, which is for a developed product.

Web Address

http://www.arm.com

Contents

Example IoT Subsystem design for V2M-MPS2+

1 Conventions and Feedback

The following describes the typographical conventions and how to give feedback:

Typographical conventions

The following typographical conventions are used:

`monospace`   denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space   denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
denotes arguments to commands and functions where the argument is to be replaced by a specific value.

`monospace bold`
denotes language keywords when used outside example code.

italic   highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold   highlights interface elements, such as menu names. Denotes signal names. Also used for emphasis in descriptive lists, where appropriate.

Feedback on this product

If you have any comments and suggestions about this product, contact your supplier and give:

- Your name and company.

- The serial number of the product.

- Details of the release you are using.

- Details of the platform you are using, such as the hardware platform, operating system type and version.

- A small standalone sample of code that reproduces the problem.

- A clear explanation of what you expected to happen, and what actually happened.

- The commands you used, including any command-line options.

- Sample output illustrating the problem.

- The version string of the tools, including the version number and build numbers.

Feedback on documentation

If you have comments on the documentation, e-mail `errata@arm.com`. Give:

- The title.

- The number, DAI0505B.

- If viewing online, the topic names to which your comments apply.

- If viewing a PDF version of a document, the page numbers to which your comments apply.

- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

ARM periodically provides updates and corrections to its documentation on the ARM Information Center, together with knowledge articles and *Frequently Asked Questions* (FAQs).

Other information

- ARM Information Center, `http://infocenter.arm.com/help/index.jsp`

- ARM Technical Support Knowledge Articles,
  `http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html`

- ARM Support and Maintenance,
  `http://www.arm.com/support/services/support-maintenance.php`

- ARM Glossary, `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014g/index.html`

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

2 Preface

2.1 Purpose of this application note

This application note discusses the operation of AN505. AN505 is an FPGA implementation of an IoT Subsystem that uses SIE200 components together with CMSDK peripherals to provide an example design.

2.2 References

- *ARM DDI 0218 – PrimeCell® SingleMaster DMA Controller (PL081) Technical Reference Manual.*

- *ARM 100112_0200_05_en – ARM® Versatile™ Express Cortex®-M Prototyping Systems (V2M-MPS2 and V2M-MPS2+).*

- *MCBQVGA-TS-Display-v12 – Keil MCBSTM32F200 display board schematic.*

- *ARM-ECM-0601256 – Cortex-M33 ARMv8-M IoT Kit VFP User Guide.*

2.3 Terms and abbreviations

CMSDK	*Cortex-M* System Design Kit.
DMA	Direct Memory Access.
MCC	Motherboard Configuration Controller.
RAM	Random Access Memory.
FPGA	Field Programmable Gate Array.
SCC	Serial Configuration Controller.
TRM	Technical Reference Manual.
APB	Advanced Peripheral Bus.
AHB	Advanced High-performance Bus.
RTL	Register Transfer Level.
SMM	Soft Macrocell Model.
MSC	Master Security Controller
PPC	Peripheral Protection Controller
EAM	Exclusive Access Controller
MPC	Memory Protection Controller
IDAU	Implementation Defined Attribution Unit

2.4 Subsystem version details

This SMM is generated using various packages. These are detailed below.

Version	Descriptions
BP210 r1p0	**Cortex®-M System Design Kit** Full version of the design kit supporting Cortex-M0, Cortex-M0 DesignStart, Cortex-M0+, Cortex-M3 and Cortex-M4. Also contains the AHB Bus Matrix and advanced AHB components.
SIE200_r1p0_LAC	**SIE200** SIE200 is a system IP library to enable ARMv8-M and TrustZone® for v8-M ecosystem. All SIE200 components have AHB5 interfaces to support ARMv8-M processors.
r0p1-00eac0	**ARM® Cortex®-M33** EAC release
r1p2	**PL081** PrimeCell® Single Master DMA Controller
r1p3-00rel1	**PL022** ARM PrimeCell® Synchronous Serial Port

Table 2-1 : Module versions

2.5 Encryption key

ARM supplies the V2M-MPS2+ motherboard with a decryption key programmed into the FPGA. This key is needed to enable loading of the prebuilt images, which are encrypted.

Caution

A battery supplies power to the key storage area of the FPGA. Any keys stored in the FPGA might be lost when battery power is lost. If this happens you must return the board to ARM for reprogramming of the key.

3 Overview

3.1 System block diagram

Figure 3-1 : System Overview

shows the high level diagram of the full MPS2+ FPGA System.
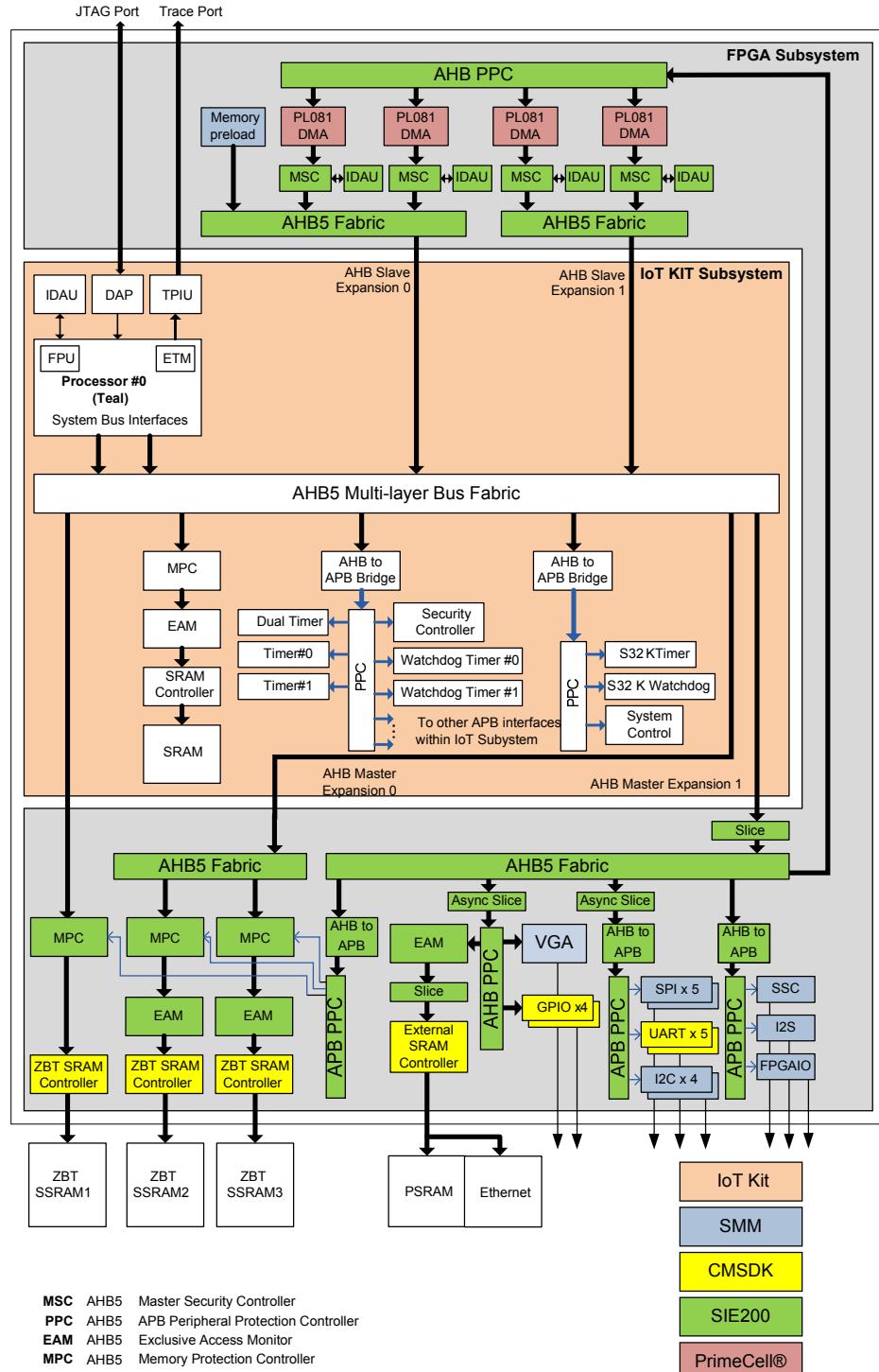
Figure 3-1 : System Overview

Note how the FPGA Subsystem extends the IoT Kit Subsystem by adding to its expansion interfaces.

3.2   SIE200 components

The following SIE200 components are used in this system:

- TrustZone AHB5 peripheral protection controller.

- TrustZone AHB5 master security controller.

- AHB5 bus matrix.

- AHB5 to AHB5 synchronous bridge.

- AHB5 to APB synchronous bridge.

- TrustZone APB4 peripheral protection controller.

- TrustZone AHB5 memory protection controller.

- AHB5 exclusive access monitor.

- AHB5 default slave.

3.3   Memory protection note

The SIE200 MPC and PPC components can affect memory and IO security management and must be configured as required for your application. Please see *Cortex-M33 ARMv8-M IoT Kit VFP User Guide* (ARM-ECM-0601256).

3.4 Memory Map Overview

This memory map includes information regarding IDAU security information for memory regions. For more information on these, please refer to the SIE200 components documentation.

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	0x0000_0000	0x0DFF_FFFF	224MB	Code Memory	Maps to AHB5 Master Expansion Code Interface	3	NS	0	0
2	0x0E00_0000	0x0FFF_FFFF	32MB	Reserved	Reserved				
3	0x1000_0000	0x1DFF_FFFF	224MB	Code Memory	Maps to AHB5 Master Expansion Code Interface	1	S	1	CODE NSC2
4	0x1E00_0000	0x1FFF_FFFF	32MB	Reserved	Reserved				
5	0x2000_0000	0x20FF_FFFF	16MB	Internal SRAM	Internal SRAM Area.	8	NS	2	0
6	0x2100_0000	0x23FF_FFFF	64MB	Reserved	Reserved				
7	0x2400_0000	0x2400_3FFF	4KB	Reserved	MTB				
8	0x2400_4000	0x27FF_FFFF	~64MB	Reserved	Reserved				
9	0x2800_0000	0x2FFF_FFFF	128MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	12			
10	0x3000_0000	0x30FF_FFFF	16MB	Internal SRAM	Internal SRAM Area.	5	S	3	RAMNSC
11	0x3100_0000	0x37FF_FFFF	112MB	Reserved	Reserved				
12	0x3800_0000	0x3FFF_FFFF	128MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	9			
13	0x4000_0000	0x4000_FFFF	64KB	Base Peripheral	Base Element Peripheral Region.	20	NS	4	0
14	0x4001_0000	0x4001_FFFF	64KB	Private CPU	CPU Element Peripheral Region.	21			
15	0x4002_0000	0x4002_FFFF	64KB	System Control	System Control Element Peripheral region.	22			
16	0x4003_0000	0x4003_FFFF		Reserved	Reserved				
17	0x4004_0000	0x4007_FFFF		Reserved	Reserved				
18	0x4008_0000	0x400F_FFFF	512KB	Base Peripheral	Base Element Peripheral Region.	25			
19	0x4010_0000	0x4FFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	26			
20	0x5000_0000	0x5000_FFFF	64KB	Base Peripheral	Base Element Peripheral Region.	13	S	5	0
21	0x5001_0000	0x5001_FFFF	64KB	Private CPU	CPU Element Peripheral Region.	14			
22	0x5002_0000	0x5002_FFFF	64KB	System Control	System Control Element Peripheral region.	15			

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	Security	IDAUID	NSC
23	0x5003_0000	0x5003_FFFF		Reserved	Reserved				
24	0x5004_0000	0x5007_FFFF		Reserved	Reserved				
25	0x5008_0000	0x500F_FFFF	512KB	Base Peripheral	Base Element Peripheral Region.	18			
26	0x5010_0000	0x5FFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	19			
27	0x6000_0000	0x6FFF_FFFF	256MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	28	NS	6	0
28	0x7000_0000	0x7FFF_FFFF	256MB	Expansion 0	Maps to AHB5 Master Expansion 0 Interface	27	S	7	0
29	0x8000_0000	0x8FFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	30	NS	8	0
30	0x9000_0000	0x9FFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	29	S	9	0
31	0xA000_0000	0xAFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	32	NS	A	0
32	0xB000_0000	0xBFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	31	S	B	0
33	0xC000_0000	0xCFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	34	NS	C	0
34	0xD000_0000	0xDFFF_FFFF	256MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	33	S	D	0
35	0xE000_0000	0xE00F_FFFF	1MB	PPB	Private Peripheral Bus. Local to each CPU	37	Exempt		
36	0xE010_0000	0xEFFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	38	NS	E	0
37	0xF000_0000	0xF00F_FFFF	1MB	System Debug	System Debug.	35	Exempt		
38	0xF010_0000	0xFFFF_FFFF	255MB	Expansion 1	Maps to AHB5 Master Expansion 1 Interface	36	S	F	0

Table 3-1 : Memory map overview

3.4.1 External ZBT SRAMs Synchronous SRAM for Code (SSRAM1)

4MB of ZBT memory is available in the code region of the memory map. The memory is named SSRAM1 and is mapped both to the Non-secure and secure code memory region as shown in Table 3-2. To Provide Security Gating, an MPC is place before this memory. It is called SSRAM1MPC, its configuration interface is located at 0x5800_7000 and its interrupt signal is connected to S_MPCEXP_STATUS[0]. All unused regions in the code memory space return bus error responses when accessed.

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	**0x0000_0000**	**0x003F_FFFF**	**4MB**		**ZBT SRAM (SSRAM1)**	5			
2	**0x0040_0000**	**0x007F_FFFF**	**4MB**	Code Memory	**SSRAM1 alias**	6			
3	0x0080_0000	0x0DFF_FFFF	116MB		Not used. Returns Bus Errors when accessed.	-	NS	0	0
4	0x0E00_0000	0x0FFF_FFFF	32MB	Reserved	Reserved	-			
5	**0x1000_0000**	**0x103F_FFFF**	**4MB**		**ZBT SRAM (SSRAM1)**	1			
6	**0x1040_0000**	**0x107F_FFFF**	**4MB**	Code Memory	**SSRAM1 alias**	2			CODE NSC
7	0x1080_0000	0x1DFF_FFFF	116MB		Not used. Returns Bus Errors when accessed.	-	S	1	
8	0x1E00_0000	0x1FFF_FFFF	32MB	Reserved	Reserved	-			

Table 3-2 : External SSRAM1 mapping to Code Memory

Because 4MB of memory exists in an 8MB window, the top 4MB of that window is aliased with the lower 4MB. As a result, both will share the same security setting. This ensures that there are no security holes that allow secure and non-secure access to the same physical location on the ZBT SSRAM at the same time.

The SSRAM1MPC is configured as follows:

DATA_WIDTH	32bits	Data Width: 32bits
ADDR_WIDTH	22	Address Width. Set at 22bits to support 4 Mbyte of memory space.
MASTER_WIDTH	5	HMASTER signal width. 5 bit for 32 masters
USER_WIDTH	0	User signal width parameter, default: 1, ports tied if 0
BLK_SIZE	8	Block size: (1 << BLK_SIZE) bytes, min. value: 5, max. value: 20. Set at 8 for 256 byte blocks.
GATE_RESP	0	Response on data AHB when accessed during programming lock: 0 – Add wait states until lock is released (default) 1 – Drive bus error

Table 3-3 : SSRAM1MPC Configuration settings.

3.4.2 External ZBT SRAMs Synchronous SRAM (SSRAM2 and SSRAM3)

4MB of ZBT memory is available in the expansion 0 region of the memory map. The memory is formed by the combination of memories SSRAM2 and SSRAM3. All unused regions shown in the table return bus error responses when accessed.

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	0x2000_0000	0x2007_FFFF	32KB	SRAM	FPGA Block Ram	6			
2	0x2080_0000	0x23FF_FFFF	56MB	Reserved	Reserved				
3	0x2400_0000	0x2400_3FFF	4KB	Reserved	MTB				
4	0x2400_4000	0x27FF_FFFF	~64MB	Reserved	Reserved		NS	2	0
5	**0x2800_0000**	**0x281F_FFFF**	**2MB**		**ZBT SRAM (SSRAM2)**	10			
6	**0x2820_0000**	**0x283F_FFFF**	**2MB**	Expansion 0	**ZBT SRAM (SSRAM3)**	11			
7	0x2840_0000	0x2FFF_FFFF	124MB		Not used. Returns Bus Errors when accessed.				
8	0x3000_0000	0x3007_FFFF	32KB	SRAM	FPGA Block Ram	1			
9	0x3080_0000	0x37FF_FFFF	~128MB	Reserved	Reserved				
10	**0x3800_0000**	**0x381F_FFFF**	**2MB**		**ZBT SRAM (SSRAM2)**	5	S	3	RAM NSC
11	**0x3820_0000**	**0x383F_FFFF**	**2MB**	Expansion 0	**ZBT SRAM (SSRAM3)**	6			
12	0x3840_0000	0x3FFF_FFFF	124MB		Maps to AHB5 Master Expansion 0 Interface				

Table 3-4 : SSRAM2 and SSRAM3 address mapping

An Exclusive Access Monitor and a Memory Protection Controller exists on the path of each ZBT SRAM. They support exclusive access and security gating so that blocks of aliased memory can be assigned individually to Secure or Non-secure regions. The two MPCs are as follows:

- SSRAM2MPC is the MPC for SSRAM2. Its APB interface is mapped to address 0x5800_8000 and its interrupt signal is connected to S_MPCEXP_STATUS[1].
- SSRAM3MPC is the MPC for SSRAM3. Its APB interface is mapped to address 0x5800_9000 and its interrupt signal is connected to S_MPCEXP_STATUS[2].

Both SSRAM1MPC and SSRAM2MPC have the same configuration settings as listed in Table 3-5.

Parameter	Configuration	Description
DATA_WIDTH	32bits	Data Width: 32bits
ADDR_WIDTH	22	Address Width. Set at 22bits to support 4 Mbyte of memory space.
MASTER_WIDTH	5	HMASTER signal width. 5 bit for 32 masters
USER_WIDTH	0	User signal width parameter, default: 1, ports tied if 0
BLK_SIZE	8	Block size: (1 << BLK_SIZE) bytes, min. value: 5, max. value: 20. Set at 8 for 256 byte blocks.
GATE_RESP	0	Response on data AHB when accessed during programming lock: 0 – Add wait states until lock is released (default) 1 – Drive bus error

Table 3-5 : SSRAM2MPC and SSRAM3MPC Configuration settings.

3.4.3 PSRAM

The V2M-MPS2+ FPGA prototyping board provides a 16bit PSRAM interface supporting two banks of Parallel SRAMs each up to 8MB, providing a total of 16MB of SRAM. These memories are currently mapped only to non-secure SRAM space as follows:

ROW ID	Address From	To	Size	Region Name	Description	Alias With Row ID	IDAU Region Values Security	IDAUID	NSC
1	**0x8000_0000**	**0x80FF_FFFF**	**16MB**	AHB Master Expansion 1 Interface Area	**PSRAM**		NS	8	0
2	0x8100_0001	0x8FFF_FFFF	246MB		Not used. Returns Bus Errors when accessed.				

Table 3-6 : External PSRAM mapping to Code Memory

3.4.4 Expansion System peripherals

Other than the SSRAMs, PSRAMs and the Ethernet MAC and PHY, all FPGA peripherals that are extensions to the IoT KIT are mapped into two key areas of the memory map:

- 0x4010_0000 to 0x4FFF_FFFF Non-Secure region which maps to AHB Master Expansion 1 interface.

- 0x5010_0000 to 0x5FFF_FFFF Secure region which maps to AHB Master Expansion 1 interface.

Table 3-7 shows how these peripherals are mapped.

To support TrustZone-ARMv8M and allow Software to map these peripherals to secure or non-secure address space, many peripherals are mapped twice and either APB PPC or AHB PPC is then used to gate access to these peripherals. An FPGA Secure Privilege Control block and a non-secure Privilege Control block then provide controls to these PPC.

For expansion AHB Masters within the system, there is a Master Security Controller (MSC) added to each master with an associated IDAU. Masters that have IDAU are:

- PL081 DMA Engine. All DMAs can be mapped as Secure or Non-Secure Masters. The intention is to support the use-case where for each pair of DMAs that shared a single AHB expansion interface, one is mapped as a secure and another is mapped as non-secure.

ROW ID	Address From	To	Size	Description	Alias With Row ID	IDAU Region Values Security	ID
1	0x4010_0000	0x4010_0FFF	4K	GPIO 0	37		
2	0x4010_1000	0x4010_1FFF	4K	GPIO 1	38		
3	0x4010_2000	0x4010_2FFF	4K	GPIO 2	39		
4	0x4010_3000	0x4010_3FFF	4K	GPIO 3	40		
5	0x4010_4000	0x4010_FFFF		Not used. Returns Bus Errors when accessed.			
6	0x4011_0000	0x4011_0FFF	4K	DMA 0	42		
7	0x4011_1000	0x4011_1FFF	4K	DMA 1	43		
8	0x4011_2000	0x4011_2FFF	4K	DMA 2	44		
9	0x4011_3000	0x4011_3FFF	4K	DMA 3	45		
10	0x4011_4000	0x401F_FFFF		Not used. Returns Bus Errors when accessed.			
11	0x4020_0000	0x4020_0FFF	4K	UART 0 - J10	47		
12	0x4020_1000	0x4020_1FFF	4K	UART 1 - XBEE	48		
13	0x4020_2000	0x4020_2FFF	4K	UART 2 - Reserved	49		
14	0x4020_3000	0x4020_3FFF	4K	UART 3 - Shield 0	50		
15	0x4020_4000	0x4020_4FFF	4K	UART 4 - Shield 1	51		
16	0x4020_5000	0x4020_5FFF	4K	FPGA - PL022 (SPI – J21)	52		
17	0x4020_6000	0x4020_6FFF	4K	FPGA - PL022 (SPI for LCD)	53		
18	0x4020_7000	0x4020_7FFF	4K	FPGA - SBCon I2C (Touch)	54	NS	4
19	0x4020_8000	0x4020_8FFF	4K	FPGA - SBCon I2C (Audio Conf)	55		
20	0x4020_9000	0x4020_9FFF	4K	FPGA - PL022 (SPI ADC)	56		
21	0x4020_A000	0x4020_AFFF	4K	FPGA - PL022 (SPI Shield0)	57		
22	0x4020_B000	0x4020_BFFF	4K	FPGA - PL022 (SPI Shield1)	58		
23	0x4020_C000	0x4020_CFFF	4K	SBCon (I^2C – Shield0)	59		
24	0x4020_D000	0x4020_DFFF	4K	SBCon (I^2C - Shield1)	60		
25	0x4020_E000	0x402F_FFFF		Not used. Returns Bus Errors when accessed.			
26	0x4030_0000	0x4030_0FFF	4K	FPGA - SCC registers	62		
27	0x4030_1000	0x4030_1FFF	4K	FPGA - I2S (Audio)	63		
28	0x4030_2000	0x4030_2FFF	4K	FPGA - IO (System Ctrl + I/O)	64		
29	0x4030_3000	0x40FF_FFFF		Not used. Returns Bus Errors when accessed.			
30	0x4100_0000	0x4100_FFFF	64K	VGA Console	66		
31	0x4110_0000	0x4113_FFFF	256K	VGA Image	67		
32	0x4114_0000	0x41FF_FFFF		Not used. Returns Bus Errors when accessed.			
33	0x4200_0000	0x420F_FFFF	1M	Ethernet	69		
34	0x4210_0000	0x4800_6FFF		Not used. Returns Bus Errors when accessed.			
35	0x4800_7000	0x4800_7FFF	4K	FPGA Non-Secure Privilege Control			
36	0x4800_8000	0x4FFFF_FFFF		Not used. Returns Bus Errors when accessed.			
37	0x5010_0000	0x5010_0FFF	4K	GPIO 0	1		
38	0x5010_1000	0x5010_1FFF	4K	GPIO 1	2	S	5
39	0x5010_2000	0x5010_2FFF	4K	GPIO 2	3		

ROW ID	Address From	Address To	Size	Description	Alias With Row ID	IDAU Region Values Security ID
40	0x5010_3000	0x5010_3FFF	4K	GPIO 3	4	
41	0x5010_4000	0x5010_FFFF		Not used. Returns Bus Errors when accessed.		
42	0x5011_0000	0x5011_0FFF	4K	DMA 0	6	
43	0x5011_1000	0x5011_1FFF	4K	DMA 1	7	
44	0x5011_2000	0x5011_2FFF	4K	DMA 2	8	
45	0x5011_3000	0x5011_3FFF	4K	DMA 3	9	
46	0x5011_4000	0x501F_FFFF		Not used. Returns Bus Errors when accessed.		
47	0x5020_0000	0x5020_0FFF	4K	UART 0 - J10	11	
48	0x5020_1000	0x5020_1FFF	4K	UART 1 - XBEE	12	
49	0x5020_2000	0x5020_2FFF	4K	UART 2 - Reserved	13	
50	0x5020_3000	0x5020_3FFF	4K	UART 3 - Shield 0	14	
51	0x5020_4000	0x5020_4FFF	4K	UART 4 - Shield 1	15	
52	0x5020_5000	0x5020_5FFF	4K	FPGA - PL022 (SPI)	16	
53	0x5020_6000	0x5020_6FFF	4K	FPGA - PL022 (SPI for LCD)	17	
54	0x5020_7000	0x5020_7FFF	4K	FPGA - SBCon I2C (Touch)	18	
55	0x5020_8000	0x5020_8FFF	4K	FPGA - SBCon I2C (Audio Conf)	19	
56	0x5020_9000	0x5020_9FFF	4K	FPGA - PL022 (SPI ADC)	20	
57	0x5020_A000	0x5020_AFFF	4K	FPGA - PL022 (SPI Shield0)	21	
58	0x5020_B000	0x5020_BFFF	4K	FPGA - PL022 (SPI Shield1)	22	
59	0x5020_C000	0x5020_CFFF	4K	SBCon (Shield0)	23	
60	0x5020_D000	0x5020_DFFF	4K	SBCon (Shield1)	24	
61	0x5020_E000	0x502F_FFFF		Not used. Returns Bus Errors when accessed.		
62	0x5030_0000	0x5030_0FFF	4K	FPGA - SCC registers	26	
63	0x5030_1000	0x5030_1FFF	4K	FPGA - I2S (Audio)	27	
64	0x5030_2000	0x5030_2FFF	4K	FPGA - IO (System Ctrl + I/O)	28	
65	0x5030_3000	0x50FF_FFFF		Not used. Returns Bus Errors when accessed.		
66	0x5100_0000	0x5100_FFFF	64K	VGA Console	30	
67	0x5110_0000	0x5113_FFFF	256K	VGA Image	31	
68	0x5114_0000	0x51FF_FFFF		Not used. Returns Bus Errors when accessed.		
69	0x5200_0000	0x520F_FFFF	1M	Ethernet	33	
70	0x5210_0000	0x5800_6FFF		Not used. Returns Bus Errors when accessed.		
71	0x5800_7000	0x5800_7FFF	4K	SSRAM1 Memory Protection Controller (MPC)		
72	0x5800_8000	0x5800_8FFF	4K	SSRAM2 Memory Protection Controller (MPC)		
73	0x5800_9000	0x5800_9FFF	4K	SSRAM3 Memory Protection Controller (MPC)		
74	0x5800_A000	0x5FFFF_FFFF		Not used. Returns Bus Errors when accessed.		

Table 3-7 : FPGA Expansion Peripheral Map

4 Programmers Model

4.1 CMSDK and SIE200 components

This programmer's model is supplemental to the CMSDK, IoT kit, and ARMv8-M IoT Kit documentation, which covers many of the included components in more detail. Figure 3-1 : System Overview shows the connectivity of the system.

4.2 External ZBT Synchronous SRAM (SSRAM1)

SSRAM1 is ZBT RAM in the CODE region. This is interfaced to two external 32-bit ZBT SSRAM devices in parallel, forming a 64-bit ZBT SSRAM. 8MB of memory space is allocated, but only 4MB is used (each ZBT SSRAM is 2MB).

4.3 External ZBT Synchronous SRAM (SSRAM2 & SSRAM3)

The ZBT SSRAM is set up as two external ZBT SSRAMs, connected to two independent ZBT interfaces. 8MB of memory space is allocated, but only 4MB is used (each ZBT SSRAM is 2MB).

The address of the ZBT SSRAM is interleaved as shown in the table below.

Upper 32-bit ZBT SSRAM3	Lower 32-bit ZBT SSRAM2
0x287FFFFC (wrap round to 0x283FFFFC)	0x287FFFF8 (wrap round to 0x283FFFF8)
…	…
0x28400004 (wrap round to 0x28000004)	0x28200000 (wrap round to 0x28000000)
0x283FFFFC	0x283FFFF8
…	…
0x2800000C	0x28000008
0x28000004	0x28000000

Table 4-1 : 32 bit ZBT Memory Map

This memory is also accessible at 0x38000000 and is interleaved in the same way at that address.

Note: SSRAM2 and SSRAM3 are in the SRAM region. Running code from SRAM region is slower than from CODE region because the internal bus structure is not optimized for running programs from this region.

4.4 External PSRAM

A 16MB 16-bit PSRAM area is available and the memory map allocates the address-range 0x80000000 - 0x80FFFFFF. This enables large test programs to be used, for example *uClinux*, in the External RAM region of the Cortex-M memory space.

Note: PSRAM is in the SRAM region. Running code from SRAM region is slower than from CODE region because the internal bus structure is not optimized for running programs from this region.

4.5 AHB GPIO

The SMM uses four CMSDK AHB GPIO blocks, each providing 16 bits of IO. These are connected to the EXP port as follows.

EXP Port	GPIO
EXP[15:0]	GPIO0[15:0]
EXP[31:16]	GPIO1[31:16]
EXP[47:32]	GPIO2[47:32]
EXP[51:48]	GPIO3[51:48]
EXP[63:49]	Not used. Read as 0.

Table 4-2 : GPIO Mapping

The GPIO alternative function lines select whether or not peripherals or GPIOs are available for each pin. See section 8 - Shield Support for mappings.

4.6 SPI (Serial Peripheral Interface)

The SMM implements five PL022 SPI modules:

- One general purpose SPI module that connects to the general-purpose SPI connector, J21.

- Three general purpose SPI modules that connect to the Expansion headers J7 and J8. Intended for use with the V2C-Shield1 which provide an interface with the ADC and provide SPI on the headers. These are alt-functions on the EXP ports. See section 8 - Shield Support for mappings.

- One Color LCD module control.

The Self-test program provided with the MPS2+ includes example code for the color LCD module control interface.

Chip Selects are controlled by SCC register fpga_misc rather than the PL022 chip select output. See *Table 4-5 : System Control and I/O Memory Map* for more details.

4.7 SBCon (I²C)

The SMM implements four SBCon serial modules:

- One SBCon module for use by the Color LCD touch interface.

- One SBCon module to configure the audio controller.

- Two general purpose SBCon modules that connect to the Expansion headers J7 and J8. Intended for use with the V2C-Shield1 which provide an I^2C interface on the headers. See section 8 - Shield Support. These are alt-functions on the EXP ports. See section 8 - Shield Support for mappings.

The Self-test program provided with the MPS2+ includes example code for the color LCD module control and Audio interfaces.

4.8 UART

The SMM implements five CMSDK UARTs:

- UART 0 - J10.

- UART 1 – XBEE on shield adaptor board.

- UART 2 – Reserved.

- UART 3 - Shield 0 on shield adaptor board.

- UART 4 - Shield 1 on shield adaptor board.

UART 1, 3 and 4 are alt-functions on the EXP ports. See section 8 - Shield Support for mappings.

4.9 Color LCD parallel interface

The color LCD module has two interfaces:

- SPI for sending image data to the LCD.

- I^2C to transfer data input from the touch screen.

These interfaces are connected to a STMicroelectronics STMPE811QTR Port Expander with Advanced Touch Screen Controller on the Keil MCBSTM32C display board (schematic listed in the reference section). The Keil display board contains a AM240320LG display panel and uses a Himax HX8347-D LCD controller.

Self-test provided with the MPS2+ includes example code for both of these interfaces.

4.10 Ethernet

The SMM design connects to an SMSC LAN9220 device through a static memory interface.

The self-test program includes example code for a simple loopback operation.

4.11 VGA

Address	Description
0x41000000 - 0x4100FFFF 0x51000000 - 0x5100FFFF	Writes to the current location of the cursor.
0x41100000 - 0x4113FFFF 0x51100000 - 0x5113FFFF	512x128 image area at the top right of the screen. 0x41100000 is the top left of the area and 0x4113FFFF is the bottom right. HADDR[16:2] = YYYYYYYYXXXXXXXX where X and Y are the horizontal and vertical pixel offset respectively.

Table 4-3 : VGA Memory Map

For the image data, each pixel requires one 32 bit word, therefore, a total of 256KB are needed. The values in the data buffer are packed as 4 bits per channel in the format 0x00000RGB.

The pixel in the top left hand corner of the display occupies address 0x41100000 with each successive row using an offset of 0x00000400 from the previous row. For example, the leftmost pixel (LMP) of the 2nd row is at 0x41100400 and the LMP of the 3rd row is at 0x41100800. These addresses are aliased at 0x51100400 and 0x51100800.

4.12 Audio I²S

A simple FIFO interface generates and receives I²S audio.

Address	Name	Information
0x40302000 0x50302000	CONTROL	Control Register [31:18] : Reserved [17] : Audio CODEC reset control (output pin) [16] : FIFO reset [15] : Reserved [14:12] : RX Buffer IRQ Water Level - Default 2 (IRQ triggers when less than 2 word spaces available) [11] : Reserved [10: 8] : TX Buffer IRQ Water Level - Default 2 (IRQ triggers when more than 2 word spaces available) [7: 4] : Reserved [3] : RX Interrupt Enable [2] : RX Enable [1] : TX Interrupt Enable [0] : TX Enable
0x40302004 0x50302004	STATUS	Status register [31:6] : Reserved [5] : RX Buffer Full [4] : RX Buffer Empty [3] : TX Buffer Full [2] : TX Buffer Empty [1] : RX Buffer Alert (Depends on Water level) [0] : TX Buffer Alert (Depends on Water level)
0x40302008 0x50302008	ERROR	Error status register [31:2] : Reserved [1] : RX overrun - write 1 to clear [0] : TX overrun/underrun - write 1 to clear
0x4030200C 0x5030200C	DIVIDE	Divide ratio register (for Left/Right clock) [31:10] : Reserved [9: 0] LRDIV (Left/Right) Default = 0x80 12.288MHz / 48KHz / 2 (L+R) = 128
0x40302010 0x50302010	TXBUF	Transmit Buffer FIFO Data Register (WO) [31:16] : Left Channel [15: 0] : Right Channel
0x40302014 0x50302014	RXBUF	Receive Buffer FIFO Data Register (RO) [31:16] Left Channel [15: 0] Right Channel

Address	Name	Information
0x40302018 – 0x403022FC 0x50302018 – 0x503022FC	RESERVED	-
0x40302300 0x50302300	ITCR	Integration Test Control Register [31:1] : Reserved [0] : ITCR
0x40302304 0x50302304	ITIP1	Integration Test Input Register 1 [31:1] : Reserved [0] : SDIN
0x40302308 0x50302308	ITOP1	Integration Test Output Register 1 [31:4] : Reserved [3] : IRQOUT [2] : LRCK [1] : SCLK [0] : SDOUT

Table 4-4 : Audio I²S Memory Map

4.13 Audio Configuration

The SMM implements a simple SBCon interface based on I^{2}C. It is used to configure the Cirrus Logic Low Power Codec with Class D Speaker Driver, CS42L52 part on the V2M-MPS2+ board.

4.14 FPGA system control and I/O

The SMM implements an FPGA system control block.

Address	Name	Information
0x40028000 0x50028000	FPGAIO->LED0	LED connections [31:2] : Reserved [1:0] : LED
0x40028004 0x50028004	RESERVED	
0x40028008 0x50028008	FPGAIO->BUTTON	Buttons [31:2] : Reserved [1:0] : Buttons
0x4002800C 0x5002800C	RESERVED	
0x40028010 0x50028010	FPGAIO->CLK1HZ	1Hz up counter
0x40028014 0x50028014	FPGAIO->CLK100HZ	100Hz up counter
0x40028018 0x50028018	FPGAIO->COUNTER	Cycle Up Counter Increments when 32-bit prescale counter reach zero.
0x4002801C 0x5002801C	FPGAIO->PRESCALE	Bit[31:0] – reload value *for* prescale counter.
0x40028020 0x50028020	FPGAIO->PSCNTR	32-bit Prescale counter – current value of the pre-scaler counter. The Cycle Up Counter increment when the prescale down counter reach 0. The pre-scaler counter is reloaded with PRESCALE after reaching 0.
0x40028024 0x40028024	RESERVED	
0x4002804C 0x5002804C	FPGAIO->MISC	Misc control [31:10] : Reserved [9] : SHIELD1_SPI_nCS [8] : SHIELD0_SPI_nCS [7] : ADC_SPI_nCS [6] : CLCD_BL_CTRL [5] : CLCD_RD [4] : CLCD_RS [3] : CLCD_RESET [2] : RESERVED [1] : SPI_nSS [0] : CLCD_CS

Table 4-5 : System Control and I/O Memory Map

4.15 Serial Communication Controller (SCC)

The SMM implements communication between the microcontroller and the FPGA system through an SCC interface.
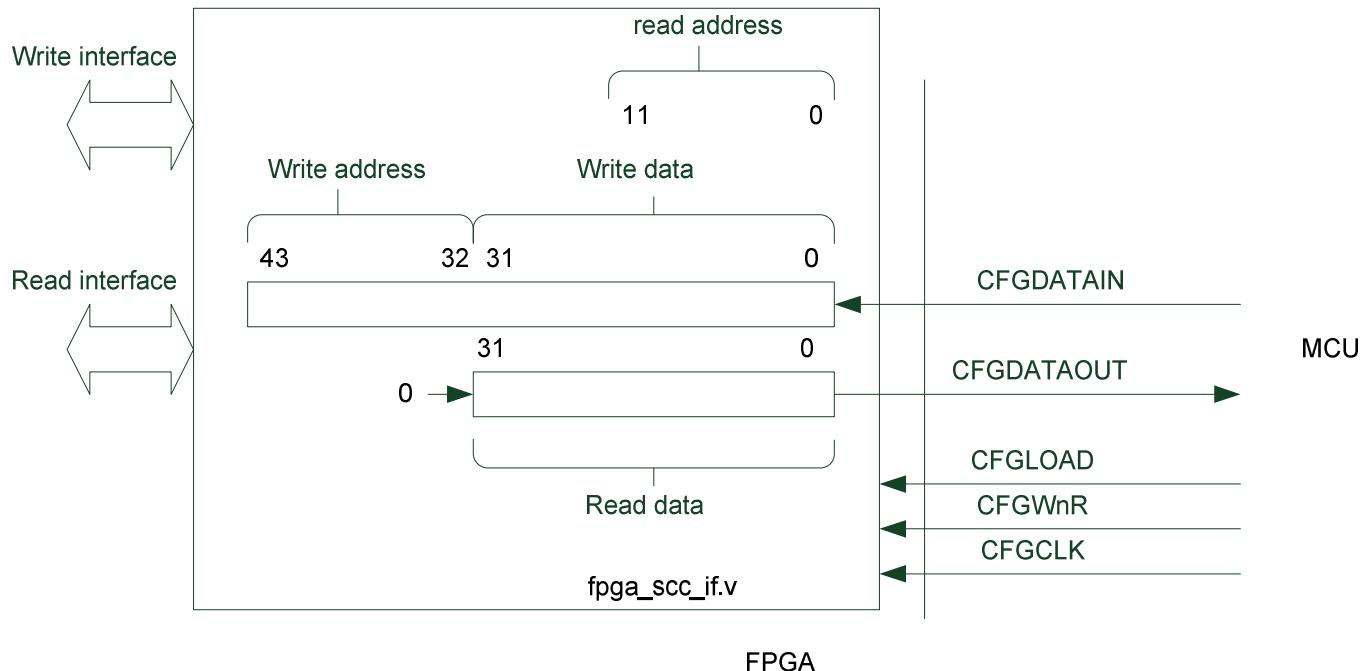
Figure 4-1 : Diagram of the SCC Interface

The read-addresses and write-addresses of the SCC interface do not use bits[1:0].
All address words are word-aligned.

Address	Name	Information
0x000	CFG_REG0	Bits[31:0] Reserved
0x004	CFG_REG1	Bits [31:8] Reserved Bits [7:0] MCC LEDs: 0 = OFF 1 = ON
0x008	CFG_REG2	Reserved
0x00C	CFG_REG3	Bits [31:8] Reserved Bits [7:0] MCC switches: 0 = OFF 1 = ON
0x010	CFG_REG4	Bits [31:4] Reserved Bits [3:0] : Board Revision
0x014	RESERVED	-
0x018	RESERVED	-
0x01C	RESERVED	-
0x020 – 0x09C	RESERVED	-
0x0A0	SYS_CFGDATA_RTN	32bit DATA [r/w]
0x0A4	SYS_CFGDATA_OUT	32bit DATA [r/w]

Address	Name	Information
0x0A8	SYS_CFGCTRL	Bit[31] : Start (generates interrupt on write to this bit)
		Bit[30] : R/W access
		Bits[29:26] : Reserved
		Bits[25:20] : Function value
		Bits[19:12] : Reserved
		Bits[11:0] : Device (value of 0/1/2 for supported clocks)
0x0AC	SYS_CFGSTAT	Bit 0 : Complete
		Bit 1 : Error
0x0AD – 0x0FC	RESERVED	-
0x100	SCC_DLL	DLL lock register
		Bits [31:24] DLL LOCK MASK[7:0] - These bits indicate if the DLL locked is masked.
		Bits [23:16] DLL LOCK MASK[7:0] - These bits indicate if the DLLs are locked or unlocked.
		Bits [15:1] : Reserved
		Bit[0] This bit indicates if all enabled DLLs are locked:
0x104 – 0xFF4	RESERVED	-
0xFF8	SCC_AID	SCC AID register is read only
		Bits[31:24] : FPGA build number
		Bits[23:20] : V2M-MPS2+ target board revision (A = 0, B = 1, C = 2)
		Bits[19:8] Reserved
		Bits[7:0] number of SCC configuration register
0xFFC	SCC_ID	SCC ID register is read only
		Bits[31:24] : Implementer ID: 0x41 = ARM
		Bits[23:20] : Reserved
		Bits[19:16] : IP Architecture: 0x4 =AHB
		Bits[15:4] : Primary part number: 505 = AN505
		Bits[3:0] : Reserved

Table 4-6 : SCC Register memory map

5 Clock architecture

The following tables list clocks entering and generated by the SMM.

5.1 Clocks

5.1.1 Source clocks

The following clocks are inputs to the system.

Clock	Input Pin	Frequency	Note
OSC0	OSCCLK[0]	40MHz	Core clock (x2)
OSC1	OSCCLK[1]	24.58MHz	Reference clock
OSC2	OSCCLK[2]	25MHz	Peripheral clock
DBGCLK	CS_TCK	Set by debugger	JTAG input
CFGCLK	CLCD_PDH[13]	Set by MCC	SCC register clock from MCC
SPICFGCLK	CLCD_PDL[6]	Set by MCC	SPI clock for memory access

Table 5-1 : Source clocks

5.1.2 Internal clocks

The following clocks are generated internally from the source clocks.

Clock	Source	Frequency	Note
MAINCLK	OSC0	20MHz	
AUDMCLK	OSC1	12.29MHz	
AUDSCLK	OSC1	3.07MHz	
DBGCLK	OSC0	20MHz	
SPICLCD	OSC2	25MHz	
SPICON	OSC2	25MHz	
I2CCLCD	OSC2	25MHz	
I2CAUD	OSC2	25MHz	
S32KCLK	OSC1	32kHz	
clk_100hz	OSC1	100Hz	
clk_zbtout	OSC0	20MHz	Phase shifted MAINCLK
traceclk	OSC0	20MHz	

Table 5-2 : Generated internal clocks

5.1.3 Clock outputs

The following clocks are generated internally and are output from the FPGA.

Clock	Output Port	Frequency	Note
spiclcd	CLCD_T_SCK	kHz	Software Configured
spicon	SPI_SCK	kHz	Software Configured
i2cclcd	CLCD_T_SCL	kHz	Software Generated
i2caud	AUD_SCL	kHz	Software Generated
i2c_shield0	EXP[5]	kHz	Software Generated
i2c_shield1	EXP[31]	kHz	Software Generated
spi_shield0	EXP[11]	kHz	Software Configured
spi_shield1	EXP[44]	kHz	Software Configured
spi_adc	EXP[19]	kHz	Software Configured
traceclk	CS_TRACECLK	20MHz	
clk_zbtout	SSRAM1_CLK[0]	20MHz	
clk_zbtout	SSRAM1_CLK[1]	20MHz	
clk_zbtout	SSRAM2_CLK	20MHz	
clk_zbtout	SSRAM3_CLK	20MHz	

Table 5-3 : Generated external clocks

5.1.4 Clocks connecting to the IoT Kit

The following clocks connect to the IoT kit. There are both clocks provided to the IoT kit and clocks generated by it.

Clock	Source / Direction	Frequency	Note
MAINCLK	OSC0	20MHz	Main Clock Input
SYSCLK	Output	20MHz	Main System Clock
S32KCLK	S32KCLK	32kHz	Asynchronous 32KHz clock input
TRACECLK	Output	20MHz	TPIU trace port clock
SWCLKTCK	DBGCLK	20MHz	SW/JTAG DP clock
TRACECLKIN	traceclk	20MHz	TPIU trace port clock input

Table 5-4 : IoT Kit clocks

6 FPGA Secure Privilege Control

The IoT Kit Subsystem's Secure Privilege Control and Non-secure Privilege Block is able to provides expansion security control signals to control the various security gating units within the subsystem. The following table lists the connectivity of system security extension signal. More details are available in *Cortex-M33 ARMv8-M IoT Kit VFP User Guide* (ARM-ECM-0601256).

Components Name	Components signals	Security Expansion Signals
DMA 0 MSC	msc_irq	S_MSCEXP_STATUS[0]
	msc_irq_clear	S_MSCEXP_CLEAR[0]
	cfg_nonsec	NS_MSCEXP[0]
DMA 1 MSC	msc_irq	S_MSCEXP_STATUS[1]
	msc_irq_clear	S_MSCEXP_CLEAR[1]
	cfg_nonsec	NS_MSCEXP[1]
DMA 2 MSC	msc_irq	S_MSCEXP_STATUS[2]
	msc_irq_clear	S_MSCEXP_CLEAR[2]
	cfg_nonsec	NS_MSCEXP[2]
DMA 3 MSC	msc_irq	S_MSCEXP_STATUS[3]
	msc_irq_clear	S_MSCEXP_CLEAR[3]
	cfg_nonsec	NS_MSCEXP[3]
APB PPC EXP 0	apb_ppc_irq	S_APBPPCEXP_STATUS[0]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[0]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP0[15:0]
	cfg_ap	APB_P_PPCEXP0[15:0]
APB PPC EXP 1	apb_ppc_irq	S_APBPPCEXP_STATUS[1]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[1]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP1[15:0]
	cfg_ap	APB_P_PPCEXP1[15:0]
APB PPC EXP 2	apb_ppc_irq	S_APBPPCEXP_STATUS[2]
	apb_ppc_clear	S_APBPPCEXP_CLEAR[2]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	APB_NS_PPCEXP2[15:0]
	cfg_ap	APB_P_PPCEXP2[15:0]
AHB PPC EXP 0	ahb_ppc_irq	S_AHBPPCEXP_STATUS[0]
	ahb_ppc_clear	S_AHBPPCEXP_CLEAR[0]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	AHB_NS_PPCEXP0[15:0]
	chg_ap	AHB_P_PPCEXP0[15:0]
AHB PPC EXP 1	ahb_ppc_irq	S_AHBPPCEXP_STATUS[1]

Components Name	Components signals	Security Expansion Signals
	ahb_ppc_clear	S_AHBPPCEXP_CLEAR[1]
	cfg_sec_resp	SEC_RESP_CFG
	cfg_non_sec	AHB_NS_PPCEXP1[15:0]
	chg_ap	AHB_P_PPCEXP1[15:0]
MPC SSRAM0	secure_error_irq	S_MPCEXP_STATUS[0]
MPC SSRAM1	secure_error_irq	S_MPCEXP_STATUS[1]
MPC SSRAM2	secure_error_irq	S_MPCEXP_STATUS[2]

Table 6-1 : Security Expansion signals connectivity.

The following table lists the peripherals that are controlled by APB PPC EXP 0. Each APB <n> interface is controlled by APB_NS_PPCEXP0[n] and APB_P_PPCEXP0[n].

APB PPC EXP 0 Interface Number <n>	Name
0	SSRAM1 Memory Protection Controller (MPC)
1	SSRAM2 Memory Protection Controller (MPC)
2	SSRAM3 Memory Protection Controller (MPC)
15:3	Reserved

Table 6-2 : Peripherals Mapping of APB PPC EXP 0

The following table lists the peripherals that are controlled by APB PPC EXP 1. Each APB <n> interface is controlled by APB_NS_PPCEXP1[n] and APB_P_PPCEXP1[n].

APB PPC EXP 1 Interface Number <n>	Name
0	SPI_0
1	SPI_1
2	SPI_2
3	SPI_3
4	SPI_4
5	UART_0
6	UART_1
7	UART_2
8	UART_3
9	UART_4
10	I2C_0
11	I2C_1
12	I2C_2
13	I2C_3
15:14	Reserved

Table 6-3 : Peripherals Mapping of APB PPC EXP 1

The following table lists the peripherals that are controlled by APB PPC EXP 2. Each APB <n> interface is controlled by APB_NS_PPCEXP2[n] and APB_P_PPCEXP2[n].

APB PPC EXP 0 Interface Number <n>	Name
0	SCC
1	AUDIO
2	FPGAIO
15:3	Reserved

Table 6-4 : Peripherals Mapping of APB PPC EXP 2

The following table lists the peripherals that are controlled by AHB PPC EXP 0. Each APB <n> interface is controlled by AHB_NS_PPCEXP0[n] and AHB_P_PPCEXP0[n].

AHB PPC EXP 0 Interface Number <n>	Name
0	VGA
1	GPIO_0
2	GPIO_1
3	GPIO_2
4	GPIO_3
15:5	Reserved

Table 6-5 : Peripherals Mapping of AHB PPC EXP 0

The following table lists the peripherals that are controlled by AHB PPC EXP 1. Each APB <n> interface is controlled by AHB_NS_PPCEXP1[n] and AHB_P_PPCEXP0[n].

AHB PPC EXP 0 Interface Number <n>	Name
0	DMA_0
1	DMA_1
2	DMA_2
3	DMA_3
15:4	Reserved

Table 6-6 : Peripherals Mapping of AHB PPC EXP1

The following table lists the Master Security Controllers (MSCs) that are controlled by NS_MSCEXP signals. These control signals are used to map each peripheral connected to their associated MSCs as Secure or Non-Secure Masters.

NS_MSCEXP bits	Name
0	MSC cfg_nonsec for DMA0
1	MSC cfg_nonsec for DMA1
2	MSC cfg_nonsec for DMA2
3	MSC cfg_nonsec for DMA3
15:4	Reserved

Table 6-7 : Peripherals Mapping of AHB PPC EXP1

7 Interrupt Map

The Interrupts in the FPGA subsystem extend the IoT Kit Interrupt map by adding to the expansion area as follows:

Interrupt Input	Interrupt Source
NMI	Combined Secure Watchdog, S32K Watchdog and NMI_Expansion
IRQ[0]	Non-Secure Watchdog Reset Request
IRQ[1]	Non-Secure Watchdog Interrupt
IRQ[2]	S32K Timer
IRQ[3]	Timer 0
IRQ[4]	Timer 1
IRQ[5]	Dual Timer
IRQ[8:6]	Reserved
IRQ[9]	MPC Combined (Secure)
IRQ[10]	PPC Combined (Secure)
IRQ[11]	MSC Combined (Secure)
IRQ[12]	Bridge Error Combined Interrupt (Secure)
IRQ[31:13]	Reserved
IRQ[32]	UART 0 Receive Interrupt
IRQ[33]	UART 0 Transmit Interrupt
IRQ[34]	UART 1 Receive Interrupt
IRQ[35]	UART 1 Transmit Interrupt
IRQ[36]	UART 2 Receive Interrupt
IRQ[37]	UART 2 Transmit Interrupt
IRQ[38]	UART 3 Receive Interrupt
IRQ[39]	UART 3 Transmit Interrupt
IRQ[40]	UART 4 Receive Interrupt
IRQ[41]	UART 4 Transmit Interrupt
IRQ[42]	UART 0 Combined Interrupt
IRQ[43]	UART 1 Combined Interrupt
IRQ[44]	UART 2 Combined Interrupt
IRQ[45]	UART 3 Combined Interrupt
IRQ[46]	UART 4 Combined Interrupt
IRQ[47]	UART Overflow (0, 1, 2, 3 & 4)
IRQ[48]	Ethernet
IRQ[49]	Audio I2S
IRQ[50]	Touch Screen
IRQ[51]	SPI #0 (SPI Header)
IRQ[52]	SPI #1 (CLCD)
IRQ[53]	SPI #2 (Shield ADC)
IRQ[54]	SPI #3 (Shield 0 SPI)

IRQ[55]	SPI #4 (Shield 1 SPI)
IRQ[56]	DMA #0 Error Interrupt Request
IRQ[57]	DMA #0 Terminal Count Interrupt Request
IRQ[58]	DMA #0 Combined Interrupt Request
IRQ[59]	DMA #1 Error Interrupt Request
IRQ[60]	DMA #1 Terminal Count Interrupt Request
IRQ[61]	DMA #1 Combined Interrupt Request
IRQ[62]	DMA #2 Error Interrupt Request
IRQ[63]	DMA #2 Terminal Count Interrupt Request
IRQ[64]	DMA #2 Combined Interrupt Request
IRQ[65]	DMA #3 Error Interrupt Request
IRQ[66]	DMA #3 Terminal Count Interrupt Request
IRQ[67]	DMA #3 Combined Interrupt Request
IRQ[68]	GPIO 0 Combined Interrupt
IRQ[69]	GPIO 1 Combined Interrupt
IRQ[70]	GPIO 2 Combined Interrupt
IRQ[71]	GPIO 3 Combined Interrupt
IRQ[87:72]	GPIO 0 individual interrupts
IRQ[103:88]	GPIO 1 individual interrupts
IRQ[119:104]	GPIO 2 individual interrupts
IRQ[123:120]	GPIO 3 individual interrupts

Table 7-1 : FPGA Expansion Interrupt Map.

7.1 UARTS Interrupts

There are five CMSDK UARTs in the system, and each has the following interrupt pins:

- TXINT

- RXINT

- TXOVRINT

- EXOVRINT

- UARTINT

The TXINT, RXINT and UARTINT interrupt signal of each UART drive a single interrupt input of the M33 CPU. In addition, The TXOVERINT and EXOVRINT interrupt signals of all five UARTs, ten signals in all, are logically ORed together to drive IRQ[47].

8 Shield Support

This SMM can support up to two external shield devices with the addition of the ARM V2C-SHIELD (HBI-0289) expansion board to the V2M-MPS2+. To enable the Shield support, three SPI, three UART and two I2C interfaces are multiplexed with GPIO over the Expansion Headers.
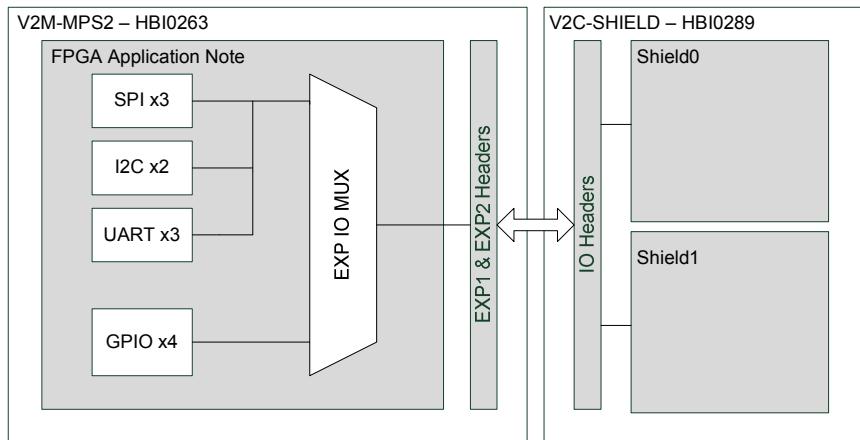

Figure 8-1 : Shield Device Expansion

Multiplexing is controlled by the alternative function output from the associated GPIO Register.

EXP Signal	GPIO Source Port	Alternative Function	Description
EXP[0]	IPO GPIO0 [0]	UART3 RXD	Shield0 UART Receive
EXP[4]	IPO GPIO0 [4]	UART3 TXD	Shield0 UART Transmit
EXP[5]	IPO GPIO0 [5]	SBCON2 SCL	Shield0 I2C Clock
EXP[15]	IPO GPIO0 [15]	SBCON2 SDA	Shield0 I2C Data
EXP[11]	IPO GPIO0 [11]	SPI3 SCK	Shield0 SPI Clock
EXP[12]	IPO GPIO0 [12]	SPI3 SS	Shield0 SPI Chip Select
EXP[13]	IPO GPIO0 [13]	SPI3 MOSI	Shield0 SPI Data Out
EXP[14]	IPO GPIO0 [14]	SPI3 MISO	Shield0 SPI Data In
EXP[26]	IPO GPIO1 [10]	UART4 RXD	Shield1 UART Receive
EXP[30]	IPO GPIO1 [14]	UART4 TXD	Shield1 UART Transmit
EXP[31]	IPO GPIO1 [15]	SBCON3 SCL	Shield1 I2C Clock
EXP[41]	AHB GPIO2 [9]	SBCON3 SDA	Shield1 I2C Data
EXP[38]	AHB GPIO2 [6]	SPI4 SS	Shield1 SPI Chip Select
EXP[39]	AHB GPIO2 7]	SPI4 MOSI	Shield1 SPI Data Out
EXP[40]	AHB GPIO2 [8]	SPI4 MISO	Shield1 SPI Data In
EXP[44]	AHB GPIO2 [12]	SPI4 SCK	Shield1 SPI Clock
EXP[16]	IPO GPIO1 [0]	SPI2 SS	ADC SPI Chip Select
EXP[17]	IPO GPIO1 [1]	SPI2 MISO	ADC SPI Data In
EXP[18]	IPO GPIO1 [2]	SPI2 MOSI	ADC SPI Data Out
EXP[19]	IPO GPIO1 [3]	SPI2 SCK	ADC SPI Clock
EXP[21]	IPO GPIO1 [5]	-	User button 0
EXP[22]	IPO GPIO1 [6]	-	User button 1

Table 8-1 : Shield Alternative Function Pinout

9 Configurations

9.1 IoT subsystem

The IoT subsystem has a number of configurable options. These are listed below.

Parameter	Implemented Values	Default Values	Description
INITSVTOR0_RST [31:0]	0x1000_0000	0x1000_0000	Reset Value of the Secure Vector table offset address register in the System Control Register.
INITNSVTOR0 [31:0]	0x0000_0000	0x0000_0000	Reset Value of the Non-Secure Vector table offset address at the M33 CPU Core.
CPU0WAIT_RST	1	0	CPU wait at boot '0' boot normally, '1' wait at boot. The MCC controller releases CPU0WAIT by writing to a register after use code is loaded to system memory at startup.
EXP_NUMIRQ	92	64	Specifies the number of expansion interrupt. This therefore means that the M33 NVIC has 92+32 = 124 interrupts.
EXP_IRQ_DIS_0 [EXP_NUMIRQ-1:0]	All set to low.	All set to high.	Disables support for individual expansion interrupts on Primary CPU Core, allowing a range of non-contiguous interrupts IRQDIS[i] = 1'b1 indicates that IRQ[i] is not present
EXP_SYS_ID_PRESENT [31:16]	0xFFFF	0xFFFF	Each bit n of this vector defines if an AHB Master with HMASTERID = n exist in the system. Bit 15 down to 0 are all IDs reserved for internal use and not available on this interface.
CPU0_FPU	1	1	Floating Point Unit (FPU) is present on the M33 CPU
CPU0_DSP	1	1	Digital Signal Processing (DSP) extension instructions are included on the M33 CPU.
CPU0_MPU_NS	8	8	Number of Non-Secure MPU entries on the M33 CPU
CPU0_MPU_S	8	8	Number of Secure MPU entries on the M33 CPU
CPU0_SAU	8	8	Number of SAU entries on the M33 CPU
CPU0_IRQ_LVL	4	4	Number of interrupt priority implemented in the NVIC, equal to $2^{CPU0\_IRQ\_LVL}$. Supports 3 to 8 bits. Currently at 4 which therefore provides 16 levels of interrupt priority.

Table 9-1 : Top Level User Configurable Parameters

9.2 DAP

The IoT kit DAP has had the following setting modified from the supplied default.

Parameter	Implemented Values	Default Values	Description
DPSEL	2	0	Debug port select: 0 JTAG-DP, 1 SW-DP, 2 SWJ-DP.
TARGETID	0x 7F15_FCFF	0x0000_0001	The TARGETID uniquely identifies the designer of the SoC and contains a part number to identify the SoC.
JEPID	0x02	0x0	This 7-bit value is your JEDEC JEP-106 identity code value.
JEPCONT	0xE	0x0	This 4-bit value is your JEDEC JEP-106 continuation code value.
PARTNUM	0x5AE	0x0	This 12-bit value is a part number that identifies your system.

Table 9-2 : Top Level User Configurable Parameters

9.3 M33

Refer to document ARM-ECM-0601256 – Cortex-M33 ARMv8-M IoT Kit VFP User Guide, section 3.4, CPU Element, for parameters used in IoT kit to configure the Cortex-M33 CPU core.