# Delay Wrapper Register Requiring Only One Register and One Scan Enable

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Testing a device at-speed has become a necessity in very deep sub-micron (VDSM) devices. There are two popular ways to test a device at the top functional speed. The first way is with functional patterns. It is very difficult to apply functional patterns to an embedded core as all of the ports must be available at the chip level or extra test infrastructure must be added. The second way is to use structural (scan) tests. With a combination of transition delay and path delay testing, the delay test coverage can be much higher than with functional tests.

Delay testing with structural test requires a data pair (1-0 or 0-1) to be applied to a node. The data pair is input at the functional speed allowing the structural pattern to detect gross delay defects and even determine the frequency of a device. In order to input the data pair in through a functional path, a combinational depth of two is required (see Figure 1). Figure 1 illustrates a node that will have a data pair applied to it for a delay test. A 1 is shifted into register A and a 0 is shifted into register B. Then the shift path is disabled and the functional path is enabled. Two clocks are applied and a 0-1 transition occurs, through the combinational logic, on the node under test.

Figure 1 Node Under Delay Test
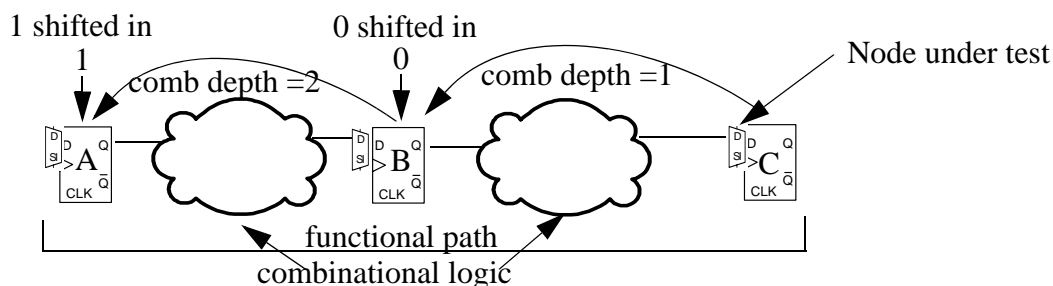
When a wrapper is employed, the input paths on a core are incapable of getting a data pair, since there is no register behind the wrapper register. A wrapper register is employed in place of a functional port during core test. The functional ports are not accessible during the test of a core. This means the highest combinational depth that can occur on these paths is one. In Figure 2, during the first functional clock, a 0 can be input into the node under test. However, since the D input of the wrapper cell is connected to an input port which is not utilized during core test, only an X can occur on the second functional clock.

Figure 2 Input Path Under Delay Test
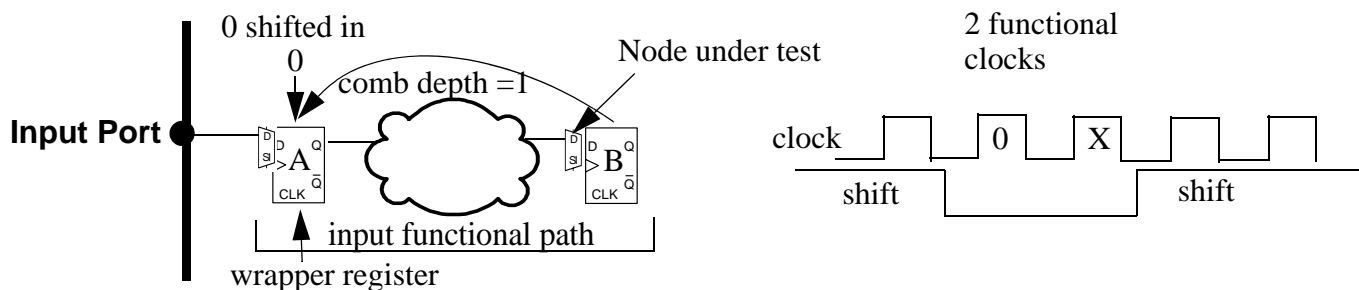
The X generation can be prevented by adding a second, test-only, wrapper register cell shown in Figure

3. The D port on register C is connected to the output of the previous wrapper register. This configuration does not require an extra wrapper scan enable, but it can only provide two bits of data. More may be needed for logic that is more difficult to test.

Figure 3 Dedicated Register for Data Pair Generation
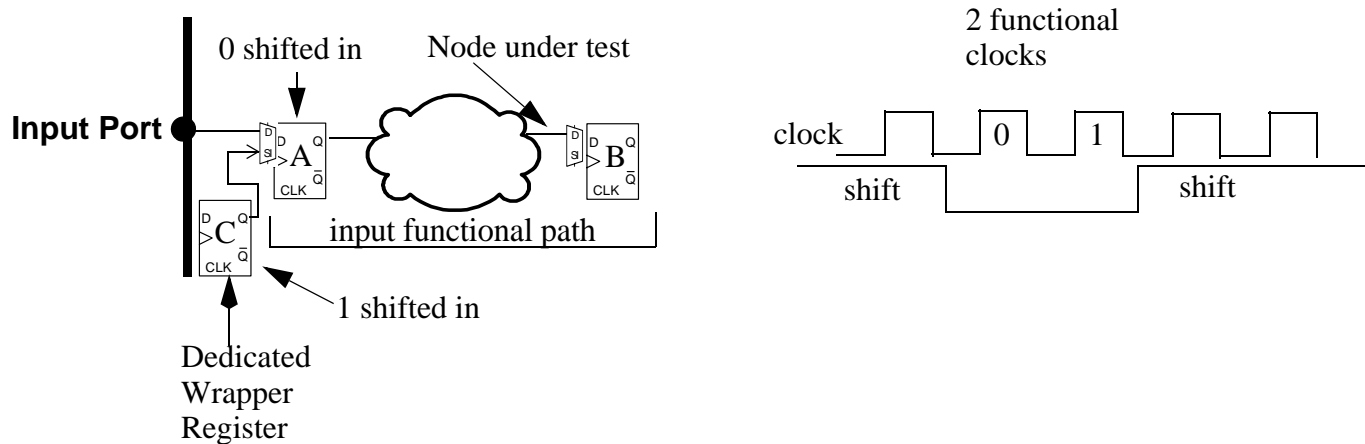
ARM cores do not add the dedicated wrapper cell to get delay coverage of the input paths. Instead this issue is addressed, on many ARM cores, by utilizing two wrapper scan enables that are separate from the core scan enable. One wrapper scan enable controls the input wrapper cells and one controls the output wrapper cells. The input wrapper scan enable (WSEI) allows us to do delay testing of the initial logic (before the first flip-flop) of a core without having two wrapper cells per input. This is done during internal test mode by holding the WSEI enabled (in shift mode). It also makes sure the wrapper cell is not an X generator when testing with deeper combinational depth such as through a memory. It allows many clocks of deterministic data to be input into the core input logic. For delay testing, this allows a data pair to be input to the first path using a single wrapper cell per port as is illustrated in Figure 4. Since WSEI is held active high, register A is able to supply the second half of the data pair through the SI port of register B. WSEO toggles with SE during internal testing as it must capture data into the output wrapper cells. Input wrapper registers do not need to capture data during the internal test mode, but the output wrapper registers must be able to capture data for full coverage. During the test of the external logic, WSEO and WSEI switch functions as the input wrapper registers capture data from the external logic and the output wrapper registers control data to the external logic. During external test mode, WSEO would be held active high (in shift mode) in order to provide data pairs to the logic external to the core.

There is a way to get the same type of behavior using a single scan enable (WSE) in conjunction with the WINTEST and WEXTEST signals. WINTEST indicates that the core wrapper is in internal test mode. WEXTEST indicates that the core wrapper is in external test mode. These two signals are utilized for dedicated wrapper registers on ARM cores shown in Figure 5. With this methodology, these ports would have to be added even for a wrapper with only shared wrapper registers. A shared wrapper register is a functional register that is reused as a wrapper register.

Figure 4 Input Path Under Delay Test with Input Wrapper Cells in Shift Mode
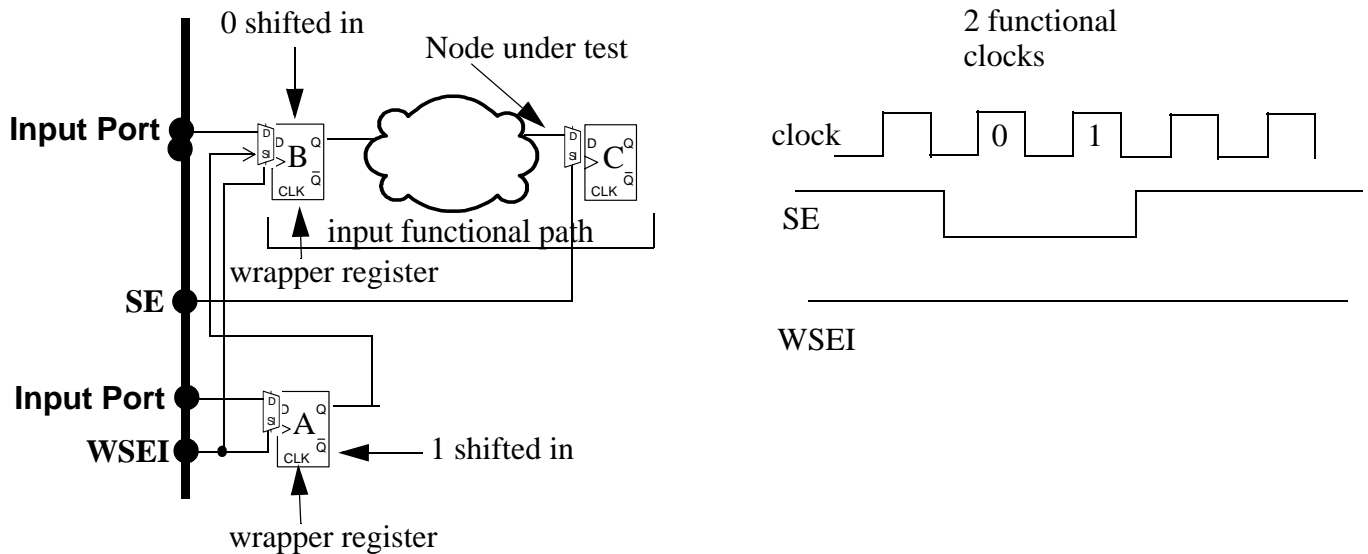
Note that the input and output wrapper cells in Figure 5 have different scan enable signals (WSEI and WSEO).

Figure 5 Example Dedicated Input and Output Wrapper Cells
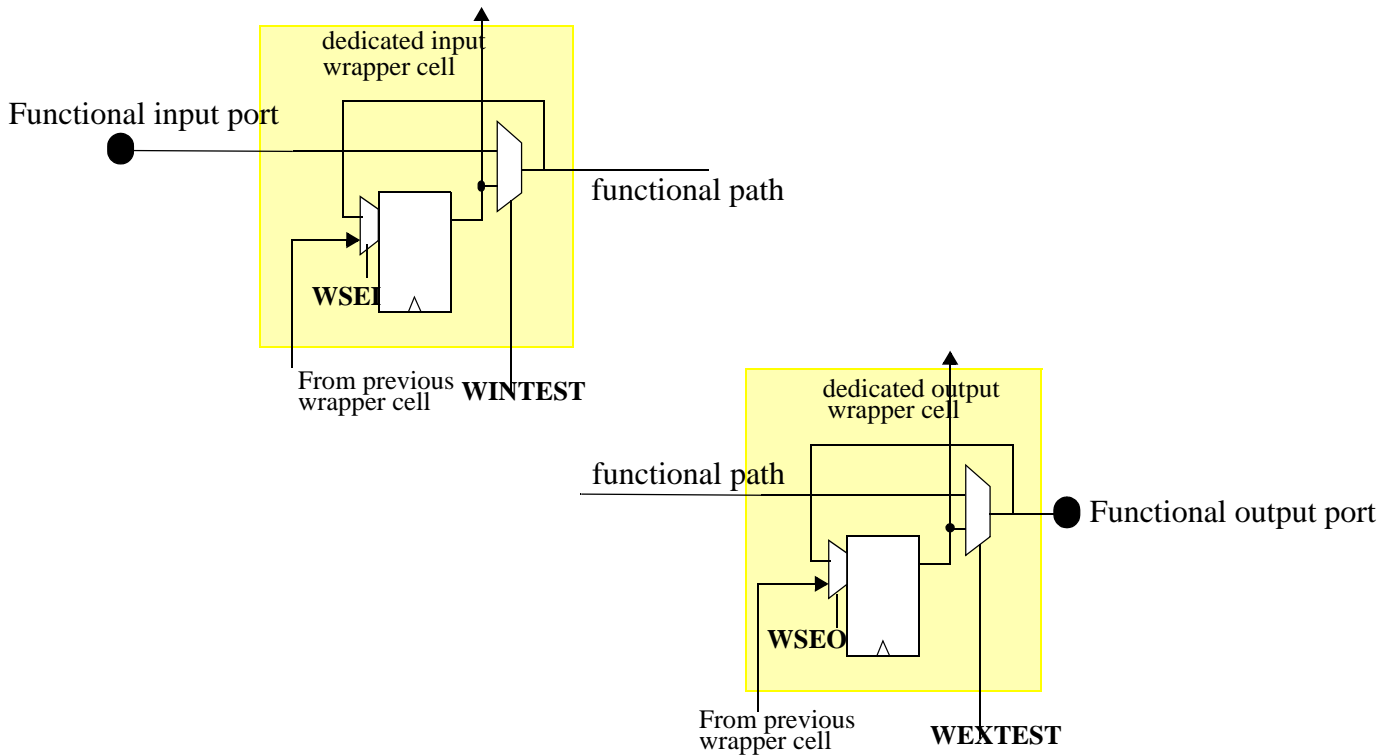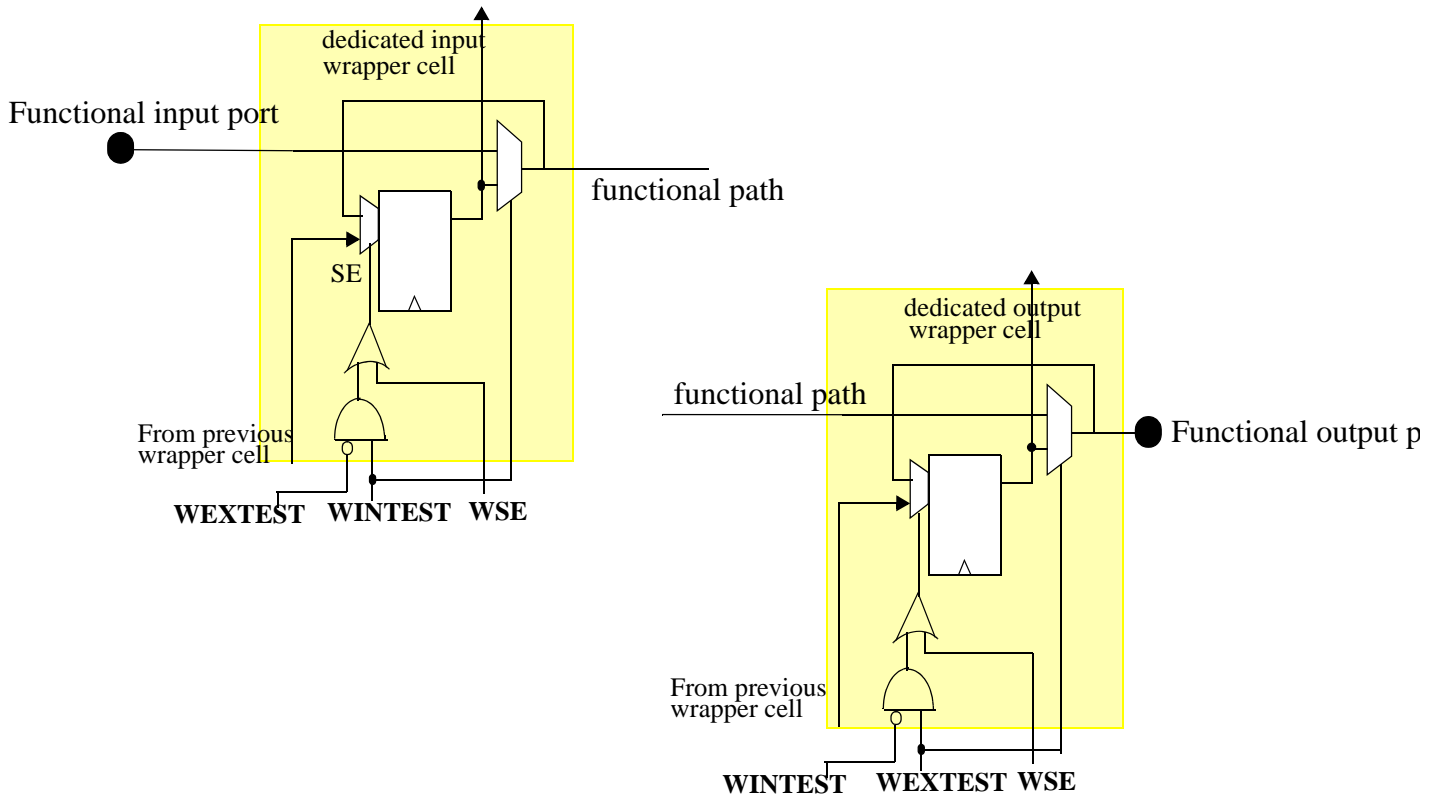

Figure 6 shows how the dedicated wrapper registers would be modified to allow for only one external wrapper scan enable and still have the capability to deliver data pairs to the core logic.

Figure 6 New Proposed Dedicated Wrapper Cells

As can be seen, while in INTEST mode (WINTEST=1 and WEXTEST=0), the input wrapper cell is forced to stay in shift mode allowing data pairs to be shifted through the wrapper chain and applied to internal paths without holding the WSE enabled. While in EXTEST mode (WEXTEST=1 and WINTEST=0), the output wrapper cell is forced to stay in shift mode allowing data pairs to be shifted through the wrapper chain and applied to external logic without holding the WSE enabled.

The same type of logic would be added to a shared wrapper register. Figure 7 shows an example shared wrapper register, which is simply a functional register with either WSEO or WSEI attached to the scan enable port of the flip-flop.

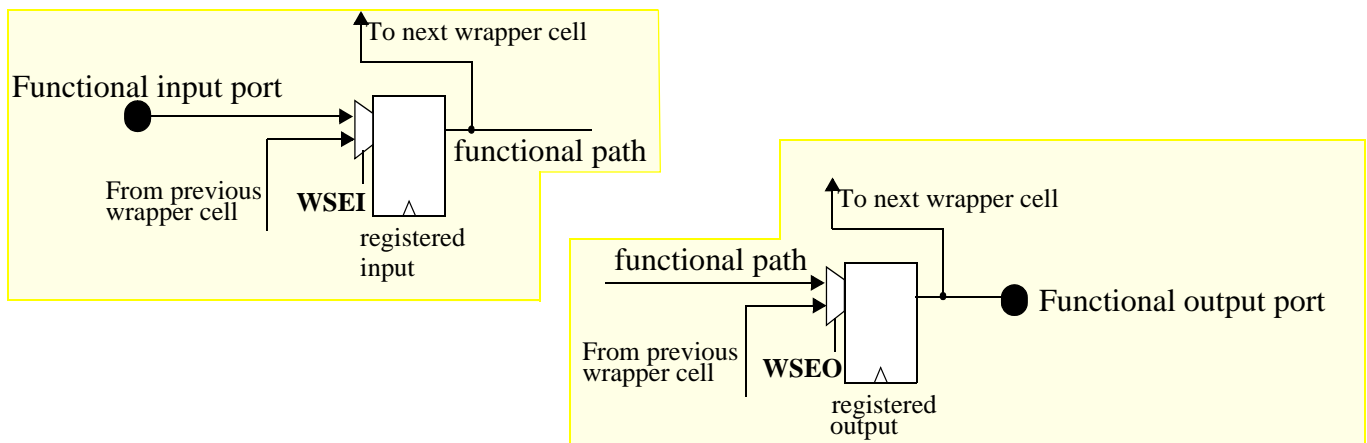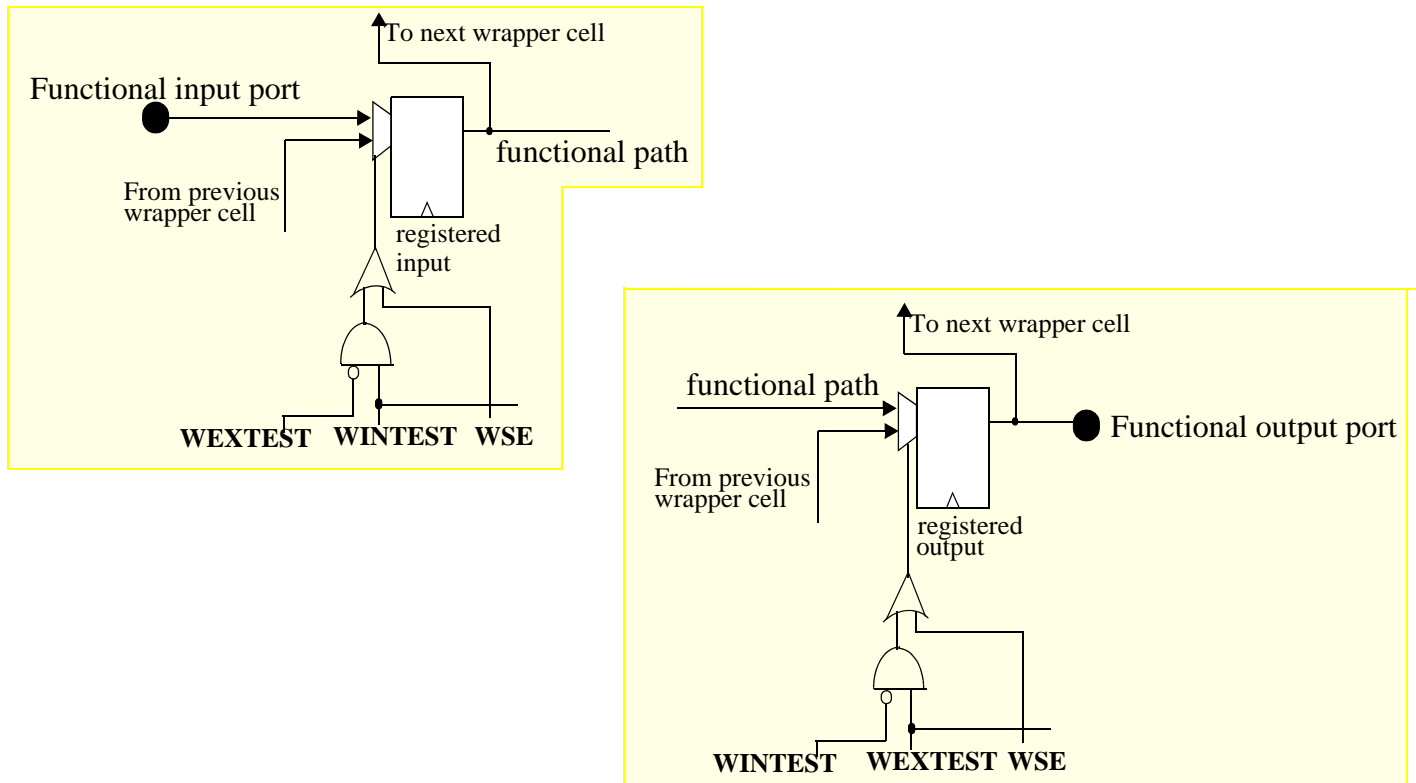**Figure 7 Current Shared Wrapper Cells**

Figure 8 shows how these shared wrapper cells would be modified to allow for a single wrapper scan enable, but still deliver data pairs to initial input paths.

Figure 8 Single Wrapper Scan Enable Solution

The extra logic does not have to be in each wrapper register. It can be created once for the input wrapper registers and once for the output wrapper registers. The output of these logic blocks can be routed, just like a scan enable (i.e. WSEI/WSEO) to the wrapper registers. This would enable only one wire to be routed to each wrapper register. However, this still means that two different scan enable signals would have to be connected - one to the input wrapper registers and one to the output wrapper registers. Figure 9 shows an example of how this would be done for the output wrapper registers.

Figure 9 WSEO Logic Connection
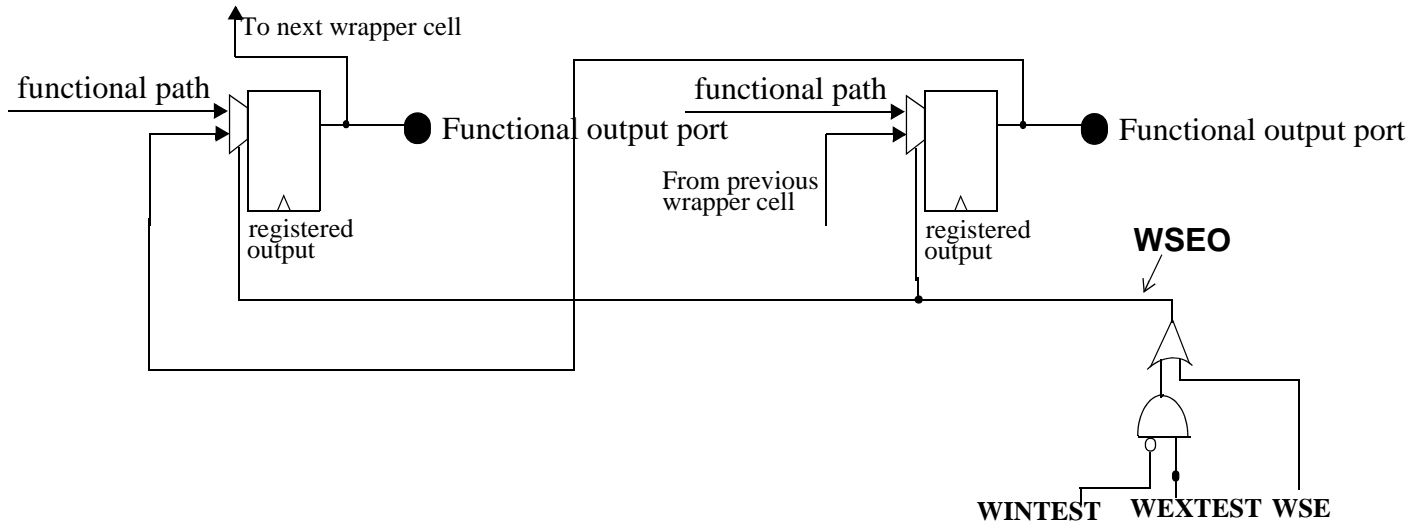
The ideas outlined in this paper resolve the X generation issue using a wrapper without having multiple wrapper registers per port. In addition, the design can be revised to have only one external wrapper scan enable port and still resolve the X generation issue. Having a single wrapper scan enable makes utilization of this core easier for implementers of the core.