ARM® LogicTile Express 3MG

V2F-1XV5

Technical Reference Manual

ARM®

DUI0449G (ID052215)

ARM LogicTile Express 3MG
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
27 November 2009	A	Non-Confidential	First release
06 August 2010	B	Non-Confidential	Second release
15 October 2010	C	Non-Confidential	Third release
28 March 2011	D	Non-Confidential	Fourth release
22 June 2012	E	Non-Confidential	Fifth release
28 May 2014	F	Non-Confidential	Sixth release
25 May 2015	G	Non-Confidential	Seventh release

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110 Fulbourn Road, Cambridge, England CB1 9NJ.

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The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

The system should be powered down when not in use.

The LogicTile Express 3MG generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the card.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

Contents
ARM LogicTile Express 3MG Technical Reference Manual

Preface

This *Technical Reference Manual* (TRM) is for the *LogicTile Express 3MG*. It contains the following sections:

About this book

This book is for LogicTile Express 3MG, V2F-1XV5, daughterboard.

Intended audience

This book is written for experienced hardware and software engineers who are developing ARM-based products using the daughterboard as part of a Versatile™ Express development platform.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the LogicTile Express 3MG board.

Appendix A *Signal Descriptions*

Read this for a description of the signals present at the external interface connectors of the daughterboard.

Appendix B *Specifications*

Read this for the electrical and timing specifications of the daughterboard.

Appendix C *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary* `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Typographical Conventions

Conventions that this book can use are described in:

- *Typographical*
- *Timing diagrams* on page ix
- *Signals* on page ix.

Typographical

The typographical conventions are:

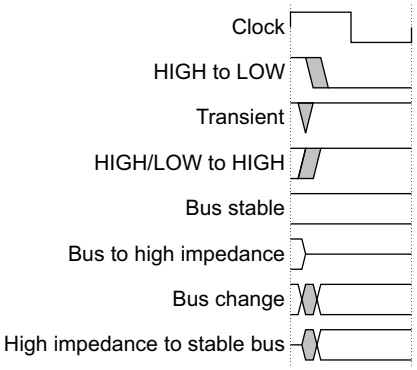
italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
< and >	Enclose replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter http://infocenter.arm.com, for access to ARM documentation.

See onARM http://onarm.com, for embedded software development resources including the *Cortex® Microcontroller Software Interface Standard* (CMSIS).

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Application Note AN224. Example LogicTile Express 3MG design for a Core Tile Express A9x4*
- *ARM® Motherboard Express µATX Technical Reference Manual* (ARM DUI 0447)
- *ARM® Versatile™ Express Configuration Technical Reference Manual* (ARM DDI 0496)
- *ARM® CoreTile Express A9x4 Technical Reference Manual* (ARM DUI 0448)
- *ARM® CoreTile Express A5x2 Technical Reference Manual* (ARM DUI 0541)
- *ARM® CoreTile Express A15x2 Technical Reference Manual* (ARM DUI 0604)
- *ARM® Versatile™ Express Boot Monitor Reference Manual* (ARM DUI 0465).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- the title
- the number, DUI0449G
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter introduces the LogicTile Express 3MG daughterboard. It contains the following sections:

1.1 Precautions

This section contains advice about how to prevent damage to your daughterboard.

1.1.1 Ensuring safety

The daughterboard is powered from a 3V3 DC and a 5V DC supply. Power is supplied to the daughterboard through the header HDRY connectors.

Warning

Do not use the daughterboard near equipment that is sensitive to electromagnetic emissions, for example medical equipment.

1.1.2 Preventing damage

The daughterboard is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure and this leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the board, observe the following precautions:

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Ensure that the voltage on the pins of the FPGA and interface circuitry on the daughterboard is at the correct level. Some of the daughterboard FPGA signals are connected directly to the Versatile Express µATX Motherboard.
- FPGA pins connected to an external signal source must not be configured as outputs.
- Do not use the board near a transmitter of electromagnetic emissions.

1.2 About the LogicTile Express 3MG daughterboard

The daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA®) that use the *Advanced eXtensible Interface* (AXI™) or custom logic for use with ARM cores.

Note

The daughterboard is designed only to be used with a Versatile Express µATX Motherboard.

The daughterboard contains the following devices:

- Xilinx Virtex-5 XC5VLX330T FPGA:
  - Speed-grade -1.
- 256MB of Flash memory for FPGA images.
- 16MB of on-board ZBT RAM.
- HDRX header with two *High-Speed Buses* (HSBs) that connects to the other daughterboard site.
- HDRY header with five buses to the motherboard.
- *Serial Advanced Technology Attachment* (SATA) connectors.
- JTAG and Trace debug interfaces.
- Eight general-purpose *Dual In-line Package* (DIP) switches.
- Eight status and user LEDs.
- Daughterboard Configuration Controller.

Figure 1-1 on page 1-4 shows the layout of the daughterboard.

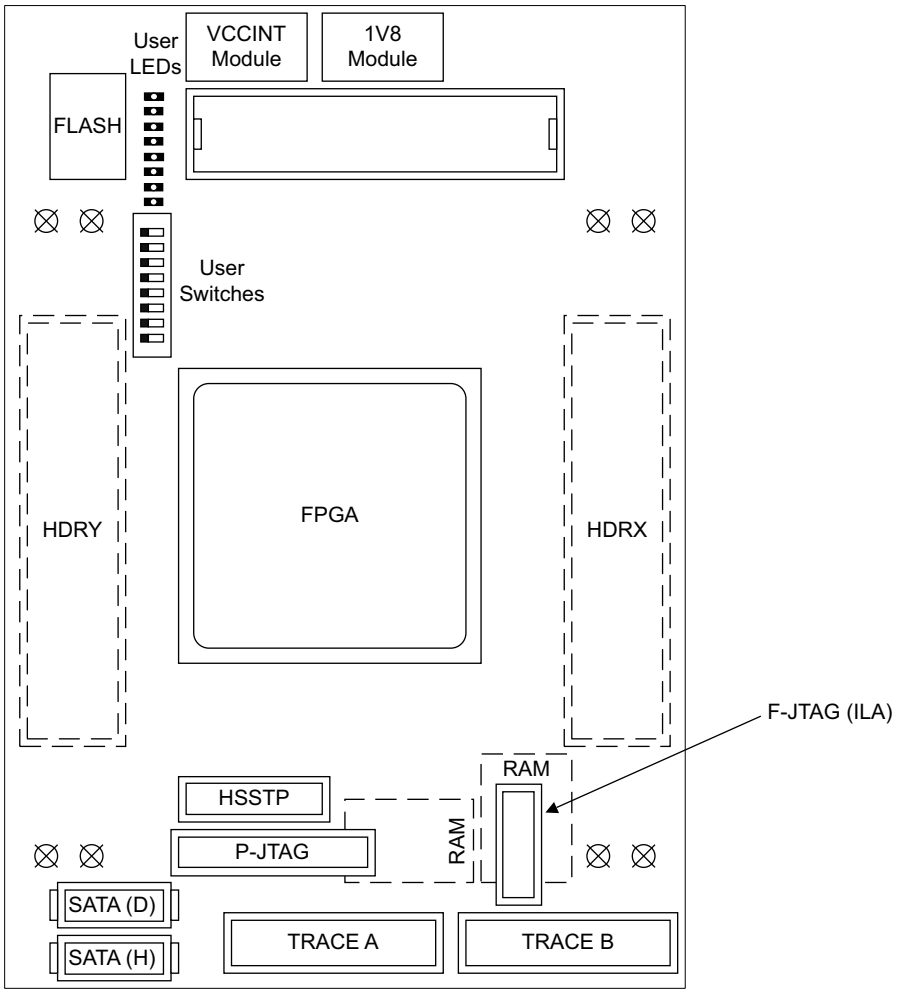


Figure 1-1 Daughterboard layout

Chapter 2
Hardware Description

This chapter describes the LogicTile Express 3MG daughterboard hardware. It contains the following sections:

2.1 Overview of the daughterboard hardware

Figure 2-1 shows the high-level hardware infrastructure.

The hardware infrastructure supports system expansion and a number of debug interfaces. For information on the connector pinouts to these additional interfaces, see Appendix A *Signal Descriptions*.

Note

A configuration image loaded into the FPGA at power-up defines the functionality of the daughterboard. The Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4*, provided by ARM, implements an example AMBA system using the daughterboard. See the documentation supplied on the accompanying media and the *Application Notes* listing `http://infocenter.arm.com` for more information.

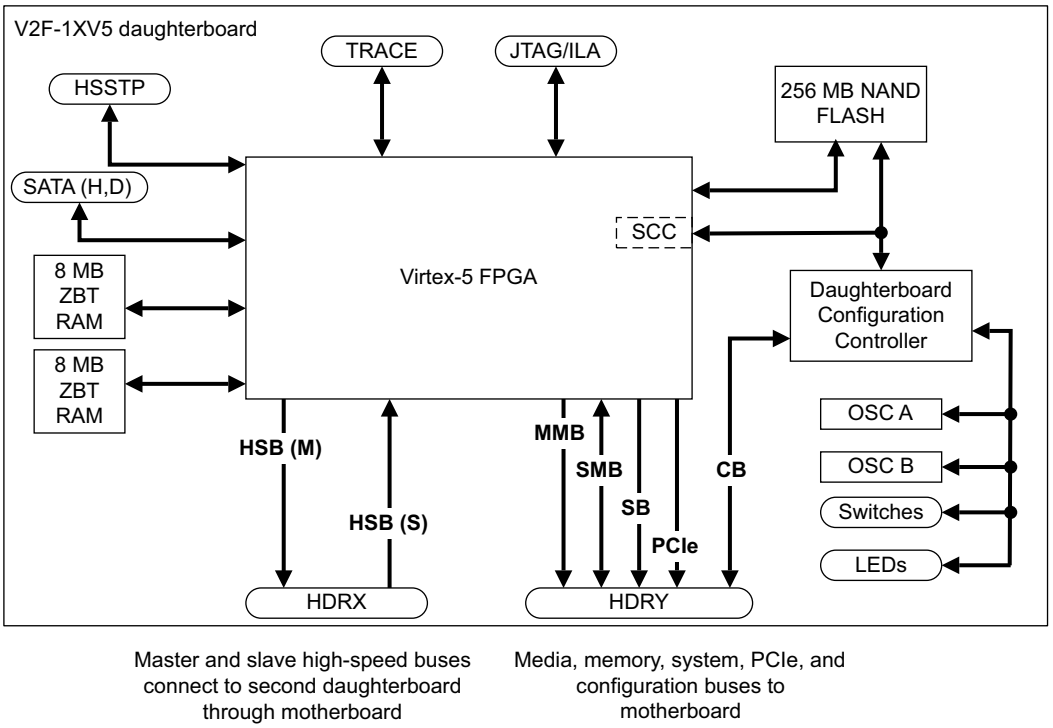


Figure 2-1 Hardware infrastructure

The hardware infrastructure of the daughterboard comprises:

- Single Xilinx Virtex-5 XC5VLX330T FPGA:
  - Up to 512KB of internal FPGA block RAM is available.
  - Speed-grade -1.
- 256MB of NAND Flash memory for FPGA images.
- 16MB of on-board ZBT RAM:
  - Two independent banks of 8MB are supported.
- Two *High-Speed Buses* (HSBs) routed to the HDRX header:
  - A high speed bus Master, M, interface.
  - A high speed bus Slave, S, interface.

  - *Low Voltage Differential Signaling* (LVDS) support.

- Motherboard interfaces routed to the HDRY header:
  - *Multi Media Bus* (MMB).
  - *PCI-Express Bus* (PCIe).
  - *System Bus* (SB).
  - *Static Memory Bus* (SMB).
  - *Configuration Bus* (CB).
- *Serial Advanced Technology Attachment* (SATA) connectors:
  - A Host, H, connector.
  - A Device, D, connector.
- Debug interfaces:
  - JTAG port for *RealView® ICE®* (RVI).
  - *Integrated Logic Analyzer* (ILA) port for *ChipScope™*.
  - Trace A and Trace B ports supporting up to 32-bit trace.
  - *High Speed Serial Trace Port* (HSSTP) for prototyping of high-speed trace.
- Eight general purpose *Dual In-line Package* (DIP) switches.
- FPGA DONE LED, FPGA configured.
- OverTemp LED.
- Eight general purpose LEDs.
- Local *Daughterboard Configuration Controller* (DCC) that configures the oscillators and power supplies on the daughterboard.
- Battery for FPGA image AES encryption key.
- On-board programmable oscillators.
- Support for *Serial Configuration Controller* (SCC) for correct functioning of LEDs and switches.

For more information, see *System interconnect* on page 2-4.

2.2 System interconnect

Figure 2-2 shows a typical system interconnect.

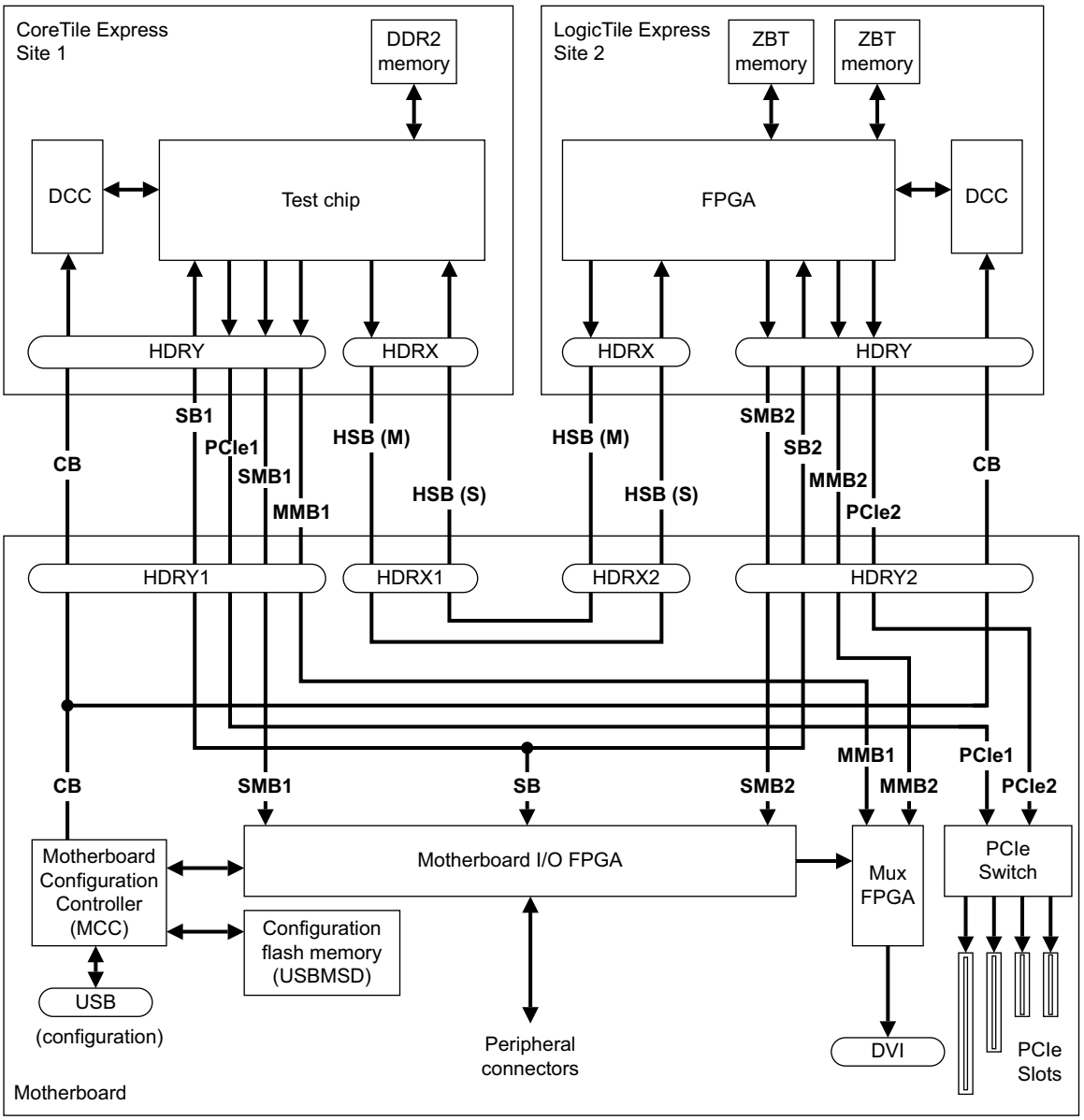


Figure 2-2 System interconnect

The signals on the daughterboard are routed to the motherboard over two header connectors, HDRX and HDRY. For more information on the motherboard signals, see the *Hardware Description* chapter in the *ARM® Motherboard Express µATX Technical Reference Manual*.

Caution

You can damage the FPGA if pins configured as outputs are connected, and output different logic levels.

2.2.1 High-Speed Buses to other daughterboard

The HDRX header connects the daughterboard high-speed master and slave buses to the other daughterboard through dedicated headers on the motherboard. The most common use of these bus lanes is to implement a multiplexed AXI master and slave interface between the V2F-1XV5 and V2P-CA9 daughterboards.

Note

The Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4* supplied on the supporting product media provides an example AXI design implementing external multiplexed AXI master and slave buses at the HDRX header.

2.2.2 *Static Memory Bus* (SMB)

The daughterboard uses the Static Memory Bus for peripheral and memory accesses to the motherboard. This is the minimum bus implementation required to enable the daughterboards to boot and run applications.

2.2.3 *MultiMedia Bus* (MMB)

The optional MultiMedia Bus is implemented to enable a daughterboard to drive audio and video data. This enables the daughterboard to drive up to 1080p UXGA video, and audio formats from stereo to 8-channel surround sound.

2.2.4 *System Bus* (SB)

The System Bus carries interrupt and DMA signals between the daughterboard and the memory and peripherals on the motherboard.

2.2.5 *Configuration Bus* (CB)

Use the Configuration Bus to determine the functionality and capabilities of the daughterboards prior to controlling the power and reset sequence. You can also use it to update the FPGA images and software on the daughterboards. See *FPGA configuration and initialization* on page 2-7.

2.2.6 *PCI-Express Bus* (PCIe)

The daughterboard can implement a *root complex* to connect to the PCI-Express Gen1 Card slots on the motherboard. The daughterboard supports a maximum of eight lanes downwards to HDRY.

Note

ARM does not supply the PCI-Express *root complex*. You can license it from a third party vendor.

Note

The V2M-P1 motherboard can support a *root complex* either on the daughterboard in Site 1 or in Site 2, but not both. You select which site contains the *root complex* by editing the `config.txt` file. By default, the daughterboard in Site 1 is the *root complex*.
The V2M-P1 motherboard tile sites do not support *endpoints* connected to the switch.

2.2.7 ZBT memory interface

The local ZBT memory interface controls two independent 8MB ZBT SRAM parts. Figure 2-3 shows the generic FPGA to ZBT SRAM interconnect.

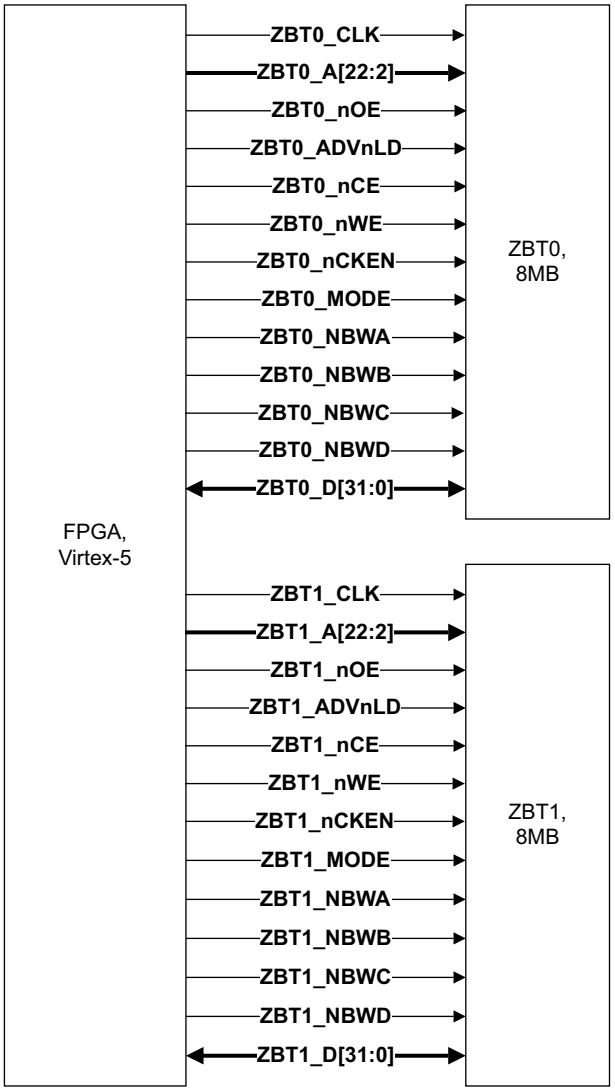


Figure 2-3 Dual ZBT SRAM interface

2.2.8 FPGA configuration flash memory interface

A local 256MB NAND Flash memory stores the FPGA image. The DCC loads data into the Flash memory and initializes the data transfer from the Flash memory to the FPGA.

2.2.9 SATA connectors

Four SATA lanes from the FPGA connect to a SATA connector.

Note

The four SATA lanes consist of two transmit lanes and two receive lanes.

2.3 FPGA configuration and initialization

The daughterboard is fitted with a Xilinx Virtex-5 XC5VLX330T FPGA. Figure 2-4 shows a simplified view of the daughterboard and shows how the FPGA connects to the other on-board devices and the external interfaces.

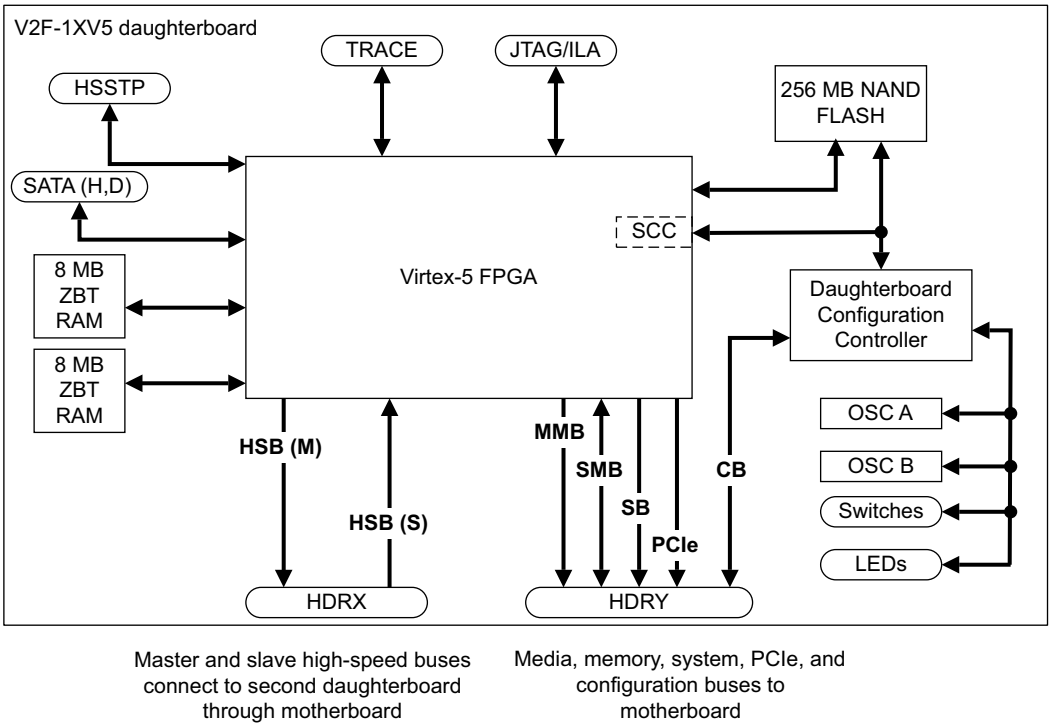


Figure 2-4 Daughterboard block diagram

2.3.1 FPGA image programming and configuration

See the *ARM® Versatile™ Express Configuration Technical Reference Manual* and *ARM® Motherboard Express (µATX)* or *ARM® Programmer Module (V2M-CP1)* for information on how to configure the V2F-1XV5 daughterboard using the configuration files on the motherboard.

Caution

ARM recommends that you use the configuration files for all system configuration. *SCC register descriptions* on page 3-5, however, describes registers that directly modify the FPGA configuration.

Note

A battery-backed encryption key enables DES encrypted FPGA images.

2.3.2 Clocks

The majority of the clocks that the daughterboard uses are generated locally by two on-board clock generators, or within the FPGA. Figure 2-5 on page 2-9 shows the clock domains of the daughterboard.

The on-board Daughterboard Configuration Controller configures the Texas Instruments CDCE937 programmable clock generators during power-up sequencing. See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for more information on how to adjust the clock values.

Note

The frequencies of the clocks that Figure 2-5 on page 2-9 shows are user-defined.

All OSC are unreserved, and reset to 24MHz with an operating range of 2MHz-230MHz with 1% resolution.

The MCC configures the daughterboard clocks on power-up with the values that the daughterboard configuration board file defines. Daughterboard clocks can also be read or written to while the system is running using the motherboard System Configuration registers (CFG) interface, or Boot Monitor. For more information, see the *ARM® Versatile™ Express Configuration Technical Reference Manual*.

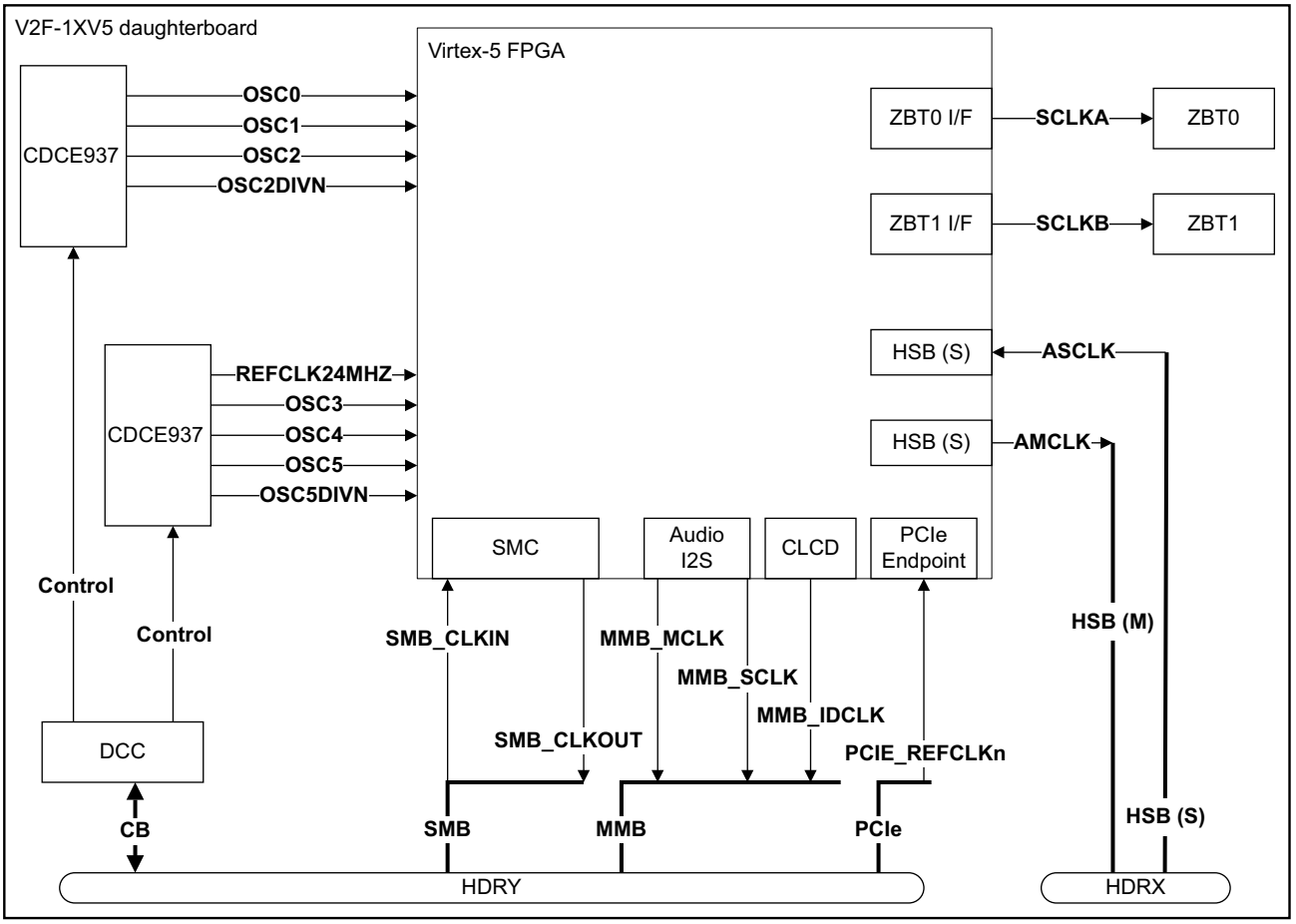


Figure 2-5 Daughterboard clock domains

2.3.3 Resets

The the MCC on the motherboard controls the daughterboard resets. Figure 2-6 on page 2-10 shows the resets from the motherboard and the reset acknowledge signals from the daughterboard.

The **nSRST** signal from the P-JTAG connector or an internal signal can be connected to the **NAND_D[7]** pin in the FPGA. This pin connects to **CB_RESTREQ** using the DCC to request an external reset. This external reset results in **CB_nRST** being asserted. **CB_nPOR** can optionally be asserted by the **ASSERTNPOR** setting, that can be either TRUE or FALSE in the daughterboard configuration files.

See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for an example of the daughterboard configuration file directory structure. See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for examples of daughterboard configuration files.

Note

Only the **CB_nPOR** and **CB_nRST** signals are driven to the daughterboard FPGA. Depending on the motherboard configuration file settings, you can drive **CB_RSTREQ** from the FPGA through the DCC to request a cold or warm reset.

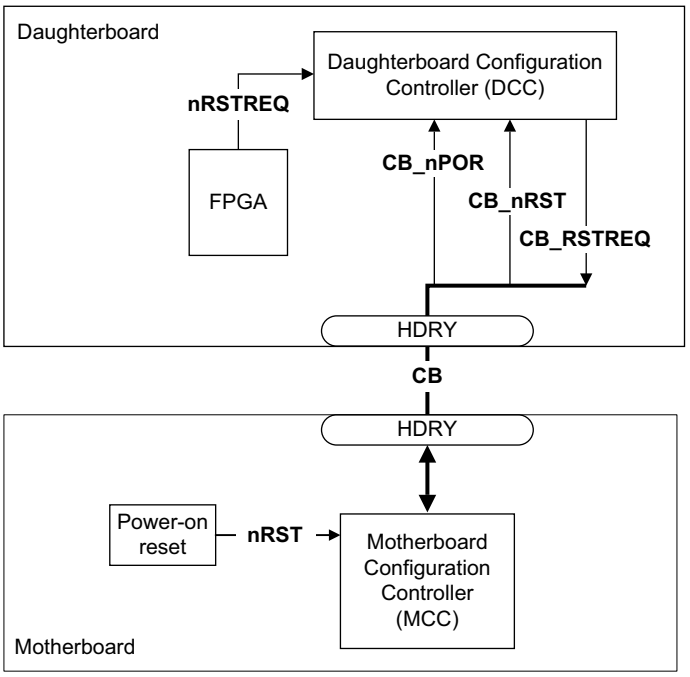


Figure 2-6 Daughterboard resets

Figure 2-7 shows the basic power-up and power-down reset cycle.

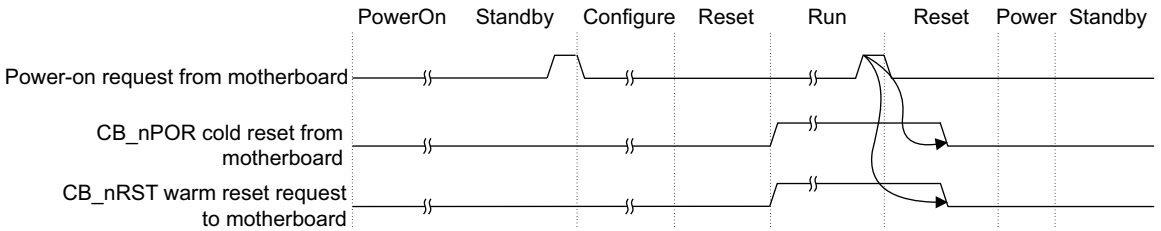


Figure 2-7 Reset timing cycle

2.3.4 DCC FPGA SERIAL INTERFACE

The DCC enables communication to the FPGA. It uses a serial communication channel to receive and transmit information to the FPGA on the daughterboard. It does this by issuing commands to the FPGA. The FPGA must implement a *Serial Configuration Controller* (SCC) to support these commands. See Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4* for an example of a SCC implementation.

The MCC configures the daughterboard SCC registers on power-up with the values that the daughterboard configuration board file defines. SCC registers can also be read or written to while the system is running, using the motherboard SYS CFG register interface.

SCC Serial Configuration Controller

The SCC serial interface operates at 0.5MHz. The serial interface is similar to a memory-mapped peripheral because it has an address and a data phase. Figure 2-8 on page 2-11 and Figure 2-9 on page 2-11 show the timing diagrams for a write and read operation of a design with one address and four data bits, for simplicity. The SCC operates a 12-bit address and 32-bit data phase.

The **nCFGRST** output from the DCC loads the default configuration settings into the FPGA. **CFGLOAD** determines when WRITE DATA is completed, or when READ DATA is expected to be ready. The DCC provides **CGFCLK** to the FPGA. **CFGWnR** changes depending on the access type.

WRITE DATA is sent *Most Significant Bit* (MSB) first.

READ DATA is received *Least Significant Bit* (LSB) first.

Note

If the SCC serial interface is not implemented in the FPGA design, ARM recommends that you tie-off the **CFGDATAOUT** and **nRSTREQ** signals as follows:

- You must tie the **CFGDATAOUT** signal LOW. This is the **NAND_D[5]** pin on the FPGA.
- You must tie the **nRSTREQ** signal HIGH. This is the **NAND_D[7]** pin on the FPGA.

Figure 2-8 shows the DCC write to SCC.

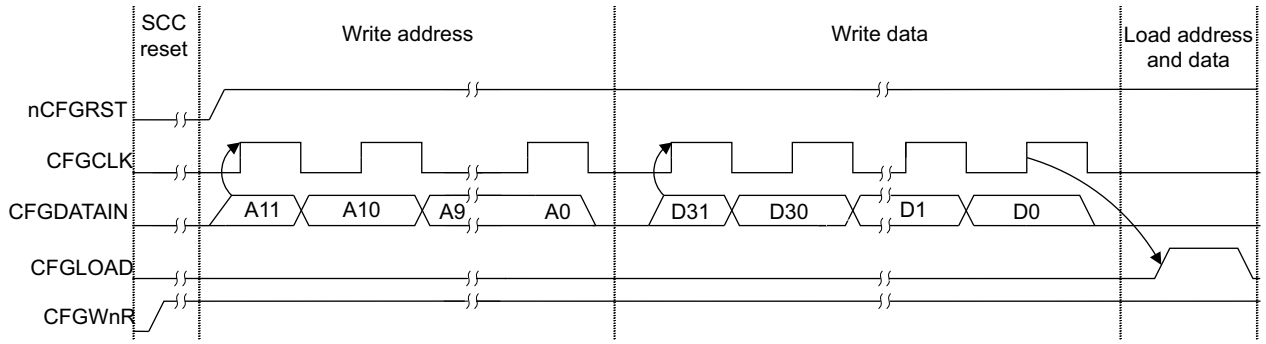


Figure 2-8 DCC write to SCC

Figure 2-9 shows the DCC read from SCC.

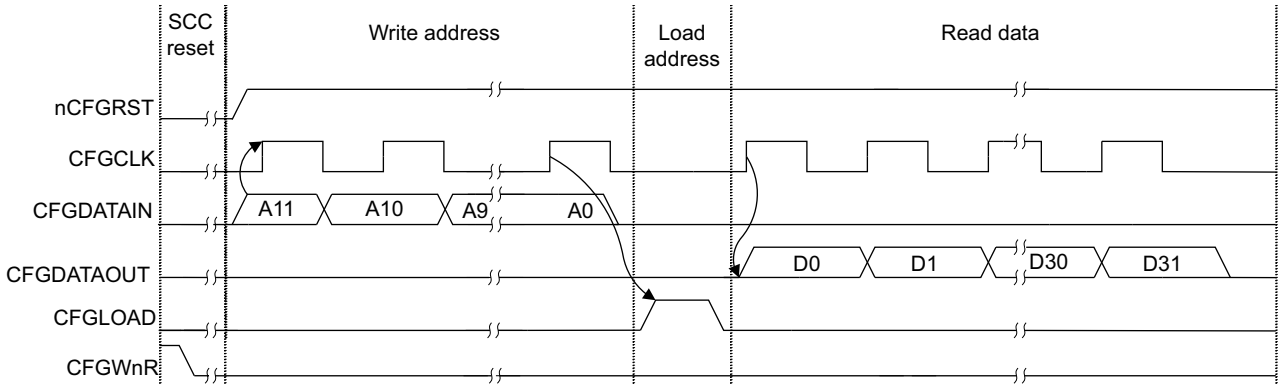


Figure 2-9 DCC read from SCC

Table 2-1 shows the DCC AC timing requirements.

Table 2-1 DCC AC timing requirements for SCC interface

Variable	Time
DCC output valid time, DCCTov	1µs
DCC output hold time, DCCToh	1µs
DCC input setup time, DCCTis	1µs
DCC input hold time, DCCTih	1µs

2.4 FPGA debug and trace

This section describes the debug and trace interfaces provided on the daughterboard.

The following separate JTAG paths exist on the daughterboard:

- F-JTAG, FPGA debug, using F-JTAG (ILA), J6.
- P-JTAG, Processor, using J 13 to connect to a virtual TAP controller synthesized into the FPGA.

The daughterboard supports 32-bit parallel TRACE and six lane HSSTP. The voltage domain for TRACE and HSSTP control is 3V3. See Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4* for FPGA connectivity.

2.5 Minimum design settings for daughterboard operation

The minimum RTL in the LogicTile Express 3MG FPGA to operate correctly involves:

- Setting the **SMB_CLK0** output to the inactive LOW state.
- Setting the SMB chip select to the inactive HIGH state.
- Setting **CFGDATAOUT** to the inactive LOW state.
- Setting the **nRSTREQ** pin to the inactive HIGH state.

1. Set the SMB_CLK0 to the inactive LOW state as follows:

   Tie **SMB_CLK0** to `b0`.

   Note

   This stops data being clocked to the IOFPGA on the motherboard.

2. Set the SMB chip select to the inactive HIGH state as follows:

   Tie the chip selects **SMB_nCS** to `b11111111`.

   Note

   This stops static memory access to the motherboard.

3. Set the CFGATAOUT signal to the inactive LOW state as follows:

   Tie **NAND_D[5]** to `b0`, as the note in *SCC Serial Configuration Controller* on page 2-10 describes.

   Note

   This informs the DCC that no DCC features are implemented.

4. Set the **nRSTREQ** pin to the inactive HIGH state as follows:

   Tie **NAND_D[7]** to `b1`.

   Note

   This prevents **nRSTREQ** from generating a reset. **nRSTREQ** is usually a system-wide master soft reset signal that is both generated and observed by the JTAG debug box.

Note

ARM recommends that all unused pins must be tied to their inactive states.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About this programmers model

The following information applies to the SCC registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or power-on reset.
- Access type in Table 3-1 on page 3-3 is described as follows:

  RW Read and write.

  RO Read only.

  WO Write only.

3.2 Register summary

Table 3-1 shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000-0x0FC	DCC_CFGx	RW	0xXXXXXXXX [a]	32	*DCC_CFGx Registers* on page 3-5
0x100	DCC_LOCK	RO	0xFFXX000X[b]	32	*DCC_LOCK Register* on page 3-5
0x104	DCC_LED	RO	0x0000000F	32	*DCC_LED Register* on page 3-6
0x108	DCC_SW	RO	0x00000000	32	*DCC_SW Register* on page 3-7
0xFF8	DCC_AID	RO	0xXXXXXXXX[a]	32	*DCC_AID Register* on page 3-7
0xFFC	DCC_ID	RO	0xXXXXXXXX[a]	32	*DCC_ID Register* on page 3-8

a. Where X = unknown at reset.

b. Last X = b000X, either b0000 or b0001.

3.3 Memory map

The LogicTile Express 3MG has an empty memory, so you must determine the memory map.

3.4 SCC register descriptions

The DCC writes to the SCC registers at power-up with the values that the configuration board file defines. The DCC also reads the LOCK and ID registers to determine whether the PLLs in the FPGA are locked, and to determine which FPGA image has been loaded. During run-time, the DCC polls the LED and Switch values to ensure that they match SCC register values. The SCC registers are also available during run-time from the motherboard SYG_CFG register interface.

3.4.1 DCC_CFGx Registers

The DCC_CFGx Registers characteristics are:

Purpose These registers write the USER configuration value. You can define up to 64 write registers. The register address must be in increments of `0x004` and the data must be 32 bits wide. The MCC reads the daughterboard configuration file during board configuration and writes the register values to the FPGA SCC registers. You must implement the appropriate decoder and logic in the FPGA for these to have any effect.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-1 shows the bit assignments.

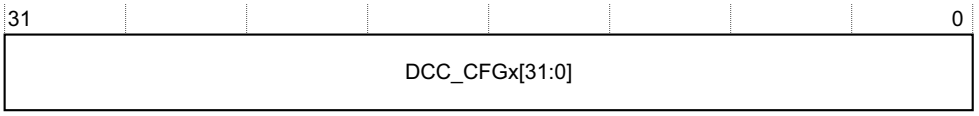


Figure 3-1 DCC_CFGx Registers bit assignments

Table 3-2 shows the bit assignments.

Table 3-2 DCC_CFGx Registers bit assignments

Bits	Name	Function
[31:0]	DCC_CFGx[31:0]	User registers configured during board initialization up from configuration file

Note

You can also update the DCC_CFGx Registers during run-time using the motherboard SYS_CFG register interface, or motherboard serial port command line interface or SCC APB interface.

3.4.2 DCC_LOCK Register

The DCC_LOCK Register characteristics are:

Purpose PLL lock status bits from the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-2 shows the bit assignments.

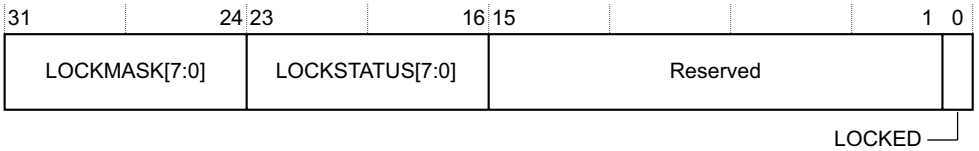


Figure 3-2 DCC_LOCK Register bit assignments

Table 3-3 shows the bit assignments.

Table 3-3 DCC_LOCK Register bit assignments

Bits	Name	Function
[31:24]	LOCK_MASK[7:0]	These bits indicate if the individual lock bits are masked.
[23:16]	LOCK_STATUS[7:0]	These bits indicate the individual lock status: `b0` Unlocked. `b1` Locked.
[15:1]	-	Reserved
[0]	LOCKED	This bit indicates whether all unmasked lock bits are locked: `b0` Unlocked. `b1` Locked.

3.4.3 DCC_LED Register

The DCC_LED Register characteristics are:

Purpose Controls the USER LEDs on the daughterboard. The DCC polls this SCC register from the FPGA and updates the appropriate LEDs.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-3 shows the bit assignments.

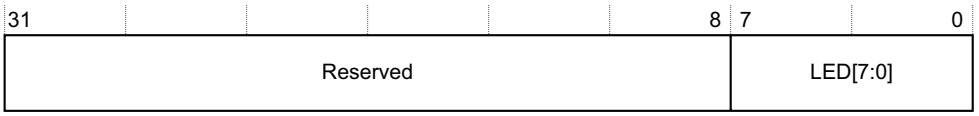


Figure 3-3 DCC_LED Register bit assignments

Table 3-4 shows the bit assignments.

Table 3-4 DCC_LED Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	LED[7:0]	These bits control the individual USER LEDs

3.4.4 DCC_SW Register

The DCC_SW Register characteristics are:

Purpose Determines the state of the eight user switches on the daughterboard. The DCC polls the switches and updates this SCC register in the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-4 shows the bit assignments.

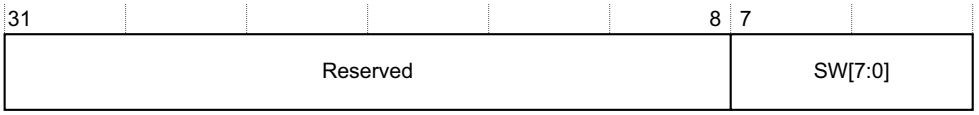


Figure 3-4 DCC_SW Register bit assignments

Table 3-5 shows the bit assignments.

Table 3-5 DCC_SW Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	SW[7:0]	These bits indicate state of user switches

3.4.5 DCC_AID Register

The DCC_AID Register characteristics are:

Purpose The DCC reads this information and uses it to determine the number of DCC_CFGx registers, and the registers that are supported that can be read from the motherboard SYS-CFG register interface. If this register is not implemented, the DCC does not support user switches or LEDs, lock, or `user config` commands.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-5 shows the bit assignments.

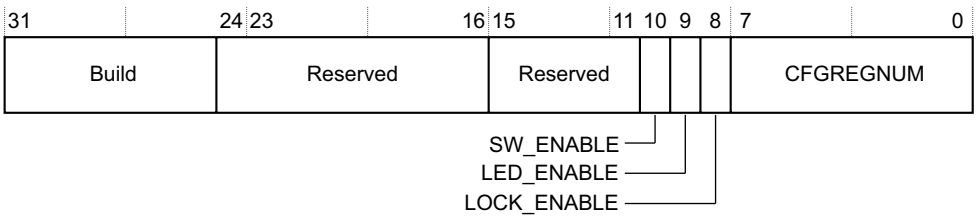


Figure 3-5 DCC_AID Register bit assignments

Table 3-6 shows the bit assignments.

Table 3-6 DCC_AID Register bit assignments

Bits	Name	Function
[31:24]	Build	FPGA build number.
[23:16]	-	Reserved.
[15:11]	-	Reserved.
[10]	SW_ENABLE	This bit indicates whether the DCC_SW_READ command is supported.
[9]	LED_ENABLE	This bit indicates whether the DCC_LED_READ command is supported.
[8]	LOCK_ENABLE	This bit indicates whether the DCC_LOCK_READ command is supported.
[7:0]	CFGREGNUM	These bits indicate the number of user config commands. The maximum number supported is 64.

3.4.6 DCC_ID Register

The DCC_ID Register characteristics are:

Purpose The DCC reads this register and uses it to determine information about the design in the FPGA that can be read through the motherboard SYS_CFG register interface.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 3MG configurations.

Attributes See Table 3-1 on page 3-3.

Figure 3-6 shows the bit assignments.

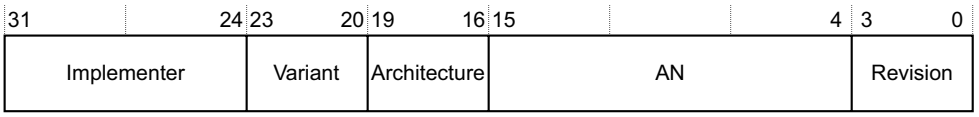


Figure 3-6 DCC_ID Register bit assignments

Table 3-7 shows the bit assignments.

Table 3-7 DCC_ID Register bit assignments

Bits	Name	Function
[31:24]	Implementer	Implementer ID
[23:20]	Variant	Variant number
[19:16]	Architecture	Architecture. `0x00` for Application Notes
[15:4]	AN	Application Note number
[3:0]	Revision	Revision number

Appendix A
Signal Descriptions

This chapter describes the signals present at the interface connectors. The on board connectors are:

A.1 Daughterboard connectors

Figure A-1 shows the connectors fitted to the daughterboard.

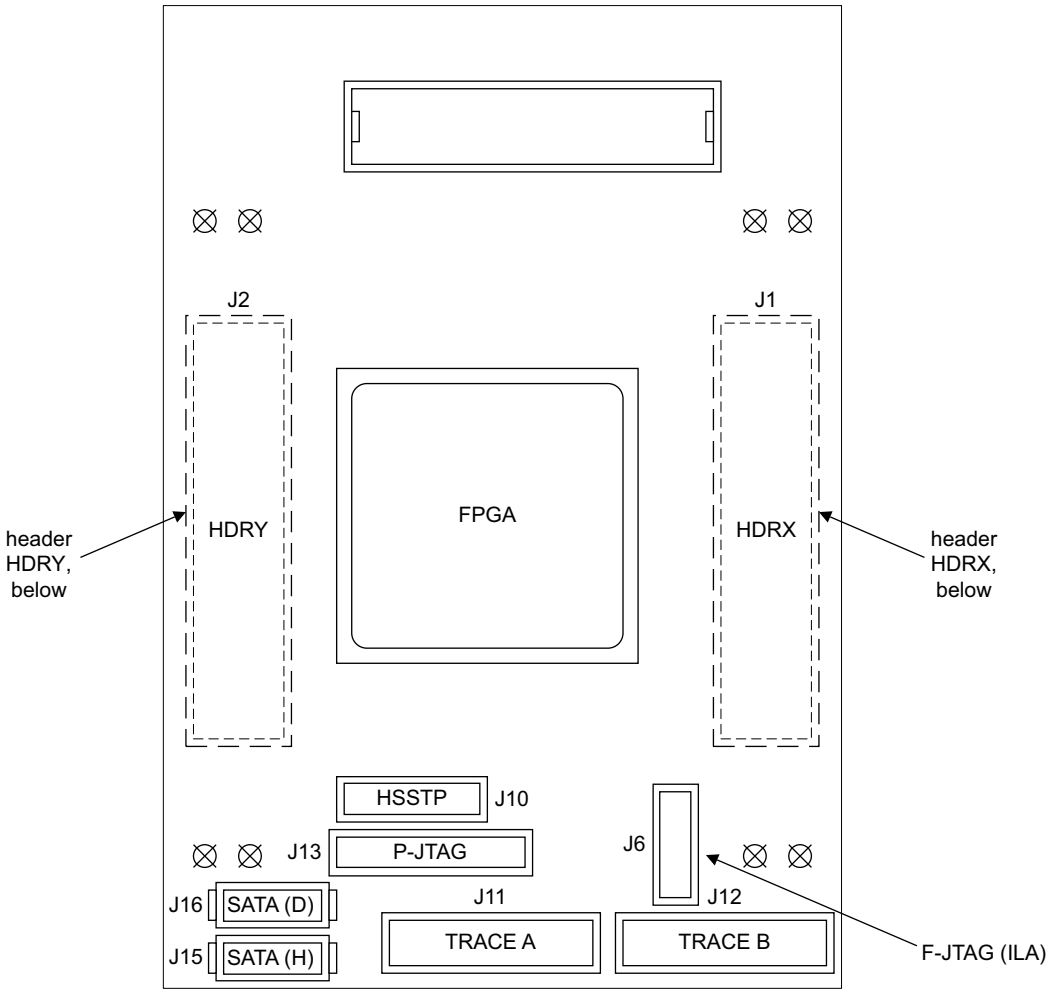


Figure A-1 Daughterboard connectors

A.1.1 Header connectors

There are two high density headers fitted to the underside of the daughterboard. These headers, designated HDRX, J1, and HDRY, J2, route the signal and power interconnect between a daughterboard and the motherboard. The daughterboard is not stackable.

A.1.2 Trace connectors

Trace connectors are provided for up to 32-bit trace. The two trace connectors provide access to a *Trace Port Interface Unit* (TPIU) that you can implement in the FPGA.

Note

The trace connectors are connected to the FPGA to support up to 32-bit trace port widths when using RealView Trace 2 and the 32-bit dual-Mictor probe. JTAG signals on the Trace Connector are wired in parallel to the ICE JTAG port. If required, you can also implement a RealView ICE JTAG connection and *Serial Wire Debug* (SWD) at the Trace A port.

Figure A-2 shows the trace connector.

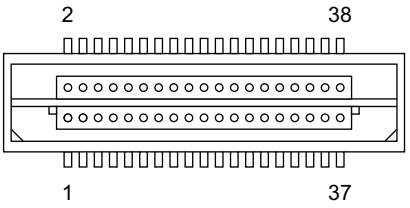


Figure A-2 Trace connector

Note

The part number for the Mictor connector is AMP 2-767004-2.

Table A-1 shows the trace pin mapping for each Trace Port A signal. See the Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4* constraints file for FPGA mapping.

Table A-1 Trace Port A connector, J11

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKA**
7	**TRACEDBGRQ**	8	**TRACEDBGACK**
9	**nSRST**	10	**TRACEEXTTRIGX**
11	**TDO**	12	**VTREFA**
13	**RTCK**	14	**VSUPPLYA**
15	**TCK**	16	**TRACEDATA7**
17	**TMS**	18	**TRACEDATA6**
19	**TDI**	20	**TRACEDATA5**
21	**nTRST**	22	**TRACEDATA4**
23	**TRACEDATA15**	24	**TRACEDATA3**
25	**TRACEDATA14**	26	**TRACEDATA2**
27	**TRACEDATA13**	28	**TRACEDATA1**
29	**TRACEDATA12**	30	**GND**
31	**TRACEDATA11**	32	**GND**
33	**TRACEDATA10**	34	**3V3**
35	**TRACEDATA9**	36	**TRACECTL**
37	**TRACEDATA8**	38	**TRACEDATA0**

Note

You must program pull-down resistors on the **TRACEDBGRQ** and **TRACEDBGACK** pins in the constraints file in Application Note AN224 *Example LogicTile Express 3MG design for a CoreTile Express A9x4*.

Table A-2 shows the Trace pin mapping for each Trace Port B signal. See the Application Note AN224 *Example LogicTile Express 3MG design for a Core Tile Express A9x4* for FPGA mapping.

Table A-2 Trace Port B connector, J12

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKB**
7	Not connected	8	Not connected
9	Not connected	10	Not connected
11	Not connected	12	**VTREFB**
13	Not connected	14	Not connected
15	Not connected	16	**TRACEDATA23**
17	Not connected	18	**TRACEDATA22**
19	Not connected	20	**TRACEDATA21**
21	Not connected	22	**TRACEDATA20**
23	**TRACEDATA31**	24	**TRACEDATA19**
25	**TRACEDATA30**	26	**TRACEDATA18**
27	**TRACEDATA29**	28	**TRACEDATA17**
29	**TRACEDATA28**	30	**GND**
31	**TRACEDATA27**	32	**GND**
33	**TRACEDATA26**	34	**3V3**
35	**TRACEDATA25**	36	**GND**
37	**TRACEDATA24**	38	**TRACEDATA16**

A.1.3 P-JTAG connector

The P-JTAG connector is provided on the daughterboard to enable connection of RealView ICE or a compatible third-party debugger. Figure A-3 on page A-5 shows the P-JTAG connector, J13.

Note

All signal connections on the P-JTAG connector have pull-up resistors to 3V3.

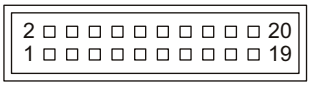


Figure A-3 P-JTAG connector, J13

Table A-3 shows the JTAG pin mapping for each JTAG signal.

Table A-3 P-JTAG connector, J13

JTAG pin	JTAG signal	JTAG pin	JTAG signal
1	**3V3**	2	**3V3**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**TMS**	8	**GND**
9	**TCK**	10	**GND**
11	**RTCK**	12	**GND**
13	**TDO**	14	**GND**
15	**nSRST**	16	**GND**
17	Not connected	18	**GND**
19	Not connected	20	**nICEDETECT**

A.1.4 F-JTAG (ILA) connector

Figure A-4 shows the F-JTAG (ILA) connector, J6. You can use an ILA device such as *ChipScope*™ to debug designs in the FPGA.

Note

Pins 4, 6, and 10 on the F-JTAG (ILA) connector have pull-up resistors to 3V3.

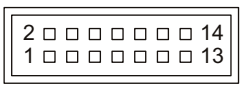


Figure A-4 F-JTAG (ILA) connector, J6

Table A-4 shows the F-JTAG (ILA) pin mapping for each ILA signal.

Table A-4 F-JTAG (ILA) connector, J6

ILA pin	ILA signal	ILA pin	ILA signal
1	**GND**	2	**3V3**
3	**GND**	4	**ILA_TMA**
5	**GND**	6	**ILA_TCLK**
7	**GND**	8	**ILA_TDO**

Table A-4 F-JTAG (ILA) connector, J6 (continued)

ILA pin	ILA signal	ILA pin	ILA signal
9	**GND**	10	**ILA_TDI**
11	**GND**	12	Not connected
13	**GND**	14	Not connected

A.1.5 SATA connectors

There are two SATA connectors on the daughterboard. Connectivity for a SATA Host, H, and SATA Device, D, interface is provided. Figure A-5 shows the SATA connector.

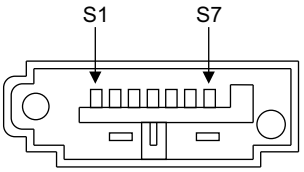


Figure A-5 SATA connector, J15, J16

Table A-5 shows the SATA Host pin mapping for each SATA signal. The GTX location for the SATA Host signals is X0Y3. See application note AN224, *Example LogicTile Express 3MG design for a CoreTile Express A9x4* constraints file `v2f_1xv5_rev(b or c).ucf` for FPGA mapping.

Caution

The SATA host signals B+ and B- connect to the FPGA with their polarity reversed from the default to improve signal integrity. Signal pairs must be swapped in the FPGA by setting the inverted polarity input in the instantiation of the transceiver module.

Table A-5 shows the SATA Host pin mapping for each SATA signal.

Table A-5 SATA host, J15, signal list

SATA pin	SATA host signal, J15
S1	**GND**
S2	**A+**
S3	**A-**
S4	**GND**
S5	**B-**
S6	**B+**
S7	**GND**

Table A-6 on page A-7 shows the SATA Device pin to FPGA pin mapping for each SATA signal. The GTX location for the SATA Device signals is X0Y3. See application note AN224, *Example LogicTile Express 3MG design for a CoreTile Express A9x4* constraints file `v2f_1xv5_rev(b or c).ucf` for FPGA mapping.

Caution

The SATA device signals A+ and A- connect to the FPGA with their polarity reversed from the default to improve signal integrity. Signal pairs must be swapped in the FPGA by setting the inverted polarity input in the instantiation of the transceiver module.

Table A-6 shows the SATA device pin to FPGA pin mapping for each SATA signal.

Table A-6 SATA device, J16, to FPGA signal list

SATA pin	SATA Device signal, J16
S1	**GND**
S2	**A+**
S3	**A-**
S4	**GND**
S5	**B-**
S6	**B+**
S7	**GND**

A.1.6 HSSTP connector

The daughterboard includes the interconnect to implement a *High Speed Serial Trace Port* (HSSTP). The interconnect supports six lanes of LVDS signaling. Figure A-6 on page A-8 shows the HSSTP connector, J10.

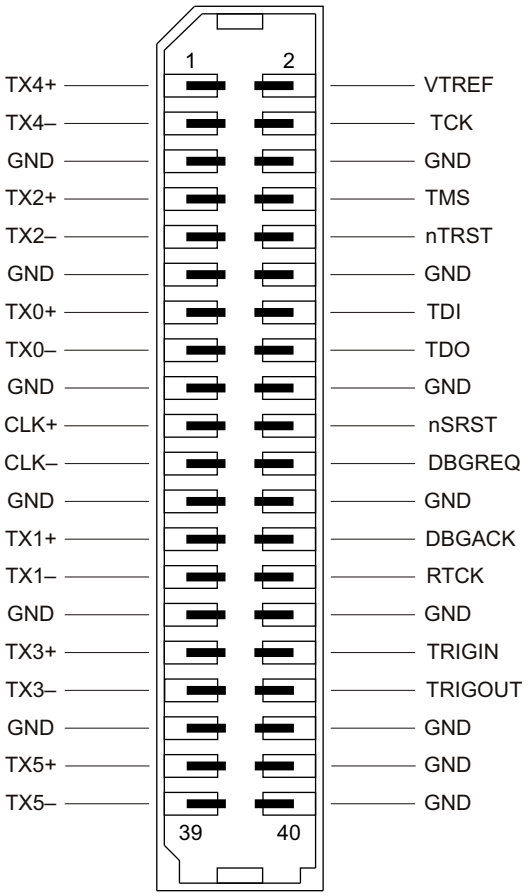


Figure A-6 HSSTP connector, J10

Table A-7 shows the HSSTP pin mapping.

Caution

The LVDS Device signal pairs, TX1+ and TX1-, TX2+ and TX2-, and TX5+ and TX5-, connect to the FPGA with their polarity reversed from the default to improve signal integrity. Signal pairs must be swapped in the FPGA by setting the inverted polarity input in the instantiation of the transceiver module.

Table A-7 shows the HSSTP pin mapping.

Table A-7 HSSTP connector, J10, signal list

HSSTP pin	HSSTP signal	HSSTP pin	HSSTP signal
1	**TX4+**	2	**VTREF**
3	**TX4-**	4	**TCK**
5	**GND**	6	**GND**
7	**TX2+**	8	**TMS**
9	**TX2-**	10	**nTRST**
11	**GND**	12	**GND**
13	**TX0+**	14	**TDI**

Table A-7 HSSTP connector, J10, signal list (continued)

HSSTP pin	HSSTP signal	HSSTP pin	HSSTP signal
15	**TX0-**	16	**TDO**
17	**GND**	18	**GND**
19	**CLK+**	20	**nSRST**
21	**CLK-**	22	**DBGREQ**
23	**GND**	24	**GND**
25	**TX1+**	26	**DBGACK**
27	**TX1-**	28	**RTCK**
29	**GND**	30	**GND**
31	**TX3+**	32	**TRIGIN**
33	**TX3-**	34	**TRIGOUT**
35	**GND**	36	**GND**
37	**TX5+**	38	**GND**
39	**TX5-**	40	**GND**

Table A-8 shows the HSSTP TX signal FPGA-GTX connectivity.

Table A-8 HSSTP TX signal FPGA-GTX connectivity

HSSTP signal	GTX location
HSSTP_TX0_P	X0Y1
HSSTP_TX0_N	
HSSTP_TX1_P	X0Y1
HSSTP_TX1_N	
HSSTP_TX2_P	X0Y0
HSSTP_TX2_N	
HSSTP_TX3_P	X0Y2
HSSTP_TX3_N	
HSSTP_TX4_P	X0Y0
HSSTP_TX4_N	
HSSTP_TX5_P	X0Y1
HSSTP_TX5_N	

Appendix B
Specifications

This appendix contains the specification of the daughterboard. It contains the following section:

- *Electrical specification* on page B-2.

B.1 Electrical specification

This section provides information on the voltage and current characteristics for the daughterboard and describes:

- *Bus interface characteristics*
- *FPGA current requirements*.

B.1.1 Bus interface characteristics

Table B-1 shows the daughterboard electrical characteristics.

Table B-1 Electrical characteristics for 3V3 I/O

Symbol	Description	Min	Max	Unit
V_{IH}	High-level input voltage	1.2	3.3	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage	2.4	-	V
V_{OL}	Low-level output voltage	-	0.4	V

B.1.2 FPGA current requirements

Table B-2 shows the maximum current requirements for the daughterboard voltage supplies listed by system component when using the example images supplied on the *Versatile Express DVD*.

Note

The actual current depends on the complexity of the design in the daughterboard and the clock speed used for the system. For a fuller implementation and higher clock rate, the observed value can be several times the value that Table B-2 shows.

Software to help in calculating the current requirements for your particular application is available on the Xilinx web site `http://www.xilinx.com`.

Table B-2 shows the maximum current requirements for the daughterboard voltage supplies.

Table B-2 Current requirements

Component	Voltage range	Maximum current
Core	1V	5A
I/O	1.2 - 3.3V	1.5A
AUX	2.5V	2A

The current requirements that Table B-2 shows require a maximum current of 2.5A from the external 5V supply to the daughterboard.

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book

Table C-1 Issue A

Change	Location	Affects
No changes, first release	-	-

Table C-2 Differences between Issue A and Issue B

Change	Location	Affects
Flash memory diagram removed because it is not required in the document.	*FPGA configuration flash memory interface* on page 2-6.	All versions
Section DCC FPGA SERIAL INTERFACE reworded.	*DCC FPGA SERIAL INTERFACE* on page 2-10.	Version B
Figure altered with daughterboard header names swapped so that site 2 becomes daughterboard site 1.	Figure 2-2 on page 2-4.	All versions
Programmers Model chapter created.	Chapter 3 *Programmers Model*.	Version B
Table Trace Port A connector, J11, pin names changed to reflect signal names in schematic: Pins 9 to 21 and Pin 34.	Table A-1 on page A-3.	All versions
Table Trace Port B connector, J12, pin 34 name changed to reflect signal names in schematic.	Table A-2 on page A-4.	All versions

Table C-2 Differences between Issue A and Issue B (continued)

Change	Location	Affects
Table headings changed from Command name to Register name.	Table A-1 on page A-3. Table A-2 on page A-4.	Version B
Updated section below SATA connector, J15, J16.	Figure A-5 on page A-6.	All versions
Caution statement changed to *The SATA host*.	*SATA connectors* on page A-6.	All versions
Updated section below SATA Host, J15, signal list.	Table A-5 on page A-6.	All versions
New table added showing HSSTP TX signal FPGA-GTX connectivity.	Table A-8 on page A-9.	All versions

Table C-3 Differences between Issue B and Issue C

Change	Location	Affects
System interconnect diagram updated: • HDRY1 position corrected. • HDRX1 position corrected. • HDRX2 position corrected. • HDRY2 position corrected.	Figure 2-2 on page 2-4.	All versions
Clocks section clarified.	*Clocks* on page 2-8.	All versions
Minimum design settings for daughterboard operation section added.	*Minimum design settings for daughterboard operation* on page 2-14.	All versions
PISMO2 connector section updated.		All versions

Table C-4 Differences between Issue C and Issue D

Change	Location	Affects
Document updated to latest Technical Publications *Element Definition Document* (EDD).	All of document.	Version D
Signal name **nRSTREQ** added to daughterboard resets diagram for additional clarification. This signal was formerly called **nSRST** but not identified in the diagram.	Figure 2-6 on page 2-10.	Version D
Reference in main text to tying **CFGDATAOUT** HIGH removed.	*DCC FPGA SERIAL INTERFACE* on page 2-10.	Version D
Note added to say that signal **nRSTREQ** must be tied HIGH when the FPGA design does not support the SCC serial interface.	*DCC FPGA SERIAL INTERFACE* on page 2-10.	Version D
Replaced **NAND_D[7]** pin with **nRSTREQ**.	*Minimum design settings for daughterboard operation* on page 2-14.	Version D
Changed signal names from **nSRST** to **nRSTREQ**.	*Minimum design settings for daughterboard operation* on page 2-14.	Version D
Signals chapter changed to Signal Descriptions appendix to match other documents in the Versatile Express set.	Appendix A *Signal Descriptions*.	Version D

Table C-5 Differences between Issue D and Issue E

Change	Location	Affects
User must program pull-down resistors on **TRACEDBGRQ** and **TRACEDBGACK** pins in constraints file.	*Trace connectors* on page A-2.	Version E
Glossary removed. Reference and link to *ARM Glossary* added to Preface.	*Glossary* on page viii.	Version E
Configuration section shortened. Information is now in new document *ARM® Versatile Express Configuration Technical Reference Manual.*	*FPGA configuration and initialization* on page 2-7.	Version E
Added new documents to Additional Reading section of Preface: • *ARM® Versatile Express Configuration Technical Reference Manual*. • *ARM® CoreTile Express A5x2 Technical Reference Manual*. • *ARM® CoreTile Express A15x2 Technical Reference Manual*.	*Additional reading* on page x.	Version E
Add speed-grade to FPGA description.	*About the LogicTile Express 3MG daughterboard* on page 1-3. *Overview of the daughterboard hardware* on page 2-2.	Version E

Table C-6 Differences between Issue E and Issue F

Change	Location	Affects
Corrected description of PCI-Express system.	*PCI-Express Bus (PCIe)* on page 2-5.	All versions

Table C-7 Differences between Issue F and Issue G

Change	Location	Affects
Removed references to PISMO2.	Throughout document.	All versions