ARM® CoreTile Express A9×4

Cortex®-A9 MPCore (V2P-CA9)

Technical Reference Manual

ARM®

ARM CoreTile Express A9×4
Technical Reference Manual

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Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
27 November 2009	A	Non-Confidential	First release for V2P-CA9
26 March 2010	B	Non-Confidential	Second release for V2P-CA9
27 August 2010	C	Non-Confidential	Third release for V2P-CA9
15 October 2010	D	Non-Confidential	Fourth release for V2P-CA9
28 March 2011	E	Non-Confidential	Fifth release for V2P-CA9
12 October 2012	F	Non-Confidential	Sixth release for V2P-CA9
31 March 2013	G	Non-Confidential	Seventh release for V2P-CA9
29 May 2014	H	Non-Confidential	Eighth release for V2P-CA9
22 May 2015	I	Non-Confidential	Ninth release for V2P-CA9

Confidentiality Status

Product Status

The information in this document is final, that is for a developed product.

Web Address

http://www.arm.com

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

$$C \in$$

The system should be powered down when not in use.

The daughterboard generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the card.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

.

——— **Note** ———

It is recommended that wherever possible shielded interface cables be used.

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ARM CoreTile Express A9×4 Technical Reference Manual

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Appendix C   **Revisions**

Preface

This preface introduces the *CoreTile Express A9×4 Technical Reference Manual*. It contains the following sections:

- *About this book* on page viii
- *Feedback* on page xii.

About this book

This book is for CoreTile Express A9×4 daughterboard.

Product revision status

The r*n*p*n* identifier indicates the revision status of any Intellectual Property, such as ARM PrimeCells, described in this book, where:

r*n*   Identifies the major revision of the product.

p*n*   Identifies the minor revision or modification status of the product.

Intended audience

This document is written for experienced hardware and software developers to aid the development of ARM-based products using the CoreTile Express A9×4 daughterboard with the Motherboard Express µATX as part of a development system.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the CoreTile Express A9x4 daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the daughterboard.

Appendix A *Signal Descriptions*

Read this for a description of the signals present on the daughterboard.

Appendix B *Specifications*

Read this for a description of the electrical specifications of the daughterboard.

Appendix C *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary* http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Conventions

This book uses the conventions that are described in:

Typographical conventions

The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
monospace	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
monospace *italic*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
monospace bold	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

Clock
HIGH to LOW
Transient
HIGH/LOW to HIGH
Bus stable
Bus to high impedance
Bus change
High impedance to stable bus
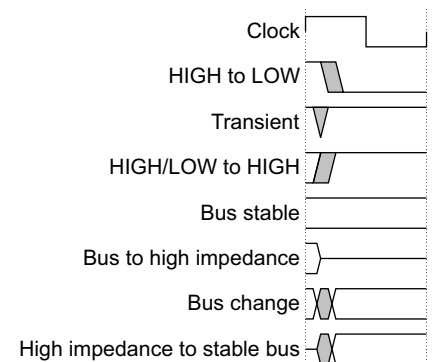
Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *ARM® Motherboard Express µATX Technical Reference Manual* (ARM DUI 0447)

- *ARM® Versatile™ Express Configuration Technical Reference Manual* (ARM DDI 0496)

- *ARM® LogicTile Express 3MG Technical Reference Manual* (ARM DUI 0449)

- *ARM® LogicTile Express 13MG Technical Reference Manual* (ARM DUI 0556)

- *ARM® Versatile™ Express Boot Monitor Technical Reference Manual* (ARM DUI 0465)

- *ARM® PrimeCell PL301 High-Performance Matrix Technical Summary* (ARM DDI 0422)

- *ARM® PrimeCell High-Performance Matrix (PL301) Technical Reference Manual* (ARM DDI 0397)

- *ARM® Cortex®-A9 MPCore Technical Reference Manual* (ARM DDI 0407)

- *ARM® PrimeCell PL341 Dynamic Memory Controller Technical Reference Manual* (ARM DDI 0331)

- *ARM® PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual* (ARM DDI 0380)

- *ARM® PrimeCell Color LCD Controller (PL111) Technical Reference Manual* (ARM DDI 0293)

- *ARM® PrimeCell Level 2 Cache Controller (PL310) Technical Reference Manual* (ARM DDI 0246)

- *ARM® Dual-Timer Module (SP804) Technical Reference Manual* (ARM DDI 0271)

- *ARM® PrimeCell DDR2 Dynamic Memory Controller (PL341) Technical Reference Manual* (ARM DDI 0418)

- *ARM® PrimeCell External Bus Interface (PL220) Technical Reference Manual* (ARM DDI 0249)

- *ARM® Watchdog Module (SP805) Technical Reference Manual* (ARM DDI 0270).

- *Embedded Trace Macrocell Architecture Specification* (ARM IHI 0014)

The following publications provide information about related ARM products and toolkits:

- *ARM® RealView ICE User Guide* (ARM DUI 0155)

- *ARM® RealView Debugger User Guide* (ARM DUI 0153)

- *ARM® RealView Compilation Tools Compilers and Libraries Guide* (ARM DUI 0205)

- *ARM® RealView Compilation Tools Developer Guide* (ARM DUI 0203)

- *ARM® RealView Compilation Tools Linker and Utilities Guide* (ARM DUI 0206)

- *ARM® CoreSight™ PTM-A9 Technical Reference Manual* (ARM DDI 0401)

- *ARM® CoreSight™ Components Technical Reference Manual* (ARM DDI 0314)

- *ARM® PrimeCell Infrastructure AMBA®3 TrustZone® Protection Controller (BP147) Technical Overview* (ARM DTO 0015)

- *Example LogicTile Express 3MG design for a CoreTile Express A9×4 Application Note AN224.*

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.

- The product revision or version.

- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:
- The title.
- The number, ARM DUI 0448I.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

——— **Note** ———

ARM tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter provides an introduction to the CoreTile Express A9×4, Cortex-A9 MPCore, daughterboard. It contains the following sections:

- *About the CoreTile Express A9×4 daughterboard* on page 1-2
- *Precautions* on page 1-4.

1.1 About the CoreTile Express A9×4 daughterboard

The daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA) that use the *Advanced eXtensible Interface* (AXI™) or custom logic for use with ARM cores.

You can use the Cortex-A9 MPCore test chip in the CoreTile Express A9×4 with a Motherboard Express µATX to create prototype systems.

──── **Note** ────

The daughterboard must be used with a Motherboard Express µATX. See the *Motherboard Express µATX Technical Reference Manual* for information about interconnection.

The daughterboard comprises the following hardware and interfaces:

- Cortex-A9 MPCore test chip.

- Daughterboard Configuration Controller.

- Multiplexed AMBA AXI Master and Slave buses to an optional LogicTile Express daughterboard.

- 1 GB DDR2 SDRAM.

- *Color LCD Controller* (CLCDC).

- CoreSight software debug and Trace ports.

Figure 1-1 on page 1-3 shows the layout of the daughterboard:
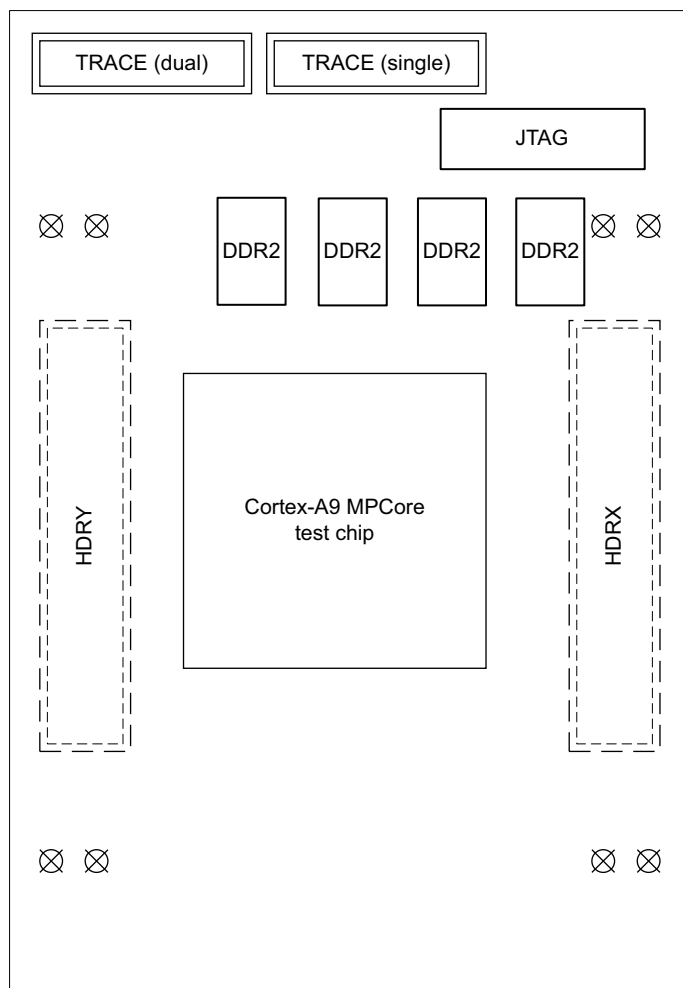
Figure 1-1 CoreTile Express A9×4 daughterboard layout

1.2 Precautions

This section contains advice about how to prevent damage to your daughterboard.

1.2.1 Ensuring safety

The daughterboard is supplied with a range of DC voltages. Power is supplied to the daughterboard through the header connectors.

——— **Warning** ———

Do not use the board near equipment that is sensitive to electromagnetic emissions, for example medical equipment.

1.2.2 Preventing damage

The daughterboard is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure which leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

——— **Caution** ———

To avoid damage to the daughterboard, observe the following precautions.

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.

- Always wear a grounding strap when handling the board.

- Only hold the board by the edges.

- Avoid touching the component pins or any other metallic element.

- Do not use the board near a transmitter of electromagnetic emissions.

Chapter 2
Hardware Description

This chapter describes the hardware on the CoreTile Express A9×4 daughterboard. It contains the following sections:

2.1 Overview of the CoreTile Express A9×4 daughterboard

Figure 2-1 shows a block diagram of the daughterboard.
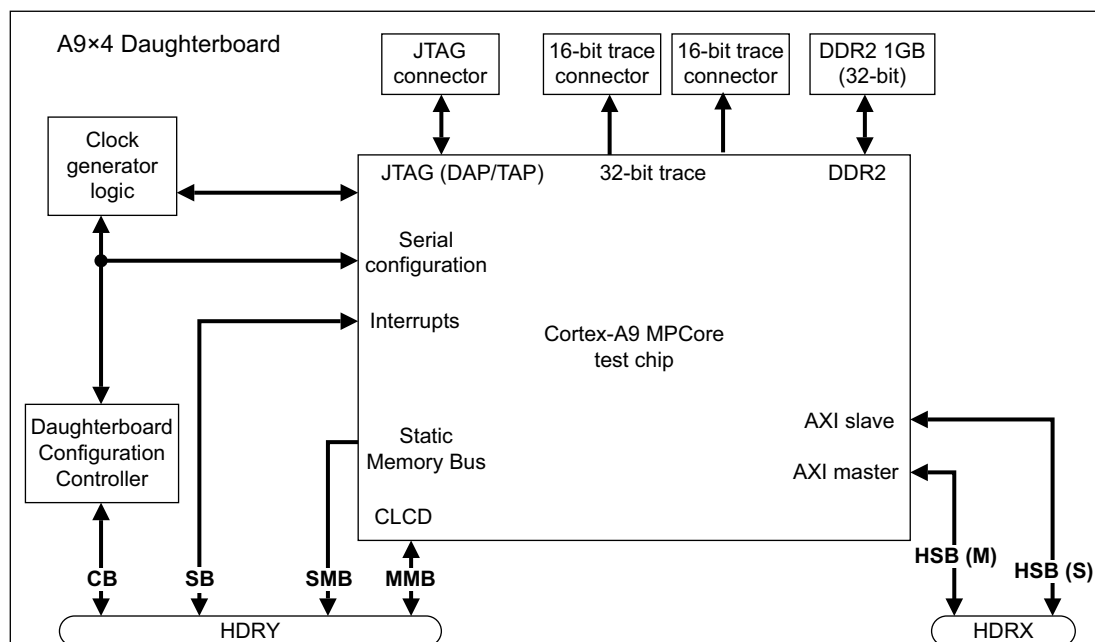
Figure 2-1 Daughterboard block diagram

The daughterboard contains the following devices and interfaces:

Cortex-A9 MPCore test chip

The test chip includes the following components and interfaces:

- Cortex-A9 quad-core MPCore processor.

- PL310 *Level 2 Cache Controller* (L2CC) consisting of 512KB of L2 unified cache.

- PL341 32-bit *Double Data Rate* 2 (DDR2) *Dynamic Memory Controller* (DMC) interface to the onboard 1GB SDRAM.

- PL354 32-bit *Static Memory Bus* (SMB) controller.

- PL111 24-bit *Color LCD* (CLCD) controller.

- *TrustZone Address Space Controller* (TZASC) and *TrustZone Protection Controller* (TZPC).

- Multiplexed 64-bit AXI master interface.

- Multiplexed 64-bit AXI slave interface.

- CoreSight debug and trace interface to the onboard connectors.

- Daughterboard Configuration Controller interface.

Daughterboard Configuration Controller

The *Daughterboard Configuration Controller* initiates, controls, and configures the test chip. The *Daughterboard Configuration Controller* interfaces with the Motherboard Express µATX.

A *Motherboard Configuration Controller* (MCC) on the Motherboard Express µATX configures the daughterboard and communicates with the *Daughterboard Configuration Controller* to configure the test chip.

DDR2 SDRAM

> The daughterboard provides 1GB of DDR2, 266MHz, memory.

CoreSight software debug and trace ports

> The daughterboard has a JTAG scan chain for processor and system debug that supports CoreSight JTAG DAP and SWD access.
>
> A 32-bit trace interface is provided through the standard dual 16-bit *Matched Impedance ConnecTOR* (MICTOR) connectors.

System interconnect buses

> The following external buses connect the Motherboard Express µATX and the CoreTile Express A9×4 daughterboard:
>
> - *System Bus* (SB) for interrupt and test chip control signals.
>
> - *Configuration Bus* (CB) from the motherboard System Configuration Controller to the Daughterboard Configuration Controller.
>
> - *Static Memory Bus* (SMB) from the test chip *Static Memory Controller* (SMC).
>
> - *MultiMedia Bus* (MMB) connects the CLCD signals to the connectors on the motherboard.
>
> - Two *High-Speed Buses* (HSBs), HSBM and HSBS, provide multiplexed AXI master and slave buses to an optional daughterboard on Site 2.

——— **Note** ———

Application Note 224, Example Logic Tile Express 3MG design for a Core Tile Express A9×4, provided by ARM, implements an example AMBA system using the LogicTile Express 3MG daughterboard to interconnect with the CoreTile Express A9×4 daughterboard. See the documentation supplied on the accompanying media and the *Application Notes* listing for more information at http://infocenter.arm.com.

———

Figure 2-2 on page 2-4 shows the daughterboard system interconnect to the Motherboard Express µATX development system. For more information on the global interconnect scheme, see the *Motherboard Express µATX Technical Reference Manual*.

——— **Note** ———

CoreTile Express A9×4 does not support PCI Express.

———
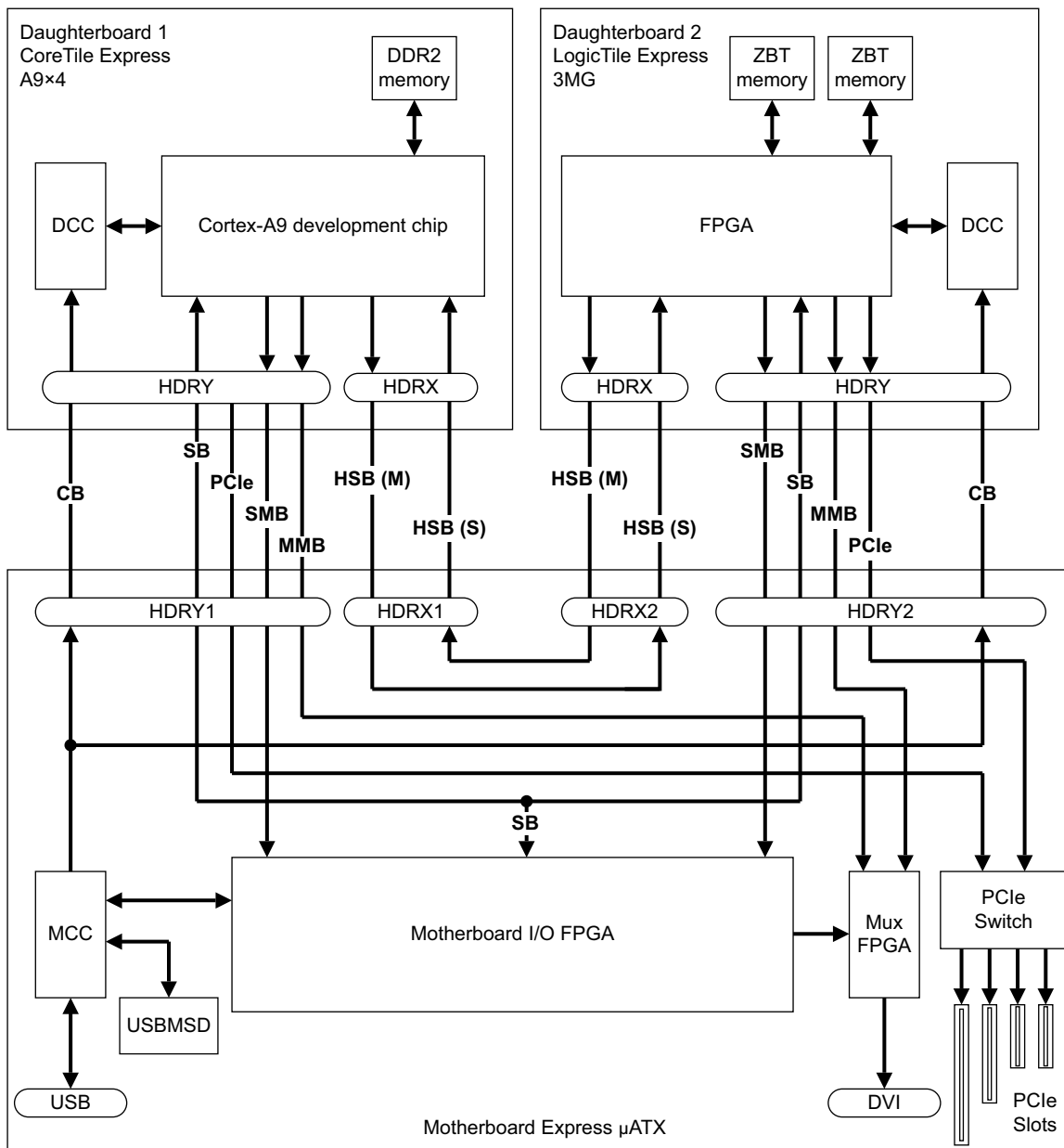
Figure 2-2 System connect example with optional LogicTile Express 3MG daughterboard

2.2   Cortex-A9 MPCore test chip

Figure 2-3 shows the main components of the test chip.
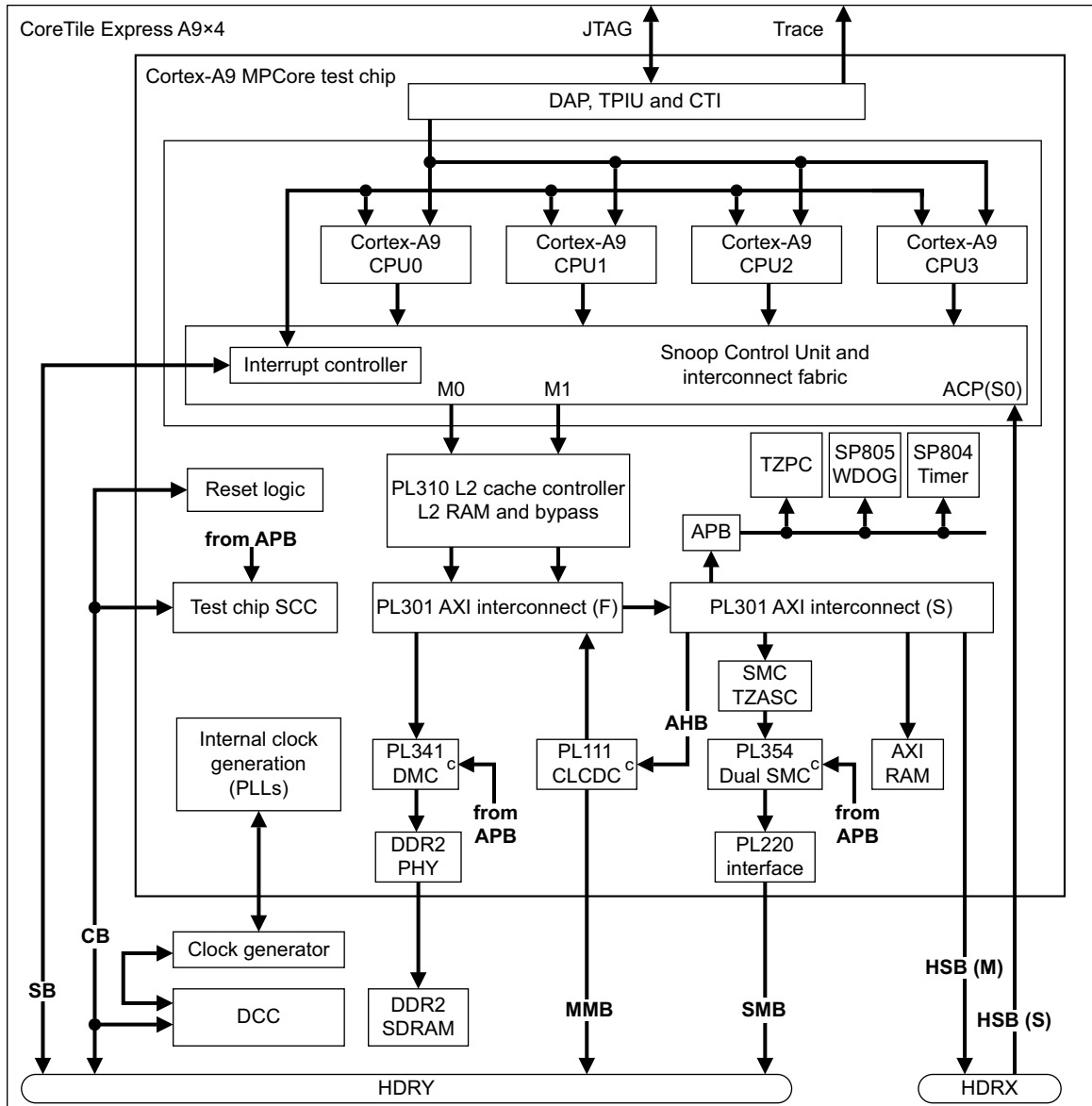
Figure 2-3 Top-level view of the test chip components

2.3　System interconnect signals

This section gives an overview of the signals present on the header connectors. The signals are:

- 32-bit *Static Memory Bus* (SMB) to Motherboard Express μATX.

- 24-bit *MultiMedia Bus* (MMB) for video from the Cortex-A9 MPCore test chip CLCD controller to the motherboard connector.

- 64-bit multiplexed AXI bus, HSB (S), from the external AXI master on a daughterboard in Site 2 to the Cortex-A9 *Snoop Control Unit* (SCU), *Accelerator Coherency Port* (ACP).

- 64-bit multiplexed AXI bus, HSB (M), to the external AXI slave on a daughterboard in Site 2.

- *System Bus* (SB) with control signals from the motherboard. This includes the external interrupts from the motherboard to the test chip.

- *Configuration Bus* (CB) between the *Daughterboard Configuration Controller* and the *System Configuration Controller* (SCC) on the motherboard.

——— **Note** ———

- The **AxUSER** signals on the HSB(S) port into the ACP port are fixed at 0. The SCU interprets all incoming AXI transactions as NON-SHARED so that there is no coherency between an external master and the Cortex-A9 MPCore L1 caches.

- For information about the multiplexing scheme for the AXI buses, see Appendix A *Signal Descriptions*.

———————

2.4 Powerup configuration and resets

This section describes the daughterboard powerup configuration and resets. It contains the following subsections:

- *Powerup configuration*
- *Resets*.

2.4.1 Powerup configuration

You can set the values for the daughterboard external reference clocks OSC0, OSC1, and OSC2, and the test chip *Serial Configuration Controller* (SCC) registers before reset by editing the `board.txt` configuration file. The CoreTile Express A9×4 daughterboard is in Site 1, so use the `board.txt` file in the `SITE1/HBI0191B` or the `SITE1/HBI0191C` directory.

——— **Note** ———

Use the directory that corresponds the version of your CoreTile Express A9×4 daughterboard.

For more information on system configuration and resets, see *ARM® Versatile™ Express Configuration Technical Reference Manual*.

——— **Caution** ———

ARM recommends that you use the `config.txt` and `board.txt` files for all system configuration. *Programmable peripherals and interfaces* on page 3-6, however, describes registers that directly modify the test chip configuration.

2.4.2 Resets

The *Daughterboard Configuration Controller* controls and sequences resets to the test chip in response to requests from the motherboard MCC as a result of, for example, pressing the motherboard reset push button.

The *Daughterboard Configuration Controller* on the daughterboard manages resets signals between the motherboard and the test chip.

Table 2-1 shows the Cortex-A9 MPCore test chip reset sources.

Table 2-1 Reset sources

Reset source	Destination	Description
CB_nPOR	Test chip **nTCPORESET**	This is the powerup reset signal that resets the Cortex-A9 MPCore multiprocessor integer core, the AMBA subsystem, and the debug logic.
CB_nRST	Test chip **nSYSRESET**	This is a reset from the motherboard.
		This signal resets the Cortex-A9 MPCore multiprocessor integer core and the AMBA subsystem. It does not reset the debug logic.

Table 2-1 Reset sources (continued)

Reset source	Destination	Description
JTAG **nTRST**	Test chip **nTRST**	This is the test logic reset to the TAP controller and the *Daughterboard Configuration Controller*.
JTAG **nSRST**	motherboard MCC	If an external source asserts the JTAG **nSRST** signal, the daughterboard generates a reset request to the motherboard MCC. The motherboard hardware is reset and the MCC asserts **CB_nPOR** and **CB_nRST**.
		A configuration option in the config.txt file selects whether to generate both **CB_nPOR** and **CB_nRST**. See the *Motherboard Express µATX Technical Reference Manual*.
		nSRST remains LOW until the reset sequence completes.
Test Chips Watchdogs	Test chip internal **nTCPORRESET**	If the internal Test Chip watchdog timers are configured and trigger, they force an internal test chip **nTCPORRESET**.
		The external system components on the motherboard are not reset.

When power is applied to the board, the *Daughterboard Configuration Controller* also asserts and controls the following resets:

nPLLRESET   This resets the PLL clock generators in the test chip.

nCFGRESET   This reconfigures the test chip based on the values in the test chip configuration registers.

Figure 2-4 shows an overview of the resets.
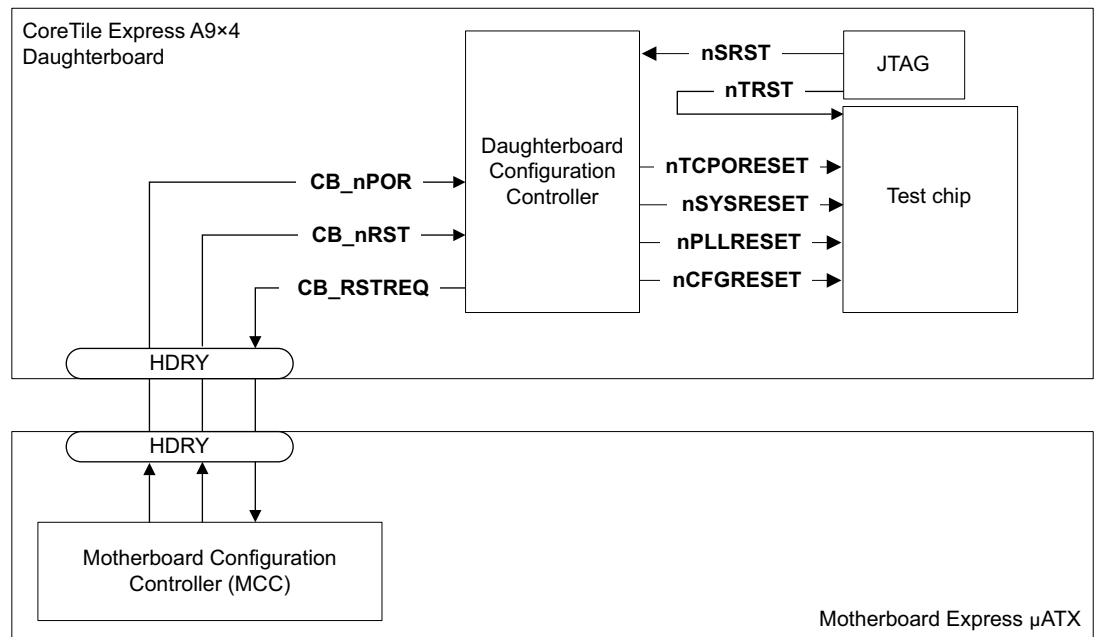
Figure 2-4 Reset overview

2.5 Clocks

This section describes the daughterboard clocks.

The daughterboard sends and receives clocks to and from the motherboard, and also generates local clocks. Figure 2-5 shows a functional overview of the daughterboard clocks and their connections to the other system components in a typical system configuration that includes a CoreTile Express A9×4 daughterboard.
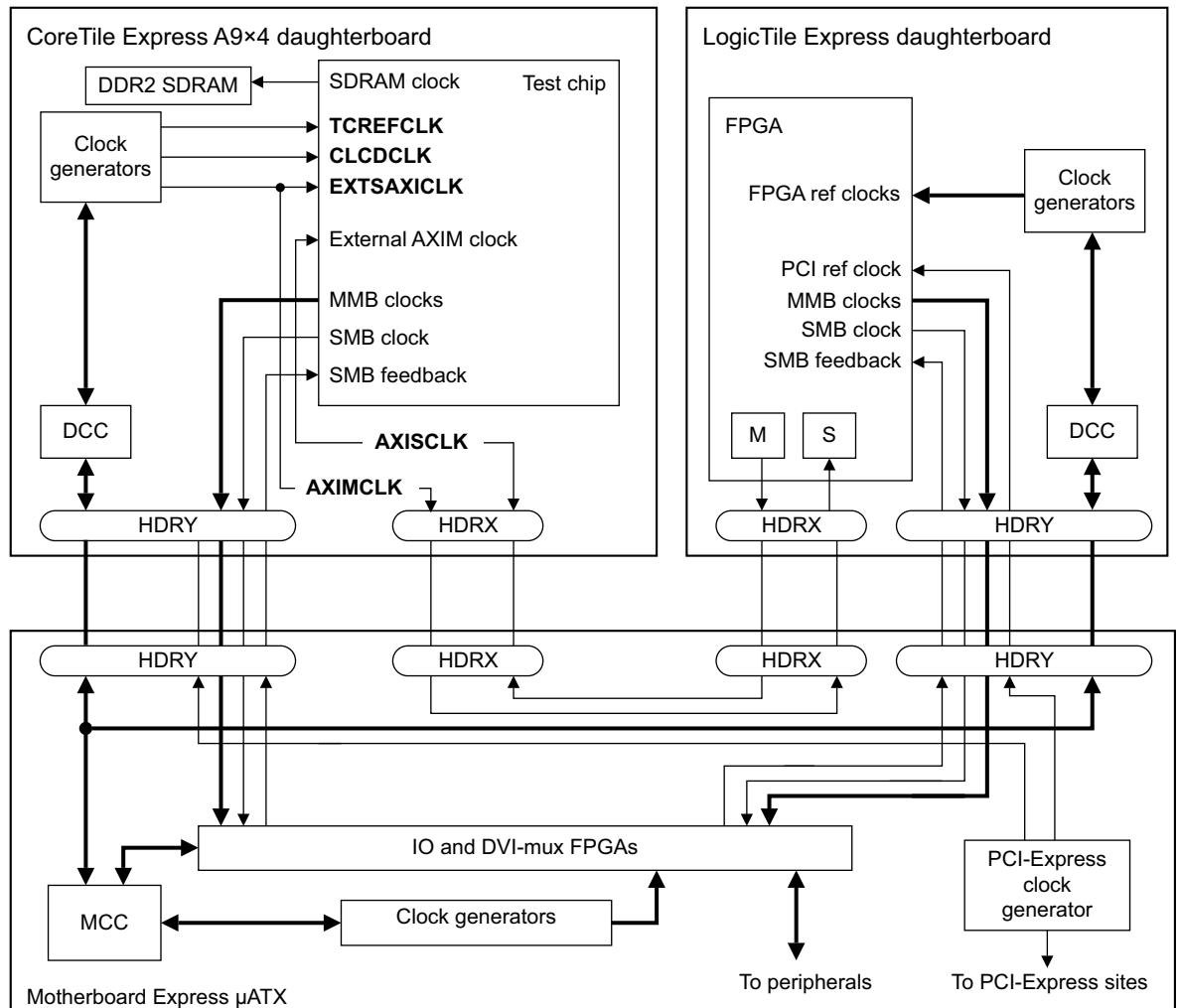
Figure 2-5 Clocks overview

─── **Note** ───

In the CoreTile Express A9×4 daughterboard, MMB clocks are generated from **CLCDCLK**, that originates from OSC1. See *PrimeCell Color LCD Controller, PL111* on page 3-7 and *Programmable clock generators*.

2.5.1 Programmable clock generators

The motherboard MCC uses the board.txt configuration file for the daughterboard to set the frequency of these clocks. For more information, see the *Motherboard Express µATX Technical Reference Manual*.

Example 2-1 shows an example of setting the frequencies for the programmable clocks in the board.txt file.

Example 2-1 Setting the daughterboard programmable clock generator values

```
[OSCCLKS]
TOTALOSCCLKS: 3                    ;Total Number of OSCCLKS
OSC0: 45.0                         ;OSC0 Frequency in MHz (EXTSAXICLK)
OSC1: 23.75                        ;OSC1 Frequency in MHz (CLCDCLK)
OSC2: 66.67                        ;OSC2 Frequency in MHz (TCREFCLK)
```

Table 2-2 shows the local daughterboard clocks generated by the programmable clock generators on the daughterboard.

Table 2-2 Daughterboard OSCCLK clock sources

Source	Function	Test chip signal	Frequency default, range	Description
OSC0	AXI	**EXTSAXICLK** and **AXIMCLK**	45MHz 30-50MHz	AMBA AXI ACLK clock to the AXI master port on the test chip and the AXI slave port on the LogicTile Express 3MG daughterboard.
OSC1	CLCDC	**CLCDCLK**	23.75MHz 10-80MHz	Reference clock for the CLCD controller in the test chip: • You must adjust the frequency of this clock to match your target screen resolution. • Different display resolutions require different data and synchronization timing. **OSCCLK1**, with 23.75MHz default, is assigned as **CLCDCLK** for the LCD controller. See the *PrimeCell Color LCD Controller (PL111) Technical Reference Manual* for a description of the LCD timing registers. See also *Display resolutions and display memory organization* on page 3-7.
OSC2	Test chip reference clock	**TCREFCLK**	66.67MHz	Reference clock for the test chip internal clock generators, PLLs, that produce the following clocks: • Cortex-A9 core. • DDR2. • Internal AXI infrastructure. ———— **Note** ———— ARM recommends that you do not change the frequency from the default value. ———————— • *Static Memory Bus* (SMB). See *Test chip SCC registers* on page 3-12.

The clock generators have an absolute accuracy of better than 1%. If you enter settings that cannot be precisely generated, the value is approximated to the nearest usable value.

2.5.2 Test chip clock generators

The test chip contains three clock *Phase Locked Loops* (PLLs) and dividers that use the **TCREFCLK** clock, from OSC2, to generate the clocks used by the internal systems on the test chip.

Table 2-3 shows the daughterboard clocks generated by the test chip PLLs.

Table 2-3 Test chip generated clocks

Clock	Frequency default, range	Description
MCLK	266MHz 100-266MHz	Clocks the memory side of the PL341 DDR2 controller. See *DMC User Configuration Register 0* on page 3-9. —— **Note** —— The default register settings for the PL341 enable operation with **MCLK** in the range 250-266MHz. If the **MCLK** frequency is outside this range, you must adjust the PL341 registers.
MCLK/2	133MHz 50-133MHz	Used internally by the DDR2 control logic. —— **Note** —— **MCLK**/2 must always be set to one half the **MCLK** frequency.
FAXI	200MHz maximum	Clocks the *fast* PL301 matrix and the higher-performance peripherals such as the DDR2 controller.
SAXI and **SMC_CLK0**	50MHz, defined by the motherboard	Clocks the *slow* PL301 matrix and components attached to it such as the SMC. The SMC accesses the motherboard peripherals so the minimum frequency is determined by the minimum-permitted frequency for peripherals on the motherboard SMB bus. See the *Motherboard Express μATX Technical Reference Manual*.
FCLK	400MHz maximum	Clocks the cores in the Cortex-A9 MPCore.

Each of the PLLs has two outputs as Figure 2-6 on page 2-12 shows.
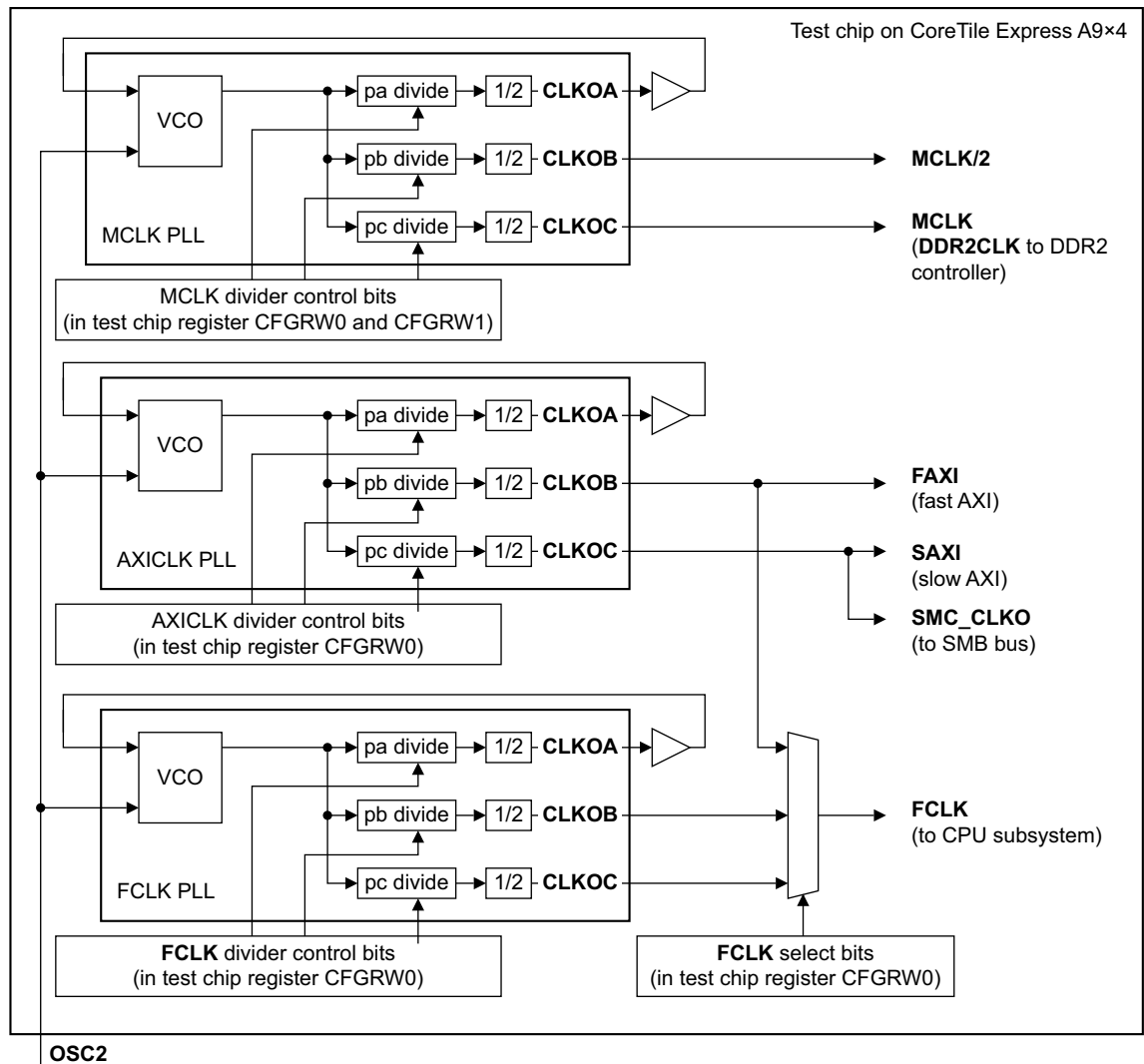
Figure 2-6 Test chip PLLs and clock divider logic

---------- **Note** ----------

- For more information on the SCC Test chip registers, see *Test chip SCC registers* on page 3-12.

- **FCLK** select bits are defined as Fclkselect in Table 3-9 on page 3-15.

For each PLL, the **CLK0B** output frequency is related to the divider input value as follows:

`CLKOB = OSC2 × (pa_divide+1)/(pb_divide+1)`

The same relationship applies for **CLKOC**:

`CLKOC = OSC2 × (pa_divide+1)/(pc_divide+1)`

---------- **Note** ----------

- The VCO output must be in the range 650-1340MHz. The VCO frequency is related to the divider input value as follows:

  `VCO = 2 × OSC2 × (pa_divide+1)`

- The ratio of **FAXI** to **SAXI** must be `n:1` where `n < 5`. The value of `n` can be incremented in half integer steps, for example, `1.5:1`.

- The ratio of **FCLK** to **FAXI** must be `n:1` where `n < 5`. The value of `n` can be incremented in half integer steps. For example, `1.5:1`.

- For more information on setting the values for the pa_divide, pb_divide, and pc_divide dividers for each of the PLLs, see *Test chip SCC registers* on page 3-12.

2.5.3 External clocks

Table 2-4 shows the external bus clocks generated by the motherboard and the optional daughterboard in Site 2:

Table 2-4 External clock sources

Function	Frequency default, range	Description
AXISCLK	30MHz, 33MHz maximum	This is the external clock from the second tile site. This connects to the AXI slave port of the test chip, the external AXIM clock. The test chip also uses an automatically generated double-rate clock to multiplex the AXI signals.
SMB feedback	Same as **SMB** clock	This is a skew-controlled version of the SMB clock sent from the motherboard to the SMC in the test chip. The test chip SMC uses this clock to adjust for optimum timing.

2.6 Interrupts

This section describes the daughterboard interrupts. It consists of the following subsections:

- *Overview of interrupts*
- *Test chip interrupts* on page 2-15.

2.6.1 Overview of interrupts

The *System Bus* (SB) carries the interrupt and control signals between the motherboard and the daughterboard. Figure 2-7 shows an overview of the interrupt signals between the daughterboard and the motherboard.
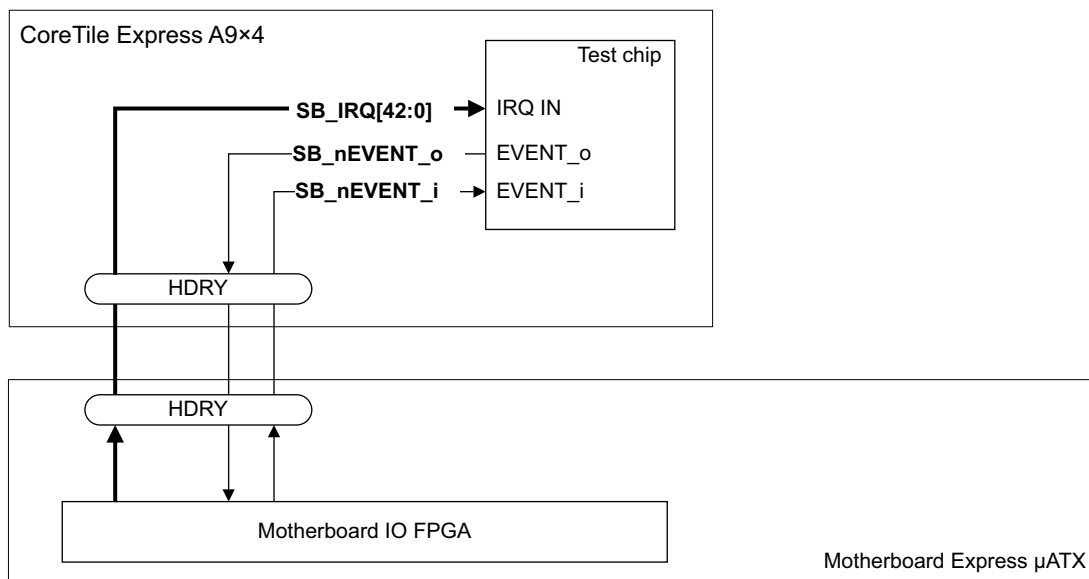
Figure 2-7 Interrupt overview

Table 2-5 shows the interrupt signals present on the SB.

Table 2-5 SB interrupt signals

Signal	Width	Direction	Description
SB_IRQ	43	Input	Interrupts from motherboard to test chip
SB_nEVENT_i	1	Input	To the motherboard IO FPGA, reserved for a processor wake-up event
SB_nEVENT_o	1	Output	From the motherboard IO FPGA, reserved for a processor wake-up event

The interrupt signals on the motherboard SB are directly connected to the interrupt controller in the Cortex-A9 MPCore test chip as Table 2-6 on page 2-15 shows.

2.6.2 Test chip interrupts

The Cortex-A9 MPCore test chip has an integrated interrupt controller that handles both external and internal interrupts. Table 2-6 shows the interrupts.

Table 2-6 Test chip interrupts

SB_IRQ[ ] interrupt from the motherboard	Test chip interrupt	Description
[42:0]	[74:32]	External interrupts from the motherboard. See the *Motherboard Express µATX Technical Reference Manual.*
[47:43]	-	Reserved. Not implemented on the daughterboard.
-	75	L2 cache controller interrupt.
-	76	CLCD interrupt.
-	77	SMC interface 0 interrupt.
-	78	SMC interface 1 interrupt.
-	79	NMC interface 0 interrupt.
-	80	System timer 0 interrupt.
-	81	System timer 1 interrupt.
-	82	Reserved.
-	83	System watchdog timer interrupt.
-	84	UART interrupt.
-	[91:85]	Reserved.
-	92	CPU0 Performance Monitor Unit interrupt.
-	93	CPU1 Performance Monitor Unit interrupt.
-	94	CPU2 Performance Monitor Unit interrupt.
-	95	CPU3 Performance Monitor Unit interrupt.

——— **Note** ———

• For more information on the motherboard peripherals that generate interrupts to the test chip, see the *Motherboard Express µATX Technical Reference Manual*.

• For more information about the internal processor interrupts, see the *Cortex-A9 MPCore Technical Reference Manual*.

2.7   Debug

You can attach a JTAG debugger to the daughterboard JTAG connector to execute programs to the daughterboard and debug them. For convenience, connect the cable from the rear panel JTAG connector to the daughterboard JTAG. For example, you can connect the RealView Debugger to this debug interface using an external RealView ICE interface box.

— Note —

The daughterboard does not support adaptive clocking. The **RTCK** signal is tied LOW on the JTAG ICE connector.

See Figure 1-1 on page 1-3 for the location of the JTAG ICE connector.

Figure 2-8 shows an overview of the CoreSight system.
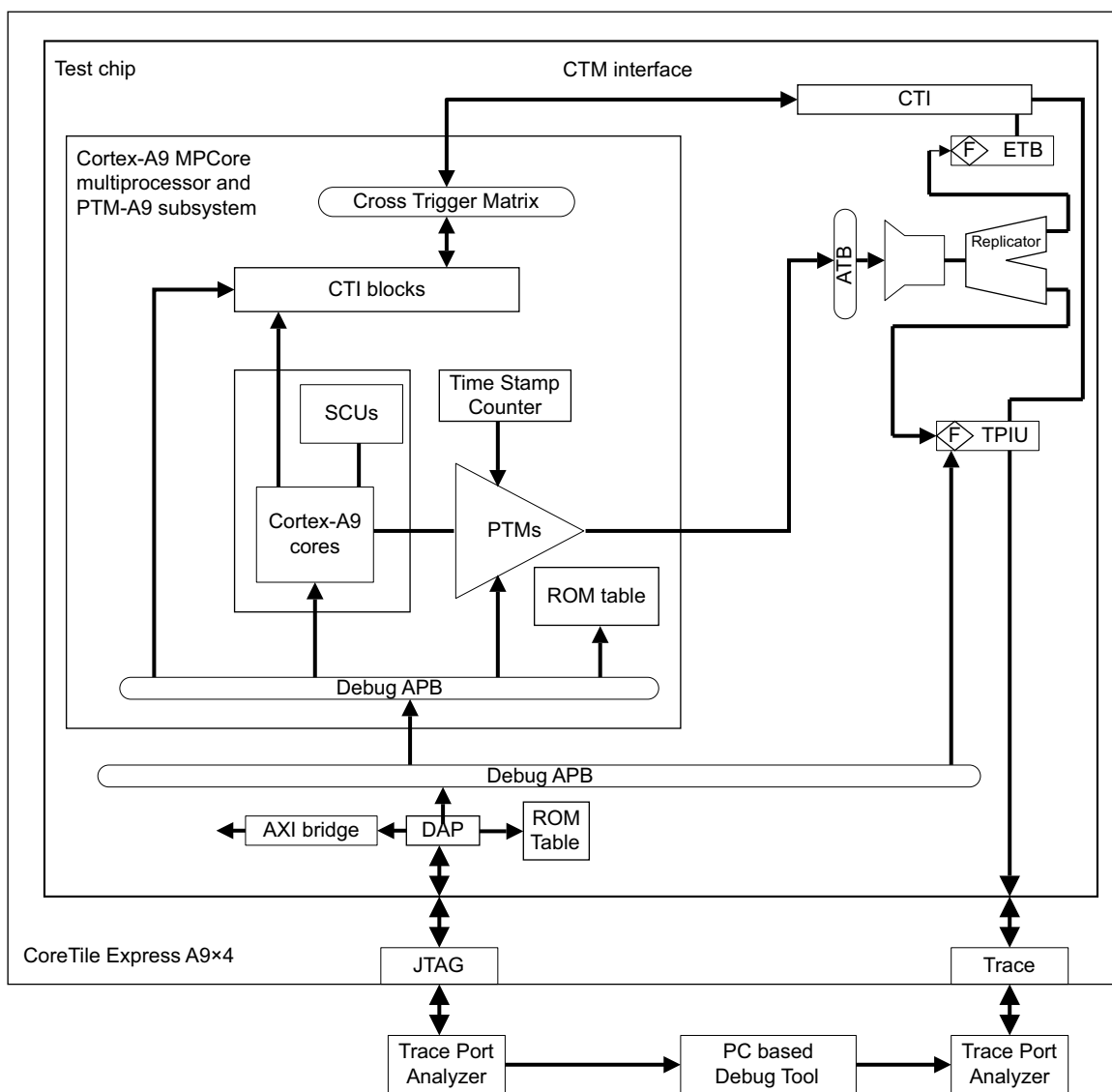
Figure 2-8 CoreSight and trace

The CoreSight debug system accesses the AXI subsystem through a bridge. The bridge includes a connection to the TZPC to enable the debug system to be treated as secure or non-secure.

For information on CoreSight components, see the *CoreSight Components Technical Reference Manual*.

For information on Cortex-A9 CoreSight PTM, see the *CoreSight PTM-A9 Technical Reference Manual*.

The daughterboard supports up to 32-bit trace in *continuous* mode. There are two MICTOR connectors for JTAG trace. See Figure 1-1 on page 1-3 for the location of these connectors.

To set up a trace connection to any of the cores on the test chip, it is necessary to know the funnel port number and PTM base address connection information associated with each core. Table 2-7 defines these addresses for each of the four cores on the test chip.

Table 2-7 Test chip trace connection addresses

Core	Core base address	Funnel port	PTM base address
Core 0	0x80110000	0	0x8011C000
Core 1	0x80112000	1	0x8011D000
Core 2	0x80114000	2	0x8011E000
Core 3	0x80116000	4	0x8011F000

2.8 Voltage, current, and power monitoring

The *Daughterboard Configuration Controller* on the daughterboard transmits voltage and current measurements for some of the supplies. The *Daughterboard Configuration Controller* transmits the measurements to the motherboard where they can be read from the SYS_CFGCTRL interface.

Table 2-8 shows the device numbers for the voltage supplies.

Table 2-8 Device numbers for voltage monitoring

Device	Voltage supply	Default voltage	Description
0	VD10	1.0 +/- 5%	Test Chip *System on Chip* (SoC) internal logic voltage.
1	VD10_S2	1.0 +/- 5%	PL310, L2 cache, RAM cell supply, not PL310 logic
2	VD10_S3	1.0 +/- 5%	Cortex-A9 system supply, Cores, MPEs, SCU, and PL310 logic
3	VCC1V8	1.8 +/- 5%	DDR2 SDRAM and Test Chip DDR2 I/O supply
4	DDR2VTT	0.9 +/- 5%	DDR2 SDRAM VTT termination voltage
5	VCC3V3	3.3 +/- 5%	Local board supply for miscellaneous logic external to the test chip.

Table 2-9 shows the device numbers for the current to the subsystems.

Table 2-9 Device numbers for current monitoring

Device	Voltage supply	Description
0	VD10_S2	Current measurement device for the PL310, L2 cache, SRAM cell supply, excluding other PL310 logic.
1	VD10_S3	Current measurement device for: the Cortex-A9 system supply including the following: • Cores. • MPEs. • SCU. • PL310 logic.

Table 2-10 shows the device numbers for power monitoring.

Table 2-10 Device numbers for power monitoring

Device	Voltage supply	Description
0	PVD10_S2	Power measurement device for the PL310, L2 cache, SRAM cell supply.
1	PVD10_S3	Power measurement device for the Cortex-A9 system supply.

See the *Motherboard Express µATX Technical Reference Manual* for more information on the SYS_CFGCTRL registers.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About this programmers model

The following information applies to the CoreTile Express A9×4 daughterboard registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.

- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.

- Unless otherwise stated in the accompanying text:
    — Do not modify undefined register bits.
    — Ignore undefined register bits on reads.
    — All register bits are reset to a logic 0 by a system or powerup reset.

- Access type in Table 3-3 on page 3-9 and Table 3-8 on page 3-14 are described as:
    RW   Read and write.
    RO   Read-only.
    WO   Write-only.

3.2   Daughterboard memory map

Figure 3-1 shows the daughterboard memory map.
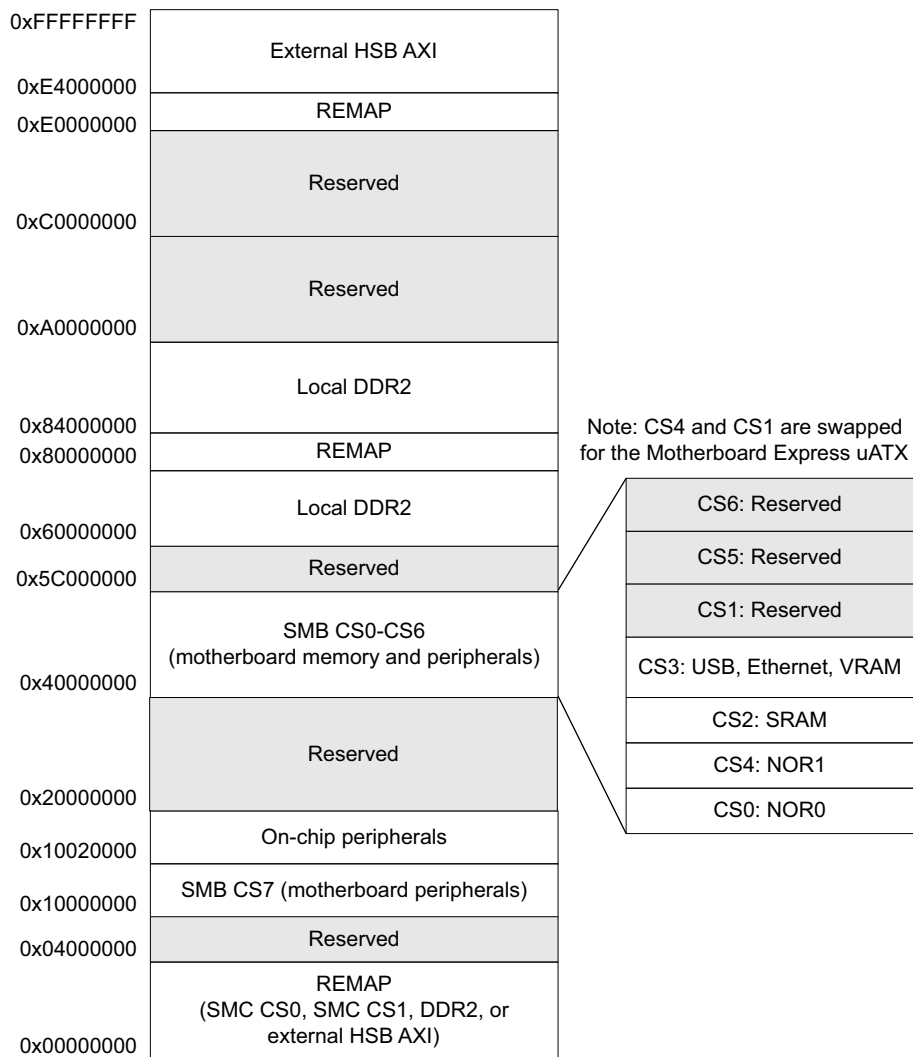
Figure 3-1 Daughterboard memory map

For information about peripherals on SMC CS7, see the *Motherboard Express µATX Technical Reference Manual*.

Table 3-1 shows the daughterboard peripheral interfaces.

Table 3-1 Peripheral memory map

Address range	Size	Description
0xE000_0000–0xFFFF_FFFF	512MB	External AXI between daughterboards
0xA000_0000–0xDFFF_FFFF	1GB	Daughterboard, private
0x8000_0000–0x9FFF_FFFF	512MB	Local DDR2
0x8000_0000–0x81FF_FFFF	64MB	Remappable memory location
0x6000_0000–0x7FFF_FFFF	512MB	Local DDR2 lower

Table 3-1 Peripheral memory map (continued)

Address range	Size	Description
0x5C00-0000-0x5FFF_FFFF	64MB	Reserved
0x4000_0000-0x5BFF_FFFF	448MB	Motherboard peripherals, typically, memory devices
0x2000_0000-0x3FFF_FFFF	512MB	Reserved
0x1002_0000-0x1FFF_FFFF	~256MB	Daughterboard, private
0x1000_0000-0x1001_FFFF	128KB	Motherboard peripherals, CS7
0x0000_0000-0x0FFF_FFFF	64MB	Remappable memory section

3.2.1 Remapping memory

You can configure remapping before or after powerup:

Remapping at powerup

Use the board.txt file if the remap option is required when the processor starts from a reset. The SCC: 0x0004 entry in the board.txt file controls the setting for the SCC register CFGRW1. See *Powerup configuration* on page 2-7.

Remapping at run time

Write directly to the SCC register CFGRW1 to change remapping after powerup. See *Test chip SCC Register 1* on page 3-15. See the Boot Monitor sys_boot.s file for an example of reconfiguring while running.

——— **Caution** ———

ARM recommends that you use the configuration file rather than directly writing to the control registers.

You can change the remap bits at runtime by writing to the Cortex-A9 MPCore SCC register CFGRW1, bits [30:28]. This configures which memory device is addressed at address 0x0. The processor fetches its first instructions from address 0x0, but the actual memory read depends on the remapped memory region.

The remap region is 64MB in size. Table 3-2 shows the four remap regions of the Cortex-A9 MPCore test chip.

You can remap the first 64MB of the memory maps from address 0x00 to the regions that Table 3-2 shows. The default value for the remap bits is 000.

Table 3-2 Remap regions

Remap bits	Remap region	Remapped address	Description
000	0x00000000–0x00FFFFFF	0x40000000 - 0x40FFFFFF	CS0 SMC to 0x0, first 16MB
001	0x00000000–0x00FFFFFF	0x44000000 - 0x44FFFFFF	CS4 SMC to 0x0, first 16MB
010	0x00000000–0x03FFFFFF	0xE0000000 - 0xE4000000	External AXI to 0x0, first 64MB
100	0x00000000–0x03FFFFFF	0x800000000 - 0x83FFFFFF	DDR2 to 0x0, first 64MB

3.2.2 Overview of the memory map for the on-chip peripherals

Figure 3-2 shows the on-chip peripheral memory map.

0x1E00B000	Reserved	Reserved	0x10320000
0x1E00A000	L2CC config (PL310)	PTM3	0x1031F000
0x1E002000	Reserved	PTM2	0x1031E000
0x1E000000	Cortex-A9 MPCore (SCU) private memory region	PTM1	0x1031D000
0x10400000	Reserved	PTM0	0x1031C000
0x10200000	CoreSight debug APB	CTI3	0x1031B000
0x100ED000	Reserved	CTI2	0x1031A000
0x100EC000	SMC_TZASC	CTI1	0x10319000
0x100EB000	Reserved	CTI0	0x10318000
0x100EA000	'Slow' AXI matrix (PL301)	PMU3	0x10317000
0x100E9000	'Fast' AXI matrix (PL301)	CoreDbg3	0x10316000
0x100E8000	Reserved	PMU2	0x10315000
0x100E7000	Reserved	CoreDbg2	0x10314000
0x100E6000	TrustZone Protection Controller (BP147)	PMU1	0x10313000
0x100E5000	Watchdog module (SP805)	CoreDbg1	0x10312000
0x100E4000	Dual Timer module (SP804)	PMU0	0x10311000
0x100E3000	Reserved	CoreDbg0	0x10310000
0x100E2000	System Configuration Controller	Reserved	0x10301000
0x100E1000	Static Memory Controller (PL354)	Debug ROM	0x10300000
0x100E0000	Dynamic Memory Controller (PL341)	Reserved	
0x10060000	AXI RAM (2KB)		0x10207000
0x10030000	Reserved	SWO	0x10206000
0x10020000	CLCDC configuration registers (PL111)	Reserved	0x10205000
		Funnel	0x10204000
		TPIU	0x10203000
		CTI	0x10202000
		ETB	0x10201000
		DAP ROM	0x10200000

Figure 3-2 On-chip peripheral memory map

— **Note** —

For more information about the Cortex-A9 MPCore private memory region, see the description of the PERIPHBASE configuration signals in the *ARM® Cortex®-A9 MPCore Technical Reference Manual.*

— **Note** —

The terms *Slow* and *Fast* for the AXI PL301 describe the type of devices on the bus rather than the AXI clocks. Both controllers are standard PL301 controllers:

• The *Fast* controller interfaces to the high-performance peripherals such as the DMC.

• The *Slow* controller interfaces to the low-speed devices on the test chip such as the onboard configuration controller.

3.3 Programmable peripherals and interfaces

The following sections describe the configurable modules in the test chip:

See also the reference manual for the individual peripheral for more information on programming these devices.

3.3.1 PrimeCell slow AXI interconnect (PL301)

The configuration interface for this component is located at address `0x100E9000` on the system APB bus. The slow AXI interconnect provides the link to the APB subsystem.

See the *PrimeCell High-Performance Matrix (PL301) Technical Reference Manual* for more information.

You can set the AXI clock in the configuration file or in the test chip configuration registers. See *Test chip SCC registers* on page 3-12.

———— **Note** ————

The AXI PL301 has standard PL301 *Fast* and *Slow* controllers:

- The *Fast* controller interfaces to the high-performance peripherals such as the DMC.

- The *Slow* controller interfaces to the low-speed devices on the test chip such as the onboard configuration controller and the memory interface to the SMC.

3.3.2 PrimeCell fast AXI interconnect, PL301

The configuration interface for this component is located at address `0x100EA000` on the system APB bus. The fast AXI interconnect provides a bridge to the slow AXI subsystem.

See the *PrimeCell High-Performance Matrix (PL301) Technical Reference Manual* for more information.

You can set the AXI clock in the configuration file or in the test chip configuration registers. See *Test chip SCC registers* on page 3-12.

3.3.3 Cortex-A9 MPCore multiprocessor

The Cortex-A9 MPCore test chip consists of a Cortex-A9 MPCore multiprocessor that includes four Cortex-A9 CPUs with NEON™ media processing technology. The L1 memory subsystem has 32KB of instruction cache and 32KB of data cache for each CPU.

The multiprocessor contains the following programmable devices:

- Snoop Control Unit.
- Interrupt controller.
- Interrupt distributor.
- Global timer.
- Private timers and watchdog.

For information about the programmable devices within the Cortex-A9 MPCore processor, see the *ARM® Cortex®-A9 MPCore Technical Reference Manual*.

3.3.4 PrimeCell Color LCD Controller, PL111

The configuration for the color LCD controller is as follows:

- There is a 64-bit master AHB interface to access the frame buffers.

- The color LCD controller configuration register has 4KB of address space. This page is located at address `0x10020000`.

- The color LCD controller runs on its own external clock (OSC1) and communicates with the FACLK domain. See *Programmable clock generators* on page 2-9 for more information on setting the clock frequency.

See the *PrimeCell Color LCD Controller (PL111) Technical Reference Manual*.

Display resolutions and display memory organization

Different display resolutions require different data and synchronization timing. Use registers CLCD_TIM0, CLCD_TIM1, CLCD_TIM2, and OSCCLK1 to define the display timings.

The mapping of the 32 bits of pixel data in memory to the RGB display signals depends on the resolution and display mode.

For information on setting the red, green, and blue brightness for direct, non-palettized, 24-bit and 16-bit color modes, see the *ARM® PrimeCell Color LCD (PL111) Technical Reference Manual*. Selftest example code, that displays 24-bit and 16-bit VGA images, is also provided on the accompanying DVD.

——— **Note** ———

For resolutions based on one to sixteen bits per pixel, multiple pixels are encoded into each 32-bit word.

All monochrome modes, and color modes using eight or fewer bits per pixel, use the palette to encode the color value from the data bits. See the *ARM® PrimeCell Color LCD (PL111) Technical Reference Manual* for information.

The interface through the V2M-P1 motherboard has been tested at 800 x 600 x 16-bit with a static color chart. However, practical resolution and color depth depend on available bus bandwidth. If a CLCDC in a daughterboard is the video source, the actual resolution range depends on the daughterboard CLCDC.

3.3.5 L2 cache controller, PL310

The configuration for the L2 cache controller is as follows:

- The L2 memory consists of 512KB of L2 unified cache. You can change the actual amount of L2 memory used by writing to the L2 control registers.

- The L2 cache controller does not use parity.

- Address filtering is supported.

- *Intelligent Energy Management* (IEM) support is not provided.

- The L2 control register has 4KB of memory space. This page is located at address `0x1E00A000`.

- The L2 cache controller and the Cortex-A9 MPCore multiprocessor are synchronous. L2 cache operates at the core frequency and **FCLK** drives it.

- The L2 RAM operates at half the controller frequency. The controller generates the clocking for the RAM.

- You can enable the L2 cache controller using the L2 control register. The L2 cache is disabled by default.

- You can completely bypass the L2 cache controller, effectively removing the cache controller from the system, by enabling the Enable L2CC Bypass bit. This bit 12 of the SCC CFGRW1 register. See Table 3-10 on page 3-16.

See the *PrimeCell Level 2 Cache Controller (PL310) Technical Reference Manual*.

3.3.6 Dual-Timer module, SP804

This component is located at address `0x100E4000` on the system APB.

See the *ARM® Dual-Timer Module (SP804) Technical Reference Manual* for more information.

3.3.7 PrimeCell DDR2 DMC interface, PL341

The configuration for the DDR2 DMC interface in the test chip is as follows:

- 64-bit AXI data width and 32-bit external bus width.

- The DDR2 DMC configuration register has 4KB of address space. This page is located at address `0x100E0000`.

- The PL341 AXI interface runs synchronously at the frequency of the fast AXI interconnect, PL301. The external memory interface for the DDR2 memory devices runs asynchronously at the frequency that the test chip MCLK PLL defines. See *Test chip SCC registers* on page 3-12 for information about how to define the MCLK frequency from the `board.txt` file.

- Arbitration FIFO depth of 16 stages.

- Read data FIFO depth of 20 stages.

- Write data FIFO depth of 20 stages.

- Two exclusive access monitors.

See the *PrimeCell DDR2 Dynamic Memory Controller (PL341) Technical Reference Manual* for more information.

——— **Note** ———

The DDR2 Dynamic Memory Controller settings typically do not require user adjustment.

The user configuration registers implement specific DDR2 PHY signals. For software configuration information, see the following file:

`\BootMonitor\Firmware\Platform\Source\sys_dmc_v2p_ca9.s`.

You must set the values as this section describes. Table 3-3 provides cross references to individual registers:

Table 3-3 DMC, PL341, register summary

Offset	Name	Type	Configuration value	Description
0x100E0000+0x304	user_config0	WO	0x7C924924	This value must be written to the register during DMC initialization. See *DMC User Configuration Register 0*.
0x100E0000+0x308	user_config1	WO	0x008A28A2	This is the default value for the register. See *DMC User Configuration Register 1* on page 3-10.
0x100E0000+0x310	user_config2	WO	-	See *DMC User Configuration Register 2* on page 3-10.
0x100E0000+0x300	user_status	RO	0x0	See *DMC User Status Register* on page 3-11.

See also *ARM® Versatile™ Express Boot Monitor Technical Reference Manual*.

DMC User Configuration Register 0

The user_config0 Register characteristics are:

Purpose   Sets board-specific values for the DDR2 interface.

> **Note**
>
> The register is write-only. Reading the register returns an undefined value.

Usage constraints   Use only the values in Table 3-3 for the reserved bits. That is, everything except the UDLFSL field in bits [26:24]. The correct values are written to the register at PL341 configuration.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-3.

Figure 3-3 shows the bit assignments.
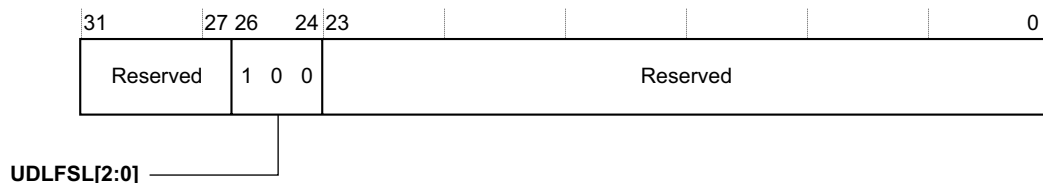
Figure 3-3 user_config0 Register bit assignments

Table 3-4 shows the bit assignments.

Table 3-4 DMC user_config0 Register bit assignments

Bits	Name	Function
[31:27]	-	Reserved. Use only the values in Table 3-3 on page 3-9.
[26:24]	UDLFSL	Maps to the DDR2 memory interface **UDLFSL[2:0]** bus to select the operating range for **MCLK**: b100 For 250-266MHz. b101 For 214-250MHz. b110 For 200-214MHz. b111 For 125-200MHz.
[23:0]	-	Reserved. Use only the values in Table 3-3 on page 3-9.

DMC User Configuration Register 1

The user_config1 Register characteristics are:

Purpose   Sets board-specific values for the DDR2 interface.

_____ **Note** _____

The register is write-only. Reading the register returns an undefined value.

Usage constraints   Use only the values in Table 3-3 on page 3-9 for the reserved bits.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-3 on page 3-9.

Table 3-5 shows the bit assignments.

Table 3-5 DMC user_config1 Register bit assignments

Bits	Name	Function
[31:0]	-	Reserved. Use only the values in Table 3-3 on page 3-9. Read as zero.

DMC User Configuration Register 2

The user_config2 Register characteristics are:

Purpose   Sets board-specific values for the DDR2 interface.

_____ **Note** _____

The register is write-only. Reading the register returns an undefined value.

Usage constraints   Use only the values in Table 3-3 on page 3-9 for the reserved bits.

The register must be programmed in a specific sequence and with a restricted range of values.

See the `BootMonitor\Firmware\Platform\Source\sys_dmc_v2p_ca9.s` Boot Monitor file for an example of how to configure this register.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-3 on page 3-9.

Table 3-6 shows the bit assignments.

Table 3-6 DMC user_config2 Register bit assignments

Bits	Name	Function
[31:0]	-	Reserved. Use only the values in Table 3-3 on page 3-9.

DMC User Status Register

The user_status Register characteristics are:

Purpose   This 16-bit register indicates the state of the DDR2 interface. Use the Boot Monitor to access the DMC status.

Usage constraints   This register is used in a specific sequence and with a restricted range of values.

See the `BootMonitor\Firmware\Platform\Source\sys_dmc_v2p_ca9.s` Boot Monitor file for an example of configuring this register

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-3 on page 3-9.

Table 3-7 show the bit assignments.

Table 3-7 DMC user_status Register bit assignments

Bits	Name	Function
[15:0]	-	Reserved. Do not modify. Read as zero.

3.3.8 PrimeCell SMC dual SRAM memory interface, PL354

This section contains information about the PrimeCell SMC dual SRAM memory interface in the following subsections:

- *SMC organization*
- *SMC Configuration* on page 3-12
- *TZASC configuration* on page 3-12
- *PrimeCell External Bus Interface, PL220* on page 3-12.

SMC organization

The SMC accesses devices using the following chip selects:

CS[0]and [4]   NOR flash on the motherboard.

CS[1]   Reserved for the motherboard.

CS2   SRAM on the motherboard.

CS3   Memory-mapped Ethernet and USB controllers on the motherboard.

CS[6:5]   Memory-mapped peripherals.

CS7   System memory-mapped peripherals on the motherboard.

SMC Configuration

The configuration for the dual SRAM memory interface is as follows:

- 64-bit AXI data width and 32-bit memory data width.

- Four chip selects on each interface.

- The dual SRAM memory interface configuration register has 4KB of address space. This page is located at address `0x100E7000`.

- TrustZone support, if enabled, is implemented using the *TrustZone Address Space Controller* (TZASC) component:
    — The TZASC configuration port is located at address `0x100EC000`.
    — The TZASC supports 16 regions.
    — The TZASC transaction depth is the same as the SMC.
    — The *TrustZone Protection Controller* (TZPC) controls the configuration enable bit of the ASC.

    See *TrustZone protection controller* on page 3-17.

- The dual SRAM memory interface is in the SAXI clock domain and is synchronous to the **FCLK** and **FACLK** domains.

See the *PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual* for more information.

TZASC configuration

The TZASC supports 16 memory protection regions for the SMC dual SRAM memory interface. The TZASC must be explicitly enabled by writing the appropriate serial configuration data prior to reset.

PrimeCell External Bus Interface, PL220

A PL220 *External Bus Interface* (EBI) is used to multiplex the dual SRAM memory interface to reduce pin count and to facilitate board layout.

See the *PrimeCell External Bus Interface (PL220) Technical Reference Manual* for more information.

3.3.9 Test chip SCC registers

The SCC in the test chip is an IP block that only configures the test chip. After reset, you read the configuration data from the test chip registers.

The MCC on the motherboard reads the `config.txt` and `board.txt` configuration files and uses the *Daughterboard Configuration Controller* to configure the motherboard and attached daughterboards. The *Daughterboard Configuration Controller* loads some of the registers in the test chip SCC.

——— **Note** ———

ARM recommends that, where possible, you perform all system configuration by loading configuration files into the flash memory on the motherboard rather than writing directly to the test chip controller. The settings in the `board.txt` file are applied to the daughterboard before reset is released.

Configuration values in the `board.txt` **file**

The test chip system configuration registers are set in the `board.txt` file by specifying SCC offsets and values to the register as Example 3-1 shows.

Example 3-1 Setting the test chip configuration register values from board.txt

```
[SCC REGISTERS]
TOTALSCCS: 3
SCC: 0x000 0xBB8A802A          ; CFGRW0 Powerup settings - MCLK, AXICLKs, FCLK PLL configuration
SCC: 0x004 0x00001F09          ; CFGRW1 Powerup settings - Remap bits, A9 static signals, MCLK PLL
SCC: 0x008 0x00000000          ; CFGRW2 Powerup settings - Misc, A9 static signals
```

The offset value selects one of the test chip SCC registers that Table 3-8 on page 3-14 shows.

The `board.txt` file might also contain alternative values for the registers that have been commented out as Example 3-2 shows.

Example 3-2 Alternative values for test chip configuration registers

```
; Alternative clock options
;
; To use these values, copy the SCC: line and replace the lines in the [SCC REGISTERS] section
; above. Do not place comments between the [SCC registers] and the last SCC: line.
; Normal : FCLK = 400, FAXI=200, SAXI = 50, MCLK = 275 ; @ OSC2 = 50 Mhz - vco = 800/1100
;SCC: 0x000 0xBB8A802A
;SCC: 0x004 0x00001F09
; Slow   : FCLK = 80, FAXI=80, SAXI = 40, MCLK = 160 ; @ OSC2 = 40 Mhz
;SCC: 0x000 0xCFBF8A3C
;SCC: 0x004 0x00001F09
```

Interface to test chip SCC

You can read and write the test-chip SCC registers:

* The interface supports word writes to the configuration controller registers.

* Writes to read-only registers are ignored.

* Writes to unused words fail. ARM recommends that you use a read-modify-write sequence to update the configuration controller registers.

* Read accesses to the peripheral support reading back 32 bits of the register at a time.

* Reads from unused words in the register return zero.

Table 3-8 shows the configuration registers and corresponding board.txt entries.

Table 3-8 Test chip SCC register summary

Entry in board.txt	Test chip register	Type	Reset	Description
SCC: 0x000	CFGRW0	RW	0xBB8A802A	PLL settings for MCLK, FAXI, SAXI, and FCLK. See *Test chip SCC Register 0*.
SCC: 0x004	CFGRW1	RW	0x00001F09	Remap, PLL settings for MCLK, and miscellaneous test chip settings. See *Test chip SCC Register 1* on page 3-15.
SCC: 0x008	CFGRW2	RW	0x00000000	Miscellaneous boot-option settings. See*Test chip SCC Register 2* on page 3-17.

Test chip SCC Register 0

The CFGRW0 Register characteristics are:

Purpose   Enables you to configure the internal PLLs settings to adjust frequency of:

- The test chip DDR2 clock, **MCLK**.
- AXI fabric clocks, **FAXI** and **SAXI**.
- The Cortex-A9 Core clock, **FCLK**.

For information about the relationship between the divider settings and the output frequency, see *Test chip clock generators* on page 2-11.

——— **Caution** ———

Changing the test chip PLL values can result in out-of-range clock frequencies that might cause unreliable operation.

In extreme cases, high-frequency clocks can cause the test chip to overheat and be permanently damaged.

——————

Usage constraints   There are no usage constraints.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-8.

Figure 3-4 shows the bit assignments.
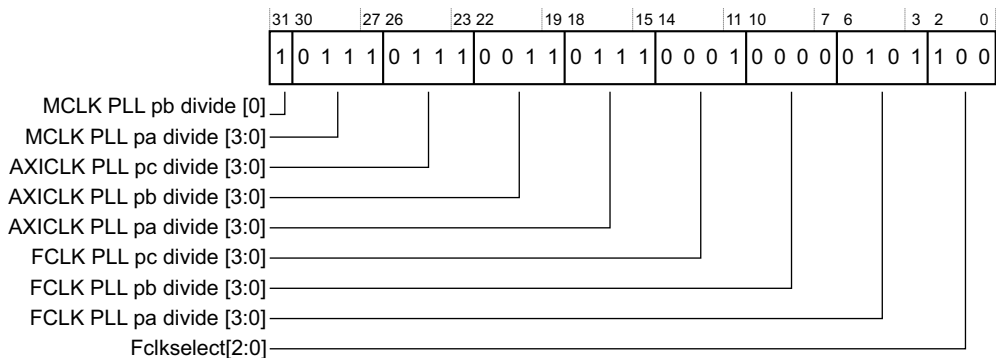
Figure 3-4 Test chip CFGRW0 Register bit assignments

Table 3-9 show the bit assignments.

Table 3-9 Test chip CFGRW0 Register bit assignments

Bits	Name	Function
[31]	MCLK PLL pb divide	Maps to **MCLK PLL pb divide[0]** of the **MCLK PLL pb divide[3:0]** bus. See Table 3-10 on page 3-16 for the remaining signal lines.
[30:27]	MCLK PLL pa divide	Maps to the **MCLK PLL pa divide[3:0]** bus.
[26:23]	AXICLK PLL pc divide	Maps to the **AXICLK PLL pc divide[3:0]** bus.
[22:19]	AXICLK PLL pb divide	Maps to the **AXICLK PLL pb divide[3:0]** bus.
[18:15]	AXICLK PLL pa divide	Maps to the **AXICLK PLL pa divide[3:0]** bus.
[14:11]	FCLK PLL pc divide	Maps to the **FCLK PLL pc divide[3:0]** bus.
[10:7]	FCLK PLL pb divide	Maps to the **FCLK PLL pb divide[3:0]** bus.
[6:3]	FCLK PLL pa divide	Maps to the **FCLK PLL pa divide[3:0]** bus.
[2:0][a]	Fclkselect	Defines the **FCLK** select bits that Figure 2-6 on page 2-12 shows. Maps to the **Fclkselect[2:0]** bus. You must select one of the following: **Fclkselect[0]** PLL **CLKOB**. **Fclkselect[1]** PLL **CLKOC**. **Fclkselect[2]** **FACLK.**

a. These bits have read and write access. The remainder of the register bits are read-only from the APB interface.

Test chip SCC Register 1

The CFGRW1 Register characteristics are:

Purpose   Enables you to read and write test chip configuration settings.

Usage constraints   There are no usage constraints.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-8 on page 3-14.

Figure 3-5 on page 3-16 shows the bit assignments.

Figure 3-5 Test chip CFGRW1 Register bit assignments

Table 3-10 shows the bit assignments.

Table 3-10 Test chip CFGRW1 Register bit assignments

Bits	Name	Function
[31]	-	Reserved. Do not modify. Read as zero.
[30:28][a]	TC_Remap	Maps to the **TC_Remap[2:0]** bus.
[27]	-	Reserved. Do not modify. Read as zero.
[26:23]	CLUSTERID	Maps to the **CLUSTERID[3:0]** bus.
[22]	L2CC CFGBIGEND	Maps to the **L2CC CFGBIGEND** signal.
[21:18]	CFGEND	Maps to the **CFGEND[3:0]** bus.
[17:14][a]	CP15DISABLE	Maps to the **CP15DISABLE[3:0]** bus.
[13]	Enable SMC TZASC	Maps to the **Enable SMC TZASC** signal.
[12][a]	Enable L2CC	Maps to the **Enable L2CC bypass** signal. 0 = PL310 L2CC is bypassed in hardware and not accessible in the memory map.
[11][a]	SPNIDEN	Maps to the **SPNIDEN** secure non-invasive debug signal.
[10][a]	SPIDEN	Maps to the **SPIDEN** secure invasive debug signal.
[9][a]	NIDEN	Maps to the **NIDEN** non-invasive debug enable signal.
[8][a]	DBGEN	Maps to the **DBGEN** invasive debug enable signal.
[7]	-	Reserved. Do not modify.
[6:3]	MCLK PLL pc divide	Maps to the **MCLK PLL pc divide[3:0]** bus.
[2:0]	MCLK PLL pb divide	Maps to **MCLK PLL pb divide[3:1]** of the **MCLK PLL pb divide[3:0]** bus. See Table 3-9 on page 3-15 for the remaining signal line.

a. These bits have read and write access. The remainder of the register bits are read-only from the APB interface.

Test chip SCC Register 2

The CFGRW2 Register characteristics are:

Purpose   Enables you to read and write test chip configuration settings.

Usage constraints   There are no usage constraints.

Configurations   Available in all CoreTile Express configurations.

Attributes   See Table 3-8 on page 3-14.
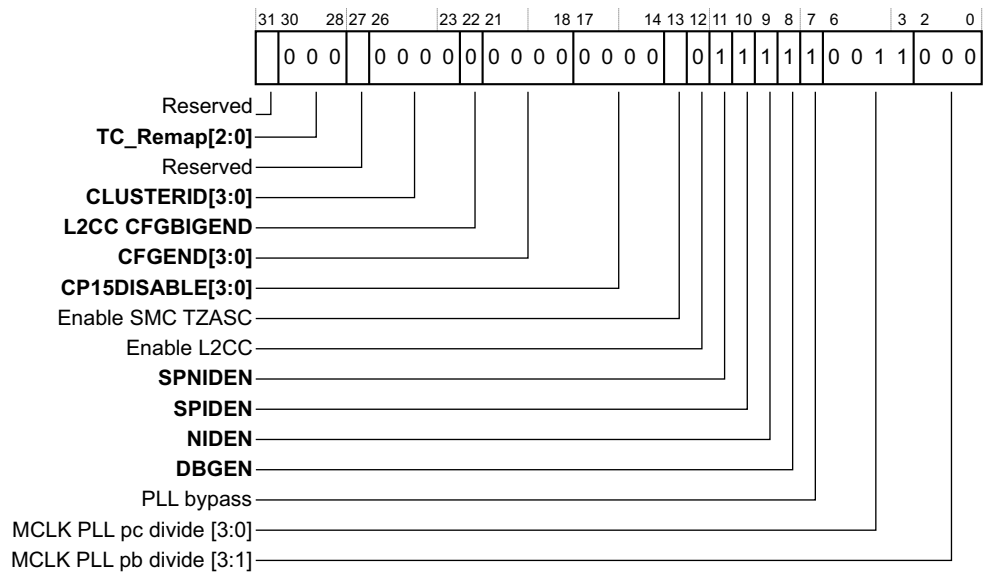
Figure 3-6 shows the bit assignments.
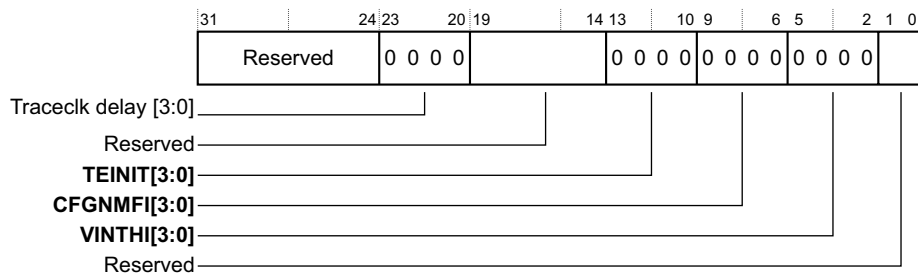
Figure 3-6 Test chip CFGRW2 Register bit assignments

Table 3-11 shows the bit assignments.

Table 3-11 Test chip CFGRW2 Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Do not modify. Read as zero.
[23:20]	Traceclk delay	Maps to the **Traceclk delay[3:0]** bus.
[19:14]	-	Reserved. Do not modify. Read as zero.
[13:10][a]	TEINIT	Maps to the **TEINIT[3:0]** processor Thumb®2 boot bus.
[9:6][a]	CFGNMFI	Maps to the **CFGNMFI[3:0]** processor FIQ acts as NMI bus.
[5:2][a]	VINTHI	Maps to the **VINTHI[3:0]** processor high-vecs mode bus.
[2:0]	-	Reserved. Do not modify. Read as zero.

a. These bits have read and write access. The remainder of the register bits are read-only from the APB interface.

3.3.10   TrustZone protection controller

——— **Note** ———

• See the *TrustZone Protection Controller Technical Overview* for general information on TrustZone. Access to more complex documentation on the TrustZone Protection Controller requires a license to the technology. Contact ARM for more information.

When the TZPC protection signal of a device under TrustZone control is 1b0, only secure transactions can access the port of that device. When the TZPC protection signal is 1b1, both secure and non-secure transactions can access the port.

Table 3-12 shows the TZPC connections:

Table 3-12 TZPC signals

TZPC protection signal	Device under control	Default setting, secure is 0
TZPCDECPROT0[0]	PL341 APB configuration	0
TZPCDECPROT0[1]	PL354 APB configuration	0
TZPCDECPROT0[2]	SCC	0
TZPCDECPROT0[3]	No connection	0
TZPCDECPROT0[4]	SP804 Dual-timer module	0
TZPCDECPROT0[5]	SP805 Watchdog module	0
TZPCDECPROT0[6]	TZPC (always secure RAZ/WI)	0
TZPCDECPROT0[7]	Reserved	0
TZPCDECPROT0[8]	No connection	0
TZPCDECPROT0[9]	Fast PL301 APB configuration	0
TZPCDECPROT0[10]	Slow PL301 APB configuration	0
TZPCDECPROT0[11]	No connection	0
TZPCDECPROT0[12]	No connection	0
TZPCDECPROT0[13]	SMC_TZASC APB configuration	0
TZPCDECPROT0[14]	Debug APB peripherals	0
TZPCDECPROT0[15]	No connection	0
TZPCDECPROT1[0]	External AXI slave port	0
TZPCDECPROT1[1]	PL354 AXI	0
TZPCDECPROT1[2]	Reserved	0
TZPCDECPROT1[3]	Entire APB	0
TZPCDECPROT1[4]	PL111 AHB configuration port	0
TZPCDECPROT1[5]	AXI RAM	0
TZPCDECPROT1[6]	PL341 AXI	0
TZPCDECPROT1[7]	No connection	0
TZPCDECPROT1[8]	Cortex-A9 advanced coherency port	0
TZPCDECPROT1[9]	Entire slow AXI system	0
TZPCDECPROT1[10:15]	No connection	0
TZPCDECPROT2[0]	External master TrustZone override: b0: Security from Master b1: Override master to make all transactions non-secure.	0

TZPC protection signal	Device under control	Default setting, secure is 0
TZPCDECPROT2[1]	DAP AHB-AP TrustZone override: `b0`: Security from Master `b1`: Override master to make all transactions non-secure.	0
TZPCDECPROT2[2]	PL111 master interface TrustZone override: `b0`: Security from Master `b1`: Override master to make all transactions non-secure.	0
TZPCDECPROT2[3]	No connection	0
TZPCDECPROT2[4]	No connection	0
TZPCDECPROT2[5]	SMC_TZASC lockdown	0
TZPCDECPROT2[6:15]	No connection	0

TrustZone Address Space Controller (TZASC)

The *TrustZone Address Space Controller* (TZASC) is a programmable unit that enables you to configure memory regions of selected peripherals with different access rights for Secure and Non-secure AXI transactions. The TZASC has 4KB memory space. The Cortex-A9 MPCore test chip design uses one TZASC to secure the SMC peripheral. See Figure 2-3 on page 2-5.

The Cortex-A9 MPCore test chip bypasses the SMC_TZASC by default. Set register CFGRW1[13] = `1b1` in the SCC to enable SMC_TZASC functionality. The settings in Table 3-12 on page 3-18 control the security of the SMC_TZASC APB configuration interface but programming of this interface only takes effect if the CFGRW1 register setting does not bypass the SMC_TZASC. See *Test chip SCC Register 1* on page 3-15.

For specific configurations on the SMC peripheral, see the *PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual*.

3.3.11 Watchdog module, SP805

This component is located at address `0x100E5000`.

See the *ARM® Watchdog Module (SP805) Technical Reference Manual* for more information.

Appendix A
Signal Descriptions

This appendix describes the signals present at the interface connectors. It contains the following sections:

- *HDRX HSB multiplexing scheme* on page A-2
- *Debug and Trace connectors* on page A-3.

------ **Note** ------

See also the *Motherboard Express µATX Technical Reference Manual*.

A.1 HDRX HSB multiplexing scheme

A bus multiplexing scheme is necessary to reduce the number of pins required on the HDRY header for the 64-bit AXI master and slave on the HSBM and HSBS buses. The LogicTile Express daughterboard must implement a similar multiplexing scheme to be compatible with the CoreTile Express signals.

──── **Note** ────

All signals on the **HSB (M)** and **HSB (S)** buses are 1.8V.

Figure A-1 shows a simplified block diagram of the multiplexing scheme for the two AXI buses.
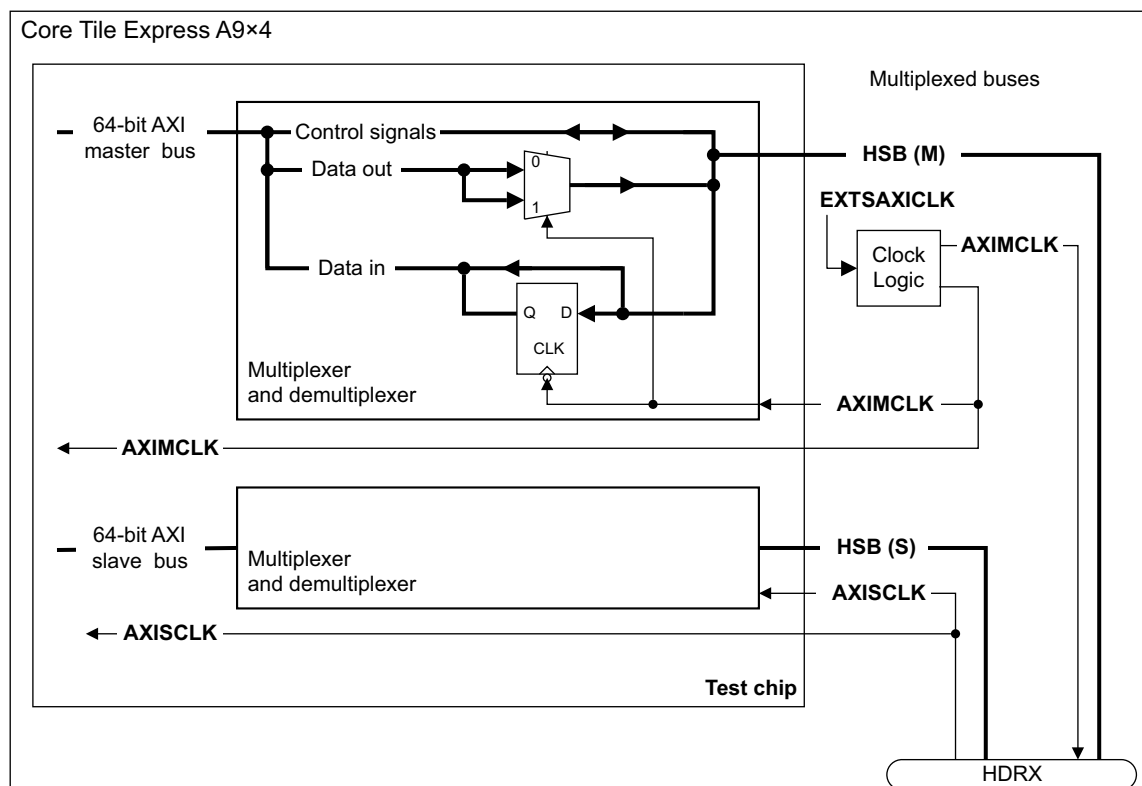
Figure A-1 HSB multiplexing

──── **Note** ────

In Figure 2-5 on page 2-9, **AMIXCLK** originates from **EXTSAXICLK**.

ARM provides *Application Note AN224 Example Logic Tile Express 3MG design for a Core Tile Express A9×4* that implements an example AMBA system using a LogicTile Express 3MG daughterboard to interconnect with the CoreTile Express A9×4 daughterboard. See the documentation supplied on the accompanying media and the *Application Notes* for more information at http://infocenter.arm.com.

A.2 Debug and Trace connectors

This section describes the debug connectors on the daughterboard and contains the following subsections:

- *JTAG connector*
- *Trace connector*.

A.2.1 JTAG connector

The daughterboard routes the JTAG signals to:

- A standard 20-way 2.54mm pitch IDC male connector.
- The Trace port MICTOR connectors.

——— **Caution** ———

- Your external debug interface unit must adapt its interface voltages to the voltage level of the daughterboard JTAG. All the Trace and JTAG signals operate at 1.8V.

- There is no guaranteed support for JTAG on the Trace connector. Use the dedicated JTAG connector on the daughterboard.

A.2.2 Trace connector

The test chip supports up to 32-bit Trace output from the CoreSight TPIU and enables connection of a compatible Trace unit. The interface uses two MICTOR connectors. The *Embedded Trace Macrocell Architecture Specification* (ARM IHI 0014N) specifies the pinout and mechanical placement of the connectors.

——— **Note** ———

- All the Trace and JTAG signals operate at 1.8V.
- The Trace connector cannot supply power to a Trace unit.
- The interface does not support the **TRACECTL** signal. This is always driven LOW.

Appendix B
Specifications

This appendix contains the electrical specification for the daughterboard. It contains the following section:

- *AC characteristics*.

B.1   AC characteristics

Table B-1 shows the recommended AC operating characteristics for the Cortex-A9 MPCore test chip.

For more information on each interface that Table B-1 describes, see the appropriate technical reference manual listed in *Additional reading* on page x.

Table B-1 AC characteristics

Interface	Parameter	Symbol	Minimum	Maximum	Description
Multiplexed Slave AXI port	Clock cycle	t_{MPcyc}	30ns	-	Cmax=49.3pF Cmin=26.13pF
	Output valid time before clock rising edge	t_{MPov}	-	0.6931ns	
	Output hold time after clock rising edge	t_{MPoh}	3.645ns	-	
	Input setup time to clock rising edge	t_{MPis}	-	3.1ns	
	Input hold time after clock rising edge	t_{MPih}	4.91ns	-	
Multiplexed Master AXI port	Clock cycle	t_{SPcyc}	20ns	-	Cmax=47.8pF Cmin=23.88pF
	Output valid time before clock edge	t_{SPov}	-	0.387ns	
	Output hold time after clock edge	t_{SPoh}	4.156ns		
	Input setup time to clock edge	t_{SPis}	-	2.59ns	
	Input hold time after clock edge	t_{SPih}	4.811ns	-	
Trace	Clock cycle	$t_{TRACEcyc}$	10ns	-	Cmax=22.5pF Cmin=16.5pF
	Output valid time before clock rising edge	$t_{TRACEov}$	-	7ns	
	Output hold time after clock rising edge	$t_{TRACEoh}$	5ns	-	
JTAG	Clock cycle	$t_{JTAGcyc}$	20ns	-	Cmax=48.5pF Cmin=10.5pF
	Output valid time before clock rising edge	t_{JTAGov}	-	8ns	
	Output hold time after clock rising edge	t_{JTAGoh}	4ns	-	
	Input setup time to clock rising edge	t_{JTAGis}	-	12ns	
	Input hold time after clock rising edge	t_{JTAGih}	8ns	-	

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

Table C-1 Issue A

Change	Location	Affects
First release	-	-

Table C-2 Differences between Issue A and Issue B

Change	Location	Affects
Replaced `SYSCON` with `SCC`.	Example 3-1 on page 3-13 Example 3-2 on page 3-13 Table 3-8 on page 3-14	All revisions
Added new section about power monitoring.	*Voltage, current, and power monitoring* on page 2-18	All revisions
Change remapped address region for External AXI to `0x0`.	Table 3-2 on page 3-4	All revisions
Denoted location of Cortex-A9 MPCore private memory region in memory map and added explanatory Note.	Figure 3-2 on page 3-5	All revisions

Table C-3 Differences between Issue B and Issue C

Change	Location	Affects
In the figure *Top-level view of the test chip components,* the bottom right hand label is changed to HDRX.	Figure 2-3 on page 2-5	All revisions
First sentence changed in Powerup configuration section to reflect `board.txt` configuration file and ease of understanding.	*Powerup configuration* on page 2-7	All revisions
In Example Typical board.txt file, corrected OSC2 value to 66.67MHz to match value in the 'Daughterboard OSCLK clock sources' table.	Table 2-2 on page 2-10	All revisions
Note added to Clocks overview figure for ease of understanding.	Figure 2-5 on page 2-9	All revisions
Test chip registers CDFRW0 and CDFRW1 corrected to CFGRW0 and CFGRW1.	Figure 2-6 on page 2-12	All revisions
Notes added to Test chip PLLs and clock divider logic diagram for ease of understanding.	Figure 2-6 on page 2-12	All revisions
VCO text and formula in Note under Test chip PLLs and clock divider logic figure, placed on two lines for readability.	Figure 2-6 on page 2-12	All revisions
Table updated for clarity	Table 2-4 on page 2-13	All revisions
In the 'Daughterboard memory map' figure, REMAP area corrected to `0xE0000000-0xE4000000`.	Figure 3-1 on page 3-3	All revisions
Third column in Remap regions table corrected to: `0x44000000-0x44FFFFFF`	Table 3-2 on page 3-4	All revisions
In Example Setting the test chip configuration register values from board.txt and Example Alternative values for test chip configuration registers, the reset values are changed to match the reset values of Example Typical board.txt file, for consistency.	Example 3-1 on page 3-13 Example 3-2 on page 3-13	All revisions
Clock names changed in example to match table for consistency.	Example 3-2 on page 3-13 Table 2-3 on page 2-11	All revisions
Reset values in Table Test chip SCC register summary, changed to match values in Example Typical board.txt file, for consistency.	Table 3-8 on page 3-14	All revisions
Test chip SCC register summary table Entry in board.txt column corrected to: `SCC:0x000` `SCC:0x004` `SCC:0x008`	Table 3-8 on page 3-14	All revisions
In t able Test chip CFGRW1 Register bit assignments: • Bit [7] changed to Reserved • The description for Bit[12] is updated.	Table 3-10 on page 3-16	All revisions
TZPC signals table updated to: **TZPCDECPROT0[11]** - DMC_TZASC **TZPCDECPROT0[12]** - NMC_TZASC **TZPCDECPROT0[13]** - SMC_TZASC	Table 3-12 on page 3-18	All revisions
Description of Fclkselect name in table is expanded for ease of understanding.	Table 3-9 on page 3-15	All revisions
Note added to HSB multiplexing figure to explain that **AXIMCLK** originates from **EXTSAXICLK**.	Figure A-1 on page A-2	All revisions

Table C-4 Differences between Issue C and Issue D

Change	Location	Affects
Note added above System connect example figure, to state that CoreTile Express A9×4 does not support PCI Express.	Figure 2-2 on page 2-4	All revisions
System interconnect diagram updated: • HDRY1 position corrected • HDRX1 position corrected • HDRX2 position corrected • HDRY2 position corrected.	Figure 2-2 on page 2-4	All revisions
Bullet changed in System interconnect signals to include SCU and ACP, and additional note added to existing note at the end of the bullets.	*System interconnect signals* on page 2-6	All revisions
Description for OSC1 in Daughterboard OSCCLK clock sources table updated	Table 2-2 on page 2-10	All revisions
New subsection added on display resolutions and display memory organization	*Display resolutions and display memory organization* on page 3-7	All revisions
Updated Test chip CFGRW2 Register bits assignments figure to match table.	Figure 3-6 on page 3-17	All revisions

Table C-5 Differences between Issue D and Issue E

Change	Location	Affects
Programmers Model updated to reflect the latest template	Chapter 3 *Programmers Model*	All revisions

Table C-6 Differences between Issue E and Issue F

Change	Location	Affects
Updated description of peripheral memory map.	Table 3-1 on page 3-3	All revisions
Updated Preface. Added Timing Diagram section.	*Timing diagrams* on page ix	All revisions
Glossary removed. References and link to *ARM Glossary* inserted.	*Glossary* on page viii	All revisions
Configuration chapter shortened. Information is now in new document *ARM® Versatile™ Express Configuration Technical Reference Manual.*	*Powerup configuration* on page 2-7	All revisions
Added new documents to Additional Reading section of Preface. *ARM® Versatile™ Express Configuration Technical Reference Manual* and *ARM® LogicTile Express 13MG Technical Reference Manual*.	*Additional reading* on page x	All revisions
Updated On-chip peripheral memory map.	Figure 3-2 on page 3-5	All revisions
Updated description of TrustZone protection controller. Updated TZPC information in test chip architecture diagram.	*TrustZone protection controller* on page 3-17 Figure 2-3 on page 2-5	All revisions

Table C-7 Differences between Issue F and Issue G

Change	Location	Affects
Added reference to board revision B and board revision C in powerup configuration section.	*Powerup configuration* on page 2-7	Revision B Revision C

Table C-8 Differences between Issue G and Issue H

Change	Location	Affects
Updated OSC2 information.	Table 2-2 on page 2-10	All revisions

Table C-9 Differences between Issue H and Issue I

Change	Location	Affects
Corrected JTAG timing information.	Table B-1 on page B-2	All revisions