Analyzer Tile

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User Guide

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Analyzer Tile
User Guide

Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidential	Change
15 October 2003	A	Non-Confidential	New document
20 April 2011	B	Non-Confidential	Updated to amend tables in appendix A

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

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Preface

This preface introduces the documentation for the Analyzer Tile. It contains the following sections::

About this document

This document describes how to set up and use the Analyzer Tile.

Intended audience

This document has been written for experienced hardware and software developers as an aid to using the Analyzer Tile with the RealView Logic Tiles.

Organization

This document is organized into the following chapters:

Chapter 1 ***Introduction***

Read this chapter for an introduction to the Analyzer Tile.

Chapter 2 ***Using the Analyzer Tile***

Read this chapter for a description of how to set up and start using the Analyzer Tile.

Appendix A ***Pinouts and Specifications***

Read this chapter for information about the signals on the Mictor, tile, and testpoint connectors and the mechanical and electrical specifications for the Analyzer Tile.

Typographical conventions

The following typographical conventions are used in this book:

`monospace` Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

`mono`space Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

`monospace italic`

Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names and buttons. Also used for terms in descriptive lists, where appropriate.

`monospace bold`

Denotes language keywords when used outside example code and ARM processor signal names.

Further reading

This section lists related publications by ARM Limited and other companies provide additional information.

ARM publications

The following publications provide information about related ARM products and toolkits:

- ARM RealView/XC2V4000+ Logic Tile User Guide (ARM DUI 00186)
- ARM Integrator/IM-LT1 Interface Module User Guide (ARM DUI 00187)
- ARM Integrator/AP User Guide (ARM DUI 0098)
- ARM Integrator/CP User Guide (ARM DUI 0159)
- ARM RealView ICE User Guide (ARM DUI 0155)
- ARM Multi-ICE User Guide (ARM DUI 0048)
- ADS Developer Guide (ARM DUI 0056)
- RealView Compilation Tools Developer Guide (ARM DUI 0203).

Feedback

ARM Limited welcomes feedback both on the Analyzer Tile and on the documentation.

Feedback on this document

If you have any comments about this document, please send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- an explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the Analyzer Tile

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- an explanation of your comments.

Chapter 1
Introduction

This chapter introduces the Analyzer Tile. It contains the following sections:

- *About the Analyzer Tile* on page 1-2
- *Analyzer Tile layout* on page 1-3.

1.1 About the Analyzer Tile

The Analyzer Tile provides access to the signals present on headers HDRX, HDRY, and HDRZ of RealView Logic Tiles. The Analyzer Tile can be inserted between tiles, as shown in Figure 1-1 on page 1-3, or it can be used on the top of a stack of Logic Tiles. The Analyzer Tile can be used with individual Logic Tiles or Logic Tiles mounted on a development board, for example, the Versatile Platform Baseboard for ARM926EJ-S.

Note

Integrator development boards, such as the Integrator/AP, do not have tile headers so an Integrator/IM-LT1 Interface Module must be used between the Integrator board and a Logic Tile. Because of the component height on the Integrator/IM-LT1 Interface Module, the Analyzer Tile cannot be used directly on top of an Interface Module.

A Logic Tile does not have a fixed bus structure, but an AMBA bus is often implemented for communication between the tiles and baseboard.

The logic analyzer connection points are AMP Mictor connectors (AMP 2-767004-2), which are specified by both Agilent and Tektronix as suitable for connection to a range of logic analyzers. The Mictor connectors are mounted on the top of the Analyzer Tile and permit you to connect flying leads and test equipment.

1.2 Analyzer Tile layout

Figure 1-1 shows the layout of the Analyzer Tile.

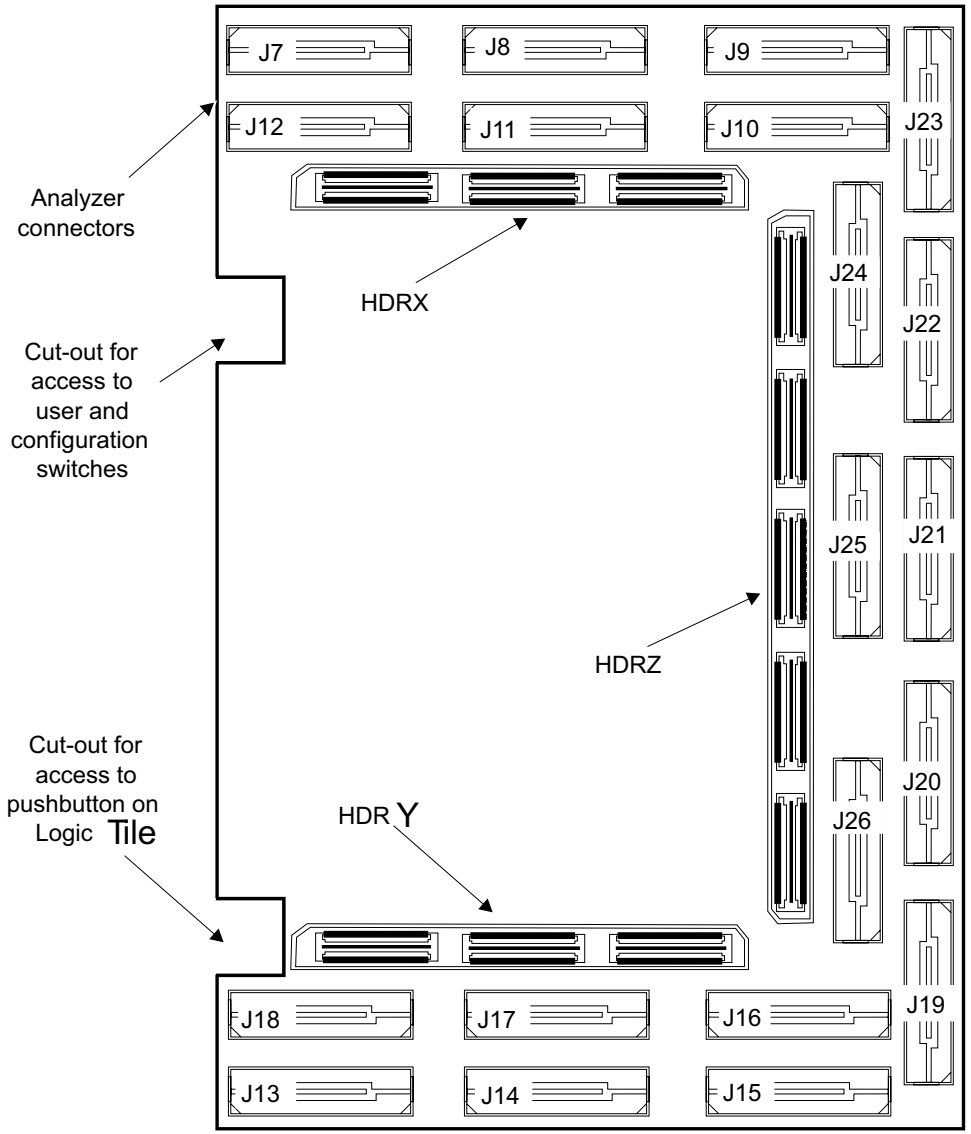

Figure 1-1 Analyzer Tile layout

Chapter 2
Using the Analyzer Tile

This chapter describes how to set up and prepare the Analyzer Tile for use. It contains the following sections:

2.1 Connecting the Analyzer Tile

The Analyzer Tile connects on top of a Logic Tile, or between tiles as shown in Figure 2-1, to monitor tile signals. The Analyzer Tile can also be connected directly on top of the Versatile Platform Baseboard for ARM926EJ-S.

The Analyzer Tile cannot, however, be connected directly on top of an Integrator/IM-LT1 or Integrator/IM-LT2 Interface Module

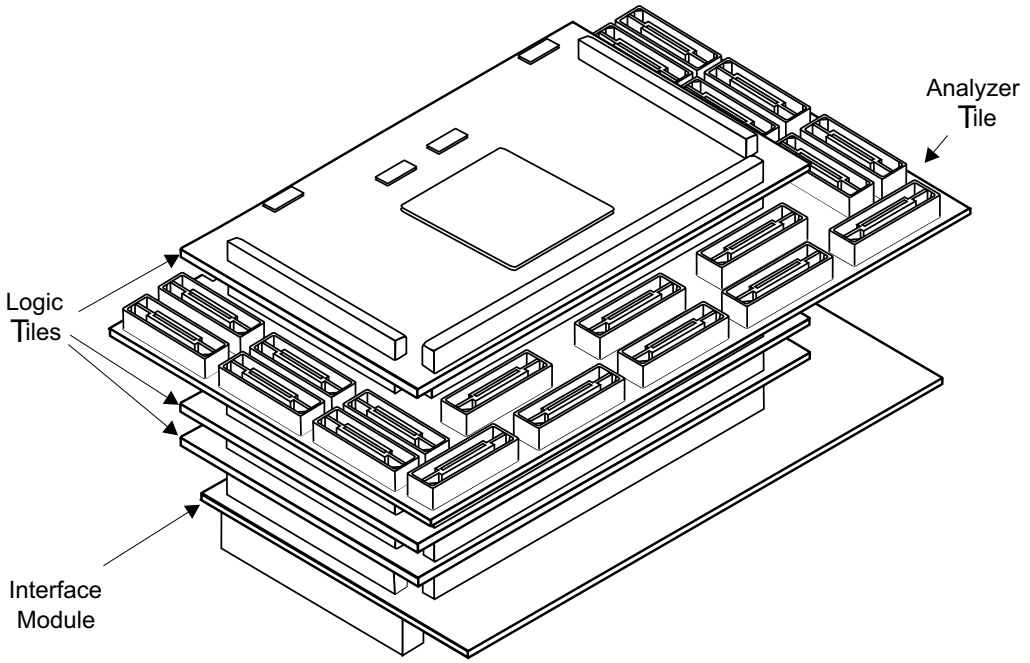

Figure 2-1 Interface Tile mounted on logic tile and interface module

All signals from the Logic Tile pass directly through the Analyzer Tile as shown in Figure 2-2 on page 2-3. There is no buffering or rotation of signals between the headers

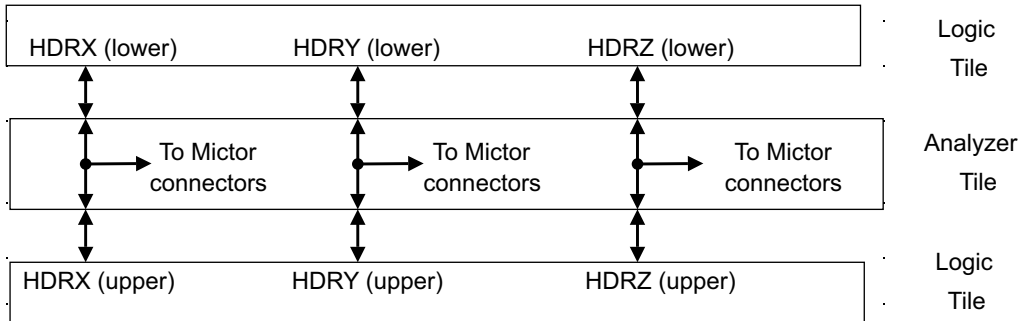

Figure 2-2 Logic Tile signals

2.2 Mictor connectors

Connect your logic analyzer to the Analyzer Tile using the high-density AMP Mictor connectors (AMP 2-767004-2). Each one of these connectors carries up to 32 signals and 2 clocks (or clock qualifiers). Figure 2-3 shows the connector and identification of pin 1.

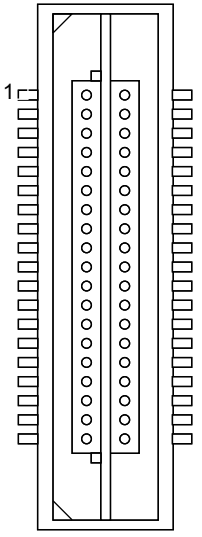

Figure 2-3 AMP Mictor connector

Agilent and Tektronix label these connectors differently, but the assignments of signals to physical pins is appropriate for both systems and pin 1 is always in the same place. The schematic is labeled according to the Agilent pin assignment.

Note

Pin 1 is labelled as +5VDC on the Agilent pin assignment, however it has no connection on the Analyzer Tile because the voltage is not required. Pin 2 is labelled as NC on the Tektronix in assignment, however it is connected to GND on the Analyzer Tile to maintain compatibility with the Agilent pin assignments.

The connectors provide access to:

- All I/O signals on HDRX, HDRY, and HDRZ
- JTAG signals
- Clock signals
- Reset signals.

2.2.1 Using an Agilent logic analyzer

Agilent label the signals as shown in Table 2-1. The Agilent E5346A 38-pin Probe can be used with an Agilent logic analyzer and the Analyzer Tile.

Table 2-1 Agilent logic analyzer probe

Channel	Pin	Pin	Channel
+5VDC	1	2	NC
GND	3	4	NC
LCLK	5	6	HCLK
D15 EVEN	7	8	D15 ODD
D14 EVEN	9	10	D14 ODD
D13 EVEN	11	12	D13 ODD
D12 EVEN	13	14	D12 ODD
D11 EVEN	15	16	D11 ODD
D10 EVEN	17	18	D10 ODD
D9 EVEN	19	20	D9 ODD
D8 EVEN	21	22	D8 ODD
D7 EVEN	23	24	D7 ODD
D6 EVEN	25	26	D6 ODD
D5 EVEN	27	28	D5 ODD
D4 EVEN	29	30	D4 ODD
D3 EVEN	31	32	D3 ODD
D2 EVEN	33	34	D2 ODD
D1 EVEN	35	36	D1 ODD
D0 EVEN	37	38	D0 ODD

2.2.2 Using an Tektronix logic analyzer

Tektronix label the signals as shown in Table 2-2. The Tektronix P6434 Mass Termination Probe can be used with a Tektronix logic analyzer and the Analyzer Tile.

Table 2-2 Tektronix logic analyzer probe

Channel	Pin	Pin	Channel
NC	1	38	NC
NC	2	37	NC
CLK/QUAL	3	36	CLK/QUAL
D3:7	4	35	D1:7
D3:6	5	34	D1:6
D3:5	6	33	D1:5
D3:4	7	32	D1:4
D3:3	8	31	D1:3
D3:2	9	30	D1:2
D3:1	10	29	D1:1
D3:0	11	28	D1:0
D2:7	12	27	D0:7
D2:6	13	26	D0:6
D2:5	14	25	D0:5
D2:4	15	24	D0:4
D2:3	16	23	D0:3
D2:2	17	22	D0:2
D2:1	18	21	D0:1
D2:0	19	20	D0:0

2.3 Signal description

This section describes the signals present on the Analyzer Tile.

2.3.1 Connector summary

Table 2-3 describes the signal allocation of each of the connectors. See *Logic analyzer connectors* on page A-4 for detailed pinouts.

Table 2-3 Connector summary

Mictor connector	Logic Tile signals	Clocks and qualifiers
J7	**[X31:X0]**	**CLK_POS_UP**, **X128**
J8	**[X63:X32]**	**CLK_DN_MINUS1**, **X129**
J9	**[X95:X64]**	**CLK_POS_UP**, **X130**
J10	**[X127:X96]**	**CLK_POS_DN**, **X131**
J11	**[X159:X128]**	**CLK_GLOBAL**, **X178**
J12	**[X179:X160]**, Configuration JTAG	**C_TCK**, **X179**
J13	**Y[31:Y0]**	**CLK_UP_PLUS1**, **X128**
J14	**Y[63:Y32]**	**CLK_DN_MINUS1**, **Y129**
J15	**Y[95:Y64]**	**CLK_NEG_UP**, **Y130**
J16	**Y[127:Y96]**	**CLK_NEG_DN**, **Y131**
J17	**Y[152:Y132]**, **SPARE[10:0]**	**CLK_GLOBAL**, **Y178**
J18	**Y[176:1Y53]**, Debug JTAG	**D_TCK**, **Y179**
J19	**Z[31:Z0]**	**CLK_UP_PLUS1**, **Z95**
J20	**Z[63:Z32]**	**CLK_DN_MINUS1**, **Z94**
J21	**Z[95:Z64]**	**CLK_UP_PLUS2**, **Z59**[a]
J22	**Z[191:Z160]**	**CLK_DN_MINUS2**, **Z128**
J23	**Z[159:128]**	**CLK_POS_UP**, **CLK_POS_DN**

Table 2-3 Connector summary (continued)

Mictor connector	Logic Tile signals	Clocks and qualifiers
J24	**Z[255:224]**	CLK_UP_THRU, Z255
J25	**Z[223:192]**	CLK_DN_THRU, Z129
J26	**Z[127:96]**	CLK_GLOBAL, Z44[b]

a. Z59 is connected to C27 when tiles are mounted on an Integrator/IM-LT1. This signal is not used on an Integrator/AP.
b. Z44 is connected to C12 (HREADY) when tiles are mounted on an Integrator/IM-LT1.

2.3.2 Clock connections

Figure 2-4 on page 2-9 shows the clock signals on the header pins and the connection to the logic analyzer connectors.

The clock signals are not buffered between the top and bottom tile headers. However, most of the Logic Tile clocks are buffered before routing to the logic analyzer connectors. The buffering prevents loading on the clock signal. The unbuffered clocks, however, permit more accurate measurements of setup and hold times. Some of the clocks are also connected to test points for easy access, see Table A-1 on page A-3. See Appendix A Pinouts and Specifications for a complete list of connector pinouts.

Note

For the Analyzer Tile, signals on the lower Logic Tile connectors (HDRX, HDRY, and HDRZ) are connected to the same pin on the upper Logic Tile connectors. There are no rotated, buffered, or modified signals on the tile header connectors.

The signal names on the upper and lower HDRZ Logic Tile connectors shown in Figure 2-4 on page 2-9 are different because some signals are rotated or buffered on the Logic Tile.

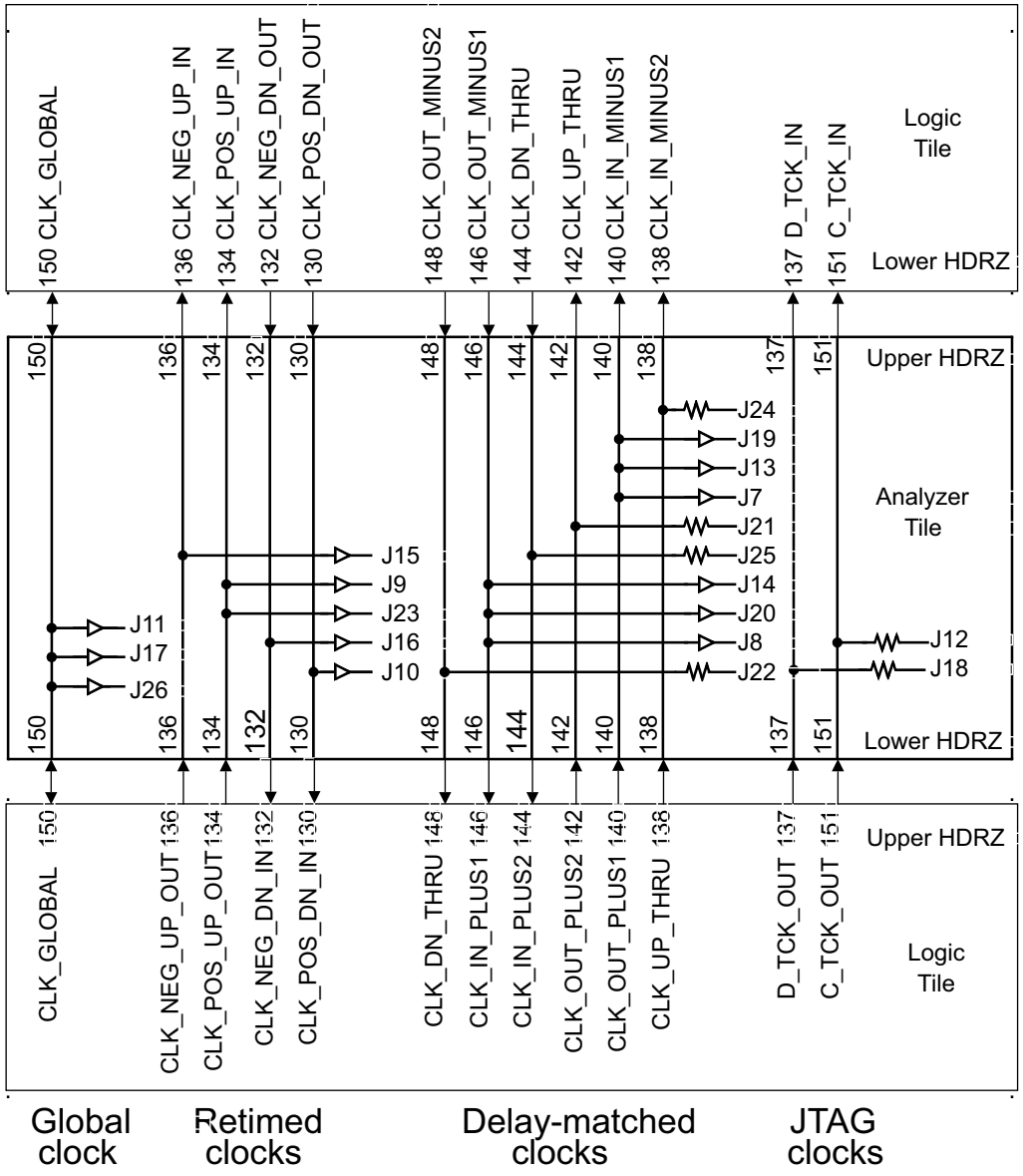

Figure 2-4 HDRZ clock signals

2.3.3 JTAG signals

The Analyzer Tile does not have a JTAG connector.

If you are using a JTAG debugger with an Integrator/AP baseboard, connect the debugger to the Integrator/IM-LT1 or IM-LT2 Interface Module. The Logic Tile JTAG signals can be monitored from logic analyzer connector J12 and J18, see *Mictor connector J12, JTAG and X179-X160* on page A-9 and *Mictor connector J18, JTAG and Y179-Y153* on page A-15. Refer to the *Multi-ICE User Guide* and the *Integrator/IM-LT1 User Guide* for more details.

If you are using a JTAG debugger with the Versatile Platform Baseboard for ARM926EJ-S, use the JTAG interface on the baseboard.

2.3.4 Trace signals

The Analyzer Tile does not have a dedicated trace port connector.

If you are using an Integrator/AP baseboard, the Mictor connectors on the Analyzer Tile can be used to output trace signals if an appropriate design is placed in the Logic Tile. Use this option if the trace signals are not routed down to the Interface Module. For example, they may have been replaced by I/O signals. Mictor connector J18 contains the JTAG run control signals and is recommended for use as the trace connector. If the Logic Tile trace signals are routed down to the Interface Module such as the Integrator/IM-LT1, you can use the trace connector on the Interface Module.

If you are using the Versatile Platform Baseboard for ARM926EJ-S, use the Trace Port interface on the baseboard.

Appendix A
Pinouts and Specifications

This appendix describes the connectors on the Analyzer Tile and the Analyzer Tile specifications. It contains the following sections:

A.1 Test points

The Analyzer Tile provides test points and ground points to aid diagnostics as shown in Figure A-1 and Table A-1 on page A-3.

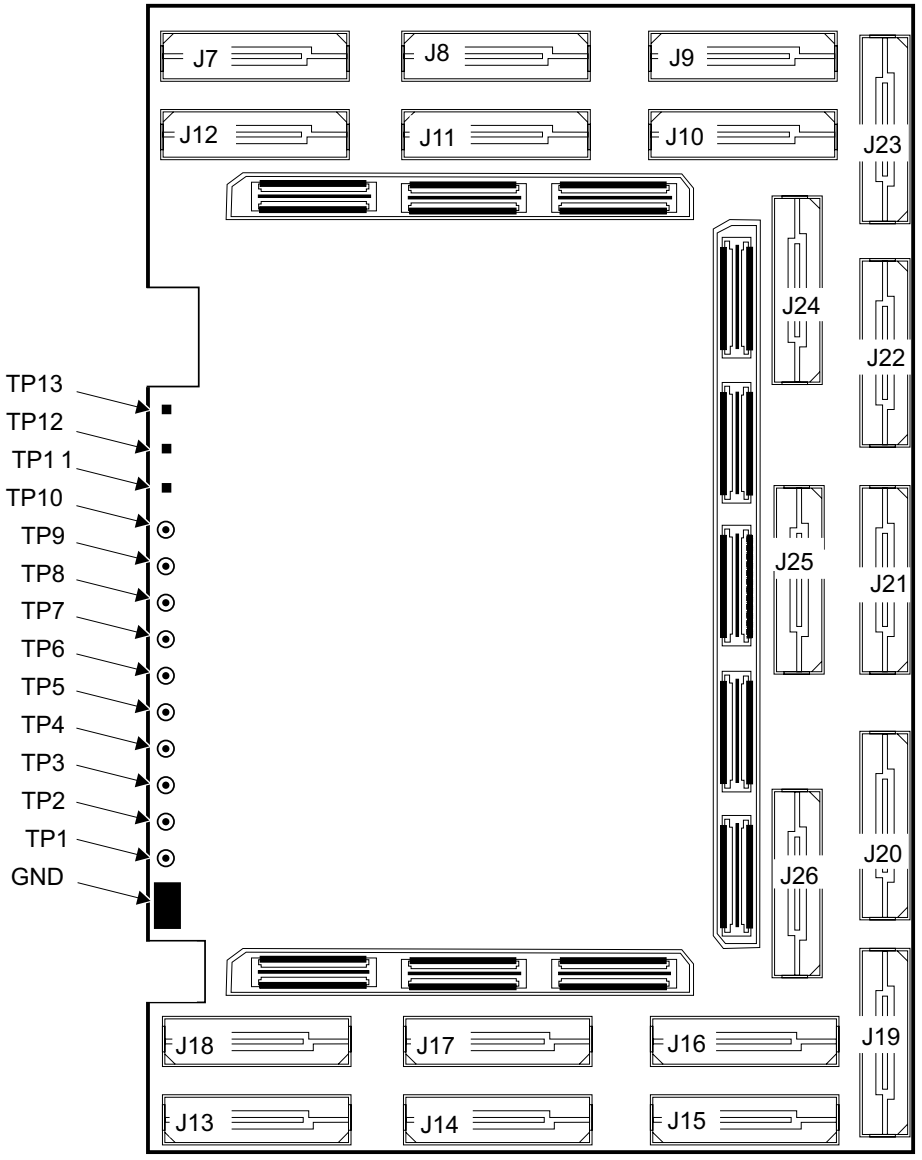

Figure A-1 Test points

The functions of these test points are summarized in Table A-1.

Table A-1 Test connections

Test point	Description
1	Buffered **CLK_NEG_DN**
2	Buffered **CLK_NEG_UP**
3	Buffered **CLK_DN_MINUS1**
4	Buffered **CLK_UP_PLUS1**
5	Buffered **CLK_POS_DN**
6	Buffered **CLK_POS_UP**
7	Buffered **CLK_GLOBAL**
8	**GLOBAL_DONE**
9	**nSYSRST**
10	**nSYSPOR**
11	(not fitted)
12	(not fitted)
13	(not fitted)

A.2 Logic analyzer connectors

The tile signals on the analyzer connectors are shown in Table A-20 on page A-22 to Table A-16 on page A-18. For a description of Agilent and Tektronix pin numbering and pin names, see Table 2-1 on page 2-5 and Table 2-2 on page 2-6.

Table A-2 Mictor connector J7, X31-X0

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_UP_PLUS1 (buffered)	5 (3)	6 (36)	**X128**
X31	7 (4)	8 (35)	**X15**
X30	9 (5)	10 (34)	**X14**
X29	11 (6)	12 (33)	**X13**
X28	13 (7)	14 (32)	**X12**
X27	15 (8)	16 (31)	**X11**
X26	17 (9)	18 (30)	**X10**
X25	19 (10)	20 (29)	**X9**
X24	21 (11)	22 (28)	**X8**
X23	23 (12)	24 (27)	**X7**
X22	25 (13)	26 (26)	**X6**
X21	27 (14)	28 (25)	**X5**
X20	29 (15)	30 (24)	**X4**
X19	31 (16)	32 (23)	**X3**
X18	33 (17)	34 (22)	**X2**
X17	35 (18)	36 (21)	**X1**
X16	37 (19)	38 (20)	**X0**

Table A-3 Mictor connector J8, X63-X32

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_DN_MINUS1 (buffered)	5 (3)	6 (36)	**X129**
X63	7 (4)	8 (35)	**X47**
X62	9 (5)	10 (34)	**X46**
X61	11 (6)	12 (33)	**X45**
X60	13 (7)	14 (32)	**X44**
X59	15 (8)	16 (31)	**X43**
X58	17 (9)	18 (30)	**X42**
X57	19 (10)	20 (29)	**X41**
X56	21 (11)	22 (28)	**X40**
X55	23 (12)	24 (27)	**X39**
X54	25 (13)	26 (26)	**X38**
X53	27 (14)	28 (25)	**X37**
X52	29 (15)	30 (24)	**X36**
X51	31 (16)	32 (23)	**X35**
X50	33 (17)	34 (22)	**X34**
X49	35 (18)	36 (21)	**X33**
X48	37 (19)	38 (20)	**X32**

Table A-4 Mictor connector J9, X95-X64

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_POS_UP (buffered)	5 (3)	6 (36)	**X130**
X95	7 (4)	8 (35)	**X79**
X94	9 (5)	10 (34)	**X78**
X93	11 (6)	12 (33)	**X77**
X92	13 (7)	14 (32)	**X76**
X91	15 (8)	16 (31)	**X75**
X90	17 (9)	18 (30)	**X74**
X89	19 (10)	20 (29)	**X73**
X88	21 (11)	22 (28)	**X72**
X87	23 (12)	24 (27)	**X71**
X86	25 (13)	26 (26)	**X70**
X85	27 (14)	28 (25)	**X69**
X84	29 (15)	30 (24)	**X68**
X83	31 (16)	32 (23)	**X67**
X82	33 (17)	34 (22)	**X66**
X81	35 (18)	36 (21)	**X65**
X80	37 (19)	38 (20)	**X64**

Table A-5 Mictor connector J10, X127-X96

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_POS_DN (buffered)	5 (3)	6 (36)	**X131**
X127	7 (4)	8 (35)	**X111**
X126	9 (5)	10 (34)	**X110**
X125	11 (6)	12 (33)	**X109**
X124	13 (7)	14 (32)	**X108**
X123	15 (8)	16 (31)	**X107**
X122	17 (9)	18 (30)	**X106**
X121	19 (10)	20 (29)	**X105**
X120	21 (11)	22 (28)	**X104**
X119	23 (12)	24 (27)	**X103**
X118	25 (13)	26 (26)	**X102**
X117	27 (14)	28 (25)	**X101**
X116	29 (15)	30 (24)	**X100**
X115	31 (16)	32 (23)	**X99**
X114	33 (17)	34 (22)	**X98**
X113	35 (18)	36 (21)	**X97**
X112	37 (19)	38 (20)	**X96**

Table A-6 Mictor connector J11, X159-X128

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_GLOBAL (buffered)	5 (3)	6 (36)	**X178**
X159	7 (4)	8 (35)	**X143**
X158	9 (5)	10 (34)	**X142**
X157	11 (6)	12 (33)	**X141**
X156	13 (7)	14 (32)	**X140**
X155	15 (8)	16 (31)	**X139**
X154	17 (9)	18 (30)	**X138**
X153	19 (10)	20 (29)	**X137**
X152	21 (11)	22 (28)	**X136**
X151	23 (12)	24 (27)	**X135**
X150	25 (13)	26 (26)	**X134**
X149	27 (14)	28 (25)	**X133**
X148	29 (15)	30 (24)	**X132**
X147	31 (16)	32 (23)	**X131**
X146	33 (17)	34 (22)	**X130**
X145	35 (18)	36 (21)	**X129**
X144	37 (19)	38 (20)	**X128**

Table A-7 Mictor connector J12, JTAG and X179-X160

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
C_TCK (unbuffered)	5 (3)	6 (36)	**X179**
NC	7 (4)	8 (35)	**X175**
C_nSRST	9 (5)	10 (34)	**X174**
C_TDO	11 (6)	12 (33)	**X173**
NC	13 (7)	14 (32)	**X172**
C_TCK (unbuffered)	15 (8)	16 (31)	**X171**
C_TMS	17 (9)	18 (30)	**X170**
C_TDI	19 (10)	20 (29)	**X169**
C_nTRST	21 (11)	22 (28)	**X168**
GLOBAL_DONE	23 (12)	24 (27)	**X167**
nSYSRST	25 (13)	26 (26)	**X166**
nSYSPOR	27 (14)	28 (25)	**X165**
SPARE12	29 (15)	30 (24)	**X164**
SPARE11	31 (16)	32 (23)	**X163**
X178	33 (17)	34 (22)	**X162**
X177	35 (18)	36 (21)	**X161**
X176	37 (19)	38 (20)	**X160**

Table A-8 Mictor connector J13, Y31-Y0

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_UP_PLUS1 (buffered)	5 (3)	6 (36)	**Y128**
Y31	7 (4)	8 (35)	**Y15**
Y30	9 (5)	10 (34)	**Y14**
Y29	11 (6)	12 (33)	**Y13**
Y28	13 (7)	14 (32)	**Y12**
Y27	15 (8)	16 (31)	**Y11**
Y26	17 (9)	18 (30)	**Y10**
Y25	19 (10)	20 (29)	**Y9**
Y24	21 (11)	22 (28)	**Y8**
Y23	23 (12)	24 (27)	**Y7**
Y22	25 (13)	26 (26)	**Y6**
Y21	27 (14)	28 (25)	**Y5**
Y20	29 (15)	30 (24)	**Y4**
Y19	31 (16)	32 (23)	**Y3**
Y18	33 (17)	34 (22)	**Y2**
Y17	35 (18)	36 (21)	**Y1**
Y16	37 (19)	38 (20)	**Y0**

Table A-9 Mictor connector J14, Y63-Y32

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_DN_MINUS1 (buffered)	5 (3)	6 (36)	**Y129**
Y63	7 (4)	8 (35)	**Y47**
Y62	9 (5)	10 (34)	**Y46**
Y61	11 (6)	12 (33)	**Y45**
Y60	13 (7)	14 (32)	**Y44**
Y59	15 (8)	16 (31)	**Y43**
Y58	17 (9)	18 (30)	**Y42**
Y57	19 (10)	20 (29)	**Y41**
Y56	21 (11)	22 (28)	**Y40**
Y55	23 (12)	24 (27)	**Y39**
Y54	25 (13)	26 (26)	**Y38**
Y53	27 (14)	28 (25)	**Y37**
Y52	29 (15)	30 (24)	**Y36**
Y51	31 (16)	32 (23)	**Y35**
Y50	33 (17)	34 (22)	**Y34**
Y49	35 (18)	36 (21)	**Y33**
Y48	37 (19)	38 (20)	**Y32**

Table A-10 Mictor connector J15, Y95-Y64

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_NEG_UP (buffered)	5 (3)	6 (36)	Y130
Y95	7 (4)	8 (35)	Y79
Y94	9 (5)	10 (34)	Y78
Y93	11 (6)	12 (33)	Y77
Y92	13 (7)	14 (32)	Y76
Y91	15 (8)	16 (31)	Y75
Y90	17 (9)	18 (30)	Y74
Y89	19 (10)	20 (29)	Y73
Y88	21 (11)	22 (28)	Y72
Y87	23 (12)	24 (27)	Y71
Y86	25 (13)	26 (26)	Y70
Y85	27 (14)	28 (25)	Y69
Y84	29 (15)	30 (24)	Y68
Y83	31 (16)	32 (23)	Y67
Y82	33 (17)	34 (22)	Y66
Y81	35 (18)	36 (21)	Y65
Y80	37 (19)	38 (20)	Y64

Table A-11 Mictor connector J16, Y127-Y96

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_NEG_DN (buffered)	5 (3)	6 (36)	**Y131**
Y127	7 (4)	8 (35)	**Y111**
Y126	9 (5)	10 (34)	**Y110**
Y125	11 (6)	12 (33)	**Y109**
Y124	13 (7)	14 (32)	**Y108**
Y123	15 (8)	16 (31)	**Y107**
Y122	17 (9)	18 (30)	**Y106**
Y121	19 (10)	20 (29)	**Y105**
Y120	21 (11)	22 (28)	**Y104**
Y119	23 (12)	24 (27)	**Y103**
Y118	25 (13)	26 (26)	**Y102**
Y117	27 (14)	28 (25)	**Y101**
Y116	29 (15)	30 (24)	**Y100**
Y115	31 (16)	32 (23)	**Y99**
Y114	33 (17)	34 (22)	**Y98**
Y113	35 (18)	36 (21)	**Y97**
Y112	37 (19)	38 (20)	**Y96**

Table A-12 Mictor connector J17, SPARE and Y152-Y132

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_GLOBAL (buffered)	5 (3)	6 (36)	**Y178**
SPARE10	7 (4)	8 (35)	**Y147**
SPARE9	9 (5)	10 (34)	**Y146**
SPARE8	11 (6)	12 (33)	**Y145**
SPARE7	13 (7)	14 (32)	**Y144**
SPARE6	15 (8)	16 (31)	**Y143**
SPARE5	17 (9)	18 (30)	**Y142**
SPARE4	19 (10)	20 (29)	**Y141**
SPARE3	21 (11)	22 (28)	**Y140**
SPARE2	23 (12)	24 (27)	**Y139**
SPARE1	25 (13)	26 (26)	**Y138**
SPARE0	27 (14)	28 (25)	**Y137**
Y152	29 (15)	30 (24)	**Y136**
Y151	31 (16)	32 (23)	**Y135**
Y150	33 (17)	34 (22)	**Y134**
Y149	35 (18)	36 (21)	**Y133**
Y148	37 (19)	38 (20)	**Y132**

Table A-13 Mictor connector J18, JTAG and Y179-Y153

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
D_TCK (unbuffered)	5 (3)	6 (36)	**Y179**
Y177	7 (4)	8 (35)	**Y168**
D_nSRST	9 (5)	10 (34)	**Y167**
D_TDO	11 (6)	12 (33)	**Y166** (1KO pull up to **VCCO_Y**)
D_RTCK	13 (7)	14 (32)	**Y165** (1KO pull up to 3.3V)
D_TCK (unbuffered)	15 (8)	16 (31)	**Y164**
D_TMS	17 (9)	18 (30)	**Y163**
D_TDI	19 (10)	20 (29)	**Y162**
D_nTRST	21 (11)	22 (28)	**Y161**
Y176	23 (12)	24 (27)	**Y160**
Y175	25 (13)	26 (26)	**Y159**
Y174	27 (14)	28 (25)	**Y158**
Y173	29 (15)	30 (24)	**Y157**
Y172	31 (16)	32 (23)	**Y156**
Y171	33 (17)	34 (22)	**Y155**
Y170	35 (18)	36 (21)	**Y154**
Y169	37 (19)	38 (20)	**Y153**

Table A-14 Mictor connector J19, Z31-Z0

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_UP_PLUS1 (buffered)	5 (3)	6 (36)	**Z95**
Z31	7 (4)	8 (35)	**Z15**
Z30	9 (5)	10 (34)	**Z14**
Z29	11 (6)	12 (33)	**Z13**
Z28	13 (7)	14 (32)	**Z12**
Z27	15 (8)	16 (31)	**Z11**
Z26	17 (9)	18 (30)	**Z10**
Z25	19 (10)	20 (29)	**Z9**
Z24	21 (11)	22 (28)	**Z8**
Z23	23 (12)	24 (27)	**Z7**
Z22	25 (13)	26 (26)	**Z6**
Z21	27 (14)	28 (25)	**Z5**
Z20	29 (15)	30 (24)	**Z4**
Z19	31 (16)	32 (23)	**Z3**
Z18	33 (17)	34 (22)	**Z2**
Z17	35 (18)	36 (21)	**Z1**
Z16	37 (19)	38 (20)	**Z0**

Table A-15 Mictor connector J20, Z63-Z32

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_DN_MINUS1 (buffered)	5 (3)	6 (36)	**Z94**
Z63	7 (4)	8 (35)	**Z47**
Z62	9 (5)	10 (34)	**Z46**
Z61	11 (6)	12 (33)	**Z45**
Z60	13 (7)	14 (32)	**Z44**
Z59	15 (8)	16 (31)	**Z43**
Z58	17 (9)	18 (30)	**Z42**
Z57	19 (10)	20 (29)	**Z41**
Z56	21 (11)	22 (28)	**Z40**
Z55	23 (12)	24 (27)	**Z39**
Z54	25 (13)	26 (26)	**Z38**
Z53	27 (14)	28 (25)	**Z37**
Z52	29 (15)	30 (24)	**Z36**
Z51	31 (16)	32 (23)	**Z35**
Z50	33 (17)	34 (22)	**Z34**
Z49	35 (18)	36 (21)	**Z33**
Z48	37 (19)	38 (20)	**Z32**

Table A-16 Mictor connector J21, Z95-Z64

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_UP_PLUS2 (unbuffered)	5 (3)	6 (36)	**Z59**
Z95	7 (4)	8 (35)	**Z79**
Z94	9 (5)	10 (34)	**Z78**
Z93	11 (6)	12 (33)	**Z77**
Z92	13 (7)	14 (32)	**Z76**
Z91	15 (8)	16 (31)	**Z75**
Z90	17 (9)	18 (30)	**Z74**
Z89	19 (10)	20 (29)	**Z73**
Z88	21 (11)	22 (28)	**Z72**
Z87	23 (12)	24 (27)	**Z71**
Z86	25 (13)	26 (26)	**Z70**
Z85	27 (14)	28 (25)	**Z69**
Z84	29 (15)	30 (24)	**Z68**
Z83	31 (16)	32 (23)	**Z67**
Z82	33 (17)	34 (22)	**Z66**
Z81	35 (18)	36 (21)	**Z65**
Z80	37 (19)	38 (20)	**Z64**

Table A-17 Mictor connector J22, Z191-Z160

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_DN_MINUS2 (unbuffered)	5 (3)	6 (36)	**Z128**
Z191	7 (4)	8 (35)	**Z175**
Z190	9 (5)	10 (34)	**Z174**
Z189	11 (6)	12 (33)	**Z173**
Z188	13 (7)	14 (32)	**Z172**
Z187	15 (8)	16 (31)	**Z171**
Z186	17 (9)	18 (30)	**Z170**
Z185	19 (10)	20 (29)	**Z169**
Z184	21 (11)	22 (28)	**Z168**
Z183	23 (12)	24 (27)	**Z167**
Z182	25 (13)	26 (26)	**Z166**
Z181	27 (14)	28 (25)	**Z165**
Z180	29 (15)	30 (24)	**Z164**
Z179	31 (16)	32 (23)	**Z163**
Z178	33 (17)	34 (22)	**Z162**
Z177	35 (18)	36 (21)	**Z161**
Z176	37 (19)	38 (20)	**Z160**

Table A-18 Mictor connector J23, Z159-Z128

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_POS_UP (buffered)	5 (3)	6 (36)	**CLK_POS_DN** (buffered)
Z159	7 (4)	8 (35)	**Z143**
Z158	9 (5)	10 (34)	**Z142**
Z157	11 (6)	12 (33)	**Z141**
Z156	13 (7)	14 (32)	**Z140**
Z155	15 (8)	16 (31)	**Z139**
Z154	17 (9)	18 (30)	**Z138**
Z153	19 (10)	20 (29)	**Z137**
Z152	21 (11)	22 (28)	**Z136**
Z151	23 (12)	24 (27)	**Z135**
Z150	25 (13)	26 (26)	**Z134**
Z149	27 (14)	28 (25)	**Z133**
Z148	29 (15)	30 (24)	**Z132**
Z147	31 (16)	32 (23)	**Z131**
Z146	33 (17)	34 (22)	**Z130**
Z145	35 (18)	36 (21)	**Z129**

Table A-19 Mictor connector J24, Z255-Z224

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_UP_THRU (unbuffered)	5 (3)	6 (36)	**Z255**
Z255	7 (4)	8 (35)	**Z239**
Z254	9 (5)	10 (34)	**Z238**
Z253	11 (6)	12 (33)	**Z237**
Z252	13 (7)	14 (32)	**Z236**
Z251	15 (8)	16 (31)	**Z235**
Z250	17 (9)	18 (30)	**Z234**
Z249	19 (10)	20 (29)	**Z233**
Z248	21 (11)	22 (28)	**Z232**
Z247	23 (12)	24 (27)	**Z231**
Z246	25 (13)	26 (26)	**Z230**
Z245	27 (14)	28 (25)	**Z229**
Z244	29 (15)	30 (24)	**Z228**
Z243	31 (16)	32 (23)	**Z227**
Z242	33 (17)	34 (22)	**Z226**
Z241	35 (18)	36 (21)	**Z225**
Z240	37 (19)	38 (20)	**Z224**

Table A-20 Mictor connector J25, Z223-Z192

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_DN_THRU (unbuffered)	5 (3)	6 (36)	**Z129**
Z223	7 (4)	8 (35)	**Z207**
Z222	9 (5)	10 (34)	**Z206**
Z221	11 (6)	12 (33)	**Z205**
Z220	13 (7)	14 (32)	**Z204**
Z219	15 (8)	16 (31)	**Z203**
Z218	17 (9)	18 (30)	**Z202**
Z217	19 (10)	20 (29)	**Z201**
Z216	21 (11)	22 (28)	**Z200**
Z215	23 (12)	24 (27)	**Z199**
Z214	25 (13)	26 (26)	**Z198**
Z213	27 (14)	28 (25)	**Z197**
Z212	29 (15)	30 (24)	**Z196**
Z211	31 (16)	32 (23)	**Z195**
Z210	33 (17)	34 (22)	**Z194**
Z209	35 (18)	36 (21)	**Z193**
Z208	37 (19)	38 (20)	**Z192**

Table A-21 Mictor connector J26, Z127-Z96

Tile signal	Agilent pin number (Tektronix number)		Tile signal
NC	1 (1)	2 (38)	NC
GND	3 (2)	4 (37)	NC
CLK_GLOBAL (buffered)	5 (3)	6 (36)	**Z44**
Z127	7 (4)	8 (35)	**Z111**
Z126	9 (5)	10 (34)	**Z110**
Z125	11 (6)	12 (33)	**Z109**
Z124	13 (7)	14 (32)	**Z108**
Z123	15 (8)	16 (31)	**Z107**
Z122	17 (9)	18 (30)	**Z106**
Z121	19 (10)	20 (29)	**Z105**
Z120	21 (11)	22 (28)	**Z104**
Z119	23 (12)	24 (27)	**Z103**
Z118	25 (13)	26 (26)	**Z102**
Z117	27 (14)	28 (25)	**Z101**
Z116	29 (15)	30 (24)	**Z100**
Z115	31 (16)	32 (23)	**Z99**
Z114	33 (17)	34 (22)	**Z98**
Z113	35 (18)	36 (21)	**Z97**
Z112	37 (19)	38 (20)	**Z96**

A.3 Tile connections

This section lists the signals on the tile connectors.

Note

Unlike the signals on Logic Tiles, all Analyzer Tile signals are the same on both the top and bottom tile connectors and there is no rotation or buffering of signals.

A.3.1 HDRX

Table A-22 describes the signals on the HDRX pins.

Table A-22 HDRX signals

Signal	Pin	Pin	Signal
Xx90	1	2	**Xx89**
Xx91	3	4	**Xx88**
Xx92	5	6	**Xx87**
Xx93	7	8	**Xx86**
Xx94	9	10	**Xx85**
Xx95	11	12	**Xx84**
Xx96	13	14	**Xx83**
Xx97	15	16	**Xx82**
Xx98	17	18	**Xx81**
Xx99	19	20	**Xx80**
Xx100	21	22	**Xx79**
Xx101	23	24	**Xx78**
Xx102	25	26	**Xx77**
Xx103	27	28	**Xx76**
Xx104	29	30	**Xx75**
Xx105	31	32	**Xx74**
Xx106	33	34	**Xx73**

Table A-22 HDRX signals (continued)

Signal	Pin	Pin	Signal
Xx107	35	36	**Xx72**
Xx108	37	38	**Xx71**
Xx109	39	40	**Xx70**
Xx110	41	42	**Xx69**
Xx111	43	44	**Xx68**
Xx112	45	46	**Xx67**
Xx113	47	48	**Xx66**
Xx114	49	50	**Xx65**
Xx115	51	52	**Xx64**
Xx116	53	54	**Xx63**
Xx117	55	56	**Xx62**
Xx118	57	58	**Xx61**
Xx119	59	60	**Xx60**
Xx120	61	62	**Xx59**
Xx121	63	64	**Xx58**
Xx122	65	66	**Xx57**
Xx123	67	68	**Xx56**
Xx124	69	70	**Xx55**
Xx125	71	72	**Xx54**
Xx126	73	74	**Xx53**
Xx127	75	76	**Xx52**
Xx128	77	78	**Xx51**
Xx129	79	80	**Xx50**
Xx130	81	82	**Xx49**
Xx131	83	84	**Xx48**

Table A-22 HDRX signals (continued)

Signal	Pin	Pin	Signal
Xx132	85	86	**Xx47**
Xx133	87	88	**Xx46**
Xx134	89	90	**Xx45**
Xx135	91	92	**Xx44**
Xx136	93	94	**Xx43**
Xx137	95	96	**Xx42**
Xx138	97	98	**Xx41**
Xx139	99	100	**Xx40**
Xx140	101	102	**Xx39**
Xx141	103	104	**Xx38**
Xx142	105	106	**Xx37**
Xx143	107	108	**Xx36**
Xx144	109	110	**Xx35**
Xx145	111	112	**Xx34**
Xx146	113	114	**Xx33**
Xx147	115	116	**Xx32**
Xx148	117	118	**Xx31**
Xx149	119	120	**Xx30**
Xx150	121	122	**Xx29**
Xx151	123	124	**Xx28**
Xx152	125	126	**Xx27**
Xx153	127	128	**Xx26**
Xx154	129	130	**Xx25**
Xx155	131	132	**Xx24**
Xx156	133	134	**Xx23**

Table A-22 HDRX signals (continued)

Signal	Pin	Pin	Signal
Xx157	135	136	**Xx22**
Xx158	137	138	**Xx21**
Xx159	139	140	**Xx20**
Xx160	141	142	**Xx19**
Xx161	143	144	**Xx18**
Xx162	145	146	**Xx17**
Xx163	147	148	**Xx16**
Xx164	149	150	**Xx15**
Xx165	151	152	**Xx14**
Xx166	153	154	**Xx13**
Xx167	155	156	**Xx12**
Xx168	157	158	**Xx11**
Xx169	159	160	**Xx10**
Xx170	161	162	**Xx9**
Xx171	163	164	**Xx8**
Xx172	165	166	**Xx7**
Xx173	167	168	**Xx6**
Xx174	169	170	**Xx5**
Xx175	171	172	**Xx4**
Xx176	173	174	**Xx3**
Xx177	175	176	**Xx2**
Xx178	177	178	**Xx1**
Xx179	179	180	**Xx0**

A.3.2 HDRY

Table A-23 describes the signals on the HDRY pins.

Table A-23 HDRY signals

	Odd pins	Even pins	
Signal	**Pin**	**Pin**	**Signal**
Yx89	1	2	**Yx90**
Yx88	3	4	**Yx91**
Yx87	5	6	**Yx92**
Yx86	7	8	**Yx93**
Yx85	9	10	**Yx94**
Yx84	11	12	**Yx95**
Yx83	13	14	**Yx96**
Yx82	15	16	**Yx97**
Yx81	17	18	**Yx98**
Yx80	19	20	**Yx99**
Yx79	21	22	**Yx100**
Yx78	23	24	**Yx101**
Yx77	25	26	**Yx102**
Yx76	27	28	**Yx103**
Yx75	29	30	**Yx104**
Yx74	31	32	**Yx105**
Yx73	33	34	**Yx106**
Yx72	35	36	**Yx107**
Yx71	37	38	**Yx108**
Yx70	39	40	**Yx109**
Yx69	41	42	**Yx110**
Yx68	43	44	**Yx111**

Table A-23 HDRY signals (continued)

	Odd pins	Even pins	
Signal	**Pin**	**Pin**	**Signal**
Yx67	45	46	**Yx112**
Yx66	47	48	**Yx113**
Yx65	49	50	**Yx114**
Yx64	51	52	**Yx115**
Yx63	53	54	**Yx116**
Yx62	55	56	**Yx117**
Yx61	57	58	**Yx118**
Yx60	59	60	**Yx119**
Yx59	61	62	**Yx120**
Yx58	63	64	**Yx121**
Yx57	65	66	**Yx122**
Yx56	67	68	**Yx123**
Yx55	69	70	**Yx124**
Yx54	71	72	**Yx125**
Yx53	73	74	**Yx126**
Yx52	75	76	**Yx127**
Yx51	77	78	**Yx128**
Yx50	79	80	**Yx129**
Yx49	81	82	**Yx130**
Yx48	83	84	**Yx131**
Yx47	85	86	**Yx132**
Yx46	87	88	**Yx133**
Yx45	89	90	**Yx134**
Yx44	91	92	**Yx135**

Table A-23 HDRY signals (continued)

	Odd pins	Even pins	
Signal	**Pin**	**Pin**	**Signal**
Yx43	93	94	**Yx136**
Yx42	95	96	**Yx137**
Yx41	97	98	**Yx138**
Yx40	99	100	**Yx139**
Yx39	101	102	**Yx140**
Yx38	103	104	**Yx141**
Yx37	105	106	**Yx142**
Yx36	107	108	**Yx143**
Yx35	109	110	**Yx144**
Yx34	111	112	**Yx145**
Yx33	113	114	**Yx146**
Yx32	115	116	**Yx147**
Yx31	117	118	**Yx148**
Yx30	119	120	**Yx149**
Yx29	121	122	**Yx150**
Yx28	123	124	**Yx151**
Yx27	125	126	**Yx152**
Yx26	127	128	**Yx153**
Yx25	129	130	**Yx154**
Yx24	131	132	**Yx155**
Yx23	133	134	**Yx156**
Yx22	135	136	**Yx157**
Yx21	137	138	**Yx158**
Yx20	139	140	**Yx159**

Table A-23 HDRY signals (continued)

	Odd pins	Even pins	
Signal	**Pin**	**Pin**	**Signal**
Yx19	141	142	**Yx160**
Yx18	143	144	**Yx161**
Yx17	145	146	**Yx162**
Yx16	147	148	**Yx163**
Yx15	149	150	**Yx164**
Yx14	151	152	**Yx165**
Yx13	153	154	**Yx166**
Yx12	155	156	**Yx167**
Yx11	157	158	**Yx168**
Yx10	159	160	**Yx169**
Yx9	161	162	**Yx170**
Yx8	163	164	**Yx171**
Yx7	165	166	**Yx172**
Yx6	167	168	**Yx173**
Yx5	169	170	**Yx174**
Yx4	171	172	**Yx175**
Yx3	173	174	**Yx176**
Yx2	175	176	**Yx177**
Yx1	177	178	**Yx178**
Yx0	179	180	**Yx179**

A.3.3 HDRZ

Table A-24 describes the signals on the HDRZ pins.

Table A-24 HDRZ signals

Signal	Pin	Pin	Signal
Z128	1	2	**Z255**
Z129	3	4	**Z254**
Z130	5	6	**Z253**
Z131	7	8	**Z252**
Z132	9	10	**Z251**
Z133	11	12	**Z250**
Z134	13	14	**Z249**
Z135	15	16	**Z248**
Z136	17	18	**Z247**
Z137	19	20	**Z246**
Z138	21	22	**Z245**
Z139	23	24	**Z244**
Z140	25	26	**Z243**
Z141	27	28	**Z242**
Z142	29	30	**Z241**
Z143	31	32	**Z240**
Z144	33	34	**Z239**
Z145	35	36	**Z238**
Z146	37	38	**Z237**
Z147	39	40	**Z236**
Z148	41	42	**Z235**
Z149	43	44	**Z234**
Z150	45	46	**Z233**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
Z151	47	48	**Z232**
Z152	49	50	**Z231**
Z153	51	52	**Z230**
Z154	53	54	**Z229**
Z155	55	56	**Z228**
Z156	57	58	**Z227**
Z157	59	60	**Z226**
Z158	61	62	**Z225**
Z159	63	64	**Z224**
Z160	65	66	**Z223**
Z161	67	68	**Z222**
Z162	69	70	**Z221**
Z163	71	72	**Z220**
Z164	73	74	**Z219**
Z165	75	76	**Z218**
Z166	77	78	**Z217**
Z167	79	80	**Z216**
Z168	81	82	**Z215**
Z169	83	84	**Z214**
Z170	85	86	**Z213**
Z171	87	88	**Z212**
Z172	89	90	**Z211**
Z173	91	92	**Z210**
Z174	93	94	**Z209**
Z175	95	96	**Z208**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
Z176	97	98	**Z207**
Z177	99	100	**Z206**
Z178	101	102	**Z205**
Z179	103	104	**Z204**
Z180	105	106	**Z203**
Z181	107	108	**ZU202**
Z182	109	110	**ZU201**
Z183	111	112	**ZU200**
Z184	113	114	**ZU199**
Z185	115	116	**ZU198**
Z186	117	118	**ZU197**
Z187	119	120	**ZU196**
Z188	121	122	**ZU195**
Z189	123	124	**ZU194**
Z190	125	126	**ZU193**
Z191	127	128	**ZU192**
D_nSRST	129	130	**CLK_POS_DN_IN**
D_nTRST	131	132	**CLK_NEG_DN_IN**
D_TDO_OUT	133	134	**CLK_POS_UP_OUT**
D_TDI	135	136	**CLK_NEG_UP_OUT**
D_TCK_IN	137	138	**CLK_UP_THRU**
D_TMS_IN	139	140	**CLK_OUT_PLUS1**
D_RTCK	141	142	**CLK_OUT_PLUS2**
C_nSRST	143	144	**CLK_IN_PLUS2**
C_nTRST	145	146	**CLK_IN_PLUS1**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
C_TDO_OUT	147	148	**CLK_DN_THRU**
C_TDI	149	150	**CLK_GLOBAL**
C_TCK_IN	151	152	**FPGA_IMAGE**
C_TMS_IN	153	154	**nSYSPOR**
GND	155	156	**nSYSRST**
nCFGEN	157	158	**nRTCKEN**
GLOBAL_DONE	159	160	**SPARE12** (reserved)
SPARE11 (reserved)	161	162	**SPARE10** (reserved)
SPARE9 (reserved)	163	164	**SPARE8** (reserved)
SPARE7 (reserved)	165	166	**SPARE6** (reserved)
SPARE5 (reserved)	167	168	**SPARE4** (reserved)
SPARE3 (reserved)	169	170	**SPARE2** (reserved)
SPARE1 (reserved)	171	172	**SPARE0** (reserved)
Z63	173	174	**Z64**
Z62	175	176	**Z65**
Z61	177	178	**Z66**
Z60	179	180	**Z67**
Z59	181	182	**Z68**
Z58	183	184	**Z69**
Z57	185	186	**Z70**
Z56	187	188	**Z71**
Z55	189	190	**Z72**
Z54	191	192	**Z73**
Z53	193	194	**Z74**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
Z52	195	196	**Z75**
Z51	197	198	**Z76**
Z50	199	200	**Z77**
Z49	201	202	**Z78**
Z48	203	204	**Z79**
Z47	205	206	**Z80**
Z46	207	208	**Z81**
Z45	209	210	**Z82**
Z44	211	212	**Z83**
Z43	213	214	**Z84**
Z42	215	216	**Z85**
Z41	217	218	**Z86**
Z40	219	220	**Z87**
Z39	221	222	**Z88**
Z38	223	224	**Z89**
Z37	225	226	**Z90**
Z36	227	228	**Z91**
Z35	229	230	**Z92**
Z34	231	232	**Z93**
Z33	233	234	**Z94**
Z32	235	236	**Z95**
Z31	237	238	**Z96**
Z30	239	240	**Z97**
Z29	241	242	**Z98**
Z28	243	244	**Z99**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
Z27	245	246	**Z100**
Z26	247	248	**Z101**
Z25	249	250	**Z102**
Z24	251	252	**Z103**
Z23	253	254	**Z104**
Z22	255	256	**Z105**
Z21	257	258	**Z106**
Z20	259	260	**Z107**
Z19	261	262	**Z108**
Z18	263	264	**Z109**
Z17	265	266	**Z110**
Z16	267	268	**Z111**
Z15	269	270	**Z112**
Z14	271	272	**Z113**
Z13	273	274	**Z114**
Z12	275	276	**Z115**
Z11	277	278	**Z116**
Z10	279	280	**Z117**
Z9	281	282	**Z118**
Z8	283	284	**Z119**
Z7	285	286	**Z120**
Z6	287	288	**Z121**
Z5	289	290	**Z122**
Z4	291	292	**Z123**
Z3	293	294	**Z124**

Table A-24 HDRZ signals (continued)

Signal	Pin	Pin	Signal
Z2	295	296	**Z125**
Z1	297	298	**Z126**
Z0	299	300	**Z127**

A.4 Electrical specification

This section provides details of the voltage and current characteristics for the Analyzer Tile.

A.4.1 Bus interface characteristics

Table A-25 shows the Analyzer Tile electrical characteristics.

Table A-25 Electrical characteristics for 3.3V I/O

Symbol	Description	Min	Max	Unit
V_{IH}	High-level input voltage	2.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage	2.4	-	V
V_{OL}	Low-level output voltage	-	0.4	V

A.4.2 Current requirements

Table A-26 shows the current requirements at room temperature and nominal voltage for an Analyzer Tile.

Table A-26 Current requirements

At 3.3V	At 5V
100mA	not used

A.5 Mechanical specification

The Analyzer Tile measurements are shown in Figure A-2.

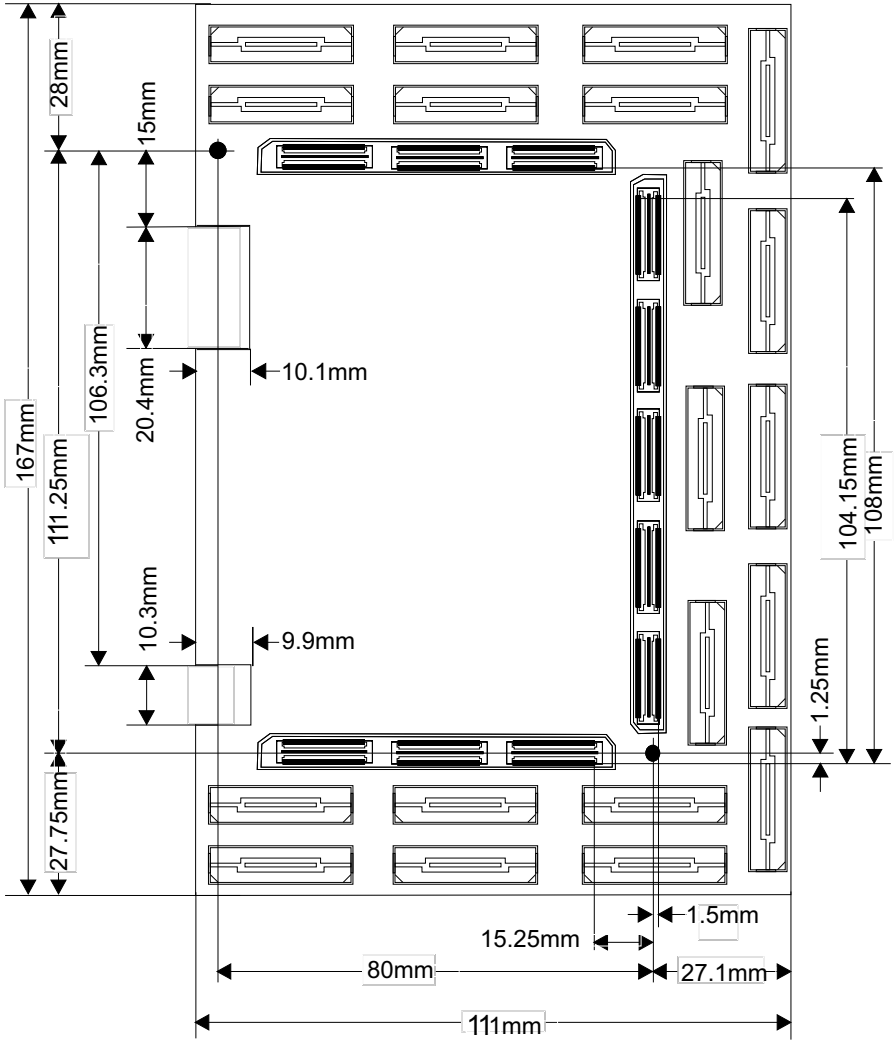

Figure A-2 Analyzer Tile measurements