# ARM® CoreLink™ QVN-400 Network Interconnect Advanced Quality of Service using Virtual Networks

**Revision: r1p0**

## Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual

ARM®


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# ARM CoreLink QVN-400 Network Interconnect Advanced Quality of Service using Virtual Networks

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### Release Information

The following changes have been made to this book.

**Change history**

| Date | Issue | Confidentiality | Change |
|---|---|---|---|
| 08 August 2012 | A | Non-Confidential | First release for r0p0 |
| 07 May 2013 | B | Non-Confidential | First release for r0p1 |
| 11 December 2013 | C | Non-Confidential | First release for r0p2 |
| 07 March 2014 | D | Non-Confidential | First release for r0p3 |
| 10 December 2015 | E | Confidential | First release for r1p0 Beta |
| 04 March 2016 | F | Non-Confidential | Second release for r1p0 |

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### Confidentiality Status

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### Product Status

The information in this document is final, that is for a developed product.

### Web Address

`http://www.arm.com`

# Contents

# ARM CoreLink QVN-400 Network Interconnect Advanced Quality of Service using Virtual Networks Supplement to ARM CoreLink NIC-400 Network Interconnect Technical Reference Manual

# Chapter 1
# **Introduction**

This chapter introduces the CoreLink QVN-400 Network Interconnect Advanced Quality of Service for Virtual Networks. It contains the following sections:

## 1.1 About the product

The CoreLink QVN-400 Network Interconnect Advanced Quality of Service for *Virtual Networks* (VNs) is an extension to the CoreLink NIC-400 Network Interconnect base product. This extension provides a mechanism to avoid head-of-line blocking and cross-path blocking between different data flows.

## 1.2 Key features

The CoreLink QVN-400 Network Interconnect Advanced Quality of Service for *Virtual Networks* has the following key features:

- Enables the prevention of congestion between traffic flows in the system, by enabling the system designer to separate masters with conflicting requirements on to different VNs. For example, high-bandwidth bus traffic sources can be separated to prevent blocking the flow of latency critical bus traffic.
- You can configure up to eight VNs.
- You can configure a maximum of four VNs on any single master or slave interface. You can configure virtual networks by assigning them to the addressable paths between masters and slaves.
- You can configure a maximum of four virtual networks on any single connection between master and slave interfaces within the NIC.
- You can configure the virtual network token request mechanism to be exported with the master and slave interfaces.
- Works over interconnects configured as AXI3 and AXI4.
- Works with the other licensable features, for example QoS-400 and TLX-400.
- You can configure slave and master interfaces for lower latency by pre-allocating tokens.
- You can dynamically mask low priority transactions from a VN termination ports arbitration.

## 1.3 Relationship between the product, AMBA Designer, and CoreLink Creator

The CoreLink QVN-400 Network Interconnect is not a stand-alone product, but integrates with the NIC-400 system. The features defined by this product are configured using the AMBA Designer, or CoreLink Creator tools, as part of the NIC-400 configuration flow when enabled with a suitable license.

## 1.4 Product revisions

This section describes the differences in functionality between product revisions:

**r0p0** First release.

**r0p1** Second release. No technical changes.

**r0p2** Third release. No technical changes.

**r0p3** Fourth release. No technical changes.

**r1p0** Fifth release. No technical changes.

**r1p0** Sixth release. Functionality to describe VNs termination arbitration options.

# Chapter 2
# **Functional Description**

This chapter provides a functional overview of the QVN-400 Network Interconnect Advanced Quality of Service for Virtual Networks. It contains the following sections:

## 2.1 Interfaces

QVN-400 enables QVN protocol functionality to be added to NIC-400 slave and master interfaces.

**Note**

- QVN configurations do not support lock functionality.
- Locks would introduce blocks between virtual networks.

The following subsections describe:

- *Slave interfaces*.
- *Master interfaces* on page 2-3.

### 2.1.1 Slave interfaces

In a QVN-enabled configuration, every slave interface must be assigned to at least one VN. Every master interface that is addressable from a particular slave interface must be assigned to one of the VNs that is enabled on that slave interface.

A slave interface can support up to four VNs.

If the slave interface is configured to be AHB then only one VN can be supported.

If the slave interface requires more than one VN then the external master interface has to support:

- A read and write issuing capability that is greater or equal to the number of VNs required.
- An ID width that is wide enough to enable at least one outstanding transaction on each VN with a unique ID. This is required to support the QVN protocol rule that outstanding transactions on different VNs must have different IDs.

When a transaction address is decoded to determine the destination, the VN is also determined. If an address does not decode to a VN that the slave interface supports, then the transaction is routed to the default slave, which responds with a decode error.

#### Connecting to VNs outside of the NIC-400

A slave interface can support virtual networks externally if the slave interface is also configured:

- To be either an AXI3 or AXI4 protocol slave.
- With between two and four VNs.

When an interface can connect to external VNs, then the QVN protocol specification permits multiplexing of different write data beats from different transactions as long as they are on different VNs.

The QVN protocol ensures that a transaction cannot be issued across an interface unless there is space allocated for it at the destination. This requires a token handshake to communicate that information. See the *ARM® CoreLink™ QVN Protocol Specification*.

**Note**

The *ARM® CoreLink™ QVN Protocol Specification* is available from ARM. This is a confidential document and a separate license is required.

The QVN protocol specification defines two modes of operation:

- With pre-allocated tokens.

- Without pre-allocated tokens.

You can configure the NIC-400 to support either mode of operation individually for each VN on each interface.

The incoming address is still decoded at the slave interface to determine the VN that is to be used. If the incoming address and decoded VN do not map to a slave that has been configured to be on that VN, then the transaction is completed with a decode error.

See *Functional Requirements* in the *ARM® CoreLink™ QVN Protocol Specification.*

### 2.1.2 Master interfaces

In a QVN-enabled configuration every master interface must be assigned to at least one VN.

A master interface can support up to four VNs.

If the master interface is configured to be AHB or APB, then only one VN can be supported.

If a master interface requires more than one VN, then the external slave interface must support:

- A read and write issuing capability that is greater or equal to the number of VNs required.
- An ID width that is wide enough to enable at least one transaction outstanding on each VN with a unique ID. This is required to support the QVN protocol rule that outstanding transactions on different VNs must have different IDs.

#### Connecting to VNs outside of the NIC-400

A master interface can support virtual networks externally if the master interface is also configured:

- To be either an AXI3 or AXI4 protocol slave.
- With between two and four VNs.

When an interface can connect to external VNs, then the QVN protocol specification permits multiplexing of different write data beats from different transactions as long as they are on different VNs.

See *Functional Requirements* in the *ARM® CoreLink™ QVN Protocol Specification*.

#### Terminating VNs at the master interface

When a master interface does not support VNs externally, if there is more than one VN, then arbitration between the VNs is done using the QoS value at each transaction.

For AXI3 or AXI4 master interfaces, there are extra signals **vawqosaccept_<block_name>_portname>** and **varqosaccept_<block_name>_portname>**.

- Any write transaction with a QoS value less than the current **vawqosaccept_<block_name>_portname>** setting is not considered for arbitration.
- Any read transaction with a QoS value less than the current **varqosaccept_<block_name>_<portname>** setting is not considered for arbitration.

You can change **vawqosaccept_<block_name>_portname>** and **varqosaccept_<block_name>_portname>** values dynamically. If you do not require this functionality, tie-off these signals to 0.

## 2.2 Operation

The protocol uses tokens to control transaction flows. For more information, see the *ARM® CoreLink™ QVN Protocol Specification*.

**Note**

The *ARM® CoreLink™ QVN Protocol Specification* is available from ARM. This is a confidential document and a separate license is required.

# Appendix A
# **Revisions**

This appendix describes the technical changes between released issues of this book.

**Table A-1 Issue A**

| Change | Location | Affects |
|---|---|---|
| First release | - | - |

**Table A-2 Differences between issue A and issue B**

| Change | Location | Affects |
|---|---|---|
| No technical changes, but section updated for clarification | *Connecting to VNs outside of the NIC-400* on page 2-2 | All revisions |

**Table A-3 Differences between issue B and issue C**

| Change | Location | Affects |
|---|---|---|
| No technical changes | - | r0p2 |

**Table A-4 Differences between issue C and issue D**

| Change | Location | Affects |
|---|---|---|
| No technical changes | - | r0p3 |

**Table A-5 Differences between issue D and issue E**

| Change | Location | Affects |
|---|---|---|
| No technical changes | - | r1p0 |

**Table A-6 Differences between issue E and issue F**

| Change | Location | Affects |
|---|---|---|
| Added bullet to Key features on dynamically masking of low transactions | *Key features* on page 1-3 | r1p0 |
| Updated section to include CoreLink Creator | *Relationship between the product, AMBA Designer, and CoreLink Creator* on page 1-4 | r1p0 |
| Updated section | *Product revisions* on page 1-5 | r1p0 |
| Added subsection on Terminating VNs at the master interface | *Terminating VNs at the master interface* on page 2-3 | r1p0 |