ARM® CoreLink™ SIE-200 System IP for Embedded

Revision: r3p1

Technical Reference Manual

ARM®

ARM DDI 0571G (ID061717)

ARM CoreLink SIE-200 System IP for Embedded
Technical Reference Manual

Release Information

The following changes have been made to this document:

Change history

Date	Issue	Confidentiality	Change
4 March 2016	A	Confidential draft	First release of r0p0
24 June 2016	B	Confidential	Beta release of r0p0
29 July 2016	C	Confidential	Beta update of r0p0
28 September 2016	D	Confidential	First release of r1p0 LAC
16 December 2016	E	Non-Confidential	First release of r2p0 EAC
31 March 2017	F	Non-Confidential	First release of r3p0 EAC2
7 June 2017	G	Non-Confidential	First release of r3p1 REL

Proprietary Notice

ARM Limited. Company 02557590 registered in England.

110 Fulbourn Road, Cambridge, England CB1 9NJ.

LES-PRE-20349

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Contents
ARM CoreLink SIE-200 System IP for Embedded Technical Reference Manual

Preface

This preface introduces the *ARM® CoreLink ™ SIE-200 System IP for Embedded Technical Reference Manual*. It contains the following sections:

About this book

This is the *Technical Reference Manual* (TRM) for the CoreLink SIE-200 System IP for Embedded product.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for system designers to design products with the ARM Cortex®-M processors that conform to the ARMv8-M processor architecture.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the system IP.

Chapter 2 *Functional Description*

Read this for an overview of the major functional components and the operation of the system IP.

Chapter 3 *Programmers Model*

Read this for an the registers and memory map for components that have a programming interface.

Appendix A *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM® Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM® Glossary* `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Typographical Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page viii.
- *Timing diagrams* on page viii.
- *Signals* on page viii.

Typographical conventions

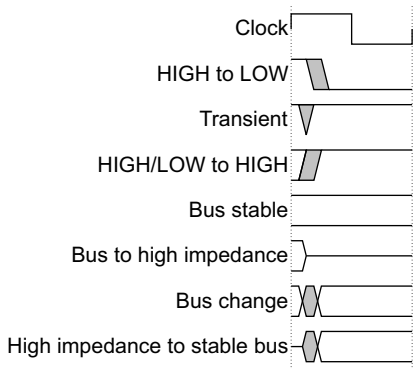
The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Signals

The signal conventions are:

Signal-level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Cortex®-M3 Technical Reference Manual* (ARM DDI 0337).

The following confidential books are only available to licensees:

- *ARM® CoreLink™ SIE-200 System IP for Embedded Configuration and Integration Manual* (ARM DIT 0067).
- *ARM® AMBA® 5 AHB Protocol Specification* (ARM IHI 0033).
- *ARM® AMBA® APB Protocol Specification* (ARM IHI 0024).
- *ARM® Low Power Interface Specification* (ARM IHI 0068).
- *ARMv8-M Architecture Reference Manual* (ARM DDI 0553).

Other publications

This section lists relevant documents published by third parties:

- JEDEC website www.jedec.org.
- Accellera website www.accellera.org.

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, ARM DDI 0571G.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

ARM tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter introduces the CoreLink SIE-200 System IP for Embedded. It contains the following sections:

1.1 About the CoreLink SIE-200 System IP for Embedded

The CoreLink SIE-200 System IP for Embedded product is a collection of interconnect, peripheral, and TrustZone® controller components for use with a processor that complies with the ARMv8-M processor architecture.

1.1.1 Bus architecture

CoreLink SIE-200 System IP for Embedded supports the following bus protocols:

- AMBA 5 AHB5 Protocol.
- AMBA 3 AHB-Lite Protocol.
- AMBA 4 APB4 Protocol.
- AMBA 3 APB3 Protocol.

Bus naming convention

It is important to always view each AMBA point-to-point connection as a master to slave connection. To distinguish between external AMBA masters or slaves and the conceptual masters or slaves on the component, masters and slaves on the interconnect are referred to as master ports or slave ports. External masters and slaves are referred to as masters and slaves.

1.1.2 Design and verification components

CoreLink SIE-200 System IP for Embedded consists of the following components and models:

- *AHB5 system components*.
- *AHB5 bridge components*.
- *TrustZone Protection controllers* on page 1-3.
- *Verification components* on page 1-3.

AHB5 system components

The AHB5 system components are:

- AHB5 bus matrix.
- AHB5 default slave.
- AHB5 example slave.
- AHB5 exclusive access monitor.
- AHB5 GPIO.
- AHB5 master multiplexer.
- AHB5 slave multiplexer.
- AHB5 timeout monitor.
- AHB5 to external SRAM interface.
- AHB5 to ROM interface.
- AHB5 to internal SRAM interface module.
- Cortex-M3/Cortex-M4 AHB5 adapter.

AHB5 bridge components

The AHB5 bridge components are:

- AHB5 access control gate.
- AHB5 downsizer.

- AHB5 to AHB5 and APB4 asynchronous bridge.
- AHB5 to AHB5 sync-down bridge.
- AHB5 to ABH5 low-latency sync-down bridge.
- AHB5 to AHB5 synchronous bridge.
- AHB5 to AHB5 sync-up bridge.
- AHB5 to AHB5 low-latency sync-up bridge.
- AHB5 to APB4 asynchronous bridge.
- AHB5 to APB4 sync-down bridge.
- AHB5 to APB4 low-latency sync-down bridge.
- AHB5 upsizer.

TrustZone Protection controllers

The TrustZone components are:

- AHB5 TrustZone master security controller.
- AHB5 TrustZone memory protection controller.
- AHB5 TrustZone peripheral protection controller.
- APB4 TrustZone peripheral protection controller.

Verification components

- AHB5 FRBM.
- Behavioral SRAM model with an AHB5 interface.
- External asynchronous 8-bit SRAM model.
- External asynchronous 16-bit SRAM model.
- FPGA SRAM synthesizable model.
- RAM wrapper model.
- ROM behavioral model.
- ROM wrapper model.

1.2 Product revisions

This section describes the differences in functionality between product revisions of the CoreLink SIE-200 System IP for Embedded:

r0p0 First release.

r1p0 Second release. Functional improvement to AMBA® AHB5 downsizer.

r2p0 Third release. Added the following:

- AHB5 example slave.
- AHB5 GPIO.
- AHB5 timeout monitor.
- AHB5 to external SRAM interface.
- AHB5 to ROM interface.
- Cortex-M3/Cortex-M4 AHB5 adapter.
- Behavioral SRAM model with an AHB5 interface.
- External asynchronous 8-bit SRAM model.
- External asynchronous 16-bit SRAM model.
- FPGA SRAM synthesizable model.
- RAM wrapper model.
- ROM behavioral model.
- ROM wrapper model.

r3p0 Fourth release. Added the following:

- ABHB5 to AHB5 low-latency sync-down bridge.
- AHB5 to AHB5 low-latency sync-up bridge.
- ABH5 to APB4 low-latency sync-down bridge.

Note

The low-latency bridges in release r3p0 are similar in function to their non-low-latency equivalents. They are options for designs that do not require Q-channel support for power management.

This option enables optimization for reduced latency in these three bridges.

r3p1 REL quality release. No feature increment.

Chapter 2
Functional Description

This chapter describes the components supplied with the CoreLink SIE-200 System IP for Embedded product.

The following sections describe the system components provided in the CoreLink SIE-200 System IP for Embedded:

- *AHB5 bus matrix* on page 2-3.
- *AHB5 default slave* on page 2-8.
- *AHB5 example slave* on page 2-10.
- *AHB5 exclusive access monitor* on page 2-12.
- *AHB5 GPIO* on page 2-17.
- *AHB5 master multiplexer* on page 2-20.
- *AHB5 slave multiplexer* on page 2-24.
- *AHB5 timeout monitor* on page 2-28.
- *AHB5 to external SRAM interface* on page 2-32.
- *AHB5 to ROM interface* on page 2-37.
- *AHB5 to internal SRAM interface module* on page 2-40.
- *Cortex-M3/Cortex-M4 AHB5 adapter* on page 2-44.

The following sections describe the SIE-200 AHB5 bridge components:

- *Comparison between bridges and their low-latency versions* on page 2-49.
- *AHB5 access control gate* on page 2-50.
- *AHB5 downsizer* on page 2-55.
- *AHB5 to AHB5 and APB4 asynchronous bridge* on page 2-59.
- *AHB5 to AHB5 sync-down bridge* on page 2-65.
- *AHB5 to AHB5 low-latency sync-down bridge* on page 2-70.

The following sections describe the SIE-200 TrustZone Protection components:

The following sections describe the SIE-200 verification components:

2.1 AHB5 bus matrix

This section describes the AHB5 bus matrix.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-5.
- *AHB5 bus properties* on page 2-7.

2.1.1 Functional description

The AHB5 bus matrix connects other AHB5 components through its slave and master ports.

The bus matrix has the following configurable features:

- Number of slave ports, from 1-16.
- Number of master ports, from 1-16.
- Data width, either 32 bits or 64 bits.
- Address width, from 32-64 bits.
- Arbiter types: round, fixed, burst, round_nolat, burst_nolat, and fixed_nolat.
- Optional **xUSER** signals, from 0-32 bits.
- Sparse connectivity:
  - The sparse connectivity feature removes any unnecessary connections, and reduces area and multiplexer delays.
  - Separate instances of the output stage and output arbiter are generated for each master port.
  - For input-output stages with only one sparse connection, the choice of arbiter is overridden with single arbiter and output stage modules. These single modules also permit 1x*n* interconnects.
- Design entry by XML configuration file that enables you to specify an address map, including REMAP support.
- User-specified module names or automatically derived top-level name.
- User-specified port suffixes.
- User-specified source and target directories.
- Optional `timescale Verilog directives.

The following figure shows the bus matrix module.

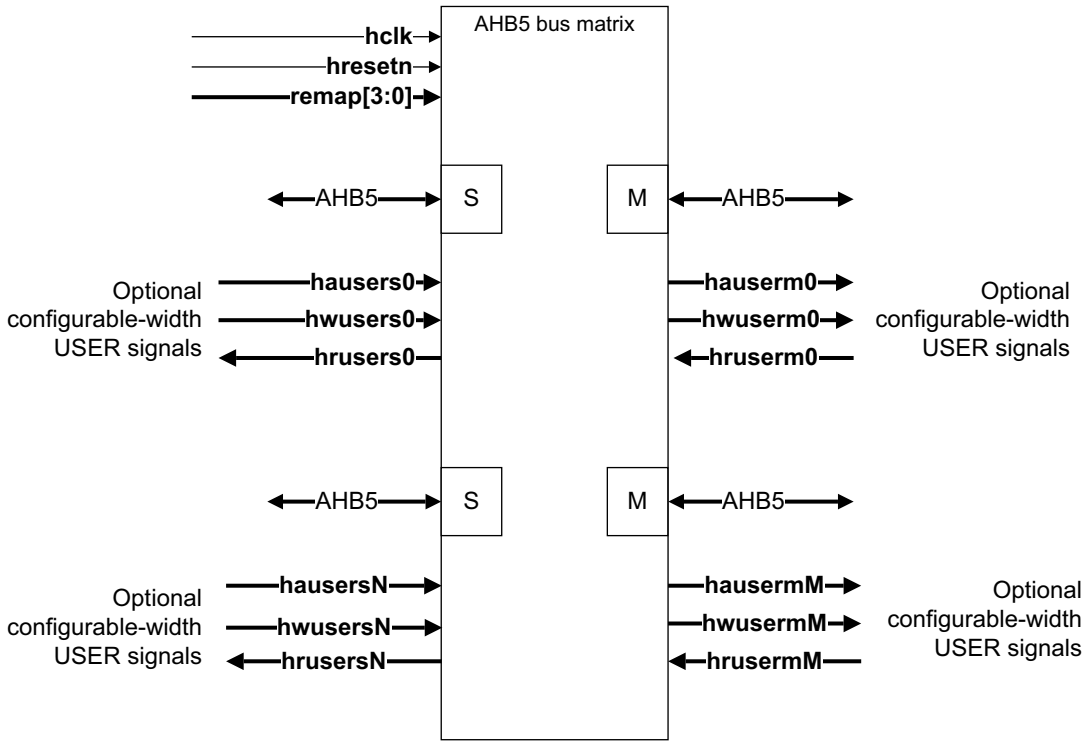


Figure 2-1 AHB 5 bus matrix

Arbitration

The arbitration in the bus matrix module determines the input port that has access to the shared slave, and each shared slave has its own arbitration. Different arbitration schemes provide different system characteristics in terms of access latency and overall system performance.

The slave switch supports the following arbitration schemes:

Fixed arbitration

This is the simplest scheme, which only provides simple selection. It provides access for the next input port when the current port has finished. The lowest order input port has priority.

Fixed (burst) arbitration

This is similar to fixed arbitration, but it does not break defined length burst transfers.

Round-robin arbitration

This is similar to burst arbitration, but it adds round robin priority handling.

Note

The arbitration schemes have two options, with or without latency. The schemes with latency insert an extra cycle each time the downstream port selects a new upstream port to service, but the others do not insert the extra cycle.

The default arbitration is round-robin with latency.

2.1.2 Port list

The following table shows the port list of the AHB5 bus matrix.

Table 2-1 AHB5 bus matrix port list

Block	SIGNAL	CONDITION	DIRECTION	DESCRIPTION
System	**hclk**		Input	Clock
	hresetn		Input	Reset
AHB5 Slave [for each slave interface defined]	**hsel_<si>**	target	Input	Slave select
	haddr_<si>[ADDR_WIDTH-1][a]		Input	Address
	htrans_<si>[1:0][a]		Input	Transfer type
	hwrite_<si>[a]		Input	Transfer direction indicator
	hsize_<si>[2:0][a]		Input	Size of the transfer
	hburst_<si>[2:0][a]		Input	Burst type
	hprot_<si>[6:0][a]		Input	Protection control
	hmaster_<si>[MASTER_WIDTH-1:0][a]		Input	Master identifier.
	hwdata_<si>[DATA_WIDTH-1:0][a]		Input	Write data
	hmastlock_<si>[a]		Input	Locked sequence indicator
	hready_<si>[a]	target	Input	Transfer completion indicator from interconnect
	hnonsec_<si>[a]		Input	Non-secure transfer indicator
	hexcl_<si>[a]		Input	Exclusive Transfer indicator
	hauser_<si>[USER_WIDTH-1:0][a]	USER_WIDTH >0	Input	Address channel user signals
	hwuser_<si>[USER_WIDTH-1:0][a]	USER_WIDTH >0	Input	Write channel user signals
	hrdata_<si>[DATA_WIDTH-1:0][a]		Output	Read data
	hreadyout_<si> or **hready_<si>**[a]	target or initiator	Output	Transfer completion indicator to interconnect or master
	hresp_<si>[a]		Output	Transfer response
	hexokay_<si>[a]		Output	Exclusive okay
	hruser_<si>[a]	USER_WIDTH >0	Output	Read channel user signals

Table 2-1 AHB5 bus matrix port list (continued)

Block	SIGNAL	CONDITION	DIRECTION	DESCRIPTION
AHB5 Master (slave initiator) [for each master interface defined]	**hrdata_<mi>[DATA_WIDTH-1:0]**		Input	Read data
	hreadyout_<mi>[b]		Input	HREADY feedback
	hresp_<mi>[b]		Input	Transfer response
	hexokay_<mi>[b]		Input	Exclusive okay
	hruser_<mi>[USER_WIDTH-1:0][b]	USER_WIDTH >0	Input	Read channel user signals
	hsel_<mi>[b]		Output	Slave select
	haddr_<mi>[ADDR_WIDTH-1][b]		Output	Address
	htrans_<mi>[1:0][b]		Output	Transfer type
	hwrite_<mi>[b]		Output	Transfer direction indicator
	hsize_<mi>[2:0][b]		Output	Size of the transfer
	hburst_<mi>[2:0][b]		Output	Burst type
	hprot_<mi>[6:0][b]		Output	Protection control
	hmaster_<mi>[MASTER_WIDTH-1:0][b]		Output	Master identifier.
	hwdata_<mi>[DATA_WIDTH-1:0][b]		Output	Write data
	hmastlock_<mi>[b]		Output	Locked sequence indicator
	hreadymux_<mi>[b]		Output	Transfer done
	hnonsec_<mi>[b]		Output	Non-secure transfer indicator
	hexcl_<mi>[b]		Output	Exclusive Transfer indicator
	hauser_<mi>[USER_WIDTH-1:0][b]	USER_WIDTH > 0	Output	Address channel user signals
	hwuser_<mi>[USER_WIDTH-1:0][b]	USER_WIDTH>0	Output	Write channel user signals
Remap	**remap[REMAP_WIDTH-1:0]**	REMAP_WIDTH >0	Input	Remap bus for memory map switching

a. si: slave interface port suffix.

b. mi: master interface port suffix.

2.1.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 bus matrix.

Table 2-2 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through. The bus matrix provides no built-in endian adaptation.
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through. The bus matrix provides no built-in endian adaptation.
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Pass-through

2.2 AHB5 default slave

This section describes the AHB5 default slave.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-9.

2.2.1 Functional description

The default slave conforms to the AHB5 specification which describes the default slave behavior. It returns a standard two-cycle ERROR response whenever the module is selected.

The AHB5 default slave responds to transfers when the bus master accesses an illegal address range:

- An OKAY response is generated for IDLE or BUSY transfers.
- An ERROR response is generated for NONSEQUENTIAL or SEQUENTIAL transfers.

Figure 2-2 shows the AHB5 default slave.

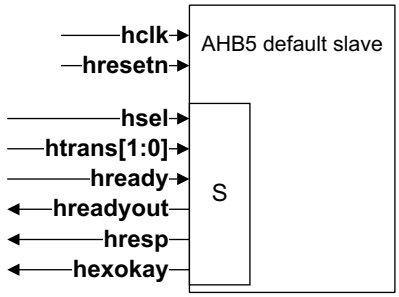


Figure 2-2 AHB5 default slave

2.2.2 Port list

The following table shows the port list of the AHB5 default slave.

Table 2-3 AHB5 default slave port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset

Table 2-3 AHB5 default slave port list (continued)

Block	Signal	Direction	Description
AHB5 Slave	**hsel**	Input	Slave select
	htrans[1:0]	Input	Transfer type
	hready	Input	Transfer completion indicator
	hreadyout	Output	Transfer completion indicator output
	hresp	Output	Transfer response
	hexokay	Output	Exclusive transfer response. This is tied to `0x0`.

2.2.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 default slave.

Table 2-4 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	FALSE	N/A
Secure_Transfers	FALSE	N/A
Endian	N/A	
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported
Multi_Copy_Atomicity	FALSE	N/A
User signaling	FALSE	Not supported

2.3 AHB5 example slave

This section describes the AHB5 example slave.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-11.

2.3.1 Functional description

The AHB5 example slave provides 3×16 bytes (3×4 words) of hardware read/write registers. It demonstrates how to implement a simple security aware AHB5 slave.

Figure 2-3 shows the AHB5 example slave.

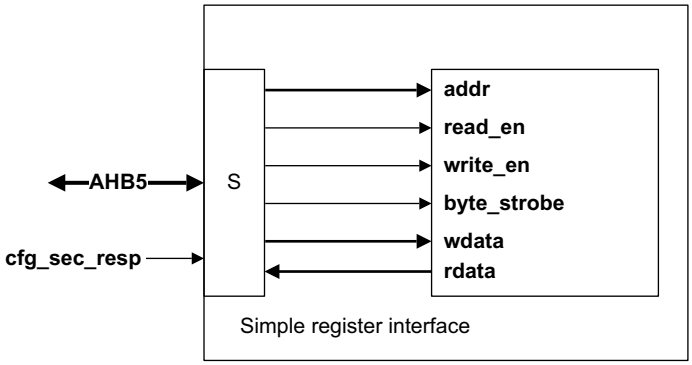


Figure 2-3 AHB5 example slave

The register sets are accessible by:

- One set (four words) with secure transfers only.
- One set (four words) with non-secure transfers only.
- One set (four words) with both secure and non-secure transfers.

The registers can be accessed by using byte, half word and word transfers.

The example slave is partitioned into two parts, the interface part converts the AHB5 protocol to a simple non-pipelined bus protocol and can be reused for porting simple peripherals from 8-bit/16-bit products to ARM easily. The security checking is done by register bank part.

2.3.2 Port list

The following table shows the port list of the AHB5 example slave.

Table 2-5 AHB5 example slave port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB5 side
	hresetn	Input	Reset for **HCLK** domain
AHB5 slave interface	**hsel**	Input	Slave select

Table 2-5 AHB5 example slave port list (continued)

Block	Signal	Direction	Description
	hnonsec	Input	Non-secure transfer indicator
	haddr[11:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	HREADY feedback from all slaves
	hwdata[31:0]	Output	Write data, configurable width
	hrdata[31:0]	Output	Read data, configurable width
	hreadyout	Output	Transfer completion indicator
	hresp[1:0]	Output	Transfer response
	cfg_sec_resp	Input	Error response (1) /RAZ/WI (0)

2.3.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 example slave.

Table 2-6 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	N/A
Secure_Transfers	TRUE	Supported
Endian	N/A	Default little endian
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not used

2.4 AHB5 exclusive access monitor

This section describes the AHB5 exclusive access monitor.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-13.
- *AHB5 bus properties* on page 2-15.

2.4.1 Functional description

You can add the AHB5 exclusive access monitor to an AHB5 path to monitor access to slaves downstream of it. The component implements the Exclusive Access Monitor feature described in the AHB5 specification.

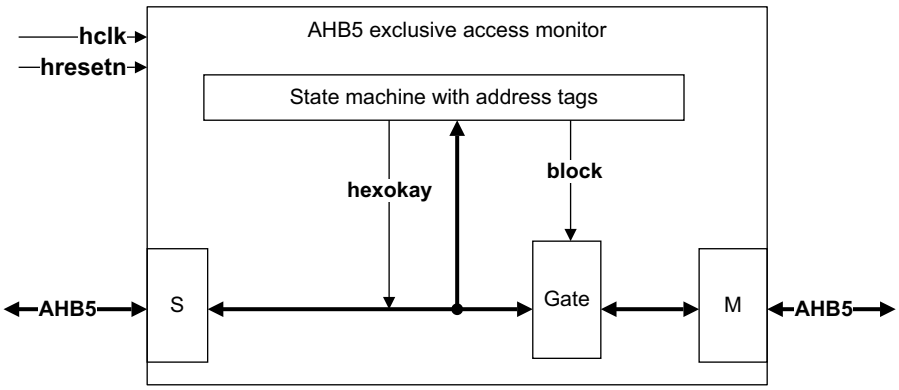


Figure 2-4 AHB5 exclusive access monitor

Due to TrustZone for ARMv8-M, this AHB5 exclusive access monitor has one difference from the AHB5 specification. HNONSEC is treated as an extra address bit in the address tag to prevent non-secure software from clearing a Secure tag.

Under TrustZone for ARMv8-M, the same data cannot be accessed in both secure and non-secure mode, therefore a write is not considered to have overwritten a tagged data if the HNONSEC is different from the state in the exclusive read.

If the exclusive access is set as not supported for a master, that is, the corresponding ID_PRESENT bit is not set, and an exclusive access arrives from that master, then the response is UNPREDICTABLE. In this implementation, the downstream HEXOKAY must either be tied low or implemented in downstream logic to provide the correct response.

If a master, for which exclusive access is set as not supported, performs a Store exclusive that conflicts with a tag, it is considered to have gone through and the tag cleared, even if another exclusive access capable slave downstream from the AHB5 exclusive access monitor would block it. The AHB5 exclusive access monitor does not check HEXOKAY from the downstream port in this case, as it would add complexity that is very unlikely to be used in practice.

The AHB5 exclusive access monitor blocks an exclusive write by setting the HTRANS signal to idle. It does not deselect the slave by setting HSEL low which means it does not interrupt a stream of transfers from the masters, that is, locked transfers, (HMASTLOCK).

The AHB5 exclusive access monitor treats non-exclusive writes from the same master to an address already tagged by the same master in the same way as writes from a different master, that is, it clears the tag and the matching exclusive write gets an exclusive access fail response.

An exclusive read with an error response will clear the exclusive tag.

2.4.2 Port list

The AHB5 exclusive access monitor has two AHB5 interfaces and associated clock and reset.

It will drive HEXOKAY upstream according to internal logic and will gate an exclusive failed write downstream.

It will still pass through the signals HEXCLS, HMASTER and have a HEXOKAY input on the downstream port. The input signals must be tied to 0, the outputs can be left open.

The following table shows the AHB5 exclusive access monitor interface signals.

Table 2-7 AHB5 exclusive access monitor port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock
	hresetn	Input	Reset

Table 2-7 AHB5 exclusive access monitor port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-7 AHB5 exclusive access monitor port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master (slave initiator)	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width

2.4.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 exclusive access monitor.

Table 2-8 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through. Note that the secure bit interacts with the AHB5 exclusive access monitor tagging.
Endian	N/A	Pass-through. The AHB5 exclusive access monitor provides no built-in endian adaptation, it functions as a simple bridge.

Table 2-8 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	This component is used to add exclusive access handling to a data path that doesn't natively handle it.
Multi_Copy_Atomicity	TRUE	Pass-through, no buffering.
User signaling	TRUE	Pass-through

2.5 AHB5 GPIO

This section describes the AHB5 GPIO.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-18.
- *AHB5 bus properties* on page 2-19.

2.5.1 Functional description

The AHB5 GPIO is a general-purpose I/O interface unit. This IP component introduces security awareness for GPIO accesses. It separates GPIOs which can be either accessed in secure or non-secure mode only.

Figure 2-5 shows the control circuit and external interface of the AHB5 GPIO.

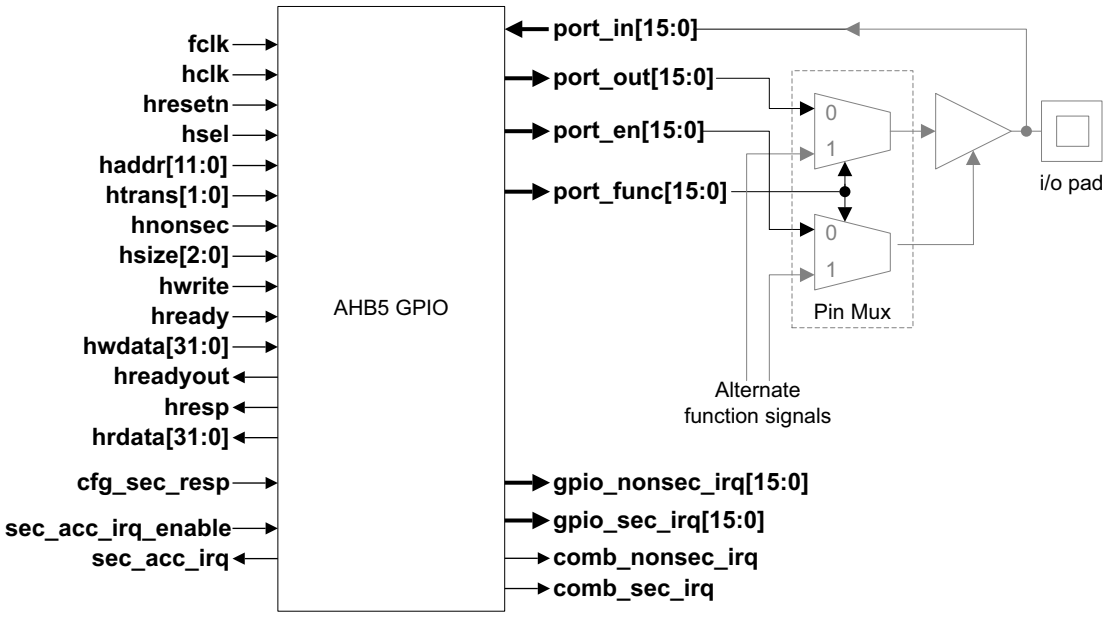


Figure 2-5 AHB5 GPIO control circuit and external interface

The AHB5 GPIO module receives transaction on the AHB5 interface which targets its register bank. The access is checked against the security configuration of the targeted register and then either accepted or responded with error or RAZ/WI depending on the value of the **cfg_sec_resp** input.

The Security error interrupt is set when enabled.

GPIO interrupts are only present on the appropriate GPIO_SEC_IRQ or GPIO_NONSEC_IRQ depending on the configuration parameter. The integrator needs to carefully connect the correct interrupt signals to secure or non-secure handlers in the same way as the configuration parameter is set. Interrupt pins with non-matching security attribute shall be set to 0 and shall never generate interrupt.

A combined interrupt can be used separately in secure and non-secure modes to summarize all relevant GPIO interrupts in one interrupt request.

The module can reach the GPIO ports in little endian, byte-invariant, and word-invariant big endian formats. The selected format can be configured using the endianness parameter.

The byte lane ordering is done according to the endianness parameter in both the read and write datapaths, as the endianness parameter is defined in *ARM® AMBA 5 AHB Protocol Specification.*

2.5.2 Port list

The following table shows the port list of the AHB5 GPIO.

Table 2-9 AHB5 GPIO port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB5 side
	fclk	Input	Clock AHB5 side free running. Same phase as **hclk** but cannot be gated off during sleep.
	hresetn	Input	Reset for **hclk** domain
AHB5 Slave Interface	**hsel**	Input	Slave select
	hnonsec	Input	Non-secure transfer indicator
	haddr[11:0]	Input	Address
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	HREADY feedback from all slaves
	hwdata[31:0]	Input	Write data
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response
GPIO	**port_in[15:0]**	Input	GPIO input port
	port_out[15:0]	Output	GPIO output port
	port_en[15:0]	Output	GPIO output enable port
	port_func[15:0]	Output	Alternate function selector for each port

Table 2-9 AHB5 GPIO port list (continued)

Block	Signal	Direction	Description
Interrupts	**gpio_sec_irq[15:0]**	Output	Interrupt signal for each secure GPIO
	gpio_nonsec_irq[15:0]	Output	Interrupt signal for each non-secure GPIO
	comb_sec_irq	Output	Combined secure interrupt signal
	comb_nonsec_irq	Output	Combined non-secure interrupt signal
	sec_acc_irq	Output	Security violation interrupt
	sec_acc_irq_enable	Input	Security violation interrupt enable. Enables security violation interrupt generation: 0: Security interrupt generation logic turned off 1: Security interrupt generation logic turned on
Configuration	**cfg_sec_resp**	Input	Response configuration in case of security violation: bus-error (1) or RAZ/WI (0).

2.5.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 GPIO.

Table 2-10 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	N/A
Secure_Transfers	TRUE	Supported
Endian	TRUE	Configurable during implementation
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not used

2.6 AHB5 master multiplexer

This section describes the AHB5 master multiplexer.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-21.
- *AHB5 bus properties* on page 2-22.

2.6.1 Functional description

The AHB5 master multiplexer has three slave ports to which three masters including interconnects can connect. It uses parameters to define the master port usage to avoid generating unnecessary additional logic.

Figure 2-6 shows the AHB5 master multiplexer.

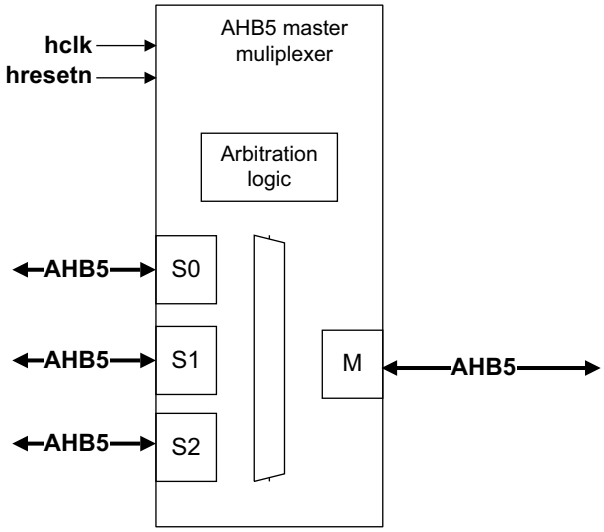


Figure 2-6 AHB5 master multiplexer

The AHB5 master multiplexer selects the transfers going to the master port based on the input requests from the downstream side and its arbitration logic.

When a valid transfer arrives an internal request is generated towards the arbiter.

Every slave port has an input stage which contains a set of flip-flops to hold the address phase of the transfer but can also be bypassed in case the current port is selected.

When holding is required, the **hreadyout_sx** for the corresponding interface is deasserted until the request is not selected by the arbitration logic.

The AHB5 master multiplexer uses a fixed arbitration scheme as follows:

Port 0 Same priority as port 1, round-robin scheme.

Port 1 Same priority as port 0, round-robin scheme.

Port 2 Higher priority master.

The **hmaster_m** output signal is driven by the selected port's **hmaster_s** input.

2.6.2 Port list

The following table shows the port list of the AHB5 master multiplexer.

Table 2-11 AHB5 master multiplexer port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
AHB5 Slave	**hsel_sx**[a]	Input	Slave select
	hnonsec_sx[a]	Input	Non-secure transfer indicator
	haddr_sx[ADDR_WIDTH-1:0][a]	Input	Address
	htrans_sx[1:0][a]	Input	Transfer type
	hsize_sx[2:0][a]	Input	Size of the transfer
	hwrite_sx[a]	Input	Transfer direction indicator
	hready_sx[a]	Input	Transfer completion indicator
	hprot_sx[6:0][a]	Input	Protection control
	hburst_sx[2:0][a]	Input	Burst type
	hmastlock_sx[a]	Input	Locked sequence indicator
	hwdata_sx[DATA_WIDTH-1:0][a]	Input	Write data, configurable width
	hexcl_sx[a]	Input	Exclusive Transfer indicator.
	hmaster_sx[MASTER_WIDTH-1:0][a]	Input	Master identifier.
	hrdata_sx[DATA_WIDTH-1:0][a]	Output	Read data, configurable width
	hreadyout_sx[a]	Output	Transfer completion indicator
	hresp_sx[a]	Output	Transfer response
	hexokay_sx[a]	Output	Exclusive okay

Table 2-11 AHB5 master multiplexer port list (continued)

Block	Signal	Direction	Description
AHB5 Master	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves.
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width

a. The **x** in **_sx** indicates the number of the master interface (from 0 to 2).

2.6.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 master multiplexer.

Table 2-12 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-12 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Pass-through

2.7 AHB5 slave multiplexer

This section describes the AHB5 slave multiplexer.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-27.

2.7.1 Functional description

The AHB5 slave multiplexer supports up to 16 AHB5 slaves. It uses parameters to define the slave port usage so that the synthesis process does not generate unnecessary additional logic. Figure 2-7 shows the AHB5 slave multiplexer.

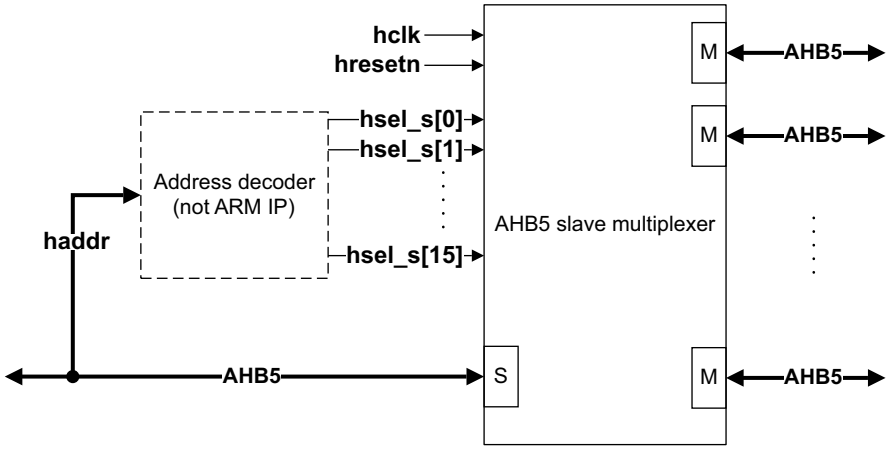


Figure 2-7 AHB5 slave multiplexer

If you require more AHB5 slave ports, you can either cascade two AHB5 slave multiplexers, or expand the design.

2.7.2 Port list

The following table shows the port list of the AHB5 slave multiplexer.

Table 2-13 AHB5 slave multiplexer port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
AHB5 Slave	**hsel_s[15:0]**	Input	Slave select for each port

Table 2-13 AHB5 slave multiplexer port list (continued)

Block	Signal	Direction	Description
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width
AHB5 Master	**hsel_mx**[a]	Output	Slave select pass-through

Table 2-13 AHB5 slave multiplexer port list (continued)

Block	Signal	Direction	Description
	hnonsec_mx[a]	Output	Non-secure transfer indicator
	haddr_mx[ADDR_WIDTH-1:0][a]	Output	Address, configurable width
	htrans_mx[1:0][a]	Output	Transfer type
	hsize_mx[2:0][a]	Output	Size of the transfer
	hwrite_mx[a]	Output	Transfer direction indicator
	hready_mx[a]	Output	HREADY feedback to all slaves.
	hprot_mx[6:0][a]	Output	Protection control
	hburst_mx[2:0][a]	Output	Burst type
	hmastlock_mx[a]	Output	Locked sequence indicator
	hwdata_mx[DATA_WIDTH-1:0][a]	Output	Write data, configurable width
	hexcl_mx[a]	Output	Exclusive Transfer indicator.
	hmaster_mx[MASTER_WIDTH-1:0][a]	Output	Master identifier
	hrdata_mx[DATA_WIDTH-1:0][a]	Input	Read data, configurable width
	hreadyout_mx[a]	Input	Transfer completion indicator
	hresp_mx[a]	Input	Transfer response
	hexokay_mx[a]	Input	Exclusive okay
	hruser_mx[USER_WIDTH-1:0][a]	Input	Read channel user signals, configurable width
	hauser_mx[USER_WIDTH-1:0][a]	Output	Address channel user signals, configurable width
	hwuser_mx[USER_WIDTH-1:0][a]	Output	Write channel user signals, configurable width

a. The **x** in **_mx** indicates the number of the interface (from 0 to 15).

2.7.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 slave multiplexer.

Table 2-14 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Pass-through

2.8 AHB5 timeout monitor

This section describes the AHB5 timeout monitor.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-29.
- *AHB5 bus properties* on page 2-30.

2.8.1 Functional description

The AHB5 timeout monitor prevents an AHB5 slave from locking up a system. It is placed between the AHB5 master or interconnect, and the slave, and is connected directly to the slave.

Figure 2-8 shows the control circuit and external interface of the AHB5 timeout monitor.

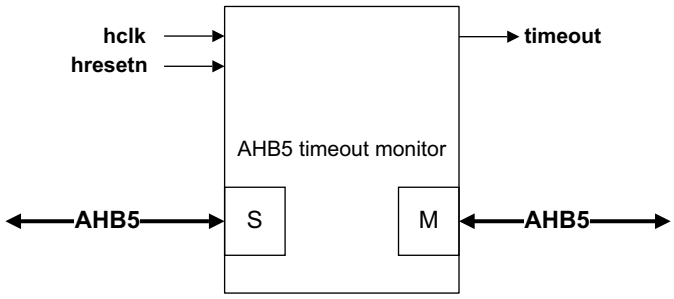


Figure 2-8 AHB5 timeout monitor

When there is an active transfer to the slave and the slave holds **HREADYOUT** low for more than a user-specified number of clock cycles, the monitor generates an error response to the bus master.

If the bus master generates any subsequent accesses to the slave, the AHB5 timeout monitor returns an error response and blocks access to the slave. The AHB5 timeout monitor stops generating error responses and preventing access to the slave when the slave completes the transfer that timed out, by asserting **hreadyout_m** high. If a burst is in progress the AHB5 timeout monitor blocks the remaining beats in the burst before becoming transparent.

If the AHB5 timeout monitor is connected directly to the processor, or connected to an AHB5 path that is used for exception handler code access, the processor cannot execute the bus fault exception handler.

Note

If you require monitoring of more than one bus slave, ARM recommends that you use one AHB5 timeout monitor for each bus slave instead of one monitor at the AHB5-slave multiplexer connection. Using multiple monitors prevents a single monitor from blocking access to the program ROM or SRAM.

You can use the **timeout** signal to export timeout events to external logic. During timeout, the **timeout** signal is asserted continuously until all conditions are met to return to the transparent state.

The configuration parameter STRICT_AHB_COMP controls the compliance level on the downstream side towards the timed out slave. If strict compliance is not required, STRICT_AHB_COMP = 0 significantly reduces the size of the AHB5 timeout monitor. See *ARM® CoreLink™ SIE-200 System IP for Embedded Configuration and Integration Manual* for more information.

2.8.2 Port list

The following table shows the port list of the AHB5 timeout monitor.

Table 2-15 AHB5 timeout monitor port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
AHB5 Slave Interface	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-15 AHB5 timeout monitor port list (continued)

Block	Signal	Direction	Description
AHB5 Master Interface	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive transfer indicator
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width
Other	**timeout**	Output	The connected slave has timed out and not yet recovered

2.8.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 timeout monitor.

Table 2-16 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-16 AHB5 properties (continued)

Property	Value	Comment
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Pass-through

2.9 AHB5 to external SRAM interface

This section describes the AHB5 to external SRAM interface.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-33.
- *AHB5 bus properties* on page 2-34.
- *Read and write timing* on page 2-34.

2.9.1 Functional description

The AHB5 to external SRAM interface module connects external SRAM, static memory devices or external peripherals to the AHB5 bus. The module supports only 8-bit or 16-bit interfaces.

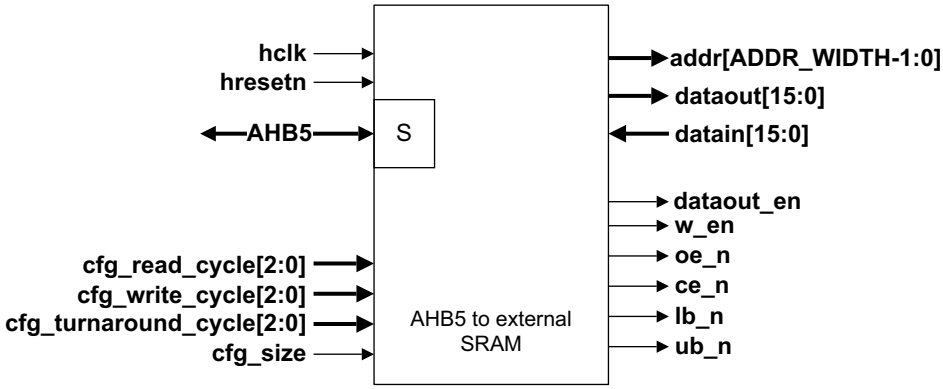


Figure 2-9 AHB5 to external SRAM interface module

The module is designed to support an external bidirectional data bus. The **dataout_en** signal controls the tristate buffer for data output. You must add your own tristate buffers in your system implementation. The design enables turnaround cycles to be inserted between reads and writes to prevent current spikes that could occur for a very short time when the processor system and the external device both drive the data bus.

The following signals control wait states for reads, wait states for writes, and the number of turnaround cycles respectively:

- **cfg_read_cycle**.
- **cfg_write_cycle**.
- **cfg_turnaround_cycle**.

You can operate the interface module in 8-bit mode, with **cfg_size** LOW, or 16-bit mode, with **cfg_size** HIGH. All the configuration control signals must remain stable during operation.

The module can store/read data to/from the memory both in little endian and byte- invariant and word invariant big endian formats. The used format can be configured using the ENDIANNESS parameter.

In both the read and write datapaths, the byte lane ordering is done according to the endianness paramater as it is defined in *ARM® AMBA 5 AHB Protocol Specification*.

Note

RTL-level byte re-ordering is only necessary for a 32-bit word-invariant big-endian data bus. In this mode, when a half-word is stored in 16-bit memory, the MSB goes to lower byte lane of the memory, that is, to bits[7:0] so the respective bytes of the AHB5 bus are swapped by the module.

2.9.2 Port list

The following table shows the port list of the AHB5 to external SRAM interface.

Table 2-17 AHB5 to external SRAM interface port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
Config signals	**cfg_read_cycle[2:0]**	Input	Number of clock cycles for a read operation. a value of 0 indicatges one read cycle.
	cfg_write_cycle[2:0]	Input	Number of clock cycles for a write operation.
	cfg_turnaround_cycle[2:0]	Input	Number of clock cycles required to switch between a read and a write operation on the tristate bus. A value of 0 indicates one turnaround cycle.
	cfg_size	Input	Memory interface data width: LOW (8) / HIGH (16).
AHB5 Slave	**haddr[ADDR_WIDTH-1:0]**	Input	Address, configurable width (ADDR_WIDTH).
	hsize[2:0]	Input	Size of the transfer
	htrans[1:0]	Input	Transfer type
	hwdata[31:0]	Input	Write data
	hwrite	Input	Transfer direction indicator
	hrdata[31:0]	Input	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response
	hsel	Input	Slave select
	hready	Input	Transfer completion indicator

Table 2-17 AHB5 to external SRAM interface port list (continued)

Block	Signal	Direction	Description
External Memory	**addr[ADDR_WIDTH-1:0]**	Output	Address
	dataout[15:0]	Output	Write data
	dataout_en	Output	Tristate buffer output enable for DATAOUT. Active LOW.
	datain[15:0]	Input	Read Data
	we_n	Output	Write strobe for external memory device. Active LOW.
	oe_n	Output	Read access output enable for external memory device. Active LOW.
	ce_n	Output	Chip enable. Active LOW.
	lb_n	Output	Lower byte enable. Active LOW
	ub_n	Output	Upper byte enable. Active LOW

2.9.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to external SRAM interface.

Table 2-18 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	Unused
Secure_Transfers	FALSE	Unused
Endian	TRUE	Configurable during implementation
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Unused
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents.
User signaling	FALSE	N/A

2.9.4 Read and write timing

The following diagram shows the AHB5 to external SRAM interread and write interface timing for the following signals:

- **cfg_read_cycle** (control wait states for reads) = 0.
- **cfg_write_cycle** (control wait states for writes) = 0.
- **cfg_turnaround_cycle** (number of turnaround cycles) = 0.

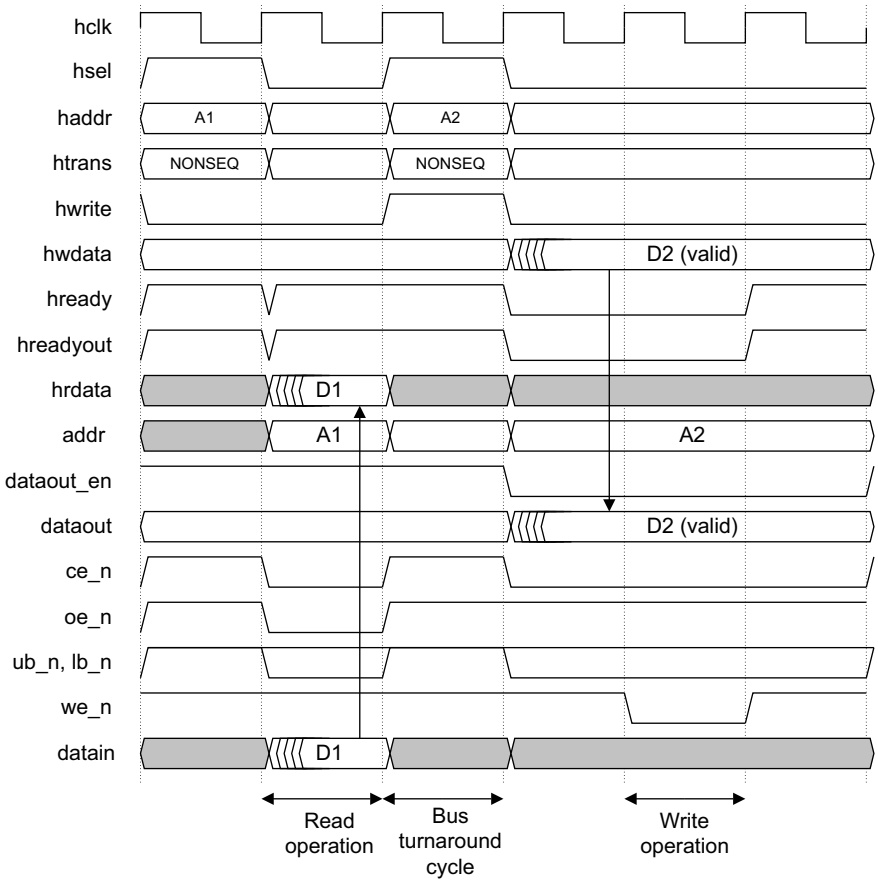


Figure 2-10 AHB5 to external SRAM interface read and write access timing

The following figure shows the AHB5 to external SRAM interface read and write access timing signals for the following case:

- **cfg_read_cycle** (control wait states for reads) = 1, that is, two cycles.
- **cfg_write_cycle** (control wait states for writes) = 1, that is, two cycles.
- **cfg_turnaround_cycle** (number of turnaround cycles) = 1, that is, two cycles.

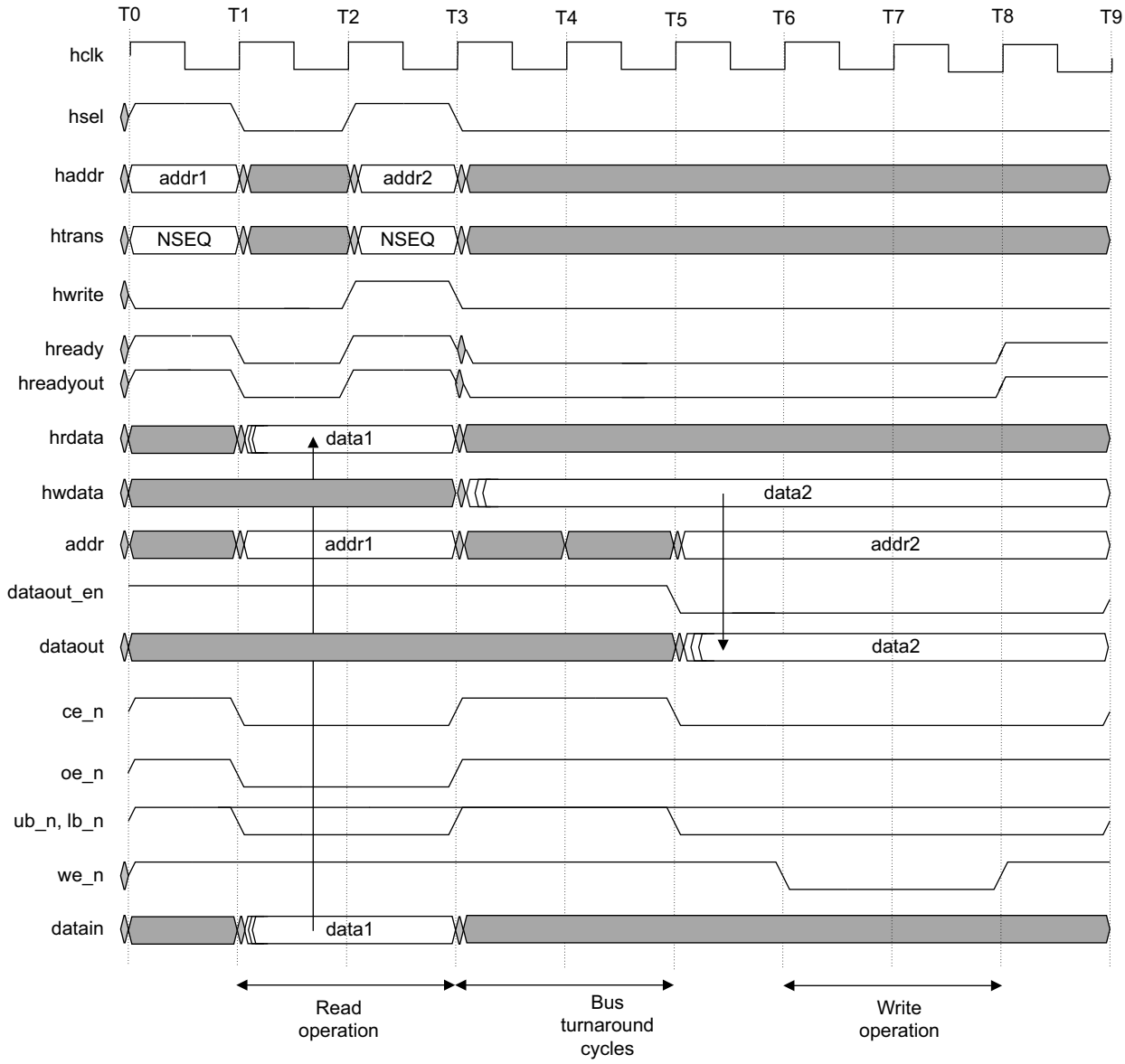


Figure 2-11 AHB5 to external SRAM interface read and write access timing

2.10 AHB5 to ROM interface

This section describes the AHB5 to ROM interface.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-38.
- *Read timing* on page 2-38.

2.10.1 Functional description

The AHB5 to ROM interface module is used to enable a simple ROM memory model to be attached to an AHB5 bus. It includes a configurable wait state generator.

Figure 2-12 shows the AHB5 to ROM interface.

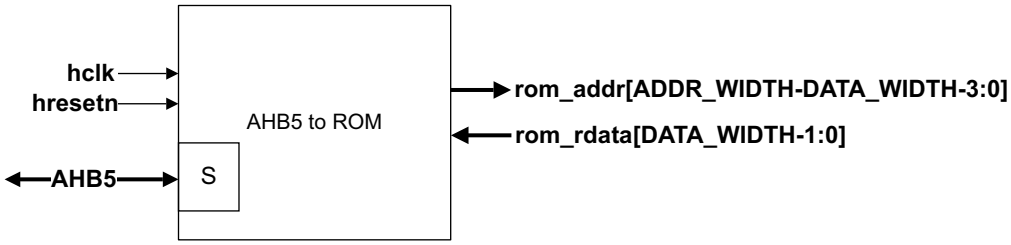


Figure 2-12 AHB5 to ROM interface module for 16 or 32-bit flash ROM

2.10.2 Port list

The following table shows the port list of the AHB5 to ROM interface.

Table 2-19 AHB5 to ROM interface port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset

Table 2-19 AHB5 to ROM interface port list (continued)

Block	Signal	Direction	Description
AHB5 Slave Interface	**haddr[ADDR_WIDTH-1:0]**	Input	Address, configurable width (ADDR_WIDTH)
	hsize	Input	Transfer size (unused)
	htrans[1:0]	Input	Transfer type
	hwdata[DATA_WIDTH-1:0]	Input	Write data (unused)
	hwrite	Input	Transfer direction indicator
	hrdata[DATA_WIDTH-1:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response
	hsel	Input	Slave select
	hready	Input	Transfer completion indicator
ROM	**rom_addr[AW-DW/16-1:0]**[a]	Output	Address, configurable width (ADDR_WIDTH)
	rom_rdata[DATA_WIDTH]	Input	Read Data

a. AW-DW = ADDR_WIDTH-DATA_WIDTH

2.10.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to ROM interface.

Table 2-20 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	Unused
Secure_Transfers	FALSE	Unused
Endian	N/A	Configuration is not required, this interface is compatible with all endianness. Only read operations are supported and they are always executed full datawidth wide.
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Unused
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	N/A

2.10.4 Read timing

The AHB5 to ROM interface only supports read operations.

Figure 2-13 and Figure 2-14 show the ROM memory read access timing with different wait states.

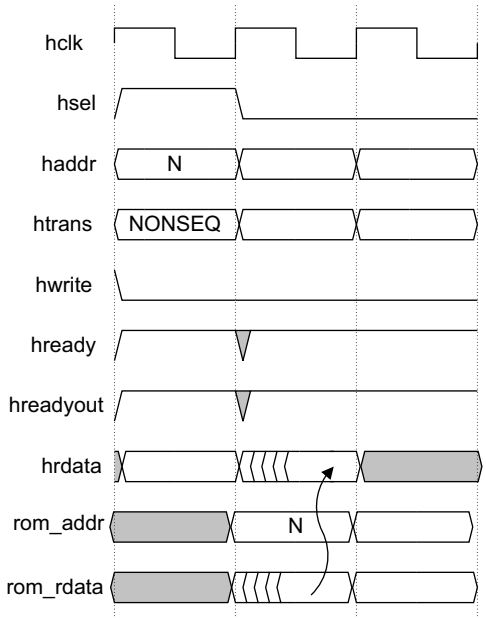


Figure 2-13 AHB5 to ROM read access timing with WS = 0

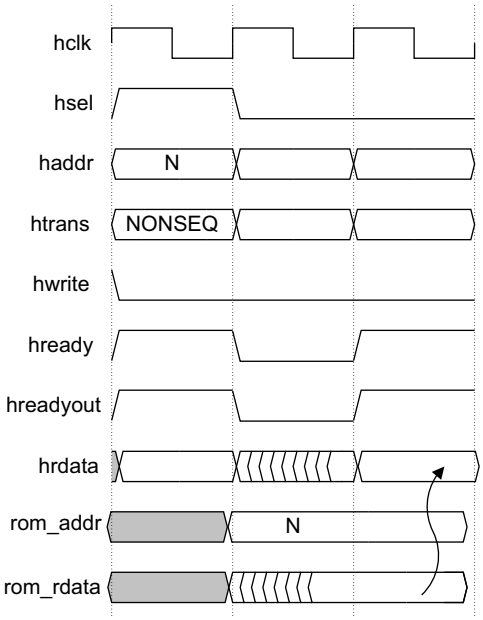


Figure 2-14 AHB5 to ROM read access timing with WS = 1

2.11 AHB5 to internal SRAM interface module

This section describes the AHB5 to internal SRAM interface module.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-41.
- *Read and write timing* on page 2-41.

2.11.1 Functional description

The AHB5 to internal SRAM interface module enables on-chip synchronous RAM blocks to attach to an AHB5 interface. It performs read and write operations with zero wait states. The design supports 32-bit SRAM with byte writes.

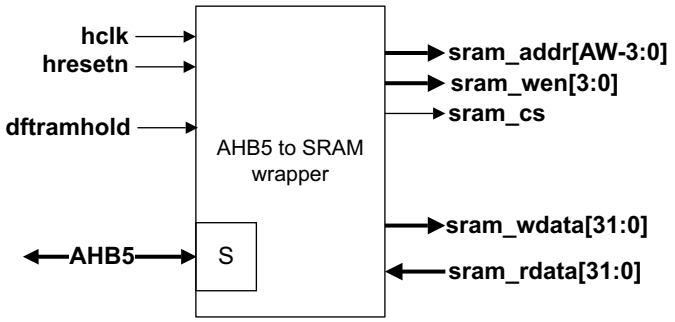


Figure 2-15 AHB5 to internal SRAM interface module

If a read operation follows immediately after a write operation, the write address and write data are stored in an internal buffer. The stalled write transfer is carried out when the AHB5 interface is idle, or when a new write transfer arrives. This process occurs transparently and does not result in any wait states.

The module can store/read data to/from the memory both in little endian and byte- invariant and word invariant big endian formats. The used format can be configured using the endianness parameter.

2.11.2 Port list

The following table shows the port list of the AHB5 to internal SRAM interface.

Table 2-21 AHB5 to internal SRAM interface port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
AHB5 Slave Initiator	**haddr[ADDR_WIDTH-1:0]**	Input	Address, configurable width (ADDR_WIDTH)
	hsize[2:0]	Input	Size of the transfer
	htrans[1:0]	Input	Transfer type

Table 2-21 AHB5 to internal SRAM interface port list (continued)

Block	Signal	Direction	Description
	hwdata[31:0]	Input	Write data
	hwrite	Input	Transfer direction indicator
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response
	hsel	Input	Slave select
	hready	Input	Transfer completion indicator
External Memory	**sram_addr[ADDR_WIDTH-1:0]**	Output	Address, configurable width (ADDR_WIDTH)
	sram_wdata[31:0]	Output	Write data
	sram_rdata[31:0]	Input	Read Data
	sram_wen[3:0]	Output	Write Enable
	sram_cs	Output	Chip Select
DFT	**dftramhold**	Input	DFT bypass for RAM CS

2.11.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to internal SRAM interface.

Table 2-22 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	FALSE	Unused
Secure_Transfers	FALSE	Unused
Endian	TRUE	Configurable during implementation
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Unused
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents.
User signaling	FALSE	N/A

2.11.4 Read and write timing

The following diagrams show the read and write access timing of the AHB5 to internal SRAM interface.

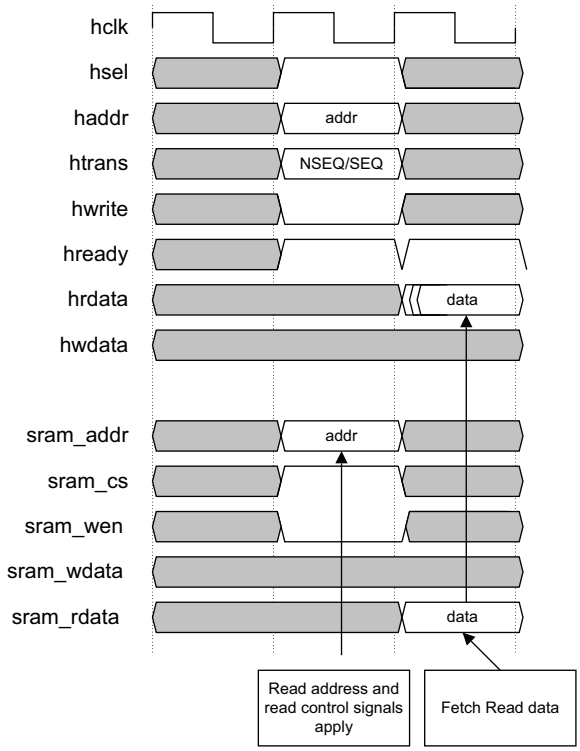


Figure 2-16 AHB5 to internal SRAM read access timing

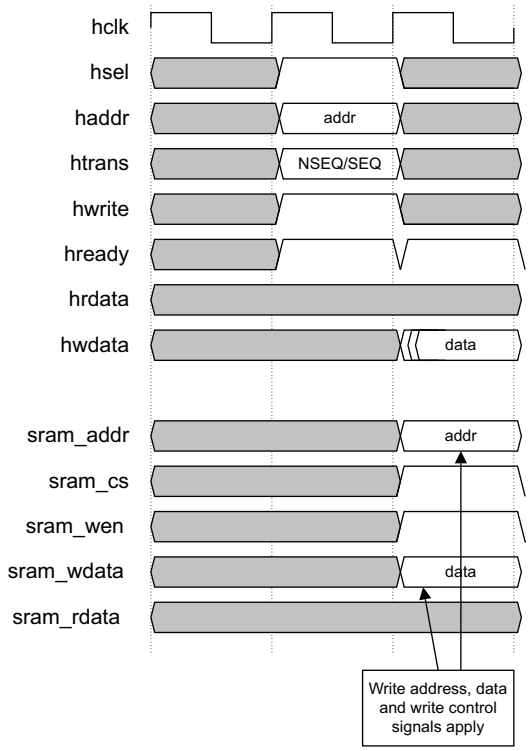


Figure 2-17 AHB5 to internal SRAM write access timing

2.12 Cortex-M3/Cortex-M4 AHB5 adapter

This section describes the Cortex-M3/Cortex-M4 AHB5 adapter.

The following subsections describe the AHB5 adapter:

- *Functional description*.
- *Port list* on page 2-45.
- *AHB5 bus properties* on page 2-48.

2.12.1 Functional description

The Cortex-M3/Cortex-M4 AHB5 adapter module realizes the following functions:

- Converts the Cortex-M3/Cortex-M4 exclusive access signaling to AHB5 exclusive access signals.
- Instantiates a Master Security Controller if enabled by configuration parameter.
- Maps the AHB-Lite HPROT + MEMATTR signaling of Cortex-M3/Cortex-M4 to the extended AHB5 HPROT.

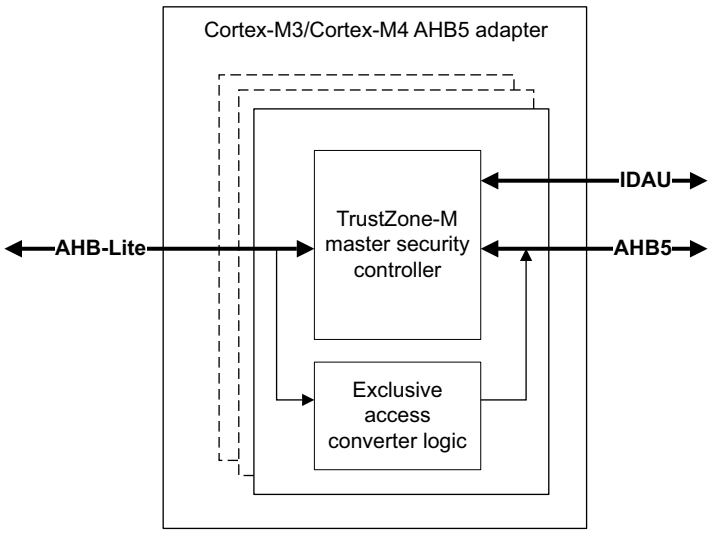


Figure 2-18 Cortex-M3/Cortex-M4 AHB5 adapter

The Cortex-M3 has three AHB-Lite ports, the Cortex-M decode logic and master security controller (MSC) logic are generated two or three times in the AHB5 adapter, depending upon the setting of the parameter CODE_MUXED. If CODE_MUXED is enabled:

- The code bus mux must be placed between the core and the Cortex-M3/Cortex-M4 AHB5 adapter module.
- The muxed code bus must be connected to the DCode interface of the Cortex-M3/Cortex-M4 AHB5 adapter module.

The additional HPROT bits of AHB5 are mapped as:

- **hprot[4]** = **hprot[3]**
- **hprot[5]** = **mematttr[0]**

- **hprot[6] = memattr[1]**

2.12.2 Port list

The following table shows the port list of the Cortex-M3/Cortex-M4 AHB5 adapter.

Table 2-23 Cortex-M3/Cortex-M4 AHB5 adapter port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB side
	hresetn	Input	Reset for **hclk** domain
AMBA 3 AHB-Lite Slave Interface (System/DCode/ICode)	**haddrx_s[31:0]**	Input	Address, configurable width
	htransx_s[1:0]	Input	Transfer type
	hsizex_s[2:0]	Input	Size of the transfer
	hwritex_s	Input	Transfer direction indicator
	hreadyx_s	Input	HREADY feedback from all slaves
	hprotx_s[3:0]	Input	Protection control
	hburstx_s[2:0]	Input	Burst type
	hmastlocks_s	Input	Locked sequence indicator **Note** Present only on the System interface, not on the DCode or ICode interfaces.
	hwdatax_s[31:0]	Input	Write data, configurable width
	hrdatax_s[31:0]	Output	Read data, configurable width
	hrespx_s[1:0]	Output	Transfer response
	hmasterx_s[1:0]	Input	Master identifier **Note** Present only on the System interface and DCode interfaces, not on the ICode interface.

Table 2-23 Cortex-M3/Cortex-M4 AHB5 adapter port list (continued)

Block	Signal	Direction	Description
M3 Additional AHB-Lite Signals (System/DCode/ICode)	**exreqx_s**	Input	Exclusive access request **Note** Present only on the System interface and DCode interfaces, not on the ICode interface.
	exrespx_s	Output	Exclusive access response **Note** Present only on the System interface and DCode interfaces, not on the ICode interface.
	memattrx_s[1:0]	Input	Additional memory attributes

Table 2-23 Cortex-M3/Cortex-M4 AHB5 adapter port list (continued)

Block	Signal	Direction	Description
AHB5 Master Interface (System/DCode/ICode)	**haddrx_m[31:0]**	Output	Address, configurable width
	htransx_m[3:0]	Output	Transfer type
	hsizex_m[2:0]	Output	Size of the transfer
	hwritex_m	Output	Transfer direction indicator
	hreadyx_m	Output	hready_s feedback to slave from all slaves (HREADY)
	hprotx_m[6:0]	Output	Protection control
	hburstx_m[2:0]	Output	Burst type
	hmastlockx_m	Output	Locked sequence indicator **Note** Present only on the System interface, not on the DCode or ICode interfaces.
	hwdatax_m[31:0]	Output	Write data, configurable width
	hexclx_m	Output	Exclusive transfer **Note** Present only on the System and DCode interfaces, not on the ICode interface.
	hmasterx_m[1:0]	Output	Master identifier, configurable width **Note** Present only on the System and DCode interfaces, not on the ICode interface.
	hrdatax_m[31:0]	Input	Read data, configurable width
	hrespx_m[1:0]	Input	Transfer response
	hexokayx_m	Input	Exclusive okay (AHB5 only) **Note** Present only on the System and DCode interfaces, not on the ICode interface.

Table 2-23 Cortex-M3/Cortex-M4 AHB5 adapter port list (continued)

Block	Signal	Direction	Description
IDAU-Lite Interface	**idauaddr[26:0]**	Output	Address to check by IDAU
	idauns	Input	Non-secure or secure
	idauunchk	Input	Unchecked – accessible both secure and non-secure

2.12.3 AHB5 bus properties

The following table shows the AHB5 properties of the Cortex-M3/Cortex-M4 AHB5 adapter.

Table 2-24 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Maps the AHB-Lite HPROT + MEMATTR signaling of M3/M4 to the extended AHB5 HPROT
Secure_Transfers	Configurable	Instantiates a Master Security Controller if enabled by configuration parameter
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Convert the M3/M4 exclusive access signaling to AHB5 exclusive access signals
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not applicable

2.13 Comparison between bridges and their low-latency versions

The following table compares the intended uses of the AHB5 to AHB5 sync-down bridge, the AHB5 to AHB5 sync-up bridge and the AHB to APB4 sync-down bridge, and their low-latency equivalents.

Table 2-25

Bridge	Power managent	Description	Uses
AHB5 to AHB5 sync-down bridge	Q-channel	Bridge that synchronizes crossing between fast AHB5 domain and slow AHB5 domain. Supports power domain crossing using Q-channels.	Boundary between fast AHB5 power domain and slow AHB5 power domain.
AHB5 to AHB5 low-latency sync-down bridge	N/A	Bridge that synchronizes crossing between fast AHB5 domain and slow AHB5 domain. Latency optimized with no support for Q-channels or power domain crossing.	Boundary between fast AHB5 power domain and slow AHB5 power domain. Designs that do not use Q-channel for power management. Latency critical paths inside one power domain.
AHB5 to AHB5 sync-up bridge	Q-channel	Bridge that synchronizes crossing between slow AHB5 power domain and fast AHB5 power domain. Supports power domain crossing using Q-channels.	Boundary between slow AHB5 domain and fast AHB5 domain.
AHB5 to AHB5 low-latency sync-up bridge	N/A	Bridge that synchronizes crossing between slow AHB5 domain and fast AHB5 domain. Latency optimized with no support for Q-channels or power domain crossing.	Boundary between slow AHB5 domain and fast AHB5 domain. Designs that do not use Q-channel for power management. Latency critical paths inside one power domain.
AHB5 to APB4 sync-down bridge	Q-channel	Bridge between AHB5 domain and APB4 domain. Uses handshaking between fast clock and slow clock to enable clean power domain crossing.	Connection between APB4 peripheral device and AHB5 bus.
AHB5 to APB4 low-latency sync-down bridge	N/A	Bridge between AHB5 domain and APB4 domain. Latency optimized by using clock enable signal.	Connection between APB4 peripheral device and AHB5 bus. Designs that do not use Q-channel for power management. Latency critical paths inside one power domain.

2.14 AHB5 access control gate

This section describes the AHB5 access control gate

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-51.
- *AHB5 bus properties* on page 2-54.

2.14.1 Functional description

The AHB5 *Access Control Gate* (ACG) IP component can be placed on a clock or power domain boundary to pass or block AHB5 transfers whenever the receiving side of the transaction cannot accept the transfer, or is explicitly asked not to do so. The transfer is latched internally and the module generates automatic responses when necessary.

The ACG serves as the boundary element of the clock or power domains:

- When both domains are on, the ACG is invisible on the bus and AHB5 transfers pass through it without any delay.
- When either the clock or the power domain is down, as indicated by the Q-channel states, the ACG generates a waited transfer response, so that an incoming transfer is delayed.

  It informs the power and clock controllers that power and clock are required, so a wake-up sequence must be initiated. The ACG also denies quiescence requests from any Q-channels when there are ongoing transfers through the ACG.

  Optionally, the ACG can respond with a standard AHB5 Error response when the transfers cannot pass through it due to quiescent Q-channel states. The wake up request is not made to the dormant Q-channel when using this mode of operation.

Table 2-26 shows the behavior of the ACG.

Table 2-26 Behavior of the ACG

EXT GATE ACK	CFG GATE RESP	Any clock or power Q-channel in Q_STOP	Expected ACG/bridge behavior
0	X	0	Transfers pass through. Deny Q-channel requests during transfers. Accept Q-channel requests when there is no incoming transfer.
X	0	1	Hold transfers and show **hreadyout_s** = 0. Wake up Q-channels when transfer arrives.
X	1	1	Generate Error response for incoming transfers. Do not wake up Q-channels.
1	0	0	Hold transfers and show **hreadyout_s** = 0. Deny Q-channel requests during transfers. Accept Q-channel requests when there is no incoming transfer.
1	1	0	Generate Error response for incoming transfers. Accept Q-channel requests even during sending error responses.

Figure 2-19 on page 2-51 shows the AHB5 access control gate:

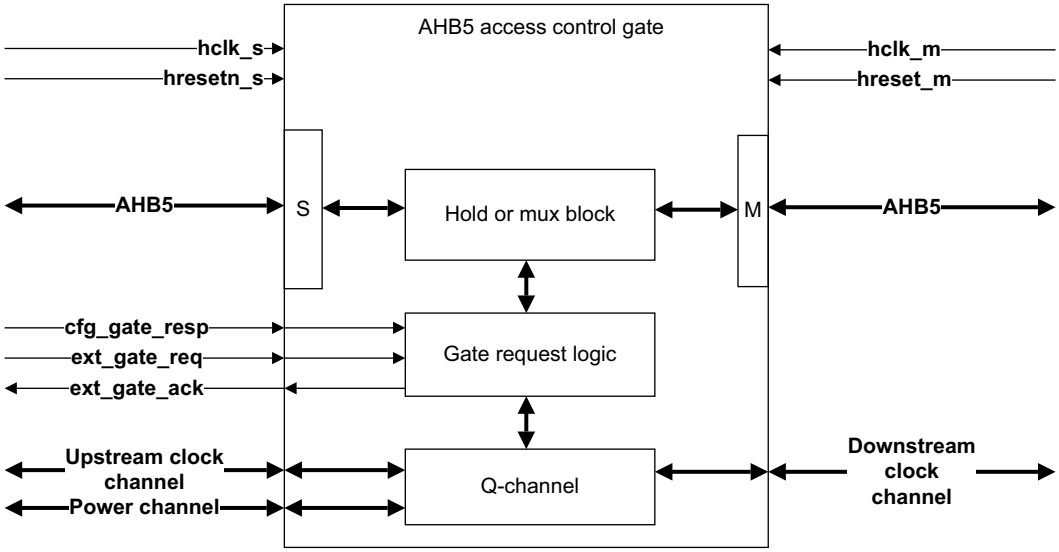


Figure 2-19 AHB5 access control gate

2.14.2 Port list

The AHB5 access control gate provides:

- One upstream AHB5 interface and one downstream AHB5 interface.
- Three Q-channel interfaces.
- Sideband signals for configuration and the external blocking feature.

The following table shows the port list of the AHB5 access control gate.

Table 2-27 AHB5 access control gate port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk_s**	Input	Clock for the downstream side
	hresetn_s	Input	Reset for the downstream side
	hclk_m	Input	Clock for the upstream side (same phase and frequency as **hclk_s**)
	hresetn_m	Input	Reset for the upstream side

Table 2-27 AHB5 access control gate port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-27 AHB5 access control gate port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves.
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Q-channel Upstream side	**hclk_qactive_s**	Output	Clock active indication to clock controller
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller

Table 2-27 AHB5 access control gate port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Q-channel Downstream side	**hclk_qactive_m**	Output	Clock active indication to clock controller
	hclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_m	Output	Clock Q Deny to clock controller
Power Q-channel (on downstream side)	**pwr_qactive_s**	Output	Power active indication to power controller
	pwr_qreqn_s	Input	Power Q Request from power controller (active low)
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low)
	pwr_qdeny_s	Output	Power Q Deny to power controller
Miscellaneous	**ext_gate_req**	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge
	cfg_gate_resp	Input	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response

See *ARM® CoreLink™ SIE-200 System IP for Embedded Configuration and Integration Manual* for more information on the use of **ext_gate_req**, **ext_gate_ack**, and **cfg_gate_resp**.

2.14.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 access control gate.

Table 2-28 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.15 AHB5 downsizer

This section describes the AHB5 downsizer.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-57.

2.15.1 Functional description

The AHB5 downsizer module enables a wider AHB5 bus master to connect to a narrower AHB5 slave. The downsizer module reduces the width of the data buses by half between an AHB master and an AHB slave.

Figure 2-20 shows the AHB downsizer module.

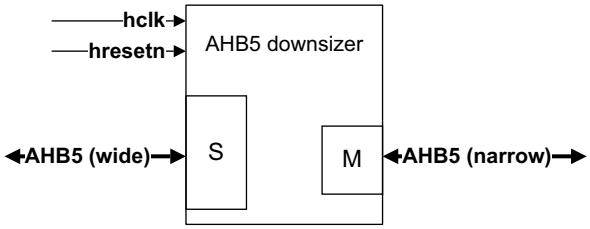


Figure 2-20 AHB5 downsizer

2.15.2 Port list

The following table shows the port list of the AHB5 downsizer.

Table 2-29 AHB5 downsizer port list

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock
	hresetn	Input	Reset for hclk domain

Table 2-29 AHB5 downsizer port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave Interface	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	HREADY feedback from all slaves
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier, configurable width
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s[1:0]	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-29 AHB5 downsizer port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master Interface	**hsel_m**	Output	Slave select
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH/2-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive transfer
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier, configurable width
	hrdata_m[DATA_WIDTH/2-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator from slave
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay (AHB5 only)
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width

2.15.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 downsizer.

Table 2-30 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	Configurable	-
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-30 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.16 AHB5 to AHB5 and APB4 asynchronous bridge

This section describes the AHB5 to AHB5 and APB4 asynchronous bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-60.
- *AHB5 bus properties* on page 2-64.

2.16.1 Functional description

The AHB5 to AHB5 and APB4 asynchronous bridge is capable of forwarding AHB5 transactions between two asynchronous clock domains. An AHB or APB transfer is generated on the downstream side, depending on the two **hsel** inputs, decoded externally. Bursts are always converted to single transfers downstream, including on the AHB5-AHB5 path.

Note

Because the bridge changes the value of **hburst**, it can affect the exclusive access sequences. This must be considered when positioning the AHB5 exclusive access monitor, if used, in the system.

Because of the Q-channel handling, the bridge can also be placed on power and clock domain boundaries.

The bridge consists of the following major components:

- An AHB slave on the upstream side.
- An AHB master on the downstream side:
  - Logic to stall the upstream transfer while a downstream transfer takes place.
  - Q-channel logic to respond to quiescence requests.

Figure 2-21 shows the AHB5 to AHB5 and APB4 asynchronous bridge module.

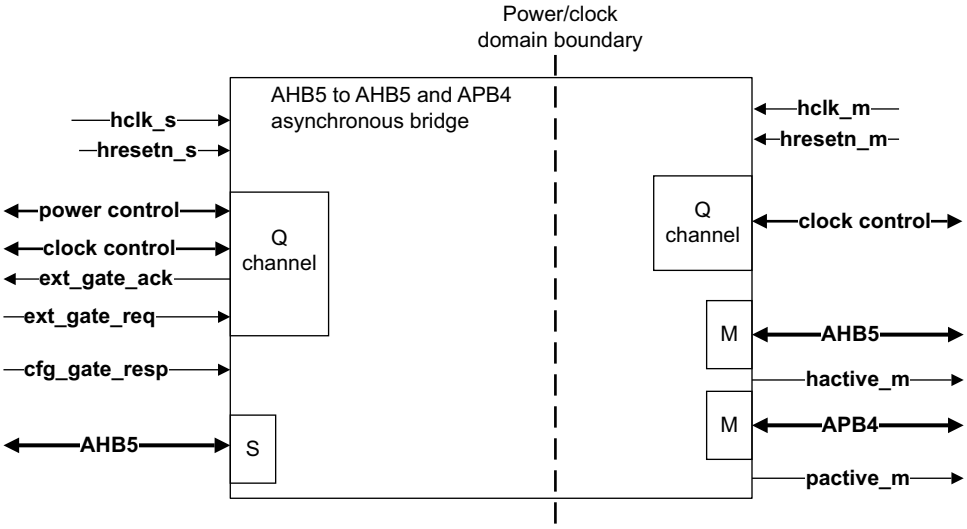


Figure 2-21 AHB5 to AHB5 and APB4 asynchronous bridge

The upstream (slave) side receives the incoming AHB5 transfers and latches drives **hready_s** signal low while the downstream transfer takes place. When the downstream transfer is complete, **hready_s** is driven high to the upstream side.

When master lock sequences are detected, the downstream side inserts IDLE transfers between two locked sequences as recommended by the AHB5 specification.

If the slave reset is deasserted before the master reset, any incoming transfers are waited until the upstream side is ready to process them.

Response configuration changes are ignored during a burst or in a locked transfer sequence. When the bridge is powered down, if **cfg_gate_resp** is asserted, the bridge responds with an AHB error response. If it is not asserted, the transfer is waited until the bridge is powered up again.

There are 3 Q-Channels on the bridge. The bridge only waits transfers or returns an error response when the Power or the downstream clock Q-Channel is in off state.

When not performing transfers, **hmastlock_s** must not be kept asserted because this can have a prolonged effect on the downstream side because of the asynchronous nature of the bridge.

2.16.2 Port list

The AHB5 to AHB5 and APB4 asynchronous bridge provides:

- One upstream interface and one downstream interface.
- A downstream APB interface.
- Three Q-channel interfaces.

The following table shows the port list of the AHB5 to AHB5 and APB4 asynchronous bridge.

Table 2-31 AHB5 to AHB5 and APB4 asynchronous bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk_s**	Input	Clock for the downstream side
	hresetn_s	Input	Reset for the downstream side
	hclk_m	Input	Clock for the upstream side
	hresetn_m	Input	Reset for the upstream side

Table 2-31 AHB5 to AHB5 and APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_ahb_s**	Input	Slave select for AHB5 interface
	hsel_apb_s	Input	Slave select for APB interface
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-31 AHB5 to AHB5 and APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width

Table 2-31 AHB5 to AHB5 and APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
APB4 Master	**paddr_m[ADDR_WIDTH-1:0]**	Output	Address
	pprot_m[2:0]	Output	Protection control
	psel_m	Output	Slave select
	penable_m	Output	Enable
	pwrite_m	Output	Transfer direction indicator
	pwdata_m[31:0]	Output	Write data
	pstrb_m[3:0]	Output	Write strobe
	pready_m	Input	Ready
	prdata_m[31:0]	Input	Read data
	pslverr_m	Input	Transfer failure
	pmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier, configurable width (MASTER_WIDTH)
Q-channel Upstream side	**hclk_qactive_s**	Output	Clock active indication to clock controller.
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller
Q-channel Downstream side	**hclk_qactive_m**	Output	Clock active indication to clock controller.
	hclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_m	Output	Clock Q Deny to clock controller
Power Q-channel (on downstream side)	**pwr_qactive_s**	Output	Power active indication to power controller.
	pwr_qreqn_s	Input	Power Q Request from power controller (active low).
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low).
	pwr_qdeny_s	Output	Power Q Deny to power controller.

Table 2-31 AHB5 to AHB5 and APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Miscellaneous	**hactive_m**	Output	AHB5 interface active
	pactive_m	Output	APB4 interface active
	ext_gate_req	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge
	cfg_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.16.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 and APB4 asynchronous bridge.

Table 2-32 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.17 AHB5 to AHB5 sync-down bridge

This section describes the AHB5 to AHB5 sync-down bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-66.
- *AHB5 bus properties* on page 2-69.

2.17.1 Functional description

The AHB5 to AHB5 sync-down bridge synchronizes AHB5 interfaces where the upstream side is faster than the downstream side and the clocks are synchronous, in phase and have an N:1 frequency ratio. It also supports Q-channel ports in order to enable placement of the bridge on a clock or power domain boundary.

A parameter defines whether burst transfers are converted into single transfers on the downstream side, or BUSY sequences are inserted while waiting for the new upstream data to arrive. Otherwise the bridge inserts IDLE transfers to the attached slave. If burst is supported and the bridge receives an error response on the downstream side during the sequential beats of the burst, it cancels the remaining transfers in the burst. The upstream side rejects the remainder of the burst by providing error responses while the downstream side is kept in IDLE state.

Note

An error response on the upstream side only appears as an error interrupt if the respective (bufferable, non-exclusive) write transfer is buffered.

A single write can be buffered in the 1-deep write buffer of the upstream side. When a non-exclusive write transfer is marked as bufferable, and there is a transfer already pending in the latch, the write buffer can store the incoming write and respond back to the slave with a ready response. Due to the nature of buffering, it is possible that an error response only occurs after the data phase of the write transfer, in which case an active high level interrupt is generated on the fast clock as an error signal towards the initiator of the transfer.

When master lock sequences are detected, the downstream side automatically inserts IDLE transfers between two locked sequences as recommended by the AHB5 specification.

The module denies Q-channel requests when there is a pending transfer or a pending error interrupt from the write buffer. Note that the same power-down procedure has to be followed regardless of the write buffer. The system has to guarantee that powerdown is not initiated before the last transfer is properly acknowledged by **hreadyout_s**. This condition guarantees that the bridge completes the transfer before the power is removed.

The bridge has two clock inputs:

- **hclk_m** on the downstream side.
- **hclk_s** on the upstream side.

The two clocks are semi-synchronous, that is, **hclk_s** is an integer multiple of **hclk_m**.

Figure 2-22 on page 2-66 shows the AHB5 to AHB5 sync-down bridge.

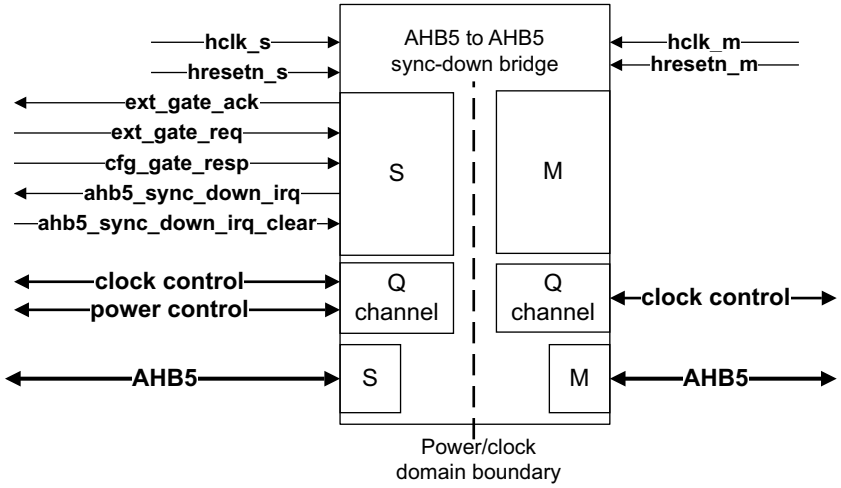


Figure 2-22 AHB5 to AHB5 sync-down bridge

If a buffered write error occurs, it generates an **ahb5_sync_down_irq** active high level interrupt in the fast **hclk** domain.

2.17.2 Port list

The following table shows the port list of the AHB5 to AHB5 sync-down bridge.

Table 2-33 AHB5 to AHB5 sync-down bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk_s**	Input	Clock for the upstream side. Synchronous with **hclk_m**, frequency is N times **hclk_m**.
	hresetn_s	Input	Reset for the upstream side
	hclk_m	Input	Clock for the downstream side
	hresetn_m	Input	Reset for the downstream side

Table 2-33 AHB5 to AHB5 sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-33 AHB5 to AHB5 sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hnonsec_m**	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Q-channel Upstream side	**hclk_qactive_s**	Output	Clock active indication to clock controller.
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller
Q-channel Downstream side	**hclk_qactive_m**	Output	Clock active indication to clock controller.
	hclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_m	Output	Clock Q Deny to clock controller

Table 2-33 AHB5 to AHB5 sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Power Q-channel (on downstream side)	**pwr_qactive_s**	Output	Power active indication to power controller
	pwr_qreqn_s	Input	Power Q Request from power controller (active low)
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low)
	pwr_qdeny_s	Output	Power Q Deny to power controller
Miscellaneous	**ahb5_sync_down_irq**	Output	Bufferable write error interrupt (active high level)
	ahb5_sync_down_irq_clear	Input	Bufferable write error interrupt clear
	ext_gate_req	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge
	cfg_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.17.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 sync-down bridge.

Table 2-34 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	TRUE	Configurable width

2.18 AHB5 to AHB5 low-latency sync-down bridge

This section describes the AHB5 to AHB5 low-latency sync-down bridge. This bridge is similar in function to the AHB5 to AHB5 sync-down bridge but it is further optimized to reduce latency for designs that do not use Q-channels for power management.

The setion contains the following subsections:

- *Functional description*.
- *Port list* on page 2-71.
- *AHB5 bus properties* on page 2-73.

2.18.1 Functional description

The AHB5 to AHB5 low-latency sync-down bridge synchronizes AHB5 interfaces where the upstream side is faster than the downstream side and the clocks are synchronous, in phase, and have an N:1 frequency ratio.

A parameter defines whether burst transfers are converted into single transfers on the downstream side, or BUSY sequences are inserted while waiting for the new upstream data to arrive. Otherwise the bridge inserts IDLE transfers to the attached slave. If burst is supported and the bridge receives an error response on the downstream side during the sequential beats of the burst, it cancels the remaining transfers in the burst. The upstream side rejects the remainder of the burst by providing error responses while the downstream side is kept in IDLE state.

Note

An error response on the upstream side only appears as an error interrupt if the respective (bufferable, non-exclusive) write transfer is buffered.

A single write can be buffered in the 1-deep write buffer of the upstream side. When a non-exclusive write transfer is marked as bufferable, and there is a transfer already pending in the latch, the write buffer can store the incoming write and respond to the slave with a ready response. Due to the nature of buffering, it is possible that an error response only occurs after the data phase of the write transfer, in which case an active high level interrupt is generated on the fast clock as an error signal towards the initiator of the transfer.

When master lock sequences are detected, the downstream side automatically inserts IDLE transfers between two locked sequences as recommended by the AHB5 specification.

The bridge has one clock input on the fast, upstream side, and one clock enable input for the slow clock on the downstream side. The clock enable signal must be synchronous with the fast clock, and it acts as a clock gating signal to control clock division between the fast and slow AHB5 domains. The slower clock might be present in the system but the AHB5 to AHB5 low-latency sync-down bridge does not use it directly.

The clock enable signal gives information about clock edge coincidences and indicates clock division between the fast and slow AHB domains. This information optimizes the bridge for low-latency. The clock enable signal enables or disables logic only on the slow side of the bridge.

The following figure shows the waveforms of the clock enable signal and the fast and slow AHB5 clocks for a 3:1 frequency ratio between the domains.

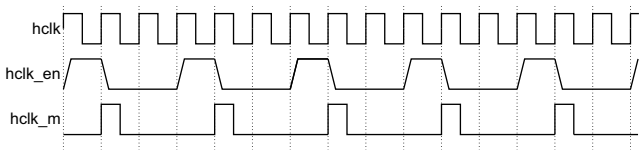


Figure 2-23 Operation of clock enable signal

Note

hclk_m is the slower clock on the downstream side, not an actual clock output from the bridge.

The following figure shows the AHB5 to AHB5 low-latency sync-down bridge.

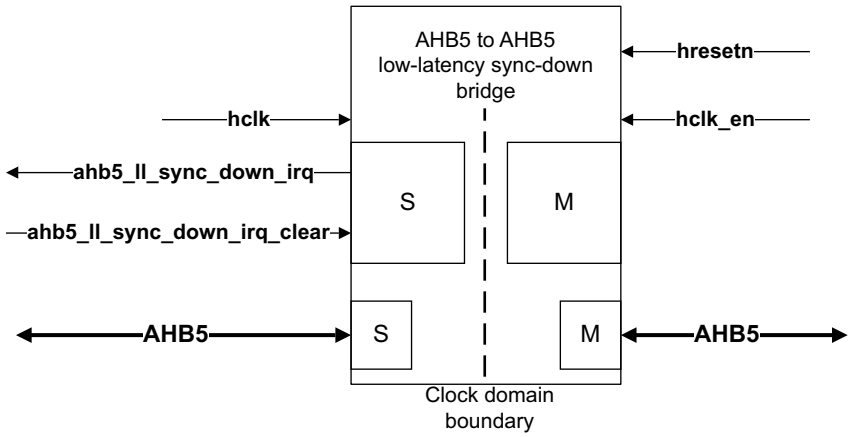


Figure 2-24 AHB5 to AHB5 low-latency sync-down bridge

If a buffered write error occurs, it does not generate an error response. Instead, it generates the active high-level interrupt, **ahb_ll_sync_down_irq**, in the fast **hclk** domain.

2.18.2 Port list

The following table shows the port list of the AHB5 to AHB5 low-latency sync-down bridge.

Table 2-35 AHB5 to AHB5 low-latency sync-down bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock for the upstream side. Synchronous to the downstream side, frequency is N times the AHB5 master clock frequency.
	hresetn	Input	Reset
	hclk_en	Input	Clock enable signal to control clock division.

Table 2-35 AHB5 to AHB5 low-latency sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-35 AHB5 to AHB5 low-latency sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hnonsec_m**	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Miscellaneous	**ahb5_ll_sync_down_irq**	Output	Bufferable write error interrupt (active high level) - clamp to 0.
	ahb5_ll_sync_down_irq_clear	Input	Bufferable write error interrupt clear

2.18.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 low-latency sync-down bridge.

Table 2-36 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through

Table 2-36 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	TRUE	Configurable width

2.19 AHB5 to AHB5 synchronous bridge

This section describes the AHB5 to AHB5 synchronous bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-78.

2.19.1 Functional description

The AHB5 to AHB5 synchronous bridge provides timing isolation. This might be required, for example, in a large AHB5 system.

A parameter defines whether burst transfers are converted into single transfers on the downstream side, or BUSY sequences are inserted while waiting for the new upstream data to arrive. Otherwise the bridge inserts IDLE transfers to the attached slave. If burst is supported and the bridge receives an error response on the downstream side during the sequential beats of the burst, it cancels the remaining transfers in the burst. The upstream side rejects the remaining bursts by providing error responses while the downstream side is kept in IDLE state.

When master lock sequences are detected, the downstream side automatically inserts an unlocked IDLE transfer after the locked sequence is finished as recommended by the AHB5 specification.

Figure 2-25 shows the AHB5 to AHB5 synchronous bridge.

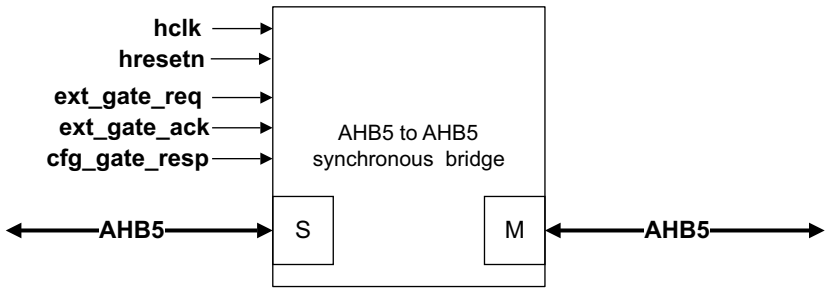


Figure 2-25 AHB5 to AHB5 synchronous bridge

2.19.2 Port list

The following table shows the port list of the AHB5 to AHB5 synchronous bridge.

Table 2-37 AHB5 to AHB5 synchronous bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock for the downstream side
	hresetn	Input	Reset for the downstream side

Table 2-37 AHB5 to AHB5 synchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-37 AHB5 to AHB5 synchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hnonsec_m**	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Miscellaneous	**ext_gate_req**	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge
	cfg_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.19.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 synchronous bridge.

Table 2-38 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.20 AHB5 to AHB5 sync-up bridge

This section describes the AHB5 to AHB5 sync-up bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-80.
- *AHB5 bus properties* on page 2-83.

2.20.1 Functional description

The AHB5 to AHB5 sync-up bridge synchronizes AHB5 interfaces where the upstream side is slower than the downstream side and the clocks are synchronous, in phase, and have a 1:N frequency ratio. It can also be placed on power and clock domain boundaries due to its Q-channel handling capabilities.

A parameter defines whether burst transfers are converted into single transfers on the downstream side, or BUSY sequences are inserted while waiting for the new upstream data to arrive. Otherwise the bridge inserts IDLE transfers to the attached slave. If burst is supported and the bridge receives an error response on the downstream side during the sequential beats of the burst, it cancels the remaining transfers in the burst. The upstream side rejects the remainder of the burst by providing error responses while the downstream side is kept in IDLE state.

Note

An error response on the upstream side only appears as an error interrupt if the respective (bufferable, non-exclusive) write transfer is buffered.

A single write can be buffered in the 1-deep write buffer of the upstream side. When a non-exclusive write transfer is marked as bufferable, and there is a transfer already pending in the latch, the write buffer can store the incoming write and respond back to the slave with a ready response. Due to the nature of buffering, it is possible that an error response only occurs after the data phase of the write transfer, in which case an active high level interrupt is generated on the slow clock as an error signal towards the initiator of the transfer.

When master lock sequences are detected, the downstream side automatically inserts IDLE transfers between two locked sequences as recommended by the AHB5 specification.

The module denies Q-channel requests when there is a pending transfer or a pending error interrupt from the write buffer. Note that the same power-down procedure has to be followed regardless of the write buffer. The system has to guarantee that power-down is not initiated before the last transfer is properly acknowledged by **hreadyout_s**. This condition guarantees that the bridge completes the transfer before the power is removed.

The bridge has two clock inputs:

- **hclk_m** on the downstream side.
- **hclk_s** on the upstream side.

The two clocks are semi-synchronous, that is, **hclk_m** is an integer multiple of **hclk_s**.

The bridge consists of three major blocks:

- An AHB slave on the upstream side.
- An AHB master on the downstream side.

- The handler for all Q-channel interfaces:
  - Logic for response handling.

The following figure shows the AHB5 to AHB5 sync-up bridge module.

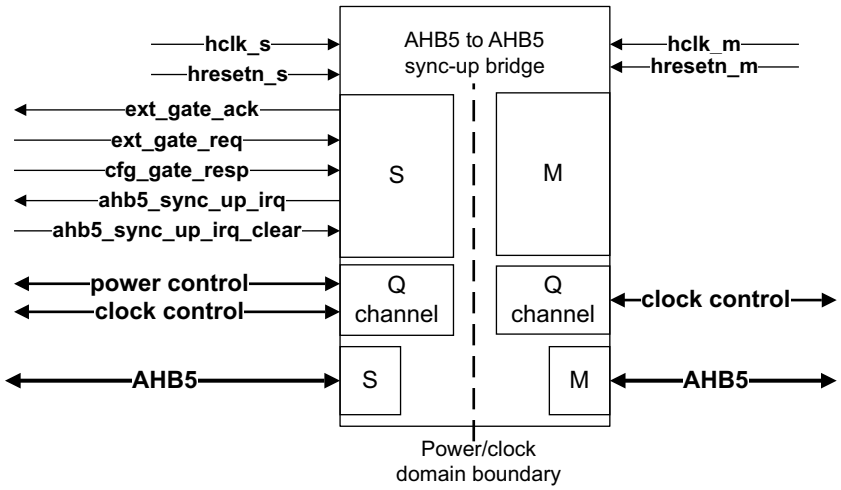


Figure 2-26 AHB5 to AHB5 sync-up bridge

2.20.2 Port list

The following table shows the port list of the AHB5 to AHB5 sync-up bridge.

Table 2-39 AHB5 to AHB5 sync-up bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk_s**	Input	Clock for the upstream side
	hresetn_s	Input	Reset for the upstream side
	hclk_m	Input	Clock for the downstream side (synchronous with **hclk_s,** frequency is N time **hclk_s)**
	hresetn_m	Input	Reset for the downstream side

Table 2-39 AHB5 to AHB5 sync-up bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-39 AHB5 to AHB5 sync-up bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hnonsec_m**	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Q-channel Upstream side	**hclk_qactive_s**	Output	Clock active indication to clock controller
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller
Q-channel Downstream side	**hclk_qactive_m**	Output	Clock active indication to clock controller
	hclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_m	Output	Clock Q Deny to clock controller

Table 2-39 AHB5 to AHB5 sync-up bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Power Q-channel (on downstream side)	**pwr_qactive_s**	Output	Power active indication to power controller
	pwr_qreqn_s	Input	Power Q Request from power controller (active low)
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low)
	pwr_qdeny_s	Output	Power Q Deny to power controller
Miscellaneous	**ahb5_sync_up_irq**	Output	Bufferable write error interrupt, active high-level
	ahb5_sync_up_irq_clear	Input	Bufferable write error interrupt clear
	ext_gate_req	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge
	ext_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.20.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 sync-up bridge.

Table 2-40 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	TRUE	Configurable width

2.21 AHB5 to AHB5 low-latency sync-up bridge

This section describes the AHB5 to AHB5 low-latency sync-up bridge. This bridge is similar in function to the AHB5 to AHB5 sync-up bridge but it is further optimized to reduce latency for designs that do not use Q-channels for power management.

The section contains the following subsections:

2.21.1 Functional description

The AHB5 to AHB5 low-latency sync-up bridge synchronizes AHB5 interfaces where the upstream side is slower than the downstream side, the clocks are synchronous, in phase, and have a 1:N frequency ratio.

A parameter defines whether burst transfers are converted into single transfers on the downstream side, or BUSY sequences are inserted while waiting for the new upstream data to arrive. Otherwise the bridge inserts IDLE transfers to the attached slave. If burst is supported and the bridge receives an error response on the downstream side during the sequential beats of the burst, it cancels the remaining transfers in the burst. The upstream side rejects the remainder of the burst by providing error responses while the downstream side is kept in the IDLE state.

Note

An error response on the upstream side only appears as an error interrupt if the respective (bufferable, non-exclusive) write transfer is buffered.

A single write can be buffered in the 1-deep write buffer of the upstream side. When a non-exclusive write transfer is marked as bufferable, and there is a transfer already pending in the latch, the write buffer can store the incoming write and respond back to the slave with a ready response. Due to the nature of buffering, it is possible that an error response only occurs after the data phase of the write transfer, in which case an active high level interrupt is generated on the slow clock as an error signal towards the initiator of the transfer.

When master lock sequences are detected, the downstream side automatically inserts IDLE transfers between two locked sequences as recommended by the AHB5 specification.

The bridge has one clock input on the fast, downstream side, and a clock enable signal for the slow clock on the upstream side. The clock enable signal must be synchronous with the fast clock, and it acts as a clock gating signal to control the clock division between the fast and slow AHB5 domains. The slower clock might be present in the system but the AHB5 to AHB5 low-latency sync-up bridge does not use it directly.

The clock enable signal gives information about clock edge coincidences and indicates clock division between the fast and slow AHB domains. This information optimizes the bridge for low-latency. The clock enable signal enables or disables logic only on the slow side of the bridge.

The following figure shows the waveforms of the clock enable signal and the fast and slow AHB5 clocks for a 3:1 frequency ratio between the domains.

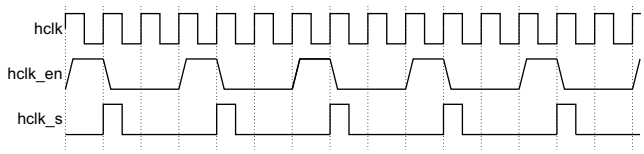


Figure 2-27 Operation of clock enable signal

Note

hclk_s is the slower clock on the upstream side, not an actual clock input to the bridge.

The following figure shows the AHB5 to AHB5 low-latency sync-up bridge module.

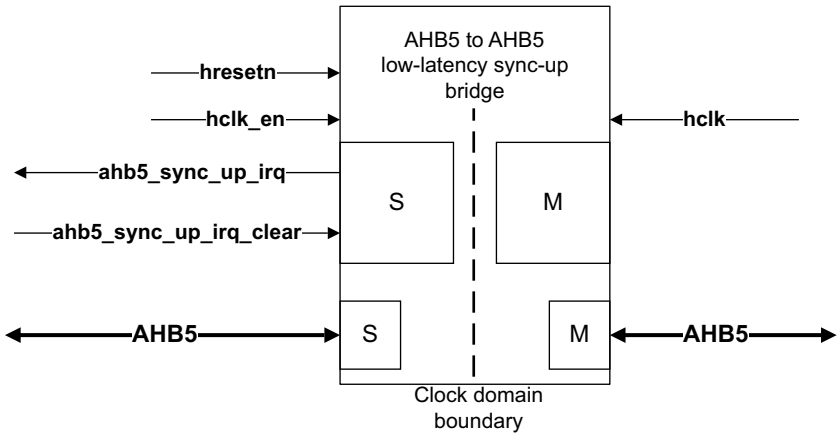


Figure 2-28 AHB5 to AHB5 low-latency sync-up bridge

2.21.2 Port list

The following table shows the port list of the AHB5 to AHB5 low-latency sync-up bridge.

Table 2-41 AHB5 to AHB5 low-latency sync-up bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock for the downstream side Synchronous to the upstream side, frequency is N times the AHB5 slave clock frequency.
	hresetn	Input	Reset for the upstream
	hclk_en	Input	Clock enable to control clock division

Table 2-41 AHB5 to AHB5 low-latency sync-up bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-41 AHB5 to AHB5 low-latency sync-up bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**hnonsec_m**	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width
Miscellaneous	**ahb5_ll_sync_up_irq**	Output	Bufferable write error interrupt, active high-level - clamp to 0.
	ahb5_ll_sync_up_irq_clear	Input	Bufferable write error interrupt clear

2.21.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to AHB5 low-latency sync-up bridge.

Table 2-42 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-42 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	TRUE	Configurable width

2.22 AHB5 to APB4 asynchronous bridge

This section describes the AHB5 to APB4 asynchronous bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-92.

2.22.1 Functional description

The AHB5 to APB4 asynchronous bridge connects an APB4 peripheral device or subsystem to the AHB5 bus. The clock of the APB4 interface is asynchronous to the AHB5 clock. The bridge can also be used to cross a power domain boundary.

There are two handshake signal pairs, request and acknowledge, synchronized between the two clock domains to ensure the correct synchronization of the AHB5 bus signals to the APB4 clock domain.

Figure 2-29 shows the AHB5 to APB4 asynchronous bridge module.

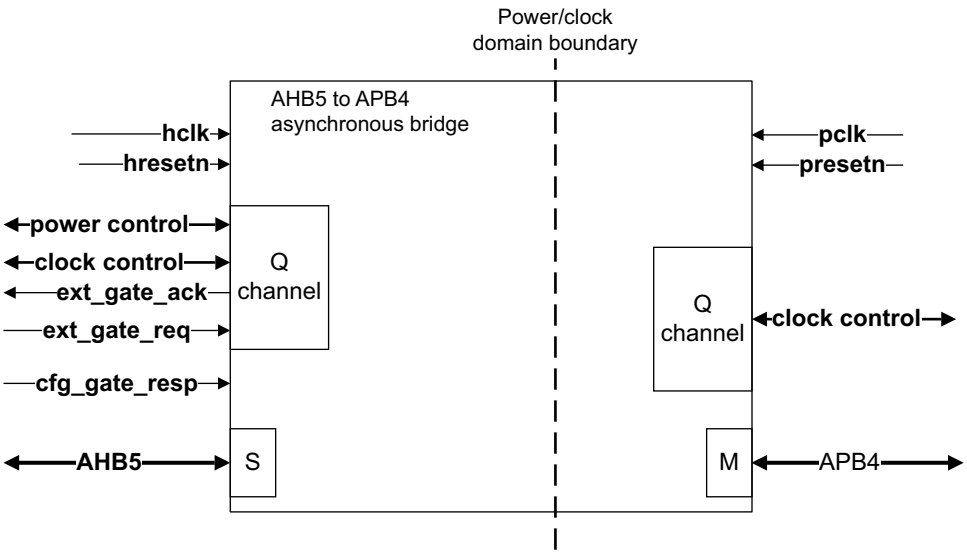


Figure 2-29 AHB5 to APB4 asynchronous bridge

2.22.2 Port list

The AHB5 to APB4 asynchronous bridge has the following interfaces:

- AHB5 Slave Initiator interface to connect to the AHB5 Bus.
- APB4 Master Interface to connect to the peripheral device.
- AHB5 Q-channel clock control.
- AHB5 Q-channel power control.
- APB4 Q-channel clock control.

The following table shows the port list of the AHB5 to APB4 asynchronous bridge.

Table 2-43 AHB5 to APB4 asynchronous bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	AHB5 clock
	hresetn	Input	AHB5 reset
	pclk	Input	APB4 clock
	presetn	Input	APB4 reset
	apb_active	Output	APB bus is active, for clock gating
AHB5 Slave Initiator	**hsel**	Input	Slave select
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	Transfer completion indicator
	hprot[6:0]	Input	Protection control
	hwdata[DATA_WIDTH-1:0]	Input	Write data, configurable width
	hmaster[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata[DATA_WIDTH-1:0]	Output	Read data, configurable width
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response
	hnonsec	Input	Non-secure Transfer Indicator

Table 2-43 AHB5 to APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
APB4 Master	**pmaster[MASTER_WIDTH-1:0]**	Output	Master identifier
	paddr[ADDR_WIDTH-1:0]	Output	Address, configurable width
	pprot[2:0]	Output	Protection control
	pwrite	Output	Transfer direction indicator
	psel	Output	Slave select
	pstrb[3:0]	Output	Write strobe
	penable	Output	Enable
	pwdata[31:0]	Output	Write data
	prdata[31:0]	Input	Read data
	pready	Input	Ready
	pslverr	Input	Transfer failure
AHB5 clock control Q-channel	**hclk_qactive_s**	Output	Clock active indication to clock controller
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller
AHB5 power control Q-channel	**pwr_qactive_s**	Output	Power active indication to power controller
	pwr_qreqn_s	Input	Power Q Request from power controller (active low)
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low)
	pwr_qdeny_s	Output	Power Q Deny to power controller
APB4 clock control Q-channel	**pclk_qactive_m**	Output	Clock active indication to clock controller
	pclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	pclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	pclk_qdeny_m	Output	Clock Q Deny to clock controller

Table 2-43 AHB5 to APB4 asynchronous bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Miscellaneous	**ext_gate_req**	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge.
	cfg_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.22.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to APB4 asynchronous bridge.

Table 2-44 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through. PPROT[1] used to generate HNONSEC
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported
Exclusive_Transfers	TRUE	Pass-through. Changes to FALSE when ports removed.
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not supported as they are not found on APB

2.23 AHB5 to APB4 sync-down bridge

This section describes the AHB5 to APB4 sync-down bridge.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-94.
- *AHB5 bus properties* on page 2-96.

2.23.1 Functional description

The AHB5 to APB4 sync-down bridge is configurable to have registered or unregistered write data.

The bridge connects an APB4 peripheral device to the AHB5 bus where the upstream AHB5 side is faster than, or equal in frequency to, the downstream APB4 side, and the clocks are synchronous, in phase, and have an N:1 frequency ratio. The bridge can also be used to cross a power domain boundary.

You can register the write data, if you set the REGISTER_WDATA parameter to 1. Registering write data can help reduce timing issues caused by large fanouts. The default value is 0.

Figure 2-30 shows the AHB5 to APB sync-down bridge.

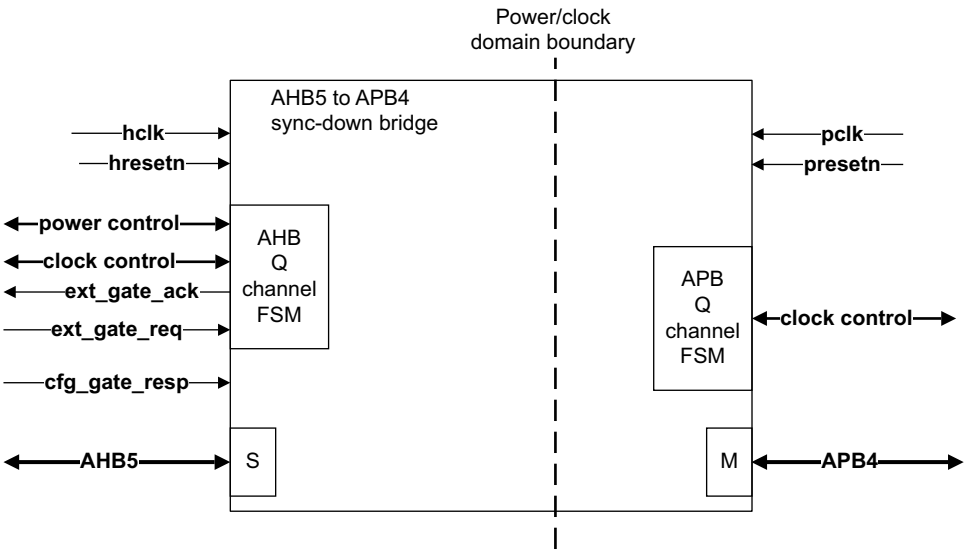


Figure 2-30 AHB5 to APB4 sync-down bridge

For systems that require a high operating frequency, set the `REGISTER_WDATA` Verilog parameter to 1 to register the AHB5 master write data. This breaks the path between **HWDATA** and **PWDATA** but increases the latency of write transfers by one cycle.

The **PPROT** signal of the APB4 is generated in the following way to include the security state of the transfer:

- **pprot[0] = hprot[1]**
- **pprot[1] = hnonsec**
- **pprot[2] = ~hprot[0]**

2.23.2 Port list

The AHB5 to APB4 sync-down bridge has the following interfaces:

- AHB5 Slave Initiator interface to connect to the AHB5 Bus.
- APB4 Master Interface to connect to the periphery device.
- Q-channel for AHB5 side clock control.
- Q-channel for APB4 side clock control.
- Q-channel for power control.

The following table shows the port list of the AHB5 to APB4 sync-down bridge.

Table 2-45 AHB5 to APB4 sync-down bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	AHB5 Clock
	hresetn	Input	AHB5 Reset
	pclk	Input	APB side clock (balanced synchronous to AHB5 Clock)
	presetn	Input	APB Reset
	apb_active	Output	APB bus is active, for clock gating
AHB5 Slave Initiator	**hsel**	Input	Slave select
	hnonsec	Input	Non-secure transfer indicator
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	Transfer completion indicator
	hprot[3:0]	Input	Protection control
	hprot[6:4]	Input	Protection control extension (AHB5 only)
	hwdata[31:0]	Input	Write data, configurable width (DATA_WIDTH)
	hmaster[MASTER_WIDTH-1:0]	Input	Master identifier (MASTER_WIDTH)
	hrdata[31:0]	Output	Read data, configurable width
	hreadyout	Output	Device ready
	hresp	Output	Transfer response

Table 2-45 AHB5 to APB4 sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
APB4 Master	**pmaster[MASTER_WIDTH-1:0]**	Output	Master identifier (MASTER_WIDTH)
	paddr[ADDR_WIDTH-1:0]	Output	Address, configurable width
	pprot[2:0]	Output	Protection control
	pwrite	Output	Transfer direction indicator
	psel	Output	Slave select
	pstrb[3:0]	Output	Write strobe
	penable	Output	Enable
	pwdata[31:0]	Output	Write data
	prdata[31:0]	Input	Read data
	pready	Input	Ready
	pslverr	Input	Transfer failure
AHB5 clock control Q-channel	**hclk_qactive_s**	Output	Clock active indication to clock controller
	hclk_qreqn_s	Input	Clock Q Request from clock controller (active low)
	hclk_qacceptn_s	Output	Clock Q Accept to clock controller (active low)
	hclk_qdeny_s	Output	Clock Q Deny to clock controller
AHB5 power control Q-channel	**pwr_qactive_s**	Output	Power active indication to power controller
	pwr_qreqn_s	Input	Power Q Request from power controller (active low)
	pwr_qacceptn_s	Output	Power Q Accept to power controller (active low)
	pwr_qdeny_s	Output	Power Q Deny to power controller
APB4 clock control Q-channel	**pclk_qactive_m**	Output	Clock active indication to clock controller
	pclk_qreqn_m	Input	Clock Q Request from clock controller (active low)
	pclk_qacceptn_m	Output	Clock Q Accept to clock controller (active low)
	pclk_qdeny_m	Output	Clock Q Deny to clock controller

Table 2-45 AHB5 to APB4 sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
Miscellaneous	**ext_gate_req**	Input	External gating request
	ext_gate_ack	Output	External gating acknowledge.
	cfg_gate_resp	Input	Response type when the Access Control Gate (ACG) is blocking the incoming transfers: 0: Waited transfer 1: Error response

2.23.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to APB4 sync-down bridge.

Table 2-46 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through. PPROT[1] used to generate HNONSEC
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through. Changes to FALSE when ports removed.
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	FALSE	Not supported as they are not found on APB

2.24 AHB5 to APB4 low-latency sync-down bridge

This section describes the AHB5 to APB4 low-latency sync-down bridge.

This section describes the AHB5 to APB4 low-latency sync-down bridge. This bridge is similar in function to the AHB5 to APB4 sync-down bridge but it is further optimized to reduce latency for designs that do not use Q-channels for power management.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-98.
- *AHB5 bus properties* on page 2-99.

2.24.1 Functional description

The bridge connects an APB4 peripheral device to the AHB5 bus where the upstream AHB5 side is faster than, or equal in frequency to, the downstream APB4 side, and the clocks are synchronous, in phase, and have an N:1 frequency ratio.

The bridge has one clock input on the fast, upstream, AHB5 side, and a clock enable signal for the slow clock on the downstream, APB4 side. The clock enable signal must be synchronous with the fast clock, and it acts as a clock enable signal for the rising edge to control the clock division between the fast and slow AHB5 domains. The clock enable signal gives timing information which is used to optimize the bridge low-latency. The actual lower frequency clock, the lower frequency, might be present in the system but the AHB5 to APB4 low-latency sync-down bridge does not use it directly.

The following figure shows the AHB5 to APB sync-down bridge.

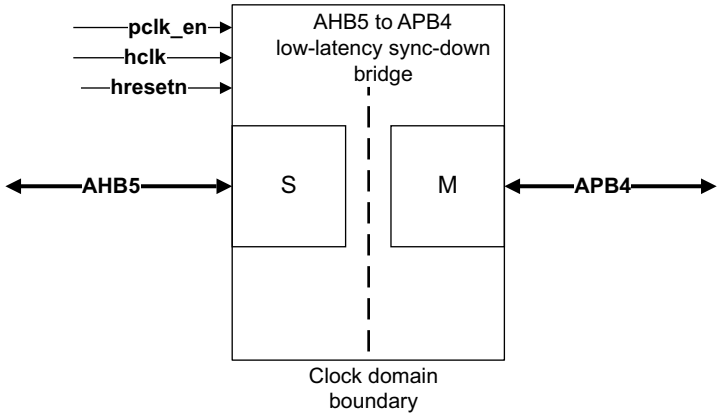


Figure 2-31 AHB5 to APB4 low-latency sync-down bridge

The AHB5 to APB4 low-latency sync-down bridge is configurable to have registered or unregistered write data.

Long timing paths can be broken to improve synthesis performance by setting the appropriate parameters:

- You can register the AHB5 master write data if you set the REGISTER_WDATA parameter to 1. Registering write data can reduce timing issues caused by large fanouts. The default is 0.
- You can register the return path, response and read data, by setting REGISTER_RDATA.

You can also independently control the registering of the address and control signals with REGISTER_CNTRL.

The **PPROT** signal of the APB4 is generated in the following way to include the security state of the transfer:

- **pprot[0] = hprot[1]**
- **pprot[1] = hnonsec**
- **pprot[2] = ~hprot[0]**

2.24.2 Port list

The following table shows the port list of the AHB5 to APB4 low-latency sync-down bridge.

Table 2-47 AHB5 to APB4 low-latency sync-down bridge port list

Block	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	AHB5 Clock
	hresetn	Input	AHB5 Reset
	pclk_en	Input	APB clock enable
	apb_active	Output	APB bus is active, for clock gating
AHB5 Slave Initiator	**hsel**	Input	Slave select
	hnonsec	Input	Non-secure transfer indicator
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	Transfer completion indicator
	hprot[6:0]	Input	Protection control
	hwdata[31:0]	Input	Write data
	hmaster[MASTER_WIDTH-1:0]	Input	Master identifier (MASTER_WIDTH)
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Device ready
	hresp	Output	Transfer response

Table 2-47 AHB5 to APB4 low-latency sync-down bridge port list (continued)

Block	SIGNAL	DIRECTION	DESCRIPTION
APB4 Master	**pmaster[MASTER_WIDTH-1:0]**	Output	Master identifier (MASTER_WIDTH)
	paddr[ADDR_WIDTH-1:0]	Output	Address, configurable width
	pprot[2:0]	Output	Protection control
	pwrite	Output	Transfer direction indicator
	psel	Output	Slave select
	pstrb[3:0]	Output	Write strobe
	penable	Output	Enable
	pwdata[31:0]	Output	Write data
	prdata[31:0]	Input	Read data
	pready	Input	Ready
	pslverr	Input	Transfer failure

2.24.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 to APB4 low-latency sync-down bridge.

Table 2-48 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through. **hnonsec** tied to **pprot[1]**.
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Exclusive access signals are not implemented.
Multi_Copy_Atomicity	FALSE	Write buffering supported (WRITE_BUFFER=1)
	TRUE	Write buffering not supported (WRITE_BUFFER=0)
User signaling	FALSE	Not supported as they are not found on APB

2.25 AHB5 upsizer

This section describes the AHB5 upsizer.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-102.

2.25.1 Functional description

The AHB5 upsizer allows a narrow AHB5 bus master to connect to a double-width AHB5 slave.

Due to the nature of upsizing, there is no need for HTRANS conversion or dividing a wide transfer to two narrow ones such as in case of the AHB5 downsizer.

Figure 2-32 shows the AHB5 upsizer module.

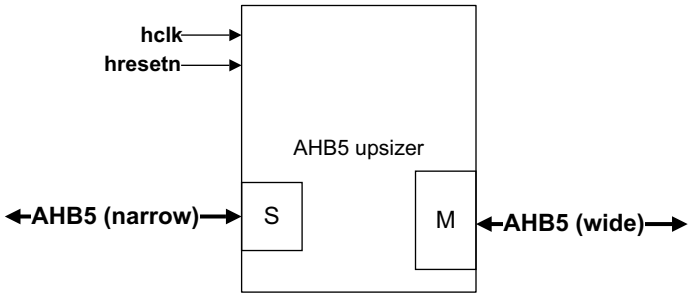


Figure 2-32 AHB5 upsizer

The HRDATA multiplexing is done in a way based on the endianness configuration setting as described in the AHB5 standard and the HADDR of the current transaction.

The HWDATA is replicated on both halves of the wide AHB5 bus, regardless of endianness setting.

2.25.2 Port list

The following table shows the port list of the AHB5 upsizer.

Table 2-49 ABHB5 upsizer port list

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock AHB5 side
	hresetn	Input	Reset for **hclk** domain

Table 2-49 ABHB5 upsizer port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Slave Interface	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width.
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	HREADY feedback from all slaves
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width.
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier, configurable width.
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width.
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width.
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width.
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width.

Table 2-49 ABHB5 upsizer port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master Interface	**hsel_m**	Output	Slave select
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width.
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[(DATA_WIDTH*2)-1:0]	Output	Write data, configurable width.
	hexcl_m	Output	Exclusive transfer
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier, configurable width.
	hrdata_m[(DATA_WIDTH*2)-1:0]	Input	Read data, configurable width.
	hreadyout_m	Input	Transfer completion indicator from slave
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay (AHB5 only)
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width.
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width.
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width.

2.25.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 upsizer.

Table 2-50 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	Configurable	-
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-50 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.26 AHB5 TrustZone master security controller

This section describes the AHB5 TrustZone master security controller.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-107.
- *AHB5 bus properties* on page 2-111.

2.26.1 Functional description

The AHB5 TrustZone master security controller (MSC) is an adapter used to connect a legacy AHB-lite master, or an AHB5 master without the security extension to an AHB5 system and add TrustZone for ARMv8-M capability.

Figure 2-33 shows the AHB5 master security controller.

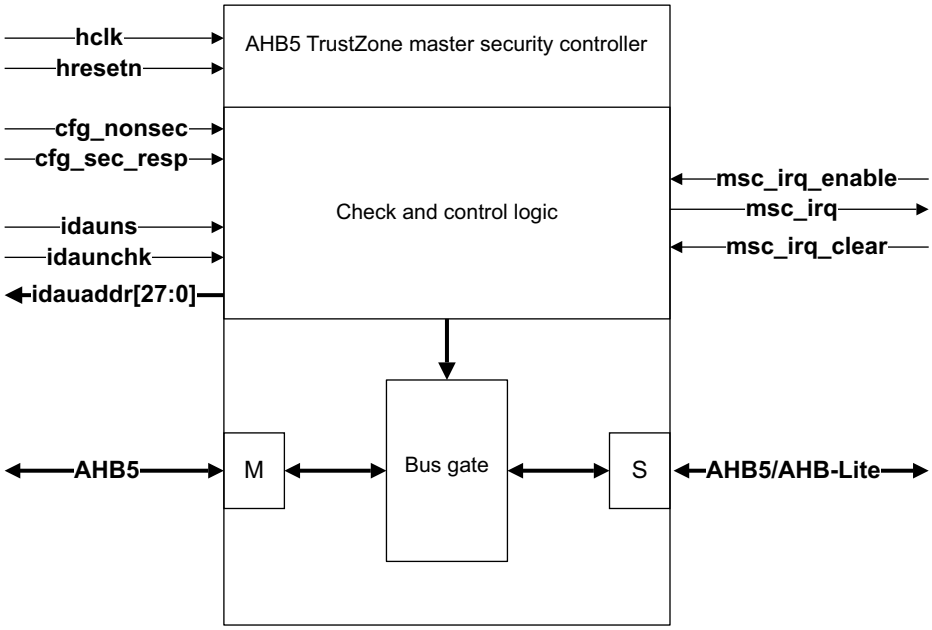


Figure 2-33 AHB5 TrustZone master security controller

The AHB5 TrustZone master security controller is connected to an AHB-Lite master, or a non security-aware AHB5 master over the AHB5 slave.

The **cfg_nonsec** input enables the system security controller to set a bus master, for example a DMA controller, to be a non-secure, **cfg_nonsec** = 1, or secure, **cfg_nonsec** = 0, master.

The upper 27 bits of the 32 bit-wide address bus are connected to the Implementation Defined Attribution Unit (IDAU).

See *ARMv8-M Architecture Reference Manual* for more information on IDAU.

The AHB5 master security controller handles the transfers on the AHB5 master according to the values of **idaunchk**, **idauns**, **cfg_nonsec**, and whether the address is inside or outside an Uncheck region.

- Address is inside an Uncheck region:
  - The transfers are always forwarded to the slave, and **hnonsec_m** is set to the value of **cfg_nonsec**.
- Address is not inside an Uncheck region:
  - If the master is configured as a secure master, **cfg_nonsec** = 0, it can access both secure, **idauns** = 0, and non-secure, **idauns** = 1, addresses. In this case, the transfers from the master are forwarded to the slave with **hnonsec_m** set to match the security of the targeted address.
  - If the master is configured as a non-secure master, **cfg_nonsec** = 1, it can access only non-secure, **idauns** = 1, addresses. If a transfer from the non-secure master tries to access a secure address, idauns = 0, the transfer is blocked and an IDLE transfer is sent to the slave.

The following table summarizes this behavior.

Table 2-51 AHB5 master transfers and hnonsec_m values

idaunchk: idauns	cfg_nonsec=0	cfg_nonsec=1
00	Transfer forwarded. **hnonsec_m** = 0	Transfer blocked
01	Transfer forwarded. **hnonsec_m** = 1	Transfer forwarded. **hnonsec_m** = 1
10	Transfer forwarded. **hnonsec_m** = 0	Transfer forwarded. **hnonsec_m** = 1
11	Transfer forwarded. **hnonsec_m** = 0	Transfer forwarded. **hnonsec_m** = 1

The configuration port **cfg_sec_resp** defines the type of response that the module gives to security violations:

- If it is set, and the transfer is blocked, the module sends an interrupt on the **msc_irq** output, and responds with an error on **hresp_s**. The IRQ can be cleared by asserting the active high **msc_irq_clear** pin. The module forwards 2 IDLE transfers to the slave in the next 2 cycles.
- If it is 0, the module generates an RAZ/WI response.

If during a burst, any of the beats of the burst tries to transfer to/from an illegal address, the module masks the rest of the burst, and forwards IDLE transfers on the master port.

Note

If the burst sent to the AHB5 TrustZone master security controller crosses security region boundaries, the value of **hnonsec_m** changes during the burst, which violates the AHB5 protocol.

This is not resolved by the AHB5 TrustZone master security controller. The master must ensure that no bursts are sent to MSC that cross security region boundaries.

Bus responses

The following diagrams summarize the bus responses for security violations.

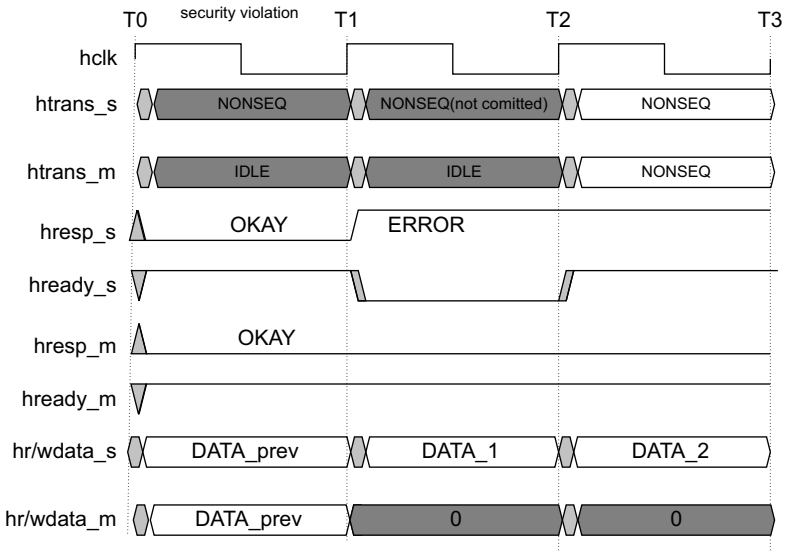


Figure 2-34 Single transfer error response

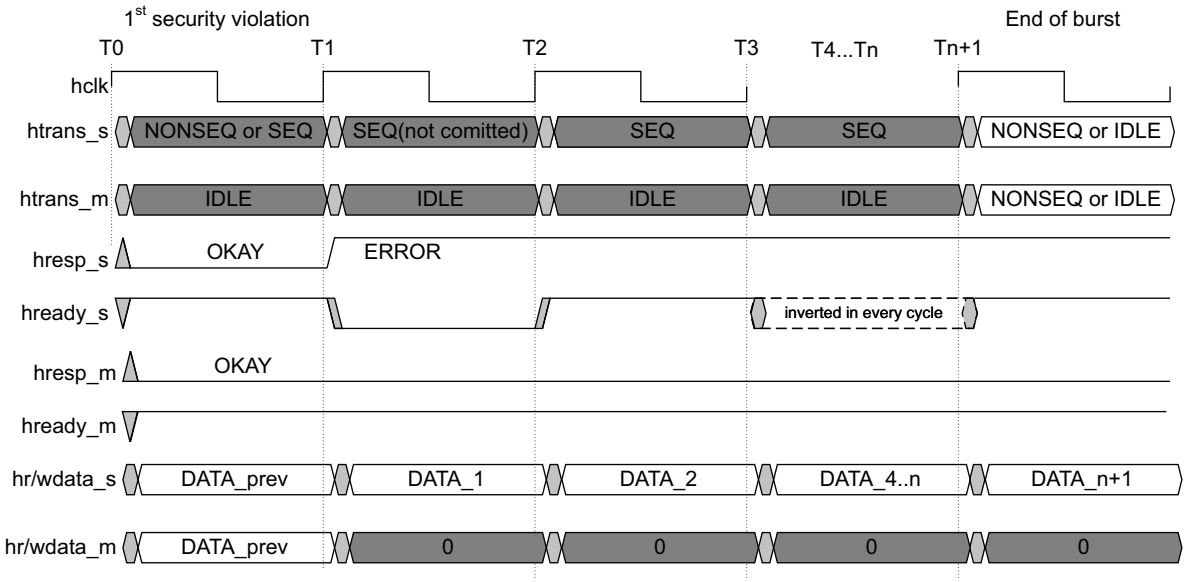


Figure 2-35 Burst transfer error response

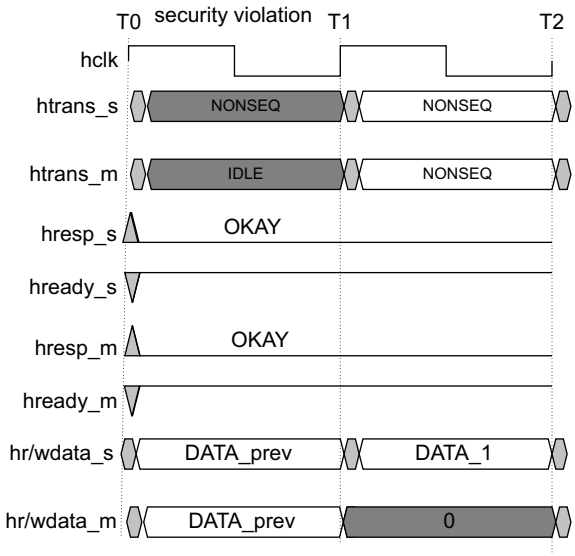


Figure 2-36 Single transfer R(A)ZWI response

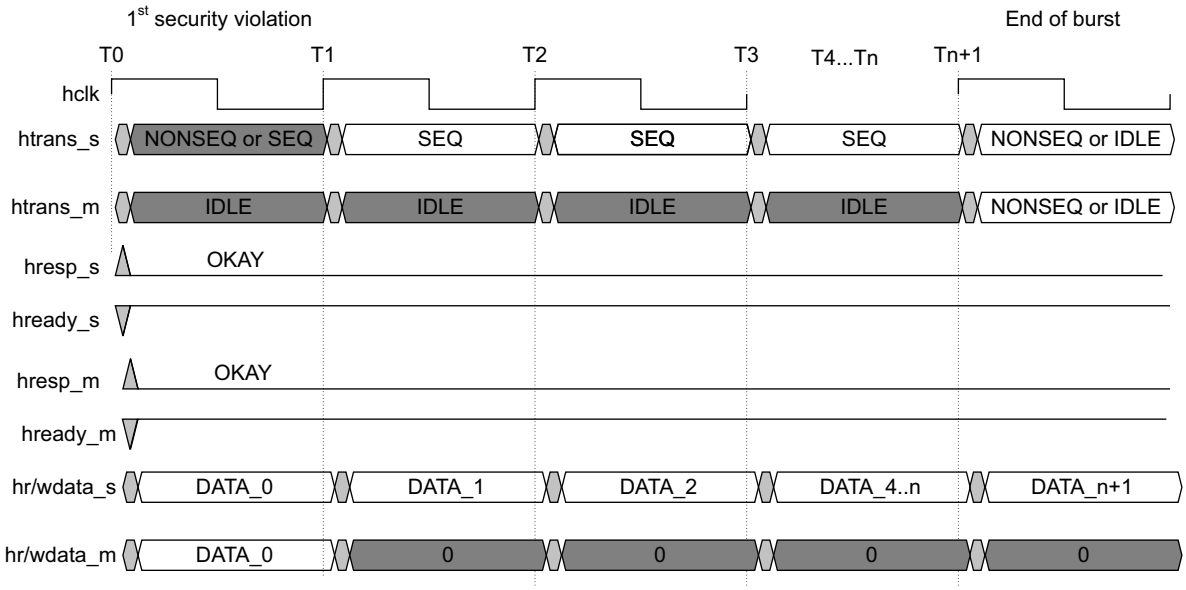


Figure 2-37 Burst transfer R(A)ZWI response

2.26.2 Port list

The AHB5 TrustZone master security controller has the following interfaces:

- AHB5-Lite Slave Initiator interface to connect to an AHB-Lite master, or an AHB5 master without the security extension.
- AHB5 Master interface to connect to the AHB5 Bus.
- IDAU Lite interface to check if the address is Secure or Non-Secure.

- Interrupt.
- Configuration.

The following table shows the port list of the AHB5 TrustZone master security controller.

Table 2-52 AHB5 TrustZone master security controller port list

Function	SIGNAL	DIRECTION	DESCRIPTION	
System	**hclk**	Input	Clock	
	hresetn	Input	Reset	
Config	**cfg_nonsec**	Input	0:	Bus master is secure. Master can send both secure and non-secure transfers. Accesses to secure addresses are not blocked and the security flag, **hnonsec**, is set accordingly.
			1:	Bus master is non-secure. Master can send only non-secure transfers. Access to secure addresses, that is, outside the Uncheck regions, are blocked.
	cfg_sec_resp	Input	0:	R(A)ZWI
			1:	1: Error response
AHB5 Slave Initiator	**haddr_s[31:0]**	Input	Address	

Table 2-52 AHB5 TrustZone master security controller port list (continued)

Function	SIGNAL	DIRECTION	DESCRIPTION
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Output	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width (DATA_WIDTH)
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier (MASTER_WIDTH)
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width (DATA_WIDTH)
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width (USER_WIDTH)
	hauser[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width (USER_WIDTH)
	hwuser[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width (USER_WIDTH)
Interrupt	**msc_irq**	Output	Security Error Interrupt
	msc_irq_clear	Input	Security Error Interrupt Clear
	msc_irq_enable	Input	Security Error Interrupt Enable. Enables security violation interrupt generation: `0`: Security interrupt generation logic turned off. `1`: Security interrupt generation logic turned on.
IDAU Lite	**idauaddr[26:0]**	Output	Address to check by IDAU
	idauns	Input	Non-secure or secure
	idaunchk	Input	Unchecked – accessible both secure and non-secure

Table 2-52 AHB5 TrustZone master security controller port list (continued)

Function	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master	**haddr_m[31:0]**	Output	Address
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Input	Transfer completion indicator
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width (DATA_WIDTH)
	hnonsec_m	Output	Non-secure transfer indicator
	hexcl_m	Output	Exclusive transfer
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier (MASTER_WIDTH)
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width (DATA_WIDTH)
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width (USER_WIDTH)
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width (USER_WIDTH)
	hwuser_m[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width (USER_WIDTH)

2.26.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 TrustZone master security controller.

Table 2-53 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Connects a conventional AHB5 Lite Master to the AHB5 bus and enhances it with the TrustZone for ARMv8-M security features
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.27 AHB5 TrustZone memory protection controller

This section describes the AHB5 TrustZone memory protection controller.

The section contains the following subsections:

- *Functional description*.
- *Port list*.
- *AHB5 bus properties* on page 2-115.

2.27.1 Functional description

The AHB5 TrustZone memory protection controller consists of the following elements:

- An AHB slave interface.
- An AHB master interface.
- A lookup table and registers to determine whether or not a transfer is blocked.

An APB slave interface is present to enable the programming of the internal register bank.

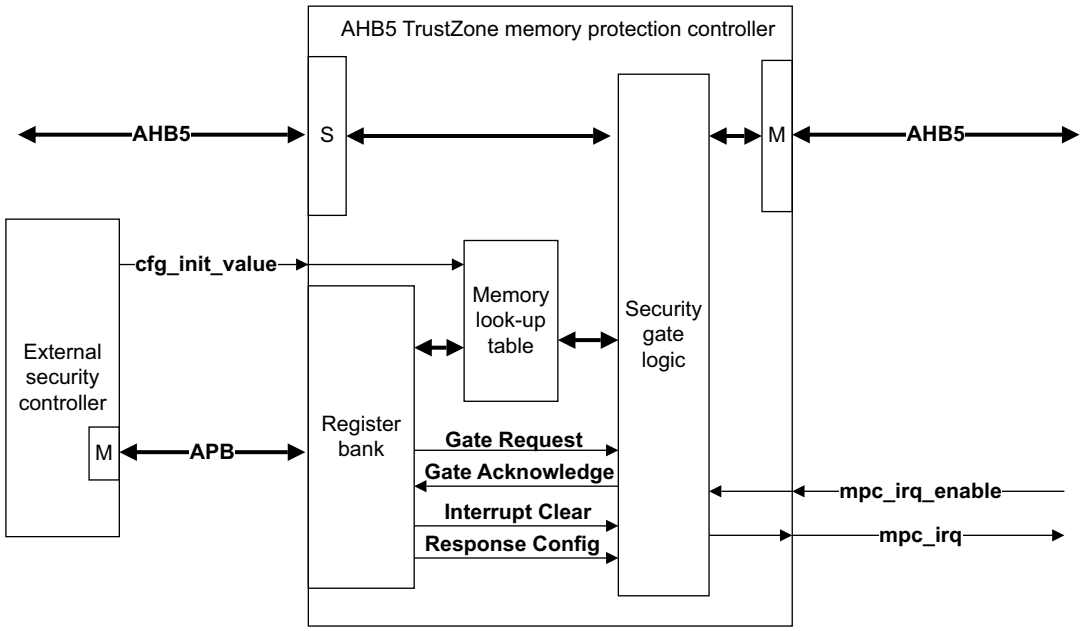


Figure 2-38 AHB5 TrustZone memory protection controller

2.27.2 Port list

The AHB5 TrustZone memory protection controller gates transactions to the AHB5 master interface when a security violation occurs. It can be instantiated in the system in connection to any non-security aware AHB5 memory. The security checking is done based on block/page level which is configured externally by the security controller through an APB interface.

The AHB5 TrustZone memory protection controller provides a full AHB5 Slave interface towards the upstream side and an AHB5 Master interface towards the downstream side of the AHB5 bus, similar to any other bridge-like component. It also provides an APB slave interface for the configuration registers which can be set by the security controller in the system with secure accesses (PPROT[1]==0) only. Identification registers can be read by any type of access.

A dedicated interrupt signal is asserted whenever a security violation is detected. The interrupt must be enabled by both the register bank, and by **mpc_irq_enable** input to enable the assertion of the interrupt signal. The interrupt is cleared by writing to the appropriate register.

The following table shows the port list of the AHB5 TrustZone memory protection controller.

Table 2-54 AHB5 TrustZone memory protection controller port list

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock AHB5 and APB side
	hresetn	Input	Reset for AHB5 and APB domain
AHB5 Slave Interface	**hsel_s**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	HREADY feedback from all slaves
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width.
	hexcl_s	Input	Exclusive Transfer indicator.
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier, configurable width
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width.
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width

Table 2-54 AHB5 TrustZone memory protection controller port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master Interface	**hsel_m**	Output	Slave select pass-through
	hnonsec_m	Output	Non-secure transfer indicator
	haddr_m[ADDR_WIDTH-1:0]	Output	Address, configurable width
	htrans_m[1:0]	Output	Transfer type
	hsize_m[2:0]	Output	Size of the transfer
	hwrite_m	Output	Transfer direction indicator
	hready_m	Output	HREADY feedback to all slaves.
	hprot_m[6:0]	Output	Protection control
	hburst_m[2:0]	Output	Burst type
	hmastlock_m	Output	Locked sequence indicator
	hwdata_m[DATA_WIDTH-1:0]	Output	Write data, configurable width
	hexcl_m	Output	Exclusive Transfer indicator.
	hmaster_m[MASTER_WIDTH-1:0]	Output	Master identifier
	hrdata_m[DATA_WIDTH-1:0]	Input	Read data, configurable width
	hreadyout_m	Input	Transfer completion indicator
	hresp_m	Input	Transfer response
	hexokay_m	Input	Exclusive okay
	hruser_m[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width
	hauser_m[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width

Table 2-54 AHB5 TrustZone memory protection controller port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
APB Interface	**psel**	Input	Slave select
	paddr[11:0]	Input	Address allowing 4 KB space
	pstrb[3:0]	Input	Write strobe
	pwrite	Input	Transfer direction indicator
	penable	Input	Enable
	pprot[2:0]	Input	Protection control
	pwdata[31:0]	Input	Write data
	prdata[31:0]	Output	Read data
	pready	Output	Transfer completion indicator
	pslverr	Output	Transfer response
Miscellaneous	**mpc_irq**	Output	Security violation interrupt
	mpc_irq_enable	Input	Enable security violation interrupt generation: 0: Security interrupt generation logic turned off 1: Security interrupt generation logic turned on
	cfg_init_value	Input	Selection of default content at initialization for all blocks 0: Secure 1: Non-Secure

2.27.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 TrustZone memory protection controller.

Table 2-55 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Pass-through
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200

Table 2-55 AHB5 properties (continued)

PROPERTY	VALUE	COMMENT
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.28 AHB5 TrustZone peripheral protection controller

This section describes the AHB5 TrustZone peripheral protection controller.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-119.
- *AHB5 bus properties* on page 2-122.

2.28.1 Functional description

The AHB5 TrustZone peripheral protection controller gates transactions to, and responses from, peripherals when a security violation occurs.

It can be instantiated in the system in connection to any non-security aware peripherals.

Security checking is based on the peripheral (HSEL) level which is configured externally by configuration inputs.

Summary of controller functions:

- Bus interfaces are AHB5.
- Implements multiplexing of slave driven AHB5 signals to the upstream interface.
- Master driven AHB5 signals are decoded and propagated to all enabled downstream interfaces.
- Sideband configuration ports are evaluated at the start of each AHB5 NONSEQ transfer.
- 16 downstream interfaces.
- Non-secure transfers to secure ports and secure transfers to non-secure ports are blocked.
- Non-privileged transfers are blocked if not enabled by cfg_ap for the given port.
- The **ahb_ppc_irq** interrupt is asserted for blocked transfers.
- The **ahb_ppc_irq** interrupt is an active high, level interrupt.
- The **ahb_ppc_irq** interrupt is cleared by **ahb_ppc_irq_clear**.
- A dedicated downstream interface is present to connect a default slave, selected by **hsel[16]**.
- No security checking is performed on transfers targeting the default slave downstream interface.
- No security checking is performed on interfaces masked by NONSEC_MASK.
- A high level on **ahb_ppc_irq_clear** prevents **ahb_ppc_irq** generation.

The following figure shows the AHB5 TrustZone peripheral protection controller.

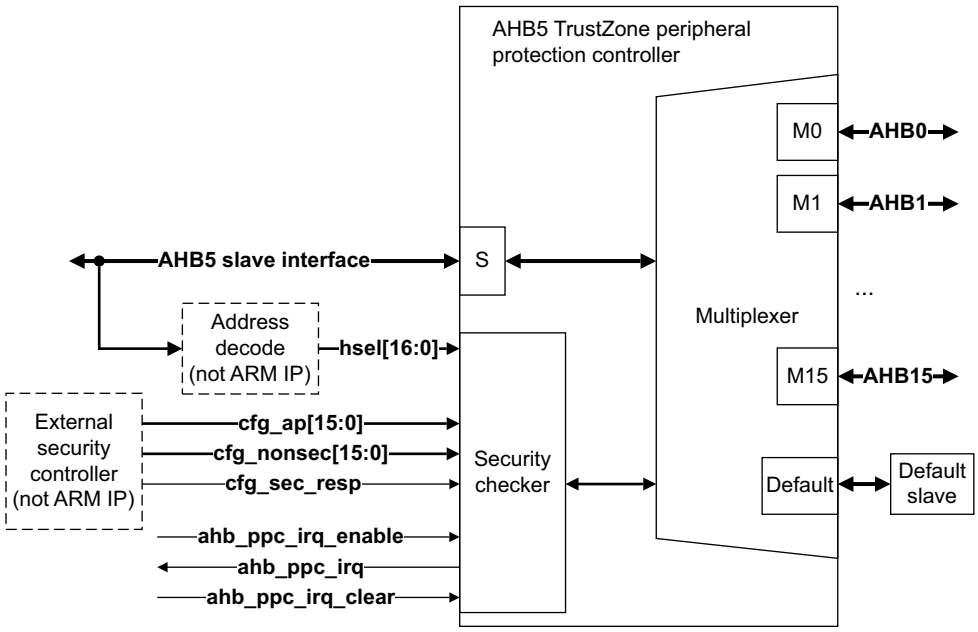


Figure 2-39 AHB5 TrustZone peripheral protection controller

Transfers entering on the AHB5 slave port are only forwarded to master port "X" if the corresponding master port is enabled and the transfer itself matches the security settings of that master port. The module has 16 master ports for peripherals and one for a default slave.

The destination master port is selected by **hsel[15:0]**, which is supplied by an external address decoder and has to be either 0x0 (nothing selected) or one-hot-encoded (valid master port). The lower sixteen bits, **hsel[15:0]**, correspond to real peripherals with configurable security settings, whereas **hsel[16]** is used to access an external default slave without performing security checking.

The security settings are applied through 16-bit wide configuration ports driven by external configuration registers: **cfg_ap[15:0]** defines the privileged access rights while **cfg_nonsec[15:0]** defines the Trustzone specific security settings. For both configurations, there is one bit assigned to each master port. Alternatively, the Trustzone specific security checking can be disabled by the Verilog parameter, NONSEC_MASK.

The configuration ports are evaluated at the first clock cycle of the address phase of each AHB5 NONSEQ transfer.

If an AHB5 transfer causes a security violation, the component blocks the transfer and generates an interrupt. In addition, depending on the configuration, **cfg_sec_resp**, the component either generates an error response or treats the violating access as RAZ/WI.

Trustzone security checking and downstream **hsel** decoding is done based on the following table:

Table 2-56 TrustZone security checking and downstream hsel decoding

hnonsec	cfg_nonsec[x]	hsel[x]	Case description	hselX output
X	X	0	No AHB5 slave is selected.	0
0	0	1	AHB5 slave #x selected with Secure transfer and slave is configured as Secure	1
0	1	1	AHB5 slave #x selected with Secure transfer and slave is configured as Non-Secure (disallowed)	0 – select Security Responder • RAZ/WI if **cfg_sec_resp**==0 • Return Error if **cfg_sec_resp**==1 • SecureErrorIRQ asserted
1	0	1	AHB5 slave #x selected with Non-Secure transfer, but slave configured as secure (Disallowed)	0 – select Security Responder: • RAZ/WI if **cfg_sec_resp**==0 • Return Error if **cfg_sec_resp**==1 • SecureErrorIRQ asserted
1	1	1	AHB5 slave #x selected with Non-Secure transfer, and slave configured as non-secure (Allowed)	1

2.28.2 Port list

The AHB5 TrustZone peripheral protection controller provides an AHB5 Slave interface towards the upstream side and multiple full AHB5 Master interfaces towards the downstream side of the AHB5 bus. It also provides some configuration signals which can be set by the security controller in the system. A dedicated interrupt signal generates a level interrupt whenever a security violation is detected, which can be cleared by an associated clear signal.

The following table shows the port list of the AHB5 TrustZone peripheral protection controller.

Table 2-57 AHB5 TrustZone peripheral protection controller port list

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
System	**hclk**	Input	Clock AHB5 side
	hresetn	Input	Reset for **hclk** domain
Configuration	**cfg_ap[15:0]**	Input	Non-privileged access enabled on selected port.
	cfg_nonsec[15:0]	Input	Non-secure access enabled on selected port.
	cfg_sec_resp	Input	Response configuration in case of security violation: • bus-error (1) • RAZ/WI (0)

Table 2-57 AHB5 TrustZone peripheral protection controller port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
Interrupt	**ahb_ppc_irq**	Output	Security violation interrupt
	ahb_ppc_irq_enable	Input	Security violation interrupt enable. Enables security violation interrupt generation 0: Security interrupt generation logic turned off 1: Security interrupt generation logic turned on
	ahb_ppc_irq _clear	Input	Security violation interrupt clear
AHB5 Slave	**hsel_s[16:0]**	Input	Slave select
	hnonsec_s	Input	Non-secure transfer indicator
	haddr_s[ADDR_WIDTH-1:0]	Input	Address
	htrans_s[1:0]	Input	Transfer type
	hsize_s[2:0]	Input	Size of the transfer
	hwrite_s	Input	Transfer direction indicator
	hready_s	Input	Transfer completion indicator
	hprot_s[6:0]	Input	Protection control
	hburst_s[2:0]	Input	Burst type
	hmastlock_s	Input	Locked sequence indicator
	hwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width.
	hexcl_s	Input	Exclusive Transfer indicator
	hmaster_s[MASTER_WIDTH-1:0]	Input	Master identifier
	hrdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width.
	hreadyout_s	Output	Transfer completion indicator
	hresp_s	Output	Transfer response
	hexokay_s	Output	Exclusive okay
	hauser_s[USER_WIDTH-1:0]	Input	Address channel user signals, configurable width.
	hwuser_s[USER_WIDTH-1:0]	Input	Write channel user signals, configurable width.
	hruser_s[USER_WIDTH-1:0]	Output	Read channel user signals, configurable width.

Table 2-57 AHB5 TrustZone peripheral protection controller port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
AHB5 Master To Peripherals	**hsel_mX**	Output	Slave select
	haddr_mX[ADDR_WIDTH-1:0]	Output	Address
	htrans_mX[1:0]	Output	Transfer type
	hsize_mX[2:0]	Output	Size of the transfer
	hwrite_mX	Output	Transfer direction indicator
	hready_mX	Output	hready feedback to all slaves
	hprot_mX[6:0]	Output	Protection control
	hburst_mX[2:0]	Output	Burst type
	hmastlock_mX	Output	Locked sequence indicator
	hwdata_mX[DATA_WIDTH-1:0]	Output	Write data, configurable width.
	hwnonsec_mX	Output	Non-secure transfer indicator
	hexcl_mX	Output	Exclusive transfer
	hmasterx_mX[MASTER_WIDTH-1:0]	Output	Master identifier
	hreadyout_mX	Input	Transfer completion indicator
	hresp_mX	Input	Transfer response
	hrdata_mX[DATA_WIDTH-1:0]	Input	Read data, configurable width.
	hexokay_mX	Input	Exclusive okay
	hauser_mX[USER_WIDTH-1:0]	Output	Address channel user signals, configurable width.
	hwuser_mX[USER_WIDTH-1:0]	Output	Write channel user signals, configurable width.
	hruser_mX[USER_WIDTH-1:0]	Input	Read channel user signals, configurable width.
AHB5 Master to default slave	**hsel_ds**	Output	Slave select
	htrans_ds[1:0]	Output	Transfer type
	hready_ds	Output	hready feedback to all slaves
	hreadyout_ds	Input	Transfer completion indicator
	hresp_ds	Input	Transfer response
	hexokay_ds	Input	Exclusive tranfer okay response. **Note** Tied to 0 in default slave.

2.28.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 TrustZone peripheral protection controller.

Table 2-58 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Implements security gating for slaves
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.29 APB4 TrustZone peripheral protection controller

This section describes the APB4 TrustZone peripheral protection controller.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-125.
- *APB4 bus properties* on page 2-127.

2.29.1 Functional description

The APB4 TrustZone peripheral protection controller gates transactions to, and responses from, peripherals when a security violation occurs.

The APB4 TrustZone peripheral protection controller can be instantiated in the system in connection to any non-security aware peripherals.

The security checking is done based on peripheral (PSEL) inputs which are configured externally by configuration inputs.

A summary of the controller functions are listed below:

- Bus interfaces are APB4.
- Implements multiplexing of slave driven APB signals to the upstream interface.
- Master driven APB signals pass through and are propagated to all enabled downstream interfaces.
- Configuration sideband signals are sampled when a transaction is not ongoing or at the end a transaction.
- 16 downstream ports.
- Non-secure transfers to secure ports and secure transfers to non-secure ports are blocked.
- Non-privileged transfers are blocked if not enabled by **cfg_ap** for the given port.
- The **apb_ppc_irq** interrupt is asserted for blocked transfers.
- The **apb_ppc_irq** interrupt is an active high, level interrupt.
- The **apb_ppc_irq** interrupt is cleared by **apb_ppc_irq_clear**.
- High level on **apb_ppc_irq_clear** prevents **apb_ppc_irq** generation.

Transfers appearing on the APB slave port are only forwarded to master port “X” if the corresponding master port is enabled and the transfer itself matches the security settings of that master port. The module has 16 master ports for peripherals.

The following figure shows the APB4 TrustZone peripheral protection controller.

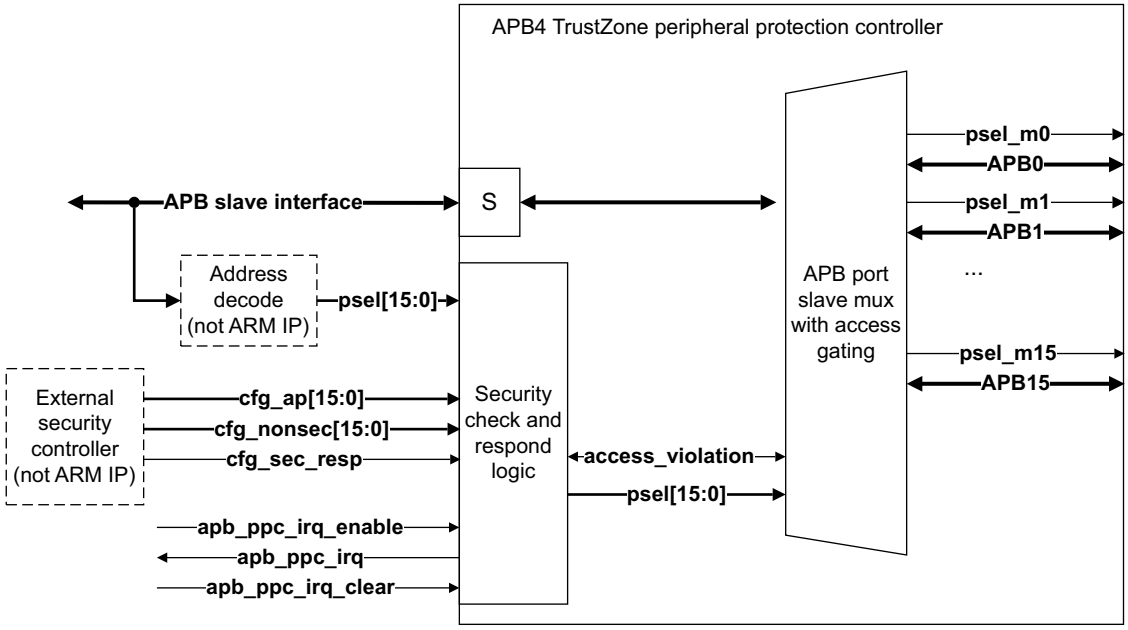


Figure 2-40 APB4 TrustZone peripheral protection controller

The destination master port is selected by **psel[15:0]**, which is supplied by an external address decoder and has to be either 0x0, nothing selected, or one-hot-encoded, valid master port. If a transfer is initiated without selecting a valid master port (**psel[15:0]**=0x0), the module returns RAZ/WI with no wait states.

The security settings are applied through 16-bit wide configuration ports driven by external configuration registers: **cfg_ap[15:0]** defines the privileged access rights while **cfg_nonsec**[15:0] defines the Trustzone specific security settings. For both configurations, there is one bit assigned to each master port. Alternatively, the TrustZone specific security checking can by disabled by the configuration parameter NONSEC_MASK.

If an APB transfer causes a security violation, the module blocks the transfer and generates an interrupt. Depending on the configuration, **cfg_sec_resp**, the module either generates an error response or treats the violating access as RAZ/WI.

Trustzone security checking and downstream psel decoding is done based on the following table:

Table 2-59

pprot_s[1]	cfg_nonsec[x]	psel_s[x]	Case description	psel_mX output
X	X	0	No APB slave is selected.	0 – select default responder: • Return RAZ/WI
0	0	1	APB slave #x selected with Secure transfer and slave is configured as Secure.	1
0	1	1	APB slave #x selected with Secure transfer and slave is configured as Non-Secure (disallowed).	0 – select security responder • RAZ/WI if **cfg_sec_resp**==0 • Return Error if **cfg_sec_resp**==1 • SecureErrorIRQ asserted
1	0	1	APB slave #x selected with Non-Secure transfer, but slave configured as secure (disallowed).	0 – select security responder • RAZ/WI if **cfg_sec_resp**==0 • Return Error if **cfg_sec_resp**==1 • SecureErrorIRQ asserted
1	1	1	APB slave #x selected with Non-Secure transfer, and slave configured as non-secure (allowed).	1

2.29.2 Port list

The APB4 TrustZone peripheral protection controller provides a full APB4 Slave interface towards the upstream side and multiple full APB4 Master interfaces towards the downstream side of the APB bus. It also provides some configuration signals which can be set by the security controller in the system. A dedicated interrupt signal generates a level interrupt whenever security violation is detected, which can be cleared by an associated clear signal.

The following table shows the port list of the APB4 TrustZone peripheral protection controller.

Table 2-60 APB4 TrustZone peripheral protection controller port list

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
System	**pclk**	Input	Clock APB side
	presetn	Input	Reset for **pclk** domain
Configuration	**cfg_ap[15:0]**	Input	Non-privileged access enabled on selected port
	cfg_nonsec[15:0]	Input	Non-secure access enabled on selected port
	cfg_sec_resp	Input	Response configuration in case of security violation: bus-error (1) or RAZ/WI (0), default 0.

Table 2-60 APB4 TrustZone peripheral protection controller port list (continued)

BLOCK	SIGNAL	DIRECTION	DESCRIPTION
Interrupt	**apb_ppc_irq**	Output	Security violation interrupt
	apb_ppc_irq_enable	Input	Security violation interrupt enable. Enables security violation interrupt generation: 0: Security interrupt generation logic turned off 1: Security interrupt generation logic turned on
	apb_ppc_irq_clear	Input	Security violation interrupt clear
APB Slave	**psel_s[15:0]**	Input	Slave select, secure.
	paddr_s[ADDR_WIDTH-1:0]	Input	Address, configurable width
	pstrb_s[3:0]	Input	Write strobe
	pwrite_s	Input	Transfer direction indicator
	penable_s	Input	Enable
	pprot_s[2:0]	Input	Protection control
	pwdata_s[DATA_WIDTH-1:0]	Input	Write data, configurable width.
	prdata_s[DATA_WIDTH-1:0]	Output	Read data, configurable width.
	pready_s	Output	Transfer completion indicator
	pslverr_s	Output	Transfer response
APB Master	**psel_mX**	Output	Slave select
	paddr_mX[ADDR_WIDTH-1:0]	Output	Address, configurable width.
	pstrb_mX[3:0]	Output	Write strobe
	pwrite_mX	Output	Transfer direction indicator
	penable_mX	Output	Enable
	pprot_mX[2:0]	Output	Protection control
	pwdata_mX[DATA_WIDTH-1:0]	Output	Write data, configurable width.
	prdata_mX[DATA_WIDTH-1:0]	Input	Read data, configurable width.
	pready_mX	Input	Transfer completion indicator
	pslverr_mX	Input	Transfer response

2.29.3 APB4 bus properties

The following table shows the APB4 properties of the APB4 TrustZone peripheral protection controller.

Table 2-61 APB4 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	TRUE	Pass-through
Secure_Transfers	TRUE	Implements security gating for APB slaves based on PPROT
Endian	N/A	Pass-through
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	TRUE	Pass-through
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	TRUE	Configurable width

2.30 AHB5 FRBM

This section describes the AHB5 *File Reader Bus Master* (FRBM).

It contains the following subsections:

- *Functional description*.
- *Port list* on page 2-129.
- *AHB5 bus properties* on page 2-130.

2.30.1 Functional description

The AHB5 *File Reader Bus Master* (FRBM) enables designers to simulate AHB5 systems quickly and efficiently by generating explicit bus transfers.

The FRBM can operate with or without an ARM core present. The FRBM and its Perl script are compatible with the version in the FRBM in the ADK and CMSDK.

The FRBM is a generic AHB *Bus Functional Model* (BFM) that directly controls bus activity by interpreting a stimulus file. The FRBM facilitates the efficient validation of components or systems.

The AHB5 File Reader Bus Master can:

- Perform all AHB burst types at data widths of 8, 16, 32, and 64 bits.
- Insert BUSY states during bursts.
- Perform idle transfers.
- Compare received data with the expected data and report the differences during simulations.
- Perform exclusive reads and writes and report exclusive fails during simulation.
- Drive USER signals.
- Compare received USER signals with the expected data and report the differences during simulations.
- Perform all AHB bursts with all the endian configurations.

The steps to use the FRBM to validate a bus are:

1. Create a stimulus file. The stimulus file controls the AHB5 file reader at simulation run time. It does not have a slave interface, and therefore other AHB5 masters cannot address it.
2. Convert the stimulus file. You must transform the human-readable input stimulus file to a data file in Verilog hexadecimal format using the `fm3conv_sie200.pl` preprocessor script.
3. Synthesize the Verilog. The FRBM is designed so that, wherever possible, RTL code is used to describe its logic. All RTL code is written for synthesis, using pragmas where necessary, to enable the component to pass through synthesis tools.
4. Run the simulation with the stimulus signals driving the bus.

Figure 2-41 on page 2-129 shows the AHB5 FRBM.

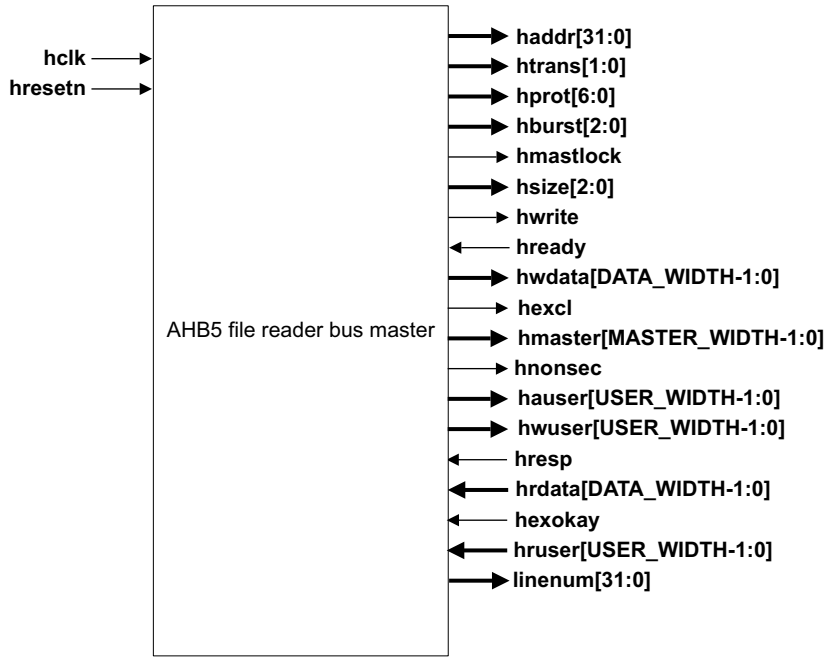


Figure 2-41 AHB5 FRBM

2.30.2 Port list

The following table shows the port list of the AHB5 FRBM.

Table 2-62 AHB5 FRBM port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB side
	hresetn	Input	Reset for **hclk** domain
	linenum	Output	Number of the currently executed line stimulus file

Table 2-62 AHB5 FRBM port list (continued)

Block	Signal	Direction	Description
AHB5 Master Interface	**haddr[31:0]**	Output	Address
	hnonsec	Output	Non-secure transfer indicator
	htrans[1:0]	Output	Transfer type
	hsize[2:0]	Output	Size of the transfer
	hwrite	Output	Transfer direction indicator
	hready	Input	hready feedback from all slaves
	hprot[6:0]	Output	Protection control
	hburst[2:0]	Output	Burst type
	hmastlock	Output	Locked sequence indicator
	hwdata[DATA_WIDTH-1:0]	Output	Write data, configurable width.
	hexcl	Output	Exclusive transfer
	hmaster[MASTER_WIDTH-1:0]	Output	Master identifier, configurable width.
	hauser[USER_WIDTH-1:0]	Output	Address user signal, configurable width.
	hwuser[USER_WIDTH-1:0]	Output	Write data user signal, configurable width.
	hrdata[DATA_WIDTH-1:0]	Input	Read data, configurable width.
	hresp	Input	Exclusive okay
	hexokay	Input	Transfer response
	hruser[USER_WIDTH-1:0]	Input	Read data user signal, configurable width.

2.30.3 AHB5 bus properties

The following table shows the AHB5 properties of the AHB5 FRBM.

Table 2-63 AHB5 properties

PROPERTY	VALUE	COMMENT
Extended_Memory_Types	FALSE	N/A
Secure_Transfers	TRUE	Supported
Endian	FALSE	Default little endian
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported for SIE-200
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents.
User signaling	FALSE	Not used

2.31 Behavioral SRAM model with an AHB5 interface

This section describes the behavioral SRAM model with an AHB5 interface.

The section contains the following subsections:

- *Functional description*.
- *Port list*.

2.31.1 Functional description

The behavioral SRAM model with an AHB5 interface enables you to define an initial memory image and generate wait states for both NONSEQUENTIAL and SEQUENTIAL transfers. The model always replies with an OKAY response.

The following figure shows the model.

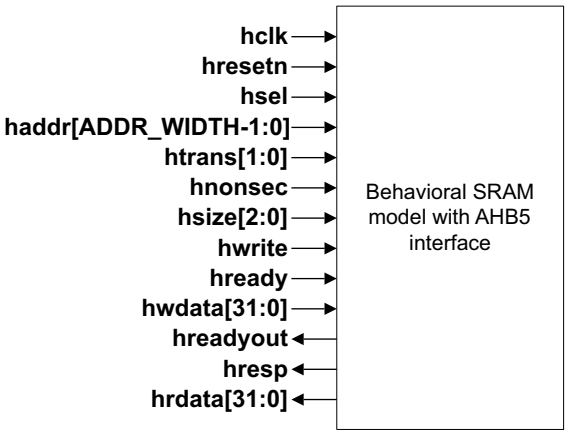


Figure 2-42 ROM wrapper model

2.31.2 Port list

The following table shows the port list of the behavioral SRAM model with an AHB5 interface.

Table 2-64 Behavioral SRAM model with an AHB5 interface port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB side
	hresetn	Input	Reset for **hclk** domain

Table 2-64 Behavioral SRAM model with an AHB5 interface port list (continued)

Block	Signal	Direction	Description
AHB5 Slave interface	**hsel**	Input	Slave select
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	hready feedback from all slaves
	hwdata[31:0]	Input	Write data
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response

2.32 External asynchronous 8-bit SRAM model

This section describes the external asynchronous 8-bit SRAM model.

The section contains the following subsections:

- *Functional description* on page 2-135.
- *Port list* on page 2-135.

2.32.1 Functional description

The external asynchronous 8-bit SRAM is a behavioral model for external 8-bit SRAM that behaves like a typical asynchronous SRAM component. This memory model is compatible with the AHB5 to external memory interface.

The following figure shows the model.

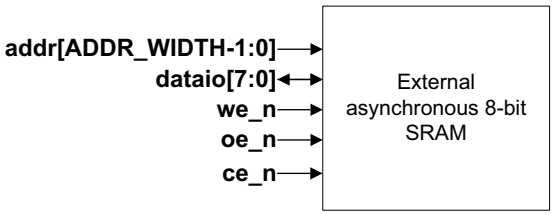


Figure 2-43 FPGA SRAM synthesizable model

2.32.2 Port list

The following table shows the port list of the external asynchronous 8-bit SRAM.

Table 2-65 External asynchronous 8-bit SRAM port list

Block	Signal	Direction	Description
System	**clk**	Input	Clock
RAM interface	**addr[ADDR_WIDTH-1:0]**	Input	Address, configurable width
	dataio[7:0]	Bidirectional	Data.
	we_n	Input	Write enable, active low.
	oe_n	Input	Output enable. Active low for read operation.
	ce_n	Input	Chip enable. Active low for both read and write operations.

2.33 External asynchronous 16-bit SRAM model

This section describes the external asynchronous 16-bit SRAM model.

The section contains the following subsections:

- *Functional description*.
- *Port list*.

2.33.1 Functional description

The external asynchronous 16-bit SRAM is a behavioral model for external 16-bit SRAM that behaves like a typical asynchronous SRAM component. This memory model is compatible with the AHB5 to external memory interface.

The following figure shows the model.

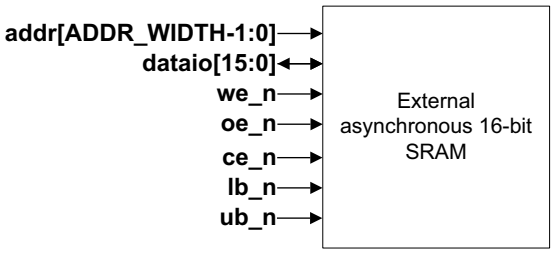


Figure 2-44 FPGA SRAM synthesizable model

2.33.2 Port list

The following table shows the port list of the external asynchronous 8-bit SRAM.

Table 2-66 External asynchronous 8-bit SRAM port list

Block	Signal	Direction	Description
System	**clk**	Input	Clock
RAM interface	**addr[ADDR_WIDTH-1:0]**	Input	Address, configurable width
	dataio[15:0]	Bidirectional	Data.
	we_n	Input	Write enable, active low.
	oe_n	Input	Output enable. Active low for read operation.
	ce_n	Input	Chip enable. Active low for both read and write operations.
	lb_n	Input	Lower byte enable, active low.
	ub_n	Input	Upper byte enable, active low.

2.34 FPGA SRAM synthesizable model

This section describes the FPGA SRAM synthesizable model.

The section contains the following subsections:

- *Functional description*.
- *Port list*.

2.34.1 Functional description

The FPGA SRAM synthesizable model is a model for SRAM that behaves like simple synchronous RAM in ASIC or FPGA. This memory does not have an AHB5 interface and the AHB5 to SRAM interface is required to connect the memory to AHB5. The model demonstrates the use of the AHB5 to SRAM interface and is suitable for FPGA synthesis.

The following figure shows the model.

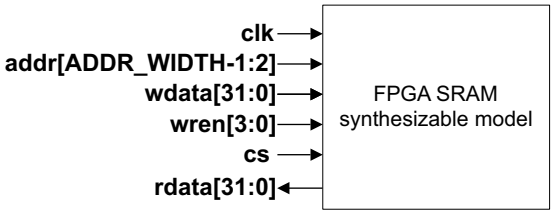


Figure 2-45 FPGA SRAM synthesizable model

2.34.2 Port list

The following table shows the port list of the FPGA SRAM synthesizable model.

Table 2-67 FPGA SRAM synthesizable model port list

Block	Signal	Direction	Description
System	**clk**	Input	Clock
RAM interface	**addr[ADDR_WIDTH-1:2]**	Input	Address, configurable width.
	wdata[31:0]	Input	Write data
	wren[31:0]	Input	Write enable
	cs	Input	Chip select
	rdata[31:0]	Output	Read data

2.35 RAM wrapper model

This section describes the RAM wrapper model.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-137.
- *AHB5 bus properties* on page 2-137.

2.35.1 Functional description

The AHB5 RAM wrapper model is a verification component and is not synthesizable RTL. The model enables easy switching between the following implementations of RAM, depending on the setting of the MEM_TYPE parameter:

- None.
- Behavioral RAM model usign behaviorial SRAM with write disabled.
- SRAM model with an AHB5 SRAM interface module, suitable for ASIC or FPGA flow.
- 16-bit SRAM model with an AHB5 external SRAM interface.
- 8-bit SRAM model with an AHB5 external SRAM interface.

The following figure shows the ROM wrapper model.

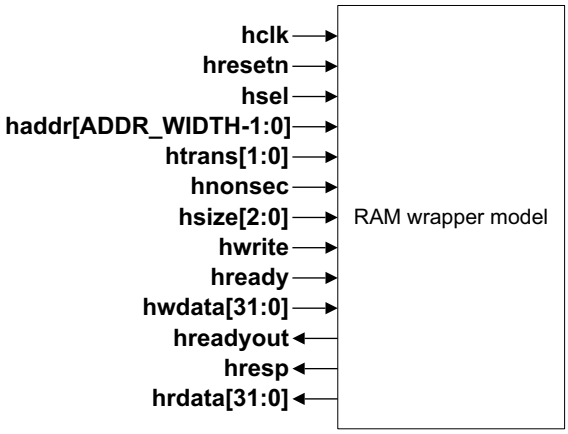


Figure 2-46 ROM wrapper model

2.35.2 Port list

The following table shows the port list of the RAM wrapper model.

Table 2-68 RAM wrapper model port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock AHB side
	hresetn	Input	Reset
AHB5 Slave interface	**hsel**	Input	Slave select
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	hready feedback from all slaves
	hwdata[31:0]	Input	Write data
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response

2.35.3 AHB5 bus properties

The following table shows the AHB5 properties of the RAM wrapper model

Table 2-69 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	Not used
Secure_Transfers	FALSE	Not used
Endian	TRUE	Configurable
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not used

2.36 ROM behavioral model

This section describes the ROM behavioral model.

The section contains the following subsections:

- *Functional description*.
- *Port list*.

2.36.1 Functional description

The ROM behavioral model is as simple behavioral model for ROM memory. Reset and clock signals are used for wait state behavioral modeling.

The following figure shows the model.

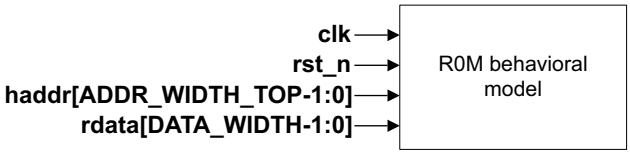


Figure 2-47 ROM behavioral model

2.36.2 Port list

The following table shows the port list of the ROM behavioral model.

Table 2-70 ROM behavioral model port list

Block	Signal	Direction	Description
System	**clk**	Input	Clock for wait state modeling
	rst_n	Input	Reset for wait state modeling
ROM interface	**haddr[ADDR_WIDTH_TOP-1:0]**	Input	Address, configurable width.
	rdata[DATA_WIDTH-1:0]	Output	Read data,configurable width

Note

ADDR_WIDTH_TOP = ADDR_WIDTH - X where X depends on DATA_WIDTH:

- DATA_WIDTH = 32: X = 2.
- DATA_WIDTH = 16: X =1.

2.37 ROM wrapper model

This section describes the ROM wrapper model.

The section contains the following subsections:

- *Functional description*.
- *Port list* on page 2-140.
- *AHB5 bus properties* on page 2-140.

2.37.1 Functional description

The AHB5 ROM wrapper model is a verification component and is not synthesizable RTL. The model enables easy switching between the following implementations of ROM, depending on the setting of the MEM_TYPE parameter:

- None.
- Behavioral ROM model usign behaviorial SRAM with write disabled.
- SRAM model with an AHB5 SRAM interface module, suitable for FPGA flow. This implementation permits read and write operations.
- ROM wrapper with simple 32-bit ROM memory.
- ROM wrapper with simple 16-bit ROM memory.

The following figure shows the ROM wrapper model.

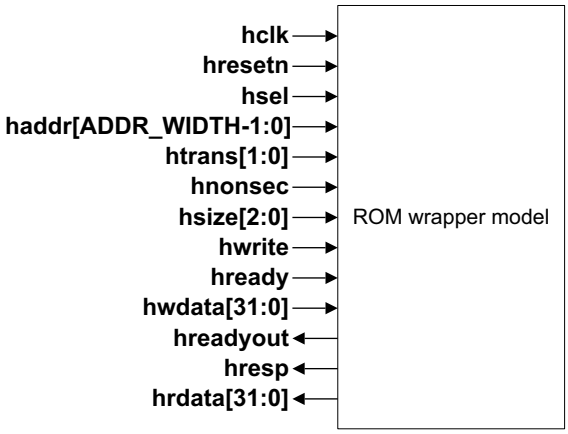


Figure 2-48 ROM wrapper model

2.37.2 Port list

The following table shows the port list of the ROM wrapper model.

Table 2-71 ROM wrapper model port list

Block	Signal	Direction	Description
System	**hclk**	Input	Clock
	hresetn	Input	Reset
AHB5 Slave interface	**hsel**	Input	Slave select
	haddr[ADDR_WIDTH-1:0]	Input	Address, configurable width.
	htrans[1:0]	Input	Transfer type
	hsize[2:0]	Input	Size of the transfer
	hwrite	Input	Transfer direction indicator
	hready	Input	hready feedback from all slaves
	hwdata[31:0]	Input	Write data
	hrdata[31:0]	Output	Read data
	hreadyout	Output	Transfer completion indicator
	hresp	Output	Transfer response

2.37.3 AHB5 bus properties

The following table shows the AHB5 properties of the ROM wrapper model

Table 2-72 AHB5 properties

Property	Value	Comment
Extended_Memory_Types	FALSE	Not used
Secure_Transfers	FALSE	Not used
Endian	TRUE	Configurable
Stable_Between_Clock	FALSE	Not supported for SIE-200
Exclusive_Transfers	FALSE	Not supported
Multi_Copy_Atomicity	TRUE	No caches or buffering that make a transfer visible to only some agents
User signaling	FALSE	Not used

Chapter 3
Programmers Model

This chapter describes the programming interface for the components supplied with the CoreLink SIE-200 System IP for Embedded.

The chapter contains the following sections:

3.1 AHB5 example slave

The following table shows the AHB5 example slave configuration registers.

Table 3-1 Registers

OFFSET	NAME	TYPE	RESET	Security	DESCRIPTION
0x00000	NS_DATA0	RW	0x00	Non-secure	Simple data register.
0x00004	NS_DATA1	RW	0x00	Non-secure	Simple data register.
0x00008	NS_DATA2	RW	0x00	Non-secure	Simple data register.
0x0000C	NS_DATA3	RW	0x00	Non-secure	Simple data register.
0x0010	S_DATA0	RW	0x00	Secure	Simple data register.
0x0014	S_DATA1	RW	0x00	Secure	Simple data register.
0x0018	S_DATA2	RW	0x00	Secure	Simple data register.
0x001C	S_DATA3	RW	0x00	Secure	Simple data register.
0x0020	UNCHK_DATA0	RW	0x00	Unchecked	Simple data register.
0x0024	UNCHK_DATA1	RW	0x00	Unchecked	Simple data register.
0x0028	UNCHK_DATA2	RW	0x00	Unchecked	Simple data register.
0x002C	UNCHK_DATA3	RW	0x00	Unchecked	Simple data register.
0x0030	INT_STAT	RO	0x00	Secure	Bit[0] eg_slv_irq triggered.
0x0034	INT_CLEAR	WO	0x00	Secure	Bit[0] Clear eg_slv_irq.
0x0038	INT_MASK	RW	0x00	Secure	Bit[0] Mask eg_slv_irq.
0x003C	INT_SET	WO	0x00	Secure	For debug. Bit[0] Set eg_slv_irq.
0x0040 - 0x0FCC	-	-	0x00	Unchecked	Reserved
0x0FD0	PIDR4	RO	0x04	Unchecked	Peripheral ID 4 Bit[7:4] block count. Bit[3:0] jep106_c_code.
0x0FD4	PIDR5	RO	0x00	Unchecked	Peripheral ID 5 Not used.
0x0FD8	PIDR6	RO	0x00	Unchecked	Peripheral ID 6 Not used.
0x0FDC	PIDR7	RO	0x00	Unchecked	Peripheral ID 7 Not used.
0x0FE0	PIDR0	RO	0x61	Unchecked	Peripheral ID 0 Bit[7:0] part number.
0x0FE4	PIDR1	RO	0xB8	Unchecked	Peripheral ID 1 Bit[7:4] jep106_id_3_0. Bit[3:0] Part number.

Table 3-1 Registers (continued)

OFFSET	NAME	TYPE	RESET	Security	DESCRIPTION
0x0FE8	PIDR2	RO	0x0B	Unchecked	Peripheral ID 2 Bit[7:4] revision. Bit[3] jedec_used. Bit[2:0] jep106_id_6_4.
0x0FEC	PIDR3	RO	0x00	Unchecked	Peripheral ID 3 Bit[7:4] ECO revision number. Bit[3:0] customer modification number.
0x0FF0	CIDR0	RO	0x0D	Unchecked	Component ID 0.
0x0FF4	CIDR1	RO	0xF0	Unchecked	Component ID 1. PrimeCell class.
0x0FF8	CIDR2	RO	0x05	Unchecked	Component ID 2.
0x0FFc	CIDR3	RO	0xB1	Unchecked	Component ID 3.

3.2 ABH5 GPIO

Most of the AHB5 GPIO registers are checked against the security attribute of the access. Where individual bits are connected to a GPIO in a register, then each bit in the register is checked with the security attribute of the corresponding GPIO port.

When reading such a register the security violating pins return 0, but no security interrupt is generated. There are a number of registers where only secure access is permitted. In these cases, read generates a security error interrupt and either results in a bus error or returns zero based on the configuration of the **cfg_sec_resp** bit.

When attempting to change a bit in a GPIO control register with the wrong security setting for the actual bit, the access generates a security interrupt, if enabled, and then is discarded. When writing to a completely secure register with non-secure access the same applies as in the case of reads.

The following table shows the AHB5 GPIO configuration registers. Undefined bits are Reserved.

Table 3-2 Registers

OFFSET	NAME	TYPE	RESET	Secure access only	DESCRIPTION
0x0000	DATA_IN	RW	0x----	No[a]	Bit[15:0] – Data value (Read value = value sampled at pin Read back value goes through double flip-flop synchronization logic with 2-cycle delay Writing to this register writes directly to the DATA_OUT register.
0x004	DATA_OUT	RW	0x0000	No[a]	Bit[15:0] - Set data output register value. Read value = current value of data output register, write = to data output register.
0x0008	-	-	-		Reserved
0x000C	-	-	-		Reserved
0x010	OUT_EN_SET	RW	0x0000	No[b]	Bit[15:0] – Clear output enable. 1 Clear output enable bit. 0: No effect. Read back: 0: Signal direction is input. 1: Signal direction is output.
0x014	OUT_EN_CLR	RW	0x0000	No[b]	Bit[15:0] – Set output enable. 1 Set output enable bit. 0: No effect. Read back: 0: Signal direction is input. 1: Signal direction is output.

Table 3-2 Registers (continued)

OFFSET	NAME	TYPE	RESET	Secure access only	DESCRIPTION
0x018	ALT_FUNC_SET	RW	0x0000	No[b]	Bit[15:0] – Set alternative function. 1 Set ALTFUNC bit. 0: No effect. Read back: 0: I/O. 1: Alternative function.
0x01C	ALT_FUNC_CLR	RW	0x0000	No[b]	Bit[15:0] – Clear alternative function. 1 Clear ALTFUNC bit. 0: No effect. Read back: 0: I/O. 1: Alternative function.
0x020	INT_EN_SET	RW	0x0000	No[b]	Bit[15:0] – Set interrupt enable. 1 Set interrupt enable. 0: No effect. Read back: 0: Disable interrupt. 1: Enable interrupt.
0x024	INT_EN_CLR	RW	0x0000	No[b]	Bit[15:0] – Clear interrupt enable. 1 Clear interrupt enable. 0: No effect. Read back: 0: Disable interrupt. 1: Enable interrupt.
0x028	INT_TYPE_SET	RW	0x0000	No[b]	Bit[15:0] – Set interrupt type. 1 Set interrupt type. 0: No effect. Read back: 0: Low or high level. 1: Falling or rising edge.
0x02C	INT_TYPE_CLR	RW	0x0000	No[b]	Bit[15:0] – Clear interrupt type. 1 Clear interrupt type. 0: No effect. Read back: 0: Low or high level. 1: Falling or rising edge.

Table 3-2 Registers (continued)

OFFSET	NAME	TYPE	RESET	Secure access only	DESCRIPTION
0x030	INT_POL_SET	RW	0x0000	No[b]	Bit[15:0] – Configure IRQ level or edge polarity. 1 Set interrupt polarity bit. 0: No effect. Read back: 0: Low level or falling edge. 1: High level or rising edge.
0x034	INT_POL_CLR	RW	0x0000	No[b]	Bit[15:0] – Configure IRQ level or edge polarity. 1 Clear interrupt polarity bit. 0: No effect. Read back: 0: Low level or falling edge. 1: High level or rising edge.
0x038	INT_STATUS INT_CLEAR	RW	0x0000	No[b]	Bit[15:0] – GPIO IRQ status register. 1 Clear interrupt request. 0: No effect.
0x003C	-	-	-		Reserved
0x0040	SEC_INT_STAT	RO	0x0000	Yes	Bit[0] – Security error interrupt status (sec_acc_irq).
0x0044	SEC_INT_CLR	WO	0x0000	Yes	Bit[0] – Clear security error interrupt.
0x0048	SEC_INT_MASK	RW	0x0000	Yes	Bit[0] – Mask security error interrupt request output pin. The interrupt generation logic still works. 0: sec_acc_irq is set when SEC_INT_STAT is set. 1: sec_acc_irq is not set when SEC_INT_STAT is set. Bit[1] - Mask PORT_NONSEC_MASK related interrupt generation. 0: Bitmask related violations generate interrupts and set the SEC_INT_STAT and SEC_INT_INFO registers. 1: SEC_INT_STAT and SEC_INT_INFO registers are not set when security violations occur.

Table 3-2 Registers (continued)

OFFSET	NAME	TYPE	RESET	Secure access only	DESCRIPTION
0x004C	SEC_INT_INFO1	RO	0x0000	Yes	Stored information for the first security violation. Set when the first interrupt is set. New values can be stored when the interrupt is cleared. Bit[11:0] - addr[11:0]. Bit[15:12] - byte_strobe. Bit[16] - nonsec. Bit[17] - write.
0x0050	SEC_INT_INFO2	RO	0x0000	Yes	Same description as SEC_INT_INFO1 register except that SEC_INT_INFO2 registers stores the write data. Bit[31:0] - hwdata[31:0].
0x0054	SEC_INT_SET	WO	0x0000	Yes	Bit[0] - Set security error interrupt. For debug only. Sets interrupt status even when sec_irq_enable = 0.
0x0058	PORT_NONSEC_MASK	RO	Parameter dependant	Yes	Bit[15:0] - PORT_NONSEC_MASK parameter value.
0x005C - 0x03FC	-	-	-		Reserved
0x0400 - 0x07FC	MASK_LOW_BYTE	RW	0x----	No[b]	Lower eight bit masked access. Address [9:2] is enable bit mask for write data update. Data is on bit[7:0].
0x0800 - 0x0BFC	MASK_HIGH_BYTE	RW	0x----	No[b]	Upper eight bit masked access. Address [9:2] is enable bit mask for write data update. Data is on bit[15:8]. Bit[7:0] not used.
0x0C00 - 0x0FCC	-	-	-		Reserved
0x0FD0	PIDR4	RO	0x04	No	Peripheral ID 4 Bit[7:4] block count. Bit[3:0] jep106_c_code.
0x0FD4	PIDR5	RO	0x00	No	Peripheral ID 5 Not used.
0x0FD8	PIDR6	RO	0x00	No	Peripheral ID 6 Not used.
0x0FDC	PIDR7	RO	0x00	No	Peripheral ID 7 Not used.

Table 3-2 Registers (continued)

OFFSET	NAME	TYPE	RESET	Secure access only	DESCRIPTION
0x0FE0	PIDR0	RO	0x62	No	Peripheral ID 0 Bit[7:0] part number.
0x0FE4	PIDR1	RO	0xB8	No	Peripheral ID 1 Bit[7:4] jep106_id_3_0. Bit[3:0] Part number.
0x0FE8	PIDR2	RO	0x0B	No	Peripheral ID 2 Bit[7:4] revision. Bit[3] jedec_used. Bit[2:0] jep106_id_6_4.
0x0FEC	PIDR3	RO	0x00	No	Peripheral ID 3 Bit[7:4] ECO revision number. Bit[3:0] customer modification number.
0x0FF0	CIDR0	RO	0x0D	No	Component ID 0.
0x0FF4	CIDR1	RO	0xF0	No	Component ID 1. PrimeCell class.
0x0FF8	CIDR2	RO	0x05	No	Component ID 2.
0x0FFc	CIDR3	RO	0xB1	No	Component ID 3.

a. Individual bits in these registers are checked against security attribute.

b. DATA_IN and DATA_OUT registers do not generate security interrupts but individual bits are checked against the PORT_NONSEC_MASK parameter and transfers result in RAZ/WI access for mismatching bits.

3.3 AHB5 TrustZone memory protection controller

APB accesses are internally aligned to word boundaries, so PADDR[1:0] are ignored. The PSTRB[3:0] write strobe signals indicate which byte or bytes of the data bus contain valid data.

The following table shows the AHB5 TrustZone memory protection controller configuration registers.

Table 3-3 Registers

OFFSET	NAME	TYPE	RESET	DESCRIPTION
0x000	CTRL	RW	0x00000100	Bit[31] – Security lockdown Bit[30:9] – Reserved Bit[8] – Autoincrement Reserved when BLK_SIZE > ADDR_WIDTH-11 Bit[7] – Data interface gating acknowledge (RO) Reserved when GATE_PRESENT = 0 Bit[6] – Data interface gating request. Reserved when GATE_PRESENT = 0 Bit[5] – Reserved Bit[4] – Security error response configuration (CFG_SEC_RESP) 0:RAZ-WI 1: Bus Error Bit[3:0] – Reserved
0x004-0x00C	RSVD	RO	0x0	Reserved
0x010	BLK_MAX	RO	-	Maximum value of block based index register
0x014	BLK_CFG	RO	-	Bit[31] – Init in progress Bit[30:4] - Reserved Bit[3:0] – Block size 0: 32 Bytes 1: 64 Bytes … 15: 1MByte Block size = 1 << (BLK_CFG+5)
0x018	BLK_IDX	RW	0x0	Index value for accessing block based look up table Reserved when BLK_SIZE > ADDR_WIDTH-11. The maximum value of BLK_IDX is defined by the BLK_MAX register.

Table 3-3 Registers (continued)

OFFSET	NAME	TYPE	RESET	DESCRIPTION
0x01C	BLK_LUT[n]	RW	IMPLEMENTATION DEFINED	Block based gating Look Up Table (LUT): Access to block based look up configuration space pointed to by BLK_IDX. Bit[31:0] – each bit indicates one block: If BLK_IDX is 0x0, bit[0] is block #0, bit[31] is block#31. If BLK_IDX is 0x1, bit[0] is block #32, bit[31] is block#63. If BLK_IDX is 0x2, bit[0] is block#64, bit[31] is block#95. … If BLK_IDX is 0xFFF, bit[0] is block#131040, bit[31] is block#131071. The maximum value of BLK_IDX is defined by the BLK_MAX register. For each configuration bit, 0 indicates secure, 1 indicates non-secure. A full word write or read to this register automatically increments the BLK_IDX by one if enabled by CTRL[8]. The upper bits are reserved if BLK_SIZE > ADDR_WIDTH - 11.
0x020	INT_STAT	RO	0x00000000	bit[31:1] – Reserved bit[0] – **mpc_irq** triggered
0x024	INT_CLEAR	WO	0x00000000	bit[31:1] – Reserved bit[0] – **mpc_irq** clear (cleared automatically)
0x028	INT_EN	RW	0x00000001	bit[31:1] - Reserved. bit[0] – **mpc_irq** enable. Enables interrupt output generation. The INT_STAT, INT_INFO1, and INT_INFO2 registers are still set for errors.
0x02C	INT_INFO1	RO	0x00000000	haddr[31:0] of the first security violating address. Bits are valid when **mpc_irq** is triggered. Subsequent security violationg transfers remain blocked, that is, not captured in this register and the register retains its value until **mpc_irq** is cleared.
0x030	INT_INFO2	RO	0x00000000	Additional control bits of the first security violating transfer. Bit [31:18] – Reserved Bit [17] – **cfg_ns** Bit [16] – **hnonse**c Bit [15:0] - **hmaster** Bits are valid when **mpc_irq** is triggered. Subsequent security violating transfers remain blocked, that is, not captured in this register and the register retains its value until **mpc_irq** is cleared.

Table 3-3 Registers (continued)

OFFSET	NAME	TYPE	RESET	DESCRIPTION
0x034	INT_SET	WO	0x00000000	bit[31:1] – Reserved bit[0] – **mpc_irq** set – Debug purpose only. Sets **mpc_irq** triggered in INT_STAT regardless of the mpc_irq_enable input.
0x038 – 0xFCC	RSVD	RO	0x0	Reserved
0xFD0	PIDR4	RO	0x04	Peripheral ID 4 ([7:4] block count, [3:0] jep106_c_code)
0xFD4	PIDR5	RO	0x00	Peripheral ID 5 (not used)
0xFD8	PIDR6	RO	0x00	Peripheral ID 6 (not used)
0xFDC	PIDR7	RO	0x00	Peripheral ID 7 (not used)
0xFE0	PIDR0	RO	0x60	Peripheral ID 0 (Part number [7:0].)
0xFE4	PIDR1	RO	0xB8	Peripheral ID 1 ([7:4] jep106_id_3_0, [3:0] Part number[11:8])
0xFE8	PIDR2	RO	0x1B	Peripheral ID 2 ([7:4] revision, [3] jedec_used, [2:0] jep106_id_6_4)
0xFEC	PIDR3	RO	0x00	Peripheral ID 3 ([7:4] ECO revision number, [3:0] customer modification number)
0xFF0	CIDR0	RO	0x0D	Component ID 0
0xFF4	CIDR1	RO	0xF0	Component ID 1 (PrimeCell class)
0xFF8	CIDR2	RO	0x05	Component ID 2
0xFFC	CIDR3	RO	0xB1	Component ID 3

3.3.1 Look Up Table (LUT) examples

The contents of the LUT can be accessed in several ways that might require different configurations of the autoincrement function of the BLK_IDX register.

To read the full contents of the LUT:

1. Set the autoincrement enable bit, CTRL[8], to 0x1.
2. Read the BLK_MAX register. This has a value 0xN which represents the last address in the LUT.
3. Write 0x0 to the BLK_IDX register.
4. Read the BLK_LUT register 0xN times to read the complete LUT.

To write the full contents of the LUT:

1. Set autoincrement enable bit, CTRL[8], to 0x1.
2. Read the BLK_MAX register. This has a value 0xN which represents the last address in the LUT.
3. Write 0x0 to the BLK_IDX register.

4. Write the new values to the BLK_LUT register `0xN` times to fill the complete LUT.

To read-modify-write a single location:

1. Set autoincrement enable bit, CTRL[8], to `0x0`.
2. Write the required address to the BLK_IDX.
3. Read the current contents of the LUT.
4. Write the new contents to the LUT.
   - Byte accesses can be used to update only the required byte of the register without reading the full contents.

To read-write for a 16-block LUT configuration (ADDR_WIDTH - BLK_SIZE = 9)

1. The autoincrement enable bit in the CTRL register and the BLK_IDX register are reserved.
2. Read the contents fo the BLK_LUT, present on bits[15:0].
3. Write the new contents to BLK_LUT, bits[15:0].

3.3.2 Configuration lockdown

The AHB5 TrustZone memory protection controller provides a configuration lockdown feature that prevents malicious software from changing the security configuration. Writing `0x1` to the security lockdown bit, CTRL[31], enables the configuration lockdown feature.

Once the configuration lockdown feature is enabled:

- It can only be disabled by a component reset which resets CTRL[31] to `0x0`.
- The following registers are read-only:
  - CTRL.
  - BLK_LUT.
  - INT_EN.

Note

ARM recommends that you write `0x1` to the LUT autoincrement bit, CTRL[8] before enabling the configuration lockdown feature. When the feature is enabled only LUT reading is available which is simpler when BLK_IDX increments automatically during the read sequence.

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue A

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue A and issue B

Changes	Location	Affects
Updates, corrections, and improvements for Beta release	Throughout document.	r0p0

Table A-3 Differences between issue B and issue C

Changes	Location	Affects
Updates, corrections, and improvements for Beta update	Throughout document.	r0p0

Table A-4 Differences between issue C and issue D

Changes	Location	Affects
Updates, corrections, and improvements for LAC release	Throughout document.	r1p0

Table A-5 Differences between issue D and issue E

Changes	Location	Affects
Updates, corrections, and improvements for EAC release	Throughout document.	r2p0
Added modules and models for EAC release	*AHB5 example slave* on page 2-10. *AHB5 GPIO* on page 2-17. *AHB5 timeout monitor* on page 2-28. *AHB5 to external SRAM interface* on page 2-32. *AHB5 to ROM interface* on page 2-37. *Cortex-M3/Cortex-M4 AHB5 adapter* on page 2-44. *Behavioral SRAM model with an AHB5 interface* on page 2-131. *External asynchronous 8-bit SRAM model* on page 2-133. *External asynchronous 16-bit SRAM model* on page 2-134. *FPGA SRAM synthesizable model* on page 2-135. *RAM wrapper model* on page 2-136. *ROM behavioral model* on page 2-138. *ROM wrapper model* on page 2-139. Other mentions of these modules and models throughout document.	r2p0

Table A-6 Differences between issue E and issue F

Changes	Location	Affects
Added modules and models for EAC2 release	*Comparison between bridges and their low-latency versions* on page 2-49. *AHB5 to AHB5 low-latency sync-down bridge* on page 2-70. *AHB5 to AHB5 low-latency sync-up bridge* on page 2-84. *AHB5 to APB4 low-latency sync-down bridge* on page 2-97. Other mentions of these modules and models throughout document.	r3p0
Modified TrustZone AHB5 memory protection controller. Minimum number of blocks changed from 64 to 2.	*AHB5 TrustZone memory protection controller* on page 3-9. Other mentions of these modules and models throughout document.	r3p0

Table A-7 Differences between issue F and issue G

Changes	Location	Affects
Memory protection controller: Updated reset value and description of INT_EN register. Updated descriptions of INT_INFO1 and INT_INFO2 registers.	*AHB5 TrustZone memory protection controller* on page 3-9. Table 3-3 on page 3-9.	r3p1
Corrected descriptions of signal **cfg_gate_resp** in bridge modules.	*AHB5 access control gate port list* on page 2-51. *AHB5 to AHB5 and APB4 asynchronous bridge port list* on page 2-60. *AHB5 to AHB5 sync-down bridge port list* on page 2-66. *AHB5 to AHB5 synchronous bridge port list* on page 2-75. *AHB5 to AHB5 sync-up bridge port list* on page 2-80. *AHB5 to APB4 asynchronous bridge port list* on page 2-90. *AHB5 to APB4 sync-down bridge port list* on page 2-94.	r3p1
Cortex-M3/Cortex-M4 AHB5 adapter: Modified description of CODE_MUXED parameter. Corrected AHB5 interface names: Data becomes DCode, Code becomes ICode.	*Cortex-M3/Cortex-M4 AHB5 adapter* on page 2-44. *Functional description* on page 2-44. *Cortex-M3/Cortex-M4 AHB5 adapter port list* on page 2-45.	r3p1