ARM® CoreSight™ ETM-M23

Revision: r0p1

Technical Reference Manual

ARM®

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ARM CoreSight ETM-M23
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
25 April 2016	A	Confidential	First release for r0p0
29 July 2016	B	Confidential	First release for r0p1
18 November 2016	C	Non-Confidential	Second release for r0p1

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110 Fulbourn Road, Cambridge, England CB1 9NJ.

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Product Status

The information in this document is final, that is for a developed product.

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ARM CoreSight ETM-M23 Technical Reference Manual

Preface

This preface introduces the *ARM® CoreSight™ ETM-M23 Technical Reference Manual*. It contains the following sections:

About this book

This book is for the CoreSight Embedded Trace Macrocell for the Cortex-M23 processor, the CoreSight ETM-M23 macrocell.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for:

- Designers of development tools providing support for ETM functionality. Implementation-specific behavior is described in this document. You can find complementary information in the *Embedded Trace Macrocell Architecture Specification* (ARM IHI 0014).
- Hardware and software engineers integrating the macrocell into an ASIC that includes a Cortex-M23 processor.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this chapter for an introduction to the functionality of the macrocell.

Chapter 2 *Functional Description*

Read this for a description of the interfaces, operation, clocking and resets of the macrocell.

Chapter 3 *Programmers Model*

Read this for a description of the programmers model for the macrocell.

Appendix A *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM® Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM® Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM® Glossary*, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page vii.

Typographical conventions

The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *ARM®v8-M Architecture Reference Manual* (ARM DDI 0553).
- *ARM® Cortex®-M23 Processor Technical Reference Manual* (ARM DDI 0550).
- *ARM® Embedded Trace Macrocell Architecture Specification* (ARM IHI 0014).
- *ARM® CoreSight™ Components Technical Reference Manual* (ARM DDI 0314).
- *ARM® CoreSight™ Architecture Specification v2.0* (ARM IHI 0029).
- *ARM® AMBA® 5 APB Protocol Specification Version: 2.0,* (ARM IHI 0024).

The following confidential books are only available to licensees:

- *ARM® Cortex®-M23 Processor Integration and Implementation Manual* (ARM DIT 0062).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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- The title.
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ARM also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the CoreSight *Embedded Trace Macrocell* (ETM) for the Cortex-M23 processor and its features. It contains the following sections:

1.1 About the ETM-M23

The CoreSight ETM-M23 is an optional debug component that enables a debugger to reconstruct program execution. The CoreSight ETM-M23 supports only instruction trace. You can use it either with the *Trace Port Interface Unit* (TPIU), or as part of a CoreSight system.

1.2 Compliance

ETM-M23 is compatible with the CoreSight architecture.

ETM-M23 implements version 3.5 of the ETM architecture, ETMv3.5. See the *Embedded Trace Macrocell Architecture Specification* for more information.

For more information about architectural compliance, see *Architecture and protocol information* on page 1-8.

1.3 Features

ETM-M23 provides:

- Tracing of 16-bit and 32-bit Thumb instructions.
- Four EmbeddedICE watchpoint inputs.
- A Trace Start/Stop block with EmbeddedICE inputs.
- One reduced functions counter.
- Two external inputs.
- A 24-byte FIFO queue.
- Global 48-bit timestamping.

See the *Embedded Trace Macrocell Architecture Specification* for information about:

- The trace protocol.
- Controlling tracing using triggering and filtering resources.

1.4 Interfaces

The system connections to the ETM-M23 are supported using a *Cross Trigger Interface* (CTI):

- 0-2 external inputs.
- Trigger output.

See *Configurable options* on page 1-6 and *Interfaces* on page 2-7 for more information about the external inputs and external outputs.

The bus interface for programming ETM registers is the APB interface.

1.5 Configurable options

The ETM-M23 macrocell includes the following configuration inputs:

- The maximum number of external inputs, see *External inputs* on page 2-5.
- Whether the system supports the FIFOFULL mechanism for stalling the processor, see Table 2-1 on page 2-3.

1.6 Test features

The ETM-M23 does not include any specific *Design For Test* (DFT) features.

1.7 Product documentation, design flow, and architecture

This section describes the ETM-M23 books, how they relate to the design flow, and the relevant architectural standards and protocols.

See *Additional reading* on page vii for more information about the books described in this section.

1.7.1 Documentation

The ETM-M23 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the ETM-M23. It is required at all stages of the design flow. Some behavior that is described in the TRM might not be relevant because of the way that the ETM-M23 is implemented and integrated.

1.7.2 Design flow

The ETM-M23 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following process:

1. Implementation. The implementer synthesizes the RTL, usually in combination with the processor, then places and routes the netlist to produce a hard macrocell.
2. Integration. The integrator instantiates the macrocell of the combined processor and ETM into a SoC. This includes testing its integration with the other SoC components to which it is connected.
3. Programming. The debug software developer programs the ETM and tests any trace software required for use with a SoC.

1.7.3 Architecture and protocol information

The ETM-M23 complies with, or implements, the specifications described in:

- *Trace macrocell*.
- *Advanced Microcontroller Bus Architecture*.

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

Trace macrocell

The ETM-M23 implements the ETM architecture version 3.5. See *Embedded Trace Macrocell Architecture Specification*.

Advanced Microcontroller Bus Architecture

This ETM-M23 complies with the *Advanced Microcontroller Bus Architecture* (AMBA) APB protocols.

See *ARM® AMBA® 5 APB Protocol Specification Version: 2.0*.

1.8 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

r0p1 There are no differences in functionality for this release.

Chapter 2
Functional Description

This chapter describes the interfaces, operation, clocking, and resets of the macrocell. It contains the following sections:

2.1 About the functions

Figure 2-1 shows a block diagram of the ETM, and shows how the ETM interfaces to the *Trace Port Interface Unit* (TPIU).

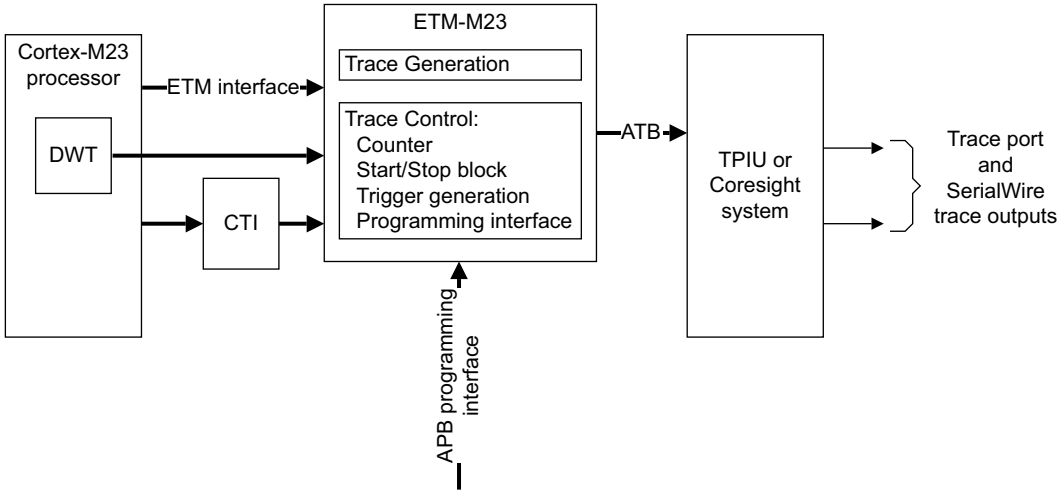

Figure 2-1 ETM block diagram

The ETM trace output is compatible with the *AMBA Trace Bus* (ATB) protocol, irrespective of the configuration of the trace port size and trace port mode within the ETM programmers model. The TPIU exports trace information from the processor. An implementation can replace the TPIU with other CoreSight trace components.

For more information, see:

- *ARM® Cortex®-M23 Processor Technical Reference Manual*.
- *Embedded Trace Macrocell Architecture Specification*.

The ETM provides a trace ID register for systems that use multiple trace sources. You must configure this register even if only a single trace source is in use.

The following sections provide information on features of the ETM:

- *Resources*.
- *Timestamp format* on page 2-5.
- *Periodic synchronization* on page 2-5.
- *Data and instruction address compare resources* on page 2-5.
- *External inputs* on page 2-5.
- *Start/stop block* on page 2-5.
- *Triggering* on page 2-6.

2.1.1 Resources

Because the ETM does not generate data trace information, the lower bandwidth reduces the requirement for complex triggering capabilities. This means that the ETM only includes a small subset of the possible resources permitted by the ETM architecture.

Table 2-1 lists the Cortex-M23 processor resources.

Table 2-1 Cortex-M23 processor resources

Feature	Present on ETM-M23
Architecture version	ETMv3.5
Address comparator pairs	0
Data comparators	0
Context ID comparators	0
Memory Map Decoders (MMDs)	0
Counters	1, reduced function counter only
Sequencer	No
Start/stop block	Yes
EmbeddedICE comparators	4
External inputs	2
External outputs	0
Extended external inputs	0
Extended external input selectors	0
FIFOFULL	Yes
FIFOFULL level setting	Yes
Branch broadcasting	Yes
ASIC Control Register	No
Data suppression	No
Software access to registers	Yes
Readable registers	Yes
FIFO size	24 bytes
Minimum ATB port size	8 bits
Maximum ATB port size	8 bits
Normal port mode	-
Normal half-rate clocking, 1:1	Yes - asynchronous
Demultiplexor port mode	-
Demultiplexor half-rate clocking, 1:2	No
Multiplexor port mode, 2:1	No
1:4 port mode	No
Dynamic port mode, including stalling	No. Supported by asynchronous port mode.
Coprocessor Register Transfer (CPRT) data	No

Table 2-1 Cortex-M23 processor resources (continued)

Feature	Present on ETM-M23
Load PC first	No
Fetch comparisons	No
Load data traced	No

Resource identification encoding

You configure the trace enable event, timestamp event, and trigger event using the same mechanism. For each event, a 17-bit register is used to define the event. This register provides:

- Resource A, bits[6:0].
- Resource B, bits[13:7].
- A boolean function, bits[16:14].

Table 2-2 shows the encodings that are used for the boolean function.

Table 2-2 Boolean function encoding for events

Encoding	Function
0b000	A
0b001	NOT(A)
0b010	A AND B
0b011	NOT(A) AND B
0b100	NOT(A) AND NOT (B)
0b101	A OR B
0b110	NOT (A) OR B
0b111	NOT (A) OR NOT (B)

Table 2-3 shows the encodings that are used for Resource identification.

Table 2-3 Resource identification encoding

Resource type[a]	Index range[b]	Description of resource type
0b010	0-3	DWT Comparator inputs (0-3)
0b100	0	Counter 1 at zero
0b101	15	Trace Start/Stop resource
0b110	0-1	ExtIn (0-1)
0b110	15	HardWired (always True)

a. For Resource A, bits[6:4]. For Resource B, bits[13:11].
b. For Resource A, bits[3:0]. For Resource B, bits[10:7].

2.1.2 Timestamp format

Timestamps are encoded as 48-bit binary numbers. A system implementation can provide a timestamp count that can be used by several trace sources as an aid to correlating the trace streams.

2.1.3 Periodic synchronization

The ETM uses a fixed synchronization packet generation frequency of every 1024 bytes of trace.

2.1.4 Data and instruction address compare resources

The DWT provides four address comparators on the data bus that provide debug functionality. Within the DWT unit, you can specify the functions triggered by a match, and one of these functions is to generate an ETM match input. These inputs are presented to the ETM as embedded *In Circuit Emulator* (ICE) comparator inputs.

A single DWT resource can trigger an ETM event and also generate instrumentation trace directly from the same event.

You can configure the four DWT comparators individually to compare with the address of the current executing instruction to permit the ETM access to an instruction address compare resource. These inputs are presented to the ETM as EmbeddedICE comparator inputs. The DWT provides either one or four comparators, depending on the implementation of the processor.

Note

Using a DWT comparator as an instruction address comparator reduces the number of available data address comparisons.

See the *ARM® Cortex®-M23 Processor Technical Reference Manual* for more information about the DWT unit.

2.1.5 External inputs

Two external inputs, **ETMEXTIN[1:0]**, enable additional components to generate trigger and enable signals for the ETM.

2.1.6 Start/stop block

The start/stop block provides a single-bit resource that can be used as an input to other parts of the resource logic, including the trace enable logic. The start/stop block can only be controlled by using the embeddedICE inputs to the ETM. The DWT controls these inputs.

The start/stop block is set to the start state if any of the EmbeddedICE watchpoint inputs selected as start resources in ETMTESSEICR go HIGH. The start/stop block is set to the stop state if any of the EmbeddedICE watchpoint inputs selected as stop resources in ETMTESSEICR go LOW.

If bit[25] of ETMTECR1 is 1, tracing is only enabled when the start/stop block is in the start state.

Tracing is also only enabled when the result of evaluating the Trace Enable Event is TRUE. This event can be set to always be TRUE by programming a value of `0x6F` to ETMTEEVR. For more information, see the *Embedded Trace Macrocell Architecture Specification*.

2.1.7 Triggering

The ETM provides a trigger resource that can be used to identify a point within a trace run. The generation of a trigger does not affect the tracing in any way, but the trigger is output in the trace stream, and can also be passed to other trace components or used to halt the processor. An external Trace Port Analyzer can use the trigger to determine when to start and stop capture of trace.

2.2 Interfaces

The ETM-M23 has the following external interfaces:

ATB A 32-bit ATB provides trace output from the macrocell. See the *ARM® AMBA® 4 ATB Protocol Specification* for more information about this interface.

APB An APB provides the control interface for the macrocell. See the *ARM® AMBA® 4 APB Protocol Specification* for more information about this interface.

CTI Your implementation can provide a *Cross Trigger Interface* to manage the interconnection of trigger and control signals between the processor core, ETM, and TPIU.

2.3 Clocking and resets

The following sections describe the ETM-M23 clocks and resets:

- *ETM-M23 clock*.
- *ETM-M23 low-power control*.
- *ETM-M23 reset*.
- *Power domain*.

2.3.1 ETM-M23 clock

The ETM-M23 has one clock, **CLK**. This clock is synchronous to the **FCLK** input of the Cortex-M23 processor.

2.3.2 ETM-M23 low-power control

The ETM-M23 has outputs to indicate whether the debugger expects power to be maintained, and also an output to indicate when tracing is inactive. The use of these signals is IMPLEMENTATION SPECIFIC.

2.3.3 ETM-M23 reset

The ETM-M23 has a single reset, **nDBGETMRESET**, and must only be reset by a debug reset event.

Note

The programming state must be reconfigured after a debug reset.

2.3.4 Power domain

The ETM-M23 is in the Debug power domain. The Debug power domain cannot be turned on if the system power domain is off.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About the programmers model

This chapter describes the mechanisms for programming the registers that are used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

3.2 Modes of operation and execution

ETM-M23 implements ETMv3.5 for tracing 16-bit and 32-bit Thumb® instructions.

The *Embedded Trace Macrocell Architecture Specification* describes the features of ETMv3.5.

See *Features* on page 1-4 for information on the trace features of the ETM-M23.

When the ETM is powered up or reset, you must program all the registers that do not have an architecturally defined reset state before you enable tracing. If you do not do so, the trace results are UNPREDICTABLE.

When programming the ETM registers, you must enable all changes at the same time. To enable all changes, use the Programming bit in ETMCR. See *Main Control Register, ETMCR* on page 3-6.

When the Programming bit is set to 0 you must not write to registers other than ETMCR, because doing so can lead to UNPREDICTABLE behavior.

When setting the Programming bit, you must not change any other bits of ETMCR. You must only change the value of bits other than the Programming bit of ETMCR when bit[1] of ETMSR is set to 1. ARM recommends that you use a read-modify-write procedure when changing ETMCR.

When authentication is not enabled, ETM-M23 behaves as follows:

- If non-invasive debug is not enabled, the ETM does not trace anything.
- If non-invasive secure debug is not enabled, the ETM traces Non-secure code, but when secure code is executed it is not visible.

3.3 Register summary

This section describes the ETM registers. Table 3-1 provides cross-references to individual registers.

Table 3-1 ETM registers

Address	Name	Reset	Type	Description
0xE0041000	ETMCR	0x00000411	RW	*Main Control Register, ETMCR* on page 3-6
0xE0041004	ETMCCR	0x80842000	RO	*Configuration Code Register, ETMCCR* on page 3-8
0xE0041008	ETMTRIGGER	UNKNOWN	RW	Trigger Event Register
0xE0041010	ETMSR	UNKNOWN	RW	ETM Status Register
0xE0041014	ETMSCR	0x00020D09	RO	*System Configuration Register, ETMSCR* on page 3-9
0xE0041020	ETMTEEVR	UNKNOWN	RW	TraceEnable Event Register
0xE0041024	ETMTECR1	UNKNOWN	RW	*TraceEnable Control 1 Register, ETMTECR1* on page 3-10
0xE0041028	ETMFFLR	UNKNOWN	RW	FIFOFULL Level Register
0xE0041140	ETMCNTRLDVR1	UNKNOWN	RW	Free-running counter reload value
0xE00411E0	ETMSYNCFR	0x00000400	RO	Synchronization Frequency Register
0xE00411E4	ETMIDR	0x4114F250	RO	*ID Register, ETMIDR* on page 3-11
0xE00411E8	ETMCCER	0x18541800	RO	*Configuration Code Extension Register, ETMCCER* on page 3-12
0xE00411F0	ETMTESSEICR	UNKNOWN	RW	*TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR* on page 3-13
0xE00411F8	ETMTSEVR	UNKNOWN	RW	Timestamp Event Register
0xE0041200	ETMTRACEIDR	0x00000000	RW	CoreSight Trace ID Register
0xE0041208	ETMIDR2	0x00000000	RO	ETM ID Register 2
0xE0041314	ETMPDSR	0x00000001	RO	*Device Power-Down Status Register, ETMPDSR* on page 3-14
0xE0041EE0	ITMISCIN	UNKNOWN	RO	*Integration Test Miscellaneous Inputs, ITMISCIN* on page 3-14
0xE0041EE8	ITTRIGOUT	UNKNOWN	WO	*Integration Test Trigger Out, ITTRIGOUT* on page 3-15
0xE0041EF0	ETM_ITATBCTR2	UNKNOWN	RO	*ETM Integration Test ATB Control 2, ETM_ITATBCTR2* on page 3-16
0xE0041EF8	ETM_ITATBCTR0	UNKNOWN	WO	*ETM Integration Test ATB Control 0, ETM_ITATBCTR0* on page 3-16
0xE0041F00	ETMITCTRL	0x00000000	RW	Integration Mode Control Register
0xE0041FA0	ETMCLAIMSET	UNKNOWN	RW	Claim Tag Set Register
0xE0041FA4	ETMCLAIMCLR	UNKNOWN	RW	Claim Tag Clear Register
0xE0041FB0	ETMLAR	UNKNOWN	RW	Lock Access Register
0xE0041FB4	ETMLSR	UNKNOWN	RO	Lock Status Register
0xE0041FB8	ETMAUTHSTATUS	UNKNOWN	RO	Authentication Status Register
0xE0041FCC	ETMDEVTYPE	0x00000013	RO	CoreSight Device Type Register

Table 3-1 ETM registers (continued)

Address	Name	Reset	Type	Description
0xE0041FD0	ETMPIDR4	0x00000004	RO	Peripheral Identification Registers
0xE0041FD4	ETMPIDR5	0x00000000	RO	
0xE0041FD8	ETMPIDR6	0x00000000	RO	
0xE0041FDC	ETMPIDR7	0x00000000	RO	
0xE0041FE0	ETMPIDR0	0x00000020	RO	
0xE0041FE4	ETMPIDR1	0x000000BD	RO	
0xE0041FE8	ETMPIDR2[a]	0x0000000B	RO	
0xE0041FEC	ETMPIDR3	0x00000000	RO	
0xE0041FF0	ETMCIDR0	0x0000000D	RO	Component Identification Registers
0xE0041FF4	ETMCIDR1	0x00000090	RO	
0xE0041FF8	ETMCIDR2	0x00000005	RO	
0xE0041FFC	ETMCIDR3	0x000000B1	RO	

a. Bits[7:4] are 0x1.

For more information on the ETM registers, see the *ARM® Embedded Trace Macrocell Architecture Specification*.

3.4 Register descriptions

The following sections describe registers which have an implementation that is specific to this product. Other registers are described in the *Embedded Trace Macrocell Architecture Specification*.

3.4.1 Main Control Register, ETMCR

The ETMCR characteristics are:

Purpose Controls general operation of the ETM, such as whether tracing is enabled.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the ETM register summary in Table 3-1 on page 3-4.

Figure 3-1 shows the ETMCR bit assignments.

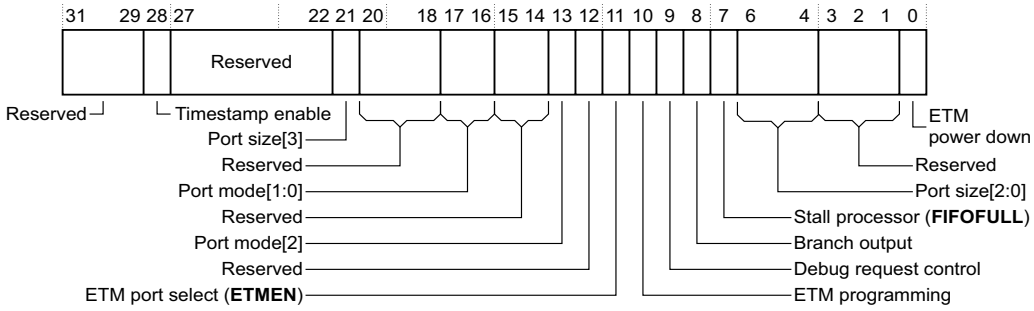

Figure 3-1 ETMCR bit assignments

Table 3-2 shows the ETMCR bit assignments.

Table 3-2 ETMCR bit assignments

Bits	Name	Function
[31:29]	-	Reserved, Read As Zero.
[28]	Timestamp enable	When set, this bit enables timestamping. An ETM reset sets this bit to 0.
[27:22]	-	Reserved, Read As Zero.
[21]	Port size[3]	This bit is implemented but has no function. An ETM reset sets this bit to 0.
[20:18]	-	Reserved.
[17:16]	Port mode[1:0]	These bits are implemented but have no function. An ETM reset sets these bits to 0.
[15:14]	-	Reserved.
[13]	Port mode[2]	This bit is implemented but has no function. An ETM reset sets this bit to 0.

Table 3-2 ETMCR bit assignments (continued)

Bits	Name	Function
[12]	-	Reserved.
[11]	ETM port select	This bit can be used to control other trace components in an implementation. The possible values are: **0** **ETMEN** is LOW. **1** **ETMEN** is HIGH. This bit must be set by the trace software tools to ensure that trace output is enabled from this ETM. An ETM reset sets this bit to 0.
[10]	ETM programming	This bit must be set to 1 at the start of the ETM programming sequence. Tracing is prevented while this bit is set to 1. An ETM reset sets this bit to `0b1`.
[9]	Debug request control	When set to 1 and the trigger event occurs, the **ETMDBGRQ** output is asserted until **HALTED** is observed. This enables the ARM processor to be forced into Debug state. An ETM reset sets this bit to 0.
[8]	Branch output	When set to 1, all branch addresses are output, even if the branch was because of a direct branch instruction. Setting this bit enables reconstruction of the program flow without having access to the memory image of the code being executed. When this bit is set to 1, more trace data is generated, and this can affect the performance of the trace system. Information about the execution of a branch is traced regardless of the state of this bit. An ETM reset sets this bit to 0.
[7]	Stall processor	The **FIFOFULL** output can be used to stall the processor to prevent overflow. The **FIFOFULL** output is only enabled when the stall processor bit is set to 1. When the bit is 0, the **FIFOFULL** output always remains LOW and the FIFO overflows if there are too many trace packets. If overflow does occur, trace resumes without corruption when the FIFO has drained. An ETM reset sets this bit to 0. For information about the interaction of this bit with the ETMFFLR register, see the *Embedded Trace Macrocell Architecture Specification*.
[6:4]	Port size[2:0]	The ETM-M23 has no influence over the external pins that are used for trace. These bits are implemented but not used. An ETM reset sets these bits to `0b001`.
[3:1]	-	Reserved.
[0]	ETM power down	This bit can be used by an implementation to control if the ETM is in a low-power state. This bit must be cleared by the trace software tools at the beginning of a debug session. When this bit is set to 1, writes to some registers and fields might be ignored. You can always write to the following registers and fields: • ETMCR bit[0]. • ETMLAR. • ETMCLAIMSET register. • ETMCLAIMCLR register. When the ETMCR is written with this bit set to 1, bits other than bit[0] might be ignored. An ETM reset sets this bit to 1.

3.4.2 Configuration Code Register, ETMCCR

The ETM Configuration Code Register characteristics are:

Purpose Enables software to read the implementation-specific configuration of the ETM.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the ETM register summary in Table 3-1 on page 3-4.

Figure 3-2 shows the ETMCCR bit assignments.

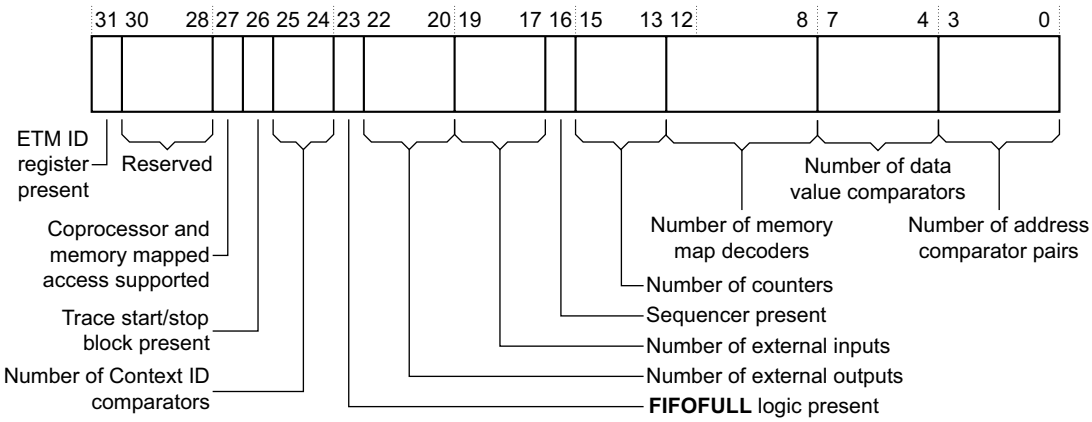

Figure 3-2 ETMCCR bit assignments

Table 3-3 shows the ETMCCR bit assignments.

Table 3-3 ETMCCR bit assignments

Bits	Name	Function
[31]	ETM ID register present	The value of this bit is 1, indicating that the ETMIDR, register `0x79`, is present and defines the ETM architecture version in use.
[30:28]	-	Reserved.
[27]	Coprocessor and memory access	The value of this bit is 1, indicating that memory-mapped access to registers is supported.
[26]	Trace start/stop block present	The value of this bit is 1, indicating that the Trace start/stop block is present.
[25:24]	Number of Context ID comparators	The value of these bits is `0b00`, indicating that Context ID comparators are not implemented.
[23]	**FIFOFULL** logic present	The value of this bit is 1, indicating that **FIFOFULL** logic is present in the ETM. To use FIFOFULL the system must also support the function, as indicated by bit[8] of ETMSCR, see *System Configuration Register, ETMSCR* on page 3-9.
[22:20]	Number of external outputs	The value of these bits is `0b000`, indicating that no external outputs are supported.
[19:17]	Number of external inputs	The value of these bits is between `0b000` and `0b010`, indicating the number of external inputs, from 0-2, implemented in the system.
[16]	Sequencer present	The value of this bit is 0, indicating that the sequencer is not implemented.

Table 3-3 ETMCCR bit assignments (continued)

Bits	Name	Function
[15:13]	Number of counters	The value of these bits is `0b001`, indicating that one counter is implemented.
[12:8]	Number of memory map decoders	The value of these bits is `0b00000`, indicating that memory map decoder inputs are not implemented.
[7:4]	Number of data value comparators	The value of these bits is `0b0000`, indicating that data value comparators are not implemented.
[3:0]	Number of address comparator pairs	The value of these bits is `0b0000`, indicating that address comparator pairs are not implemented.

3.4.3 System Configuration Register, ETMSCR

The ETMSCR characteristics are:

Purpose Shows the ETM features supported by the implementation of the ETM macrocell.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-3 shows the ETMSCR bit assignments.

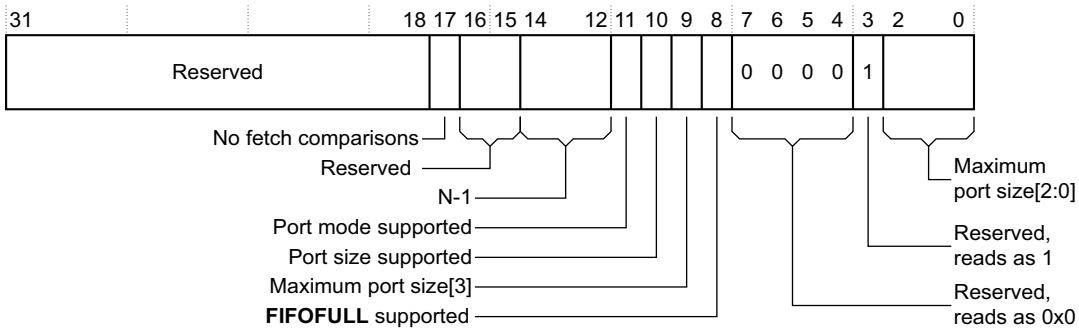

Figure 3-3 ETMSCR bit assignments

Table 3-4 shows the ETMSCR bit assignments.

Table 3-4 ETMSCR bit assignments

Bits	Name	Function
[31:18]	-	Reserved.
[17]	No Fetch comparisons	The value of this bit is 1, indicating that fetch comparisons are not implemented.
[16:15]	-	Reserved.
[14:12]	N-1	These bits indicate the number of supported processors, N, minus 1. The value of these bits is `0b000`, indicating that there is only one processor connected.
[11]	Port mode supported	This bit reads as 1 if the currently selected port mode is supported. This has no effect on the TPIU trace port.

Table 3-4 ETMSCR bit assignments (continued)

Bits	Name	Function
[10]	Port size supported	This bit reads as 1 if the currently selected port size is supported. This has no effect on the TPIU trace port.
[9]	Maximum port size[3]	Maximum ETM port size bit[3]. This bit is used with bits[2:0]. Its value is 0. This has no effect on the TPIU trace port.
[8]	**FIFOFULL** supported	The value of this bit is 1, indicating that **FIFOFULL** is supported. This bit is used with bit[23] of the ETMCCR.
[7:4]	-	Reserved, Read As Zero.
[3]	-	Reserved, Read As One.
[2:0]	Maximum port size[2:0]	Maximum ETM port size bits[2:0]. These bits are used with bit[9]. The value of these bits is `0b001`.

3.4.4 TraceEnable Control 1 Register, ETMTECR1

The ETMTECR1 characteristics are:

Purpose Enables the start/stop logic that is used for trace enable.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-4 shows the ETMTECR1 bit assignments.

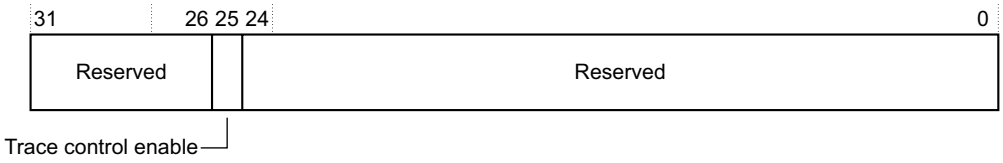

Figure 3-4 ETMTECR1 bit assignments

Table 3-5 shows the ETMTECR1 bit assignments.

Table 3-5 ETMTECR1 bit assignments

Bits	Name	Function
[31:26]	-	Reserved.
[25]	Trace control enable	Trace start/stop enable. The possible values of this bit are: **0** Tracing is unaffected by the trace start/stop logic. **1** Tracing is controlled by the trace on and off addresses that are configured for the trace start/stop logic. The trace start/stop resource, resource `0x5F`, is unaffected by the value of this bit.
[24:0]	-	Reserved.

3.4.5 ID Register, ETMIDR

The ETMIDR characteristics are:

Purpose Holds the ETM architecture variant, and defines the programmers model for the ETM.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-5 shows the ETMIDR bit assignments.

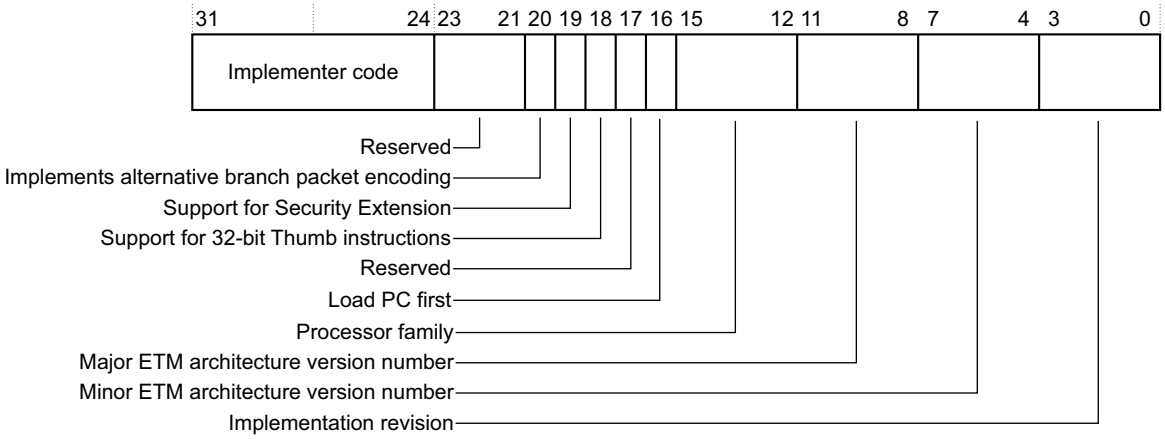

Figure 3-5 ETMIDR bit assignments

Table 3-6 shows the ETMIDR bit assignments.

Table 3-6 ETMIDR bit assignments

Bits	Name	Function
[31:24]	Implementer code	These bits identify ARM as the implementer of the processor. The value of these bits is `0b1000001`.
[23:21]	-	Reserved.
[20]	Branch packet encoding	The value of this bit is 1, indicating that alternative branch packet encoding is implemented.
[19]	Security Extension support	The value of this bit is 0, indicating that the ETM behaves as if the processor is in Secure state always.
[18]	32-bit Thumb instruction tracing	The value of this bit is 1, indicating that a 32-bit Thumb instruction is traced as a single instruction.
[17]	-	Reserved.
[16]	Load PC first	The value of this bit is 0, indicating that data tracing is not supported.
[15:12]	Processor family	The value of these bits is `0b1111`, indicating that the processor family is not identified in this register.

Table 3-6 ETMIDR bit assignments (continued)

Bits	Name	Function
[11:8]	Major ETM architecture version	The value of these bits is `0b0010`, indicating major architecture version number 3, ETMv3.
[7:4]	Minor ETM architecture version	The value of these bits is `0b0101`, indicating minor architecture version number 5.
[3:0]	Implementation revision	The value of these bits is `0b0001`, indicating implementation revision, 1.

3.4.6 Configuration Code Extension Register, ETMCCER

The ETMCCER characteristics are:

Purpose Holds ETM configuration information in addition to that in the ETMCCR. See *Configuration Code Register, ETMCCR* on page 3-8.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-6 shows the ETMCCER bit assignments.

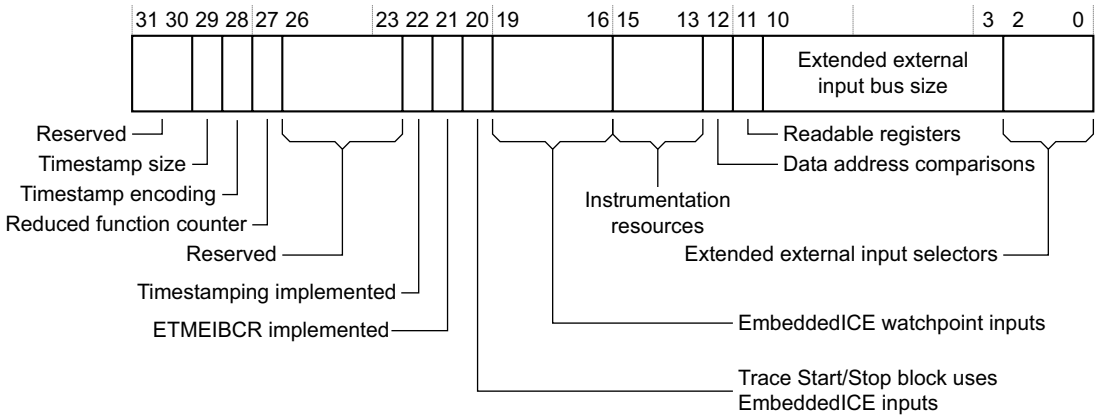

Figure 3-6 ETMCCER bit assignments

Table 3-7 shows the ETMCCER bit assignments.

Table 3-7 ETMCCER bit assignments

Bits	Name	Function
[31:30]	-	Reserved, Read As Zero.
[29]	Timestamp size	Set to 0 to indicate a size of 48 bits.
[28]	Timestamp encoding	Set to 1 to indicate that the timestamp is encoded as a natural binary number.
[27]	Reduced function counter	Set to 1 to indicate that Counter 1 is a reduced function counter.
[26:23]	-	Reserved, Read As Zero.
[22]	Timestamping implemented	This bit is set to 1, indicating that timestamping is implemented.

Table 3-7 ETMCCER bit assignments (continued)

Bits	Name	Function
[21]	EmbeddedICE behavior control implemented	The value of this bit is 0, indicating that the ETMEIBCR is not implemented. For more information on EmbeddedICE behavior, see the *Embedded Trace Macrocell Architecture Specification*.
[20]	Trace Start/Stop block uses EmbeddedICE watchpoint inputs	The value of this bit is 1, indicating that the Trace Start/Stop block uses the EmbeddedICE watchpoint inputs.
[19:16]	EmbeddedICE watchpoint inputs	The value of these bits is `0b0100`, indicating that the number of EmbeddedICE watchpoint inputs that are implemented is four. These inputs come from the DWT.
[15:13]	Instrumentation resources	The value of these bits is `0b000`, indicating that no Instrumentation resources are supported.
[12]	Data address comparisons	The value of this bit is 1, indicating that data address comparisons are not supported.
[11]	Readable registers	The value of this bit is 1, indicating that all registers are readable.
[10:3]	Extended external input bus size	The value of these bits is 0, indicating that the extended external input bus is not implemented.
[2:0]	Extended external input selectors	The value of these bits is 0, indicating that extended external input selectors are not implemented.

3.4.7 TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR

The ETMTESSEICR characteristics are:

Purpose Specifies the EmbeddedICE watchpoint comparator inputs that are used to control the start/stop resource.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-7 shows the ETMTESSEICR bit assignments.

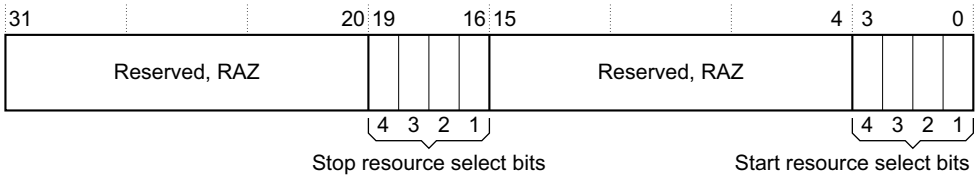

Figure 3-7 ETMTESSEICR bit assignments

Table 3-8 shows the ETMTESSEICR bit assignments.

Table 3-8 ETMTESSEICR bit assignments

Bits	Name	Function
[31:20]	-	Reserved, Read As Zero.
[19:16]	Stop resource select	Setting any of these bits to 1 selects the corresponding EmbeddedICE watchpoint input as a **TraceEnable** stop resource. Bit[16] corresponds to input 1, bit[17] corresponds to input 2, bit[18] corresponds to input 3, and bit[19] corresponds to input 4.
[15:4]	-	Reserved, Read As Zero.
[3:0]	Start resource select	Setting any of these bits to 1 selects the corresponding EmbeddedICE watchpoint input as a **TraceEnable** start resource. Bit[0] corresponds to input 1, bit[1] corresponds to input 2, bit[2] corresponds to input 3, and bit[3] corresponds to input 4.

3.4.8 Device Power-Down Status Register, ETMPDSR

The ETMPDSR characteristics are:

Purpose Indicates the powerdown status of the ETM.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use an ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-8 shows the ETMPDSR bit assignments.

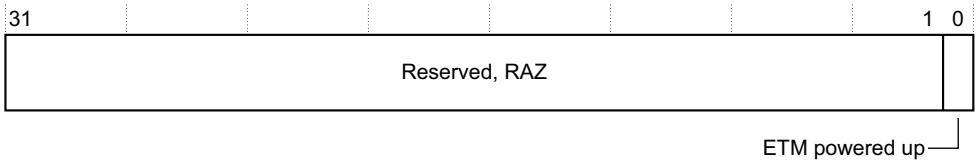

Figure 3-8 ETMPDSR bit assignments

Table 3-9 shows the ETMPDSR bit assignments.

Table 3-9 ETMPDSR bit assignments

Bits	Name	Function
[31:1]	-	Reserved, Read As Zero.
[0]	ETM powered up	The value of this bit indicates whether you can access the ETM Trace Registers. The value of this bit is always 1, indicating that the ETM Trace Registers can be accessed.

3.4.9 Integration Test Miscellaneous Inputs, ITMISCIN

The ITMISCIN characteristics are:

Purpose Integration test.

Usage constraints There are no usage constraints.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-9 shows the ITMISCIN bit assignments.

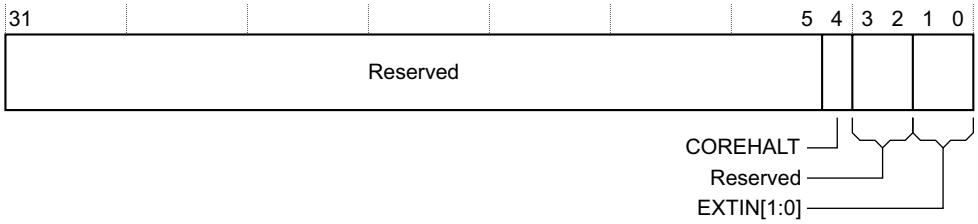

Figure 3-9 ITMISCIN bit assignments

Table 3-10 shows the ITMISCIN bit assignments.

Table 3-10 ITMISCIN bit assignments

Bits	Name	Function
[31:5]	-	Reserved.
[4]	COREHALT	A read of this bit returns the value of the **COREHALT** input pin.
[3:2]	-	Reserved.
[1:0]	EXTIN[1:0]	A read of these bits returns the value of the **EXTIN[1:0]** input pins.

3.4.10 Integration Test Trigger Out, ITTRIGOUT

The ITMISCIN characteristics are:

Purpose Integration test.

Usage constraints You must set bit[0] of ETMITCTRL to use this register.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-10 shows the ITTRIGOUT bit assignments.

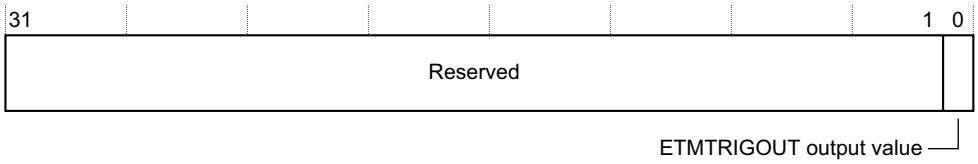

Figure 3-10 ITTRIGOUT bit assignments

Table 3-11 shows the ITTRIGOUT bit assignments.

Table 3-11 ITTRIGOUT bit assignments

Bits	Name	Function
[31:1]	-	Reserved.
[0]	TRIGGER output value	A write to this bit sets the ETMTRIGOUT output.

3.4.11 ETM Integration Test ATB Control 2, ETM_ITATBCTR2

The ETM_ITATBCTR2 characteristics are:

Purpose Integration test.

Usage constraints You must set bit[0] of ETMITCTRL to use this register.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-11 shows the ETM_ITATBCTR2 bit assignments.

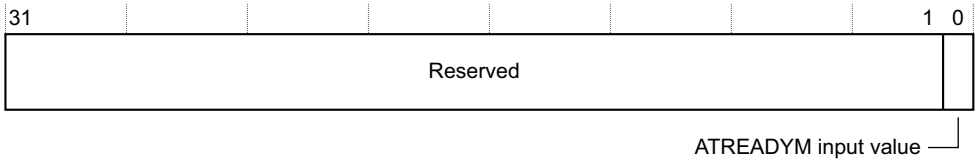

Figure 3-11 ETM_ITATBCTR2 bit assignments

Table 3-12 shows the ETM_ITATBCTR2 bit assignments.

Table 3-12 ETM_ITATBCTR2 bit assignments

Bits	Name	Function
[31:1]	-	Reserved.
[0]	ATREADYM input value	A read of this bit returns the value of the ETM ATREADYM input.

3.4.12 ETM Integration Test ATB Control 0, ETM_ITATBCTR0

The ETM_ITATBCTR0 characteristics are:

Purpose Integration test.

Usage constraints You must set bit[0] of ETMITCTRL to use this register.

Configurations This register is only available if the processor is configured to use the ETM.

Attributes See the register summary in Table 3-1 on page 3-4.

Figure 3-12 shows the ETM_ITATBCTR0 bit assignments.

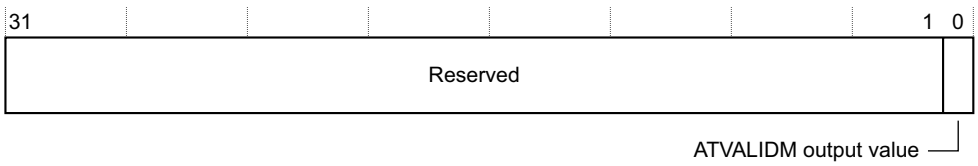

Figure 3-12 ETM_ITATBCTR0 bit assignments

Table 3-13 shows the ETM_ITATBCTR0 bit assignments.

Table 3-13 ETM_ITATBCTR0 bit assignments

Bits	Name	Function
[31:1]	-	Reserved.
[0]	ATVALIDM output value	A write to this bit sets the value of the ETM ATVALIDM output.

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue A

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue A and issue B

Change	Location	Affects
Updated the ETMIDR register	*ID Register, ETMIDR* on page 3-11	r0p1
Removed the Signal Descriptions Appendix	-	r0p1

Table A-3 Differences between issue B and issue C

Change	Location	Affects
Changed product name to Cortex-M23	-	r0p1
Added the timestamp input width	*Features* on page 1-4	r0p1