ARM® CoreSight™ ETM-M7

Revision: r0p1

Technical Reference Manual

ARM®

ARM DDI 0494D (ID082615)

ARM CoreSight ETM-M7
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
25 April 2014	A	Confidential	First release for r0p0
05 December 2014	B	Non-Confidential	First release for r0p1
19 March 2015	C	Non-Confidential	Second release for r0p1
06 July 2015	D	Confidential Draft	Third release for r0p1

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Product Status

The information in this document is final, that is for a developed product.

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Preface

This preface introduces the *ARM® CoreSight™ ETM-M7 Technical Reference Manual*. It contains the following sections:

About this book

This book is for the Embedded Trace Macrocell for the Cortex-M7 processor (ETM-M7).

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for:

- Designers of development tools providing support for ETM functionality. Implementation-specific behavior is described in this document. You can find complementary information in the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*.
- Hardware and software engineers integrating the macrocell into an ASIC that includes a Cortex-M7 processor. You can find complementary information in the *ARM® Cortex®-M7 Integration and Implementation Manual*.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the functionality of the macrocell.

Chapter 2 *Functional Description*

Read this for a description of the interfaces, operation, clocking and resets of the macrocell.

Chapter 3 *Programmers Model*

Read this for a description of the programmers model for the macrocell.

Appendix A *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM® Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM® Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM® Glossary,* http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page viii.
- *Timing diagrams* on page viii.
- *Signals* on page ix.

Typographical conventions

The following table describes the typographical conventions:

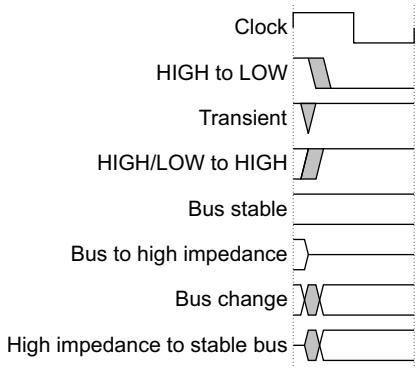
Typographical conventions

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are UNDEFINED, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See *Infocenter*, http://infocenter.arm.com, for access to ARM documentation.

See *on ARM*, www.arm.com/cmsis, for embedded software development resources including the *Cortex® Microcontroller Software Interface Standard* (CMSIS).

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:
- *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* (ARM IHI 0064).
- *ARM® Cortex®-M7 Technical Reference Manual* (ARM DD I0489).
- *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480).
- *ARM® CoreSight™ SoC-400 User Guide* (ARM DUI 0563).
- *ARM® CoreSight™ Technology System Design Guide* (ARM DGI 0016).
- *ARM® AMBA® 3 APB Protocol Specification* (ARM IHI 0024).
- *ARM® AMBA® 3 ATB Protocol Specification* (ARM IHI 0032).

The following confidential books are only available to licensees:
- *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029).
- *ARM® Cortex®-M7 Integration and Implementation Manual* (ARM DIT 0034).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, ARM DDI 0494D.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the CoreSight ETM-M7. It contains the following sections:

1.1 About the CoreSight ETM-M7

Depending on your implementation, the CoreSight ETM-M7 provides non-intrusive program-flow trace and data trace capabilities for the Cortex-M7 processor. The ETM-M7 generates information that trace software tools use to reconstruct the execution of all or part of a program.

The ETM-M7 implementation options are:

- Full instruction and data trace.
- Instruction trace only.

For full reconstruction of program execution, the ETM-M7 is able to trace:

- All instructions, including condition code pass/fail.
- Load/store address and data values.
- Target addresses of taken direct and indirect branch operations.
- Exceptions.
- Entry to and return from debug state when Halting debug-mode is enabled.
- Cycle counts relating to instruction execution.

For instruction trace only, the ETM-M7 is able to trace:

- All instructions, including condition code pass/fail.
- Target addresses of taken direct and indirect branch operations.
- Exceptions.
- Entry to and return from debug state when Halting debug-mode is enabled.
- Cycle counts relating to instruction execution.

The ETM-M7 contains *resource* logic that enables you to control both instruction trace and data trace, depending on your configuration. Resource logic includes address comparators and data value comparators, counters, and a sequencer. You specify the exact set of trigger and filter conditions required for a particular application.

The ETM-M7 is a CoreSight component. For more information about CoreSight, see the *ARM® CoreSight™ Architecture Specification* and *ARM® CoreSight™ Technology System Design Guide*. For more information about the ETM architecture, see the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*.

1.1.1 The CoreSight debug environment

The ETM-M7 is designed for use with CoreSight, an extensible, system-wide debug and trace architecture from ARM. See the *ARM® CoreSight™ SoC-400 User Guide* for more information about how to test the integration of the ETM-M7 in a full CoreSight system.

A software debugger provides a user interface to the ETM-M7. You can use this interface to:

- Configure ETM-M7 facilities such as filtering.
- Configure optional trace features such as cycle-accurate tracing.
- Configure the other CoreSight components such as the *Trace Port Interface Unit* (TPIU).
- Access the processor debug and performance monitor units.

The ETM-M7 outputs its trace to the AMBA 3 *Advanced Trace Bus* (ATB) interfaces. If the ETM-M7 is configured for instruction trace only, it has a single ATB interface. If the ETM-M7 is configured for instruction and data trace, it has two ATB interfaces, and two trace streams are generated. If data trace is not enabled, the data trace stream on the data ATB interface is not used. Each trace stream can be buffered and captured independently because they contain the synchronization information that is required to decompress the data trace.

You can use the CoreSight infrastructure to design systems that provide the following options:

- Export the trace information through a trace port. An external *Trace Port Analyzer* (TPA) captures the trace information as Figure 1-1 shows.
- Write the trace information to a trace-capable device that can access local or system memory. You can read out the trace at low speed using a JTAG or Serial Wire interface.

The debugger has a copy of the executed image from memory and the captured trace information from the TPA or on-chip trace buffer. It decompresses the image to provide full disassembly, with symbols, of the code that was executed. The trace information generated by the ETM-M7 gives the debugger the capability to link this data back to the original high-level source code, to provide a visualization of how the code was executed on the Cortex-M7 processor.

Figure 1-1 shows an example of how the ETM-M7 fits into a CoreSight debug environment to provide full trace capabilities in a single processor system. In this example, the external debug software configures the trace and debug components through the *Debug Access Port* (DAP). The top level ROM table contains a unique identification code for the SoC and the base addresses of the components connected to the External PPB. The ETM-M7 trace interfaces are replicated to provide on-chip storage using the CoreSight ETB or output off-chip using the TPIU. Cross-triggering operates through the *Cross Trigger Interface* (CTI) and *Cross Trigger Matrix* (CTM) components.

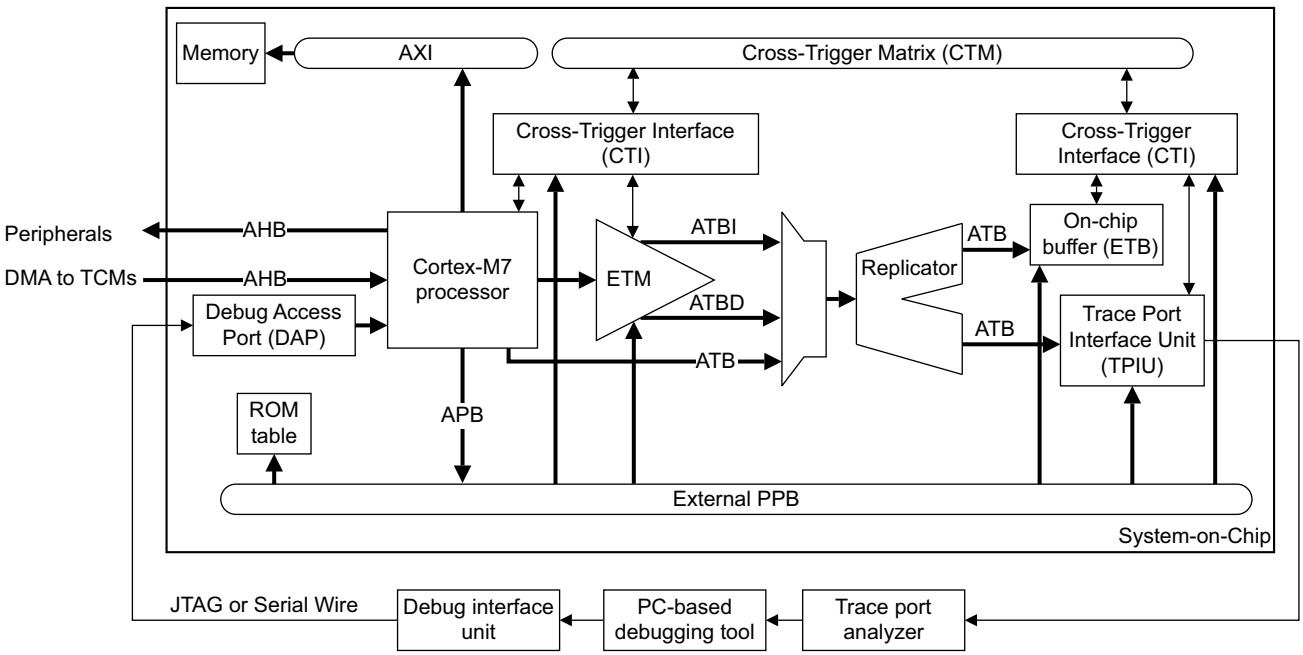


Figure 1-1 ETM-M7 system diagram

Note

In Figure 1-1, the arrows on the thick lines show the transaction direction on buses, from master to slave port. Each bus contains individual signals that go from master to slave and other signals that go from slave to master.

The ETM has a external trace multiplex control bus, **PROCSEL**, that the system can use to share the ETM amongst up to four instances of the Cortex-M7 processor. This can only be used in the full instruction and data configuration.

As an alternative to using an external computer to run a software debugger, the Cortex-M7 processor (or another processor on the SoC) can access the ETM-M7 and on chip trace buffer to provide self-hosted debug and trace functionality.

1.2 Compliance

The ETM-M7 complies with, or implements, the specifications described in:

- *Trace macrocell*.
- *Interconnect architecture*.

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

1.2.1 Trace macrocell

The ETM-M7 implements the ETM architecture version 4. See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*.

1.2.2 Interconnect architecture

The ETM-M7 complies with the *Advanced Microcontroller Bus Architecture* (AMBA) 3 *Advanced Peripheral Bus* (APB) and *Advanced Trace Bus* (ATB) protocols. See the *ARM® AMBA® 3 APB Protocol Specification* and *ARM® AMBA® 3 ATB Protocol Specification*.

1.3 Features

See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for information about:

- The trace protocol.
- The features of ETMv4.
- Controlling tracing using triggering and filtering resources.
- ETM sharing.

Table 1-1 shows the features of the ETM-M7 that are IMPLEMENTATION DEFINED, in terms of either:

- The number of times the feature is implemented.
- The size of the feature.

Table 1-1 ETM-M7 features with implementation-defined number of instances or size

Feature	ETM-M7 configurations		Notes
	Instruction trace only	Instruction and data trace	
Address comparators	0 pairs	4 pairs	See bits[3:0] of the *ID Register 4* on page 3-44.
Data value comparators	0	2	See bits[7:4] of the *ID Register 4* on page 3-44.
Context ID comparators	0	0	See bits[27:24] of the *ID Register 4* on page 3-44.
Single-Shot comparator resource	1	1	In instruction only configuration, the single-shot comparators are only sensitive to the processor comparator inputs.
Counters	1[a]	2	See bits[30:28] of the *ID Register 5* on page 3-45.
Cycle count size	12	12	See bits[28:25] of the *ID Register 2* on page 3-42.
Sequencer	0	1	One four-state sequencer. See bits[27:25] of the *ID Register 5* on page 3-45.
Processor comparator inputs	4	4	See bits[15:12] of the *ID Register 4* on page 3-44.
External inputs	2	4	See bits[8:0] of the *ID Register 5* on page 3-45.
External outputs	2	4	-
External input selectors	0	0	See bits[11:9] of the *ID Register 5* on page 3-45.
Resource selector pairs	2	8	See bits[19:16] of the *ID Register 4* on page 3-44.
Instruction trace port size	8-bit	8-bit	-
Data trace port size	-	64-bit	-

Table 1-1 ETM-M7 features with implementation-defined number of instances or size (continued)

Feature	ETM-M7 configurations		Notes
	Instruction trace only	Instruction and data trace	
Instruction FIFO[b]	64 byte with 8-bit output	64 byte with 8-bit output	Uses ATB.
Data FIFO	-	256 byte with 64-bit output	Uses ATB.
Claim tag bits	4	4	-

a. Minimal counter implementation.

b. Instruction trace can be configured to take priority over data trace. See bit[10] of the TRCSTALLCTLR.

Table 1-2 shows the optional features of the ETM architecture that the ETM-M7 implements.

Table 1-2 ETM-M7 implementation of optional features

Feature	Implemented Instruction trace only	Implemented Instruction and data trace	Notes
Configurable FIFO	No	No	-
Trace Start/Stop block	Yes	Yes	-
Trace all branches option	Yes	Yes	See bit[5] of the *ID Register 0* on page 3-40
Trace of conditional instructions	Yes	Yes	See bits[13:12] and bit[6] of the *ID Register 0* on page 3-40
Cycle counting in instruction trace	Yes	Yes	See bit[7] of the *ID Register 0* on page 3-40
Data trace supported	No	Yes	See bits[4:3] of the *ID Register 0* on page 3-40
Data address comparison	No	Yes	See bit[8] of the *ID Register 4* on page 3-44
OS Lock mechanism	No	No	The Cortex-M7 processor does not implement OS Lock
Secure non-invasive debug	No	No	The Cortex-M7 processor does not implement the Security Extensions
Context ID tracing	No	No	See bits[9:5] of the *ID Register 2* on page 3-42
Trace output	Yes	Yes	ATB
Timestamp size	64-bit	64-bit	See bits[28:24] of the *ID Register 0* on page 3-40
Memory-mapped access to ETM registers	Yes	Yes	See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for more information about the Access permissions behaviors on register accesses for different trace unit states
External debugger access to ETM registers	Yes	Yes	
System instruction access to ETM registers	No	No	
VMID comparator support	No	No	See bits[31:28] of the *ID Register 4* on page 3-44
ATB trigger support	Yes	Yes	See bit[22] of the *ID Register 5* on page 3-45

1.4 Interfaces

The ETM-M7 has the following main interfaces:

- Processor trace.
- ATB.
- External PPB.
- Production test.

Interfaces on page 2-4 describes the ETM-M7 interfaces in more detail.

1.5 Configurable options

The ETM-M7 includes the following configuration inputs:

- **NUMPROC**.
- **SYSSTALL**.

1.6 Test features

The ETM-M7 provides the **DFTSE** input for testing the implemented device. See the *ARM® Cortex®-M7 Integration and Implementation Manual*.

1.7 Product documentation and design flow

This section describes the ETM-M7 books, how they relate to the design flow, and the relevant architectural standards and protocols.

See *Additional reading* on page ix for more information about the books described in this section.

1.7.1 Documentation

The ETM-M7 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the ETM-M7. It is required at all stages of the design flow. Some behavior described in the TRM might not be relevant because of the way that the ETM-M7 is implemented and integrated.

Integration and Implementation Manual

For both the processor and the ETM, the *Cortex-M7 Integration and Implementation Manual* (IIM) describes:

- The available build configuration options and related issues in selecting them.
- How to configure the *Register Transfer Level* (RTL) with the build configuration options.
- How to integrate the processor into a SoC. This includes a description of the pins that the integrator must tie off to configure the macrocell for the required integration.
- The processes to sign off the integration and implementation of the design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by ARM are example reference implementations. Contact your EDA vendor for EDA tool support.

Reference methodology documentation from your EDA tools vendor complements the IIM.

The IIM is a confidential book that is only available to licensees.

1.7.2 Design flow

The ETM-M7 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following process:

Implementation

For MCUs, often a single design team integrates the processor before synthesizing the complete design. Alternatively, the team can synthesise the processor on its own or partially integrated, to produce a hard macrocell. The hard macrocell is then integrated, possibly by a separate team, which might include integrating RAMs into the design.

Integration The integrator connects the implemented design into a SoC. This includes connecting it to a memory system and peripherals.

Programming

This is the last process. The system programmer develops the software required to configure and initialize the ETM-M7, and tests the required application software.

Each stage of the process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the ETM-M7.

The operation of the final device depends on:

Build configuration

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting design.

Configuration inputs

The integrator configures some features of the ETM-M7 by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration

The programmer configures the ETM-M7 by programming particular values into registers. This affects the behavior of the ETM-M7.

See Chapter 3 *Programmers Model* for information on the ETM-M7 registers.

Note

This manual refers to IMPLEMENTATION DEFINED features that are applicable to build configuration options. Reference to a feature that is included means that the appropriate build and pin configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

1.8 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

r0p1 The following changes have been made in this release:

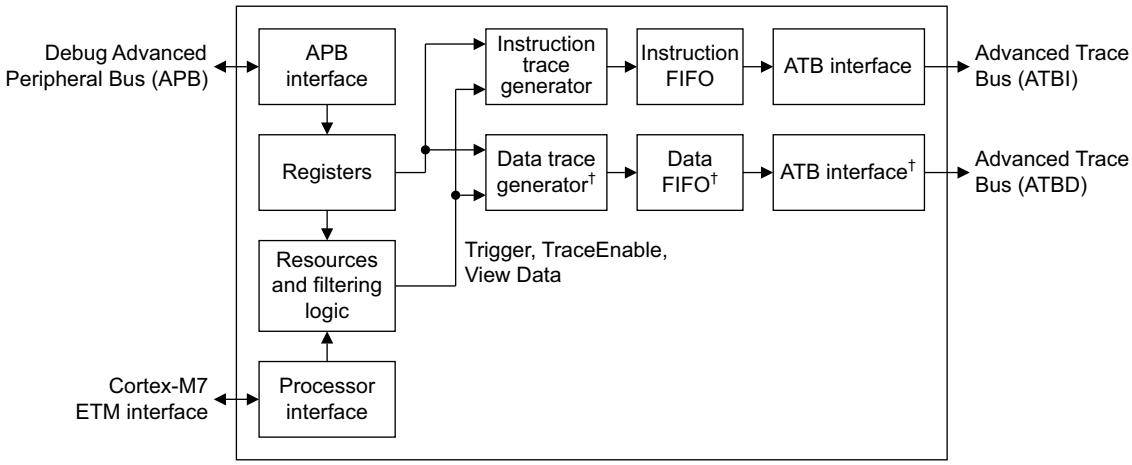
- The TRCIDR1 register reset value is updated to `0b0001`.

Chapter 2
Functional Description

This chapter describes the interfaces, operation, clocking and resets of the ETM-M7. It contains the following sections:

2.1 About the functions

Figure 2-1 shows the main functional blocks of the ETM-M7.



†Only present if your ETM implementation has both instruction trace and data trace.

Figure 2-1 ETM-M7 block diagram

2.1.1 Processor interface

This block connects to the ETM-M7 interface. It tracks the execution and speculation information from the processor, decodes the control signals and passes on the information to the internal interfaces.

2.1.2 Instruction trace generator

This block generates the trace packets that are a compressed form of the instruction execution information provided by the Cortex-M7 processor. The trace packets are then passed to the instruction FIFO.

2.1.3 Data trace generator

This block generates trace packets that are a compressed form of the data transfers provided by the Cortex-M7 processor. The trace packets are then passed to the data FIFO.

2.1.4 FIFO

This block buffers bursts of trace packets. Separate FIFOs are provided, one for the instruction trace stream, and one for the data trace stream when present.

2.1.5 Resources and filtering logic

These blocks contain various comparators and state machines that are programmed by trace software to trigger and filter the trace information. They start and stop trace generation, depending on the conditions that have been set.

2.1.6 ATB interfaces

There are two ATB interfaces:

Instruction ATB interface

This reads single bytes of packet information from the instruction FIFO and sends them over the instruction ATB interface.

Data ATB interface

This reads up to eight bytes of packet information from the data FIFO and sends them over the data ATB interface.

2.1.7 APB interface

This block implements the interface to the APB that provides access to the programmable registers.

2.1.8 Global timestamping

The ETM-M7 supports connection to a global timestamp source. This provides a 64-bit timestamp that a debugger can use for coarse-grained profiling, and correlation of trace sources. ARM recommends that the timestamp counter is no slower than 10% of the processor clock frequency.

Note

Decompression of data trace relies on the presence of a global timestamp count.

2.2 Interfaces

The ETM-M7 has the following interfaces:

ATB Two ATB interfaces:

- An 8-bit AMBA 3 ATB interface for instruction only trace.
- An optional 64-bit AMBA 3 ATB interface for data trace.

These export trace output from the macrocell. Both interfaces have handshaking signals that indicate when trace data is valid and when the receiving component is ready to accept data. There are also signals to request and acknowledge a flush of the trace information and to indicate when a trigger condition has occurred.

See the *ARM® AMBA® 3 ATB Protocol Specification* for more information about these interfaces.

APB An APB interface that provides access to the programmable registers in the ETM-M7 and connects to the PPB. You can use this interface to configure the ETM-M7 for a trace session.

See the *ARM® AMBA® 3 APB Protocol Specification* for more information about this interface.

Processor trace

The Cortex-M7 processor passes its execution information to the ETM-M7 over the processor trace interface. This interface provides both instruction and data execution history and contains address, data, and control information. The information carried on the control bus includes:

- The number of instructions executed in the same cycle.
- Changes in program flow.
- The current processor instruction state.
- The addresses of memory locations accessed by load and store instructions.
- The data values transferred by load and store instructions.
- The type, direction, and size of a transfer.
- Condition code information.
- Exception information.

This interface also includes:

- Wait for interrupt state information signals.
- A signal from the ETM to power up the interface.

Miscellaneous

The ETM-M7 has other interface signals that:

- Configure the ETM. See *Configurable options* on page 1-9.
- Input and output external resource information that controls triggering and filtering of the trace.
- Control which core is enabled, as the trace source, on the processor trace interface of the ETM.
- Enable invasive and non-invasive debug.

Test This interface contains the scan enable signal used in production testing of the ETM-M7.

2.2.1 ETMEVENT connectivity

Table 2-1 shows the connection of the **ETMEVENTS** inputs that come from the CTI.

Table 2-1 ETMEVENTS connections

Bits	Description
[3:0]	**CTITRIGOUT**

The ETM output resources, **ETMEVENTM**, are connected to the CTI, as Table 2-2 shows.

Table 2-2 ETMEVENTM connections to CTI

ETM output	CTI input
ETMEVENTM[0]	**CTITRIGIN[2]**
ETMEVENTM[1]	**CTITRIGIN[3]**
ETMEVENTM[2]	**CTITRIGIN[4]**
ETMEVENTM[3]	**CTITRIGIN[5]**

2.3 Clocking and resets

The following sections describe the ETM-M7 clocks and resets:

- *ETM-M7 clock*.
- *ETM-M7 low power control*.
- *ETM-M7 reset*.
- *Access permissions and power domains*.

2.3.1 ETM-M7 clock

The ETM-M7 has one clock, **CLK**. This clock is synchronous to the **CLK** input of the Cortex-M7 processor.

2.3.2 ETM-M7 low power control

The ETM-M7 has outputs to indicate whether the debugger expects power to be maintained, and also an output to indicate when tracing is inactive. The use of these signals is IMPLEMENTATION SPECIFIC.

The ETM can be configured to remain active even if the Cortex-M7 processor enters a low power state. See bit[23] of the *ID Register 5* on page 3-45.

2.3.3 ETM-M7 reset

The ETM-M7 has a single reset, **nDBGETMRESET**, and must only be reset by a debug reset event.

Note

The programming state must be reconfigured after a debug reset.

2.3.4 Access permissions and power domains

To determine the access permissions as described in the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*, the ETM implements a SinglePower domain. The ETM debug power domain is typically separate from the processor power domain.

2.4 Operation

This section describes the IMPLEMENTATION DEFINED features of the ETM-M7 macrocell. It contains the following sections:

- *Implementation defined registers*.
- *Precise TraceEnable events*.
- *Parallel instruction execution*.
- *Trace and comparator features* on page 2-8.
- *Packet formats* on page 2-8.
- *Resource selection* on page 2-8.
- *Trace flush behavior* on page 2-10.
- *Low power state behavior* on page 2-10.
- *Cycle counter* on page 2-10.
- *Micro-architectural exceptions* on page 2-10.
- *Trace synchronization* on page 2-10.

See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for more information about the operation of the ETM-M7.

2.4.1 Implementation defined registers

There are two groups of ETM registers:

- Registers that are completely defined by the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*.
- Registers that are partly IMPLEMENTATION DEFINED.

See Chapter 3 *Programmers Model* for more information about the ETM-M7 registers.

2.4.2 Precise TraceEnable events

The *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* states that **ViewInst** and **ViewData** are imprecise under certain conditions, with some IMPLEMENTATION DEFINED exceptions. The only condition that ensures **ViewInst** and **ViewData** are precise is that the enabling event condition is TRUE.

2.4.3 Parallel instruction execution

The Cortex-M7 processor supports parallel instruction execution. This means the macrocell is capable of tracing two instructions per cycle and two data transfers per cycle.

If **ViewInst** is active for a cycle, the ETM-M7:

- Always traces the first of any paired instructions.
- Can trace data for any of the instructions traced.

2.4.4 Trace and comparator features

This section specifies the implementation of the trace and comparator features of the ETM-M7:

- *Trace features*.
- *Comparator features*.

Trace features

The ETM-M7 implements all of the ETMv4 trace features. This means it supports:

- Data value and data address tracing.
- Data suppression.
- Cycle-accurate tracing.
- Timestamping.

See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for descriptions of these features.

Comparator features

The ETM-M7 implements data address comparison. See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for a description of data address comparison.

2.4.5 Packet formats

The ETM instruction trace interface does not implement the following instruction trace packet types:

- Speculation resolution:
  - Mispredict packet.
  - Cancel format 2 and 3 packets.
- Conditional tracing:
  - All instruction format packets.
  - Result format 1 and 4 packets.
- Q packets.

The ETM data trace interface implements all data trace packet types, except for the P1 format 6 and 7 data trace packets.

See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for the trace packet format descriptions.

2.4.6 Resource selection

The ETM-M7 uses event selectors to control the following resources:

- Trace events (triggers and markers in the trace stream).
- Timestamp event.
- ViewInst event.
- ViewData event.
- Counter control.
- Sequencer state transitions, only available in instruction and data trace configuration.

Each event selector is configured to be sensitive to a resource selector pair, and one resource selector pair can control more than one event selector.

The ETM provides one fixed resource selector pair, with static values of 0 and 1, and one or seven configurable selector pairs depending on the selected configuration. A resource selector pair provides a bitfield OR selector for resources in two different groups, with each group and a configurable boolean combination provided.

Table 2-3 shows the resources that can be selected for the instruction-only configuration.

Table 2-3 Instruction-only resource selection

Group	Select	Resource
0b0000	0-1	External input selector 0-1
0b0001	0-3	Processor comparator inputs 0-3
0b0010	0	Counter at zero 0
0b0011	0	Single-Shot comparator 0

Table 2-4 shows the resources that can be selected for the Instruction and data configuration.

Table 2-4 Instruction and data resource selection

Group	Select	Resource
0b0000	0-3	External input selector 0-3
0b0001	0-3	Processor comparator inputs 0-3
0b0010	0-1	Counter at zero 0-1
	4-7	Sequencer states 0-3
0b0011	0	Single-Shot comparator 0
0b0100	0-7	Single address comparator 0-7
0b0101	0-3	Address range comparator 0-3

For example, Figure 2-2 shows the steps necessary to use a single address comparator to generate a trigger event and an ATB trigger. This example uses the first single resource selector that can be user-configured.

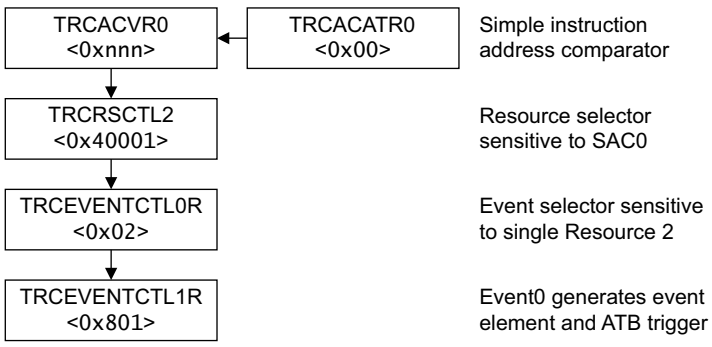


Figure 2-2 Trigger event resource selection

The processor comparator inputs are controlled by the *Data Watchpoint and Trace* (DWT) unit in the processor. The ETM single shot and start-stop logic, when present, might not reliably trigger where DWT comparators are programmed for data address comparison.

2.4.7 Trace flush behavior

Events that are observed by the ETM can be confirmed to have reached the trace bus output with the use of the ATB flush protocol. Both ATB ports must be flushed if all trace is required. The ETM internally flushes instruction and data trace together whenever either flush request is seen but does not guarantee that the trace data has drained from the ETM. When the processor enters a low power state, this also causes all trace to be output from the ETM.

2.4.8 Low power state behavior

When the processor enters a low power state there is a delay before the resources to the ETM become inactive. This permits the last instruction executed to trigger a comparator, update the counter or sequencer, and the resultant event packet to be inserted in the specified trace stream. This event packet is presented on the trace bus before the ETM itself enters a low power state.

If an event packet is generated for a different reason, it is not guaranteed to be output before the ETM enters a low power state, but is traced when the processor leaves the low power state, if the ETM logic is not reset before this can occur.

This low power behavior can be disabled using TRCEVENTCTL1R.LPOVERRIDE bit, see *Event Control 1 Register* on page 3-20. In this case the ETM resources remain active.

2.4.9 Cycle counter

The cycle counter is a 12-bit counter. It does not count when non-invasive debug is disabled, or when the processor is in a low power state.

2.4.10 Micro-architectural exceptions

The ETM indicates exceptions for the following micro-architectural behaviors using the following TYPE encodings:

`0b0000100001` Entered a restricted region.

`0b0000100000` ETM disabled before completion of exception operation.

2.4.11 Trace synchronization

The ETM receives and combines all sources of trace synchronization requests before inserting trace synchronization in both trace streams, provided that data trace is active.

To decompress the trace streams, synchronization information in the data trace stream determines the alignment with synchronization information in the instruction stream. If the ETM is configured to trace only events in the data stream, you must configure the instruction trace stream to contain sufficient elements to permit the required data trace stream synchronization.

2.4.12 Event tracing and triggers

Instruction event packets can be inserted in the instruction trace stream on every cycle, but if events are traced continuously on every cycle the instruction FIFO is unable to drain and overflows.

When used in conjunction with the optimized Cortex-M7 TPIU, ATB triggers must not be enabled, TRCEVENTCTL1R.ATB must be set to 0.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About the programmers model

This chapter describes the mechanisms for programming the registers used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

3.2 Modes of operation and execution

This section describes how to control ETM programming and program and read the ETM registers. It contains:

- *Controlling ETM programming*.
- *Programming and reading ETM registers* on page 3-4.

3.2.1 Controlling ETM programming

When programming the ETM registers, you must enable all the changes at the same time. For example, if the counter is reprogrammed, it might start to count based on incorrect events, before the trigger condition has been correctly set up.

To disable all trace operations during programming use:

- The ETM main enable in the TRCPRGCTLR, see *Programming Control Register* on page 3-14.
- The TRCSTATR to indicate the ETM status, see *Status Register* on page 3-15.

Figure 3-1 shows the procedure to use.

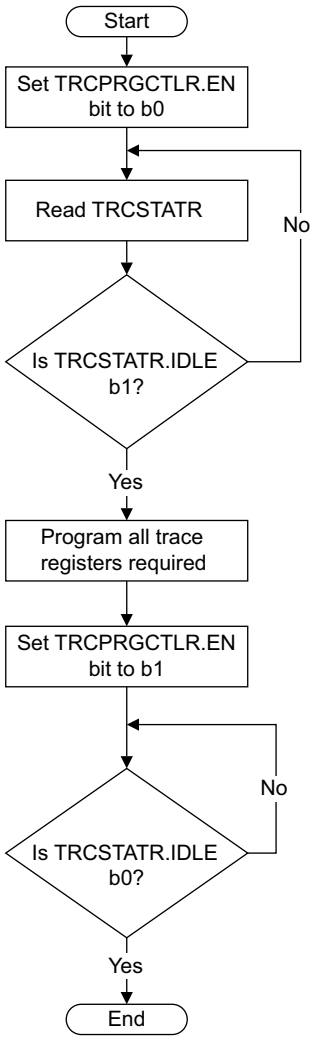


Figure 3-1 Programming ETM-M7 registers

The Cortex-M7 processor does not have to be in debug state while you program the ETM registers.

3.2.2 Programming and reading ETM registers

You program and read the ETM registers using the external PPB interface. This provides a direct method of programming the ETM-M7.

3.3 Register summary

This section summarizes the ETM registers. For full descriptions of the ETM registers, see:

- *Register descriptions* on page 3-14, for the IMPLEMENTATION DEFINED registers.
- The *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*, for the other registers.

Table 3-1 shows the ETM registers in numerical order and describes each register.

The macrocell registers are listed by functional group in *Functional grouping of registers* on page 3-9. The functional group register tables include additional information about each register:

- The register access type. This is read-only, write-only, or read and write.
- The base offset address of the register. The base offset of a register is always four times its register number.
- Additional information about the implementation of the register, where appropriate.

Note

- Registers not listed here are not implemented. Reading a non-implemented register address returns 0. Writing to a non-implemented register address has no effect.
- In Table 3-1:
  - The Reset value column shows the value of the register immediately after an ETM reset. For read-only registers, every read of the register returns this value.
  - Access type is described as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

All ETM registers are 32 bits wide.

Table 3-1 ETM-M7 register summary

Register number	Base offset	Name	Type	Reset value	Description
1	0x004	TRCPRGCTLR	RW	0x00000000	*Programming Control Register* on page 3-14
2	0x008	TRCPROCSELR	RW	0x00000000	*Processor Select Control Register* on page 3-14
3	0x00C	TRCSTATR	RO	-	*Status Register* on page 3-15
4	0x010	TRCCONFIGR	RW	-	*Trace Configuration Register* on page 3-16
8	0x020	TRCEVENTCTL0R	RW	-	*Event Control 0 Register* on page 3-18
9	0x024	TRCEVENTCTL1R	RW	-	*Event Control 1 Register* on page 3-20
11	0x02C	TRCSTALLCTLR	RW	-	*Stall Control Register* on page 3-21
12	0x030	TRCTSCTLR	RW	-	*Global Timestamp Control Register* on page 3-22
13	0x034	TRCSYNCPR	RW[c]	-	*Synchronization Period Register* on page 3-23
			RO[d]	0xA	

Table 3-1 ETM-M7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
14	0x038	TRCCCCTLR	RW	-	*Cycle Count Control Register* on page 3-24
15	0x03C	TRCBBCTLR[a]	RW	-	*Branch Broadcast Control Register* on page 3-24
16	0x040	TRCTRACEIDR	RW	-	*Trace ID Register* on page 3-25
32	0x080	TRCVICTLR	RW	-	*ViewInst Main Control Register* on page 3-26
33	0x084	TRCVIIECTLR[a]	RW	-	*ViewInst Include/Exclude Control Register* on page 3-27
34	0x088	TRCVISSCTLR	RW	-	*ViewInst Start/Stop Control Register* on page 3-29
35	0x08C	TRCVIPCSSCTLR	RW	-	*ViewInst Start-Stop Processor Comparator Control Register* on page 3-28
40	0x0A0	TRCVDCTLR[a]	RW	-	*ViewData Main Control Register* on page 3-30
41	0x0A4	TRCVDSACCTLR[a]	RW	-	*ViewData Include/Exclude Single Address Comparator Register* on page 3-31
42	0x0A8	TRCVDARCCTLR[a]	RW	-	*ViewData Include/Exclude Address Range Comparator Register* on page 3-31
64-66	0x100-0x108	TRCSEQEVR0-2[a]	RW	-	*Sequencer State Transition Control Registers 0-2* on page 3-32
70	0x118	TRCSEQRSTEVR[a]	RW	-	*Sequencer Reset Control Register* on page 3-33
71	0x11C	TRCSEQSTR[a]	RW	-	*Sequencer State Register* on page 3-34
80-81	0x140-0x144	TRCCNTRLDVR0-1[b]	RW	-	*Counter Reload Value Registers 0-1* on page 3-35
84-85	0x150-0x154	TRCCNTCTLR0-1[a]	RW	-	*Counter Control Registers 0-1* on page 3-35
88-89	0x160-0x164	TRCCNTVR0-1[a]	RW	-	*Counter Value Registers 0-1* on page 3-36
96	0x180	TRCIDR8	RO	0x00000001	*ID Register 8-13* on page 3-37
97	0x184	TRCIDR9	RO	0x00000020[c]	
				0x00000000[d]	
98	0x188	TRCIDR10	RO	0x00000002[c]	
				0x00000000[d]	
99	0x18C	TRCIDR11	RO	0x00000000	
100	0x190	TRCIDR12	RO	0x00000001	
101	0x194	TRCIDR13	RO	0x00000000	
112	0x1C0	TRCIMSPEC0	RW	0x00000000	*Implementation Specific Register 0* on page 3-39
120	0x1E0	TRCIDR0	RO	0x0C000EFF[c]	*ID Register 0* on page 3-40
				0x0C000EE1[d]	
121	0x1E4	TRCIDR1	RO	0x4100F401	*ID Register 1* on page 3-41

Table 3-1 ETM-M7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
122	0x1E8	TRCIDR2	RO	0x00420004[c]	*ID Register 2* on page 3-42
				0x00000004[d]	
123	0x1EC	TRCIDR3	RO	0x05090004[ce]	*ID Register 3* on page 3-43
				0x37090004[de]	
124	0x1F0	TRCIDR4	RO	0x00174124[c]	*ID Register 4* on page 3-44
				0x00114000[d]	
125	0x1F4	TRCIDR5	RO	0x28C70004[c]	*ID Register 5* on page 3-45
				0x90C70002[d]	
130-143	0x208-0x23C	TRCRSCTLR2-15[f]	RW	-	*Resource Selection Registers 2-15* on page 3-47
160	0x280	TRCSSCCR0	RW	-	*Single-shot Comparator Control Register 0* on page 3-47
168	0x2A0	TRCSSCSR0	RW	-	*Single-shot Comparator Status Register 0* on page 3-48
176	0x2C0	TRCSSPCICR0	RW	-	*Single-shot Comparator Status Register 0* on page 3-48
193	0x304	TRCOSLSR	RO	0x0	*OS Lock Status Register* on page 3-50
196	0x310	TRCPDCR	RW	0x00000000	*Power Down Control Register* on page 3-50
197	0x314	TRCPDSR	RO	0x00000003	*Power Down Status Register* on page 3-51
256-270	0x400-0x438	TRCACVR0-7[a]	RW	-	*Address Comparator Value Registers 0-7* on page 3-52
288-302	0x480-0x4B8	TRCACATR0-7[a]	RW	-	*Address Comparator Access Type Registers 0-7* on page 3-52
320-324	0x500-0x510	TRCDVCVR0-1[a]	RW	-	*Data Value Comparator Value Registers 0-1* on page 3-54
352-356	0x580-0x590	TRCDVCMR0-1[a]	RW	-	*Data Value Comparator Mask Registers 0-1* on page 3-55
951	0xEDC	TRCITMISCOUTR	WO	-	*Integration Miscellaneous Outputs Register* on page 3-57
952	0xEE0	TRCITMISCINR	RO	-	*Integration Miscellaneous Inputs Register* on page 3-58
953	0xEE4	TRCITATBIDR	WO	-	*Integration ATB Identification Register* on page 3-59
954	0xEE8	TRCITDDATAR	WO	-	*Integration Data ATB Data Register* on page 3-59
955	0xEEC	TRCITIDATAR	WO	-	*Integration Instruction ATB Data Register* on page 3-60
956	0xEF0	TRCITDATBINR	RO	-	*Integration Data ATB In Register* on page 3-61

Table 3-1 ETM-M7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
957	0xEF4	TRCITIATBINR	RO	-	*Integration Instruction ATB In Register* on page 3-61
958	0xEF8	TRCITDATBOUTR	WO	-	*Integration Data ATB Out Register* on page 3-62
959	0xEFC	TRCITIATBOUTR	WO	-	*Integration Instruction ATB Out Register* on page 3-63
960	0xF00	TRCITCTRL	RW	0x00000000	*Integration Mode Control Register* on page 3-64
1000	0xFA0	TRCCLAIMSET	RW	0x00000004	*Claim Tag Set Register* on page 3-64
1001	0xFA4	TRCCLAIMCLR	RW	0x00000000	*Claim Tag Clear Register* on page 3-65
1004	0xFB0	TRCLAR	WO	-	*Software Lock Access Register* on page 3-65
1005	0xFB4	TRCLSR	RO	-	*Software Lock Status Register* on page 3-66
1006	0xFB8	TRCAUTHSTATUS	RO	-	*Authentication Status Register* on page 3-67
1007	0xFBC	TRCDEVARCH	RO	0x47704A13	*Device Architecture Register* on page 3-68
1010	0xFC8	TRCDEVID	RO	0x00000000	*Device ID Register* on page 3-69
1011	0xFCC	TRCDEVTYPE	RO	0x00000013	*Device Type Register* on page 3-69
1012-1019	0xFD0-0xFEC	TRCPIDR0-7	RO	-	*Peripheral Identification Registers* on page 3-70
1020-1023	0xFF0-0xFFC	TRCCIDR0-3	RO	-	*Component Identification Registers* on page 3-73

a. Only available in instruction and data trace configuration.
b. TRCCNTRLDVR1 only available in instruction and data trace configuration.
c. The reset value in instruction and data trace configuration.
d. The reset value in instruction trace only configuration.
e. Bits[30:27] are implementation dependent.
f. TRCRSCTLR4-15 only available in instruction and data trace configuration.

3.3.1 Functional grouping of registers

This section shows the macrocell registers by functional group, as follows:

- *General control and ID registers*.
- *Trace filtering control registers* on page 3-10.
- *Derived resource registers* on page 3-10.
- *Implementation specific and identification registers* on page 3-11.
- *Resource selection registers* on page 3-11.
- *Single-shot comparator registers* on page 3-11.
- *Power control registers* on page 3-12.
- *Comparator registers* on page 3-12.
- *Integration test registers* on page 3-13.
- *CoreSight management registers* on page 3-13.

These functional groups include all of the registers.

General control and ID registers

Table 3-2 shows the general control and ID registers in numerical order.

Table 3-2 General control and ID registers

Register number	Name	Base offset	Description
1	TRCPRGCTLR	0x004	*Programming Control Register* on page 3-14
2	TRCPROCSELR	0x008	*Processor Select Control Register* on page 3-14
3	TRCSTATR	0x00C	*Status Register* on page 3-15
4	TRCCONFIGR	0x010	*Trace Configuration Register* on page 3-16
8	TRCEVENTCTL0R	0x020	*Event Control 0 Register* on page 3-18
9	TRCEVENTCTL1R	0x024	*Event Control 1 Register* on page 3-20
11	TRCSTALLCTLR	0x02C	*Stall Control Register* on page 3-21
12	TRCTSCTLR	0x030	*Global Timestamp Control Register* on page 3-22
13	TRCSYNCPR	0x034	*Synchronization Period Register* on page 3-23
14	TRCCCCTLR	0x038	*Cycle Count Control Register* on page 3-24
15	TRCBBCTLR[a]	0x03C	*Branch Broadcast Control Register* on page 3-24
16	TRCTRACEIDR	0x040	*Trace ID Register* on page 3-25

a. Instruction and data trace implementation only

Trace filtering control registers

Table 3-3 shows the trace filtering control registers in numerical order.

Table 3-3 Trace filtering control registers

Register number	Name	Base offset	Description
32	TRCVICTLR	0x080	*ViewInst Main Control Register* on page 3-26
33	TRCVIIECTLR[a]	0x084	*ViewInst Include/Exclude Control Register* on page 3-27
34	TRCVISSCTLR	0x088	*ViewInst Start/Stop Control Register* on page 3-29
35	TRCVIPCSSCTLR	0x08C	*ViewInst Start-Stop Processor Comparator Control Register* on page 3-28
40	TRCVDCTLR[a]	0x0A0	*ViewData Main Control Register* on page 3-30
41	TRCVDSACCTLR[a]	0x0A4	*ViewData Include/Exclude Single Address Comparator Register* on page 3-31
42	TRCVDARCCTLR[a]	0x0A8	*ViewData Include/Exclude Address Range Comparator Register* on page 3-31

a. Only available in instruction and data trace configuration.

Derived resource registers

Table 3-4 shows the derived resource registers in numerical order. These registers control:

- The two counters, and associated events.
- The sequencer, and associated state change events.
- Trigger events.
- External output events.
- External input selection.

Table 3-4 Derived resource registers

Register number	Name	Base offset	Description
64-66	TRCSEQEVR0-2[a]	0x100-0x108	*Sequencer State Transition Control Registers 0-2* on page 3-32
70	TRCSEQRSTEVR[a]	0x118	*Sequencer Reset Control Register* on page 3-33
71	TRCSEQSTR[a]	0x11C	*Sequencer State Register* on page 3-34
80-81	TRCCNTRLDVR0-3[b]	0x140-0x14C	*Counter Reload Value Registers 0-1* on page 3-35
84	TRCCNTCTLR0[a]	0x150	*Counter Control Registers 0-1* on page 3-35
85	TRCCNTCTLR1[a]	0x154	
88-89	TRCCNTVR0-1[a]	0x160-0x164	*Counter Value Registers 0-1* on page 3-36

a. Only available in instruction and data trace configuration.

b. Only TRCCNTRLDVR0 is available in instruction trace only configuration.

Implementation specific and identification registers

Table 3-5 shows the IMPLEMENTATION SPECIFIC and identification registers in numerical order.

Table 3-5 Implementation specific and identification registers

Register number	Name	Base offset	Description
96	TRCIDR8	0x180	*ID Register 8-13* on page 3-37
97	TRCIDR9	0x184	
98	TRCIDR10	0x188	
99	TRCIDR11	0x18C	
100	TRCIDR12	0x190	
101	TRCIDR13	0x194	
112	TRCIMSPEC0	0x1C0	*Implementation Specific Register 0* on page 3-39
120	TRCIDR0	0x1E0	*ID Register 0* on page 3-40
121	TRCIDR1	0x1E4	*ID Register 1* on page 3-41
122	TRCIDR2	0x1E8	*ID Register 2* on page 3-42
123	TRCIDR3	0x1EC	*ID Register 3* on page 3-43
124	TRCIDR4	0x1F0	*ID Register 4* on page 3-44
125	TRCIDR5	0x1F4	*ID Register 5* on page 3-45

Resource selection registers

Table 3-6 shows the resource selection registers in numerical order.

Table 3-6 Resource selection registers

Register number	Name	Base offset	Description
130-143	TRCRSCTLR2-15[a]	0x208-0x23C	*Resource Selection Registers 2-15* on page 3-47

a. Only TRCRSCTLR4-15 are available in instruction and data trace configuration.

Single-shot comparator registers

Table 3-7 shows the single-shot comparator registers in numerical order.

Table 3-7 Single-shot comparator registers

Register number	Name	Base offset	Description
160	TRCSSCCR0	0x280	*Single-shot Comparator Control Register 0* on page 3-47
168	TRCSSCSR0	0x2A0	*Single-shot Comparator Status Register 0* on page 3-48
176	TRCSSPCICR0	0x2C0	*Single-shot Processor Comparator Input Control Register* on page 3-49

Power control registers

Table 3-8 shows the power control registers in numerical order.

Table 3-8 Power control registers

Register number	Name	Base offset	Description
193	TRCOSLSR	0x304	*OS Lock Status Register* on page 3-50
196	TRCPDCR	0x310	*Power Down Control Register* on page 3-50
197	TRCPDSR	0x314	*Power Down Status Register* on page 3-51

Comparator registers

The comparator registers are only available in instruction and data trace configuration. Table 3-9 shows the comparator registers in numerical order.

Table 3-9 Comparator registers

Register number	Name	Base offset[a]	Description
256-270	TRCACVR0-7	0x400-0x438	*Address Comparator Value Registers 0-7* on page 3-52
288-302	TRCACATR0-7	0x480-0x4B8	*Address Comparator Access Type Registers 0-7* on page 3-52
320-324	TRCDVCVR0-1	0x500-0x510	*Data Value Comparator Value Registers 0-1* on page 3-54
352-356	TRCDVCMR0-1	0x580-0x590	*Data Value Comparator Mask Registers 0-1* on page 3-55

a. The base offset is doubleword aligned and not on a word boundary.

Integration test registers

Table 3-10 shows the integration test registers in numerical order.

Table 3-10 Integration test registers

Register number	Name	Base offset	Description
951	Integration Miscellaneous Outputs Register	0xEDC	*Integration Miscellaneous Outputs Register* on page 3-57
952	Integration Miscellaneous Inputs Register	0xEE0	*Integration Miscellaneous Inputs Register* on page 3-58
953	Integration ATB Identification Register	0xEE4	*Integration ATB Identification Register* on page 3-59
954	Integration Data ATB Data Register	0xEE8	*Integration Data ATB Data Register* on page 3-59
955	Integration Instruction ATB Data Register	0xEEC	*Integration Instruction ATB Data Register* on page 3-60
956	Integration Data ATB In Register	0xEF0	*Integration Data ATB In Register* on page 3-61
957	Integration Instruction ATB In Register	0xEF4	*Integration Instruction ATB In Register* on page 3-61
958	Integration Data ATB Out Register	0xEF8	*Integration Data ATB Out Register* on page 3-62
959	Integration Instruction ATB Out Register	0xEFC	*Integration Instruction ATB Out Register* on page 3-63

CoreSight management registers

Table 3-11 shows the CoreSight management registers in numerical order.

Table 3-11 CoreSight management registers

Register number	Name	Base offset	Description
960	TRCITCTRL	0xF00	*Integration Mode Control Register* on page 3-64
1000	TRCCLAIMSET	0xFA0	*Claim Tag Set Register* on page 3-64
1001	TRCCLAIMCLR	0xFA4	*Claim Tag Clear Register* on page 3-65
1004	TRCLAR	0xFB0	*Software Lock Access Register* on page 3-65
1005	TRCLSR	0xFB4	*Software Lock Status Register* on page 3-66
1006	TRCAUTHSTATUS	0xFB8	*Authentication Status Register* on page 3-67
1007	TRCDEVARCH	0xFBC	*Device Architecture Register* on page 3-68
1010	TRCDEVID	0xFC8	*Device ID Register* on page 3-69
1011	TRCDEVTYPE	0xFCC	*Device Type Register* on page 3-69
1012-1019	TRCPIDR0-7	0xFD0-0xFEC	*Peripheral Identification Registers* on page 3-70
1020-1023	TRCCIDR0-3	0xFF0-0xFFC	*Component Identification Registers* on page 3-73

3.4 Register descriptions

This section describes ETM-M7 registers.

3.4.1 Programming Control Register

The TRCPRGCTLR characteristics are:

Purpose Enables the ETM-M7.

Usage constraints See *Controlling ETM programming* on page 3-3.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-2 shows the TRCPRGCTLR bit assignments.

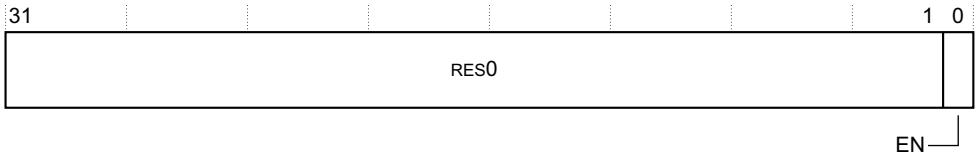


Figure 3-2 TRCPRGCTLR bit assignments

Table 3-12 shows the TRCPRGCTLR bit assignments.

Table 3-12 TRCPRGCTLR bit assignments

Bits	Name	Function
[31:1]	-	RES0.
[0]	EN	Trace program enable: `0` The external pin **STIMREQ** is LOW, and clocks are only enabled when necessary to process APB accesses, or drain any already generated trace. No trace is generated and all resources are inactive. This is the value after reset. `1` The external pin **STIMREQ** is HIGH, and clocks are enabled except for when the **CPUACTIVE** input is deasserted, or non-invasive debug is disabled, and all trace has been drained. The trace unit is enabled. Writes to most registers are ignored.

3.4.2 Processor Select Control Register

The TRCPROCSELR characteristics are:

Purpose Controls which processor to trace.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-3 on page 3-15 shows the TRCPROCSELR bit assignments.

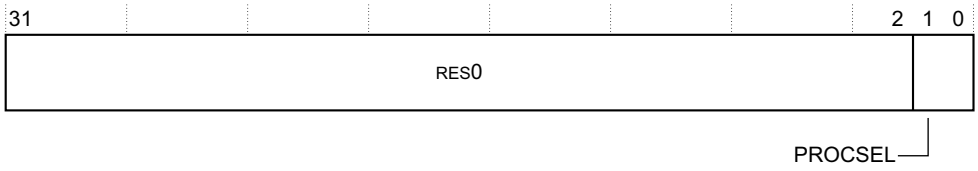


Figure 3-3 TRCPROCSELR bit assignments

Table 3-13 shows the TRCPROCSELR bit assignments.

Table 3-13 TRCPROCSELR bit assignments

Bits	Name	Function
[31:2]	-	RES0.
[1:0]	PROCSEL	Drives the **PROCSEL[1:0]** pin. The supported values are: `0b00` Processor 0. `0b01` Processor 1. `0b10` Processor 2. `0b11` Processor 3.

3.4.3 Status Register

The TRCSTATR characteristics are:

Purpose Indicates the ETM-M7 status.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-4 shows the TRCSTATR bit assignments.

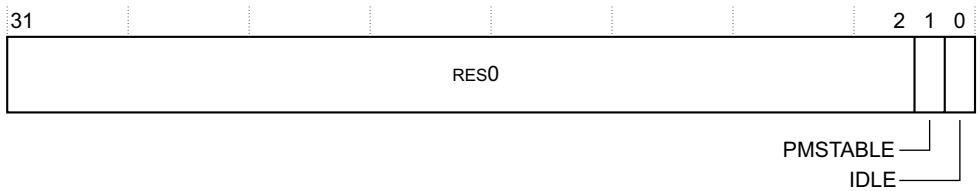


Figure 3-4 TRCSTATR bit assignments

Table 3-14 shows the TRCSTATR bit assignments.

Table 3-14 TRCSTATR bit assignments

Bits	Name	Function
[31:2]	-	RES0.
[1]	PMSTABLE	Indicates whether the ETM-M7 registers are stable and can be read: 0 The programmers model is not stable. 1 The programmers model is stable.
[0]	IDLE	Indicates that the trace unit is inactive: 0 The ETM-M7 is not idle. 1 The ETM-M7 is idle.

3.4.4 Trace Configuration Register

The TRCCONFIGR characteristics are:

Purpose Sets the basic tracing options for the trace unit.

Usage constraints This register must always be programmed as part of the trace unit initialization.

Only accepts writes when the trace unit is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-5 shows the TRCCONFIGR bit assignments.

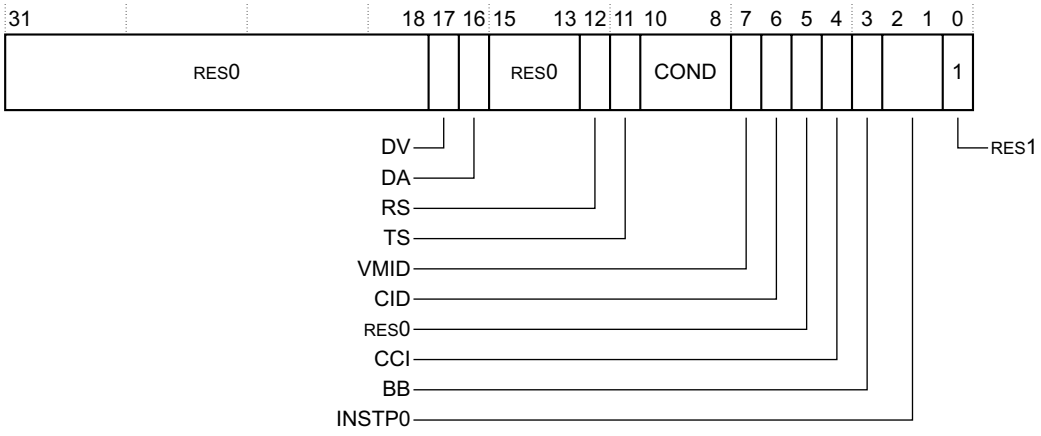


Figure 3-5 TRCCONFIGR bit assignments

Table 3-15 shows the TRCCONFIGR bit assignments for instruction and data configuration.

Table 3-15 TRCCONFIGR bit assignments for instruction and data configuration

Bits	Name	Function
[31:18]	-	RES0.
[17]	DV	Data value tracing: 0 Data value tracing disabled. 1 Data value tracing enabled.
[16]	DA	Data address tracing: 0 Data address tracing disabled. 1 Data address tracing enabled.
[15:13]	-	RES0.
[12]	RS	Return stack enable: 0 Return stack disabled. 1 Return stack enabled.
[11]	TS	Global timestamp tracing: 0 Global timestamp tracing disabled. 1 Global timestamp tracing enabled. For more global timestamping options, see *Global Timestamp Control Register* on page 3-22.
[10:8]	COND	Conditional instruction tracing. The supported values are: 0b000 Conditional instruction tracing disabled. 0b001 Conditional load instructions are traced. 0b010 Conditional store instructions are traced. 0b011 Conditional load and store instructions are traced. 0b111 All conditional instructions are traced. All other values are Reserved.
[7]	VMID	RES0.
[6]	CID	RES0.
[5]	-	RES0.
[4]	CCI	Cycle counting in instruction trace: 0 Cycle counting in instruction trace disabled. 1 Cycle counting in instruction trace enabled. For more cycle counting options, see *Cycle Count Control Register* on page 3-24.
[3]	BB	Branch broadcast mode: 0 Branch broadcast mode disabled. 1 Branch broadcast mode enabled. For more branch broadcast mode options, see *Branch Broadcast Control Register* on page 3-24.
[2:1]	INSTP0	Determines the instructions that are P0 instructions: 0b00 Only branches are P0 instructions. 0b01 Load instructions and branches are P0 instructions. 0b10 Store instructions and branches are P0 instructions. 0b11 Load and store instructions and branches are P0 instructions.
[0]	-	RES1.

Table 3-16 shows the TRCCONFIGR bit assignments for instruction trace only configuration.

Table 3-16 TRCCONFIGR bit assignments for instruction trace only configuration

Bits	Name	Function
[31:18]	-	RES0.
[17]	DV	RES0.
[16]	DA	RES0.
[15:13]	-	RES0.
[12]	RS	Return stack enable: 0 Return stack disabled. 1 Return stack enabled.
[11]	TS	Global timestamp tracing: 0 Global timestamp tracing disabled. 1 Global timestamp tracing enabled. For more global timestamping options, see *Global Timestamp Control Register* on page 3-22.
[10:8]	COND	Conditional instruction tracing. The supported values are: 0b000 Conditional instruction tracing disabled. 0b001 Conditional load instructions are traced. 0b010 Conditional store instructions are traced. 0b011 Conditional load and store instructions are traced. 0b111 All conditional instructions are traced. All other values are Reserved.
[7]	VMID	RES0.
[6]	CID	RES0.
[5]	-	RES0.
[4]	CCI	Cycle counting in instruction trace: 0 Cycle counting in instruction trace disabled. 1 Cycle counting in instruction trace. For more cycle counting options, see *Cycle Count Control Register* on page 3-24.
[3]	BB	Branch broadcast mode: 0 Branch broadcast mode disabled. 1 Branch broadcast mode trace. For more branch broadcast mode options, see *Branch Broadcast Control Register* on page 3-24.
[2:1]	INSTP0	RES0, only branches are P0 instructions.
[0]	-	RES1.

3.4.5 Event Control 0 Register

The TRCEVENTCTL0R characteristics are:

Purpose Controls the tracing of events in the trace streams. The events also drive the external outputs from the ETM-M7.

Usage constraints This register must always be programmed as part of the trace unit initialization.

Only accepts writes when the trace unit is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-6 shows the TRCEVENTCTL0R bit assignments.

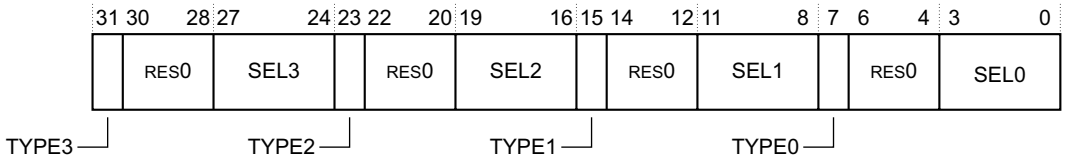


Figure 3-6 TRCEVENTCTL0R bit assignments

Table 3-17 shows the TRCEVENTCTL0R bit assignments.

Table 3-17 TRCEVENTCTL0R bit assignments

Bits	Name	Function
[31]	TYPE3[a]	Selects the resource type for event 3: 0 Single selected resource. 1 Boolean combined resource pair.
[30:28]	-	RES0.
[27:24]	SEL3[a]	Selects the resource number, based on the value of TYPE3: When TYPE3 is 0, selects a single selected resource from 0-15 defined by SEL3[3:0]. When TYPE3 is 1, selects a Boolean combined resource pair from 0-7 defined by SEL3[2:0].
[23]	TYPE2[a]	Selects the resource type for event 2: 0 Single selected resource. 1 Boolean combined resource pair.
[22:20]	-	RES0.
[19:16]	SEL2[a]	Selects the resource number, based on the value of TYPE2: When TYPE2 is 0, selects a single selected resource from 0-15 defined by SEL2[3:0]. When TYPE2 is 1, selects a Boolean combined resource pair from 0-7 defined by SEL2[2:0].
[15]	TYPE1	Selects the resource type for event 1: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RES0.
[11:8]	SEL1	Selects the resource number, based on the value of TYPE1: When TYPE1 is 0, selects a single selected resource from 0-15 defined by SEL1[3:0]. When TYPE1 is 1, selects a Boolean combined resource pair from 0-7 defined by SEL1[2:0].

Table 3-17 TRCEVENTCTL0R bit assignments (continued)

Bits	Name	Function
[7]	TYPE0	Selects the resource type for event 0: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	SEL0	Selects the resource number, based on the value of TYPE0: When TYPE0 is 0, selects a single selected resource from 0-15 defined by SEL0[3:0]. When TYPE0 is 1, selects a Boolean combined resource pair from 0-7 defined by SEL0[2:0].

a. Not present in instruction trace only configuration, this field is RES0.

3.4.6 Event Control 1 Register

The TRCEVENTCTL1R characteristics are:

Purpose Controls the how the events selected by TRCEVENTCTL0R behave. See *Event Control 0 Register* on page 3-18.

Usage constraints This register must always be programmed as part of the trace unit initialization.

Only accepts writes when the trace unit is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-7 shows the TRCEVENTCTL1R bit assignments.

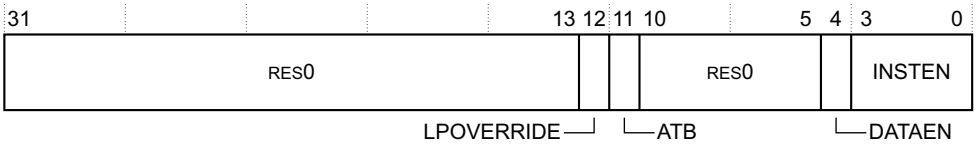


Figure 3-7 TRCEVENTCTL1R bit assignments

Table 3-18 shows the TRCEVENTCTL1R bit assignments.

Table 3-18 TRCEVENTCTL1R bit assignments

Bits	Name	Function
[31:13]	-	RES0.
[12]	LPOVERRIDE	Low power state behavior override: 0 Low power state behavior unaffected. 1 Low power state behavior overridden. The resources and Event trace generation are unaffected by entry to a low power state.
[11]	ATB	ATB trigger enable: 0 ATB trigger disabled. 1 ATB trigger enabled.

Table 3-18 TRCEVENTCTL1R bit assignments (continued)

Bits	Name	Function
[10:5]	-	RES0.
[4]	DATAEN[a]	Enables generation of an event element in the data trace stream when the selected event occurs: 0 Event does not cause an event element. 1 Event causes an event element.
[3:0]	INSTEN	One bit per event, to enable generation of an event element in the instruction trace stream when the selected event occurs: 0 Event does not cause an event element. 1 Event causes an event element.

a. Not present in instruction trace only configuration, this field is RES0.

3.4.7 Stall Control Register

The TRCSTALLCTLR characteristics are:

Purpose Enables trace unit functionality that prevents trace unit buffer overflows.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must always be programmed as part of the trace unit initialization.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-8 shows the TRCSTALLCTLR bit assignments.

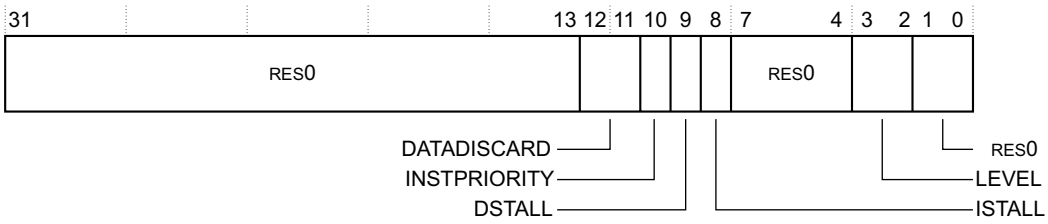


Figure 3-8 TRCSTALLCTLR bit assignments

Table 3-19 shows the TRCSTALLCTLR bit assignments.

Table 3-19 TRCSTALLCTLR bit assignments

Bits	Name	Function
[31:13]	-	RES0.
[12:11]	DATADISCARD[a]	Sets the priority of data trace components, enabling the ETM-M7 to discard some data if the data trace buffer space is less than LEVEL: 0b00 The trace unit must not discard any data trace elements. 0b01 The trace unit can discard P1 and P2 elements associated with data loads. 0b10 The trace unit can discard P1 and P2 elements associated with data stores. 0b11 The trace unit can discard P1 and P2 elements associated with both data loads and stores.
[10]	INSTPRIORITY[a]	Prioritize instruction trace if instruction trace buffer space is less than LEVEL: 0 The trace unit must not prioritize instruction trace. 1 The trace unit can prioritize instruction trace.
[9]	DSTALL[a]	Stall processor based on data trace buffer space: 0 The trace unit must not stall the processor. 1 The trace unit can stall the processor.
[8]	ISTALL	Stall processor based on instruction trace buffer space: 0 The trace unit must not stall the processor. 1 The trace unit can stall the processor.
[7:4]	-	RES0.
[3:2]	LEVEL	Threshold at which stalling becomes active. This provides four levels. This level can be varied to optimize the level of invasion caused by stalling, balanced against the risk of a FIFO overflow: 0b00 Zero invasion. This setting has a greater risk of a FIFO overflow. 0b11 Maximum invasion occurs but there is less risk of a FIFO overflow. **Note** If LEVEL is nonzero then a trace unit might suppress the generation of: • Global timestamps in the instruction trace stream and the data trace stream. • Cycle counting in the instruction trace stream, although the cumulative cycle count remains correct.
[1:0]	-	RES0.

a. Not present in instruction trace only configuration, this field is RES0.

3.4.8 Global Timestamp Control Register

The TRCTSCTLR characteristics are:

Purpose Controls the insertion of global timestamps into the trace streams. A timestamp is always inserted into the instruction trace stream, and also in the data trace stream if any data tracing is enabled.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must always be programmed as part of the trace unit initialization.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-9 shows the TRCTSCTLR bit assignments.

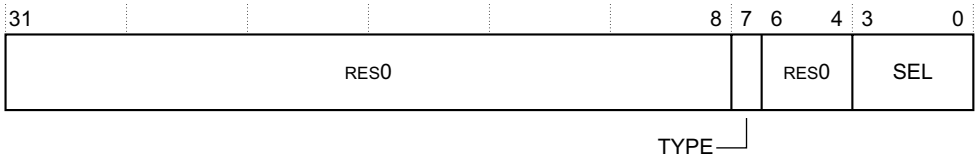


Figure 3-9 TRCTSCTLR bit assignments

Table 3-20 shows the TRCTSCTLR bit assignments.

Table 3-20 TRCTSCTLR bit assignments

Bits	Name	Function
[31:8]	-	RES0.
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.9 Synchronization Period Register

The TRCSYNCPR characteristics are:

Purpose Specifies the period of trace synchronization of the trace streams. TRCSYNCPR defines a number of bytes of trace between requests for trace synchronization. This value is always a power of two.

Usage constraints Only accepts writes when the trace unit is disabled.

If TRCIDR3.SYNCPR is 0 then the register is a RW register and the register must be programmed.

If TRCIDR3.SYNCPR is 1 then the register is RO and the synchronization period, given in PERIOD, is `0b01010`.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-10 shows the TRCSYNCPR bit assignments.

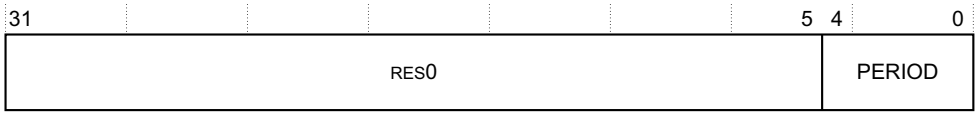


Figure 3-10 TRCSYNCPR bit assignments

Table 3-21 shows the TRCSYNCPR bit assignments.

Table 3-21 TRCSYNCPR bit assignments

Bits	Name	Function
[31:5]	-	RES0.
[4:0]	PERIOD	Defines the number of bytes of trace between trace synchronization requests as a total of the number of bytes generated by both the instruction and data streams. The number of bytes is 2^N where N is the value of this field: • A value of zero disables these periodic trace synchronization requests, but does not disable other trace synchronization requests. • The minimum value that can be programmed, other than zero, is 8, providing a minimum trace synchronization period of 256 bytes. • The maximum value is 20, providing a maximum trace synchronization period of 2^{20} bytes.

3.4.10 Cycle Count Control Register

The TRCCCCTLR characteristics are:

Purpose Sets the threshold value for instruction trace cycle counting. The threshold represents the minimum interval between cycle count trace packets.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must always be programmed as part of the trace unit initialization.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-11 shows the TRCCCCTLR bit assignments.

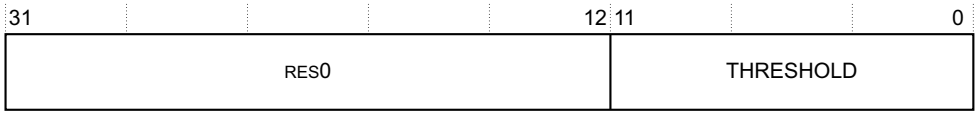


Figure 3-11 TRCCCCTLR bit assignments

Table 3-22 shows the TRCCCCTLR bit assignments.

Table 3-22 TRCCCCTLR bit assignments

Bits	Name	Function
[31:12]	-	RES0
[11:0]	THRESHOLD	Instruction trace cycle count threshold

3.4.11 Branch Broadcast Control Register

The TRCBBCTLR characteristics are:

Purpose Controls how branch broadcasting behaves, and enables branch broadcasting to be enabled for certain memory regions.

Usage constraints Only accepts writes when the trace unit is disabled.

Reads as zero in instruction trace configuration.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-12 shows the TRCBBCTLR bit assignments.

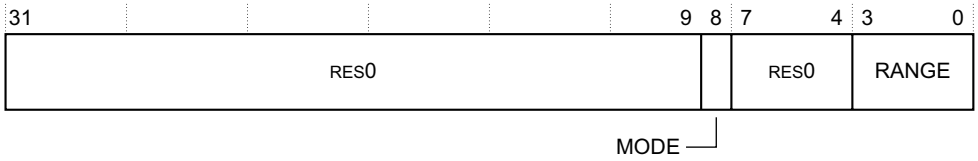


Figure 3-12 TRCBBCTLR bit assignments

Table 3-23 shows the TRCBBCTLR bit assignments.

Table 3-23 TRCBBCTLR bit assignments

Bits	Name	Function
[31:9]	-	RES0.
[8]	MODE	Selects mode: `0` Exclude mode. The Address Range Comparators defined by the RANGE field indicate address ranges where branch broadcasting is not enabled. Selecting no ranges results in branch broadcasting being enabled over the whole memory map. `1` Include mode. The Address Range Comparators defined by the RANGE field indicate address ranges where branch broadcasting is enabled. Setting RANGE to all zeroes is UNPREDICTABLE when in Include mode.
[7:4]	-	RES0.
[3:0]	RANGE	Selects Address Range Comparators to control where branch broadcasting is enabled. One bit is provided for each implemented Address Range Comparator.

3.4.12 Trace ID Register

The TRCTRACEIDR characteristics are:

Purpose Sets the trace ID on the trace bus. Controls two trace IDs, one for instruction trace and one for data trace.

Usage constraints In a CoreSight system, writing of reserved trace ID values, `0x00` and `0x70-0x7F`, is UNPREDICTABLE. This register must always be programmed as part of the trace unit initialization.

Only accepts writes when the trace unit is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-9.

Figure 3-13 on page 3-26 shows the TRCTRACEIDR bit assignments.

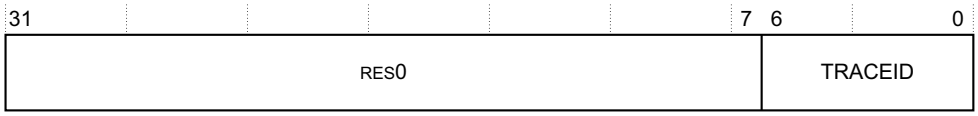


Figure 3-13 TRCTRACEIDR bit assignments

Table 3-24 shows the TRCTRACEIDR bit assignments.

Table 3-24 TRCTRACEIDR bit assignments

Bits	Name	Function
[31:7]	-	RES0.
[6:0]	TRACEID	Trace ID value. When only instruction tracing is enabled, this provides the trace ID. When data tracing is enabled, this field must be written with bit[0] set to 0. The instruction and data trace streams use adjacent trace ID values: • The instruction trace stream uses the trace ID {[6:1],0}. • The data value trace stream uses the trace ID {[6:1],1}.

3.4.13 ViewInst Main Control Register

The TRCVICTLR characteristics are:

Purpose Controls instruction trace filtering.

Usage constraints Only accepts writes when the trace unit is disabled.

Only returns stable data when TRCSTATR.PMSTABLE is 1.

Must be programmed, particularly to set the value of the SSSTATUS bit, that sets the state of the start-stop logic.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-14 shows the TRCVICTLR bit assignments.

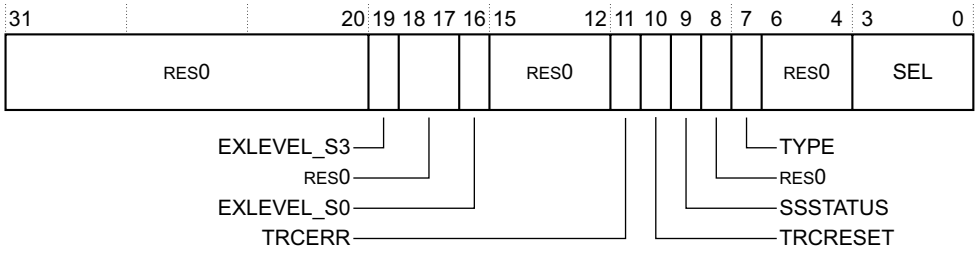


Figure 3-14 TRCVICTLR bit assignments

Table 3-25 shows the TRCVICTLR bit assignments.

Table 3-25 TRCVICTLR bit assignments

Bits	Value	Function
[31:20]	-	RES0.
[19]	EXLEVEL_S3	Disables tracing in the specified exception level in Secure state for exception level 3. 0 Enable ViewInst in this exception level. 1 Disable ViewInst in this exception level.
[18:17]	-	RES0.
[16]	EXLEVEL_S0	Disables tracing in the specified exception level in Secure state for exception level 0. 0 Enable ViewInst in this exception level. 1 Disable ViewInst in this exception level.
[15:12]	-	RES0.
[11]	TRCERR	Selects whether a system error exception must always be traced: 0 System error exception is traced only if the instruction or exception immediately before the system error exception is traced. 1 System error exception is always traced regardless of the value of ViewInst.
[10]	TRCRESET	Selects whether a reset exception must always be traced: 0 Reset exception is traced only if the instruction or exception immediately before the reset exception is traced. 1 Reset exception is always traced regardless of the value of ViewInst.
[9]	SSSTATUS	Indicates the current status of the start/stop logic: 0 Start/stop logic is in the stopped state. 1 Start/stop logic is in the started state.
[8]	-	RES0.
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.14 ViewInst Include/Exclude Control Register

The TRCVIIECTLR characteristics are:

Purpose Defines the address range comparators that control the ViewInst Include/Exclude control.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must be programmed in instruction and data trace configuration

Configurations Available in instruction and data trace configuration only.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-15 shows the TRCVIIECTLR bit assignments.

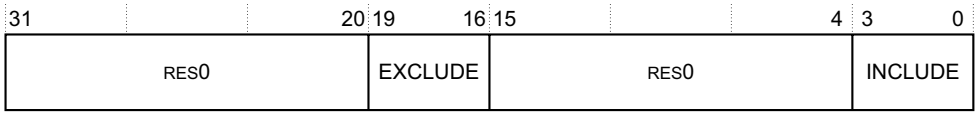


Figure 3-15 TRCVIIECTLR bit assignments

Table 3-26 shows the TRCVIIECTLR bit assignments.

Table 3-26 TRCVIIECTLR bit assignments

Bits	Name	Function
[31:20]	-	RES0.
[19:16]	EXCLUDE	Defines the address range comparators for ViewInst exclude control. One bit is provided for each implemented Address Range Comparator.
[15:4]	-	RES0.
[3:0]	INCLUDE	Defines the address range comparators for ViewInst include control. Selecting no include comparators indicates that all instructions must be included. The exclude control indicates which ranges must be excluded. One bit is provided for each implemented Address Range Comparator.

3.4.15 ViewInst Start-Stop Processor Comparator Control Register

The TRCVIPCSSCTLR characteristics are:

Purpose Use this to set, or read, which processor comparator inputs can control the ViewInst start-stop logic.

Usage constraints

- Only accepts writes when the trace unit is disabled.
- This register must be programmed.
- CONSTRAINED UNPREDICTABLE behavior of the start-stop logic occurs if a single processor comparator input is programmed as both a stop resource and a start resource. That is, the start/stop logic is either active or inactive for the instruction and the start/stop logic is either active or inactive after the instruction.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-16 shows the TRCVIPCSSCTLR bit assignments.

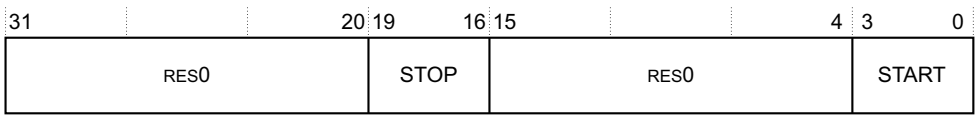


Figure 3-16 TRCVIPCSSCTLR bit assignments

Table 3-28 shows the TRCVIPCSSCTLR bit assignments.

Table 3-27 TRCVIPCSSCTLR bit assignments

Bits	Name	Function
[31:20]	-	RES0.
[19:16]	STOP	Selects which processor comparator inputs are in use with ViewInst start-stop control, for the purpose of stopping trace. One bit is provided for each processor comparator input.
[15:4]	-	RES0.
[3:0]	START	Selects which processor comparator inputs are in use with ViewInst start-stop control, for the purpose of starting trace. One bit is provided for each implemented processor comparator input.

3.4.16 ViewInst Start/Stop Control Register

The TRCVISSCTLR characteristics are:

Purpose Defines the single address comparators that control the ViewInst Start/Stop logic.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must always be programmed as part of the trace unit initialization.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-17 shows the TRCVISSCTLR bit assignments.

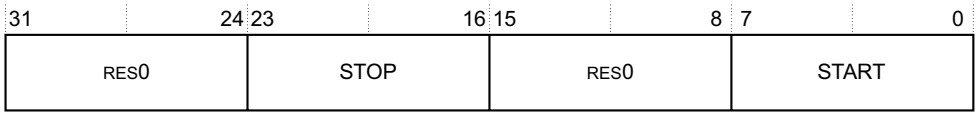


Figure 3-17 TRCVISSCTLR bit assignments

Table 3-28 shows the TRCVISSCTLR bit assignments.

Table 3-28 TRCVISSCTLR bit assignments

Bits	Name	Function
[31:24]	-	RES0.
[23:16]	STOP	Defines the single address comparators to stop trace with the ViewInst Start/Stop control. One bit is provided for each implemented single address comparator.
[15:8]	-	RES0.
[7:0]	START	Defines the single address comparators to start trace with the ViewInst Start/Stop control. One bit is provided for each implemented single address comparator.

3.4.17 ViewData Main Control Register

The TRCVDCTLR characteristics are:

Purpose Controls data trace filtering.

Usage constraints Only accepts writes when the trace unit is disabled.

This register must be programmed when data tracing is enabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-18 shows the TRCVDCTLR bit assignments.

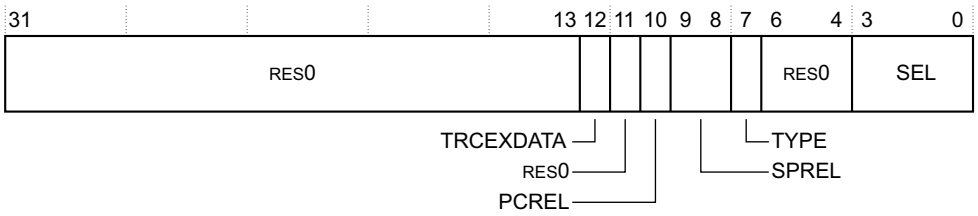


Figure 3-18 TRCVDCTLR bit assignments

Table 3-29 shows the TRCVDCTLR bit assignments.

Table 3-29 TRCVDCTLR bit assignments

Bits	Name	Function
[31:13]	-	RES0.
[12]	TRCEXDATA	Controls the tracing of data transfers for exceptions and exception returns: 0 Exception and exception return data transfers are not traced. 1 Exception and exception return data transfers are traced if the other aspects of ViewData indicate that the data transfers must be traced.
[11]	-	RES0.
[10]	PCREL	Controls tracing of data for transfers that are relative to the *Program Counter* (PC): 0 Tracing of PC-relative transfers is unaffected. 1 Do not trace either the address or value portions of PC-relative transfers.
[9:8]	SPREL	Controls tracing of data for transfers that are relative to the *Stack Pointer* (SP): 0b00 Tracing of SP-relative transfers is unaffected. 0b01 Reserved. 0b10 Do not trace the address portion of SP-relative transfers. A P1 data address element is generated if data value tracing is enabled. 0b11 Do not trace either the address or value portions of SP-relative transfers.

Table 3-29 TRCVDCTLR bit assignments (continued)

Bits	Name	Function
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.18 ViewData Include/Exclude Single Address Comparator Register

The TRCVDSACCTLR characteristics are:

Purpose Defines the single address comparators that control the ViewData Include/Exclude control.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-19 shows the TRCVDSACCTLR bit assignments.

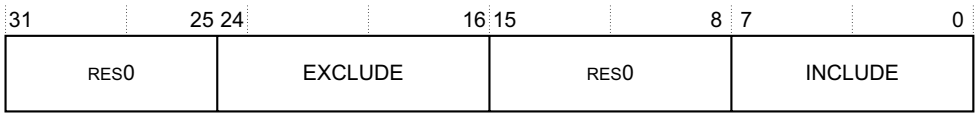


Figure 3-19 TRCVDSACCTLR bit assignments

Table 3-30 shows the TRCVDSACCTLR bit assignments.

Table 3-30 TRCVDSACCTLR bit assignments

Bits	Name	Function
[31:25]	-	RES0.
[24:16]	EXCLUDE	Defines the single address comparators for ViewData exclude control. One bit is provided for each implemented address comparator.
[15:8]	-	RES0.
[7:0]	INCLUDE	Defines the single address comparators for ViewData include control. One bit is provided for each implemented address comparator.

3.4.19 ViewData Include/Exclude Address Range Comparator Register

The TRCVDARCCTLR characteristics are:

Purpose Defines the address range comparators that control the ViewData Include/Exclude control.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-10.

Figure 3-20 shows the TRCVDARCCTLR bit assignments.

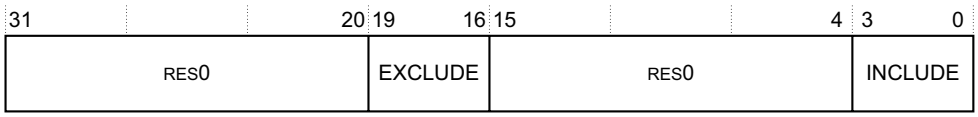


Figure 3-20 TRCVDARCCTLR bit assignments

Table 3-31 shows the TRCVDARCCTLR bit assignments.

Table 3-31 TRCVDARCCTLR bit assignments

Bits	Name	Function
[31:20]	-	RES0.
[19:16]	EXCLUDE	Defines the address range comparators for ViewData exclude control. One bit is provided for each implemented address range comparator.
[15:4]	-	RES0.
[3:0]	INCLUDE	Defines the address range comparators for ViewData include control. One bit is provided for each implemented address range comparator.

3.4.20 Sequencer State Transition Control Registers 0-2

The TRCSEQEVRn characteristics are:

Purpose Defines the sequencer transitions that progress to the next state or backwards to the previous state. The ETM-M7 implements a sequencer state machine with up to four states.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-21 shows the TRCSEQEVRn bit assignments.

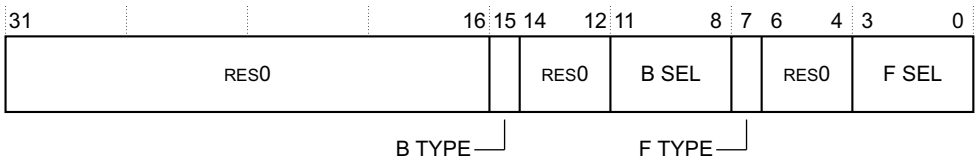


Figure 3-21 TRCSEQEVRn bit assignments

Table 3-32 shows the TRCSEQEVRn bit assignments.

Table 3-32 TRCSEQEVRn bit assignments

Bits	Name	Function
[31:16]	-	RES0.
[15]	B TYPE	Selects the resource type to move backwards to this state from the next state: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RES0.
[11:8]	B SEL	Selects the resource number, based on the value of B TYPE: When B TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When B TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[7]	F TYPE	Selects the resource type to move forwards from this state to the next state: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	F SEL	Selects the resource number, based on the value of F TYPE: When F TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When F TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.21 Sequencer Reset Control Register

The TRCSEQRSTEVR characteristics are:

Purpose Resets the sequencer to state 0.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-22 shows the TRCSEQRSTEVR bit assignments.

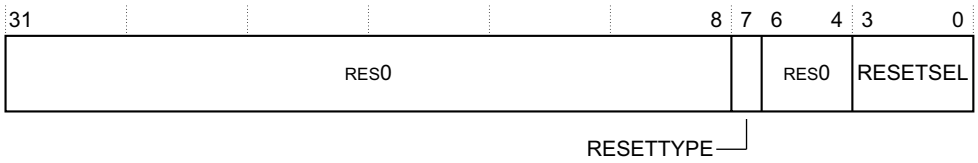


Figure 3-22 TRCSEQRSTEVR bit assignments

Table 3-33 shows the TRCSEQRSTEVR bit assignments.

Table 3-33 TRCSEQRSTEVR bit assignments

Bits	Name	Function
[31:8]	-	RES0.
[7]	RESETTYPE	Selects the resource type to move back to state 0: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	RESETSEL	Selects the resource number, based on the value of RESETTYPE: When RESETTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When RESETTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.22 Sequencer State Register

The TRCSEQSTR characteristics are:

Purpose Holds the value of the current state of the sequencer.

Usage constraints Only accepts writes when the trace unit is disabled.

Must be programmed with an initial value when programming the sequencer.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-23 shows the TRCSEQSTR bit assignments.

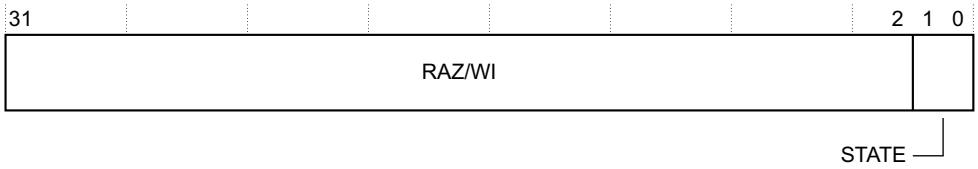


Figure 3-23 TRCSEQSTR bit assignments

Table 3-34 shows the TRCSEQSTR bit assignments.

Table 3-34 TRCSEQSTR bit assignments

Bits	Name	Function
[31:2]	-	RES0.
[1:0]	STATE	Current sequencer state: 0b00 State 0. 0b01 State 1. 0b10 State 2. 0b11 State 3.

3.4.23 Counter Reload Value Registers 0-1

The TRCCNTRLDVRn characteristics are:

Purpose Defines the reload value for the counter.

Usage constraints Only accepts writes when the trace unit is disabled.

The count value is only stable when TRCSTATR.PMSTABLE is 1.

If software uses counter <n> then it must write to this register to set the counter reload value.

Configurations TRCCNTRLDVR0 available in all configurations.

TRCCNTRLDVR1 available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-24 shows the TRCCNTRLDVRn bit assignments.

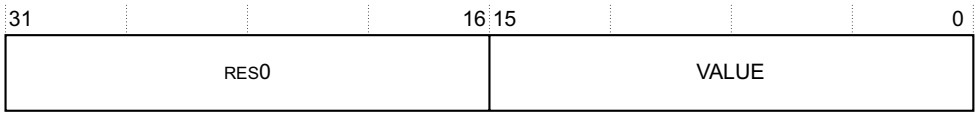


Figure 3-24 TRCCNTRLDVRn bit assignments

Table 3-35 shows the TRCCNTRLDVRn bit assignments.

Table 3-35 TRCCNTRLDVRn bit assignments

Bits	Value	Function
[31:16]	-	RES0.
[15:0]	VALUE	Defines the reload value for the counter. This value is loaded into the counter each time the reload event occurs.

3.4.24 Counter Control Registers 0-1

The TRCCNTCTLRn characteristics are:

Purpose Controls the counter.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-25 on page 3-36 shows the TRCCNTCTLRn bit assignments.

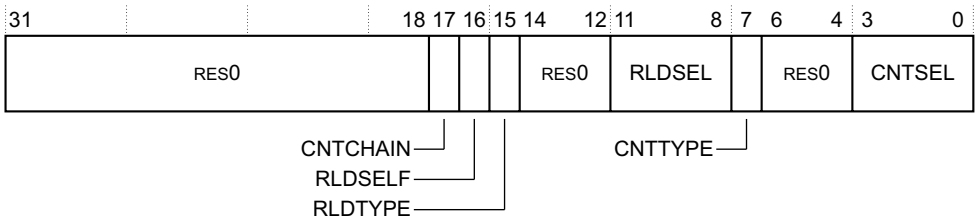


Figure 3-25 TRCCNTCTLRn bit assignments

Table 3-36 shows the TRCCNTCTLRn bit assignments.

Table 3-36 TRCCNTCTLRn bit assignments

Bits	Name	Function
[31:18]	-	RES0.
[17]	CNTCHAIN[a]	Defines whether the counter decrements when the counter reloads. This enables two counters to be used in combination to provide a larger counter: 0 The counter operates independently from the counter. The counter only decrements based on CNTTYPE and CNTSEL. 1 The counter decrements when the counter reloads. The counter also decrements when the resource selected by CNTTYPE and CNTSEL is active.
[16]	RLDSELF	Defines whether the counter reloads when it reaches zero: 0 The counter does not reload when it reaches zero. The counter only reloads based on RLDTYPE and RLDSEL. 1 The counter reloads when it reaches zero and the resource selected by CNTTYPE and CNTSEL is also active. The counter also reloads based on RLDTYPE and RLDSEL.
[15]	RLDTYPE	Selects the resource type for the reload: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RES0.
[11:8]	RLDSEL	Selects the resource number, based on the value of RLDTYPE: When RLDTYPE is 0, selects a single selected resource from 0-15 defined by RLDSEL[3:0]. When RLDTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by RLDSEL[2:0].
[7]	CNTTYPE	Selects the resource type for the counter: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RES0.
[3:0]	CNTSEL	Selects the resource number, based on the value of CNTTYPE: When CNTTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When CNTTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

a. Only present on TRCCNTCTLR1.

3.4.25 Counter Value Registers 0-1

The TRCCNTVRn characteristics are:

Purpose This sets or returns the value of counter <n>.

Usage constraints Only accepts writes when the trace unit is disabled.

Must be programmed with an initial value when programming the counter.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-10.

Figure 3-26 shows the TRCCNTVRn bit assignments.

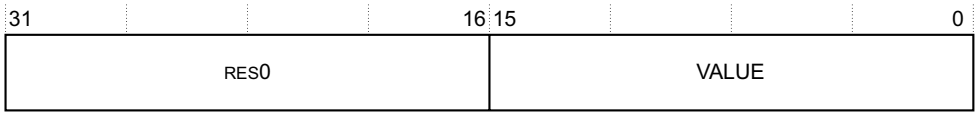


Figure 3-26 TRCCNTVRn bit assignments

Table 3-37 shows the TRCCNTVRn bit assignments.

Table 3-37 TRCCNTVRn bit assignments

Bits	Value	Function
[31:16]	-	RES0.
[15:0]	VALUE	Contains the current counter value.

3.4.26 ID Register 8-13

The TRCIDRn characteristics are:

Purpose Indicate information about the implemented trace streams that are required to analyze the trace.

Usage constraints There are no usage constraints.

Configurations These registers are available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-27 shows the TRCIDR8 bit assignments.

Figure 3-27 TRCIDR8 bit assignments

Table 3-38 shows the TRCIDR8 bit assignments.

Table 3-38 TRCIDR8 bit assignments

Bits	Name	Function
[31:0]	MAXSPEC	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements that have not been committed in the trace stream at any one time. `0x00000001` Maximum trace speculation depth is one.

Figure 3-28 on page 3-38 shows the TRCIDR9 bit assignments.

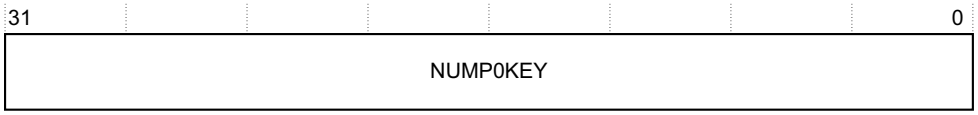


Figure 3-28 TRCIDR9 bit assignments

Table 3-39 shows the TRCIDR9 bit assignments.

Table 3-39 TRCIDR9 bit assignments

Bits	Name	Function
[31:0]	NUMP0KEY	Indicates the number of P0 right-hand keys that are used: `0x00000000` No P0 keys used in instruction trace only configuration. `0x00000020` The instruction and data trace configuration supports 32 P0 keys.

Figure 3-29 shows the TRCIDR10 bit assignments.

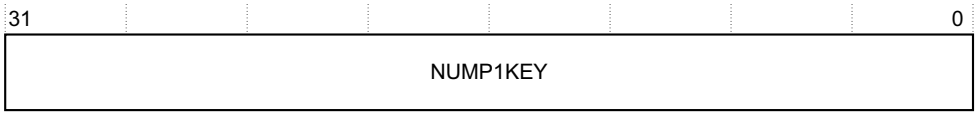


Figure 3-29 TRCIDR10 bit assignments

Table 3-40 shows the TRCIDR10 bit assignments.

Table 3-40 TRCIDR10 bit assignments

Bits	Name	Function
[31:0]	NUMP1KEY	Indicates the total number of P1 right-hand keys, including normal and special keys: `0x00000000` No P1 right-hand keys used in instruction trace only configuration. `0x00000002` The instruction and data trace configuration supports 2 P1 right-hand keys.

Figure 3-30 shows the TRCIDR11 bit assignments.

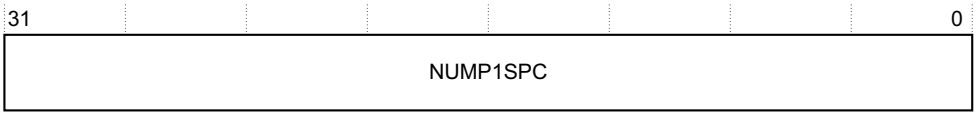


Figure 3-30 TRCIDR11 bit assignments

Table 3-41 shows the TRCIDR11 bit assignments.

Table 3-41 TRCIDR11 bit assignments

Bits	Name	Function
[31:0]	NUMP1SPC	Indicates the number of special P1 right-hand keys. `0x00000000` No special P1 right-hand keys used in any configuration.

Figure 3-31 on page 3-39 shows the TRCIDR12 bit assignments.

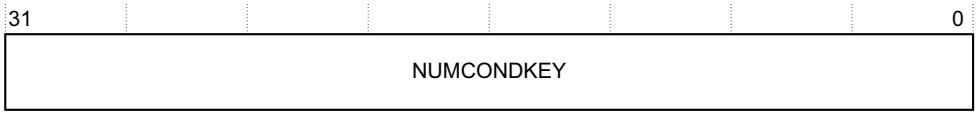


Figure 3-31 TRCIDR12 bit assignments

Table 3-42 shows the TRCIDR12 bit assignments.

Table 3-42 TRCIDR12 bit assignments

Bits	Name	Function
[31:0]	NUMCONDKEY	Indicates the total number of conditional instruction right-hand keys, including normal and special keys: 0x00000001 One conditional instruction right-hand key implemented.

Figure 3-32 shows the TRCIDR13 bit assignments.

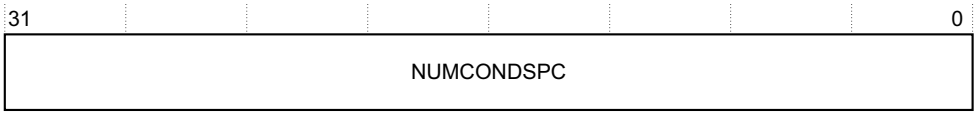


Figure 3-32 TRCIDR13 bit assignments

Table 3-43 shows the TRCIDR13 bit assignments.

Table 3-43 TRCIDR13 bit assignments

Bits	Name	Function
[31:0]	NUMCONDSPC	This indicates the number of special conditional instruction right-hand keys. 0x00000000 No special conditional instruction right-hand keys implemented.

3.4.27 Implementation Specific Register 0

The TRCIMSPEC0 characteristics are:

Purpose Shows the presence of any IMPLEMENTATION SPECIFIC features, and enables any features that are provided.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-33 shows the TRCIMSPEC0 bit assignments.

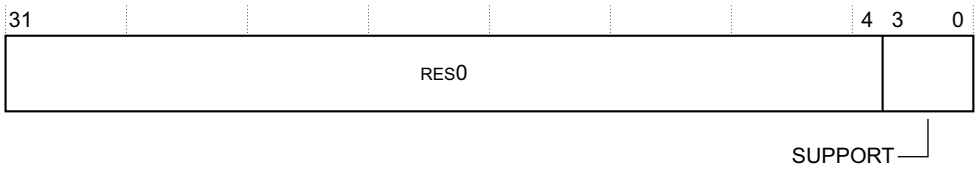


Figure 3-33 TRCIMSPEC0 bit assignments

Table 3-44 shows the TRCIMSPEC0 bit assignments.

Table 3-44 TRCIMSPEC0 bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3:0]	SUPPORT	Set to 0. No IMPLEMENTATION SPECIFIC extensions are supported.

3.4.28 ID Register 0

The TRCIDR0 characteristics are:

Purpose Indicates the tracing capabilities of the ETM-M7 for the:

- Instruction trace only configuration.
- Instruction and data trace configuration.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-34 shows the TRCIDR0 bit assignments.

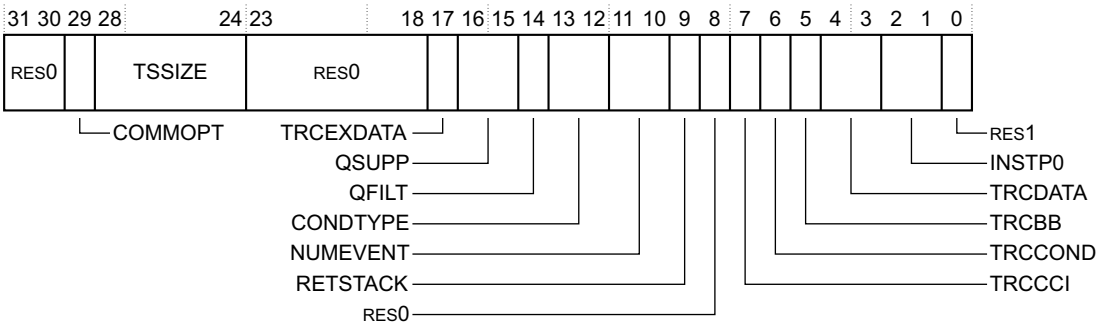


Figure 3-34 TRCIDR0 bit assignments

Table 3-45 shows the TRCIDR0 bit assignments.

Table 3-45 TRCIDR0 bit assignments

Bits	Name	Function
[31:30]	-	RES0.
[29]	COMMOPT	Indicates the meaning of the commit field in some packets: 0b0 Commit mode 0.
[28:24]	TSSIZE	Global timestamp size: 0b01000 Maximum of 64-bit global timestamp implemented.
[23:18]	-	RES0.
[17]	TRCEXDATA	Indicates support for the tracing of data transfers for exceptions and exception returns: 0b0 TRCVDCTLR.TRCEXDATA is not implemented. 0b1 TRCVDCTLR.TRCEXDATA is implemented.

Table 3-45 TRCIDR0 bit assignments (continued)

Bits	Name	Function
[16:15]	QSUPP	Indicates Q element support: 0b00 Q elements not supported.
[14]	QFILT	RES0.
[13:12]	CONDTYPE	Indicates how conditional results are traced: 0b00 The trace unit indicates only if a conditional instruction passes or fails its condition code check.
[11:10]	NUMEVENT	Number of events supported in the trace: 0b11 Four events supported for instruction and data configuration. 0b01 Two events supported for instruction only configuration.
[9]	RETSTACK	Return stack support: 1 2 entry return stack implemented.
[8]	-	RES0.
[7]	TRCCCI	Support for cycle counting in the instruction trace: 1 Cycle counting in the instruction trace is implemented.
[6]	TRCCOND	Support for conditional instruction tracing: 1 Conditional instruction tracing is implemented.
[5]	TRCBB	Support for branch broadcast tracing: 1 Branch broadcast tracing is implemented.
[4:3]	TRCDATA	Support for tracing of data: 0b00 Data tracing is not supported in the instruction trace only configuration. 0b11 Tracing of data addresses and data values is supported in the instruction and data trace configuration.
[2:1]	INSTP0	Support for tracing of load and store instructions as P0 elements: 0b00 Tracing of load and store instructions as P0 elements is not supported in the instruction trace only configuration. 0b11 Tracing of load and store instructions as P0 elements is supported in the instruction and data trace configuration.
[0]	-	RES1.

3.4.29 ID Register 1

The TRCIDR1 characteristics are:

Purpose Indicates the basic architecture of the ETM-M7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-35 on page 3-42 shows the TRCIDR1 bit assignments.

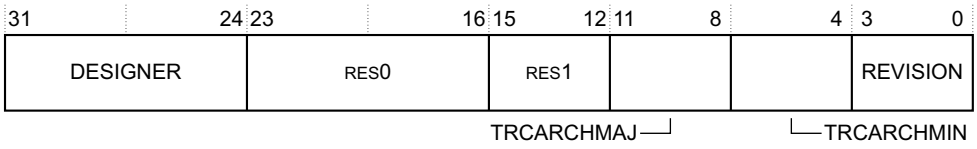


Figure 3-35 TRCIDR1 bit assignments

Table 3-46 shows the TRCIDR1 bit assignments.

Table 3-46 TRCIDR1 bit assignments

Bits	Name	Function
[31:24]	DESIGNER	Indicates the designer of the trace unit: 0x41 ARM.
[23:16]	-	RES0.
[15:12]	-	RES1.
[11:8]	TRCARCHMAJ	Major trace unit architecture version number: 0b0100 ETMv4.
[7:4]	TRCARCHMIN	Minor trace unit architecture version number: 0b0000 Minor revision 0.
[3:0]	REVISION	Implementation revision number: 0b0001 Implementation revision 1.

3.4.30 ID Register 2

The TRCIDR2 characteristics are:

Purpose Indicates the maximum sizes of certain aspects of items in the trace.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-36 shows the TRCIDR2 bit assignments.

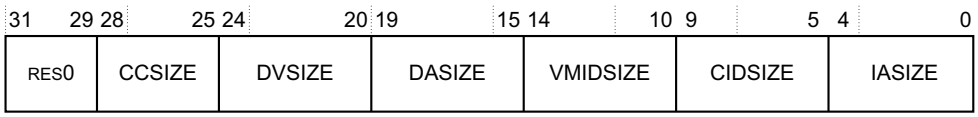


Figure 3-36 TRCIDR2 bit assignments

Table 3-47 shows the TRCIDR2 bit assignments.

Table 3-47 TRCIDR2 bit assignments

Bits	Name	Function
[31:29]	-	RES0.
[28:25]	CCSIZE	Indicates the size of the cycle counter in bits minus 12: 0b0000 Cycle count is 12 bits.
[24:20]	DVSIZE	Data value size in bytes: 0b00000 Data value size not supported in instruction trace only configuration. 0b00100 Maximum of 32-bit data value size is supported in instruction and data trace configuration.
[19:15]	DASIZE	Data address size in bytes: 0b00000 Data address size not supported in instruction trace only configuration. 0b00100 Maximum of 32-bit address size is supported in instruction and data trace configuration.
[14:10]	VMIDSIZE	Virtual Machine ID size: 0b00000 Virtual Machine ID tracing not implemented.
[9:5]	CIDSIZE	Context ID tracing: 0b00000 Context ID tracing not implemented.
[4:0]	IASIZE	Instruction address size : 0b00100 Maximum of 32-bit address size.

3.4.31 ID Register 3

The TRCIDR3 characteristics are:

Purpose Indicates certain aspects of the ETM-M7 configuration.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-37 shows the TRCIDR3 bit assignments.

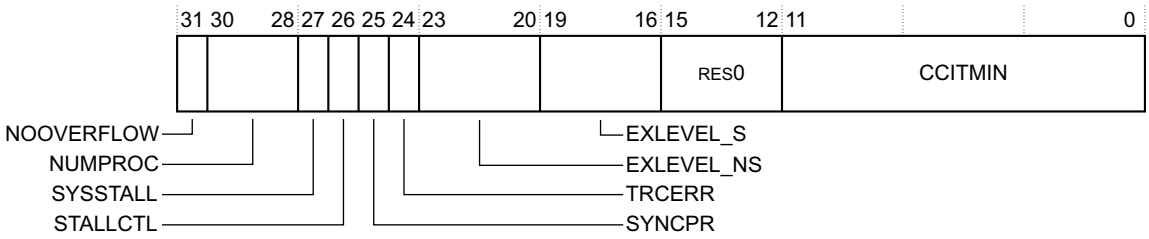


Figure 3-37 TRCIDR3 bit assignments

Table 3-48 shows the TRCIDR3 bit assignments.

Table 3-48 TRCIDR3 bit assignments

Bits	Name	Function
[31]	NOOVERFLOW	Indicates whether TRCSTALLCTLR.NOOVERFLOW is implemented: 0 NOOVERFLOW is not implemented.
[30:28]	NUMPROC	Indicates the number of processors available for tracing. This is driven from the ETM **NUMPROC** input pin, reflecting system implementation: 0b000 The trace unit can trace one processor, and is the fixed value in the instruction trace configuration. 0b001 The trace unit can trace two processors. 0b010 The trace unit can trace three processors. 0b011 The trace unit can trace four processors.
[27]	SYSSTALL	System support for stall control of the processor. This is driven from the ETM **SYSSTALL** input pin, reflecting the system implementation: 0 System does not support stall control of the processor. 1 System supports stall control of the processor. This field is used in conjunction with STALLCTL. Only when both SYSSTALL and STALLCTL are 0b1 does the system support stalling of the processor.
[26]	STALLCTL	Stall control support: 1 TRCSTALLCTLR is implemented.
[25]	SYNCPR	Indicates trace synchronization period support: 0 TRCSYNCPR is read/write for instruction and data trace configuration. Software can change the synchronization period. 1 TRCSYNCPR is read-only for instruction trace only configuration. The trace synchronization period is fixed.
[24]	TRCERR	Indicates whether TRCVICTLR.TRCERR is implemented: 1 TRCERR is implemented.
[23:20]	EXLEVEL_NS	RES0.
[19:16]	EXLEVEL_S	Privilege levels implemented. One bit for each level. 0b1001 Privilege levels Thread and Handler are implemented.
[15:12]	-	RES0.
[11:0]	CCITMIN	Instruction trace cycle counting minimum threshold: 0x4 Minimum threshold is 4 instruction trace cycle.

3.4.32 ID Register 4

The TRCIDR4 characteristics are:

Purpose Indicates the resources available in the ETM-M7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-38 on page 3-45 shows the TRCIDR4 bit assignments.

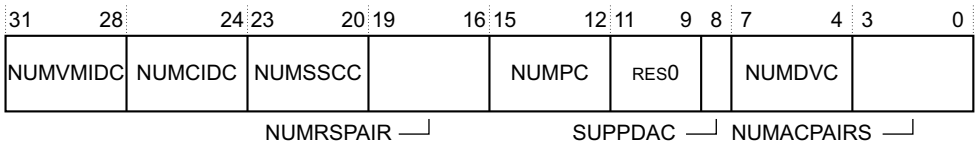


Figure 3-38 TRCIDR4 bit assignments

Table 3-49 shows the TRCIDR4 bit assignments.

Table 3-49 TRCIDR4 bit assignments

Bits	Name	Function
[31:28]	NUMVMIDC	Number of *Virtual Machine ID* (VMID) comparators implemented: `0b0000` VMID comparators are not implemented.
[27:24]	NUMCIDC	Number of Context ID comparators implemented: `0b0000` Context ID comparators are not supported.
[23:20]	NUMSSCC	Number of single-shot comparator controls implemented: `0b0001` One single-shot comparator control is implemented.
[19:16]	NUMRSPAIR	Number of resource selection pairs implemented: `0b0001` Two resource selection pairs are implemented in instruction trace only configuration. `0b0111` Eight resource selection pairs are implemented in instruction and data trace configuration.
[15:12]	NUMPC	Number of processor comparator inputs implemented: `0b0100` Four processor comparator inputs.
[11:9]	-	RES0.
[8]	SUPPDAC	Data address comparisons implemented: `0` Data address comparisons are not supported in instruction trace only configuration. `1` Data address comparisons are supported in instruction and data trace configuration.
[7:4]	NUMDVC	Number of data value comparators implemented: `0b0000` No data value comparators are implemented in instruction trace only configuration. `0b0010` Two data value comparators are implemented in instruction and data trace configuration.
[3:0]	NUMACPAIRS	Number of address comparator pairs implemented: `0b0000` No address comparator pairs are implemented in instruction trace only configuration. `0b0100` Four address comparator pairs are implemented in instruction and data trace configuration.

3.4.33 ID Register 5

The TRCIDR5 characteristics are:

Purpose Indicates the resources available in the ETM-M7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-39 shows the TRCIDR5 bit assignments.

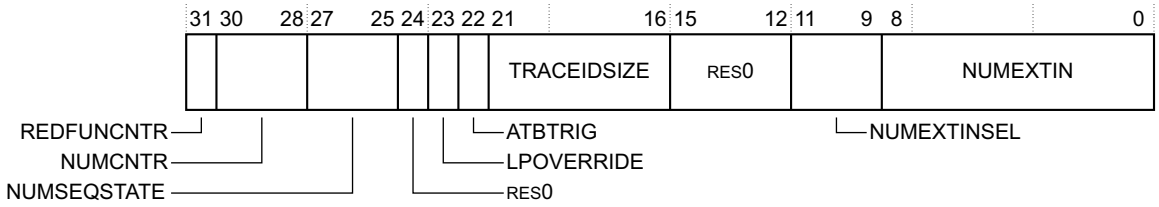


Figure 3-39 TRCIDR5 bit assignments

Table 3-50 shows the TRCIDR5 bit assignments.

Table 3-50 TRCIDR5 bit assignments

Bits	Name	Function
[31]	REDFUNCNTR	Reduced Function Counter implemented: `0` Reduced Function Counter not implemented for instruction and data trace configuration. `1` Reduced Function Counter implemented. This is present in instruction trace only configuration.
[30:28]	NUMCNTR	Number of counters implemented: `0b001` One counter implemented for instruction trace only configuration. `0b010` Two counters implemented for instruction and data trace configuration.
[27:25]	NUMSEQSTATE	Number of sequencer states implemented: `0b000` No sequencer states implemented for instruction trace only configuration. `0b100` Four sequencer states implemented for instruction and data trace configuration.
[24]	-	RES0.
[23]	LPOVERRIDE	Low power state override support: `1` Low power state override support implemented.
[22]	ATBTRIG	ATB trigger support: `1` ATB trigger support implemented.
[21:16]	TRACEIDSIZE	Number of bits of trace ID: `0x07` Seven-bit trace ID implemented.
[15:12]	-	RES0.
[11:9]	NUMEXTINSEL	Number of external input selectors implemented: `0b000` No external input selectors are implemented.
[8:0]	NUMEXTIN	Number of external inputs implemented: `0x02` 2 external inputs implemented in instruction trace only configuration. `0x04` 4 external inputs implemented in instruction and data trace configuration.

3.4.34 Resource Selection Registers 2-15

The TRCRSCTLRn characteristics are:

Purpose Controls the trace resources.

Usage constraints There are no usage constraints.

Configurations TRCRSCTLR4-15 only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-11.

Figure 3-40 shows the TRCRSCTLRn bit assignments.

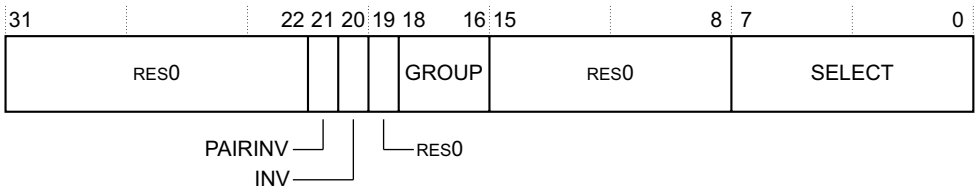


Figure 3-40 TRCRSCTLRn bit assignments

Table 3-51 shows the TRCRSCTLRn bit assignments.

Table 3-51 TRCRSCTLRn bit assignments

Bits	Name	Function
[31:22]	-	RES0.
[21]	PAIRINV	Inverts the result of a combined pair of resources. This bit is only implemented on the lower register for a pair of resource selectors.
[20]	INV	Inverts the selected resources: 0 Resource is not inverted. 1 Resource is inverted.
[19]	-	RES0.
[18:16]	GROUP	Selects a group of resources.
[15:8]	-	RES0.
[7:0]	SELECT	Selects one or more resources from the wanted group. One bit is provided per resource from the group.

3.4.35 Single-shot Comparator Control Register 0

The TRCSSCCR0 characteristics are:

Purpose Controls the single-shot comparator.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-7 on page 3-11.

Figure 3-41 shows the TRCSSCCR0 bit assignments.

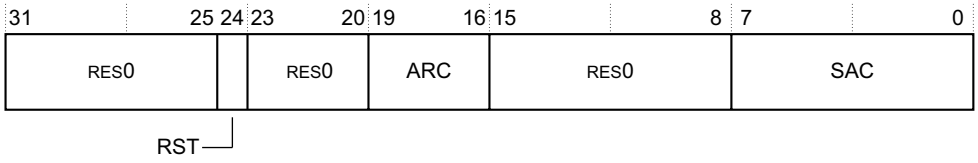


Figure 3-41 TRCSSCCR0 bit assignments

Table 3-52 shows the TRCSSCCR0 bit assignments.

Table 3-52 TRCSSCCR0 bit assignments

Bits	Name	Function
[31:25]	-	RES0.
[24]	RST	Enables the single-shot comparator resource to be reset when it occurs, to enable another comparator match to be detected: 1 Reset enabled. Multiple matches can occur.
[23:20]	-	RES0.
[19:16]	ARC[a]	Selects one or more address range comparators for single-shot control. One bit is provided for each implemented address range comparator.
[15:8]	-	RES0.
[7:0]	SAC[a]	Selects one or more single address comparators for single-shot control. One bit is provided for each implemented single address comparator.

a. Not available in instruction trace only configuration, RES0.

3.4.36 Single-shot Comparator Status Register 0

The TRCSSCSR0 characteristics are:

Purpose Indicates the status of the single-shot comparators:
- TRCSSCSR0 is sensitive to instruction addresses.

Usage constraints There are no usage constraints.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-7 on page 3-11.

Figure 3-42 shows the TRCSSCSR0 bit assignments.

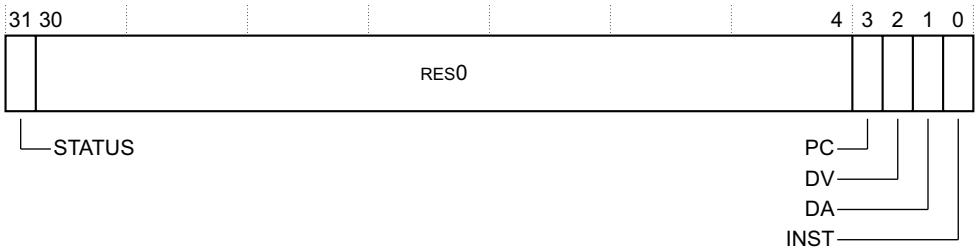


Figure 3-42 TRCSSCSR0 bit assignments

Table 3-53 shows the TRCSSCSR0 bit assignments.

Table 3-53 TRCSSCSR0 bit assignments

Bits	Name	Function
[31]	STATUS	Single-shot status. This indicates whether any of the selected comparators have matched: 0 Match has not occurred. 1 Match has occurred at least once. When programming the ETM-M7, if TRCSSCCR0.RST is 0b0, the STATUS bit must be explicitly written to 0 to enable this single-shot comparator control.
[30:4]	-	RES0.
[3]	PC	Indicates that the Single-shot comparator is sensitive to processor comparator inputs: 1 Single-shot comparator is sensitive to processor comparator inputs.
[2]	DV	Data value comparator support: 0 Single-shot data value comparisons not supported. 1 Single-shot data value comparisons are supported.
[1]	DA	Data address comparator support: 0 Single-shot data address comparisons not supported. 1 Single-shot data address comparisons are supported.
[0]	INST	Instruction address comparator support: 1 Single-shot instruction address comparisons supported.

3.4.37 Single-shot Processor Comparator Input Control Register

The TRCSSPCICR0 characteristics are:

Purpose Selects the processor comparator inputs for Single-shot control.

Usage constraints Can only be written when the trace unit is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-12.

Figure 3-43 shows the TRCSSPCICR0 bit assignments.

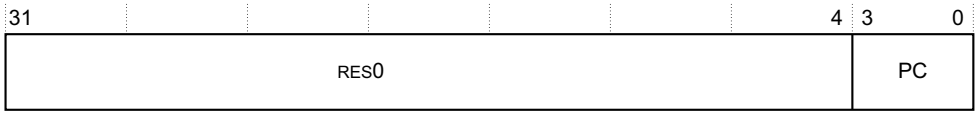


Figure 3-43 TRCSSPCICR0 bit assignments

Table 3-54 shows the TRCSSPCICR0 bit assignments.

Table 3-54 TRCSSPCICR0 bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3:0]	PC	Selects one or more processor comparator inputs for Single-shot control. One bit is provided for each processor comparator input.

3.4.38 OS Lock Status Register

The TRCOSLSR characteristics are:

Purpose Returns the status of the OS Lock.

Usage constraints There are no usage constraints.

Configurations Available in all implementations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-12.

Figure 3-44 shows the TRCOSLSR bit assignments.

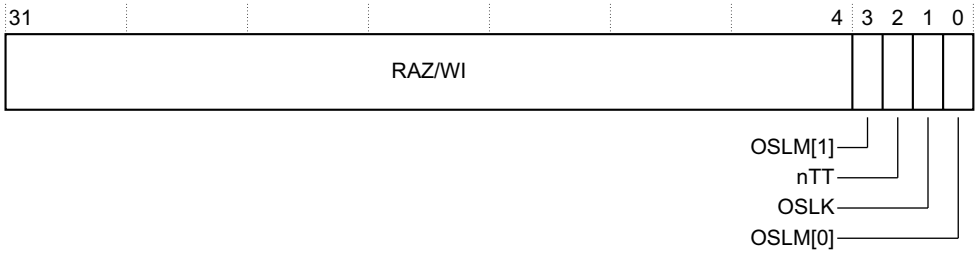


Figure 3-44 TRCOSLSR bit assignments

Table 3-55 shows the TRCOSLSR bit assignments.

Table 3-55 TRCOSLSR bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3, 0]	OSLM	Indicates whether the OS Lock model is implemented or not. 0b00 OS Lock is not implemented.
[2]	nTT	This bit is RAZ, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
[1]	OSLK	RES0.

3.4.39 Power Down Control Register

The TRCPDCR characteristics are:

Purpose Request to the system power controller to keep the ETM-M7 powered up.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-12.

Figure 3-45 on page 3-51 shows the TRCPDCR bit assignments.

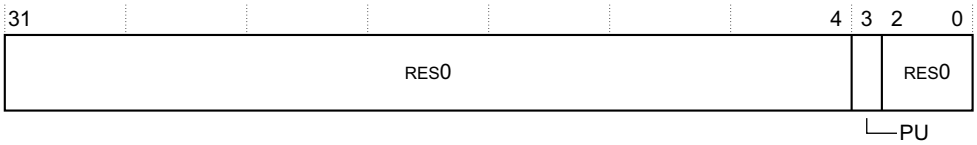


Figure 3-45 TRCPDCR bit assignments

Table 3-56 shows the TRCPDCR bit assignments.

Table 3-56 TRCPDCR bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3]	PU	Power up request, to request that power to the ETM-M7 and access to the trace registers is maintained: 0 Power not requested. 1 Power requested. This bit is reset to 0 on a trace unit reset.
[2:0]	-	RES0.

3.4.40 Power Down Status Register

The TRCPDSR characteristics are:

Purpose Indicates the power down status of the ETM-M7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-12.

Figure 3-46 shows the TRCPDSR bit assignments.

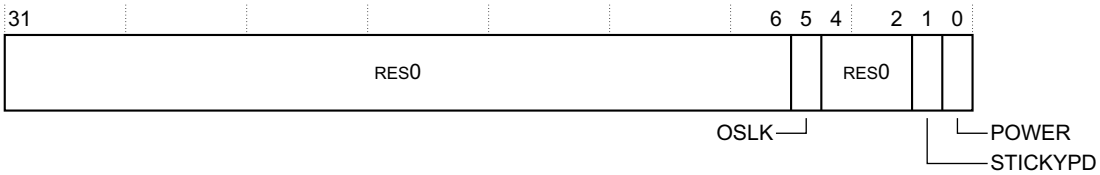


Figure 3-46 TRCPDSR bit assignments

Table 3-57 shows the TRCPDSR bit assignments.

Table 3-57 TRCPDSR bit assignments

Bits	Name	Function
[31:6]	-	RES0.
[5]	OSLK	RES0.

Table 3-57 TRCPDSR bit assignments (continued)

Bits	Name	Function
[4:2]	-	RES0.
[1]	STICKYPD	Sticky power down state. 0 Trace register power has not been removed since the TRCPDSR was last read. 1 Trace register power has been removed since the TRCPDSR was last read. This bit is set to 1 when power to the ETM-M7 registers is removed, to indicate that programming state has been lost. It is cleared after a read of the TRCPDSR.
[0]	POWER	Indicates the ETM-M7 is powered up: 1 ETM-M7 is powered up. All registers are accessible. If a system implementation allows the ETM to be powered down independently of the debug power domain, the system must ensure: • Accesses to the ETM complete correctly. • Reads to this location return 0 to indicate that the ETM is powered down.

3.4.41 Address Comparator Value Registers 0-7

The TRCACVRn characteristics are:

Purpose Indicates the address for the data address comparators.

Usage constraints Only accepts writes when the trace unit is disabled.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-12.

Figure 3-47 shows the TRCACVRn bit assignments.

Figure 3-47 TRCACVRn bit assignments

Table 3-58 shows the TRCACVRn bit assignments.

Table 3-58 TRCACVRn bit assignments

Bits	Name	Function
[31:0]	ADDRESS	The address value to compare against

3.4.42 Address Comparator Access Type Registers 0-7

The TRCACATRn characteristics are:

Purpose Controls the access for the data address comparators.

Usage constraints There are no usage constraints.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-12.

Figure 3-48 shows the TRCACATR0 bit assignments.

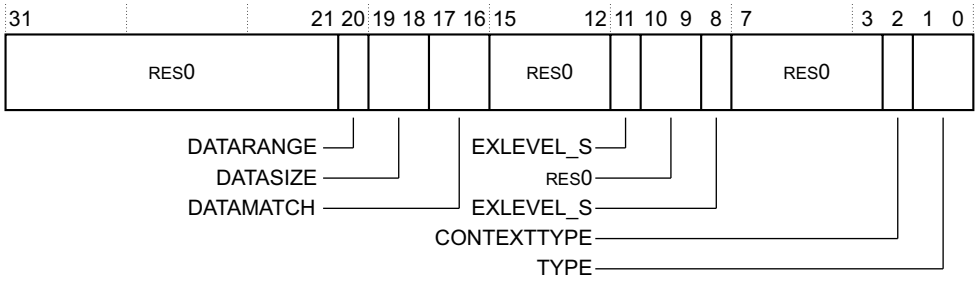


Figure 3-48 TRCACATR0 bit assignments

Table 3-59 shows the TRCACATR0 bit assignments.

Table 3-59 TRCACATR0 bit assignments

Bits	Name	Function
[31:21]	-	RES0.
[20]	DATARANGE	Data value comparison range control, to select whether the data value comparison is made against the single address comparator or the address range comparator: 0 Only the single address comparator matches. 1 Only the address range comparator matches.
[19:18]	DATASIZE	Data value comparison size control: 0b00 Byte size. 0b01 Halfword size. 0b10 Word size. 0b11 Doubleword size.
[17:16]	DATAMATCH	Data value comparison control: 0b01 Comparator matches only if the data value comparison matches. 0b11 Comparator matches only if the data value comparison does not match.
[15:12]	-	RES0.
[11]	EXLEVEL_S	Indicates whether the comparator matches in Handler privilege level: 1 The comparator must not match in this privilege level.
[10:9]	-	RES0.
[8]	EXLEVEL_S	Indicates whether the comparator matches in Thread privilege level: 1 The comparator must not match in this privilege level.
[7:3]	-	RES0.
[2]	CONTEXTTYPE	Indicates whether the context comparator is used in the comparison: 0 Context comparators is not supported.
[1:0]	TYPE	The type of comparison: 0b00 Instruction address. 0b01 Data load address. 0b10 Data store address. 0b11 Data load or store address.

Note

TRCACATR2, 4 and 6 are functionally identical to TRCACATR0.

Figure 3-48 on page 3-53 shows the TRCACATR1 bit assignments.

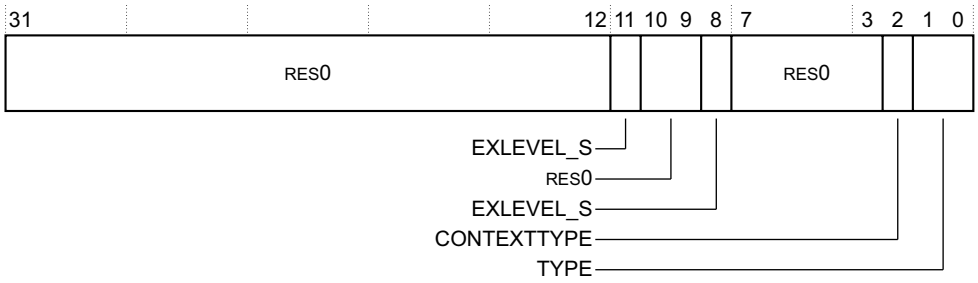


Figure 3-49 TRCACATR1 bit assignments

Table 3-59 on page 3-53 shows the TRCACATR1 bit assignments.

Table 3-60 TRCACATR1 bit assignments

Bits	Name	Function
[31:12]	-	RES0.
[11]	EXLEVEL_S	Indicates whether the comparator matches in exception level 3 in Secure state: 1 The comparator must not match in this exception level.
[10:9]	-	RES0.
[8]	EXLEVEL_S	Indicates whether the comparator matches in exception level 0 in Secure state: 1 The comparator must not match in this exception level.
[7:3]	-	RES0.
[2]	CONTEXTTYPE	Indicates whether the context comparator is used in the comparison: 0 Use no context comparators.
[1:0]	TYPE	The type of comparison: 0b00 Instruction address. 0b01 Data load address. 0b10 Data store address. 0b11 Data load or store address.

Note

TRCACATR3, 5 and 7 are functionally identical to TRCACATR1.

3.4.43 Data Value Comparator Value Registers 0-1

The TRCDVCVRn characteristics are:

Purpose Indicates the value for the data value comparators.

Usage constraints There are no usage constraints.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-12.

Figure 3-50 shows the TRCDVCVRn bit assignments.

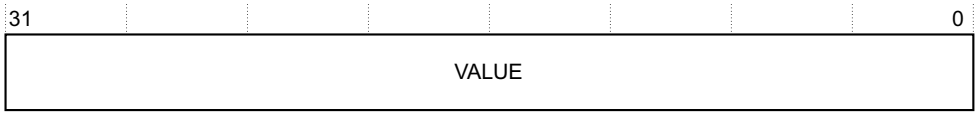


Figure 3-50 TRCDVCVRn bit assignments

Table 3-61 shows the TRCDVCVRn bit assignments.

Table 3-61 TRCDVCVRn bit assignments

Bits	Name	Function
[31:0]	VALUE	The data value to compare against

3.4.44 Data Value Comparator Mask Registers 0-1

The TRCDVCMRn characteristics are:

Purpose Controls the mask value for the data value comparators.

Usage constraints There are no usage constraints.

Configurations Only available in instruction and data trace configuration.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-12.

Figure 3-51 shows the TRCDVCMRn bit assignments.

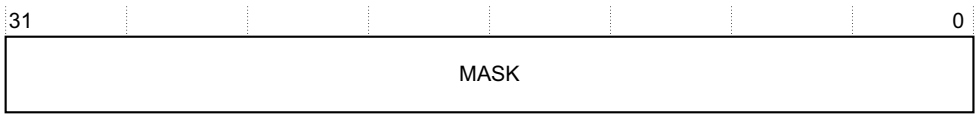


Figure 3-51 TRCDVCMRn bit assignments

Table 3-62 shows the TRCDVCMRn bit assignments.

Table 3-62 TRCDVCMRn bit assignments

Bits	Name	Function
[31:0]	MASK	The mask value to apply to the data value comparison

3.4.45 Integration test registers

The following subsections describe the Integration test registers. To access these registers you must first set bit[0] of the *Integration Mode Control Register* on page 3-64 to 1.

- You can use the write-only Integration test registers to set the outputs of some of the ETM signals. Table 3-63 shows the signals that can be controlled in this way.
- You can use the read-only Integration test registers to read the state of some of the ETM input signals. Table 3-64 shows the signals that can be read in this way.

See the *ARM® Embedded Trace Macrocell Architecture Specification ETMv4* for more information about TRCITCTRL.

Table 3-63 Output signals that the integration test registers can control

Signal	Register	Bits	Register description
AFREADYMD[a]	TRCITDATBOUTR	[1]	See *Integration Data ATB Out Register* on page 3-62
AFREADYMI	TRCITIATBOUTR	[1]	See *Integration Instruction ATB Out Register* on page 3-63
ATBYTESMD[2:0][a]	TRCITDATBOUTR	[10:8]	See *Integration Data ATB Out Register* on page 3-62
ATDATAMD[63, 55, 47, 39, 31, 23, 15, 7, 0][a]	TRCITDDATAR	[8:0]	See *Integration Data ATB Data Register* on page 3-59
ATDATAMI[7, 0]	TRCITIDATAR	[1:0]	See *Integration Instruction ATB Data Register* on page 3-60
ATIDMD[6:0][a]	TRCITATBIDR	[6:0]	See *Integration ATB Identification Register* on page 3-59
ATIDMI[6:0]	TRCITATBIDR	[6:0]	See *Integration ATB Identification Register* on page 3-59
ATVALIDMD[a]	TRCITDATBOUTR	[0]	See *Integration Data ATB Out Register* on page 3-62
ATVALIDMI	TRCITIATBOUTR	[0]	See *Integration Instruction ATB Out Register* on page 3-63
ETMEVENTM[3:0][b]	TRCITMISCOUTR	[11:8]	See *Integration Miscellaneous Outputs Register* on page 3-57

a. Only available in instruction and data trace configuration.
b. Only 2 in instruction trace configuration.

Table 3-64 Input signals that the integration test registers can read

Signal	Register	Bits	Register description
AFVALIDMD[a]	TRCITDATBINR	[1]	See *Integration Data ATB In Register* on page 3-61
ATREADYMD[a]	TRCITDATBINR	[0]	See *Integration Data ATB In Register* on page 3-61
AFVALIDMI	TRCITIATBINR	[1]	See *Integration Instruction ATB In Register* on page 3-61
ATREADYMI	TRCITIATBINR	[0]	See *Integration Instruction ATB In Register* on page 3-61
CPUACTIVE	TRCITMISCINR	[4]	See *Integration Miscellaneous Inputs Register* on page 3-58
HALTED	TRCITMISCINR	[5]	See *Integration Miscellaneous Inputs Register* on page 3-58
ETMEVENTS[3:0][b]	TRCITMISCINR	[3:0]	See *Integration Miscellaneous Inputs Register* on page 3-58

a. Only available in instruction and data trace configuration.
b. Only 2 in instruction trace configuration.

Using the integration test registers

When:

- Bit[0] of TRCITCTRL is set to 1:
  - Values written to the write-only integration test registers map onto the specified outputs of the macrocell. For example, writing `0x3` TRCITMISCOUTR[11:8] causes **ETMEVENTM[3:0]** to take the value `0x3`.
  - Values read from the read-only integration test registers correspond to the values of the specified inputs of the macrocell. For example, if you read TRCITMISCINR[3:0] you obtain the value of **ETMEVENTS[3:0]**.
- Bit[0] of TRCITCTRL is set to 0:
  - Reading an Integration test register returns an UNPREDICTABLE value.
  - The effect of attempting to write to an Integration test register, other than the read-only integration test registers, is unpredictable.

Note

You must not attempt to write to an integration test register unless you have set bit[0] of TRCITCTRL to 1.

Integration Miscellaneous Outputs Register

The TRCITMISCOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-65.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-52 shows the TRCITMISCOUTR bit assignments.

Figure 3-52 TRCITMISCOUTR bit assignments

Table 3-65 shows the TRCITMISCOUTR bit assignments.

Table 3-65 TRCITMISCOUTR bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero.
[11:8]	EXTOUT	Drives the **ETMEVENTM[3:0]** output pins[a].
[7:0]	-	Reserved. Write as zero.

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITMISCOUTR bit values correspond to the physical state of the output pins.

Integration Miscellaneous Inputs Register

The TRCITMISCINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-66.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-64 on page 3-56.

Figure 3-53 shows the TRCITMISCINR bit assignments.

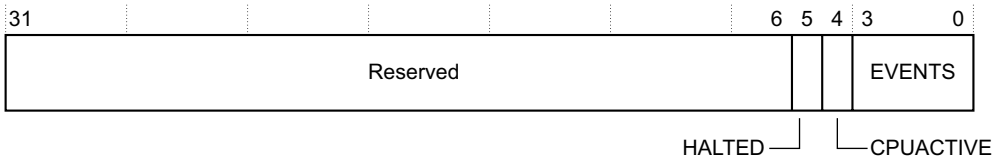


Figure 3-53 TRCITMISCINR bit assignments

Table 3-66 shows the TRCITMISCINR bit assignments.

Table 3-66 TRCITMISCINR bit assignments

Bits	Name	Function
[31:6]	-	Reserved. Read undefined.
[5]	HALTED	Returns the value of the **HALTED** input pin[a].
[4]	CPUACTIVE	Returns the value of the **CPUACTIVE** input pin[a].
[3:0]	EVENTS	Returns the value of the **ETMEVENTS[3:0]** input pins[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITMISCINR bit values always correspond to the physical state of the input pins.

Integration ATB Identification Register

The TRCITATBIDR characteristics are:

Purpose Sets the state of output pins shown in Table 3-67.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-54 shows the TRCITATBIDR bit assignments.

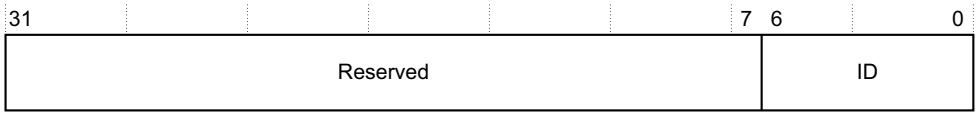


Figure 3-54 TRCITATBIDR bit assignments

Table 3-67 shows the TRCITATBIDR bit assignments.

Table 3-67 TRCITATBIDR bit assignments

Bits	Name	Function
[31:7]	-	Reserved. Read undefined.
[6:0]	ID	Drives the **ATIDMD[6:0]** and **ATIDMI[6:0]** output pins[a].

a. Bits[6:1] drive both **ATIDMD[6:1]** and **ATIDMI[6:1]**. Bit[0] drives **ATIDMI[0]**.
When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
ATIDMD[0] is always driven HIGH.
The TRCITATBIDR bit values correspond to the physical state of the output pins.

Integration Data ATB Data Register

The TRCITDDATAR characteristics are:

Purpose Sets the state of the **ATDATAMD** output pins shown in Table 3-68 on page 3-60.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-55 on page 3-60 shows the TRCITDDATAR bit assignments.

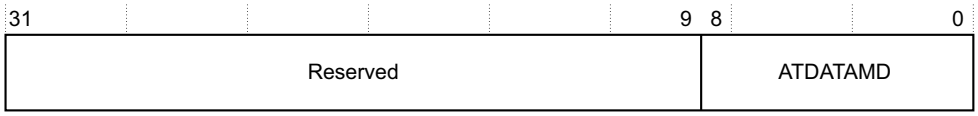


Figure 3-55 TRCITDDATAR bit assignments

Table 3-68 shows the TRCITDDATAR bit assignments.

Table 3-68 TRCITDDATAR bit assignments

Bits	Name	Function
[31:9]	-	Reserved. Write as zero.
[8:0]	ATDATAMD	Drives the **ATDATAMD[63, 55, 47, 39, 31, 23, 15, 7, 0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITDDATAR bit values correspond to the physical state of the output pins.

Integration Instruction ATB Data Register

The TRCITIDATAR characteristics are:

Purpose Sets the state of the **ATDATAMI** output pins shown in Table 3-69.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-56 shows the TRCITIDATAR bit assignments.

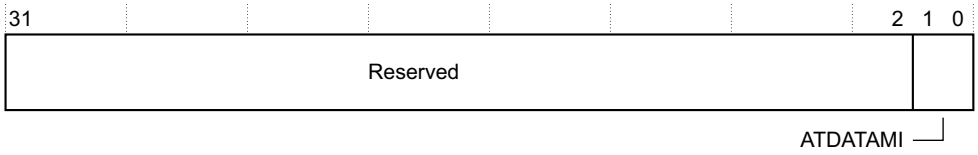


Figure 3-56 TRCITIDATAR bit assignments

Table 3-69 shows the TRCITIDATAR bit assignments.

Table 3-69 TRCITIDATAR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Write as zero.
[1:0]	ATDATAMI	Drives the **ATDATAMI[7, 0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITIDATAR bit values correspond to the physical state of the output pins.

Integration Data ATB In Register

The TRCITDATBINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-70.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-64 on page 3-56.

Figure 3-57 shows the TRCITDATBINR bit assignments.

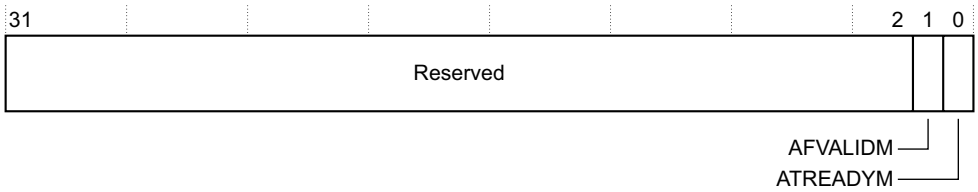


Figure 3-57 TRCITDATBINR bit assignments

Table 3-70 shows the TRCITDATBINR bit assignments.

Table 3-70 TRCITDATBINR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Read undefined.
[1]	AFVALIDM	Returns the value of the **AFVALIDMD** input pin[a].
[0]	ATREADYM	Returns the value of the **ATREADYMD** input pin[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITDATBINR bit values always correspond to the physical state of the input pins.

Integration Instruction ATB In Register

The TRCITIATBINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-71 on page 3-62.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-64 on page 3-56.

Figure 3-58 on page 3-62 shows the TRCITIATBINR bit assignments.

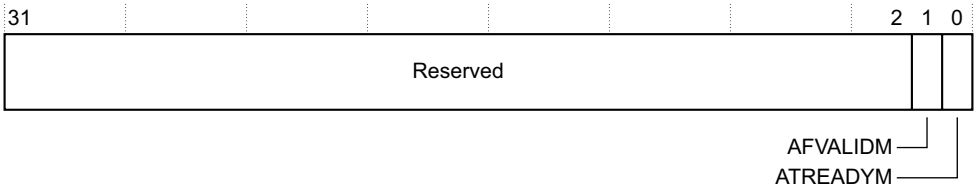


Figure 3-58 TRCITIATBINR bit assignments

Table 3-71 shows the TRCITIATBINR bit assignments.

Table 3-71 TRCITIATBINR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Read undefined.
[1]	AFVALIDM	Returns the value of the **AFVALIDMI** input pin[a].
[0]	ATREADYM	Returns the value of the **ATREADYMI** input pin[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITIATBINR bit values always correspond to the physical state of the input pins.

Integration Data ATB Out Register

The TRCITDATBOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-72 on page 3-63.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-59 shows the TRCITDATBOUTR bit assignments.

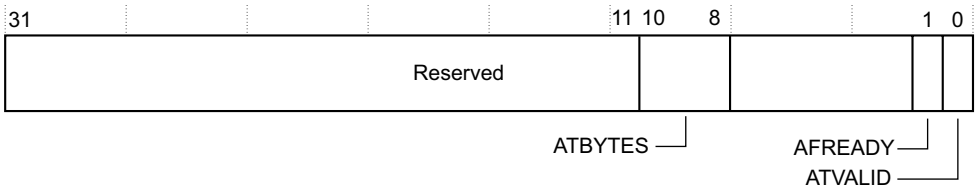


Figure 3-59 TRCITDATBOUTR bit assignments

Table 3-72 shows the TRCITDATBOUTR bit assignments.

Table 3-72 TRCITDATBOUTR bit assignments

Bits	Name	Function
[31:11]	-	Reserved. Read undefined.
[10:8]	ATBYTES	Drives the **ATBYTESMD[2:0]** output pins[a].
[1]	AFREADY	Drives the **AFREADYMD** output pin[a].
[0]	ATVALID	Drives the **ATVALIDMD** output pin[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITDATBOUTR bit values always correspond to the physical state of the output pins.

Integration Instruction ATB Out Register

The TRCITIATBOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-73.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-13, and Table 3-63 on page 3-56.

Figure 3-60 shows the TRCITIATBOUTR bit assignments.

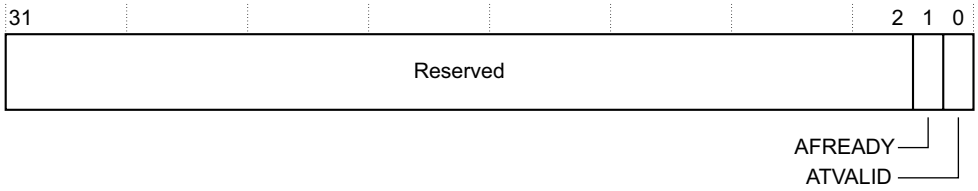


Figure 3-60 TRCITIATBOUTR bit assignments

Table 3-73 shows the TRCITIATBOUTR bit assignments.

Table 3-73 TRCITIATBOUTR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Read undefined.
[1]	AFREADY	Drives the **AFREADYMI** output pin[a].
[0]	ATVALID	Drives the **ATVALIDMI** output pin[a].

Integration Mode Control Register

The TRCITCTRL characteristics are:

Purpose Enables topology detection or integration testing, by putting the ETM-M7 into integration mode.

Usage constraints ARM recommends that you perform a debug reset after using integration mode.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-61 shows the TRCITCTRL bit assignments.

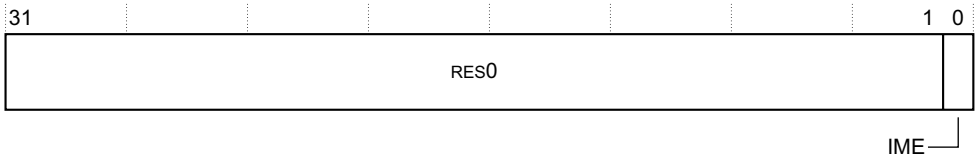


Figure 3-61 TRCITCTRL bit assignments

Table 3-74 shows the TRCITCTRL bit assignments.

Table 3-74 TRCITCTRL bit assignments

Bits	Name	Function
[31:1]	-	RES0.
[0]	IME	Integration mode enable: 0 ETM-M7 is not in integration mode. This is the reset value. 1 ETM-M7 is in integration mode.

3.4.46 Claim Tag Set Register

The TRCCLAIMSET characteristics are:

Purpose Sets bits in the claim tag and determines the number of claim tag bits implemented.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-62 shows the TRCCLAIMSET bit assignments.

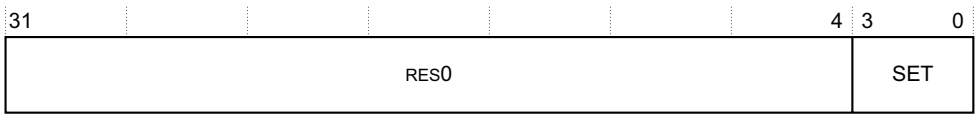


Figure 3-62 TRCCLAIMSET bit assignments

Table 3-75 shows the TRCCLAIMSET bit assignments.

Table 3-75 TRCCLAIMSET bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3:0]	SET	On reads, for each bit: 0 Claim tag bit is not implemented. 1 Claim tag bit is implemented. This value is returned for each of the claim bits 0-3, indicating 4 claim bits are implemented. On writes, for each bit: 0 Has no effect. 1 Sets the relevant bit of the claim tag.

3.4.47 Claim Tag Clear Register

The TRCCLAIMCLR characteristics are:

Purpose Clears bits in the claim tag and determines the current value of the claim tag.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-63 shows the TRCCLAIMCLR bit assignments.

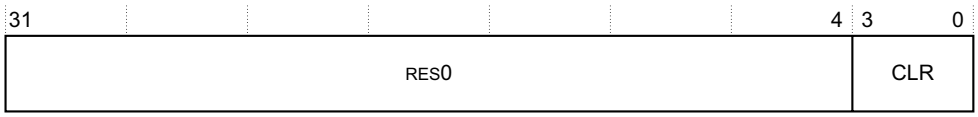


Figure 3-63 TRCCLAIMCLR bit assignments

Table 3-76 shows the TRCCLAIMCLR bit assignments.

Table 3-76 TRCCLAIMCLR bit assignments

Bits	Name	Function
[31:4]	-	RES0.
[3:0]	CLR	On reads, for each bit: 0 Claim tag bit is not set. 1 Claim tag bit is set. On writes, for each bit: 0 Has no effect. 1 Clears the relevant bit of the claim tag.

3.4.48 Software Lock Access Register

The TRCLAR characteristics are:

Purpose Controls access to registers when **PADDRDBG31** is LOW.

When the software lock is set, write accesses when **PADDRDBG31** is LOW to all ETM-M7 registers are ignored except for write accesses to the TRCLAR.

When the software lock is set, read accesses of TRCPDSR with **PADDRDBG31** is LOW do not change the TRCPDSR.STICKYPD bit. Read accesses of all other registers are not affected.

Accesses with **PADDRDBG31** HIGH are not affected by the software lock.

Usage constraints This register is only present for accesses with **PADDRDBG31** LOW, and is RES0 for accesses with **PADDRDBG31** HIGH.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-64 shows the TRCLAR bit assignments.

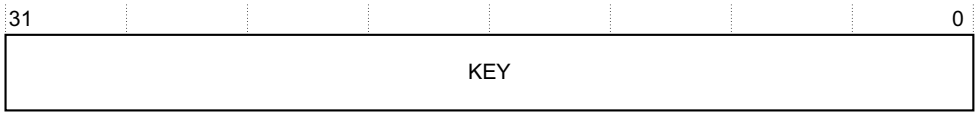


Figure 3-64 TRCLAR bit assignments

Table 3-77 shows the TRCLAR bit assignments.

Table 3-77 TRCLAR bit assignments

Bits	Name	Function
[31:0]	KEY	Software lock key value: 0xC5ACCE55 Clear the software lock. All other write values set the software lock.

3.4.49 Software Lock Status Register

The TRCLSR characteristics are:

Purpose Indicates whether the software lock is implemented, and indicates the current status of the software lock.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-65 on page 3-67 shows the TRCLSR bit assignments.

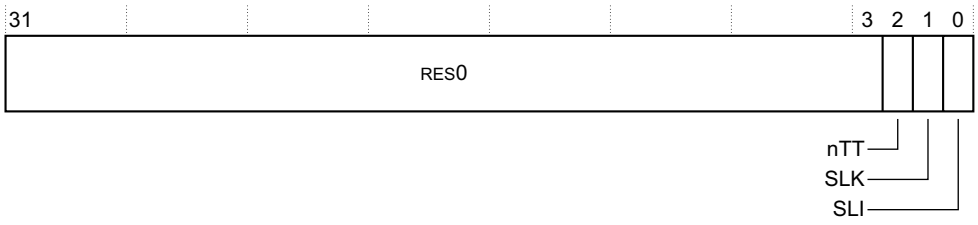


Figure 3-65 TRCLSR bit assignments

Table 3-78 shows the TRCLSR bit assignments.

Table 3-78 TRCLSR bit assignments

Bits	Name	Function
[31:3]	-	RES0.
[2]	nTT	Indicates size of TRCLAR: 0 TRCLAR is always 32 bits.
[1]	SLK	Software lock status: 0 Software lock is clear. This value is returned for all accesses with **PADDRDBG31** HIGH. 1 Software lock is set.
[0]	SLI	Indicates whether the software lock is implemented on this interface. 1 Software lock is not implemented. This is returned for all accesses with **PADDRDBG31** HIGH. 1 Software lock is implemented. This is returned for all accesses with **PADDRDBG31** LOW.

3.4.50 Authentication Status Register

The TRCAUTHSTATUS characteristics are:

Purpose Indicates the current level of tracing permitted by the system.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-66 shows the TRCAUTHSTATUS bit assignments.

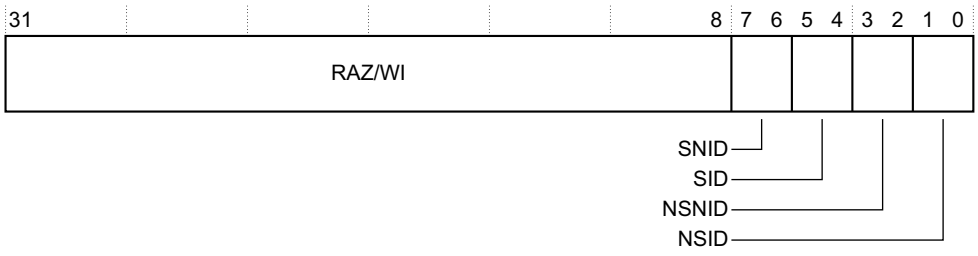


Figure 3-66 TRCAUTHSTATUS bit assignments

Table 3-79 shows the TRCAUTHSTATUS bit assignments.

Table 3-79 TRCAUTHSTATUS bit assignments

Bits	Name	Function
[31:8]	-	RES0.
[7:6]	SNID	Secure Non-Invasive Debug: 0b10 Secure Non-Invasive Debug implemented but disabled. 0b11 Secure Non-Invasive Debug implemented and enabled.
[5:4]	SID	Secure Invasive Debug: 0b00 Secure Invasive Debug not implemented.
[3:2]	NSNID	Non-Secure Non-Invasive Debug: 0b00 Non-Secure Non-Invasive Debug not implemented.
[1:0]	NSID	Non-Secure Invasive Debug: 0b00 Non-Secure Invasive Debug not implemented.

3.4.51 Device Architecture Register

The TRCDEVARCH characteristics are:

Purpose Identifies the ETM-M7 as an ETMv4 component.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-67 shows the TRCDEVARCH bit assignments.

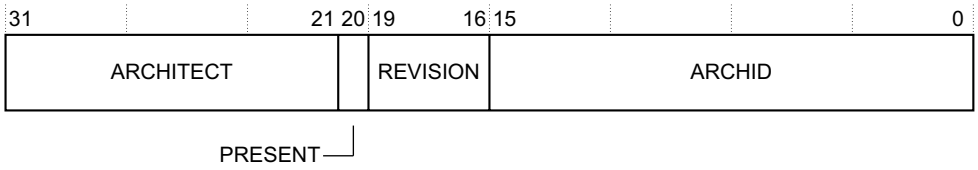


Figure 3-67 TRCDEVARCH bit assignments

Table 3-80 shows the TRCDEVARCH bit assignments.

Table 3-80 TRCDEVARCH bit assignments

Bits	Name	Function
[31:21]	ARCHITECT	Defines the architect of the component: 0x23B ARM.

Table 3-80 TRCDEVARCH bit assignments (continued)

Bits	Name	Function
[20]	PRESENT	Indicates the presence of this register: 0b1 Register is present.
[19:16]	REVISION	Architecture revision: 0b0000 Architecture revision 0.
[15:0]	ARCHID	Architecture ID: 0x4A13 ETMv4 component.

3.4.52 Device ID Register

The TRCDEVID characteristics are:

Purpose This register is reserved.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-68 shows the TRCDEVID bit assignments.

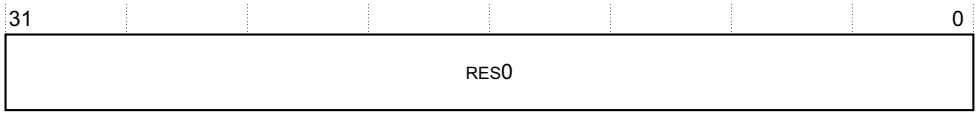


Figure 3-68 TRCDEVID bit assignments

Table 3-81 shows the TRCDEVID bit assignments.

Table 3-81 TRCDEVID bit assignments

Bits	Name	Function
[31:0]	RES0	Reserved.

3.4.53 Device Type Register

The TRCDEVTYPE characteristics are:

Purpose Indicates the type of the component.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-69 on page 3-70 shows the TRCDEVTYPE bit assignments.

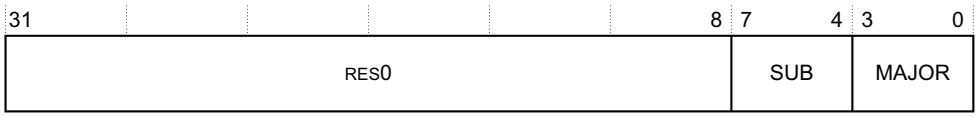


Figure 3-69 TRCDEVTYPE bit assignments

Table 3-82 shows the TRCDEVTYPE bit assignments.

Table 3-82 TRCDEVTYPE bit assignments

Bits	Name	Function
[31:8]	-	RES0.
[7:4]	SUB	The sub-type of the component: 0b0001 Processor trace.
[3:0]	MAJOR	The main type of the component: 0b0011 Trace source.

3.4.54 Peripheral Identification Registers

The TRCPIDR0-7 characteristics are:

Purpose Provides the standard Peripheral ID required by all CoreSight components. See the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* for more information.

Usage constraints Only bits[7:0] of each register are used. This means that TRCPIDR0-7 define a single 64-bit *Peripheral ID*, as Figure 3-70 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-70 shows the mapping between TRCPIDR0-7 and the single 64-bit *Peripheral ID* value.

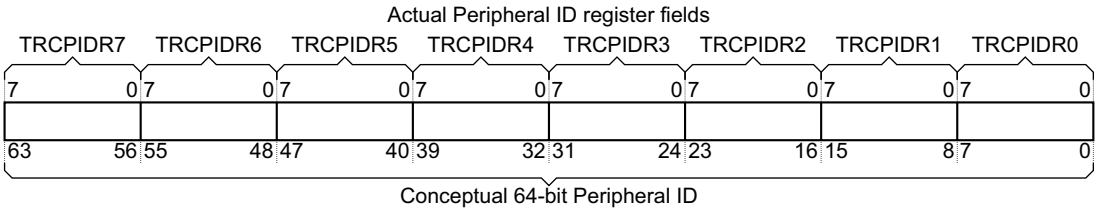


Figure 3-70 Mapping between TRCPIDR0-7 and the Peripheral ID value

Figure 3-71 on page 3-71 shows the Peripheral ID bit assignments in the single conceptual Peripheral ID register.

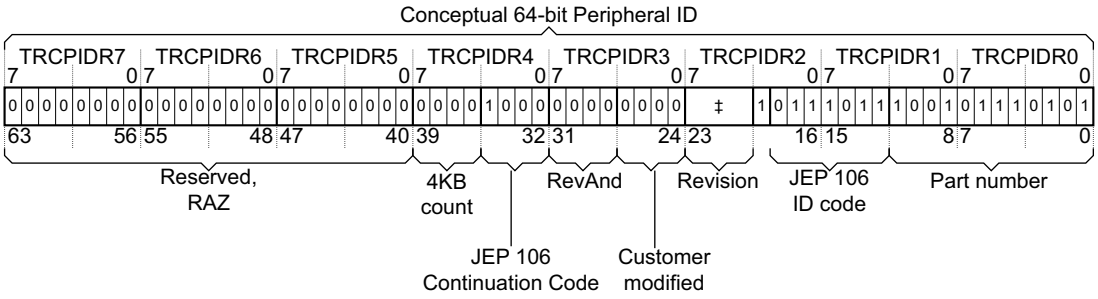


Figure 3-71 Peripheral ID fields

Table 3-83 shows the values of the fields when reading this set of registers. The *ARM® Embedded Trace Macrocell Architecture Specification ETM v4* gives more information about many of these fields.

Table 3-83 TCRPIDR0-7 bit assignments

Register	Register number	Register offset	Bits	Value	Description
TRCPIDR7	0x3F7	0xFDC	[31:8]	-	RES0.
			[7:0]	0x00	RES0.
TRCPIDR6	0x3F6	0xFD8	[31:8]	-	RES0.
			[7:0]	0x00	RES0.
TRCPIDR5	0x3F5	0xFD4	[31:8]	-	RES0.
			[7:0]	0x00	RES0.
TRCPIDR4	0x3F4	0xFD0	[31:8]	-	RES0.
			[7:4]	0x0	n, where 2^n is number of 4KB blocks used.
			[3:0]	0x4	JEP 106 continuation code.
TRCPIDR3	0x3FB	0xFEC	[31:8]	-	RES0.
			[7:4]	0x0	RevAnd (at top level). Manufacturer revision number.
			[3:0]	0x0	Customer Modified. 0x0 indicates from ARM.
TRCPIDR2	0x3FA	0xFE8	[31:8]	-	RES0.
			[7:4]	a	Revision Number of Peripheral. This value is the same as the Implementation revision field of the TRCIDR, see *ID Register 1* on page 3-41.
			[3]	1	Always 1. Indicates that a JEDEC assigned value is used.
			[2:0]	0x3	JEP 106 identity code [6:4].

Table 3-83 TCRPIDR0-7 bit assignments (continued)

Register	Register number	Register offset	Bits	Value	Description
TRCPIDR1	0x3F9	0xFE4	[31:8]	-	RES0.
			[7:4]	0xB	JEP 106 identity code [3:0].
			[3:0]	0x9	Part Number[11:8].
TRCPIDR0	0x3F8	0xFE0	[31:8]	-	RES0.
			[7:0]	0x75	Part Number [7:0].

a. See the Description column for more information.

Note

In Table 3-83 on page 3-71, the *Peripheral Identification Registers* on page 3-70 are listed in order of register name, from most significant (TRCPIDR7) to least significant (TRCPIDR0). This does not match the order of the register offsets.

3.4.55 Component Identification Registers

The TRCCIDR0-3 characteristics are:

Purpose Identifies the ETM as a CoreSight component. For more information, see the *ARM® Embedded Trace Macrocell Architecture Specification ETM v4*.

Usage constraints Only bits[7:0] of each register are used. This means that TRCCIDR0-3 define a single 32-bit Component ID, as Figure 3-72 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-13.

Figure 3-72 shows the mapping between TRCCIDR0-3 and the single 64-bit *Component ID* value.

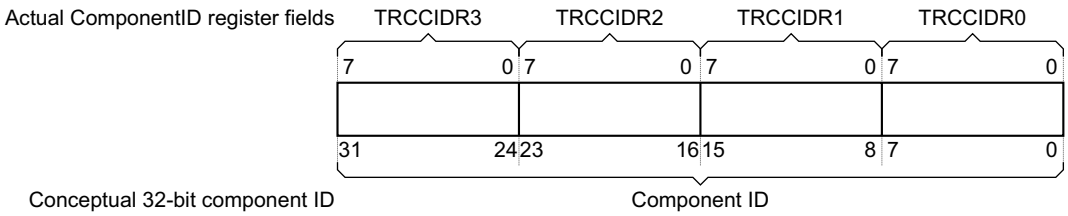


Figure 3-72 Mapping between TRCCIDR0-3 and the Component ID value

Table 3-84 shows the Component ID bit assignments in the single conceptual Component ID register.

Table 3-84 TRCCIDR0-3 bit assignments

Register	Register number	Register offset	Bits	Value	Description
TRCCIDR3	0x3FF	0xFFC	[31:8]	-	RES0.
			[7:0]	0xB1	Component identifier, bits[31:24].
TRCCIDR2	0x3FE	0xFF8	[31:8]	-	RES0.
			[7:0]	0x05	Component identifier, bits[23:16].
TRCCIDR1	0x3FD	0xFF4	[31:8]	-	RES0.
			[7:4]	0x9	Debug component with CoreSight-compatible registers (component identifier, bits[15:12]).
			[3:0]	0x0	Component identifier, bits[11:8].
TRCCIDR0	0x3FC	0xFF0	[31:8]	-	RES0.
			[7:0]	0x0D	Component identifier, bits[7:0].

Note

In Table 3-84 the *Component Identification Registers* are listed in order of register name, from most significant (TRCCIDR3) to least significant (TRCCIDR0). This does not match the order of the register offsets.

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue A

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue A and issue B

Change	Location	Affects
Table title changed to ETMEVENTM connections to CTI	Table 2-2 on page 2-5	All revisions
Packet formats description updated	*Packet formats* on page 2-8	All revisions
Micro-architectural exceptions updated	*Micro-architectural exceptions* on page 2-10	All revisions
TRCIDR4 reset values updated	Table 3-1 on page 3-5	All revisions
PROCSEL bit field functional description updated	Table 3-13 on page 3-15	All revisions
REVISION implementation revision number updated	Table 3-46 on page 3-42	r0p1

Table A-2 Differences between issue A and issue B (continued)

Change	Location	Affects
Usage constraint updated	• *Trace Configuration Register* on page 3-16 • *Event Control 0 Register* on page 3-18 • *Event Control 1 Register* on page 3-20 • *Stall Control Register* on page 3-21 • *Global Timestamp Control Register* on page 3-22 • *Cycle Count Control Register* on page 3-24 • *Trace ID Register* on page 3-25 • *ViewInst Start/Stop Control Register* on page 3-29	All revisions
NUMPROC bit field functional description updated	Table 3-48 on page 3-44	All revisions
TRCSSCSR0 bit assignments corrected	Table 3-53 on page 3-49	All revisions
POWER bit field functional description updated	Table 3-57 on page 3-51	All revisions
Device ID Register description updated	*Device Type Register* on page 3-69	All revisions
TSVALUE[63:0] miscellaneous signal description updated	Table A-7 on page A-8	All revisions

Table A-3 Differences between issue B and issue C

Change	Location	Affects
TRCACVR0-7 base offset in ETM-M7 register summary table updated	Table 3-1 on page 3-5	All revisions
Added footnote to Comparator registers table	Table 3-9 on page 3-12	
Stall Control Register updated	*Stall Control Register* on page 3-21	
TRCITDATBOUTR.ATBYTES function updated	Table 3-72 on page 3-63	
Appendix A Signal Descriptions removed	-	

Table A-4 Differences between issue C and issue D

Change	Location	Affects
Added a description on how ETM single shot and start-stop logic, when present, responds using DWT comparators	*Resource selection* on page 2-8	All revisions