SC054 ASB

Static Memory Controller

Technical Reference Manual

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SC054 ASB
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidentiality	Change
15 March 2000	A	Non-Confidential	First release.
12 May 2000	B	Non-Confidential	Changes to Para 2.2.1, Table 3-1, and 3-2.
15 March 2000	C	Non-Confidential	EBRI and signals SMBUSREQ and SMBUSGNT added to Chapters 1,2, and Appdendix A.
30 June 2000	D	Non-Confidential	Changes to 1.1.1, 2.1.7, 2.2.2, 2.2.3, 2.2.5, 2.2.7, 2.2.8, 2.2.10, Figure 2-1 and Table 3-3.

Proprietary Notice

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Product Status

The information in this document is final, that is for a developed product.

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Preface

This preface introduces the SC054 ASB Static Memory Controller and its reference documentation. It contains the following sections:

About this manual

This is the *Technical Reference Manual* (TRM) for the SC054 ASB Static Memory Controller.

Intended audience

This manual is written for hardware and software engineers implementing System-on-Chip designs. It provides the necessary information to enable engineers to integrate the peripheral into a target system as quickly as possible.

Using this manual

This manual is organized into the following chapters:Chapter 1 *Introduction*

Chapter 1 ***Introduction***

Read this chapter for an introduction to the SC054 ASB Static Memory Controller and its features.

Chapter 2 ***Functional Overview***

Read this chapter for a description of the major functional blocks of the SC054 ASB Static Memory Controller.

Chapter 3 ***Programmer's Model***

Read this chapter for a description of the SC054 ASB Static Memory Controller registers and programming details.

Appendix A ***SC054 ASB Static Memory ControllerSignal Descriptions***

Read this appendix for details on the SC054 ASB Static Memory Controller signals.

Conventions

Conventions that this manual can use are described in:

- *Typographical* on page xiii
- *Timing diagrams* on page xiii
- *Signals* on page xiv
- *Numbering* on page xv.

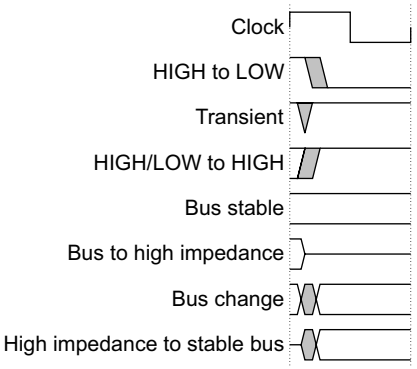
Typographical

This manual uses the following typographical conventions:

italic	Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
< and >	Angle brackets enclose replaceable terms for assembler syntax where they appear in code or code fragments. The replaceable terms appear in normal font in running text. For example: • `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>` • The Opcode_2 value selects which register is accessed.

Timing diagrams

The figure named *Key to timing diagram conventions* on page xiv on page xiv explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams. Shaded bus and signal areas are undefined, and the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means HIGH for active-HIGH signals and LOW for active-LOW signals.

Lower-case n Denotes an active-LOW signal.

Prefix A Denotes global *Advanced eXtensible Interface* (AXI) signals:

Prefix AR Denotes AXI read address channel signals.

Prefix AW Denotes AXI write address channel signals.

Prefix B Denotes AXI write response channel signals.

Prefix C Denotes AXI low-power interface signals.

Prefix H Denotes *Advanced High-performance Bus* (AHB) signals.

Prefix P Denotes *Advanced Peripheral Bus* (APB) signals.

Prefix R Denotes AXI read data channel signals.

Prefix W Denotes AXI write data channel signals.

Numbering

The numbering convention is:

<size in bits>`<base><number>

This is a Verilog method of abbreviating constant numbers. For example:

- `h7B4 is an unsized hexadecimal value.
- `o7654 is an unsized octal value.
- 8`d9 is an eight-bit wide decimal value of 9.
- 8`h3F is an eight-bit wide hexadecimal value of `0x3F`. This is equivalent to b00111111.
- 8`b1111 is an eight-bit wide binary value of b00001111.

Further reading

This section lists publications by ARM Limited, and by third parties.

ARM Limited periodically provides updates and corrections to its documentation. See `http://www.arm.com` for current errata sheets, addenda, and the Frequently Asked Questions list.

ARM publications

This manual contains information that is specific to the SC054 ASB Static Memory Controller. See the following documents for other relevant information:

- AMBA Specification (Rev 2.0) (ARM DDI 0011)
- *Example AMBA System (Micropack v1.3) Technical Reference Manual* (ARM DDI 0138).

Feedback

ARM Limited welcomes feedback on the SC054 ASB Static Memory Controller and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier giving:

- the product name
- a concise explanation of your comments.

Feedback on this manual

If you have any comments on this manual, send your emails to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments apply
- a concise explanation of your comments.

ARM Limited also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter introduces the SC054 ASB Static Memory Controller and contains the following section:

- *About the SC054 ASB Static Memory Controller* on page 1-2.

1.1 About the SC054 ASB Static Memory Controller

The SC054 ASB *Static Memory Controller* (SMC) is an *Advanced Microcontroller Bus Architecture* (AMBA) compliant System-on-Chip peripheral that is developed, tested, and licensed by ARM.

The SC054 ASB SMC is an AMBA slave module, and connects to the Advanced System Bus (ASB).

The SC054 ASB SMC is a reusable soft-IP block that has been developed with the prime aim of reducing time-to-market for ASIC development.

A carefully chosen set of design rules has been followed to allow faster integration in most ASIC design flows using standard synthesis and test tools. You can easily customize the implementation to suit specific customer requirements.

For more information on AMBA refer to the *AMBA Specification (Rev 2.0)*.

1.1.1 Features of the SC054 ASB SMC

The SC054 ASB SMC macro block offers the following features:

- soft macrocell available in VHDL
- fully scan insertable design
- functional verification using ARM BusTalk functional test environment
- compatibility with AMBA ASB on-chip bus systems.

The SC054 ASB SMC supports:

- static memory-mapped devices including RAM, ROM, FLASH, and Burst ROM
- asynchronous page mode read operation in non-clocked memory subsystems
- asynchronous burst mode read access to burst mode ROM devices
- 8, 16, and 32-bit wide external memory data paths
- little-endian and big-endian memory architectures
- independent configuration for up to eight memory banks, each up to 8MB
- programmable wait states (up to 32)
- decode cycle in ASB address decoder (WAIT state in the first cycle of nonsequential transfers)
- chip select polarity programmability for each bank independently
- external asynchronous wait control by external memory controller

- programmability of polarity of the external wait input signal
- handshaking for interfacing to shared memory bus systems
- interfacing to ARM *Test Interface Controller* (TIC) in both single and shared memory bus systems.

The SC054 ASB SMC is not compatible with AMBA address decoders that have no decode cycle.

Figure 1-1 shows a diagram of a typical ASB-based microcontroller system with a TIC interface, through the SC054 ASB SMC.

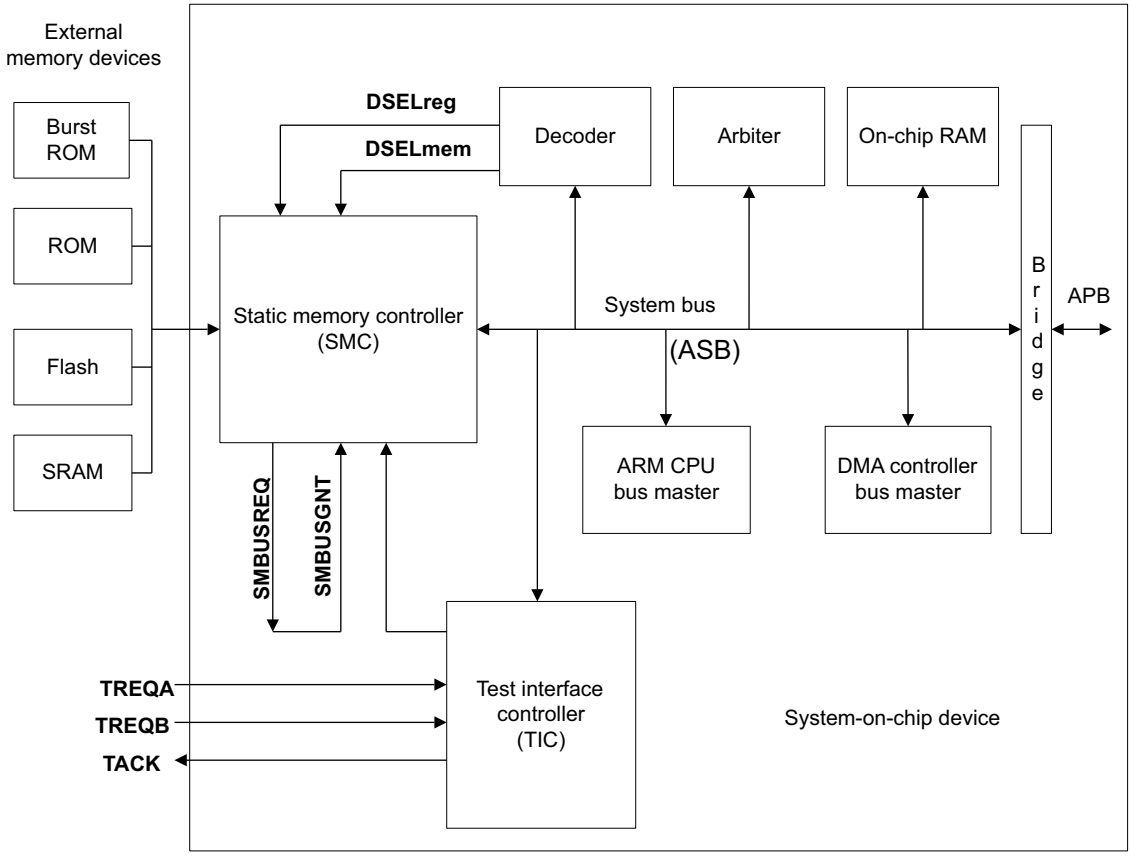


Figure 1-1 Typical ASB-based microcontroller system with a TIC interface through the SC054 ASB SMC

In the above configuration, that can be classed as a single memory bus system, the TIC access is performed through the SC054 ASB SMC interface. The bus arbitration signals are not used, but must be tied together.

Figure 1-2 shows a diagram of a typical ASB-based microcontroller system with a TIC interface through a shared memory bus system.

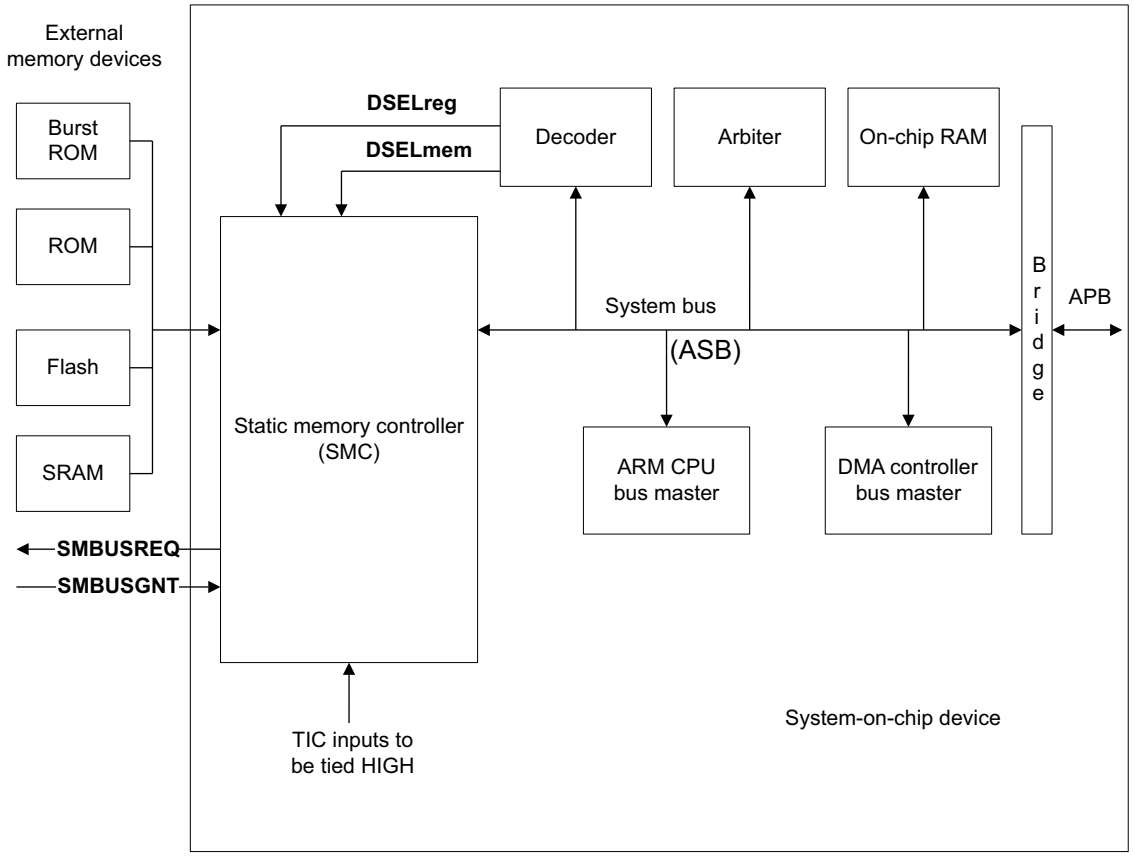


Figure 1-2 Typical ASB-based microcontroller system with a TIC interface through a shared memory bus system

In the above configuration, the handshaking signals **SMBUSREQ** and **SMBUSGNT,** can be used to facilitate the implementation of a shared memory bus system where pin count can be reduced. In this case the TIC controller is also connected to the shared bus as a bus master, with its appropriate bus request and grant signals. The inherent TIC interface signals are not used and must be tied HIGH.

Figure 1-3 on page 1-5 shows a diagram of the SC054 ASB SMC input/output connections.

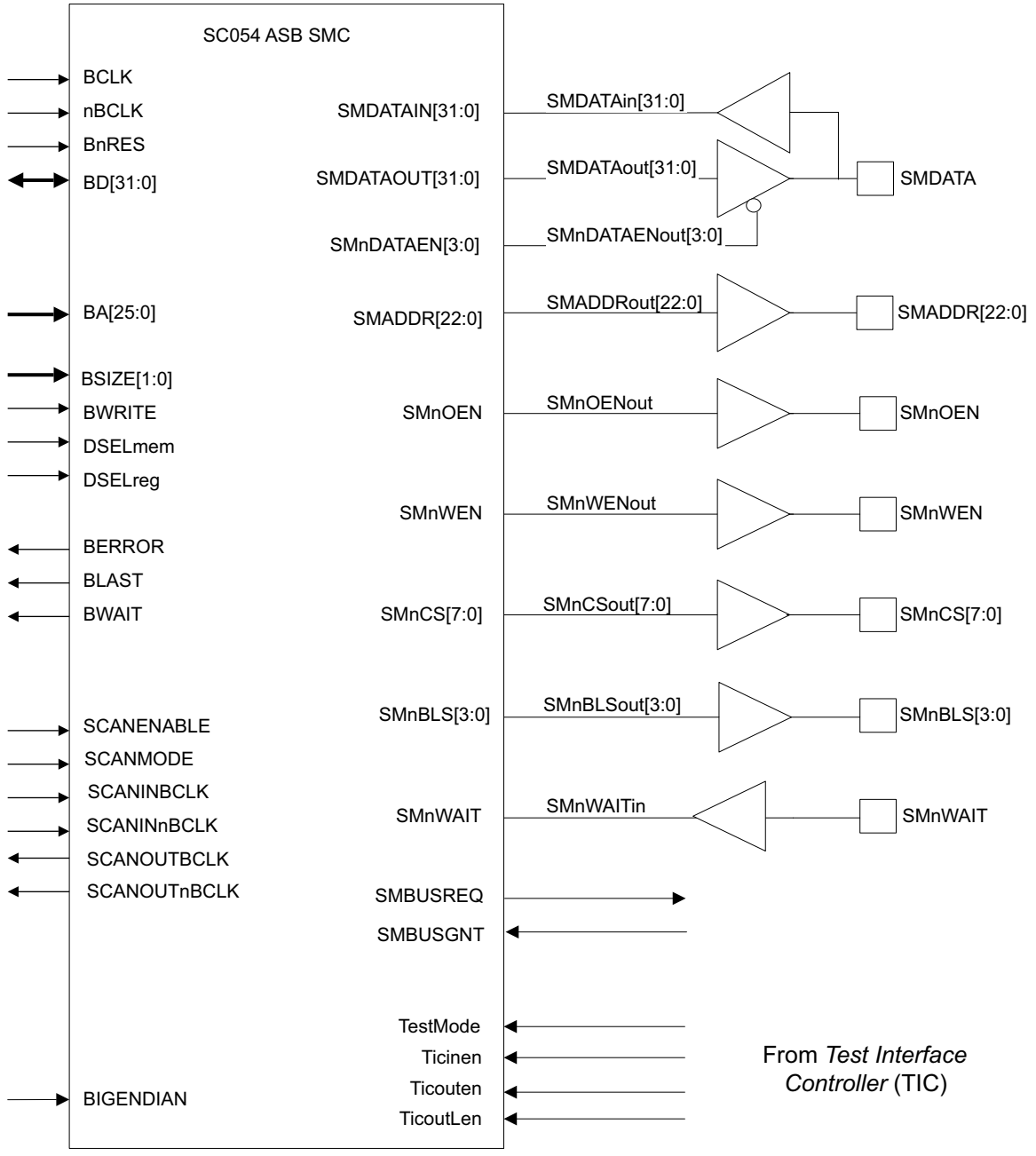


Figure 1-3 SC054 ASB SMC input/output connections

Chapter 2
Functional Overview

This chapter describes the SC054 ASB Static Memory Controller operation. It contains the following sections:

2.1 About the SC054 ASB SMC

The SC054 ASB(SMC) is an AMBA ASB slave module that can be used to provide an interface between an AMBA ASB system bus and external (off-chip) memory devices.

The SC054 ASB SMC provides support for up to eight independently configurable memory banks simultaneously. Each memory bank is capable of supporting:

- SRAM
- ROM
- flash EPROM
- burst ROM memory.

Each memory bank can use devices using either 8, 16, or 32-bit external memory data paths.

You can configure the SC054 ASB SMC to support either little-endian or big-endian operation.

The SC054 ASB SMC is only designed to work with an AMBA address decoder that implements a decode cycle by inserting a wait state in the first cycle of NONSEQUENTIAL transfers. This ensures that systems with high **BCLK** frequency have sufficient time for the decoder to examine high-order address lines and assert the appropriate DSELx select lines during the HIGH phase of decode cycle.

The SC054 ASB SMC is not compatible with AMBA address decoders that have no decode cycle.

You can configure the SC054 ASB SMC memory banks to support:

- nonburst read and write accesses only to high-speed CMOS Static RAM, for example Samsung KM681002A
- nonburst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory, for example Intel 28F800F3 and 28F160F3.

A block diagram of the SC054 ASB SMC is shown in Figure 2-1 on page 2-3.

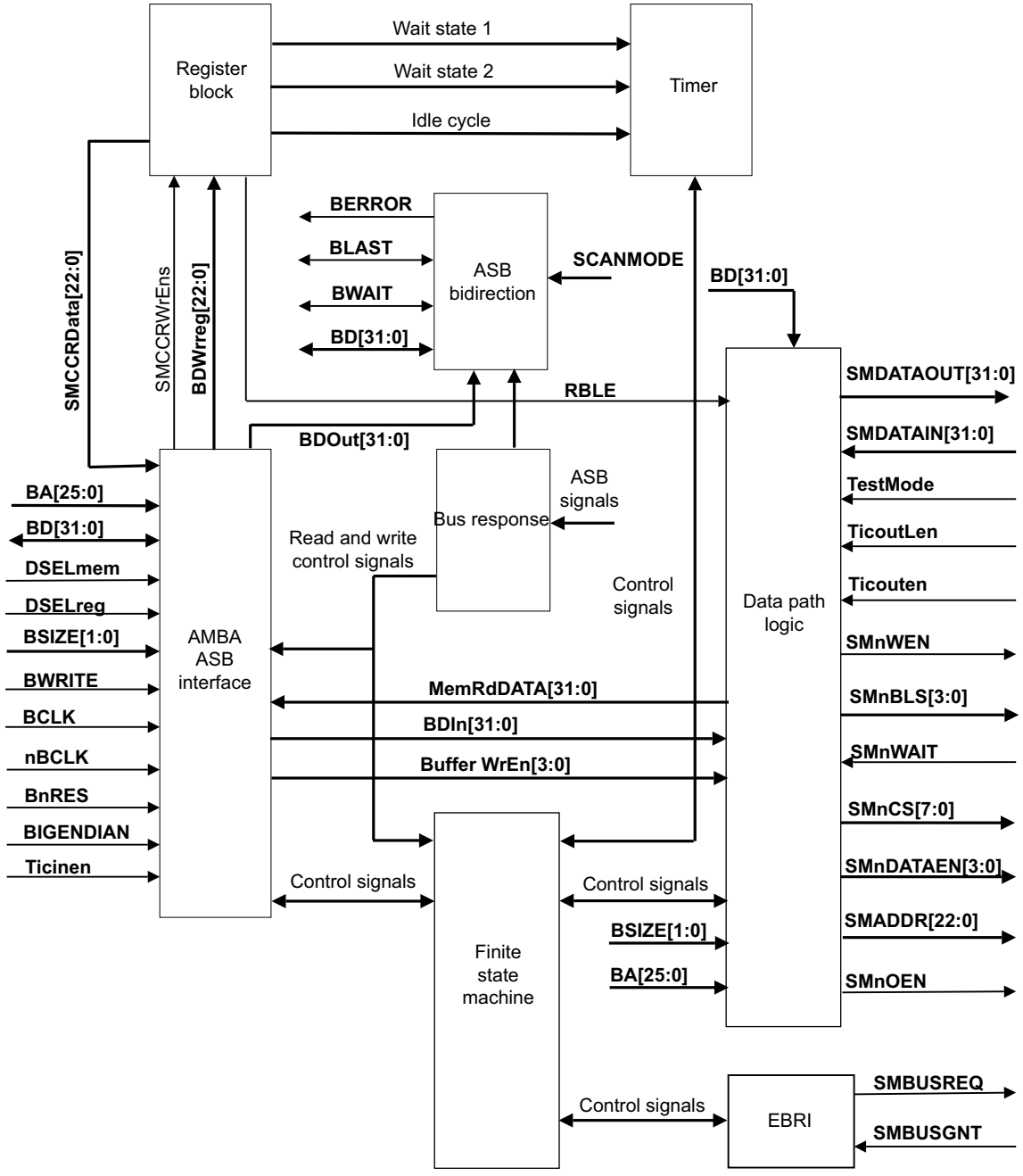


Figure 2-1 SC054 ASB SMC block diagram

The sub-blocks in the SC054 ASB SMC design are described below:

- *AMBA ASB interface*
- *Register block*
- *Timing control*
- *Bus response state machine*
- *External memory control logic*
- *External memory data path logic* on page 2-5
- *External bus request interface* on page 2-5.

2.1.1 AMBA ASB interface

The AMBA ASB interface:

- decodes the base address for external memory banks and bank configuration registers
- controls read and write transfers to registers from the AMBA ASB.

2.1.2 Register block

The register block implements the memory bank configuration registers. Read and write transfers to these registers are controlled by the AMBA ASB interface. The values programmed in these registers are used by the timing control block that generates external memory control signals in the external memory control logic.

2.1.3 Timing control

The timing block contains a 6-bit counter that is used to generate:

- wait states for read and write accesses
- bus turnaround cycles between read and write transfers on the external data bus.

2.1.4 Bus response state machine

This block generates the bus response signals, **BWAIT**, **BLAST,** and **BERROR**, based on control information from other blocks.

2.1.5 External memory control logic

External memory banks control logic gets the asynchronous wait input during the external wait control mode.

External memory banks control logic generates the following control signals:

- chip selects for the memory banks

- write enables for the internal buffers
- write enables for external memory bank
- read enables for read data from external memory to AMBA ASB interface
- data sequencing for both memory read and write
- output enable for the external memory banks
- external databus enable
- control signals to timing control block.

2.1.6 External memory data path logic

The external memory data path logic includes a 4-word buffer and control logic to interface the TIC to the AMBA ASB bus.

Write enables to buffers are generated from the external memory interface logic. Control signals from the external memory interface logic block are used to:

- drive write data from the memory buffer on SMDATAOUT bus for the write request from the AMBA ASB master
- drive read data to the AMBA ASB interface either from the buffer or SMDATAIN bus for the read request from the AMBA ASB master.

2.1.7 External bus request interface

The *External Bus Request Interface* (EBRI) is used in shared memory bus architectures. It raises a request signal (**SMBUSREQ**) when it requires access to the external bus. When it is granted access (**through SMBUSGNT**) it accesses the external bus, but keeps **SMBUSREQ** HIGH. **SMBUSREQ** is taken LOW at the end of the access.

Note

In a system where EBRI is not utilized, signals **SMBUSREQ** and **SMBUSGNT** must be tied together.

2.2 SC054 ASB SMC operation

The functions of SC054 ASB SMC are described under the following headings:

- *Memory bank select*
- *Access sequencing and memory width* on page 2-8
- *Wait state generation* on page 2-8
- *Write protection* on page 2-10
- *Static memory read control* on page 2-10
- *Static memory write control* on page 2-14
- *Byte lane write control* on page 2-16
- *External bus interface* on page 2-19
- *System test access* on page 2-20
- *External wait control mode* on page 2-21.

2.2.1 Memory bank select

Eight independently-configurable memory banks are supported, with separate programmable polarity chip select outputs for each bank.

Note

On assertion of **BnRES**, all chip select outputs are set HIGH.

The memory bank selection is controlled by the AMBA ASB address lines BA[25:23], as shown in Table 2-1.

Table 2-1 Static memory bank select coding

BA [25:23]	CSPol[x]	SMnCS[x]	Memory configuration
000	0	0 (default)	Bank 0 (SMnCS[0])
000	1	1	Bank 0 (SMnCS[0])
001	0	0 (default)	Bank 1 (SMnCS[1])
001	1	1	Bank 1 (SMnCS[1])
010	0	0 (default)	Bank 2 (SMnCS[2])
010	1	1	Bank 2 (SMnCS[2])
011	0	0 (default)	Bank 3 (SMnCS[3])
011	1	1	Bank 3 (SMnCS[3])

Table 2-1 Static memory bank select coding (continued)

BA [25:23]	CSPol[x]	SMnCS[x]	Memory configuration
100	0	0 (default)	Bank 4 (SMnCS[4])
100	1	1	Bank 4 (SMnCS[4])
101	0	0 (default)	Bank 5 (SMnCS[5])
101	1	1	Bank 5 (SMnCS[5])
110	0	0 (default)	Bank 6 (SMnCS[6])
110	1	1	Bank 6 (SMnCS[6])
111	0	0 (default)	Bank7 (SMnCS[7])
111	1	1	Bank7 (SMnCS[7])

The base address of the external memory banks and the base address of the SC054 ASB SMC memory bank configuration registers, must both be defined in the address decoder for AMBA ASB slave select signals **DSELmem** and **DSELreg**.

If the default base address of the external memory banks begins at `0x00000000`, then the memory banks occupy address space up to `0x3FFFFFF` (8 x 8MB). The base address for the bank configuration registers must then be located above the memory bank address space.

Table 2-2 shows the address mapping of **BA[25:0]** for external memory banks.

Table 2-2 Address mapping for external memory banks

31-26	25:23	22-0
Base address for memory bank	Chip select address space for eight memory banks	8MB memory banks address space

Table 2-3 shows the address mapping of **BA[31:0]** for memory bank configuration registers.

Table 2-3 Address mapping for memory bank configuration registers

31-5	4-2	1-0
Base address for SC054 ASB SMC memory bank configuration registers	SMCBCRx register select	Byte select

2.2.2 Access sequencing and memory width

You must configure the data width of each external memory bank data by programming the appropriate bank configuration register SMCBCRx. When the external memory bus is narrower than the transfer initiated from the current AMBA bus master, the internal bus transfer takes several external bus transfers to complete. For example, in the case that Bank 0 is configured as 8-bit wide memory and a 32-bit read is initiated, the AMBA ASB bus is appropriately waited while the SC054 ASB SMC reads four consecutive bytes from the memory. During these accesses the data path is controlled (in the external bus interface) to demultiplex the four bytes into one 32-bit word on the AMBA ASB bus.

The access sequencing supports both little-endian and big-endian operation as defined by a dedicated **BIGENDIAN** input signal to the SC054 ASB SMC.

2.2.3 Wait state generation

You must configure each bank of the SC054 ASB SMC for wait states in read and write accesses. This is achieved by programming the appropriate fields of the bank configuration registers SMCBCRx.

Wait state control refers to external transfer wait states. The number of cycles in which an AMBA transfer completes is controlled by two other factors:

- access width
- external memory width.

You can program the WST1 wait state field to select from 1 to 32 wait states for read memory accesses to SRAM and ROM, or the initial burst read access to burst ROM.

You can program the WST2 wait state field to select from 0 to 32 wait states for write access to SRAM or 0 to 31 wait states in the case of burst mode reads from Burst ROM devices. For example, the configuration for an access to a burst ROM with a 120ns initial access time followed by a 60ns burst access time, using a 150MHz system clock is 18 wait states for the first access and 9 for the subsequent accesses.

The SC054 ASB SMC can also be configured for each memory bank to use external bus turnaround cycles between read and write memory accesses. The IDCY field can be programmed for 1 to 16 bus turnaround wait cycles. This is to avoid bus contention on the external memory data bus.

Figure 2-2 on page 2-9 illustrates a single bus turnaround cycle added before a write access that follows a read access.

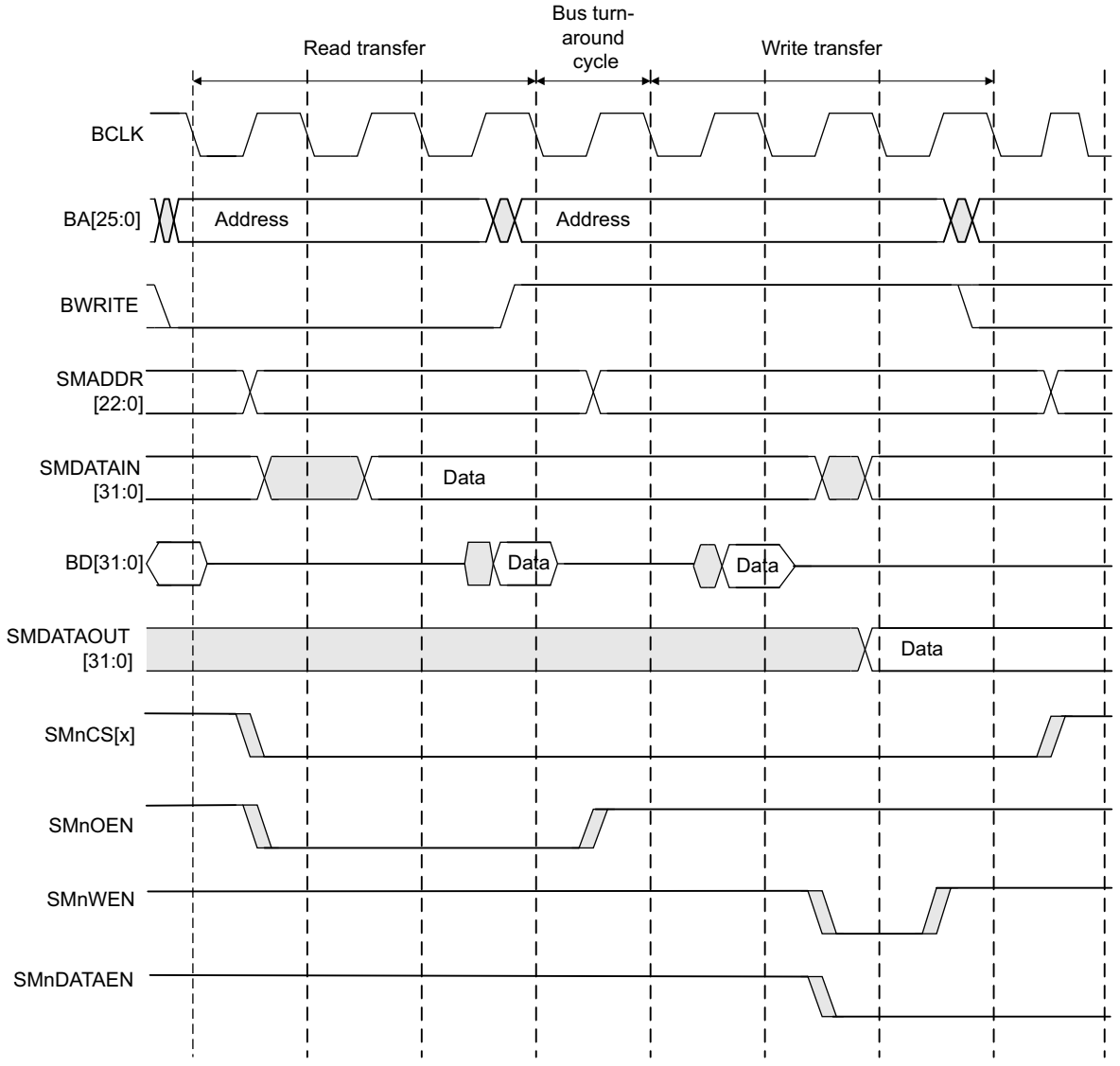


Figure 2-2 External data bus turnaround timing diagram

After the read transfer completes successfully, read data is driven onto **BD[31:0]** and a DONE response is given. **BA** and **BWRITE** then change immediately. As the next transaction is a write, there is a one cycle turnaround to avoid possible external bus contention. Data is then transferred from **BD** to **SMDATAOUT**.

2.2.4 Write protection

You can configure each memory bank for write protection. Usually SRAM is unprotected and ROM devices must be write-protected, but you can set the WP field in the bank configuration registers SMCBCRx to write protect SRAM in addition to ROM devices.

If a write access is made to a write protected memory bank, an error is indicated by the signals **BERROR**, **BWAIT,** and **BLAST**. If a write access is made to a read only memory bank that is not write protected, no error indication is returned.

2.2.5 Static memory read control

The static memory read controls are described in the following sections:

- *ROM, SRAM, and FLASH*
- *Burst ROM* on page 2-12.

ROM, SRAM, and FLASH

The SC054 ASB SMC has the same type of read timing control for ROM, SRAM, and FLASH devices. Each read starts with the assertion of the appropriate memory bank chip select signals **SMnCS[x]** and memory address **SMADDR[22:0]**. The read access time is determined by the number of wait states programmed for the WST1 field of the bank configuration register SMCBCRx. The IDCY field in the bank configuration register determines the number of bus turnaround wait cycles added between external read and write transfers.

Figure 2-3 on page 2-11 shows an external memory read transfer with the minimum one WAIT state (WST1 = 0).

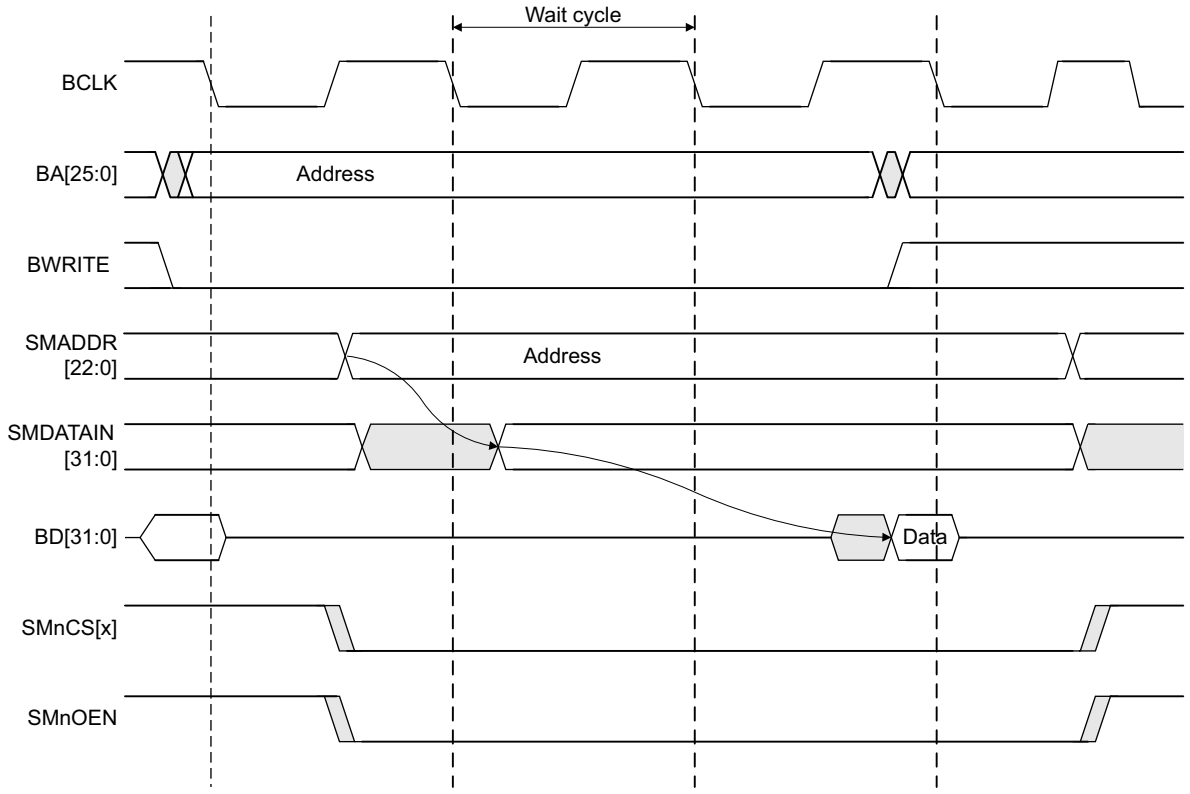


Figure 2-3 External memory one WAIT state read timing diagram

Figure 2-4 on page 2-12 shows an external memory read transfer with two WAIT states (WST1 = 1).

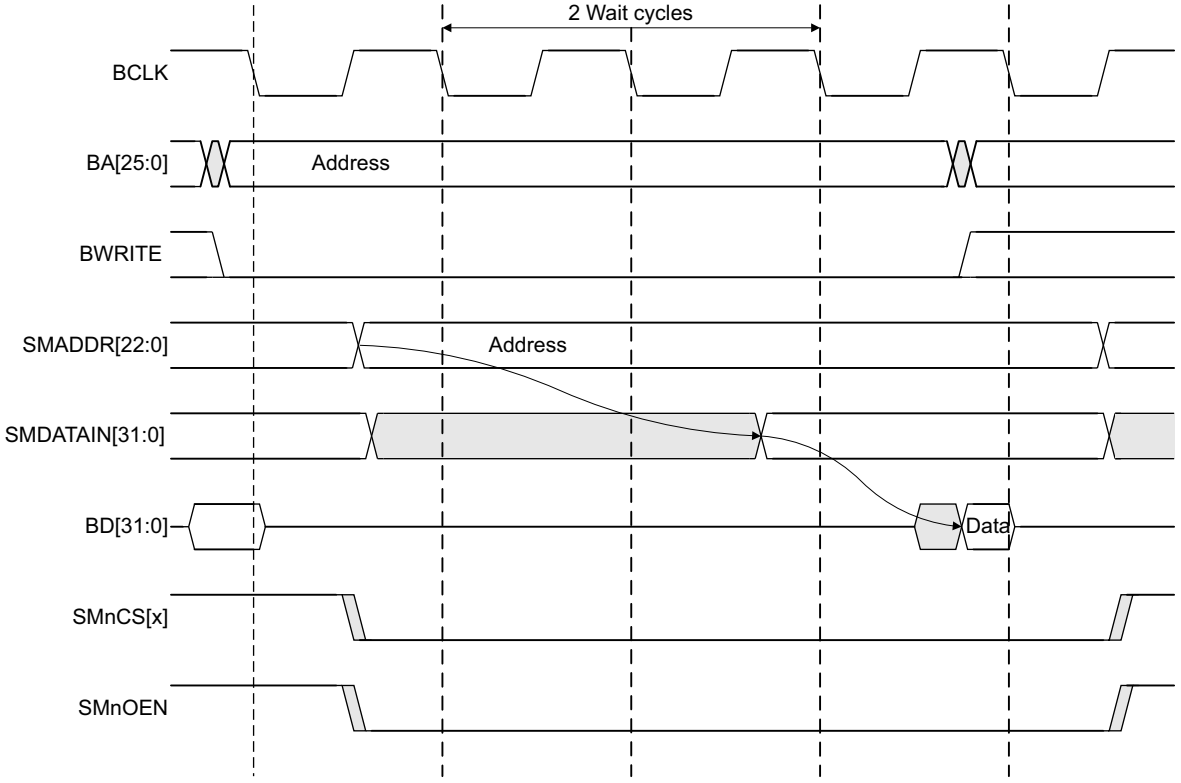


Figure 2-4 External memory two WAIT state read timing diagram

Burst ROM

The SC054 ASB SMC supports sequential access burst reads of up to four consecutive locations in 8, 16, or 32-bit memories. This feature supports burst mode ROM devices and increases the bandwidth by using a reduced (configurable) access time for three sequential reads following a quad-location boundary read.

Note

Quad-location boundaries occur when:
BA[1:0] = 11 for byte-wide memories, or
BA[2:1] = 11 for halfword memories, or
BA[3:2] = 11 for word memories.

Burst ROM read behavior

For the burst ROM the property of slower initial access (as programmed in the WST1 register) and subsequent faster access (as programmed in the WST2 register) is exploited. The WST2 for the subsequent access is used until the quad boundary for the memory device is reached. The quad boundary for different memory device sizes are indicated in the note under question.

For example, if the first access is to boundary for a byte wide device, which occurs when **BA[1:0] =** 11, then it means that the quad location boundary is already reached. The next read access is done again with the longer access time as in WST1. The subsequent read accesses then use the faster access time as in WST2 until the quad location is reached.

Figure 2-5 on page 2-14 shows an external memory burst read transfer, using 2 initial WAIT states and 0 WAIT cycles for the subsequent burst read accesses. The transfer size is 32 bits wide, but the memory is only byte wide. Therefore, in this case a word is built up from four byte reads.

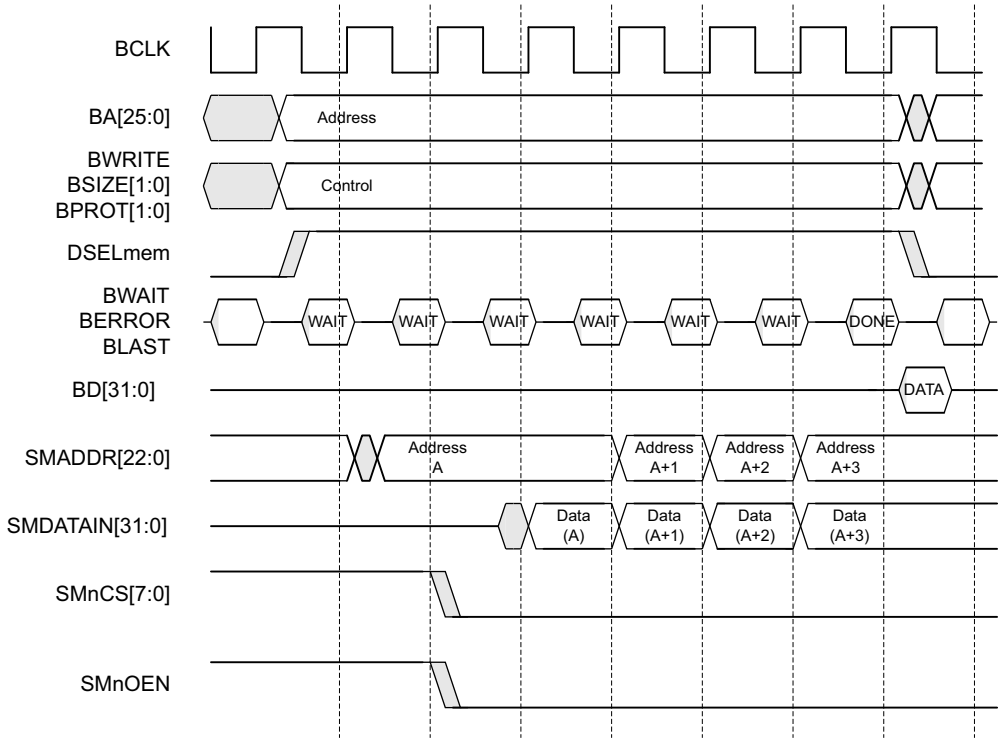


Figure 2-5 External memory burst read timing diagram

2.2.6 Static memory write control

Write timing is described in the following sections:

- *SRAM*
- *FLASH* on page 2-16.

SRAM

Write timing for SRAM starts with assertion of the appropriate memory bank chip selects **SMnCS[x]** and address signals **SMADDR[22:0]**. The write access time is determined by the number of wait states programmed for the WST2 field of the bank configuration register SMCBCRx. The IDCY field in the bank configuration register determines the number of bus turnaround wait cycles added between external read and write transfers.

Figure 2-6 on page 2-15 shows an external memory write transfer with minimum one WAIT state (WST2 = 0).

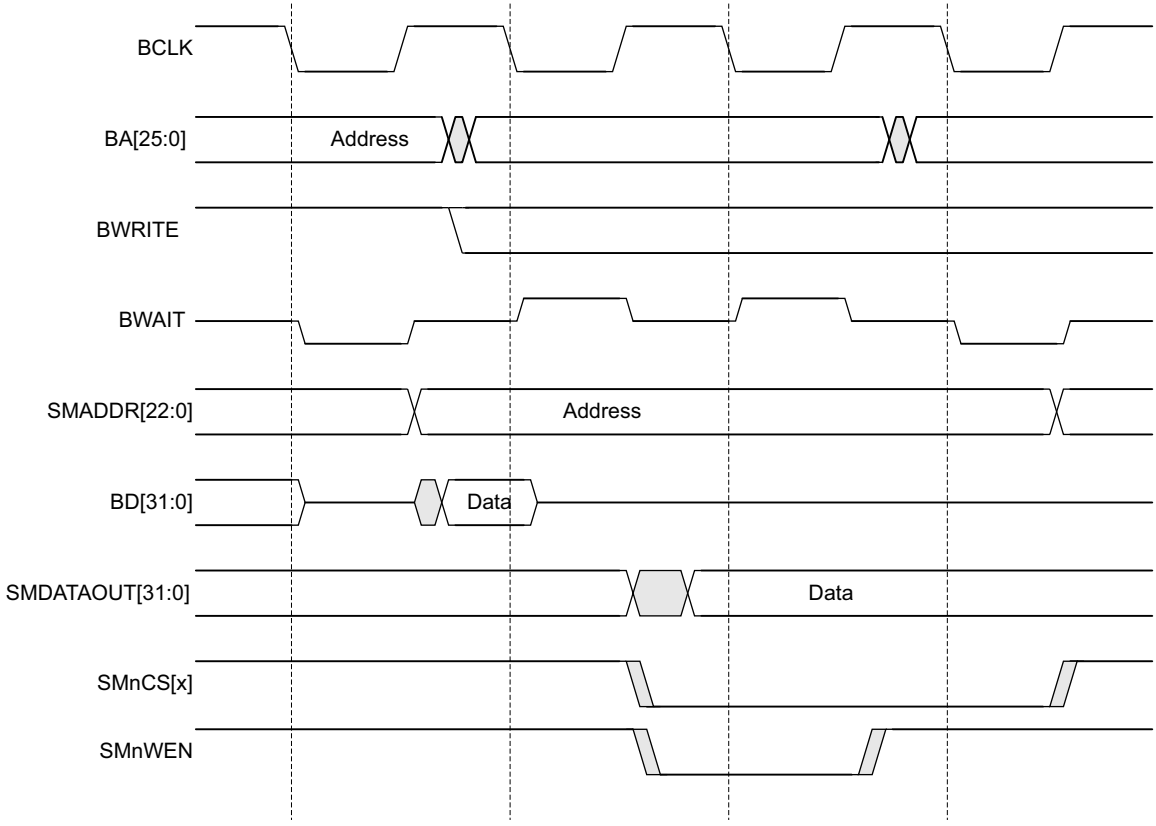


Figure 2-6 External memory one WAIT state write timing diagram

Figure 2-7 on page 2-16 shows an external memory write transfer with two WAIT states (WST2 = 1).

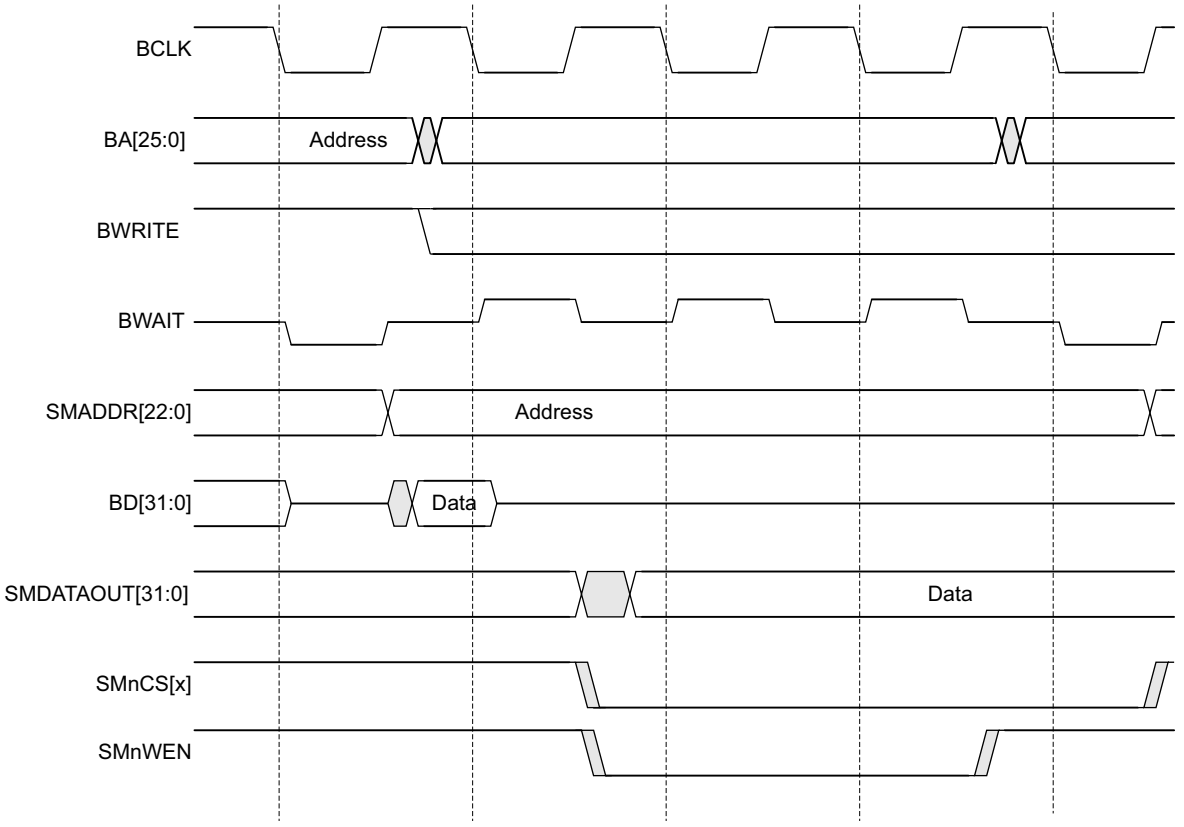


Figure 2-7 External memory two WAIT state write timing diagram

FLASH

Write timing for flash memory devices is the same as for SRAM devices.

2.2.7 Byte lane write control

The SC054 ASB SMC generates byte lane write control signals **SMnBLS[3:0]** according to:

- AMBA transfer width (indicated by **BSIZE[1:0]**)
- external memory data bus width, **BA[1:0]**
- access sequencing.

Table 2-4 shows the basic coding assuming 32-bit external memory.

Table 2-4 SMnBLS coding

BSIZE[1:0]	BA [1:0]	SMnBLS[3:0] (little-endian)	SMnBLS[3:0] (big-endian)
10 (word)	XX	0000	0000
01 (halfword)	1X	0011	1100
01 (halfword)	0X	1100	0011
00 (byte)	11	0111	1110
00 (byte)	10	1011	1101
00 (byte)	01	1101	1011
00 (byte)	00	1110	0111

Both big-endian and little-endian operations are supported as defined by a dedicated input signal to the SC054 ASB SMC.

Word transfers are the largest sized transfers supported by the SC054 ASB SMC. Any access attempted with a size greater than a word is treated as invalid and causes the error response to be generated.

Figure 2-8 on page 2-18 shows typical connections for a little-endian memory system with different data width memory devices.

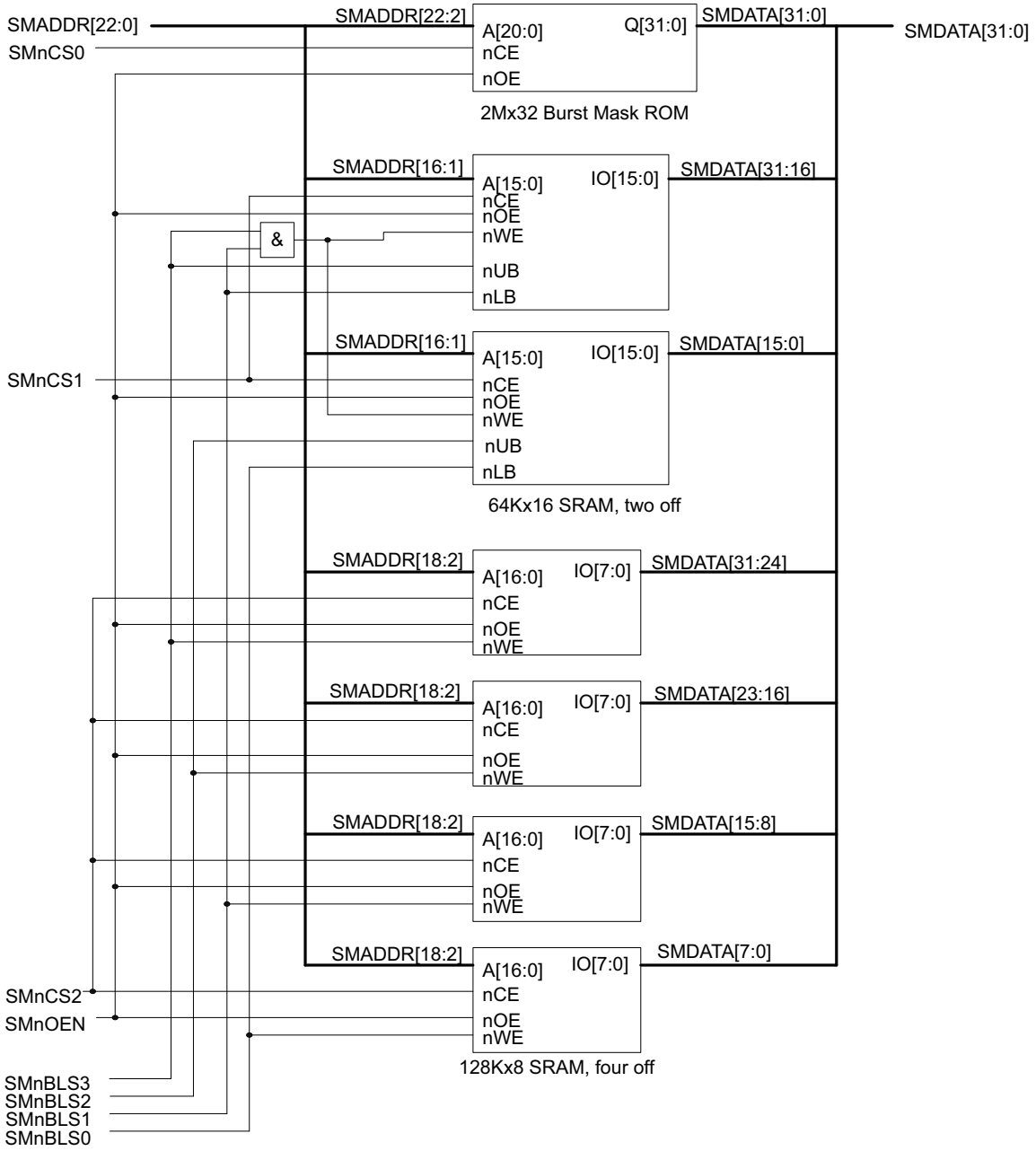


Figure 2-8 Typical memory connection diagram

If the device is a byte partioned device with the memory constructed using 16-bit, or 32-bit devices, this is indicated by programming the RBLE = 1 in the configuration register. In this case both the **SMnWEN** and **SMnBLS** signals are used. The **SMnWEN** gates the **SMnBLS** lines.

If the device is a nonbyte partioned device with the memory constructed using only 8-bit devices, this is indicated by programming RBLE = 0. Here the **SMnWEN** line is not used and only **SMnBLS** lines are used as write enables for the memory device.

2.2.8 External bus interface

To ensure low-power operation, the transitions on the external address bus are kept to a minimum by enabling the address bus transitions only during memory accesses.

The data out path allows 32-bit AMBA writes to be converted into several external memory halfword or byte writes. The separate byte lane write signals ensure that the entire memory bus is driven at all times, no matter what width of memory is being accessed. The data in path constructs 32-bit ASB data words from halfword and byte wide external static memory devices. For buses less than 32-bits wide unused bits are automatically driven by the SC054 ASB SMC. Devices are always connected from bit 0 upwards for both little and big-endian configurations.

The **SMBUSREQ** signal is driven HIGH when external bus access is required. After the **SMBUSGNT** signal is received the SC054 ASB SMC starts driving address and data information on the next cycle. The SC054 ASB SMC keeps the **SMBUSREQ** signal HIGH as long as it requires the bus. Once the external transaction is completed **SMBUSREQ** is driven LOW. Figure 2-9 shows when **SMBUSGNT** is given immediate access to the bus, and Figure 2-10 on page 2-20 shows when the access is delayed for two cycles because another memory controller is accessing the bus.

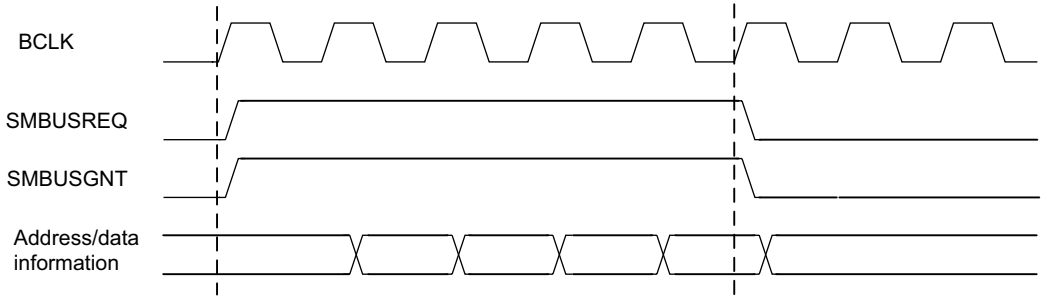


Figure 2-9 Access granted immediately

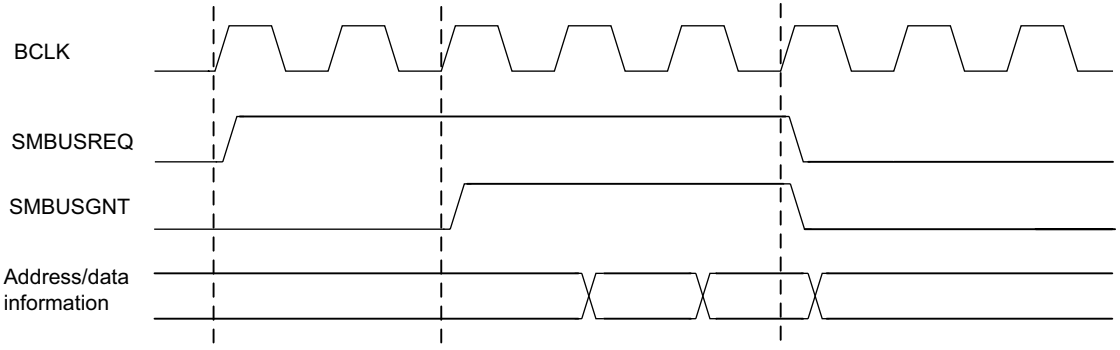


Figure 2-10 Access delayed two cycles

When the EBRI is not required the SC054 ASB SMC supports the use of its external memory data bus as the bidirectional test port (TBUS) for the AMBA TIC. The system allows testing by application of parallel TicTalk test vectors through the external bus interface to test AMBA blocks by creating bus transfers on the AMBA ASB and AMBA APB buses. For systems using less than 32-bit external data width, other device pins (for example the address pins) must have special test functionality to provide a 32-bit test data width, connecting bidirectional pads that can act as inputs during system test.

Note

When the SC054 ASB SMC is using the EBRI the TIC inputs must be tied HIGH.

2.2.9 System test access

You can use the SC054 ASB SMC with a TIC AMBA bus master for system testing.

During system test the SC054 ASB SMC is controlled by three active LOW signals from the TIC:

- **Ticinen** (test data in enable)
- **Ticouten** (test data out enable)
- **TicoutLen** (test data out latch).

For more information on system test and the TIC, see the *AMBA Specification (2.0)* and the *Example AMBA System Technical Reference Manual*.

For the SC054 ASB SMC, **BCLK** is used as **TCLK** and **SMDATA** as **TBUS**. The TIC signals control the data bus drivers directly. It is necessary to override the normal operation of the SMC interface when in test mode. This is done with the **TestMode** signal from the TIC.

2.2.10 External wait control mode

The SC054 ASB SMC supports the extension of the access cycle by an external device like an external memory controller by using the **SMnWAIT** input pin of the SC054 ASB SMC. For this you must program appropriately the WaitEn bit of the bank configuration registers SMCBCRx.

The polarity of the external **SMnWAIT** input is programmed through the WaitPol field of the SMCBCRx register. In the external wait control mode the SC054 ASB SMC looks for the assertion of the **SMnWAIT** input line. The SC054 ASB SMC is in the wait mode as long as the **SMnWAIT** input line is asserted. The transaction completes as soon as the **SMnWAIT** line is deasserted.

In the wait enabled or external wait control mode, when the SC054 ASB SMC is waiting for the **SMnWAIT** assertion, it also starts counting down according to the values programmed in the wait state count field (that is WST1 and WST2 respectively). The external memory controller must assert the **SMnWAIT** line before the expiry of the WST1 or WST2 counters, otherwise the transaction completes on expiry.

In the external wait enable or control mode, it is recommended that the maximum values (default on reset) are programmed into the WST1 and WST2 fields, otherwise the transaction completes on expiry. If the external wait control mode is disabled, then the SC054 ASB SMC ignores the **SMnWAIT** input, and the access time is generated normally according to the values programmed in the WST1 and WST2 registers.

Chapter 3
Programmer's Model

This chapter describes the registers of the SC054 ASB Static Memory Controller and provides details required when programming the microcontroller. It contains the following:

3.1 About the programmer's model

You can configure the base addresses for the SC054 ASB SMC bank configuration registers and memory banks to suit each particular system implementation. The base addresses must be configured by constant definitions in the Hardware Description Language (HDL) code for the AMBA address decoder. The base addresses are not software-programmable.

The SC054 ASB SMC registers and memory banks have fixed address offsets from the base addresses described above.

3.2 SC054 ASB SMC memory bank address space

The SC054 ASB SMC memory bank address space is shown in Table 3-1.

Table 3-1 SC054 ASB SMC memory bank address space

Address	Description
SMC MemBase + `0x00000000`	SMC memory bank 0
SMC MemBase + `0x00800000`	SMC memory bank 1
SMC MemBase + `0x01000000`	SMC memory bank 2
SMC MemBase + `0x01800000`	SMC memory bank 3
SMC MemBase + `0x02000000`	SMC memory bank 4
SMC MemBase + `0x02800000`	SMC memory bank 5
SMC MemBase + `0x30000000`	SMC memory bank 6
SMC MemBase + `0x03800000`	SMC memory bank 7

SMC MemBase is the base address of the SC054 ASB SMC memory banks.

3.3 SC054 ASB SMC registers

The SC054 ASB SMC registers are shown in Table 3-2.

Table 3-2 SC054 ASB SMC register summary

Address	Type	Width	Reset value	Name	Description
SMCCR RegBase + 0x00	Read/write	32	0x1000FBEF	SMCBCR0	Configuration register for memory bank 0
SMCCR RegBase + 0x04	Read/write	32	0x1000FBEF	SMCBCR1	Configuration register for memory bank 1
SMCCR RegBase+ 0x08	Read/write	32	0x1000FBEF	SMCBCR2	Configuration register for memory bank 2
SMCCR RegBase + 0x0C	Read/write	32	0x1000FBEF	SMCBCR3	Configuration register for memory bank 3
SMCCR RegBase + 0x10	Read/write	32	0x1000FBEF	SMCBCR4	Configuration register for memory bank 4
SMCCR RegBase + 0x14	Read/write	32	0x1000FBEF	SMCBCR5	Configuration register for memory bank 5
SMCCR RegBase + 0x18	Read/write	32	0x1000FBEF	SMCBCR6	Configuration register for memory bank 6
SMCCR RegBase + 0x1C	Read/write	32	0x1000FBEF	SMCBCR7	Configuration register for memory bank 7

SMC RegBase is the base address of the SC054 ASB SMC memory banks.

3.3.1 Bank configuration registers SMCBCR0-7

The descriptions of the bits for the bank configuration registers are given in Table 3-3.

Table 3-3 SMCBCR 0 - 7 register definition

Bits	Name	Type	Description
31-30	AT	Read/write	Reserved, do not modify, unpredictable when read.
29-28	MW	Read/write	Memory width:[a] 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = reserved.
27	BM	Read/write	Burst mode: 0 = nonburst devices (default at reset) 1 = burst ROM.
26	WP	Read/write	Write protect: 0 = SRAM, not write protected (default at reset) 1 = ROM, burst ROM and SRAM are write-protected.
25	WPERR	Read/write	Write protect error status flag, read: 0 = no error (default at reset) 1 = write protect error. Writing a 1 to this bit clears the write protect error status flag.
24	BUSERR	Read/write	Bus transfer error status flag, read: 0 = no error (default at reset) 1 = bus transfer error. Writing a 1 to this bit clears the bus transfer error status flag.
23	CSPol	Read/write	Chip select polarity bit indication for each bank: 0 = active LOW CS (default at reset) 1 = active HIGH CS.
22	WaitEn	Read/write	External memory controller wait signal enable: 0 = the SC054 ASB SMC is not controlled by the external wait signal (default at reset) 1 = the SC054 ASB SMC looks for the external wait input signal, **SMnWAIT**.

Table 3-3 SMCBCR 0 - 7 register definition (continued)

Bits	Name	Type	Description
21	WaitPol	Read/write	Polarity of the external wait input for activation: 0 = the **SMnWAIT** signal is active LOW (default at reset) 1 = the **SMnWAIT** signal is active HIGH.
20-16	-	-	Reserved, do not modify, unpredictable when read.
15-11	WST2	Read/write	Wait state 2. Defaults to 11111 at reset. SRAM, the WST2 field controls the number of wait states for write accesses. This wait state time is (WST2 + 1) x **tBCLK** in the case of SRAM. Burst ROM, the WST2 field controls the number of wait states for the burst read accesses after the first read. This wait state time is (WST2) x **tBCLK** in the case of burst ROM. ROM: WST2 does not apply to ROM devices.
10	RBLE	Read/write	Read byte lane enable. Defaults to 0 at reset. 0 = SMnBLS[3:0] all deasserted HIGH during system reads from external memory. 1 = SMnBLS[3:0] all asserted LOW during system reads from external memory.
9-5	WST1	Read/write	Wait state 1. Defaults to 11111 at reset. SRAM and ROM, the WST1 field controls the number of wait states for read accesses. Burst ROM, the WST1 field controls the number of wait states for the first read access only. Wait state time = (WST1 + 1) x **tBCLK**.
4	-	-	Reserved, do not modify, unpredictable when read.
3-0	IDCY	Read/write	Idle or turnaround cycles. Defaults to 11111 at reset. This field controls the number of bus turnaround cycles added between read and write accesses, to prevent bus contention on the external memory data bus. The turn around time is (IDCY + 1) x **tBCLK**.

a. In the SC054 ASB SMC, the MW field defaults to 16-bit width for all memory banks at reset, (see Table 3-4 on page 3-7).

Table 3-4 SC054 ASB SMC reset default memory width

SMC memory bank	Default memory width
Bank 0	16-bit
Bank 1	16-bit
Bank 2	16-bit
Bank 3	16-bit
Bank 4	16-bit
Bank 5	16-bit
Bank 6	16-bit
Bank 7	16-bit

At reset the memory bank default external memory width is as shown in Table 3-4.

Note

If the system boots from a Bank0 external ROM device that is not 16-bit wide, you must amend the VHDL RTL code and the C verification test program to configure the correct default external memory width at reset.

Appendix A
SC054 ASB Static Memory Controller Signal Descriptions

This chapter describes the ASB and module-specific non-ASB signals used with the ARM SC054 ASB SMC. It contains the following sections:

A.1 ASB interface signals

The SC054 ASB SMC is connected to the ASB as a bus slave. Refer to Table A-1 for a list of the ASB interface signals.

Table A-1 ASB signals

Signal name	Type	Source/ destination	Description
BCLK	Input	Clock control	Bus clock input, that times all bus transfers.
nBCLK	Input	Clock control	Inverted input clock version of **BCLK** signal. Both LOW and HIGH phases of **BCLK** are used to control transfers on the bus.
BnRES	Input	Reset controller	Bus reset input, active LOW, used to reset the system and the bus when asserted LOW.
BA[25:0]	Input	ASB master	System address bus, least significant 26 bits, driven by the active bus master.
BD[31:0]	Input/output	ASB master	Bidirectional system data bus, 32-bit. The data bus is driven by the current bus master during write transfers and by the selected slave during read transfers.
DSELreg	Input	ASB decoder	Slave select signal for SC054 ASB SMC configuration registers. When HIGH, the select signal indicates the slave is selected and a transfer is required.
DSELmem	Input	ASB decoder	Slave select signal for SC054 ASB SMC memory banks. When HIGH, the select signal indicates the slave is selected and a transfer is required.
BWRITE	Input	ASB master	Transfer direction signal. When HIGH, this signal indicates a write to the SC054 ASB SMC and when LOW, a read from the SC054 ASB SMC block. This signal is driven by the current bus master and has the same timing as the address bus.
BSIZE[1:0]	Input	ASB master	Transfer size signal. This signal indicates the size of the current transfer, which can be byte, halfword, or word. This signal is driven by the current bus master and has the same timing as the address bus.

Table A-1 ASB signals (continued)

Signal name	Type	Source/ destination	Description
BWAIT	Output	ASB master	Wait response signal. When HIGH, a further bus cycle is required and when LOW, the transfer might complete in the current bus cycle. When no slave is selected, this signal is driven by the bus decoder.
BERROR	Output	ASB master	Error response signal. When HIGH, this signal indicates a bus transfer error, and when LOW the transfer is successful. This signal is also used in combination with the **BLAST** signal to indicate a bus retract operation. When no slave is selected, this signal is driven by the bus decoder.
BLAST	Output	ASB master	Last response signal. When HIGH, this signal indicates that the current transfer must be the last of a burst sequence. When no slave is selected, this signal is driven by the bus decoder. This signal is also used in combination with the **BERROR** signal to indicate a bus retract operation. When no slave is selected, this signal is driven by the bus decoder.

A.2 Non-ASB signals

Table A-2 lists the module-specific non-ASB on-chip signals

Table A-2 Block-specific on-chip signal

Signal name	Type	Source/ destination	Description
TestMode	Input	Test interface controller	Test mode input. This signal indicates the test controller has taken control of the bus. When HIGH, this signal enables the *External Bus Interface* (EBI) for the 32-bit test bus. It also selects **TCLK** as the system clock source.
Ticinen	Input	Test interface controller	Test data in enable input. This active LOW signal indicates that the SC054 ASB SMC should drive the **SMDATIN** (TBUS) into the **BD.** Must be tied HIGH when not connected to the TIC.
Ticouten	Input	Test interface controller	Test data out enable input. This active LOW signal indicates that the SC054 ASB SMC must drive its latched version of **BD** onto the external **SMDATAOUT** (TBUS). Must be tied HIGH when not connected to the TIC.
TicoutLen	Input	Test interface controller	Test data out latch enable input. BD latch enable for the data bus in the external memory bus. When LOW the BD latch should be transparent. Must be tied HIGH when not connected to the TIC.
BIGENDIAN	Input	System	This static configuration bit indicates the type of endianness of the memory system: 1 = big-endian 0 = little-endian.

Table A-3 lists the scan test on-chip signals.

Table A-3 Scan test on-chip signals

Signal name	Type	Source/ destination	Description
SCANMODE	Input	Scan test controller	Scan test mode input. This signal must be asserted HIGH during scan testing to ensure that bidirectional tristate signals are tristated and not driven. **SCANENABLE** must be deasserted LOW during normal use or when applying TicTalk test vectors through the TIC macro block.
SCANENABLE	Input	Scan test controller	Scan test enable input. This signal must be driven during scan testing to control the input multiplexors of scan flip-flops. **SCANENABLE** must be deasserted LOW during normal use or when applying TicTalk test vectors through the TIC macro block. This signal is not functionally connected within the peripheral. It is a dummy pin that is used during the scan insertion process.
SCANINBCLK	Input	Scan test logic	Dedicated scan chain input for flip-flops clocked by **BCLK**. This signal is not functionally connected within the peripheral. It is a dummy pin that is used during the scan insertion process.
SCANINnBCLK	Input	Scan test logic	Dedicated scan chain input for flip-flops clocked by **nBCLK**. This signal is not functionally connected within the peripheral. It is a dummy pin that is used during the scan insertion process.

Table A-3 Scan test on-chip signals (continued)

Signal name	Type	Source/ destination	Description
SCANOUTBCLK	Input	Scan test logic	Dedicated scan chain output for flip-flops clocked by **BCLK**. This signal is not functionally connected within the peripheral. It is a dummy pin that is used during the scan insertion process.
SCANOUTnBCLK	Input	Scan test logic	Dedicated scan chain output for flip-flops clocked by **nBCLK**. This signal is not functionally connected within the peripheral. It is a dummy pin that is used during the scan insertion process.
SMBUSREQ	Output	EBI	When asserted HIGH, **SMBUSREQ** requests access to EBI.
SMBUSGNT	Input	EBI	When asserted HIGH, **SMBUSGNT** indicates that the slave is granted the EBI.

Note

If an EBRI is not required, **SMBUSREQ** and **SMBUSGNT** must be connected together.

Table A-4 lists the signals to the input/output pads.

Table A-4 Input/output pad signals

Signal name	Type	Source / destination	Description
SMDATAIN[31:0]	Input	Input/output pad	External data input bus. Data read from external memory.
SMnWAIT	Input	Input/output pad	Wait mode input from external memory controller. Active HIGH or active LOW activation as programmed in the SMC configuration registers for each bank.
SMDATAOUT[31:0]	Output	Input/output pad	External data output bus. Data is written to external memory.
SMADDR[22:0]	Output	Input/output pad	External address bus to off-chip memory.
SMnDATAEN[3:0]	Output	Input/output pad	Tristate input/output pad enables to control the byte lanes of the external data output bus **SMDATAOUT**, active LOW. The **SMnDATAEN** signals 0 to 3, independently control **SMDATAOUT** signals 0 to 7, 8 to15, 16 to 23, and 24 to 31 respectively. The **SMnDATAEN** signals are connected to the appropriate **SMDATAOUT** input/output pad enables and asserted LOW to drive data out on the data pads.
SMnCS[7:0]	Output	Input/output pad	Chip select for external memory banks 0 to 7, active LOW or active HIGH programmable by configuring the CS polarity for each bank independently.

Table A-4 Input/output pad signals (continued)

Signal name	Type	Source / destination	Description
SMnOEN	Output	Input/output pad	Output enable for external memory banks, active LOW.
SMnWEN	Output	Input/output pad	Write enable for the external memory banks, active LOW.
SMnBLS[3:0]	Output	Input/output pad	Byte lane select signals, active LOW. The signals **SMnBLS[3:0]** select byte lanes [31:24], [23:16], [15:8], and [7:0] on external memory devices.

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