AMBA Color LCD Controller

Data Sheet

ARM®

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AMBA Color LCD Controller
Data Sheet

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Contents
AMBA Color LCD Controller Data Sheet

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Chapter 1
AMBA Color LCD Controller

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1.1 Module overview

The LCD controller provides all the necessary control signals to interface directly to an ARM AMBA bus as a bus master controller. The LCD controller can operate in single-panel or dual-panel modes when connected to the associated multiplexed LCD. The block is designed to work with a separate RAM block to provide data to the FIFO at the front end of the LCD controller data path, at a rate sufficient to support the chosen display mode and resolution.

The panel size is programmable, and can be any width (line length) from 16 to 1024 pixels in 16-pixel increments. The number of lines is set by programming the total number of pixels in the LCD. The total video frame size is programmable up to 1024x1024; single- or dual-panel display mode is also supported.

The screen is intended to be mapped to the video buffer as one contiguous block where each horizontal line of pixels is mapped to a set of consecutive bytes of words in the video memory. The pixels stored in memory can be programmed and arranged in a little or big endian manner.

Assuming a bus clock frequency of 30MHz, the maximum screen resolution for this bandwidth would be 640x480 pixels. To display a resolution of 800x600 pixels, the bus clock frequency would have to be 50MHz.

The principal features of the LCD controller are:

- encoded pixel data is stored in external memory in a frame buffer in 4-, 8- or 16-bit increments, and is loaded into a four-entry FIFO (32 bits per entry) and holding latch on a demand basis using the LCD's own dedicated dual-channel DMA controller
- programmable pixel display modes
- programmable display size
- 16 grayscale levels
- palette allowing full logical-to-physical address mapping
- programmable pixel rate
- four types of displays are supported—passive and active color, and passive and active monochrome
- in passive STN mode a total of 3375 possible colors is available, allowing any 256 colors to be displayed in each frame, as well as 15 grayscale levels for monochrome screens

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- any screen size up to 1024x1024 (assuming big enough bandwidth) is supported, as well as single- or dual-panel display mode
- frame, line and pixel clocks
- AC-bias drive signal
- AMBA compatible
- 4, 8 and 16 bit-per-pixel display modes
- patented dithering algorithm

Frame buffer data contains encoded pixel values: these are used by the LCD controller as pointers to index into a 256-entry by 12-bit wide palette. Monochrome palette entries are 4bits wide, and color are 12 bits wide. Encoded pixel data from the frame buffer which is 4 bits wide addresses the first16 locations of the palette, and 8-bit pixel data accesses any of the 256 entries within the palette. When passive color 12-bit pixel mode is enabled, the color pixel values bypass the palette and are fed directly to the LCD's dither logic. When active color 16-bit pixel mode is enabled, the pixel value not only bypasses the palette but also the dither logic, and is sent directly to the LCD's data pins.

Once the 4- or 8-bit encoded pixel value is used to select a palette entry, the value programmed within the entry is transferred to the dither logic; this uses a patented space or time-based dithering algorithm to produce the pixel data that is output to the screen. Dithering causes individual pixels to be turned off and on in each frame at varying rates to produce the 15 levels of gray for monochrome screens, and 15 levels each for the red, green and blue pixel components for color screens: this provides a total of 3375 colors, 256 of which are available in each frame. The data output from the dither logic is placed in a FIFO before it is placed on the LCD's pins and is driven to the display using the pixel clock.

Depending on the type of panel used, the LCD controller is programmed to use either 4-, 8- or 16-pixel data output pins. Single-panel monochrome displays use 4- or 8-bit data registers to output four or eight pixels respectively to each pixel clock, and single-panel color displays use eight pins to output 22/3 pixels to each pixel clock (8 pins / 3 colors/pixel = 22/3 pixels per clock). The LCD controller also supports dual-panel mode, which causes the LCD controller's data lines to be split into two groups: one to drive the top half, and one to drive the bottom half of the screen. For dual-panel displays, the number of pixel data output pins are doubled, allowing twice as many pixels to be output from each pixel clock to the two halves of the screen.

In active (TFT) display mode, the LCD can be used with an external palette and DAC to drive a video monitor. The LCD's line clock pin functions as a horizontal sync (HSYNC) signal and the frame clock pin functions as a vertical sync (VSYNC) signal.

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In TFT mode, the LCD's dither logic is bypassed, sending selected palette entries directly to the LCD's data output pins. Additionally, 16-bit pixels can be used, which bypass both the palette and the dither logic.

Details relating to the LCD controller's signals are shown in Table 1-1 and Table 1-2 on page 1-6.

Table 1-1 AMBA signal descriptions

Name	Type	Source/ Destination	Description
BnRES	In	Reset Controller	The bus reset signal is active LOW and is used to reset the system and the bus.
BA[31:0]	InOut	Current Master/LCD	System address bus. The addresses become valid before the transfer to which they refer and remain valid until the last phase 2 of the transfer.
BCLK	In	AMBA Bus	The ASB clock, timing and all bus transfers. It has two distinct phases: phase 1 in which BCLK is LOW and phase 2 in which BCLK is HIGH.
BD[31:0]	InOut	Current Master, AMBA Bus	Bi-directional system data bus. The data bus is driven by the current bus master during write transfers and by this block during register read transfers.
BERROR	In	AMBA Bus	LCD slave signalling that a bus error has occurred.
BLAST	In	AMBA Bus	This signal is driven by the selected bus slave to indicate if the current transfer should be the last of a burst sequence. When **BLAST** is HIGH, the decoder must allow sufficient time for address decoding. When **BLAST** is LOW, the next transfer may continue a burst sequence. When no slave is selected, this signal is driven by the bus decode
BSIZE[1:0]	Out	Current Master	These signals indicate the size of the transfer, which may be byte, halfword or word. These signals have the same timing as the system address bus.
BWAIT	In	Current Master	Wait slave response signal. Driven in phase 1 when the DRAM controller is selected. Asserted while the DRAM transaction is incomplete.
BWRITE	InOut	Current Master	When HIGH this signal indicates a write transfer, and when LOW a read transfer. This signal has the same timing as the address bus.
BTRAN[1:0]	Out	Current Master	These signals are used to determine sequential and non-sequential accesses for RAM burst mode access control.
BPROT[1:0]	Out	Current Master	These signals indicate if the transfer is an opcode fetch of data access. The transfer will always be a supervisor mode.

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Table 1-2 LCD controller panel signal descriptions

Name	Type	Source/ Destination	Description
UPLcdData	Out	DMA	Register used to store either four or eight data values at a time to the LCD display. For monochrome displays, each bit value represents a pixel; for passive color displays, groupings of three bit values represent one pixel (red, green and blue data values). UPLcdData[3:0] is used for single-panel monochrome displays; UPLcdData is used for dual-panel monochrome, as well as singlepanel color displays and active color modes.
LPLcdData	Out	DMA	When dual-panel color or TFT operation is programmed, LPLcdData is used as the additional, required LCD data register to output pixel data to the screen.
LcdCP	Out	LCD	Pixel clock used by the LCD display to clock the pixel data into the line shift register. In passive mode, pixel clock only transitions which valid data is available on the data lines. In active mode the pixel clock transitions continuously and the AC-bias pin is used as an output enable to signal when data is available on the LCD's pins.
LcdLP	Out	LCD	Line clock used by the LCD display to signal the end of a line of pixels that transfers line data from the shift register to the screen, and to increment the line pointer(s). Also used by TFT displays as the horizontal synchronization signal.
LcdFP	Out	LCD	Frame clock used by the LCD displays to signal the start of a new frame of pixels. Also used by TFT displays as the vertical synchronization signal.
LcdAC	Out	LCD	AC-bias used to signal the LCD display to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. Used in TFT mode as the output enable to signal when data should be latched from the data pins using the pixel clock.

The pixel clock frequency should be derived from the output of the on-chip PLL (BCLK) and is programmable from BCLK/2 to BCLK/257. Each time new data is supplied to the LCD data pins, the pixel clock is toggled to latch the data into the LCD display's serial shifter. The line clock toggles after all pixels in a line have been transmitted to the LCD driver, and a programmable number of pixel clock wait states have elapsed both at the beginning and end of each line. In passive mode, the frame clock toggles during the first line of the screen, and the beginning and end of each frame is separated by a programmable number of line clock wait states (Horizontal Front Porch, HFP and Horizontal Back Porch, HBP should be programmed to zero in passive mode).

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In active mode, the frame clock is asserted at the end of a frame after a programmable number of line clock wait states occur. In passive display mode, the pixel clock does not transition during wait state insertion or when the line clock is asserted. Finally, the AC-bias (LcdAC) can be configured to transition each time a programmable number of line clocks occurs.

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1.2 Display Specifications

The following information shows the number of palette entries and thus the number of possible screen colors per frame that can be displayed in each mode with the corresponding number of bits-per-pixel (BPP).

Mono passive: 4 BPP only:

- 16 palette entries selecting one of 15 grayscale.

  Note

  8 BPP would work, but is not practicable as there are only 15 physical grayscales.

Color passive: 4 BPP, 8 BPP, 12 BPP "true-color"

- 4 BPP: 16 palette entries from 3375 possible colors
- 8 BPP: 256 palette entries from 3375 possible colors
- 12 BPP: 3375 possible on-screen colors

TFT: 4bpp, 8bpp, 16bpp

- 4 BPP: 16 palette entries selecting from 4096 colors
- 8 BPP: 256 palette entries selecting from 4096 colors
- 16 BPP: Maximum 64K colors, depending on LCD panel

Palette entries are 16 bits wide (2 bytes) and 4 BPP, so require 32 bytes of storage. 8 BPP modes require 256 bytes. 12 or 16 BPP modes do not use palette data but need the bits per- pixel information to be loaded, so these modes uses 32 byte similar to that of the 4 BPP modes.

Mono passive modes supports two different interfaces: 4 bits per panel and 8 bits per panel. Both Mono and color passive modes can operate in single- or dual-panel modes. All modes (color/mono, 4, 8, 12 or 16 bits-per-pixel, 4- or 8-bit mono, single- or dual-panel) operate independently of each other.

Vertical Back Porch (VBP) and Vertical Front Porch (VFP) must be zero on passive screen. The vertical synchronization signal (VSync) width must be programmed to be as small as possible on passive screen modes, but long enough to load the palette without stealing all the memory bandwidth from the CPU.

Pixels-per-line (PPL) must be in multiples of 16. Most LCD panels ignore data at the end of the line that is not needed—that is, they ignore data at the right hand side of the screen.

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1.3 AMBA Signal Descriptions

This section provides detailed information on the relevant AMBA signals, including their intended use and phase-accurate timing requirements.

1.3.1 Address and Control Signal Timing

The address and control information is generated by the bus master from the rising-edge of BCLK. The timing of the address and control information, however, is considered separately for Non-sequential and Sequential transfer types. This is because a bus master will typically have significantly different timing parameters in each case.

It is a common characteristic that bus masters will have fast address and control output valid timings for Sequential transfers, as shown in Figure 1-1. This is because a bus master is usually able to generate a sequential address well before the start of the transfer, and therefore the output valid time from the bus master is mainly dependent on the time required to drive the new value onto the bus.

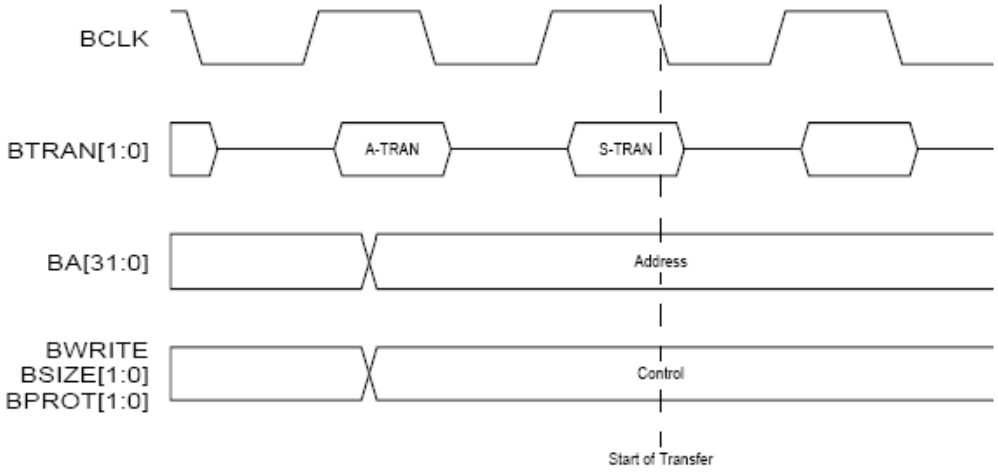

Figure 1-1 Address and control output timings

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1.4 ASB Bus Master

This section provides detailed information on the relevant AMBA signals, including their intended use and phase-accurate timing requirements.

1.4.1 Bus Master Interface Description

The main bus interface state machine is falling-edge triggered and contains six states. The entire state diagram, as shown in Figure 1-3 on page 1-11, is quite complex but can be considered in four quadrants.

No Transfer Request Not Granted	Transfer Request Not Granted
No Transfer Request Transfer Granted	Transfer Request Granted (Retract not supported)

Figure 1-2 Quadrants

The Transfer Request, Granted quadrant contains two states, which handle handover bus turnaround (the retract operation is not supported).

The two signals internal bus master signals Granted and Request control the majority of the transitions around the state diagram. Granted is generated from the simpler state machine and Request is generated directly by the bus master. Request is asserted HIGH when the bus master requires a transfer on the bus, and is LOW when the bus master does not need access to the bus.

The only time when a transition around the state diagram is not controlled by Granted and Request is when the bus master is in the ACTIVE state. In this state, the transition to the next state is determined by the transfer response that is received. WAIT, DONE, LAST and ERROR shown in Figure 1-3 on page 1-11 correspond to the encodings of the transfer response signals.

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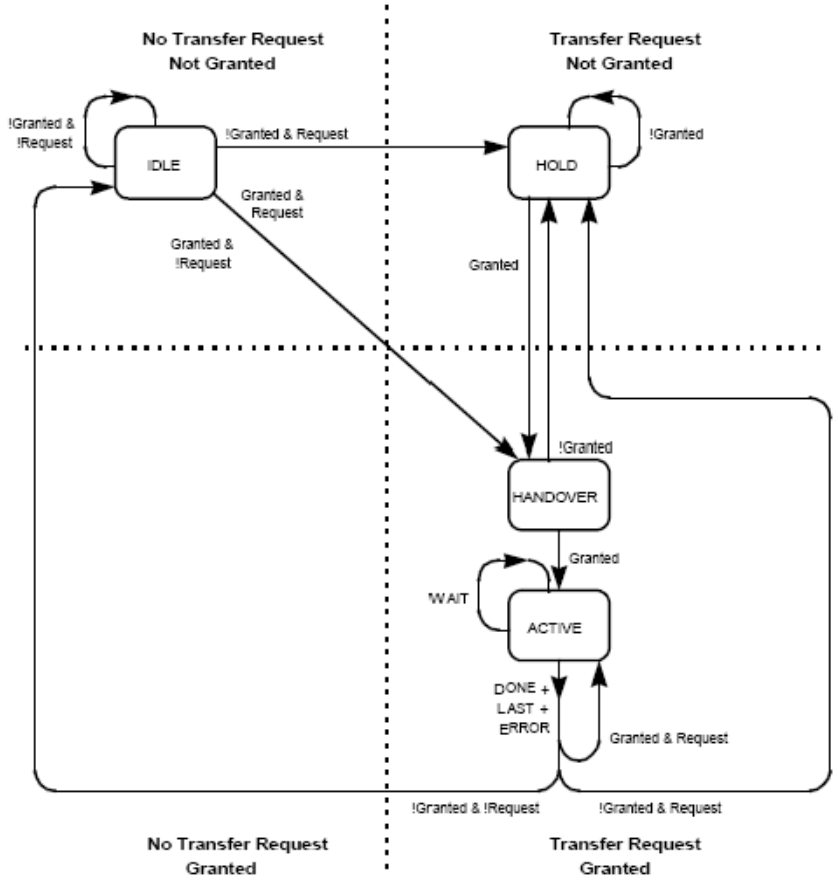

Figure 1-3 Bus master main state machine

Note

The state diagram assumes that, once the LCD controller has made a request for a transfer as indicated by Request, then the LCD controller de-assert Request and assert BLOK for the remainder of the time Granted is required.

As the main bus master state machine is operating from the falling-edge of the clock, it is necessary to use latched versions of the transfer response signals BWAIT, BERROR and BLAST to control the exit from the ACTIVE state. The reset conditions are not shown on the state diagram, as the main bus master state machine has a complex reset

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term. BUSIDLE state is not supported as the LCD controller should not be default bus master. If AGNT is not asserted during reset then the bus master enters the IDLE state. Table 1-3 indicates the actions that must occur in each state.

Table 1-3 State actions

Name	Description	Action
IDLE	The master does not require the bus and is not granted.	Internal BTRAN is Address-only Master clock is enabled Master address bus is tri-state Master data bus is tri-state
BUSIDLE	The master does not require the bus, but has been granted anyway.	Internal BTRAN as indicated by master Master clock is enabled Master address bus enable is generated from the Granted signal Master data bus is tri-state
HOLD	The master requires the bus, but has not been granted.	Internal BTRAN is Address-only Master clock is disabled Master address bus is tri-state Master data bus is tri-state
HANDOVER	This state provides bus turnaround when changing between different bus masters.	Internal BTRAN is Sequential Master clock is disabled Master address bus enable is generated from Granted signal Master data bus is tri-state
ACTIVE	Active state when data transfers occur. Exiting this state is dependent on the transfer response.	Internal BTRAN as indicated by master Master clock enable is derived from BWAIT Master address bus enable is generated from Granted signal Master data bus enable is enabled if a write transaction

BTRAN[1:0] tri-state drivers are enabled when AGNT and BCLK are both HIGH. Master Address Bus Enable is used to control the tri-state enable of BA[31:0], BWRITE, BSIZE[1:0], BPROT[1:0] and BLOK. Master Data Bus Enable is used to control the tri-state enable of BD[31:0].

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1.4.2 Bus Master Timing Diagrams

The following diagrams show the timing parameters related to an ASB bus master operating in an AMBA system. Figure 1-4 shows the parameters related to Sequential transfers; Figure 1-5 on page 1-14 shows the reset signal and arbitration timing.

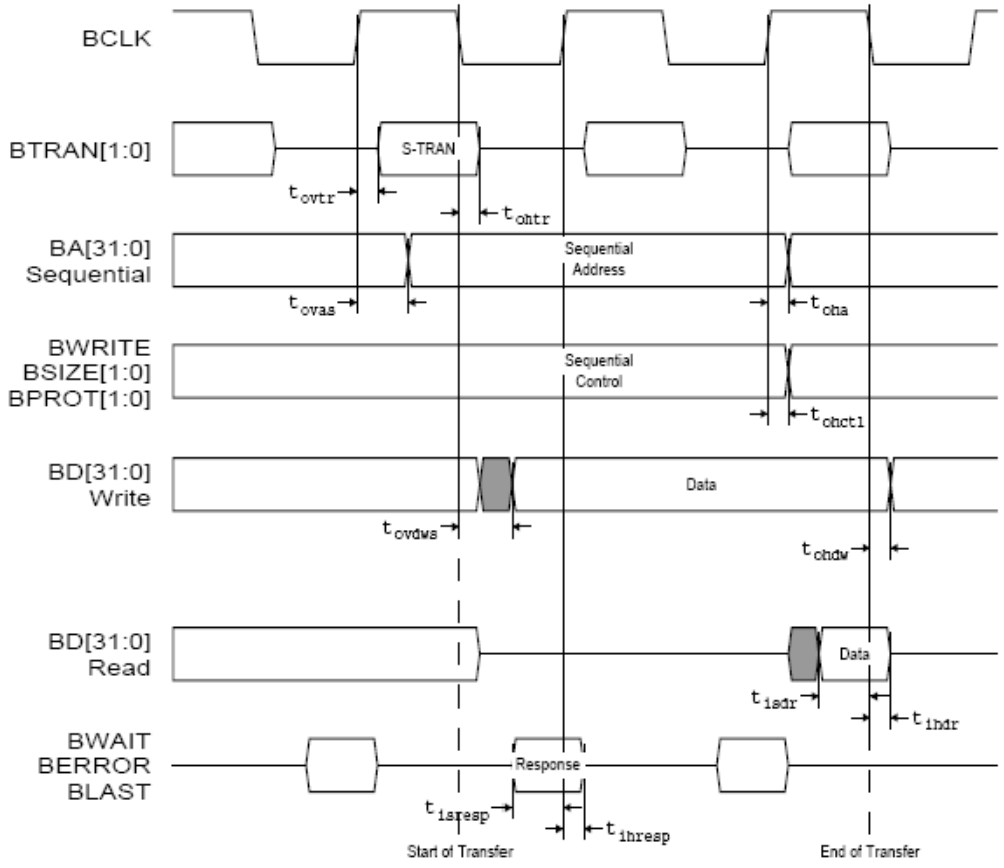

Figure 1-4 ASB bus master sequential transfer

A sequential transfer has different timing parameters for the address and control signal valid times. In a typical bus master, the output valid times for sequential transfers will be far better than for Non-sequential transfers. The output hold times for address, control and data are identical and independent of the transfer type. The other difference between the Sequential and Non-sequential transfers is that during a Sequential transfer the data may be driven during the first phase of the transfer and hence the data valid parameter is specified from the falling-edge of BCLK.

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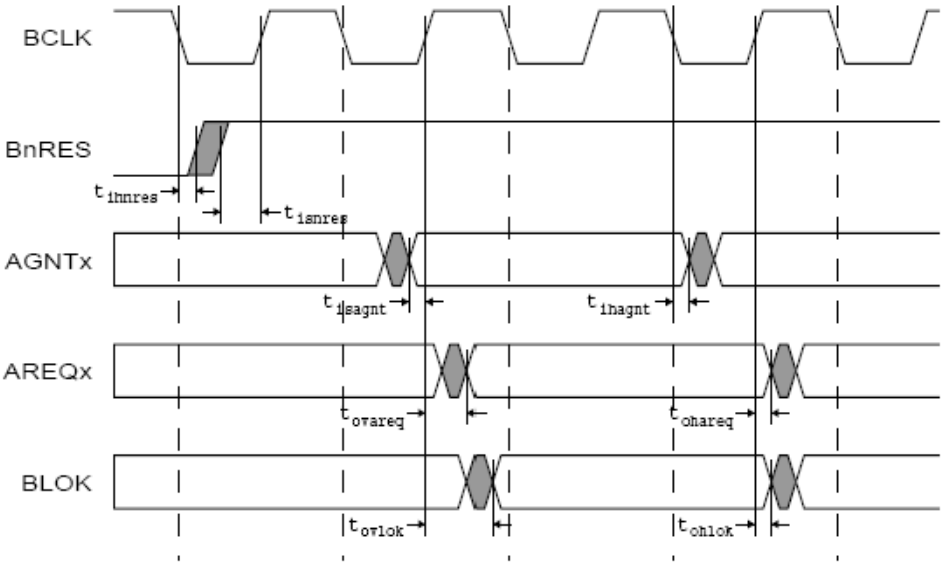

Figure 1-5 ASB bus master arbitration and reset signal

The BnRES signal may be asserted asynchronously and so there is no setup and hold parameter relating to the assertion of the signal. The AREQ signal, which is an output from the bus master, changes during the HIGH clock phase and the AGNT signal, which is returned from the arbiter changes during the LOW clock phase. BLOK should be driven low when the LCD is bus master.

Note

The LCD controller should have the highest (but not default) bus master priority.

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1.4.3 Timing Parameters

The timing parameters related to an ASB bus master operating in an AMBA system are also shown in textual form in the following two tables: Table 1-4 details the input signals; Table 1-5 details the output signals. Bi-directional signals can be found in both tables.

Table 1-4 Bus master input timing parameters

Parameter	Description
Tclkl	BCLK LOW time
Tclkh	BCLK HIGH time
Tisnres	BnRes de-asserted setup to rising BCLK
Tihnres	BnRes de-asserted hold after falling BCLK
Tisresp	BWAIT, BERROR and BLAST setup to rising BCLK
Tihresp	BWAIT, BERROR and BLAST hold after rising BCLK
Tisdr	For read transfers, BD[31:0] setup to falling BCLK
Tihdr	For read transfers, BD[31:0] hold after falling BCLK
Tisagnt	AGNT setup to rising BCLK
Tihagnt	AGNT hold after falling BCLK

Table 1-5 Bus master output timing parameters

Parameter	Description
Tovtr	BTRAN valid after rising BCLK
Tohtr	BTRAN hold after falling BCLK
Tovan	For Non-sequential transfers, BA[31:0] valid after rising BCLK
Tovas	For Sequential transfers, BA[31:0] valid after rising BCLK
Tovaa	For Address-only transfers, BA[31:0] valid after falling BCLK
Toha	BA[31:0] hold after rising BCLK
Tovctln	For Non-sequential transfers, BWRITE, BSIZE[1:0] and BPROT[1:0] valid after rising BCLK

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Table 1-5 Bus master output timing parameters (continued)

Parameter	Description
Tovctla	For Address-only transfers, BWRITE, BSIZE[1:0] and BPROT[1:0] valid after falling BCLK
Tohctl	BWRITE, BSIZE[1:0] and BPROT[1:0] hold after rising BCLK
Tovdwn	For Non-sequential write transfers, BD[31:0] valid after rising BCLK
Tovdwn	For Sequential write transfers, BD[31:0] valid after falling BCLK
Tohdw	For write transfers, BD[31:0] hold after BCLK
Tovlok	BLOK valid after rising BCLK
Tohlok	BLOK hold after rising BCLK
Tovareq	AREQ valid after rising BCLK
Tohareq	AREQ hold after rising BCLK

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1.5 LCD Controller Operation

The LCD controller supports a variety of user-programmable options, including display type and size, frame buffer pixel size and output data width. Although all programmable combinations are possible, the selection of displays available within the market dictate which combinations of these programmable options are practical. In addition, the type of external memory system implemented by the user limits the bandwidth of the LCD's DMA controller, which in turn limits the size and type of screen which can be controlled.

The following sections describe individual functional blocks within the LCD controller, the frame buffer and palette memory organization, and the LCD's DMA controller. The sections are arranged in order of data flow, starting with the off-chip frame buffer and ending with the pins that interface to the LCD display.

1.5.1 DMA to Memory (AMBA) Interface

Palette RAM data and encoded pixel data is stored in off-chip memory (usually DRAM) in an area called the frame buffer. This data is transferred to the LCD controller's 4-entry, 32- bit wide input FIFO and holding latch on a demand basis using the LCD controller's dedicated DMA controller. The LCD controller has been placed on the ARM system bus (ASB) as a bus master rather than the ARM peripheral bus (APB) where all other peripherals are located, because it is a higher-speed synchronous bus that is able to maintain the data rate required for demanding displays such as dual-panel color. The LCD's DMA contains two channels that transfer data from external memory to the input FIFO for LCD control mode. One channel is used for single-panel displays and two are used for dual-panel displays.

The LCD controller issues a service request to the DMA after it has been initialized and enabled. The DMA automatically performs four-word transfers, filling all but one entry of the FIFO. Values are taken from the bottom of the FIFO one entry at a time, and each 32-bit value is unpacked into individual pixel encodings that are 4, 8, 12 or 16 bits each. When enough entries are read from the FIFO, a service request is issued to the DMA.

1.5.2 Frame Buffer

The frame buffer is an area within off-chip memory that is used to supply enough encoded pixel values to fill the entire screen one or more times. At the start or lowest order address of the LCD controller's frame buffer is a 32-byte buffer for 4- and 12-bit mode operation (512-byte buffer for all other modes of operation), used to store the look-up palette data for each frame. A 32-byte buffer is used to load the top 16 entries of the palette for 4, 12 and 16 bits-per-pixel encodings, and a 512-byte buffer is used to load the entire 256-entry palette for 8 bits-per-pixel encodings. Note that the palette is

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not used for 12 or 16 bits-per pixel encodings. The 32 bytes at the top of the frame buffer, however, must be zero-filled even though the data is not used. This is due to the fact that the bits-per-pixel must be loaded regardless of operation.

Each time a new frame is fetched from the frame buffer, the LCD controller's palette is first loaded with data contained within the palette buffer. Each of the 256 palette entries is stored in adjacent half-words. Figure 1-6 on page 1-19 show the palette entry organization for both little and big endian memory organization. The user may select how the LCD views the ordering of frame buffer palette/pixel entries by programming the Lcd Big Endian (LcdBE) bit in LCD control register (LcdControl). In little endian mode, palette entries are ordered starting with the least significant half-word followed by the most significant. In big endian mode, palette entries are arranged in an order starting with the most significant half-word followed by the least significant. Note that the ordering of the 4-bit R, G, B and mono pixel data (and the BPP field) does not change between little and big endian modes: only the relative positioning of the individual 16-bit palette entries changes.

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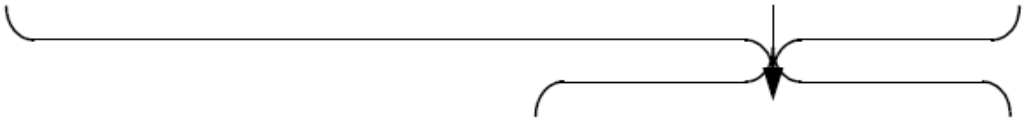
Individual Palette Entry

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color	Unused		BPP*		Red (R)				Green (G)				Blue (B)			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mono	Unused		BPP*		Unused								Mono (M)			

Note: bits-per-pixel (BPP) is only contained within the first palette entry (palette entry 0).



256 Entry Palette Buffer (Little Endian)

Bit	31 — 16	15 — 0
Base + 0x0	Palette Entry 1	Palette Entry 0
Base + 0x4	Palette Entry 3	Palette Entry 2
	⋮	⋮
Base + 0x20	Palette Entry 31	Palette Entry 30
Base + 0x24	Palette Entry 33	Palette Entry 32
	Note: Entries 16 through to 255 do not exist for 4, 12 and 16 bit/pixel modes	⋮
Base + 0x1FC	Palette Entry 255	Palette Entry 254
Base + 0x200	Start of Pixel Data	

Figure 1-5: Palette Entry/Buffer Format (Little Endian)

256 Entry Palette Buffer (Big Endian)

Bit	31 — 16	15 — 0
Base + 0	Palette Entry 0	Palette Entry 1
Base + 4	Palette Entry 2	Palette Entry 3

Figure 1-6 Palette Entry/Buffer Format (Big Endian and Little Endian)

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The first palette entry (Palette Entry 0) also contains an extra field that is used to configure synchronously the LCD controller at the beginning of each frame. Bits 12 and 13 of the first palette entry contain a field that is used to select the number of bits-per-pixel that is to be used in the following frame and the number of entries that are used in the palette RAM. The bits-per-pixel (BPP) bit-field is decoded by the LCD to correctly unpack pixel data into nibbles, bytes, 12-bit values or half-words, and decoded by the palette to tell it how many address bits are contained in the pixel data it is supplied, configuring the palette size to 16 or 256 entries. Note that 12- and 16-bit pixel mode bypasses the LCD palette and supplies 12-bit values directly to the dither logic when passive mode is enabled, or 16-bit values directly to the output FIFOs when active mode is enabled. Table 1-6 shows the encoding of the BPP bit-field (in little endian mode).

Table 1-6 Bits-per-pixel encoding for palette entry 0 buffer

Bit	Name	Description
13–12	BPP	bits-per-pixel 00 - 4 bits-per-pixel 01 - 8 bits-per-pixel 1x - 12 bits-per-pixel in passive mode (LcdTFT=0), 16 bits-per-pixel in active mode (LcdTFT=1). Note: Two 4-bit pixels are packed into each byte, and 12-bit pixels are right-justified on half-word boundaries (in the same format as palette entry).

Following the palette buffer is the pixel data buffer that contains one encoded pixel value for each of the pixels present on the display. The number of pixel data values depends on the size of the screen (ie. 1024 x 768 = 786 432 encoded pixel values). Again, each pixel data value can be 4, 8 or 16 bits wide. Figures from Figure 1-7 on page 1-21 through to Figure 1-10 on page 1-22 show the memory organization (little endian mode) within the frame buffer for each size pixel encoding. Note that for 4-bit encodings, two pixels are placed into each byte, and for 12-bit encodings the value is right-justified within a half-word. These figures show the encoded pixel organization for little endian memory organization. Again, the user may select how the LCD views the ordering of frame buffer pixel entries by programming the Lcd Big Endian (LcdBE) bit in LCD control register. In big endian mode, pixel entries are arranged in an order starting with the most significant nibble, byte, or half-word and ending with the least significant.

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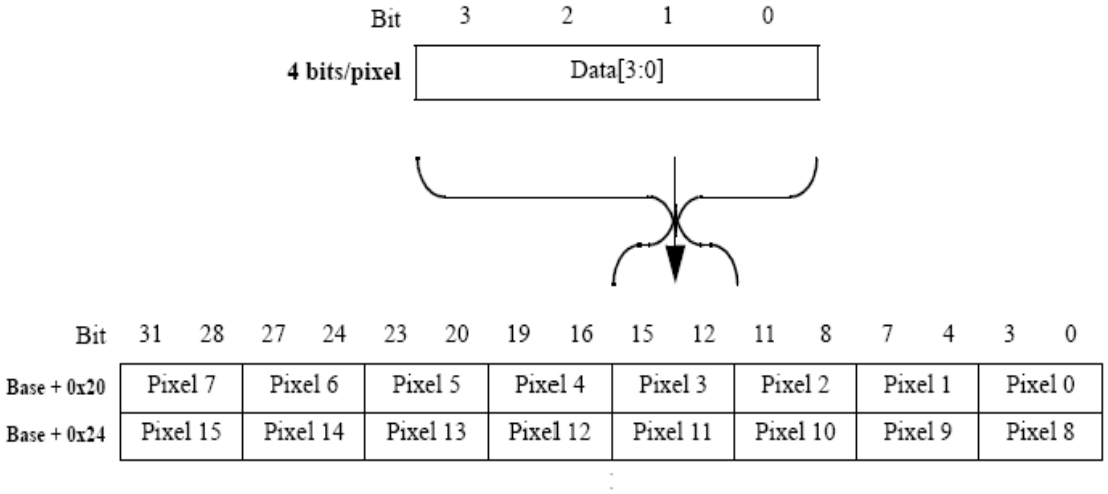

Figure 1-7 4bpp data memory organization (Little Endian)

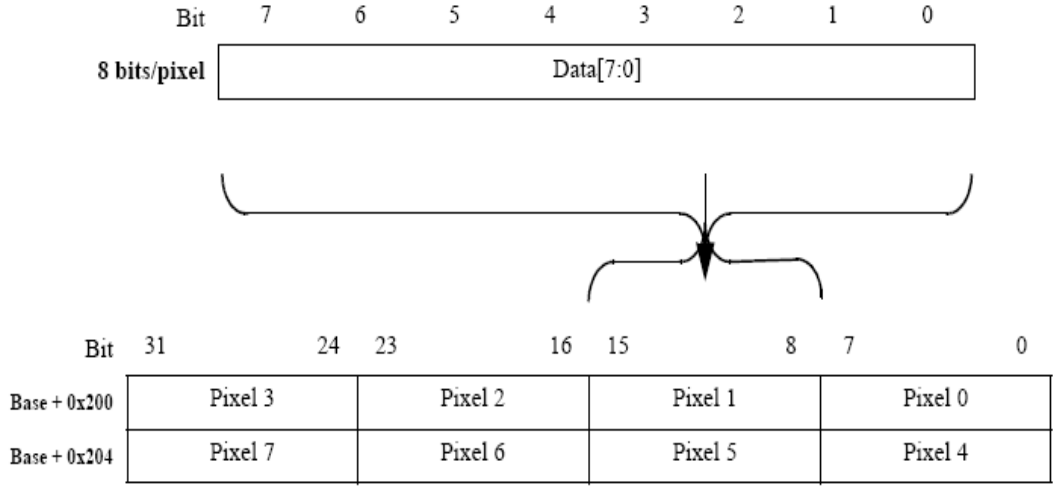

Figure 1-8 8bpp data memory organization (Little Endian)

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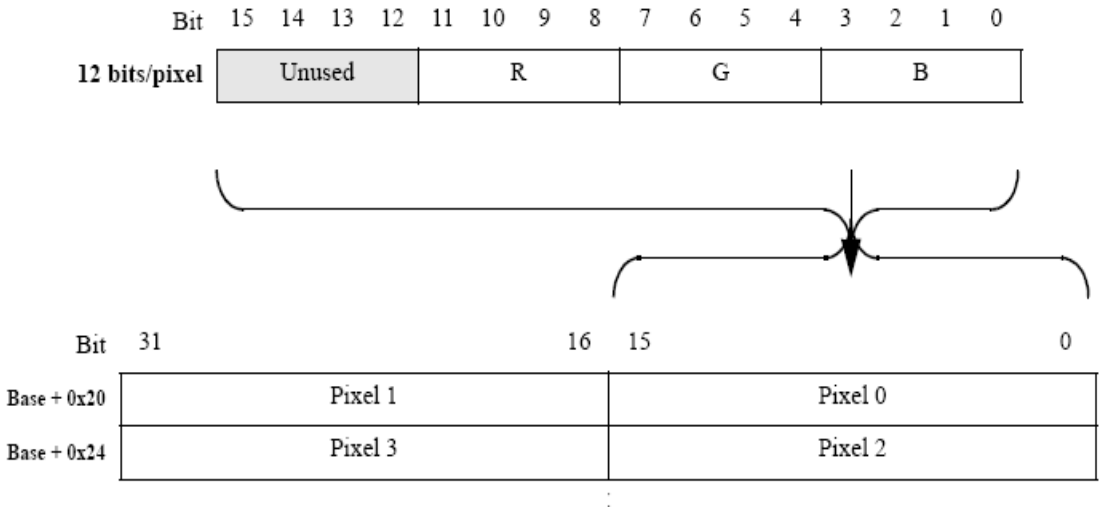

Figure 1-9 12bpp data memory organization (STN Mode Only) - Little Endian

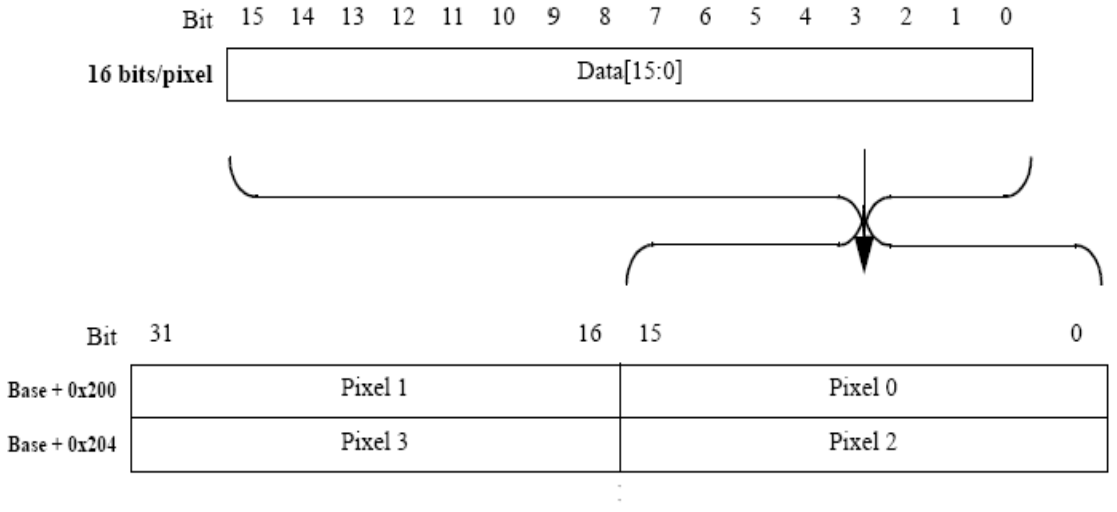

Figure 1-10 16bpp data memory organization (TFT Mode Only) - Little Endian

In dual-panel mode, pixels are presented to two halves of the screen at the same time (upper and lower). A second DMA channel and input FIFO exists to support dual-panel operation. The DMA channels alternate service requests when filling the two input FIFOs. The palette buffer is implemented in DMA channel 1 but not channel 2, so the base address points to the top of the encoded pixel values for channel 2. The DMA

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controller contains a base and current address pointer register. The end address is calculated automatically by the LCD using display information such as pixels-per-line, lines per frame, single-/dualpanel mode, color/monochrome mode, and bits-per-pixel that are programmed by the user.

The LCD's DMA may overshoot the end of the frame buffer by one burst cycle (4 word read). The LCD's DMA reads these extra values but they are flushed from the input FIFO each time the frame clock is pulsed. The user must ensure that the four words immediately following the end of the frame buffer reside in legal memory space (ie. that do not cause a bus error if read). Since the LCD does not alter this memory (only reads are performed), these locations can be used for data storage unrelated to the LCD.

The equations below are used to calculate the total frame buffer size (in bytes) that should be programmed in the DMA, based on varying pixel size encodings and screen sizes. Note that for dual-panel mode the frame buffer size is equally distributed between the two DMA channels, and the DMA channel 2's buffer is either 32 or 512 bytes smaller (no palette buffer).

For 4 bits/pixel: $$\text{FrameBufferSize} = 32 + 16 + \left(\frac{\text{Lines} \times \text{Columns}}{2}\right)$$

For 8 bits/pixel: $$\text{FrameBufferSize} = 512 + 16 + (\text{Lines} \times \text{Columns})$$

For 12/16 bits/pixel: $$\text{FrameBufferSize} = 32 + 16 + 2(\text{Lines} \times \text{Columns})$$

Figure 1-11 Equations

1.5.3 Input FIFO

Data from the LCD's DMA is directed either to the palette or the input FIFO. The direction of data flow is switched whenever the LCD controller is first enabled by each frame pulse. After the LCD controller is configured and enabled, the first 32 or 512 bytes supplied by the DMA is sent to the palette. All subsequent encoded pixel data is sent to the FIFO. For passive mode displays the frame clock is pulsed at the beginning of the frame. This signal is also used to change the direction of DMA input data from the FIFO back to the palette. A modulus of 8 or 128 is used to count during loading of the palette RAM, depending on the pixel bit size shown above. A 7-bit counter is loaded

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each time a frame clock pulse occurs or the LCD is enabled. The counter is decremented each time a word is stored to the palette (that is, two palette entries). When the counter wraps around to zero, the data input from the DMA is switched back to the FIFO.

The LCD controller contains a 4-entry by 32-bit wide input FIFO and holding latch that is used to store encoded pixels fetched from the frame buffer. The FIFO signals a service request to the DMA whenever four entries of the FIFO are read. In turn, the DMA automatically fills the FIFO with a four-word blast.

Pixel data from the frame buffer remains packed within individual 32-bit words when it is loaded into the FIFO. The LCD controller's port size is 32 bits wide to accommodate the heavy data flow from the frame buffer. Depending on the number of bits-per-pixel, as words are taken from the bottom of the FIFO they are unpacked and supplied to the look-up palette in either nibbles (4 bits/pixel) or bytes (8 bits/pixel), to the dither logic (12 bits/pixel), or directly to the pins in half-words (16 bits/pixel). When four entries are read, a service request is issued to the DMA.

1.5.4 Look Up Palette

The encoded pixel data from the input FIFO is used as an address to index and select individual palette locations. 4-bit pixels address 16 locations, and 8-bit pixels select any of the 256 palette entries. Note that the user may program 1, 2 and 3 bits-per-pixel as well by zeroing-out the upper 3, 2 or 1 bits or each encoded pixel value in the frame buffer and within the LCD controller's input FIFO.

Once a palette entry is selected by the encoded pixel value, the contents of the entry are sent to the color/grayscale space/time base dither circuit. In color mode, the value within the palette is made up of three 4-bit fields, one for each color component: red, green and blue. In monochrome mode, only one 4-bit value is present. For both modes, the 4-bit values represent 1 of 15 intensity levels. For color operation, an individual frame is limited to a selection of 256 colors (the number of palette entries). The LCD controller, however, is capable of generating a total of 3375 colors (15 levels per color x 3 colors). When 12 or 16 bit-per-pixel mode is enabled, the palette is bypassed. For passive displays, 12-bit pixels are sent directly to the dither logic, and 16-bit pixels are sent to the output FIFO to be driven directly to the LCD's data pins.

1.5.5 Color/grayscale Dithering

Entries selected from the look-up palette are sent to the color/grayscale space/timebase dither generator. Each 4-bit value is used to select one of 15 intensity levels. Note that two of the 16 dither values are identical (most intense). The gray/color intensity is controlled by turning individual pixels on and off at varying periodic rates. More intense grays/colors are produced by making the average time that the pixel is off longer than the average time that it is on. The dither generator also uses the intensity of adjacent

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pixels in its calculations to give the screen image a smooth appearance. The proprietary dither algorithm is optimized to provide a range of intensity values that match the eye's visual perception of color/gray gradations. In color mode, three separate dither blocks are used to process the three color components: red, green and blue.

The duty cycle and resultant intensity level for all 15 color/grayscale levels is summarized in Table 1-7.

Table 1-7 Color/grayscale intensities and modulation rates

Dither Value (4-bit value from palette)	Intensity (0% is white)	Modulation Rate (ratio of ON to ON+OFF pixels)
0000	0.0%	0
0001	11.1%	1/9
0010	20.0%	1/5
0011	26.7%	4/15
0100	33.3%	3/9
0101	40.0%	2/5
0110	44.4%	4/9
0111	50.0%	1/2
1000	55.6%	5/9
1001	60.0%	3/5
1010	66.6%	6/9
1011	73.3%	11/15
1100	80.0%	4/5
1101	88.9%	8/9
1110	100.0%	1
1111	100.0%	1

1.5.6 Output FIFO

The LCD controller contains a 19-entry by 16-bit wide output FIFO that is used to store pixel pin data before it is driven out to the pins. Each time a modulated pixel value is output from the dither generator it is placed into a serial shifter. The size of the shifter

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is controlled by programming the color/monochrome select and Lcd Dual Panel bits in the LCD's control registers. The shifter can be configured to be 4, 8 or 16 bits wide. Single-panel monochrome screens use either four or eight data lines, single-panel color and dual-panel monochrome screens use eight data pins, and dual-panel color and active screens use 16 data pins. Once the correct number of pixels have been placed within the shifter (4-, 8- or 16-pixel values), the value is transferred to the top of the output FIFO. The value is then transferred down until it reaches the last empty location within the FIFO. As values reach the bottom of the FIFO, they are driven out one by one onto the LCD's data pins on the edge selected by the Invert Pixel Clock (IPC) bit.

1.5.7 LCD controller Pins

For dual-panel mode, the pixels for the upper half of the screen are loaded to the least significant half of the LCD's output FIFO shifter, and the pixels for the lower half are loaded to the most significant half of the shifter. When the shifter is filled, the value is driven to the LCD controller data bus pins (**UpLcdData[3:0]** for a 4-bit wide bus, to the **UPLcdData** for an 8-bit wide bus, and to the **UPLcdData** and **LPLcdData** for a 16-bit wide bus); in addition, the pixel clock pin (**LcdCP**) is toggled.

When an entire line of pixels has been output to the LCD screen, the line clock pin (**LcdLP**) is toggled. In the same manner, if the controller is in passive mode and when the start of the first line of a new frame of pixels has been output to the LCD controller screen, the frame clock pin (**LcdFP**) is toggled. To prevent a DC charge from building within the screen's pixels, the display's power and ground supplies are periodically switched. The LCD controller signals the display to switch the polarity by toggling the AC-bias pin (**LcdAC**). The user can control the frequency of the bias pin by programming the number of line clock transitions between each toggle.

When active display mode is enabled, the timing of the pixel, line and frame clocks as well as the AC-bias pin change. The pixel clock transitions continuously in this mode as long as the LCD is enabled. The AC-bias pin functions as an output enable. When it is asserted, the display latches data from the LCD's pins using the pixel clock. The line clock pin is used as the horizontal synchronization signal (HSYNC), and the frame clock used as the vertical synchronization signal (VSYNC). See Figure 1-12 on page 1-27.

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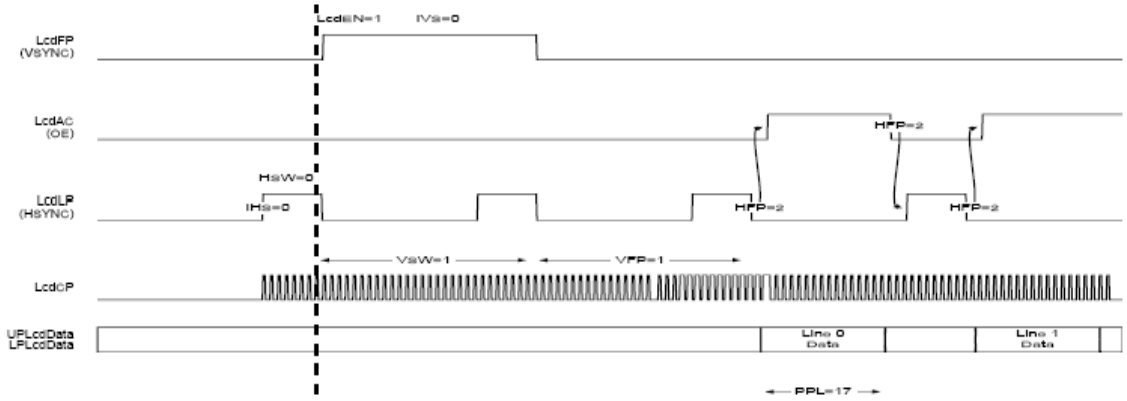

Figure 1-12 Active mode timing

The timing of the line and frame clock pins is programmable to support both passive and active mode. Programming options include:

- delay insertion both at the beginning and end of each line and frame
- pixel clock, line clock, frame clock and AC-bias signal polarity
- line and frame clock pulse width.

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1.6 LCD Controller Register Definitions

The LCD controller contains four control registers, four DMA address registers and one status register. The control registers contain bit-fields to enable and disable the LCD controller to define:

- the height and width of the screen being controlled
- single- or dual-panel display mode
- color or monochrome mode
- passive or active display
- polarity of the control lines
- pulse width of the line and frame clocks
- the pixel clock and AC-bias frequency
- the number of delays to insert before/after each line and after each frame.

An additional control field exists to tune the DMA's performance, based on the type of memory system in which the LCD controller is used. This field controls the placement of a minimum delay between each LCD palette request to ensure enough bus bandwidth is given to other ARM systems' bus masters for access. This field is only used for palette load.

The DMA address registers are used to define the base address of the off-chip frame buffer as well as to which address the DMA is currently pointing. Both of these registers exist for DMA channel 1 and 2.

The status registers contain bits that signal:

- FIFO underrun error
- DMA bus errors
- when the DMA base address can be re-programmed
- when the last active frame has completed after the LCD is disabled

Each of these hardware-detected events signal an interrupt request to the interrupt controller.

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1.7 LCD Control Register

LCD control register (LcdControl) contains seven bit-fields that are used to control various functions within the LCD controller.

1.7.1 LCD Enable (LcdEn)

The LCD enable (LcdEn) bit is used to enable and disable all LCD controller operation. When LcdEn=0 the LCD controller is disabled. When LcdEn=1, the LCD controller is enabled.

Note

All other control registers should be initialized before setting LcdEn.

The user may program LcdControl last, and configure all eight bit-fields at the same time via a word write to the register. If the user clears LcdEn while the LCD controller is enabled, it is permitted to complete transmission of the current frame before being disabled. Completion of the current frame is signalled by the DMA when it sets the Frame Done (Done) within the LCD status register, which generates an interrupt request.

1.7.2 LCD Monochrome (LcdBW)

The color/monochrome select (LcdBW) bit is used to determine whether the LCD controller operates in color or monochrome mode. When LcdBW=0:

- color mode is selected
- palette entries are 12 bits wide (4 bits per color)
- 8-bit data register (UPLcdData) is enabled for single-panel mode, and 16-bit for dual-panel mode (LPLcdData register is used as the extra 8 bits)
- all three dither blocks are used, one each for the red, green and blue pixel components

When LcdBW=1:

- monochrome mode is selected
- monochrome mode is selected
- 4 or 8 data lines are enabled for single-panel mode, and 8 pins for dual-panel mode

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The LCD Dual Panel(LcdDP) bit is used to select the type of display control that is implemented by the LCD screen. When LcdDP=0, single-panel operation is selected (pixels presented to screen one line at a time); when LcdDP=1, dual-panel operation is selected (pixels presented to screen two lines at a time). Single-panel LCD drivers have one line/row shifter and driver for pixels and one line pointer, while dual-panel LCD controller drivers have two line/row shifters (one for the top half of the screen, one for the bottom) and two line pointers. When dual-panel mode is programmed, both of the LCD controller's DMA channels are used. DMA channel 1 is used to load the palette RAM from the frame buffer and to drive the upper half of the display; DMA channel 2 drives the lower half. The two channels alternate when fetching data for both halves of the screen, placing encoded pixel values within the two separate input FIFOs. When dual-panel operation is enabled, the LCD controller doubles its pin use: for monochrome screens, 8 pins are used and for color screens, 16 pins are used. Table 1-8 shows which set of LCD data pins (and LPLcdData pins) are used for each mode of operation, and Table 1-11: LCD Timing 1 Register (LcdTiming1) on page 1-35 shows the ordering of pixels delivered to a screen, again for each mode of operation.

Table 1-8 LCD controller data pin utilization

Color/Mono	Single-/Dual-panel	Passive/Active panel	Screen portion	Pins
Mono	Single	Passive	Whole	UPLcdData[3:0]
Mono	Single	Passive	Whole	UPLcdData[7:0]
Mono	Dual	Passive	Top Bottom	UPLcdData[3:0] UPLcdData[7:4]
Color	Single	Passive	Whole	UPLcdData
Color	Dual	Passive	Top Bottom	UPLcdData[7:0] LPLcdData[7:0]
Color	Single	Active	Whole	UPLcdData[7:0] LPLcdData[7:0]

1.7.3 LCD Done Mask (DoneMask)

The LCD Done Mask (DoneMask) bit masks the Frame Done (Done) bit of the LCD Status Register. When DoneMask = 0, the Frame Done (Done) bit of the LCD Status Register is masked. When DoneMask = 1, the Frame Done (Done) bit of the LCD Status Register is not masked.

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1.7.4 LCD Next Mask (Next Mask)

The LCD Next Mask (NextMask) bit masks the Next Frame (Next) bit of the LCD Status Register. When NextMask = 0, the Next Frame (Next) bit of the LCD Status Register is masked. When NextMask = 1, the Next Frame (Next) bit of the LCD Status Register is not masked.

1.7.5 LCD Error Mask (Error Mask)

The LCD Error Mask (ErrorMask) bit masks the Bus Error Status (BER) bit of the LCD Status Register. When ErrorMask = 0, the Bus Error Status (BER) bit of the LCD Status Register is masked. When ErrorMask = 1, the Bus Error Status (BER) bit of the LCD Status Register is not masked.

1.7.6 LCD TFT (LcdTFT)

The LCD TFT (LcdTFT) bit selects whether the LCD controller operates in passive (STN) or active (TFT) display control mode. When LcdTFT=0 : passive or STN mode is selected; all LCD data flow operates normally (including the use of the LCD's dither logic); and all LCD controller pin timing operates as described in 1.5.7 LCD controller Pins on page 1-21. When LcdTFT=1, active or TFT mode is selected. Video data is transferred via the DMA from off-chip memory to the input FIFO, is unpacked and used to select an entry from the palette (for 4 and 8 bits-per-pixel modes), just as for passive mode. See Figure 1-13 on page 1-32.

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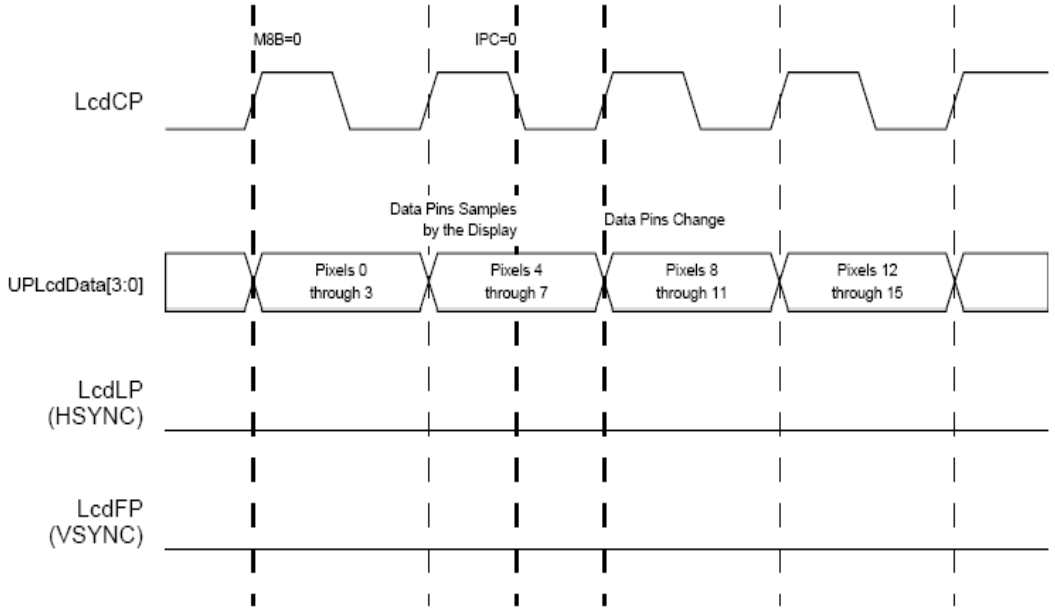

Figure 1-13 Passive mode pixel clock and data pin timing

The value read from the palette, however, bypasses the LCD's dither logic and is sent directly to the output FIFO to be output on the LCD's data pins. In TFT mode, the pixel size within the frame buffer is increased to 16 bits when 12- or 16-bit pixel encoding mode is enabled (BPP=11). Thus two 16-bit values are packed into each word in the frame buffer. See Figure 1-14 on page 1-33.

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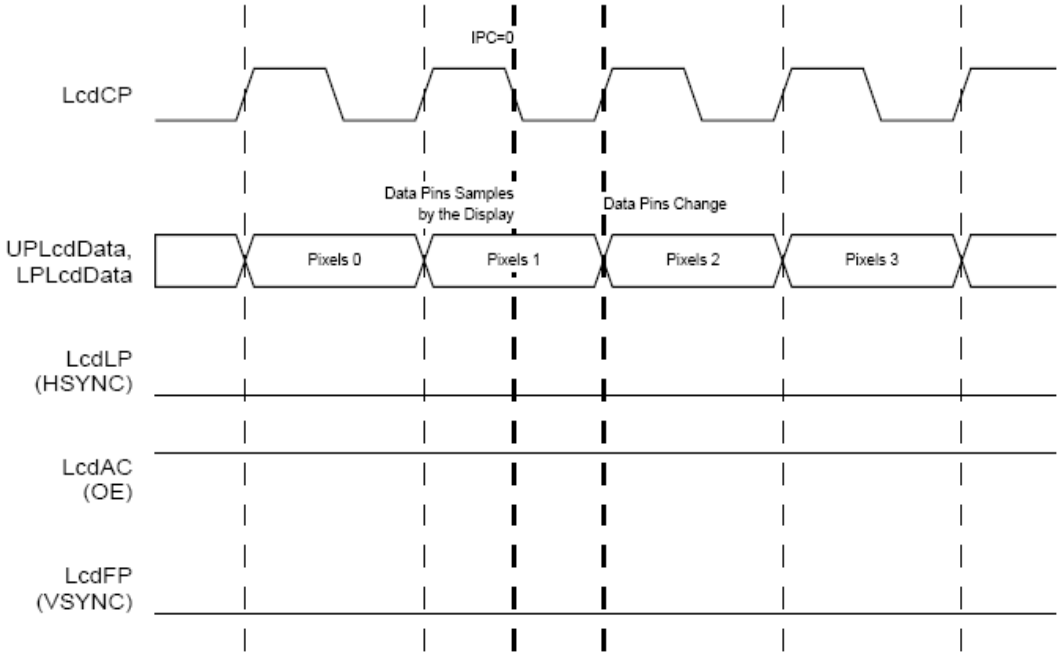

Figure 1-14 Active mode pixel clock and data pin timing

The size of the pixel encoding is increased in TFT mode because the LCD's dither logic is bypassed (which only supports 3-bit RGB dithering). Increasing the size of the pixel representation allows a total of 64K colors to be addressed using an off-chip palette that is used in conjunction with the LCD controller.

1.7.7 LCD Big Endian (LcdBE)

The LCD Big Endian (LcdBE) bit selects whether the LCD controller views external memory organization or the frame buffer as big or little endian. When LcdBE=0, little endian mode is selected, and pixel data is organized within the off-chip frame buffer. This is shown between Figure 1-7 on page 1-21 and Figure 1-10 on page 1-22. Pixels are packed into words starting with the least significant nibble, byte or half-word. When LcdBE=1, big endian mode is selected and pixel data is organized in memory in individual words starting with the most significant nibble, byte or half-word. The big/little endian select bit also effects the ordering of palette buffer entries in the external

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frame buffer. When LcdBE=0, half-word palette entries are packed into words starting with the least significant half-word. When LcdBE=1, palette entries are packed into half-words starting with the most significant half-word.

Note

The LcdBE does not affect the ordering of the 4-bit red/green/blue bit-fields, the 4-bit mono field within each 16-bit palette entry or the 2 bit-per-pixel (BPP) field contained with palette entry 0.

1.7.8 Mono 8 Bit Mode (M8B)

The Mono 8 Bit Mode (M8B) mode bit selects whether 4 or 8 bits are used to output pixel data to the LCD screen in single-panel or dual-panel monochrome mode.

When M8B=0, UPLcdData[3:0] is used to output four pixel values to the upper panel each pixel clock transition and UPLcdData[7:4] are used to output four pixel values to the lower panel of each pixel clock transition.

When M8B=1, UPLcdData[7:0] is used to output eight pixel values to the upper panel of each pixel clock, and LPLcdData[7:0] is used to output eight pixel values to the lower panel of each pixel clock.

Note

M8B does not affect any of the color modes.

1.7.9 1.7.10 FIFO DMA Request Delay (FDD)

The 8-bit FIFO DMA request delay (FDD) field is used to select the minimum number of memory controller clock cycles (half the frequency of the CPU clock) to wait between the servicing of each DMA request issued by the input FIFO. After a DMA request has completed, the value contained within FDD is loaded to a down counter that disables the input FIFO from issuing another DMA request until the counter decrements to zero. This counter ensures that the LCD's DMA does not fully consume the bandwidth of the AMBA bus. Once the counter reaches zero, any pending or future DMA requests by the FIFO cause the DMA to arbitrate for the ARM system bus (ASB). Once the DMA burst cycle has completed, the process re-starts and the value in FDD is loaded to the counter to create another delay period: this disables the FIFO from issuing a DMA request. FDD can be programmed with a value that causes the FIFO to wait from 0–255 memory clock cycles after the completion of one DMA request and before the start of the next request. When FDD=0h00, the FIFO DMA request delay function is disabled. This function is only used for palette loading.

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Table 1-9 on page 1-36 shows the location of all seven bit-fields located in LCD control register (LcdControl). LcdEn is the only control bit that is reset to a known state, ensuring that the LCD is disabled after a reset of the LCD controller. The user must program all other control bit-fields before setting LcdEn=1 (a half-word or word write can be used to configure the whole register while setting LcdEn), and must also disable the LCD controller when changing the state of any control bit within the LCD controller.

Note

Writes to reserved bits are ignored, and reads return zeros.

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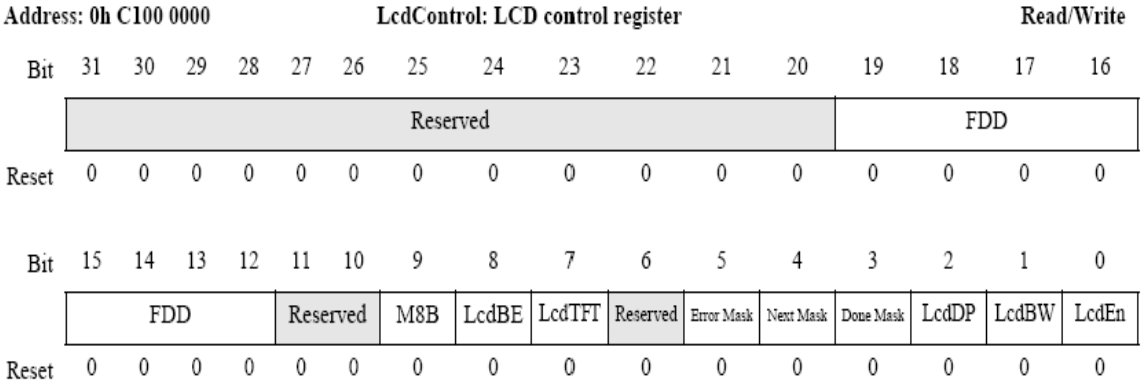

Figure 1-15 LCD control register LcdControl

Table 1-9 LCD control register LcdControl

Bit	Name	Description
0	LcdEn	LCD Controller Enable 0 - LCD controller disabled 1 - LCD controller enabled
1	LcdBW	LCD Monochrome 0 - Color operation enabled 1 - Monochrome operation enabled
2	LcdDP	LCD Dual-Panel 0 - Single-panel display enabled, UPLcdData[3:0] used for monochrome, UPLcdData[7:0] used for color 1 - Dual-panel display enabled, UPLcdData used for monochrome, UPLcdData and LPLcdData used for color
3	DoneMask	Done Mask 0 - Mask out the Frame Done (Done) Interrupt. 1 - Mask not active.
4	NextMask	Next Mask 0 - Mask out the Next Frame (Next) Interrupt. 1 - Mask not active

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Table 1-9 LCD control register LcdControl (continued)

Bit	Name	Description
5	ErrorMask	Error Mask 0 - Mask out the Bus Error Status (BER) Interrupt 1 - Mask not active.
7	LcdTFT	LCD TFT 0 - Passive or STN display operation enabled, dither logic is enabled 1 - Active or TFT display operation enabled, external palette and DAC required, dither logic bypassed, pin timing changes to support continuous pixel clock, output enable, VSYNC, HSYNC signals
8	LcdBE	Lcd Big Endian 0 - Little endian operation is selected, frame/pin buffer data is arranged into individual words of memory starting with the least significant nibble, byte or half-word 1 - Big endian operation is selected, frame/pin buffer data is arranged into individual words of memory starting with the most significant nibble, byte or half-word
9	M8B	Mono 8 Bit Mode 0 - UPLcdData[3:0] is used to output four pixel values to the upper panel each pixel clock transition and UPLcdData[7:4] are used to output four pixel values to the lower panel of each pixel clock transition. 1 - UPLcdData[7:0] is used to output eight pixel values to the upper panel of each pixel clock, and LPLcdData[7:0] is used to output eight pixel values to the lower panel of each pixel clock **Note** This bit is ignored in all other modes of operation except for single panel mode
11-10	-	Reserved
19-12	FDD	FIFO DMA Request Delay Encoded value (0—255) used to specify the number of memory controller clocks. The input FIFO DMA request should be disabled. The clock count starts after the last write of each burst cycle. While the counter is decrementing, all DMA requests from the input FIFO are masked. When the counter reaches zero, any pending or subsequent DMA requests are allowed to generate a four-word burst. Programming FDD=0h00 disables this function.
31-16	-	Reserved

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1.8 LCD Timing 0 Register

LCD Timing 0 Register (LcdTiming0) contains four bit-fields that are used as modulus values for a collection of down counters, each of which performs a different function to control the timing of several of the LCD's pins.

1.8.1 Pixels-per-line (PPL)

The pixels-per-line (PPL) bit-field is used to specify the number of pixels in each line or row on the screen. PPL is a 10-bit value that represents between 1–1024 pixels-per-line. PPL is used to count the correct number of pixel clocks that must occur before the line clock can be pulsed. (The bottom 4 bits of this register are not used).

1.8.2 Horizontal Sync Pulse Width (HSW)

The 6-bit horizontal sync pulse width (HSW) field is used to specify the pulse width of the line clock in passive mode, or horizontal synchronization pulse in active mode. **LcdLP** is asserted each time a line or row of pixels is output to the display and a programmable number of pixel clock delays have elapsed. When line clock is asserted, the value in HSW is transferred to a 6-bit down counter that uses the programmed pixel clock frequency to decrement. When the counter reaches zero, the line clock is negated. HSW can be programmed to generate a line clock pulse width ranging from 0–63 pixel clock periods (program to value required minus one).

Note

The pixel clock does not transition during the line clock pulse in passive display mode, but transitions in active display mode. Also, the polarity (active and inactive state) of the line clock is programmed using the Invert Hsync (IHS) bit in LcdTiming2.

1.8.3 Horizontal Front Porch (HFP)

The 8-bit Horizontal Front Porch (HFP) field is used to specify the number of dummy pixel clocks to insert at the end of each line or row of pixels before pulsing the line clock pin. Once a complete line of pixels is transmitted to the LCD driver, the value in HFP is used to count the number of pixel clocks to wait before pulsing the line clock. HFP generates a wait period ranging from 0–255 pixel clock cycles (program to value required minus one).

Note

The pixel clock pin **LcdCP**, does not transition during these dummy pixel clock cycles in passive display mode (pixel clock transitions continuously in active display mode).

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1.8.4 Horizontal Back Porch (HBP)

The 8-bit Horizontal Back Porch (HBP) field is used to specify the number of dummy pixel clocks to insert at the beginning of each line or row of pixels. After the line clock for the previous line has been negated, the value in HBP is used to count the number of pixel clocks to wait before starting to output the first set of pixels in the next line. HBP generates a wait period ranging from 0–255 pixel clock cycles (program to value required minus one).

Note

The pixel clock pin **LcdCP**, does not transition during these dummy pixel clock cycles in passive display mode (pixel clock transitions continuously in active display mode).

Table 1-10 on page 1-40 shows the location of the four bit-fields located in LCD Timing 0 Register (LcdTiming0). The LCD controller must be disabled (LcdEn=0) when changing the state of any field within this register. The reset state of all bitfields is unknown and must be initialized before enabling the LCD.

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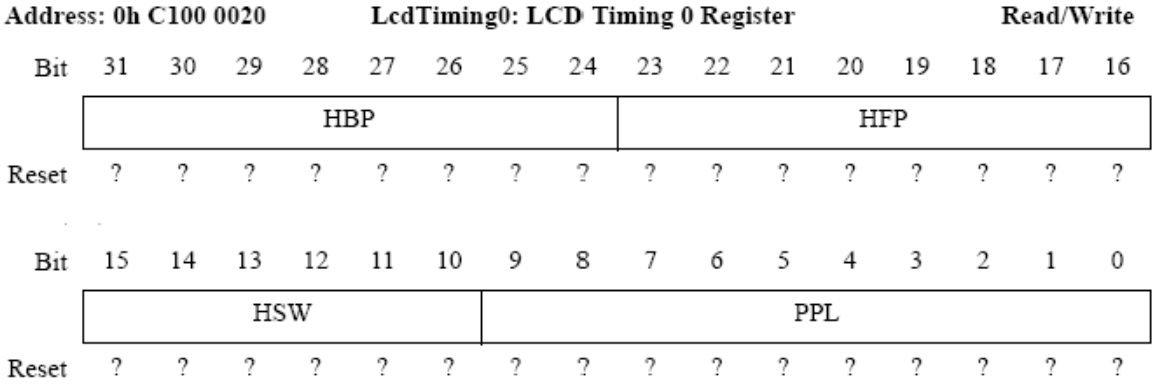

Figure 1-16 LCD Timing 0 Register (LcdTiming0)

Table 1-10 LCD Timing 0 Register (LcdTiming0)

Bit	Name	Description
9-0	PPL	Pixels-per-line Encoded value (from 1–1024) used to specify number of pixels contained within each line on the LCD display
15-10	HSW	Horizontal Sync Pulse Width Encoded value (from 0–63) used to specify number of pixel clock periods to pulse the line clock at the end of each line. Note that pixel clock is held in its inactive state during the generation of the line clock in passive display mode, and is permitted to transition in active display mode.
23-16	HFP	Horizontal Front Porch Encoded value (from 0–255) used to specify number of pixel clock periods to add to the end of a line transmission before line clock is asserted. Note that pixel clock is held in its inactive state during the end of line wait period in passive display mode, and is permitted to transition in active display mode.
31-24	HBP	Horizontal Back Porch Encoded value (from 0–255) used to specify number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display. Note that pixel clock is held in its inactive state during the beginning of line wait period in passive display mode, and is permitted to transition in active display mode.

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1.9 LCD Timing 1 Register

LCD Timing 1 Register (LcdTiming1) contains four bit-fields that are used as modulus values for a collection of down counters, each of which performs a different function to control the timing of several of the LCD lines.

1.9.1 Lines Per Panel (LPP)

The Lines Per Panel (LPP) bit-field is used to specify the number of lines or rows per LCD panel being controlled. In single-panel mode, it represents the total number of lines for the entire LCD display. In dual-panel mode it represents half the number of lines of the entire LCD display, since it is split into two panels. LPP is a 10-bit value which represents between 1–1024 Lines Per Panel. LPP is used to count the correct number of line clocks that must occur before the frame clock can be pulsed.

The LCD's DMA may overshoot the end of the frame buffer by one burst cycle (4 word read). The LCD's DMA reads these extra values but they are flushed from the input FIFO each time the frame clock is pulsed. The user must ensure that the four words immediately following the end of the frame buffer reside in legal memory space (that is, they do not cause a bus error if read). Since the LCD does not alter this memory (only reads are performed), these locations can be used for data storage unrelated to the LCD

1.9.2 Vertical Sync Pulse Width (VSW)

The 6-bit vertical sync pulse width (VSW) field is used to specify the pulse width of the vertical synchronization pulse in active mode, or is used to add extra dummy line clock delays between the Vertical Front Porch and Vertical Back Porch is in passive mode.

In active mode (LcdTFT=1), **LcdFP** is used to generate the vertical sync signal. It is asserted each time the last line or row of pixels for a frame is output to the display and a programmable number of line clock delays have elapsed. When **LcdFP** is asserted, the value in VSW is transferred to a 6-bit down counter that uses the line clock frequency to decrement. When the counter reaches zero, **LcdFP** is negated. VSW can be programmed to generate a vertical sync pulse width ranging from 0–63 line clock periods (program to value required minus one).

Note

The line clock transitions during generation of the vertical sync pulse. Also, the polarity (active and inactive state) of the **LcdFP** pin is programmed using the frame clock polarity (FCP) bit in LcdTiming2.

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In passive mode (LcdTFT=0), VSW does not affect the timing of the **LcdFP** pin, but instead can be used to add extra line clock delays between the end and beginning of frame line clock delay counts. The total number of line clock delays that are inserted between each frame is equal to the sum of the values in VFP, VSW and VBP. A counter is used to insert dummy line clock delays between frames by first using the value in VFP, then VSW, then VBP. In passive mode, it is irrelevant if one or all three of the fields are used to insert delays: the user need only ensure that the sum of the values in the three fields is equal to the total number of line clock delays that are needed between frames. Refer to 1.9.3 Vertical Front Porch (VFP) on page 1-34 and 1.9.4 Vertical Back Porch (VBP) on page 1-34 for a description of VFP and VBP.

Note

The line clock transitions during the insertion of the dummy line clock delay periods. VSW must be long enough to load the palette. VFP and VBP must be zero for passive mode display.

As mentioned above, VSW does not affect generation of the frame clock signal in passive mode. Passive LCD displays require that the frame clock is active on the rising-edge of the first line clock pulse of each frame, with adequate set-up and hold time. To meet this requirement, the LCD controller's frame clock pin is asserted on the rising-edge of the first pixel clock for each frame. The frame clock remains asserted for the remainder of the first line as pixels are output to the display, also during the assertion of the first line clock for the frame, and then negated on the rising-edge of the first pixel clock of the second line of each frame.

1.9.3 Vertical Front Porch (VFP)

The 8-bit Vertical Front Porch (VFP) field is used to specify the number of line clocks to insert at the end of each frame. Once a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed the VSYNC (LcdFP) signal is pulsed in active mode, or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates from 0–255 line clock cycles (program to value required minus one).

Note

The line clock pin **LcdLP** transitions during the generation of the VFP line clock periods.

See Figure 1-17 on page 1-43.

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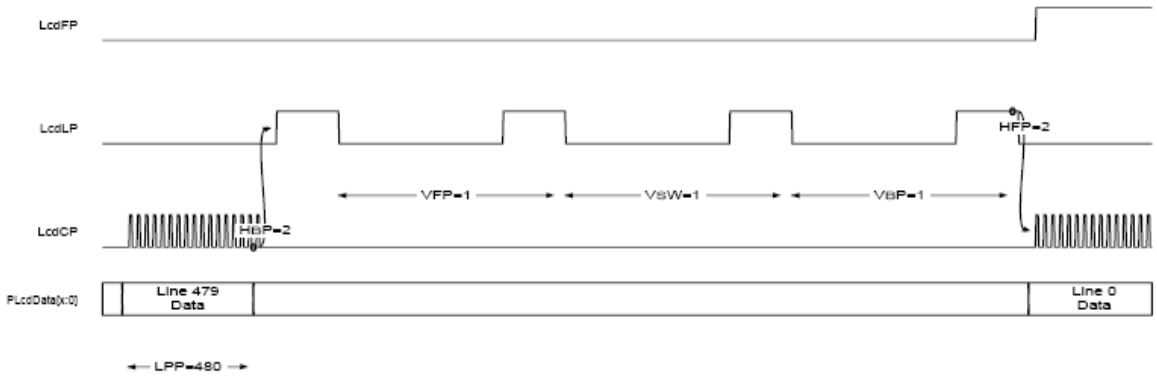

Figure 1-17 Passive mode end of frame timing

1.9.4 Vertical Back Porch (VBP)

The 8-bit Vertical Back Porch (VBP) field is used to specify the number of line clocks to insert at the beginning of each frame. The VBP count starts just after the VSYNC signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit-field in passive mode. After this has occurred, the value in VBP is used to count the number of line clock periods to insert before starting to output pixels in the next frame. VBP generates from 0–255 extra line clock cycles (program to value required minus one).

Note

The line clock pin LcdLP transitions during the generation of the VBP line clock wait periods. Note also that the user should adjust the value of VBP appropriately such that enough line clock cycles are permitted to elapse: this allows the on-chip palette to be completely filled via the DMA, and allows a sufficient number of encoded pixel values to be input from the frame buffer, processed by the dither logic then placed in the output FIFO, ready to be output to the LCD's data lines.

See Figure 1-18 on page 1-44.

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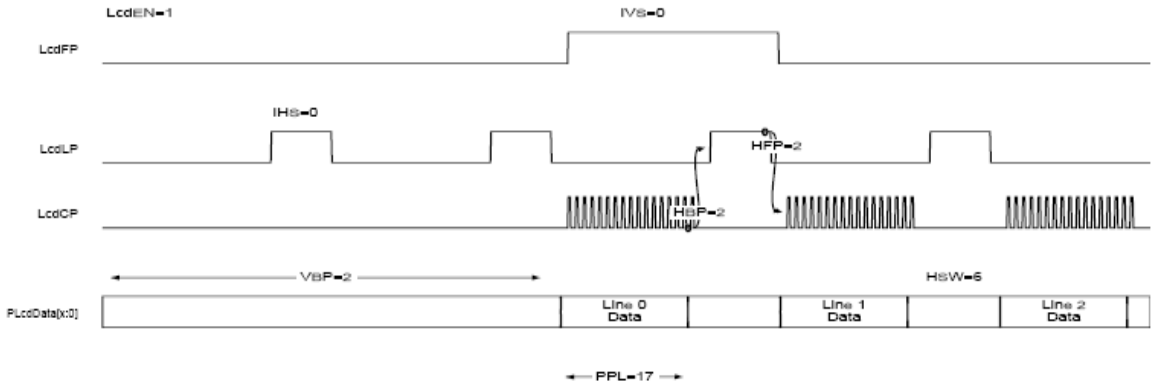

Figure 1-18 Passive mode beginning of frame timing

Table 1-11 on page 1-45 shows the location of the four bit-fields located in LCD Timing 1 Register (LcdTiming1). The LCD controller must be disabled (LcdEn=0) when changing the state of any field within this register. The reset state of all bitfields is unknown and must be initialized before enabling the LCD.

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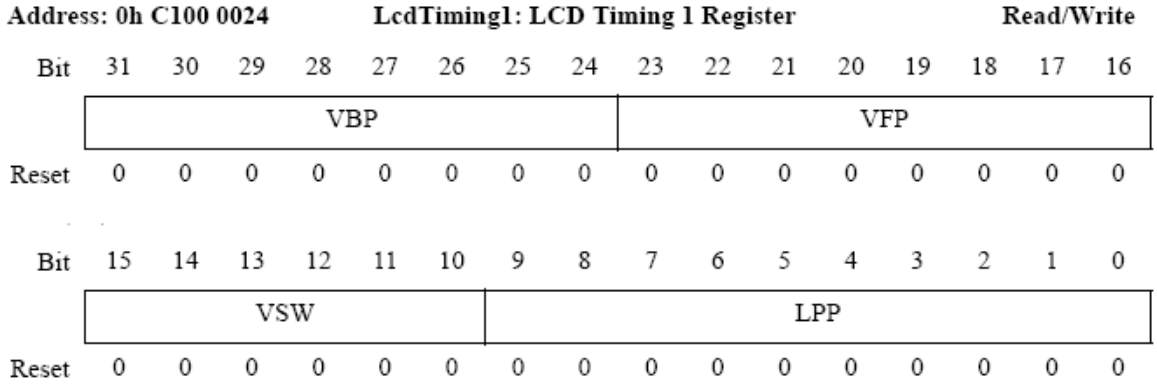

Figure 1-19 LCD Timing 1 Register (LcdTiming1)

Table 1-11 LCD Timing 1 Register (LcdTiming1)

Bit	Name	Description
9-0	LPP	Lines Per Panel Value (from 1–1024) used to specify number of lines per panel. For single-panel mode, this represents the total number of lines on the LCD display; for dual-panel mode, this represents half the number of lines on the whole LCD display.
15-10	VSW	Vertical Sync Pulse Width In active mode (LcdTFT=1), value (from 0–63) used to specify number of line clock periods to pulse the **LcdFP** pin at the end of each frame after the end of frame wait (VFP) period elapses. Frame clock used as VSYNC signal in active mode. In passive mode (LcdTFT=0), value (from 0–63) used to specify number of extra line clock periods to insert after the vertical front porch (VFP) period has elapsed. Note that the width of **LcdFP** is not effected by VSW in passive mode, and that line clock transitions during the insertion of the extra line clock periods.
23-16	VFP	Vertical Front Porch Value (from 0–255) used to specify number of line clock periods to add to the end of each frame. Note that the line clock transitions during the insertion of the extra line clock periods.
31-24	VBP	Vertical Back Porch Value (from 0–255) used to specify number of line clock periods to add to the beginning of a frame before the first set of pixels is output to the display. Note that line clock transitions during the insertion of the extra line clock periods.

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1.10 LCD Timing 2 Register

LCD Timing 2 Register (LcdTiming2) contains seven different bit-fields that are used to control various functions associated with the timing of the LCD controller.

1.10.1 Pixel Clock Divider (PCD)

The 8-bit pixel clock divider (PCD) field is used to select the frequency of the pixel clock. PCD can generate a range of pixel clock frequencies from BCLK/2 to BCLK/257, where BCLK is the programmed frequency of the crystal clock. The pixel clock frequency should be adjusted to meet the required screen refresh rate. The refresh rate depends on:

- the number of pixels for the target display
- whether single- or dual-panel mode is selected
- whether monochrome or color mode is selected
- the number of pixel clock delays programmed at the beginning and end of each line
- the number of line clocks inserted at the beginning and end of each frame
- the width of the VSYNC signal in active mode or VSW line clocks inserted in passive mode
- the width of the frame clock or HSYNC signal

All of these factors alter the time duration from one frame transmission to the next. Different display manufacturers require different frame refresh rates, depending on the physical characteristics of the display. PCD is used to alter the pixel clock frequency in order to meet these requirements. Note that PCD is also used in parallel data input mode to select the frequency of pixel clock. Pixel clock is used to synchronously signal the off-chip device to drive data to the LCD's data pins, and to signal the output FIFO to latch the data from the pins. The frequency of the pixel clock for a set PCD value, or the required PCD value to yield a target pixel clock frequency can be calculated using the following equations:

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$$PixelClock = \frac{BCLK}{PCD + 2}$$

$$PCD = \frac{PixelClock}{BCLK} - 2$$

Figure 1-20 Equations

Note

For TFT mode, the minimum PCD is 2. For STN mode, the minimum PCD is 4 for mono 4 bit mode, 8 for mono 8 bit mode and 3 for color mode.

1.10.2 AC-bias Pin Frequency (ACB)

The 8-bit AC-bias frequency (ACB) field is used to specify the number of line clock periods to count between each toggle of the AC-bias pin (**LcdAC**). After the LCD controller is enabled, the value in ACB is loaded to an 8-bit down counter, and the counter begins to decrement using the line clock. When the counter reaches zero it stops, the state of LcdAC is reversed, and the whole procedure starts again. The number of line clocks between each AC-bias pin transition ranges from 0–255 (program to value required minus one). This line is used by the LCD display to periodically reverse the polarity of the power supplied to the screen to eliminate DC offset.

Note

The ACB bit field has no effect on LcdAC in active mode. This is due to the fact that the pixel clock transitions continuously in active mode; the AC Bias line is used as an output enable signal. The AC Bias is asserted by the LCD controller in active mode; this occurs whenever pixel data is driven out to the data pins to signal to the display when it may latch pixels using the pixel clock.

1.10.3 AC-bias Line Transitions Per Interrupt (ACBI)

The 4-bit AC Bias line transitions-per-interrupt (ACBI) field is used to specify the number of **LcdAC** line transitions to count before setting the AC bias count status (ABC) bit in the LCD controller status register, which signals an interrupt request. After the LCD controller is enabled, the value in ACBI is loaded to a 4-bit down counter, and the counter decrements each time the AC bias line state is inverted. When the counter reaches zero it stops, and the AC bias count (ABC) bit is set in the status register. Once

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ABC is set, the 4-bit down counter is reloaded with the value in ACBI and is disabled until ABC is cleared. Once ABC is cleared by the CPU, the down counter is enabled, and again decrements each time the AC bias line is flipped. The number of AC bias line transitions between each interrupt request ranges from 0–15. Note that programming ACBI = 0h0000 disables the AC bias line transitions-per-interrupt function.

1.10.4 Invert Vsync (IVS)

The Invert VSync (IVS) bit is used to invert the polarity of the LcdFP signal (for passive mode display). When IVS=1, LcdFP is active low. When IVS=0, LcdFP is active high. (LcdFP is used as VSYNC signal in active display mode.)

1.10.5 Invert Hsync (IHS)

The Invert HSync (IHS) bit is used to invert the polarity of the LcdLP signal. When IVS=1, LcdLP is active low. When IVS=0, LcdLP is active high. (LcdLP is used as HSYNC signal in active display mode.)

1.10.6 Invert Pixel Clock (IPC)

The Invert Pixel Clock (IPC) bit is used to select which edge of the pixel clock pixel data is driven out onto the LCD's data lines. When IPC=0, data is driven onto the LCD's data lines on the rising-edge of **LcdCP**. When IPC=1, data is driven onto the LCD's data lines on the falling-edge of **LcdCP**.

1.10.7 Invert Output Enable (IEO)

The Invert Output Enable (IEO) bit is used to select the active and inactive state of the output enable signal in active display mode. In this mode, the AC-bias pin is used as an enable that signals the off-chip device when data is actively being driven out using the pixel clock. When IEO=0, the **LcdAC** pin is active high. When IEO=1, the **LcdAC** pin is active low. In active display mode, data is driven onto the LCD's data lines on the programmed edge of **LcdCP** when **LcdAC** is in its active state.

Note

IEO does not affect **LcdAC** in passive display mode.

Table 1-12 on page 1-49 shows the location of the seven different bit-fields located in LCD Timing 2 Register (LcdTiming2). The LCD controller must be disabled (LcdEn=0) when changing the state of any field within this register. The reset state of all bit-fields is unknown and must be initialized before enabling the LCD. Note that writes to reserved bits are ignored and reads return zeros.

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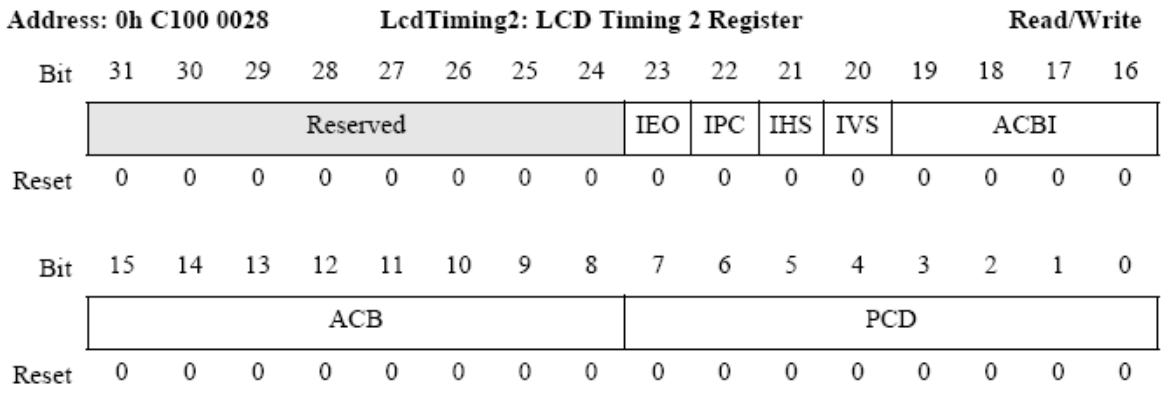

Figure 1-21 LCD Timing 2 Register LcdTiming2

Table 1-12 LCD Timing 2 Register LcdTiming2 (continued)

Bit	Name	Description
7–0	PCD	Pixel Clock Divisor Value (from 0–255) used to specify the frequency of the pixel clock based on the CPU clock (BCLK) frequency. Pixel clock frequency can range from BCLK/2 to BCLK/257. Pixel Clock Frequency = BCLK/2(PCD+2). Note that PCD must also be programmed in parallel data input mode to select the rate in which data is synchronously driven into and latched by the LCD controller.
15–8	ACB	AC Bias Pin Frequency Value (from 0–255) used to specify the number of line clocks to count before transitioning the AC Bias pin. This pin is used to periodically invert the polarity of the power supply to prevent DC charge build-up within the display. ACB = Number of line clocks/toggle of the **LcdAC** pin.
19–16	ACBI	AC Bias Pin Transitions per Interrupt Value (from 0–255) used to specify the number of AC Bias pin transitions to count before setting the line count status (LCS) bit, signalling an interrupt request. Counter is frozen when LCS is set, and is restarted when LCS is cleared by software. This function is disabled when ACBI=0x0000.

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Table 1-12 LCD Timing 2 Register LcdTiming2 (continued) (continued)

Bit	Name	Description
20	IVS	Invert Vsync 0 - **LcdFP** pin is active high and inactive low. 1 - **LcdFP** pin is active low and inactive high. Active mode: vertical sync pulse active between frames, after end of frame wait period. Passive mode: frame clock active during first line of each frame.
21	IHS	Invert Hsync 0 - **LcdLP** pin is active high and inactive low. 1 - **LcdLP** pin is active low and inactive high. Active and passive mode: horizontal sync pulse/line clock active between lines, after end of line wait period.
22	IPC	Invert Pixel Clock 0 - Data is driven on the LCD's data lines on the rising-edge of **LcdCP**. 1 - Data is driven on the LCD's data lines on the falling-edge of **LcdCP**.
23	IEO	Invert Output Enable 0 - **LcdAC** pin is active high in active display mode. 1 - **LcdAC** pin is active low in active display mode. Active display mode: data driven out to the LCD's data lines on programmed pixel clock edge when AC-bias is active. Note that IEO is ignored in passive display mode.
31–24	-	Reserved

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1.11 LCD Controller DMA Registers

The LCD controller has two fully-independent DMA channels. These are used to transfer frame buffer data (relating to each frame displayed) from off-chip memory to the LCD's palette RAM and the input FIFO. DMA channel 1 is used for single-panel display mode, and for the upper screen in dual-panel mode. DMA channel 2 is used exclusively for the lower screen in dual-panel mode. Both DMA channels contain a base address pointer and current address pointer register.

Note

The LCD's DMA engine has the highest priority on the AMBA bus as a bus master in order to prevent other bus masters from starving the LCD screen.

The two DMA channels use a separate set of base address and current address pointers. The user must initialize the base address pointer registers before enabling the LCD. Once enabled, the base address is transferred to the current address pointer.

After the LCD is enabled, the input FIFO requests a DMA transfer and the DMA makes a four-word burst access from off-chip memory using the address contained within the current address pointer. The pointer is incremented by four (bytes) each time a word is read from memory (ie. bit 2 of the pointer is incremented). Each of the four words from the burst are loaded into the top of the input FIFO. The LCD then takes one value at a time from the bottom of the FIFO, unpacks it into individual encoded pixel values and uses the values to index into the palette. Each time the input FIFO contains four empty entries, another DMA request is made and another four-word burst is performed. To calculate the frame buffer end address, the DMA controller uses the values programmed in the pixels-per-line (PPL), Lines Per Panel (LPP), LCD Dual Panel (LcdDP), LCD Black and White (LcdBW) and Mono Eight Bit (M8B) bit-fields within the control registers, as well as the bits-per-pixel (BPP) field contained within the first entry of the palette buffer from the off-chip frame buffer. When the current address pointer reaches the calculated end of buffer address, the value in the base address pointer is again transferred to the current address pointer.

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1.12 DMA Channel 1 Base Address Register

DMA channel 1 base address register (DBAR1) is a 32-bit register that is used to specify the base address of the off-chip frame buffer for DMA channel 1. The base address pointer register can be both read and written. Addresses programmed in the base address register must be aligned on word boundaries, thus the least significant two bits (DBAR1[1:0]) must always be written with zeros. The user must initialize the base address register before enabling the LCD, and may also write a new value to it while the LCD is enabled to allow a new frame buffer to be used for the next frame. The user can change the state of DBAR1 while the LCD controller is active just after the Next Frame (Next) status bit is set with the LCD's status register that generates an interrupt request. This status bit indicates that the value in the base address pointer has transferred to the current address pointer register and that it is safe to write a new base address value. DMA channel 1 is used to transfer frame buffer data from off-chip memory to the LCD's input FIFO and the palette RAM for single-panel mode, and for the top half of the screen in dual-panel mode.

Note

DBAR1 is not reset and must be initialized before enabling the LCD.

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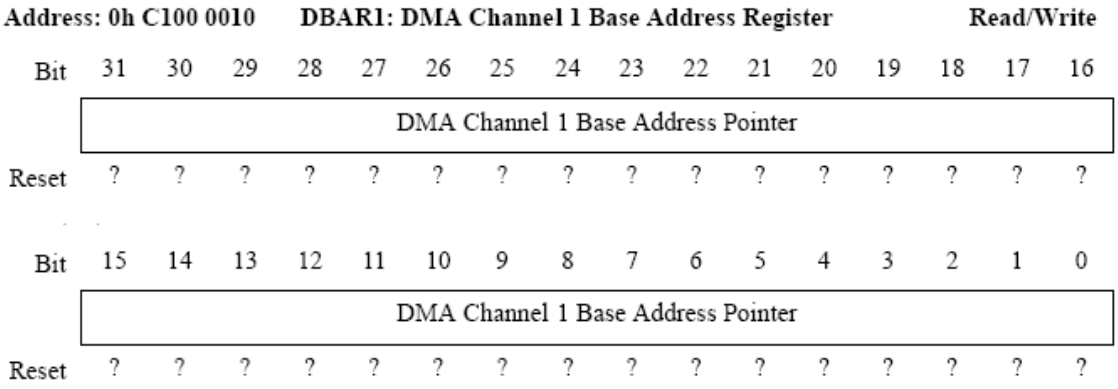

Figure 1-22 DMA channel 1 base address register DBAR1

Table 1-13 DMA channel 1 base address register DBAR1

Bit	Name	Description
31-0	DBAR1	DMA Channel 1 Base Address Pointer Used to specify the base address of the frame buffer within off-chip memory. Value in DBAR1 transferred to current address pointer register 1 when LCD is first enabled (LcdEN=1). DBAR1 should only be written when the LCD is disabled, or immediately after an interrupt is generated by the setting of the Next Frame (Next) status bit. The base address must be on a quad-word boundary, so the user must always write bits 0 and 1 to zero.

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1.13 DMA Channel 1 Current Address Register

DMA channel 1 current address register (DCAR1) is a 32-bit read-only register that is used by DMA channel 1 to keep track of the address of the DMA transfer currently in progress, or the address of the next DMA transfer. Any time the LCD is enabled or the value in the current address pointer register equals the calculated end address value, the contents of the base address pointer register is transferred to the current address pointer. This register can be read to determine the approximate line that the LCD controller is currently processing and driving out to the display.

Note

DCAR1 is a read-only register that is not reset, and is not initialized until after the LCD is first enabled, causing the contents of the base address register to be transferred to it.

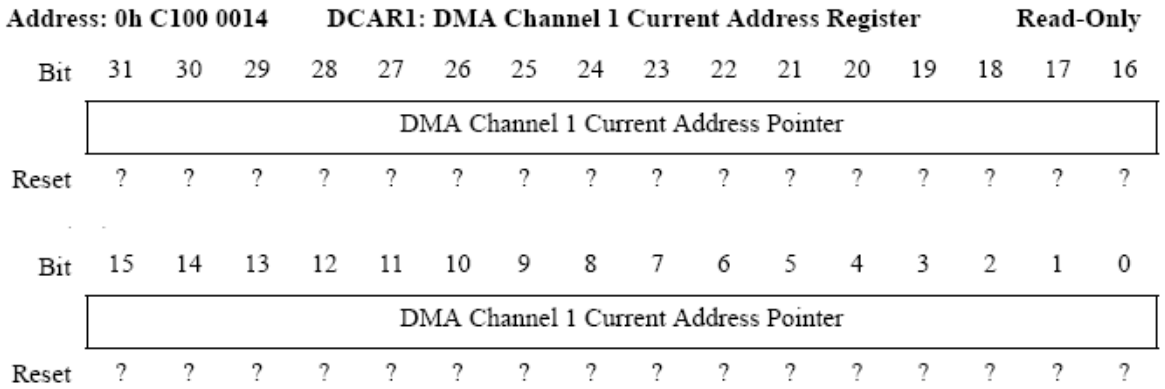

Figure 1-23 DMA channel 1 current address register DCAR1

Table 1-14 DMA channel 1 current address register DCAR1

Bit	Name	Description
31-0	DCAR1	DMA Channel 1 Current Address Pointer Read-only register that continuously reflects the current address that DMA channel 1 is transferring from/to, or will use in the next transfer. Base address register is transferred to this register whenever the LCD is first enabled (LcdEN=1).

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1.14 DMA Channel 2 Base and Current Address Registers

DMA channel 2's base and current address registers function exactly like DMA channel 1's except that they are used exclusively for dual-panel operation. Refer to *DMA Channel 1 Base Address Register* on page 1-52 and *DMA Channel 1 Current Address Register* on page 1-54. When LcdDP=1, DMA channel 2 is used to supply frame buffer data to the lower half of the display.

Note

The palette buffer that resides within the first 16 or 256 entries of the frame buffer is only utilized by DMA channel 1. The user should not place palette entries into the frame buffer for DMA channel 2. Thus the base address for channel 2 points to the first encoded pixel values for the lower half of the display.

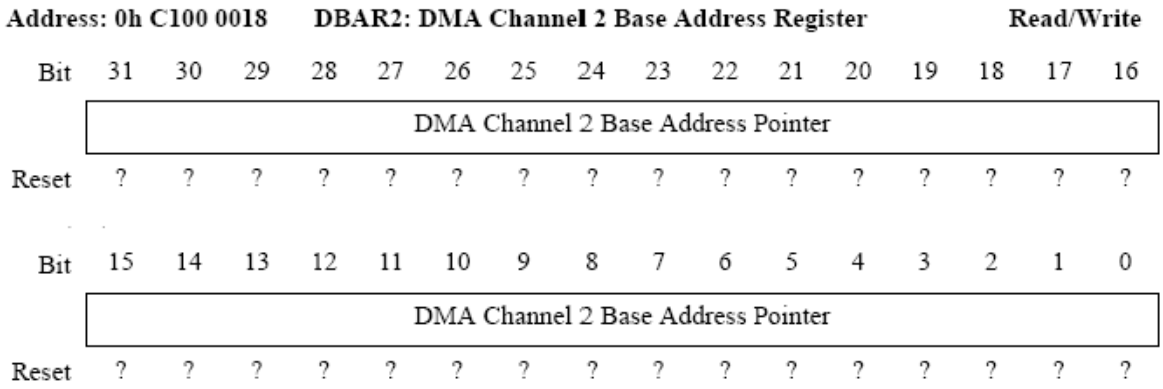

Figure 1-24 DMA channel 2 base address register DBAR2

Table 1-15 DMA channel 2 base address register DBAR2

Bit	Name	Description
31-0	DBAR2	DMA Channel 2 Base Address Pointer Used to specify the base address of the frame buffer within off-chip memory for the lower half of the display in dual-panel operation. Value in DBAR2 transferred to current address pointer register 2 when LCD first enabled (LcdEN=1). DBAR2 should only be written when the LCD is disabled, or immediately after an interrupt is generated by the setting of the Next Frame (Next) status bit. The base address must be on a quad-word boundary, so the user must always write bits 0 and 1 to zero.

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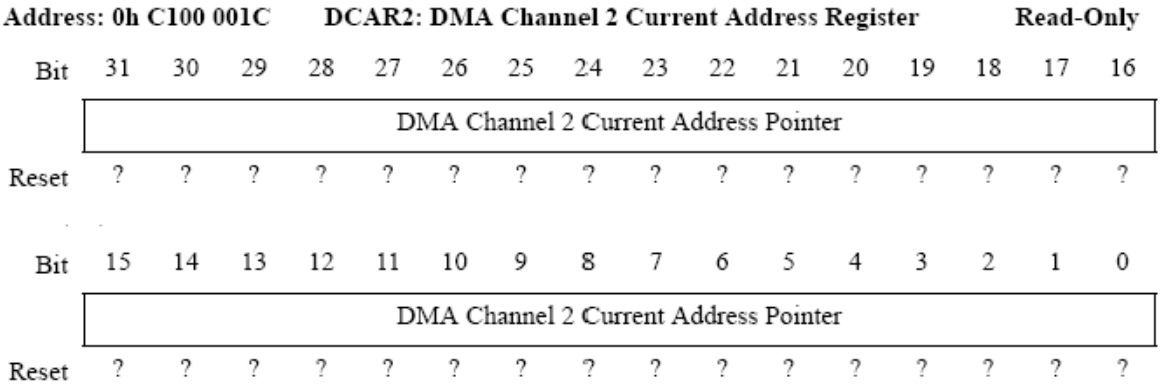

Figure 1-25 DMA channel 2 current address register DCAR2

Table 1-16 DMA channel 2 current address register DCAR2

Bit	Name	Description
31-0	DBAR2	DMA Channel 2 Current Address Pointer Read-only register that continuously reflects the current address that DMA channel 2 is transferring from or will use in the next transfer. Base address register is transferred to this register whenever the LCD is enabled, or when the current address is equal to the calculated end address of the buffer.

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1.15 LCD Controller Status Register

The LCD controller status register (LCSR) contains bits that signal over- and under-run errors for both the input and output FIFOs, as well as the AC-bias pin transition count/LCD disabled/DMA base update ready/and DMA transfer bus error conditions. Each of these hardware-detected events signals an interrupt request to the interrupt controller.

Each of the LCD's status bits signals an interrupt request as long as the bit is set. Once the bit is cleared, the interrupt is cleared. Read/write bits are called status bits; read-only bits are called flags. Status bits are referred to as "sticky" (that is, once set by hardware, must be cleared by software). Writing 1 to a sticky status bit clears it; writing zero has no effect. Read-only flags are set and cleared by hardware; writes have no effect.

1.15.1 Frame Done (Done) (read-only)

The Frame Done (Done) is a read-only bit that is set after the LCD has been disabled and the frame that is active finishes being output to the LCD's data pins. It is cleared by writing the base address and enabling the LCD for single-panel mode. In dual-panel mode, set M8B to 1, write the upper and lower base addresses, then enable the LCD. When the LCD is disabled by clearing the LCD enable bit (LcdEn=0) in LcdControl, the LCD allows the current frame to complete before it is disabled. After the last set of pixels is clocked out onto the LCD's data pins by the pixel clock, the LCD is disabled and Done is set.

1.15.2 Next Frame (Next) (read-only)

The Next Frame (Next) is a read-only bit that is set after the contents of the DMA base address register are transferred to the DMA current address register 1, and is cleared when the DMA base address register 1 is written, or by writing the lower panel base address in dual-panel mode (LcdDP=1).

1.15.3 Bus Error Status (BER) (read/write)

The bus error status (BER) bit is set when a DMA transfer causes a bus error to occur on the ARM system bus. A bus error is signalled when the DMA controller attempts to access a reserved or non-existent memory space. When this occurs, the LCD controller's memory controller returns zeros for a read; it asserts the bus error signal to the LCD's DMA, which in turn causes the BER bit to be set. The DMA is not disabled as a result of the bus error, and operation continues as normal. If a DMA access causes a bus error, zeros are returned by the memory controller that either causes a palette entry to be filled with zeros (lowest intensity color or white) or, if pixel data is being DMA'd, the LCD accesses the first location of the palette RAM one or more times.

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1.15.4 AC Bias Count Status (ABC) (read/write)

The AC bias count status (ABC) bit is set each time the AC bias line (LcdAC) transitions a particular number of times as specified by the AC bias line transitions per interrupt (ACBI) field in LcdTiming2. If ACBI is programmed with a non-zero value, a counter is loaded with the value in ACBI and is decremented each time the LcdAC line reverses state. When the counter reaches zero the ABC bit is set, which signals an interrupt request to the interrupt controller. The counter reloads using the value in ACBI, but does not start to decrement again until ABC is cleared by the user.

1.15.5 FIFO Underflow Status (FUF) (read/write)

In LCD mode, the FIFO underflow status (FUF) bit is set when the output FIFO is completely empty and the LCD's data pins driver logic attempts to fetch data from the FIFO. This area of the register is cleared by writing 1 to the bit.

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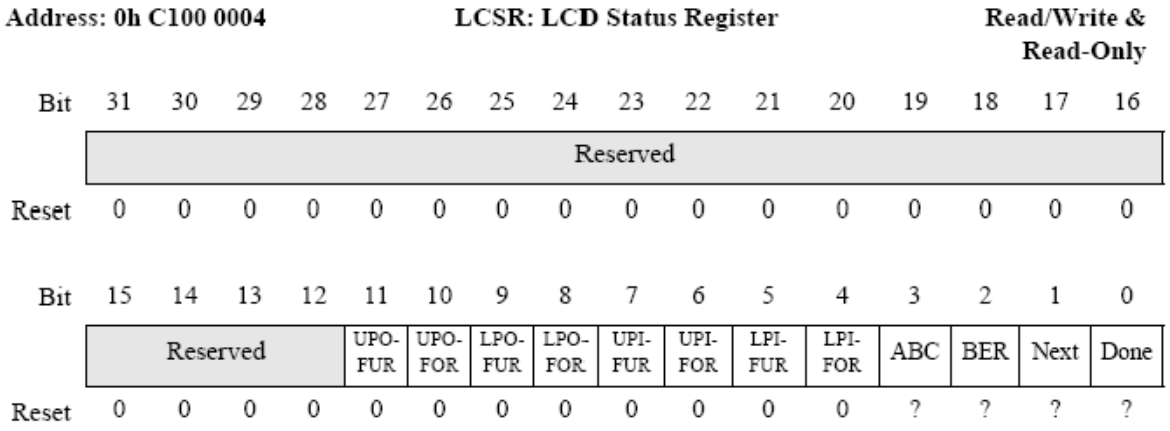

Figure 1-26 LCD status register

Table 1-17 LCD status register

Bit	Name	Description
0	Done	Frame Done (read-only) 0 - LCD is enabled 1 - LCD disabled and the active frame has just completed
1	Next	Next Frame (read-only) 0 - Next Frame has been written and has not yet been transferred to the current address register 1 - Next Frame has been transferred to the current address register, triggered either by enabling the LCD, or when the current address equalled the end address pointer value
2	BER	Bus Error Status 0 - DMA has not attempted an access to reserved/non-existent memory space 1 - DMA has attempted an access to a reserved/non-existent location in external memory. The errant DMA read returns zeros.
3	ABC	AC Bias Count Status 0 - AC bias transition counter has not decremented to zero. 1 - AC bias transition counter has decremented to zero, indicating that the LcdAC line has transitioned the number of times which is specified by the ACBI control bit-field. Counter is reloaded with the value in ACBI but is disabled until the user clears ABC.

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Table 1-17 LCD status register (continued)

Bit	Name	Description
4	LPIFOR	Lower Panel Input Fifo Overrun 0 - Input FIFO has not overrun 1 - DMA attempted to place data into the input FIFO after it has been filled
5	LPIFUR	Lower Panel Input Fifo Underrun 0 - Input FIFO has not underrun 1 - DMA not supplying data to the input FIFO at a sufficient rate, FIFO has completely emptied and pixel unpacking logic has attempted to take added data from the FIFO
6	UPIFOR	Upper Panel Input Fifo Overrun 0 - Input FIFO has not overrun 1 - DMA attempted to place data into the input FIFO after it has been filled
7	UPIFUR	Upper Panel Input Fifo Underrun 0 - Input FIFO has not underrun 1 - DMA not supplying data to the input FIFO at a sufficient rate, FIFO has completely emptied and pixel unpacking logic has attempted to take added data from the FIFO
8	LPOFOR	Lower Panel Output Fifo Overrun 0 - Output FIFO has not overrun 1 - LCD dither logic attempted to place data into the output FIFO after it had been filled
9	LPOFUR	Lower Panel Output Fifo Underrun 0 - Output FIFO has not underrun 1 - LCD dither logic not supplying data to output FIFO at a sufficient rate, FIFO had completely emptied and data pin driver logic has attempted to take added data from the FIFO.
10	UPOFOR	Upper Panel Output Fifo Overrun 0 - Output FIFO has not overrun 1 - LCD dither logic attempted to place data into the output FIFO after it had been filled
11	UPOFUR	Upper Panel Output Fifo Underrun 0 - Output FIFO has not underrun 1 - LCD dither logic not supplying data to output FIFO at a sufficient rate, FIFO had completely emptied and data pin driver logic has attempted to take added data from the FIFO.
31-12	-	Reserved

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1.16 Gray Scaler Test Read Frame Phase Register

If the Gray Scaler Test mode read of the Frame Phase Accumulator is read, the data returned in this register is the data out of the Gray Scaler's Frame Phase accumulator.

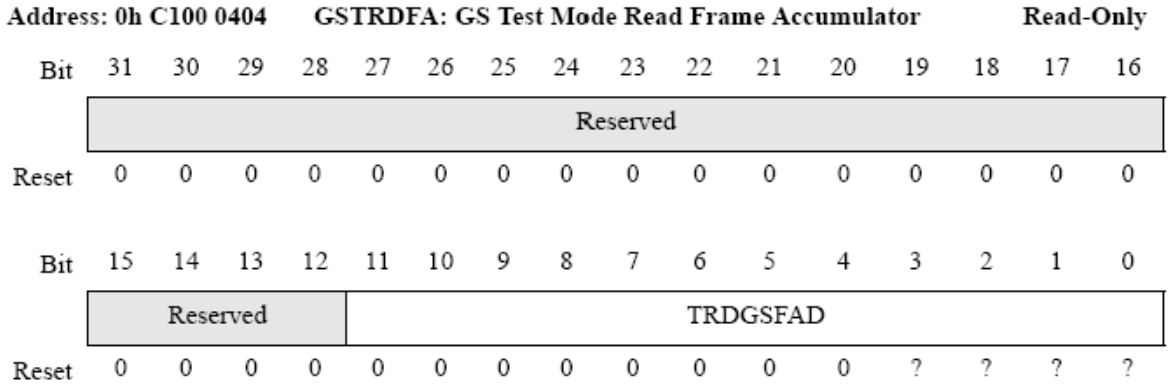

Figure 1-27 GS Test Mode Read Frame Accumulator register

Table 1-18 GS Test Mode Read Frame Accumulator register

Bit	Name	Description
11-0	GSTRDFAD	GS Test Mode Read Frame Accumulator Data When read, the data in this register is the data of the Frame Phase Accumulator.
31-12	-	Reserved.

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1.17 Gray Scaler Test Read Row Phase Register

If the Gray Scaler Test mode read of the Row Phase Accumulator is read, the data returned in this register is the data out of the Gray Scaler's Row Phase accumulator.

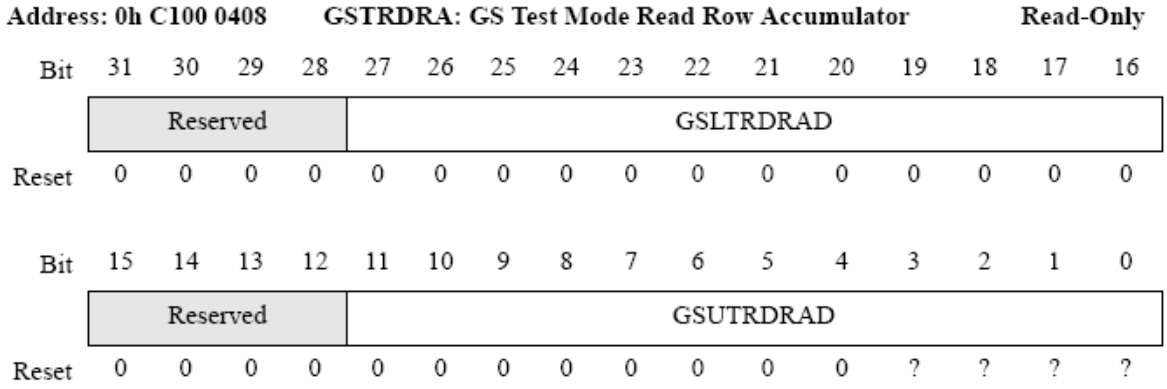

Figure 1-28 GS Test Mode Read Row Accumulator register

Table 1-19 GS Test Mode Read Row Accumulator register

Bit	Name	Description
11-0	GSUTRDRAD	GS Upper Panel Test Mode Read Row Accumulator Data When read, the data in this register is the data of the Upper Panel Row Phase Accumulator.
15-12	-	Reserved.
27-16	GSLTRDRAD	GS Lower Panel Test Mode Read Row Accumulator Data When read, the data in this register is the data of the Lower Panel Row Phase Accumulator.
31-28	-	Reserved.

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1.18 Gray Scaler Test Read Column Phase Register

If the Gray Scaler Test mode read of the Column Phase Accumulator is read the data returned in this register is the data out of the Gray Scaler's Column Phase accumulator.

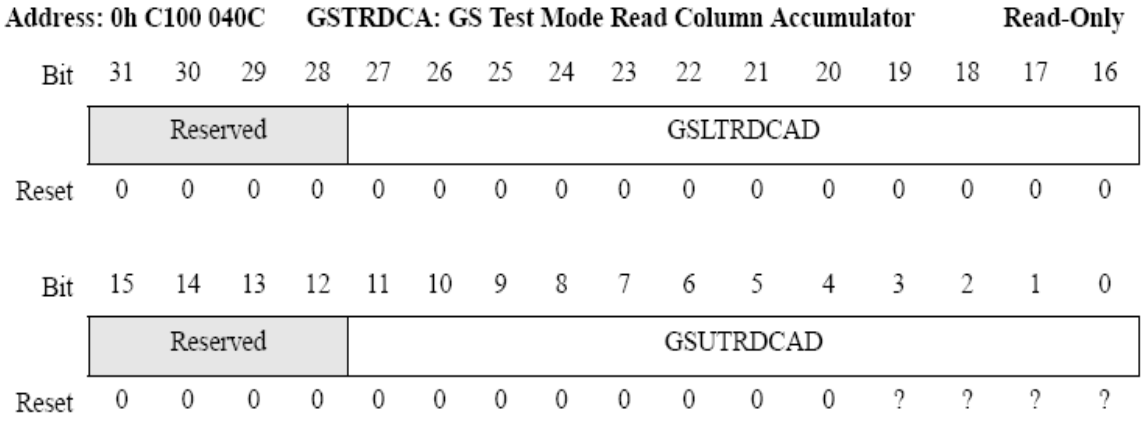

Figure 1-29 GS Test Mode Read Column Accumulator register

Table 1-20 GS Test Mode Read Column Accumulator register

Bit	Name	Description
11-0	GSUTRDCAD	GS Upper Panel Test Mode Read Column Accumulator When read, the data in this register is the data of the Upper Panel Column Phase Accumulator.
15-12	-	Reserved.
27-16	GSLTRDCAD	GS Lower Panel Test Mode Read Column Accumulator When read, the data in this register is the data of the Lower Panel Column Phase Accumulator.
31-28	-	Reserved.

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1.19 Upper Panel Palette Test Read

If the Upper Panel Palette test locations are read then the data in the location is the data in the Upper panel Palette at the corresponding address.

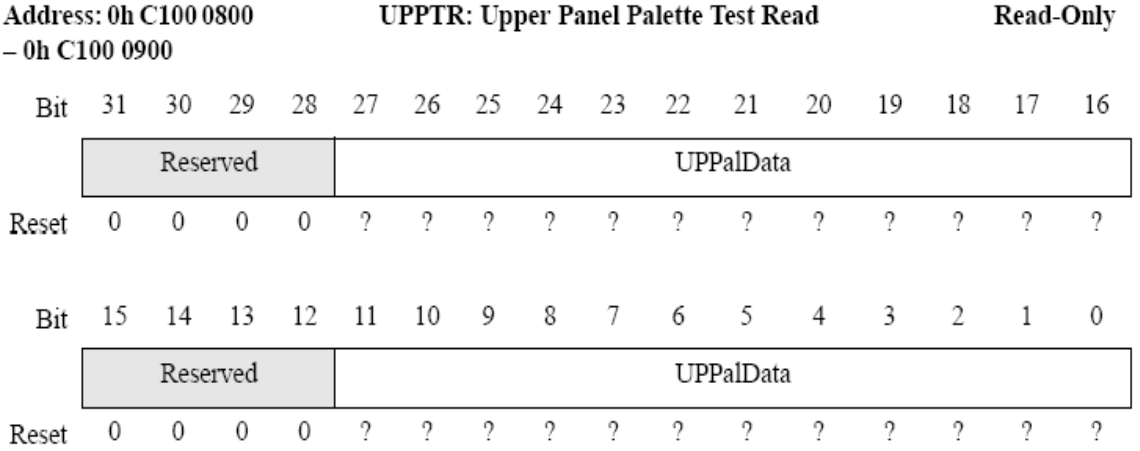

Figure 1-30 Upper Panel Palette Test Read register

Table 1-21 Upper Panel Palette Test Read register

Bit	Name	Description
11-0	UPPalData	Upper Panel Palette Test Read Data When read, the data in the location is the data of the Upper Panel Palette.
15-12	-	Reserved.
27-16	UPPalData	Upper Panel Palette Test Read Data When read, the data in the location is the data of the Upper Panel Palette.
31-28	-	Reserved

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1.20 Lower Panel Palette Test Read

If the Lower Panel Palette test locations are read, the data in the location is the data in the Upper panel Palette at the corresponding address.

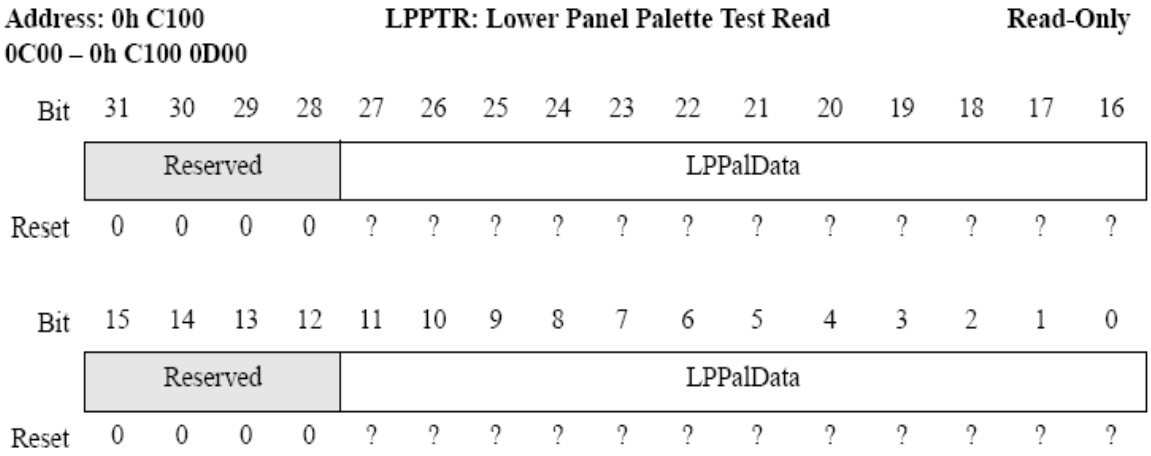

Figure 1-31 Lower Panel Palette Test Read register

Table 1-22 Lower Panel Palette Test Read register

Bit	Name	Description
11-0	LPPalData	Lower Panel Palette Test Read When read, the data in the location is the data of the Lower Panel Palette.
15-12	-	Reserved.
27-16	LPPalData	Lower Panel Palette Test Read When read, the data in the location is the data of the Lower Panel Palette.
31-28	-	Reserved

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1.21 Gray Scaler Test Write

If the Lower Panel Palette test read register is read, the data in this register is the data in the Lower Panel Palette at the corresponding address.

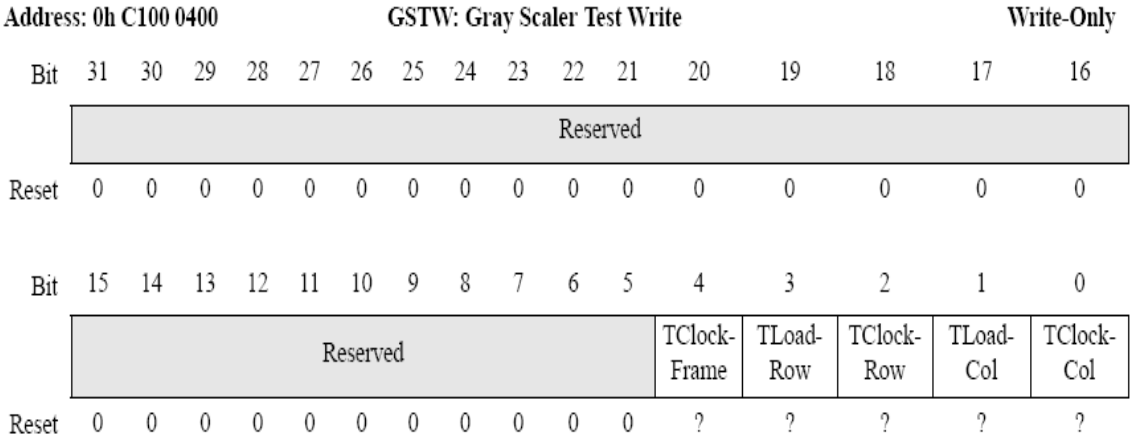

Figure 1-32 Lower Panel Palette Test Read register

Table 1-23 Lower Panel Palette Test Read register

Bit	Name	Description
0	TClockCol	Test Clock Gray Scaler Column 0 - Don't force the column in the Gray Scaler to be clocked 1 - Force the column in the Gray Scaler to be clocked
1	TLoadCol	Test Load Gray Scaler Column 0 - Don't force the column to be loaded 1 - Force the column to be loaded
2	TClockRow	Test Clock Gray Scaler Row 0 - Don't force the row in the Gray Scaler to be clocked 1 - Force the row in the Gray Scaler to be clocked

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Table 1-23 Lower Panel Palette Test Read register (continued)

Bit	Name	Description
3	TLoadRow	Test Load Gray Scaler Column 0 - Don't force the row to be loaded 1 - Force the row to be loaded
4	TClockFrame	Test Clock Gray Scaler Frame 0 - Don't force the frame in the Gray Scaler to be clocked 1 - Force the frame in the Gray Scaler to be clocked
31-5	-	Reserved

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1.22 LCD Controller Register Locations

Table 1-24 shows the registers associated with the LCD controller and the physical addresses used to access them.

Table 1-24 LCD register map locations

Name	Type	Description
0hC100 0000	LcdControl	LCD Control Register
0hC100 0004	LcdStatus	LCD Status Register
0hC100 0008	-	Reserved
0hC100 000C	-	Reserved
0hC100 0010	DBAR1	DMA Channel 1 Base Address Register
0hC100 0014	DCAR1	DMA Channel 1 Current Address Register
0hC100 0018	DBAR2	DMA Channel 2 Base Address Register
0hC100 001C	DBAR2	DMA Channel 2 Current Address Register
0hC100 0020	LcdTiming0	LCD Timing 0 Register
0hC100 0024	LcdTiming1	LCD Timing 1 Register
0hC100 0028	LcdTiming2	LCD Timing 2 Register
0hC100 0400	GSTW	Gray Scaler Test mode Write Register
0hC100 0404	GSTRDFA	Gray Scaler Test mode Read Frame Phase Accumulator Register
0hC100 0408	GSTRDRA	Gray Scaler Test mode Read Row Phase Accumulator Register
0hC100 040C	GSTRDCA	Gray Scaler Test mode Read Column Phase Accumulator Register
0hC100 0800–0hC100 0900	UPPTR	Upper Panel Palette Test Read Mapped Registers
0hC100 0C00–0hC100 0D00	LPPTR	Lower Panel Palette Test Read Mapped Registers

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