Joystick Interface Data Sheet

Data Sheet

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Release Information

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Chapter 1
Joystick interface

This chapter descibes the joystick interface.

1.1 About the Joystick Interface

The joystick interface is an AMBA slave module which connects to the *Advanced Peripheral Bus* (APB). For more information about AMBA, please refer to the *AMBA Specification* (ARM IHI 0001).

1.2 Features of the Joystick Interface

The joystick interface:

- has a 4-channel joystick controller
- requires minimal external RC passive components
- uses quad slope integration type A/D converters
- has software controllable integration cycle starts, and automatic hardware terminations
- has simple read access to conversion counters
- has a single external interrupt, with internal interrupt status register for source identification.

The following key features are programmable, allowing:

- combinations of channel interrupts that result in the final external interrupt via an interrupt control register
- individual control of the enable and disable of each of the four conversion counters via a converter control register
- independent control of the discharging of the external RC networks.

Additional test registers and modes are implemented to provide efficient testing.

Chapter 2
Joystick interface signals

This chapter details the joystick interface signals.

2.1 APB Signals

The joystick interface peripheral is connected to the APB bus as a slave. The table below describes the APB signals used.

Table 2-1 APB signal descriptions

Name	Type	Source/Destination	Description
BnRES	Input	Reset controller	System reset clock. Initiates a cold reset.
PA[5:2]	Input	APB bus	APB address signals; internal register map address source.
PD[15:0]	BiDir	APB bus	Driven by APB bridge during writes, by the peripheral during reads.
PSEL	Input	APB bus	APB slave select.
PSTB	Input	APB bus	APB strobe signal; times all APB bus transfers.
PWRITE	Input	APB bus	APB write/read input signal; defines access type. Write when HIGH, read when LOW.

2.2 Internal Signals

This table describes the internal signals.

Table 2-2 Internal signal descriptions

Name	Type	Source/Destination	Description
ATOD[3:0]	Input	Pads	Analogue comparator inputs.
ATODIref	Input	Pad	Comparator current reference.
ATODREF	Input	Pad	Common comparator voltage reference.
ATODVdd	Supply	Pad	Comparator analogue Vdd.
ATODVss	Supply	Pad	Comparator analogue ground.
CompOn	Output	Comparators	Common comparator current reference enable.
Joyint	Output	Interrupt controller	Joystick interrupt request.
Ndchg[3:0]	Output	Pads	ATOD[3:0] pad discharge control.
RefClk	Input	**REFCLK** Pad	Reference clock input signal, free running clock.
TestOut[3:0]	Output	Pads	Buffered comparator outputs.

Chapter 3
Functional description

This chapter describes how the joystick interface functions.

3.1 Block diagram

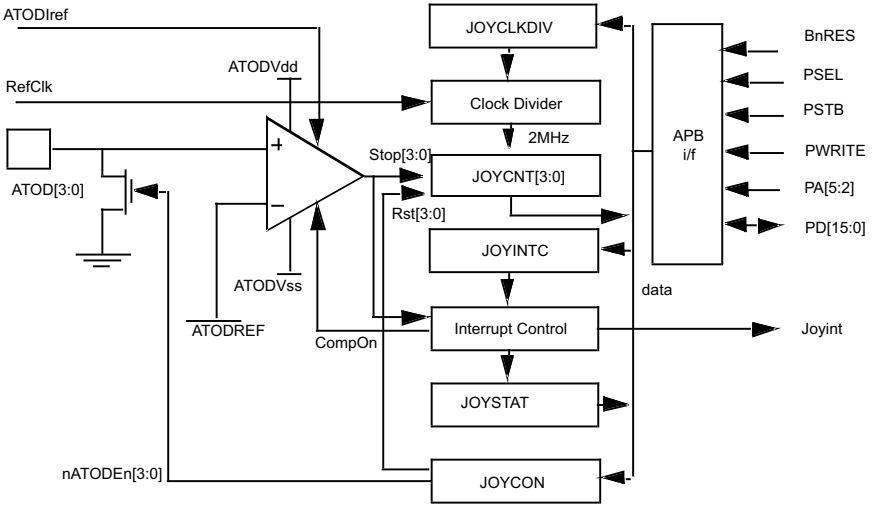

Figure 3-1 Joystick interface block diagram

3.2 How the Interface Works

The joystick interface is based on four identical analog-to-digital converters, each comprising an analog comparator and 16-bit counter pair.

Each converter is of the slope integration type, using an external RC network attached to the appropriate **ATOD[3:0]** pin to generate a variable ramp delay.

A16-bit counter measures the time taken for the voltage at the input to the comparator to reach the comparator's threshold. When the threshold is reached, the counter stops, and an internal "stop" flag for that channel is set. The value is held in the counter until it has been read, and the channel is then reset.

Discharge transistors on the analogue inputs are used to discharge the external capacitor, and to initiate a new integration cycle.

3.3 Analog Comparators

The comparators must be supplied with an appropriate reference bias current. All four comparators use the same **ATODREF** voltage source. The **ATODREF** input will be around half **ATODVdd**, at 1.5V.

When **ATOD[3:0]** voltage inputs rise above the voltage of the reference current, the digital output of the appropriate comparator stops the counters.

The **Ndchg[3:0]** signals can be used to force the **ATOD[3:0]** pins down to ground, thus discharging the external RC network which forms the analog-to-digital conversion circuit.

The reference current is controlled (enabled/disabled) by the **CompOn** signal.

Chapter 4
Programmer's model

This chapter describes the programmer's model.

4.1 Introduction

The base address of the joystick interface varies according to your system implementation. However, the offset of any register from the base address is fixed as defined in Table 4-1 on page 4-3 and *Test registers map* on page A-2.

Note

The locations at offsets +0x1C through +0x20 are reserved for test purposes and should not be used during normal operation.

4.2 Summary of Joystick Interface Registers

Table 4-1 Joystick interface registers

Offset	Type	Width	Reset Value	Name	Description
0x00	R/W	8	0x0F	JOYINTC	Joystick Interrupt Control Register
0x04	R/W	8	0x0	JOYSTAT	Joystick Status Register
0x08	R/W	8	0x00	JOYCON	Joystick A/D Converter Control Register
0x0C	R	16	0x00	JOYCNT1	Current Joystick Counter 1 Value
0x10	R	16	0x00	JOYCNT1	Current Joystick Counter 2 Value
0x14	R	16	0x00	JOYCNT1	Current Joystick Counter 3 Value
0x18	R	16	0x00	JOYCNT1	Current Joystick Counter 4 Value
0x1C	R/W	6	0x00	JOYCLKDIV	Reference Clock Divisor Value

4.3 Joystick Register Descriptions

JOYINTC [8] (+0x000) Joystick interrupt control register

The Interrupt Control register is provided so that various combinations of channels can generate the final interrupt.

There are four internal interrupt sources, one for each channel. Each channel attempts to raise its interrupt when the comparator threshold is reached and the "stop" flag is set internally. These interrupt sources can be individually enabled using the four LSBs of this register; the upper four bits determine which combination of channels will create the main interrupt output sent to the Interrupt Controller block.

Note that the OR of bits [3:0] is used to enable (power up) all the comparators. Thus they reset to the powered-up state.

Table 4-2 JOYINTC bit functions

Bit	Name	Function
7	**S**	Second pair of enables channels generates interrupt
6	**F**	First pair of enabled channels generates interrupt
5	**A**	Only all channels enabled generates interrupt
4	**C**	Any combination of channels generates interrupt
3	**chan4en**	Channel 4 interrupt enable
2	**chan3en**	Channel 3 interrupt enable
1	**chan2en**	Channel 2 interrupt enable
0	**chan1en**	Channel 1 interrupt enable

For all bits:

- Write0=disabled, 1=enabled
- Read current values are returned
- Reset set to 0F (individual channels enabled, all combinations off).

JOYSTAT [8] (+0x004) Joystick status register The status of the "stop" flags for each channel can be read from the Status register. From this, you can also derive each interrupt status; this is simply the logical AND of the "stop" flag and the corresponding enable bit from the Interrupt Control register.

Table 4-3 JOYSTAT bit functions

Bit	Name	Function
7:4	R[3:0]	Interrupt request state for channels 4 to 1
3:0	S[3:0]	Stop flags for channels 4 to 1

- Writeignored
- **Readbits**[7:4]: 0=not requesting,1=request active
- bits[3:0]: 0=not stopped, 1=stopped
- Resetset to 00 (ie. no requests/not stopped).

JOYCON [8] (+0x008) Joystick converter control The Converter Control register allows the discharge transistors and counters for each channel to be enabled/disabled, giving full control over counter resetting and the start time of a conversion cycle. Before a conversion can be started, the appropriate discharge bit and counter enable bit should be forced to 1 and 0 respectively, and then inverted, to initiate a conversion cycle. This allows the external capacitor to begin to ramp up, and the counters begin to increment simultaneously.

Table 4-4 JOYCON bit functions

Bit	Name	Function
7:4	**D**[3:0]	Discharge transistor control for channels 4 to 1(0 =transistor OFF, 1 = transistor ON)
3:0	**C**]3:0]	Clear counter for channels 4 to 1 (1 = enable, 0 = clear)

- **Writebit**[7:4]:0=transistor off; 1=transistor on (discharge). bit[3:0]:0=clear counter; 1=enable counter
- Readreturn above values
- Resetset all zero (clear counters and do not discharge)

JOYCNT1 [16] (+0x00C) Joystick counter 1 status

JOYCNT2 [16] (+0x010) Joystick counter 2 status .

JOYCNT3 [16] (+0x014) Joystick counter 3 status .

JOYCNT4 [16] (+0x018) Joystick counter 4 status

These read-only registers are used to read back the state of the relevant channel counter.

The counter outputs are not synchronized to bus timing for read back; the values should not be read until the relevant "stop" bits have been detected as set in the status register, as these indicate that the counter value is stable.

Table 4-5 JOYCNT[4:1] bit functions

Bit	Name	Function
15:0	**CNT**(n)	Counter output state

JOYCLKDIV [6] (+0x01C) Joystick reference clock divisor register

The **JOKCLKDIV** register is used to define the divide ratio required to generate a 2MHz Joystick clock from the **RefClk** input clock

Table 4-6 JOYCLKDIV register bit function

Bits	Name	Function
5:0	**DivVal**	Divide ValueThe RefClk division ration is given by the equation:divide ratio = 2 x DivVal

4.4 Interupts

The interrupt signal Joyint is available as an internal output signal from the peripheral.

The Joyint interrupt is asserted HIGH when the programmed channel, or combination of channels, raise their interrupt request lines as a consequence of the respective channels reaching the common comparator threshold voltage.

Internally, the respective counter is stopped, and is then available for reading.

For further information, refer to *Joystick Register Descriptions* on page 4-4.

Appendix A
Test Harness

This appendix describes the test harness.

A.1 Introduction

Extra registers are provided inside the Joystick Interface for test purposes only; they should not be accessed during normal mode of operation.

They are memory mapped as follows:

A.1.1 Summary of Joystick Interface Test Registers

The table below shows the memory mappings of the test registers.

Table A-1 Test registers map

Offset	Type	Width	Reset Value	Name	Description
0x1C	R/W	5	0x00	**JOYTEST1**	Joystick Test Register 1: Test clock control register.
0x20	R	6	0x10	**JOYTEST2**	Joystick Test Register 2: Primary output status register.
0x20	W	5	0x00	**JOYTEST3**	Joystick Test Register 3: Primary input control.

A.2 Test Register Descriptions

Functions can be controlled within test mode using registers provided in the Joystick module. These registers are intended for test purposes only, and should not be used in normal operational use. The test registers are:

- **JOYTEST1**: Joystick test register 1
- **JOYTEST2**: Joystick test register 2
- **JOYTEST3**: Joystick test register 3.

JOYTEST1 [5] (+0x020): Joystick test register 1

This register provides control over the clock source to the function while in test mode

Table A-2 JOYTEST1 bit functions

Bit	Name	Function
7-5	-	Not used.
4	**Stop**	Stop test clock. When set to 1, the strobe clock is stopped (gated out).
3	**T**	Test bit: enables counter test mode. When set, the four 16-bit counters are split into 4-bit parts, to shorten test times.
2:1	**C[1:0]**	Clock select bits X0Normal operation. The input clock is selected. 01PSEL ANDed with PSTB is driven as the internal clock. This means that when this clock source is selected, every access to the block generates a positive clock pulse internally. 11The RC bit is used as the clock. Therefore to generate an internal clock transition you have to program this bit with the last written value inverted (ie. write 0 and then 1 creates a LOW to HIGH transition and vice versa)
0	**RC**	Registered clock bit. Can be used as a clock source when selected as described above.

JOYTEST2 [6] (+0x024): Joystick test register 2

This read-only register stores the current values of the module output signals.

Table A-3 JOYTEST2 bit functions

Bit	Name	Function
7-6	-	Not used.
5	J	Returns current value of **JoyInt** interrupt flag.
4	**C**	Returns current value of **CompOn** output signal.
3:0	**S[3:0**]	Returns current values of comparator outputs.

JOYTEST3 [5] (+0x028): Joystick test register 3

his write-only test register provides control of the module input signals. The table below, Table A-4, shows the bit details of the register.

Table A-4 JOYTEST3 bit functions

Bit	Name	Function
7:1	**TESTS[3:0]**	Registered comparator input bits used in test mode.
0	SEL	Mux Select line for use in test mode. When set to 1, selects the TestS bits for use internally. Otherwise the normal block inputs are used.