AMBA Interrupt Controller

Data Sheet

ARM®

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AMBA Interrupt Controller
Data Sheet

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Contents
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Chapter 1
AMBA Interrupt Controller Data sheet

This datasheet provides information on the AMBA interrupt controller. It contains the following sections:

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1.1 Overview

The interrupt controller has:

- source status and interrupt request status
- separate enable set and enable clear registers to allow independent bit enable control of interrupt sources
- level-sensitive interrupts
- programmable interrupt source available.

Figure 1-1 shows the block diagram for the interrupt controller module.

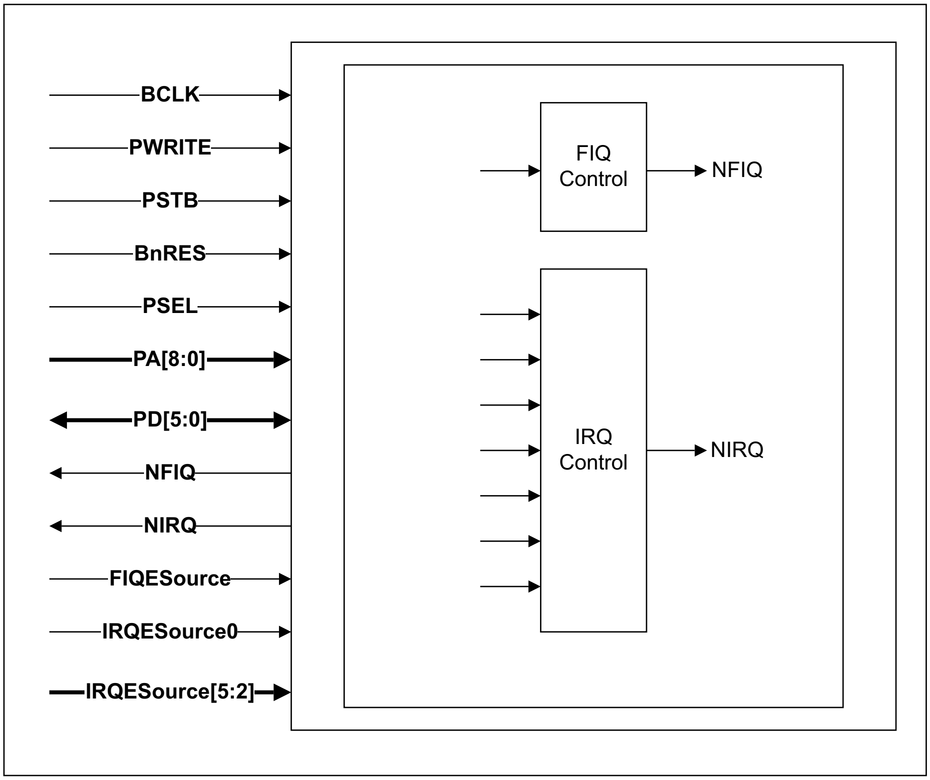

Figure 1-1 Interrupt Controller module block diagram

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1.2 Hardware interface and signal description

The Interrupt Controller module is connected to the APB bus. Table 1-1 shows the APB signals.

Table 1-1 APB signal descriptions

Name	Type	Source/destination	Description
BCLK	In	-	System (bus) clock. This clock times all bus transfers. The clock has two distinct phases. Phase 1 with **BCLK** LOW, and phase 2 with **BCLK** HIGH.
PA[8:0]	In	APB Bridge	This is the peripheral address bus, which is used by an individual peripheral for decoding register accesses to that peripheral. The addresses become valid before **PSTB** goes HIGH and remain valid after **PSTB** goes LOW.
PD[5:0]	InOut	APB peripherals, BD bus	This is the bidirectional peripheral data bus. The data bus is driven by this block during read cycles (when **PWRITE** is LOW).
PSTB	In	APB Bridge	This strobe signal is used to time all accesses on the peripheral bus. The falling edge of **PSTB** is coincident with the falling edge of **BCLK**.
PWRITE	In	APB Bridge	When HIGH, this signal indicates a write to a peripheral. When LOW, it indicates a read from a peripheral. This signal has the same timing as the peripheral address bus. It becomes valid before **PSTB** goes HIGH and remains valid after goes LOW.
PSEL	In	APB Bridge	When HIGH, this signal indicates that this module has been selected by the APB bridge. This selection is a decode of the system address bus (ASB). See *AMBA Peripheral Bus Controller*(ARM DDI - 0044) for more details.
FIQESource	In	APB peripherals/external world	**FIQ** interrupt signal into the Interrupt module. This active HIGH signal indicates that a Fast Interrupt Request has been generated.

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Table 1-1 APB signal descriptions (continued)

Name	Type	Source/destination	Description
IRQESource0 and **IRQESource[5:2]**	In	APB peripherals/external world	IRQ interrupt signals into the Interrupt module. These active HIGH signals indicate that interrupt requests have been generated (**IRQESource[1]** is internally generated in the Interrupt Controller module and is used to provide a software triggered IRQ).
NFIQ	Out	ARM Core	Active LOW **NFIQ** interrupt input to the ARM core.
NIRQ	Out	ARM Core	Active LOW **NIRQ** interrupt input to the ARM core.
BnRES	In	Reset Controller	Reset signal generated from the Reset Controller.

Writes to the Interrrupt Controller module are generated from the Peripheral Bus Controller module. Figure 1-2 summarizes this.

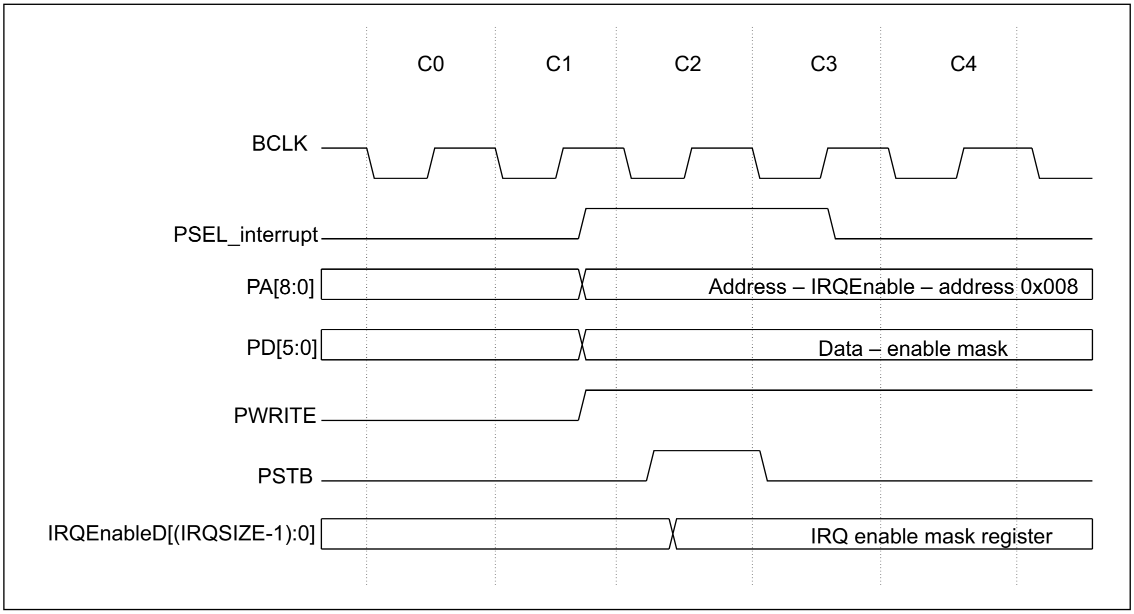

Figure 1-2 Interrupt control module APB write cycle

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1.3 Interrupt controller

The interrupt controller provides a simple software interface to the interrupt system. Certain interrupt bits are defined for the basic functionality required in any system, while the remaining bits are available for use by other devices in any particular implementation.

In an ARM system, two levels of interrupt are available:

- *Fast Interrupt Request* (FIQ) for fast, low latency interrupt handling
- *Interrupt Request* (IRQ) for more general interrupts.

Ideally, in an ARM system, only a single FIQ source would be in use at any particular time. This provides a true low-latency interrupt, because a single source ensures that the interrupt service routine may be executed directly without the need to determine the source of the interrupt. It also reduces the interrupt latency because the extra banked registers, which are available for FIQ interrupts, may be used to maximum efficiency by preventing the need for a context save.

Separate interrupt controllers are used for FIQ and IRQ. Only a single bit position is defined for FIQ, which is intended for use by a single interrupt source, while up to 32 bits are available in the IRQ controller. The standard configuration only makes six interrupt request lines available. This can be extended up to 32 sources by altering the IRQSize constant and increasing the width of PD

The IRQ interrupt controller uses a bit position for each different interrupt source. Bit positions are defined for a software programmed interrupt, a communications channel and counter-timers. Bit 0 is unassigned in the IRQ controller so that it may share the same interrupt source as the FIQ controller.

All interrupt source inputs must be active HIGH and level sensitive. Any inversion or latching required to provide edge sensitivity must be provided at the generating source of the interrupt.

No hardware priority scheme nor any form of interrupt vectoring is provided, because these functions can be provided in software.

A programmed interrupt register is also provided to generate an interrupt under software control. Typically this may be used to downgrade a FIQ interrupt to an IRQ interrupt.

1.3.1 Interrupt control

The interrupt controller provides interrupt source status, interrupt request status and an enable register. The enable register is used to determine whether or not an active interrupt source should generate an interrupt request to the processor.

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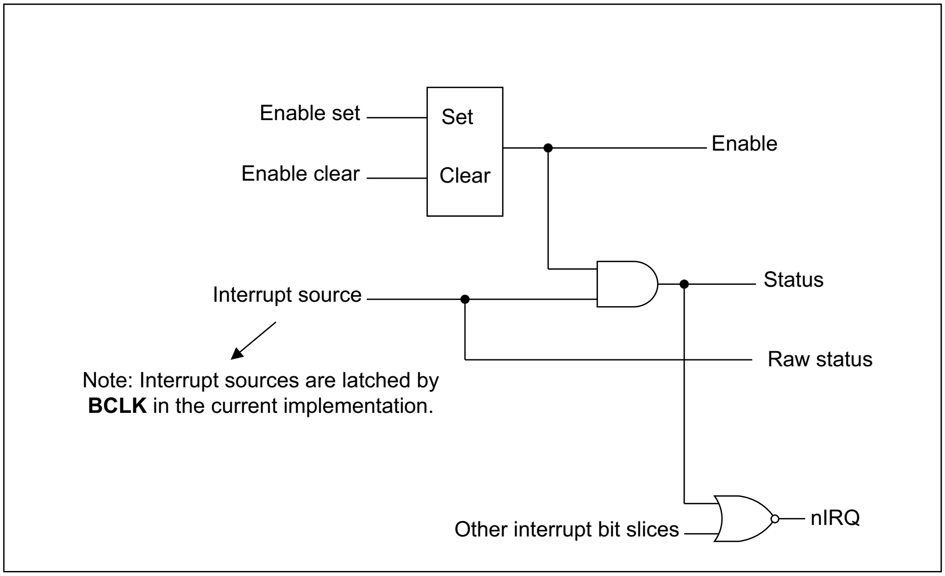
The interrupt source status indicates whether or not the appropriate interrupt source is active prior to masking and the interrupt request status indicates whether or not the interrupt source is causing a processor interrupt.

The enable register has a dual mechanism for setting and clearing the enable bits. This allows enable bits to be set or cleared independently, with no knowledge of the other bits in the enable register.

When writing to the enable set location, each data bit that is HIGH sets the corresponding bit in the enable register. All other bits of the enable register are unaffected. Conversely, the enable clear location is used to clear bits in the enable register while leaving other bits unaffected.

Figure 1-3 shows a single bit slice of the interrupt controller.

IRQ Interrupt Controller Bit Slice



Note: Interrupt sources are latched by **BCLK** in the current implementation.

Figure 1-3 Single bit slice of the interrupt controller

The FIQ interrupt controller consists of a single bit slice, located on bit 0. However, the IRQ controller will have a larger number of bit slices, where the exact size is dependent on the system implementation.

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1.4 Interrupt controller memory map

The base address of the interrupt controller is not fixed and may be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

Table 1-2 shows the memory map of the interrupt controller APB peripheral.

Table 1-2 Memory map of the interrupt controller APB peripheral

Address	Read location	Write location
IntBase + 0x000	IRQStatus	Reserved
IntBase + 0x004	IRQRawStatus	Reserved
IntBase + 0x008	IRQEnable	IRQEnableSet
IntBase + 0x00C	-	IRQEnableClear
IntBase + 0x010	-	IRQSoft
IntBase + 0x100	FIQStatus	Reserved
IntBase + 0x104	FIQRawStatus	Reserved
IntBase + 0x108	FIQEnable	FIQEnableSet
IntBase + 0x10C	-	FIQEnableClear
	Test registers	
IntBase + 0x014	IRQTestSource	IRQTestSource
IntBase + 0x018	IRQSourceSel	IRQSourceSel
IntBase + 0x114	FIQTestSource	FIQTestSource
IntBase + 0x118	FIQSourceSel	FIQSourceSel

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1.5 Interrupt controller register descriptions

The following registers are provided for both FIQ and IRQ interrupt controllers:

Enable Read-only. The enable register is used to mask the interrupt input sources and defines which active sources will generate an interrupt request to the processor. This register is read-only, and its value can only be changed by the enable set and enable clear locations. If certain bits within the interrupt controller are not implemented, the corresponding bits in the enable register must be read as undefined.

An enable bit value of 1 indicates that the interrupt is enabled and will allow an interrupt request to reach the processor. An enable bit value of 0 indicates that the interrupt is disabled. On reset, all interrupts are disabled.

Enable Set Write-only. This location is used to set bits in the interrupt enable register. When writing to this location, each data bit that is HIGH causes the corresponding bit in the enable register to be set. Data bits that are LOW have no effect on the corresponding bit in the enable register.

Enable Clear Write-only. This location is used to clear bits in the interrupt enable register. When writing to this register, each data bit that is HIGH causes the corresponding bit in the enable register to be cleared. Data bits that are LOW have no effect on the corresponding bit in the interrupt enable register.

Raw Status Read-only. This location provides the status of the interrupt sources to the interrupt controller. A HIGH bit indicates that the appropriate interrupt request is active prior to masking.

Status Read-only. This location provides the status of the interrupt sources after masking. A HIGH bit indicates that the interrupt is active and will generate an interrupt to the processor.

The following register is also provided:

Programmed IRQ Interrupt

Write only. A write to bit 1 of this register sets or clears a programmed interrupt. Writing to this register with bit 1 set HIGH generates a programmed interrupt, while writing to it with bit 1 set LOW clears the programmed interrupt. The value of this register may be determined by reading bit 1 of the Source Status register. Bit 0 of this register is not used.

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1.6 Interrupt registers standard configuration

The FIQ interrupt controller is one bit wide and is located on bit 0. The source of this interrupt is implementation dependent

The interrupt controller will be customized to fit into each application. The following is a minimum set of interrupt bits assigned in a system.

IRQ register Bits 1 to 5 in the IRQ interrupt controller are defined. Bit 0 and Bits 6 up to 31 are available for use as required. Bit 0 is left available so that the FIQ source may also be routed to the IRQ controller in an identical bit position.

Table 1-3 shows an example of IRQ sources.

Table 1-3 Example of IRQ sources

Bit	Interrupt source
0	-
1	Programmed interrupt
2	Comms Rx
3	Comms Tx
4	Timer 1
5	Timer 2

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1.7 Test registers

Four extra registers are defined to facilitate testing of the interrupt controller module using the AMBA test methodology:

IRQTestSource Same size as IRQRawStatus

IRQSourceSel 1-bit wide (bit 0). When set, the value in IRQTestSource is multiplexed into IRQRawStatus

FIQTestSource Same size as FIQRawStatus

FIQSourceSel 1-bit wide (bit 0). When set, the value in FIQTestSource is multiplexed into FIQRawStatus

These four registers are all read-write registers. They must not be accessed during normal operation.

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