AMBA Arbiter

Data Sheet

ARM®

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Data Sheet

Release Information

The following changes have been made to this document.

Change History

Date	Issue	Confidentiality	Change
October 1995	A-01	Non-Confidential	Created
December 1995	A-02	Non-Confidential	Signal and Description Update
January 1996	B	Non-Confidential	Edited for style and content
April 1997	C	Non-Confidential	Minor edits

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The following sections provide information on the function of the AMBA bus arbiter.

1.1 Overview

The AMBA bus specification is a multi-master bus standard. As a result, a bus arbiter is needed to ensure that only one bus master has access to the bus at any particular point in time. Each bus master can request the bus; the Arbiter decides which has the highest priority and issues a grant signal accordingly.

Every system must have a default bus master which is granted use of the bus during reset, when no other bus master requires the bus.

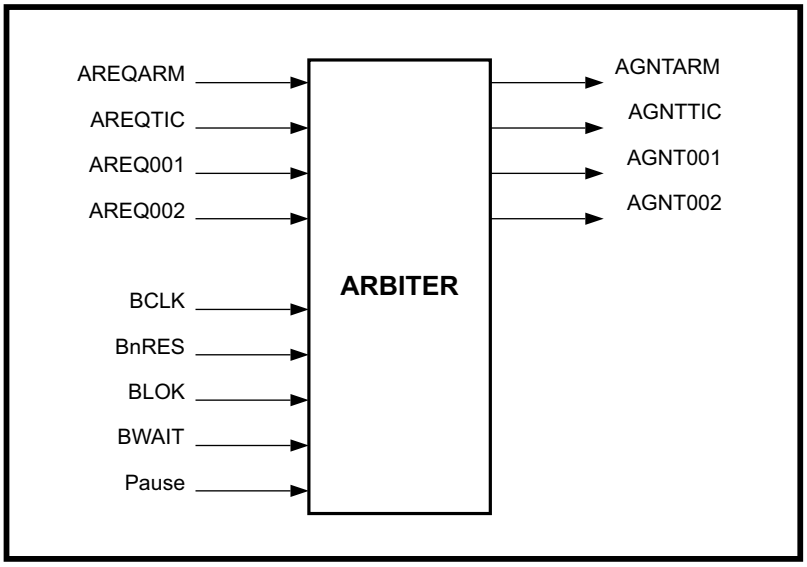

Figure 1-1 Arbiter block diagram

1.2 Signal Description

Table 1-1 Signal descriptions

Name	Type	Description
AGNTARM	Out	Grant signal to the ARM processor. When HIGH, this signal indicates that the ARM bus master is currently the highest priority master requesting the bus. This signal changes during the LOW phase of **BCLK** and remains valid through the HIGH phase.
AGNTTIC	Out	Grant signal to the test interface controller. When HIGH this signal indicates that the test interface controller is currently the highest priority master requesting the bus. This signal changes during the LOW phase of **BCLK** and remains valid through the HIGH phase.
AGNT001	Out	Grant signal to bus master 001. When HIGH, this signal indicates that this bus master is currently the highest priority master requesting the bus. This signal changes during the LOW phase of **BCLK** and remains valid through the HIGH phase.
AGNT002	Out	Grant signal to bus master 002. When HIGH this signal indicates that this bus master is currently the highest priority master requesting the bus. This signal changes during the LOW phase of **BCLK** and remains valid through the HIGH phase.
AREQARM	In	Request from the ARM processor indicating that it requires the bus. This signal must be set up to the falling edge of **BCLK**.
AREQTIC	In	Request from the test interface controller indicating that it requires the bus. This signal must be set up to the falling edge of **BCLK**.
AREQ001	In	Request from a bus master 001 indicating that the master requires the bus. This signal must be set up to the falling edge of **BCLK**.
AREQ002	In	Request from a bus master 002 indicating that the master requires the bus. This signal must be set up to the falling edge of **BCLK**.
BCLK	In	System (bus) clock. This clock times all bus transfers. The clock has two distinct phases: phase 1 in which **BCLK** is LOW, and phase 2 in which **BCLK** is HIGH.
BnRES	In	This signal is active LOW and indicates the reset status of the bus. It is driven by the reset controller.
BLOK	In	A shared bus lock signal driven by the currently granted bus master is used to indicate that the current transfer is indivisible from the following transfer, and that no other master should be granted the bus.

Table 1-1 Signal descriptions (continued)

Name	Type	Description
BWAIT	In	This signal is driven by the selected bus slave to indicate whether the current transfer may complete. If **BWAIT** is HIGH, a further bus cycle is required. If **BWAIT** is LOW, the transfer may complete in the current bus cycle. When no bus transfer is taking place, this signal is driven by the bus decoder. This signal is driven in the LOW phase of **BCLK** and is valid before the rising edge of **BCLK**. **BWAIT** is used by the arbiter block to determine when a turnaround cycle is happening on the bus.
Pause	In	This signal allows the processor system to enter a low-power, wait for interrupt state, when the system does not require the processor to be active.

Note

In systems that only have the ARM and the Test Interface Controller as potential bus masters, the unused **AREQxxx** lines must be tied LOW.

1.3 Signal Timing

The arbitration signal timing is shown in Figure 1-2 below.

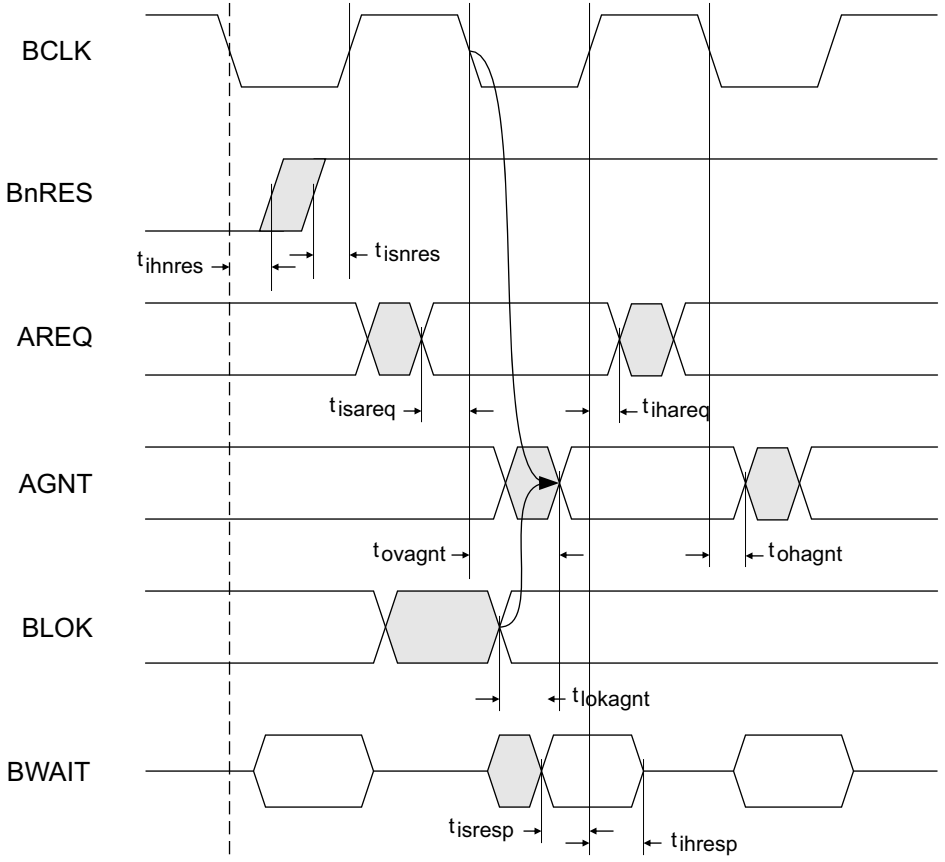

Figure 1-2 Arbitration timing

Note that the arbiter produces grant signals on a cycle-by-cycle basis, showing which bus master currently has the highest priority. However, the bus mastership does not change every cycle, and a new bus master is only granted when:

- **AGNT** is HIGH, indicating that the bus master is currently the highest priority, and
- **BWAIT** is LOW, indicating that the current transfer has completed.

Each bus master is responsible for monitoring these signals to determine when it is granted use of the bus.

1.4 Arbitration Priorities

During reset, when **BnRES** is LOW, the arbiter grants use of the bus to the default bus master, and holds all other grant signals inactive.

The following arbitration priorities are implemented:

Highest	Test Interface Controller
	Bus master 1
	Bus master 2
Lowest	ARM Processor

The default bus master—that is, the test interface controller—is granted use of the bus during standby, as indicated by **Pause** being HIGH, and when no other master is requesting the bus.

BWAIT is used by the arbiter to determine when a turnaround cycle is happening. On a turnaround cycle, when a new grant has occured on the previous cycle **BLOK** will not be valid on time, and hence should not be sampled.