ARM® CoreLink™ NIC-450 Network Interconnect

Revision: r0p0

Technical Overview

ARM®

ARM® CoreLink™ NIC-450 Network Interconnect

Technical Overview

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Release Information

Document History

Issue	Date	Confidentiality	Change
0000-00	04 March 2016	Non-Confidential	First release for r0p0
0000-01	22 July 2016	Non-Confidential	Second release for r0p0

Unrestricted Access is an ARM internal classification.

Product Status

The information in this document is Final, that is for a developed product.

Web Address

http://www.arm.com

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ARM® CoreLink™ NIC-450 Network Interconnect Technical Overview

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Preface

This preface introduces the *ARM® CoreLink™ NIC-450 Network Interconnect Technical Overview*.

It contains the following:
- *About this book* on page 7.
- *Feedback* on page 9.

About this book

This book is for the ARM® CoreLink™ NIC-450 Network Interconnect.

Product revision status

The r*mpn* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m*   Identifies the major revision of the product, for example, r1.

p*n*   Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the NIC-450 Network Interconnect.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
> Use the following information for an overview of the ARM CoreLink NIC-450 Network Interconnect and how you can use it in SoC design.

Chapter 2 NIC-450 Components
> Use the following information as a reference for the individual components that are contained in the CoreLink NIC-450 Network Interconnect library.

Chapter 3 System IP Tooling
> The following information describes the different ARM System IP Tooling options that you can use to enable the configuration and integration of System IP.

Appendix A Revisions
> This appendix describes the changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

italic
> Introduces special terminology, denotes cross-references, and citations.

bold
> Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
> Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

<u>`mono`</u>`space`
> Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
> Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
> Denotes language keywords when used outside example code.

`<and>`

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Additional reading

This section lists publications by ARM and by third parties.

See *Infocenter* for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DDI 0475).
- *ARM® CoreLink™ QoS-400 Network Interconnect Advanced Quality of Service Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0026).
- *ARM® CoreLink™ QVN-400 Network Interconnect Advanced QoS for Virtual Networks Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0027).
- *ARM® CoreLink™ TLX-400 Network Interconnect Thin Links Supplement to ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (ARM DSU 0028).
- *ARM® CoreLink™ AXI4 to AHB-Lite XHB-400 Bridge Technical Reference Manual* (ARM DDI 0523).
- *ARM® CoreLink™ LPD-500 Low Power Distributor Technical Reference Manual* (ARM 100361).
- *ARM® AMBA® Designer ADR-400 User Guide* (ARM DUI 0333).

The following confidential books are only available to licensees:

- *ARM® CoreLink™ NIC-450 Network Interconnect Release Note* (ARM EPM 099098).
- *ARM® CoreLink™ NIC-400 Network Interconnect Integration Manual* (ARM DII 0269).
- *ARM® CoreLink™ NIC-400 Network Interconnect Implementation Guide* (ARM DII 0273).
- *ARM® CoreLink™ NIC-400 Network Interconnect Supplement to ARM® AMBA® Designer ADR-400 User Guide* (ARM DSU 0018).
- *ARM® CoreLink™ ADB-400 AMBA Domain Bridge User Guide* (ARM DUI 0615).
- *ARM® CoreLink™ Creator User Guide* (ARM 100447).

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *ARM CoreLink NIC-450 Network Interconnect Technical Overview*.
- The number ARM 100459_0000_01_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

───────── **Note** ─────────

ARM tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

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Chapter 1
Introduction

Use the following information for an overview of the ARM CoreLink NIC-450 Network Interconnect and how you can use it in SoC design.

It contains the following sections:
- *1.1 About the CoreLink NIC-450 Network Interconnect* on page 1-11.
- *1.2 Product documentation* on page 1-12.

1.1   About the CoreLink NIC-450 Network Interconnect

The ARM CoreLink NIC-450 Network Interconnect is a library of highly configurable and multi-power domain tools.

The CoreLink NIC-450 Network Interconnect is a bundle of key interconnect IP that enables you to build a scalable and configurable network interconnect. You can integrate the NIC-400 with the ADB-400 AMBA Domain Bridge or TLX-400 Network Interconnect Thin Links bridges into a single interconnect. The NIC-450 also includes:

- CoreLink LPD-500 Low Power Distributor.
- CoreLink AXI4 to AHB-Lite XHB-400 Bridge.
- CoreLink QoS-400 Network Interconnect Advanced Quality of Service.
- CoreLink QVN-400 Advanced Quality of Service for Virtual Networks.

You can utilize the high level of configurability of NIC-450 for optimization and tuning.

The benefits of using the NIC-450 are:
- Unified low-power interfaces when applicable.
- Single design environment to configure IP blocks and connect them together.

Use the NIC-450 with CoreLink Creator, a tool that employs algorithms to aid the creation of valid configurations that are based on your specific design requirements.
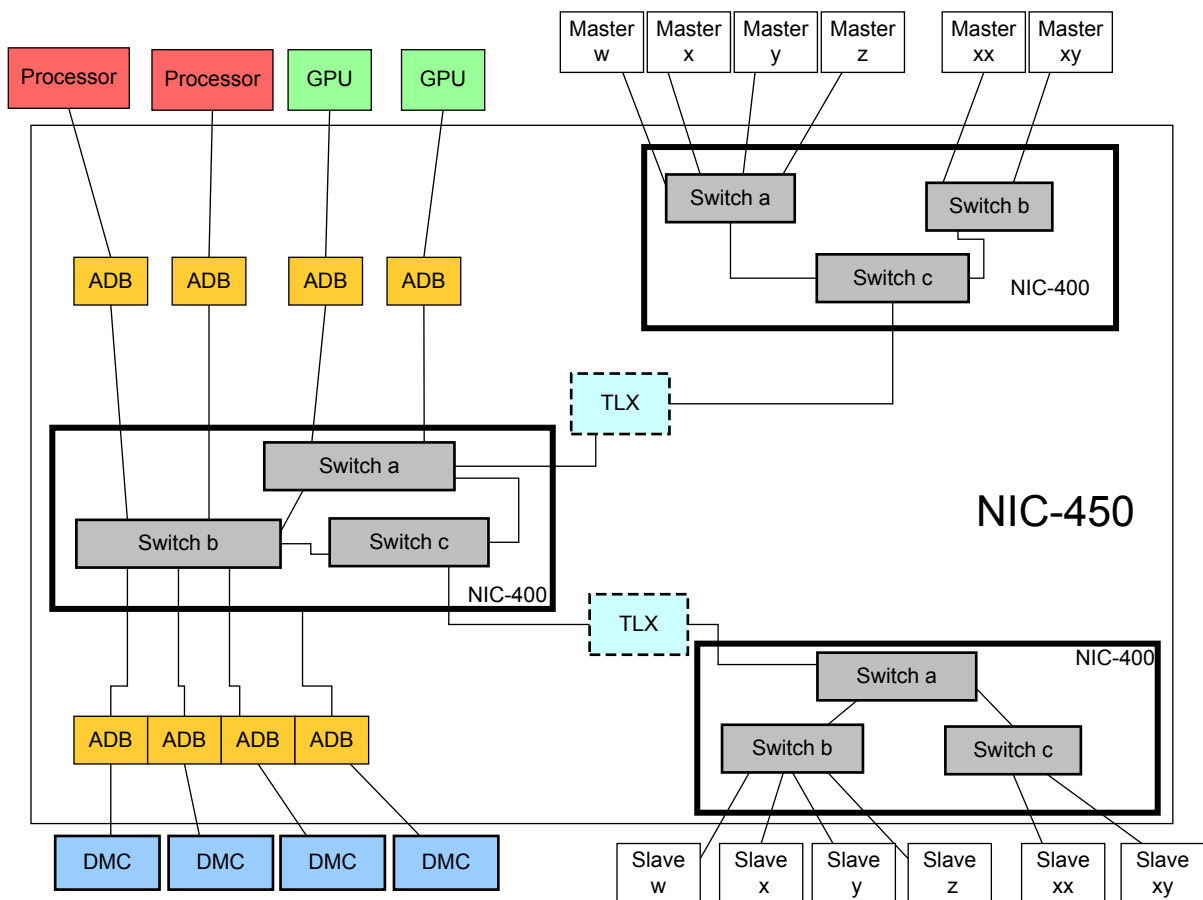
Figure 1-1 NIC-450 block diagram

1.2 Product documentation

This section describes the documentation of the CoreLink NIC-450 Network Interconnect.

Documentation

The NIC-450 documentation is as follows:

Technical Overview

The *Technical Overview* (TO) summarizes the functionality of the CoreLink NIC-450 Network Interconnect and describes the library of components that make up the NIC-450 product.

Chapter 2
NIC-450 Components

Use the following information as a reference for the individual components that are contained in the CoreLink NIC-450 Network Interconnect library.

It contains the following sections:

2.1 NIC-400 Network Interconnect

The CoreLink NIC-400 Network Interconnect is a cascading, routing interconnect component. The NIC-400 is a hierarchical, low latency and low-power connection for various other components.

You can use the NIC-400 to create a complete high performance, optimized, and AMBA-compliant network infrastructure because it is highly configurable. The possible configurations for the NIC-400 can range from a single bridge component, to a complex interconnect. For example, from an AHB to AXI protocol conversion bridge, to a complex interconnect that consists of up to 128 masters and 64 slaves of AMBA protocols.

——————— **Note** ———————

The NIC-400 does not bridge power, voltage, or geographic domains.

The NIC-400 configuration can consist of multiple switches with many topology options. The following diagram shows a top-level block diagram of the NIC-400 that contains multiple:
- Switches.
- *AMBA Slave Interface Blocks* (ASIBs).
- *AMBA Master Interface Blocks* (AMIBs).
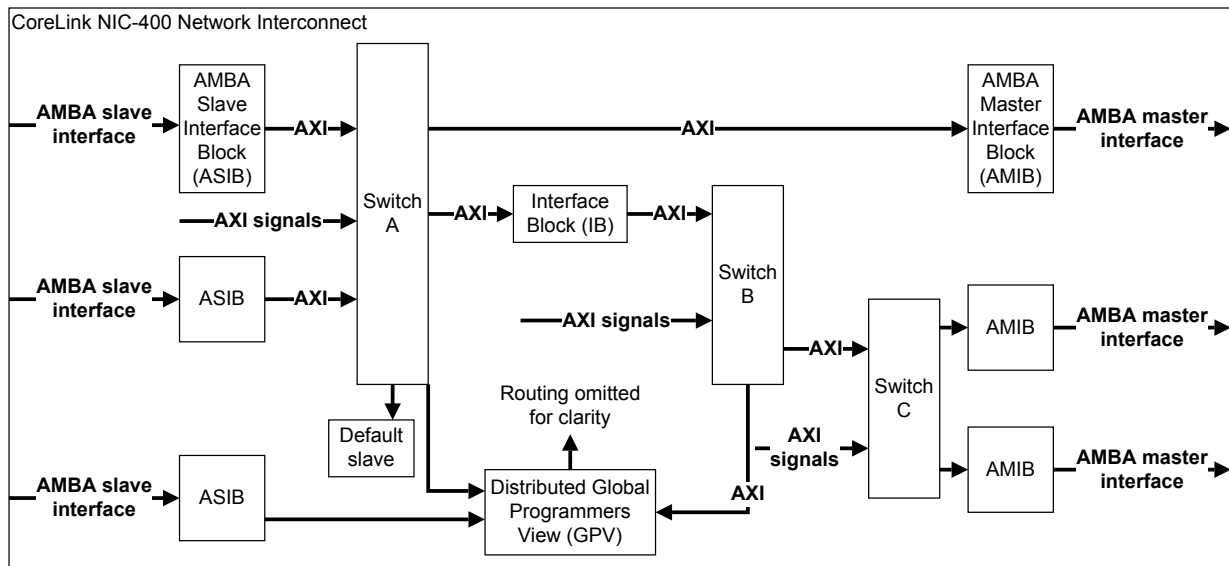
Figure 2-1 NIC-400 top-level block diagram

2.1.1 NIC-400 key features

The CoreLink NIC-400 Network Interconnect has many features to support interfaces, gates, and other components to make up your SoC.

The NIC-400 supports:
- 1-128 slave interfaces that can be:
  — AXI3.
  — AXI4.
  — AHB-Lite slave interface.
  — AHB-Lite mirrored master interface.
- 1-64 master interfaces that can be:
  — AXI3.
  — AXI4.
  — AHB-Lite master interface.

- — AHB-Lite mirrored slave interface.
- — APB2.
- — APB3.
- — APB4.
- Hierarchical clock-gating.
- The configuration of an:
  - — APB AMIB that can have up to 16 subports. Each subport can be APB2, APB3, or APB4.
  - — AXI port to support four region control bits.
  - — AXI port to support *Quality of Service* (QoS) signaling.
- Single-cycle arbitration.
- Full pipelining to prevent master stalls.
- Programmable control for FIFO transaction release.
- Multiple switch networks.
- Complex topologies, including *Network on Chip* (NOC) loop-back connections between switches.
- 1-5 cascaded switch networks between any master and slave interface pair.
- AXI or AHB-Lite masters and slaves with:
  - — An address width of 32-64 bits.
  - — A data width of 32, 64, 128, or 256 bits.
- Non-contiguous APB slave address map for a single master interface.
- Independent widths of user-defined sideband signals for each channel.
- *Global Programmers View* (GPV) for the entire interconnect that you can configure so that any master, or a discrete configuration slave interface, can access it.
- Highly flexible timing closure options.
- Hierarchical clock-gating to reduce idle or near idle power.
- QoS, using the ARM CoreLink QoS-400 product.
- *Virtual Networks* (VN) using the ARM CoreLink QVN-400 Network Interconnect Advanced *Quality of Service for Virtual Networks* (QVN) product.

Related information

ARM® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual.

2.2 QoS-400 Network Interconnect Advanced Quality of Service

The ARM CoreLink QoS-400 Network Interconnect Advanced Quality of Service is an optional extension to the CoreLink NIC-400 Network Interconnect product.

The QoS-400 provides programmable QoS facilities for any attached masters. See *2.1 NIC-400 Network Interconnect* on page 2-14 for a block diagram showing a CoreLink NIC-400 Network Interconnect design with QoS-400 regulators.

2.2.1 QoS-400 key features

The CoreLink QoS-400 Network Interconnect Advanced Quality of Service has specific features that you can utilize when used in a NIC-400 Network Interconnect SoC.

The main features are:
- Programmable maxima for read and write requests:
  — Separate maxima for read and write requests.
  — Combined maxima for all requests.
  — Fractional value to provide finer control.
- Regulation of read and write request-issuing rates to meet programmed traffic specifications:
  — Separate regulation for read and write requests.
  — Combined regulation for all requests.
- Regulation of read and write request QoS values to target a programmed transaction latency.
- Regulation of read and write request QoS values to target a programmed address request latency, so the targeted latency indirectly sets the period.
- Low gate count:
  — You can configure the QoS facilities individually for each ASIB and IB.
  — Efficient measurement of transaction latency.
- Low power consumption. QoS-400 consumes no dynamic power, except clock power, when the regulators are disabled.
- No cycles of latency added to requests when inactive.

Related information

ARM® CoreLink™ QoS-400 Network Interconnect Advanced QoS Supplement.

2.3 QVN-400 Network Interconnect Advanced QoS for Virtual Networks

The CoreLink QVN-400 Network Interconnect Advanced QoS for Virtual Networks is an optional extension to the CoreLink NIC-400 Network Interconnect product.

The QVN-400 extension provides a mechanism to avoid head-of-line blocking and cross-path blocking between different data flows. Use the QVN-400 mechanism to allocate buffer space to different virtual channels in the interconnect and the *Dynamic Memory Controller* (DMC) in the SoC.

2.3.1 QVN-400 key features

The CoreLink QVN-400 Network Interconnect Advanced QoS for Virtual Networks has specific key features that you can utilize when used in a NIC-400 Network Interconnect SoC.

The key features are:
- The QVN-400 helps to prevent congestion between traffic flows in the system by enabling the system designer to separate masters with conflicting requirements onto different virtual networks. For example, high-bandwidth bus traffic sources can be separated to prevent blocking of the flow of latency-critical bus traffic.
- The QVN-400 works over interconnects that are configured as AXI3 and AXI4.
- The QVN-400 works with other optional, licensable features, such as the QoS-400 and TLX-400.
- You can configure up to eight virtual networks, by assigning them to addressable paths between masters and slaves.
- You can configure a maximum of four virtual networks on any single master or slave interface.
- You can configure a maximum of four virtual networks on any single connection between master and slaves interfaces within the NIC.
- You can configure the virtual network token request mechanism to be exported with the master and slave interfaces.
- You can configure slave and master interfaces for lower latency by pre-allocating tokens.
- You can dynamically change a low priority threshold to exclude low priority transactions from arbitration when terminating more than one virtual network in a master interface.

Related information

ARM® CoreLink™ QVN-400 Network Interconnect Advanced QoS using Virtual Networks Supplement.

2.4 TLX-400 Network Interconnect Thin Links

CoreLink TLX-400 Network Interconnect Thin Links is an optional extension to the CoreLink NIC-400 Network Interconnect product.

TLX-400 provides a mechanism to reduce the number of signals in an AXI point-to-point connection. The TLX-400 also enables the base product to be routed over a longer distance.

——————— Note ———————

Thin Links are used to cross geographic domains but an *AMBA Domain Bridge* is required to cross between voltage domains.

———————————————

2.4.1 TLX-400 key features

There are several features that you can utilize when you use CoreLink TLX-400 Network Interconnect Thin Links as part of a SoC with NIC-400.

The features are:
- Thin Links reduce routing congestion and aids timing closure of point-to-point connections. These connections are implemented as forward and reverse links. Each link can be independently configured to reduce the number of wires that the connection requires.
- Thin Links support clock domain crossing to aid physical implementation. This implementation means that the end points of the TLX are always specified to be in a different clock domain. The relationship of the clocks must be defined as asynchronous.
- Thin Links can incorporate other NIC-400 functions. For example:
  — A connection between components of different data widths.
  — A connection between components of different protocols.
- Thin Links can be used with the QoS-400 Network Interconnect Advanced Quality of Service.
- Thin Links can be used with QVN-400 Advanced Quality of Service for Virtual Networks.

Related information

ARM® CoreLink™ TLX-400 Thin Links Supplement.

ARM® CoreLink™ QoS-400 Network Interconnect Advanced QoS Supplement.

ARM® CoreLink™ QVN-400 Network Interconnect Advanced Quality of Services using Virtual Network Supplement.

2.5 AXI4 to AHB-Lite XHB-400 Bridge

You can use the CoreLink AXI4 to AHB-Lite XHB-400 Bridge as an optional extension with the NIC-400 Network Interconnect product.

Use the XHB-400 to convert AXI4 protocol to AHB-Lite protocol. The XHB-400 also has an AXI4 slave interface and an AHB-Lite master interface. The interfaces are as follows:

- AXI4-slave interface. This interface connects to either the AXI4 master interface of a processor, or to an AXI interconnect.
- AHB-Lite master interface. This interface implements an AHB-Lite master to drive AHB-Lite subsystems.

2.5.1 XHB-400 key features

The CoreLink AXI4 to AHB-Lite XHB-400 Bridge has several features that you can utilize in a NIC-400 Network Interconnect SoC.

The key features are:

- Full support of the AXI4 protocol.
- Efficient conversion of the AXI4 transactions to AHB-Lite.
- Conversion of sparse write transactions to AHB-Lite.
- Read acceptance capability is two transactions.
- Write acceptance capability is two transactions.
- Combined acceptance capability is four transactions.
- Configurable data width options.
- Zero latency conversion to AHB-Lite.
- Two entry FIFOs for buffering read data and write response channels.
- Processor performance is improved by prioritizing read transactions over write transactions, when AXI read and write address channels are valid in the same cycle. Also read transactions might interrupt sparse write transactions. Write transactions are guaranteed to be accepted for every one in eight transactions, when back-to-back read transactions occur.
- Support of exclusive accesses on the AHB-Lite interface using the **EXREQ** and **EXRESP** signals.

Related information

ARM® CoreLink™ AXI4 to AHB-Lite XHB-400 Bridge Technical Reference Manual.

2.6 ADB-400 AMBA Domain Bridge

The CoreLink ADB-400 AMBA Domain Bridge is an asynchronous bridge between two components or systems that can be in a different power, clock, or voltage domains.

The ADB-400 supports:

- An optional configurable destination register for the payload of each channel.
- Simple reset requirements.
- A power management interface.
- *Dynamic Voltage and Frequency Scaling* (DVFS).
- *Quality of Service (QoS) Virtual Network* (QVN).
- Clock status indication.

The ADB-400 consists of a slave domain and a master domain. The slave domain received transfers from the AMBA master and the master domain transmits transfers to an AMBA slave.

——————— **Note** ———————

The ADB-400 does not perform protocol translation, or bridge geographic domains.

2.6.1 ADB-400 key features

The CoreLink ADB-400 AMBA Domain Bridge has different features depending on how it is being utilized.

You can use the ADB-400 AMBA Domain Bridge as two different types of bridges:

- A *Dynamic Voltage Frequency Scaling* (DVFS) bridge. The ADB slave and master domains must be in different voltage domains.
- A clock bridge. This bridge type requires the master and slave domains to be in the same voltage domain.

The following properties of the ADB-400 are configurable:
- Address widths.
- Data widths.
- ID widths.
- User signal widths.
- FIFO depths.
- Presence or absence of output registers on channels that have payload.
- Number of stages in the synchronizers in the ADB master domain.
- Number of stages in the synchronizers in the ADB slave domain.
- Presence or absence of powerdown functionality for AXI4-Stream bridges only.

For more information about these configurable options and how to change the values, see the *ARM® CoreLink™ ADB-400 AMBA® Domain Bridge User Guide*.

2.7 LPD-500 Low Power Distributor

The CoreLink LPD-500 Low Power Distributor is a standalone configurable component to distribute Q-Channel interfaces to multiple devices and subsystems.

The LPD-500 uses Q-Channels to manage quiescence in components of the system that allow the clock to be gated off or power to be removed. Therefore, managing quiescence saves power when the system is not operational.

2.7.1 LPD-500 key features

The CoreLink LPD-500 Low Power Distributor provides a low latency method of controlling multiple, device-level, *Low Power Interfaces* (LPIs) from a single controller. There are several features you can utilize in LPD-500 when it is used in a NIC-400 SoC.

The LPD-500 supports the following key features:

- Expands a single Q-Channel LPI from a power controller or a clock controller into multiple Q-Channel LPIs for controlled devices.
- Low latency to and from device channels.
- Up to 32 device control channels.
- Cascadable to multiple levels to expand beyond 32 devices.
- Optionally integrates synchronizers on request and accepts inputs for use in systems with different clock domains.
- Configurable as an expander, where all devices are controlled together, or as a sequencer, where all devices are controlled in a sequence.
- Optional active deny feature to allow denial of quiescence that is based on a device **QACTIVE** signal.

Related information

ARM® CoreLink™ LPD-500 Low Power Distributor Technical Reference Manual.

Chapter 3
System IP Tooling

The following information describes the different ARM System IP Tooling options that you can use to enable the configuration and integration of System IP.

There are two System IP Tools to configure CoreLink NIC-450 Network Interconnect IP. These tools are:
- CoreLink Creator.
- AMBA Designer.

It contains the following sections:

3.1 CoreLink Creator

This section provides an overview of CoreLink Creator.

You must use CoreLink Creator version 16.1 or later for the configuration of CoreLink NIC-450 Network Interconnect IP.

——————— **Note** ———————

CoreLink Creator is separately licensed and is not included in the NIC-450 product.

3.1.1 About CoreLink Creator

CoreLink Creator is a license-only application of Socrates™ IP tooling. Use CoreLink Creator to configure and integrate the component IP of the CoreLink NIC-450 Network Interconnect product.

Use CoreLink Creator to guide you through the configuration and integration of CoreLink System IP. You can utilize the rules-based design methodology and IP-XACT specification in CoreLink Creator to generate the IP components, combine them, and generate the IP-XACT and Verilog RTL descriptions of your SoC. You can quickly work out the best working SoC by repeating and refining your design, then check for validity and correctness at every stage using *Design Rule Checks* (DRCs). The following figure shows the CoreLink Creator workflow.
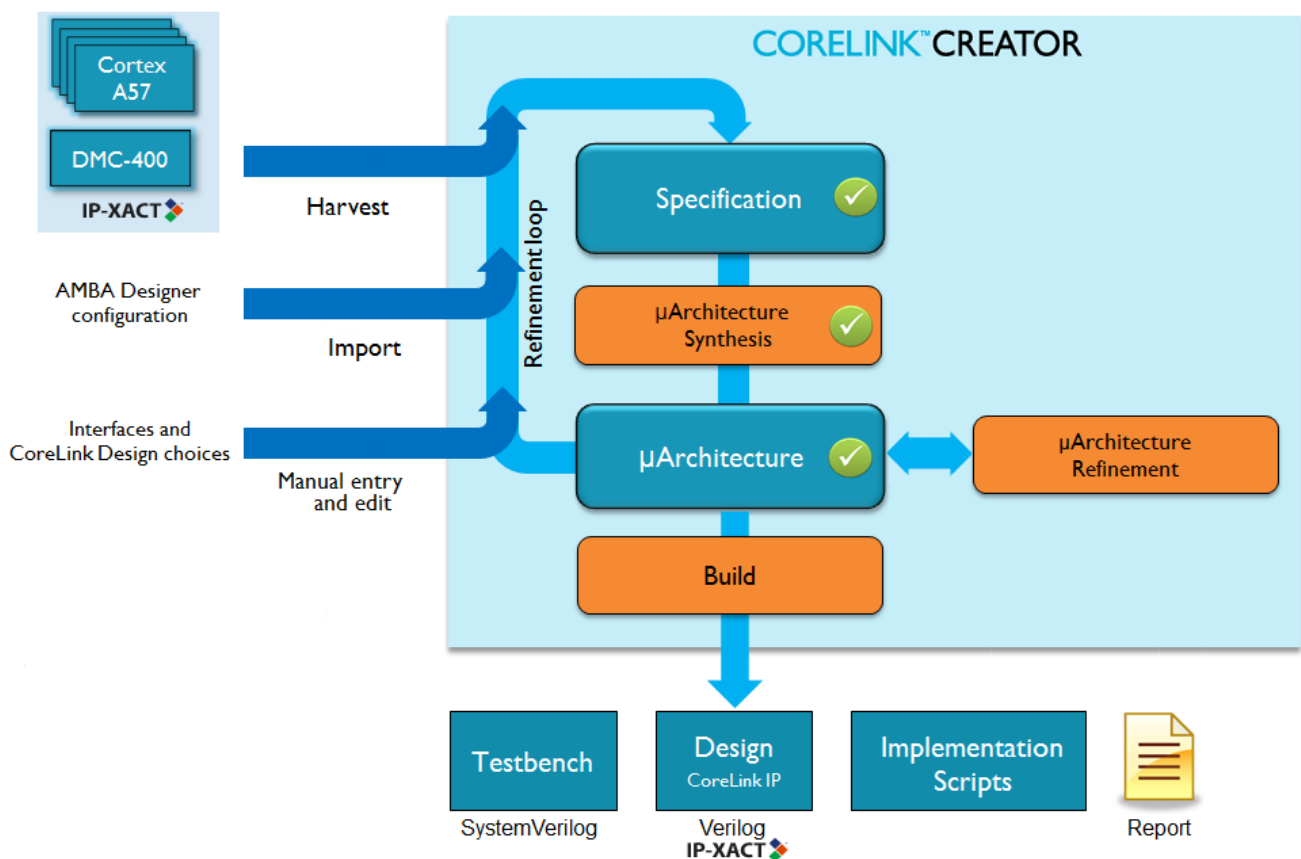
Figure 3-1 CoreLink Creator Workflow

CoreLink Creator allows you to manually change NIC-450 IP components and the individual NIC-400 microarchitectures, leading to flexible, and highly configurable designs. When you use CoreLink Creator with NIC-450, you can generate a CoreLink System IP component that you can then integrate into a larger system design.

3.1.2 CoreLink Creator key features

There are specific features of CoreLink Creator for you to use to configure various CoreLink IP products.

These features are:

- Configures and integrates CoreLink System IP.
- Performs automatic high-level specification generation that is based on IP-XACT. This identifies and defines the typical interfaces that are required to generate a CoreLink interconnect.
- Performs automatic microarchitecture generation of a CoreLink interconnect.
- Executes multiple DRCs. These checks ensure that the system is viable and valid, so it is correct by construction.
- Sets every interface for NIC-400 Network Interconnect automatically, providing simple configuration.
- Generates deliverables, for example:
  — CoreLink component IP-XACT.
  — CoreLink component Verilog RTL.
  — Behavioral testbench.
  — Design specification report.

For more information, see the *ARM® CoreLink™ Creator User Guide*.

3.2 AMBA Designer

This section provides an overview of AMBA Designer (ADR-400).

Use this IP tool for ongoing support of configured legacy NIC-400 implementations, including NIC-400 r0p3 and earlier releases. For compatibility, it also supports the NIC-400 r1p0 and NIC-400 r1p1 releases.

——————— Note ———————

• This section refers to AMBA Designer r3p5 and later versions.
• ARM recommends that you use CoreLink Creator to configure the new generation of products in the CoreLink System IP collection of interconnect products. This includes NIC-450 Network Interconnect r0p0 and NIC-400 r1p0.

3.2.1 About AMBA Designer

AMBA Designer (ADR-400) enables you to configure ARM IP and create AMBA-compliant systems.

AMBA Designer supports:
• IP-XACT versions 1.2 and 1.4.
• Configuring CoreLink and CoreSight™ devices.
• Generating RTL for the configured devices.
• Optimizing the AMBA interconnects.
• Stitching together interconnects and CoreLink and CoreSight system IP components into an AMBA-compliant system with IP-XACT stitching.

After you generate the components, you can stitch them together in the AMBA Designer Canvas to create systems. These systems are shown in a graphical format and highlight the components, their ports, and the connections between the ports.

The ADR-400 workflow is illustrated in the following figure.
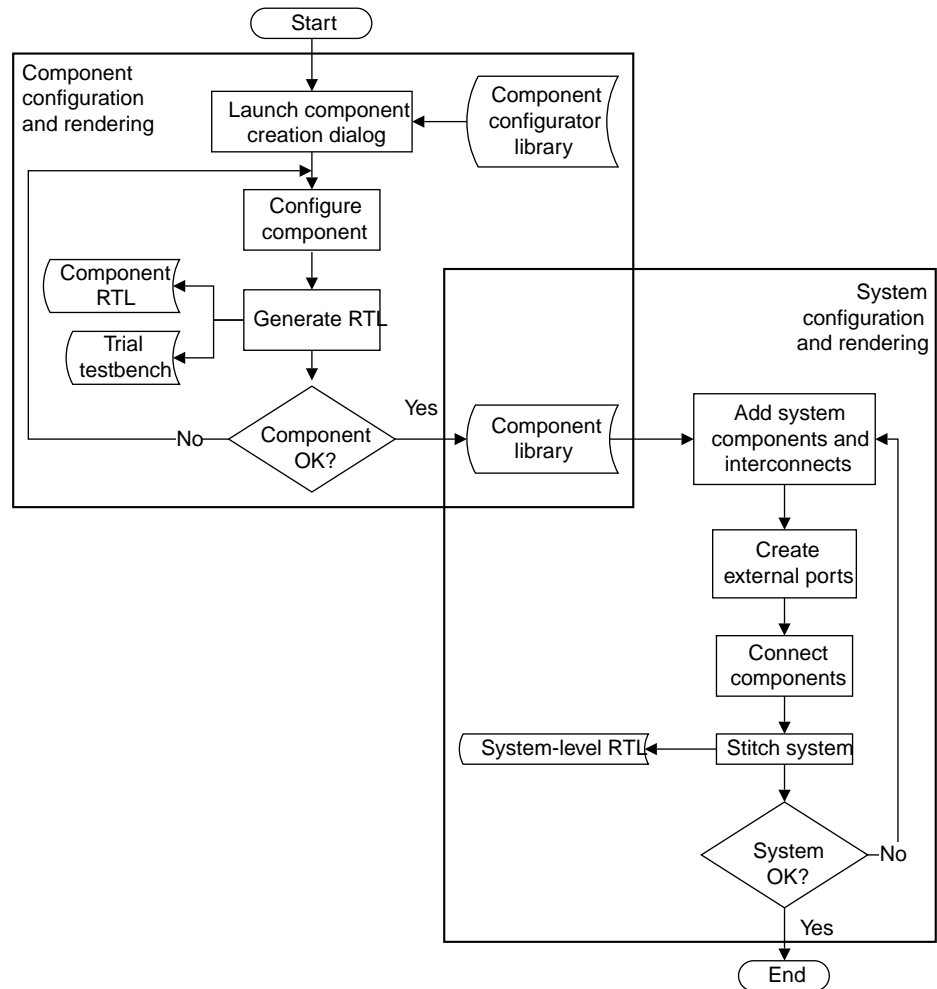
Figure 3-2 AMBA Designer Workflow

ADR-400 outputs configured Verilog RTL together with industry-standard IP-XACT enabling easier integration and implementation. To verify the Verilog RTL files, use the associated Out-of-Box testbenches.

3.2.2   AMBA Designer key features

The AMBA Designer ADR-400 has some key features to accelerate AMBA protocol-based design.

These key features are:

- Configuration engines for System IP, allowing for rapid configuration of ARM AMBA components.
- A drag and drop integration environment in the GUI, allowing for easy assembly of configured components.
- Industry standard IP-XACT 1.2 and 1.4 support, allowing for maximum reuse of existing configurations because you can create your own IP library.

Related information

ARM® AMBA® Designer ADR-400 User Guide.

Appendix A
Revisions

This appendix describes the changes between released issues of this book.

It contains the following section:

A.1 Revisions

This appendix describes changes between released issues of this book.

Table A-1 Issue 0000-00

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue 0000-00 and issue 0000-01

Change	Location	Affects
Updated Introduction information	*1.1 About the CoreLink NIC-450 Network Interconnect* on page 1-11	r0p0