

# ARM® DynamIQ™ Shared Unit

Revision: r0p2

## Technical Reference Manual



# ARM® DynamIQ™ Shared Unit

## Technical Reference Manual

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### Release Information

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# Preface

This preface introduces the *ARM® DynamIQ™ Shared Unit Technical Reference Manual*.

It contains the following:

- [About this book](#) on page 10.
- [Feedback](#) on page 14.

## About this book

This Technical Reference Manual is for the DynamIQ™ Shared Unit (DSU). It describes the overall structure of the DSU including the main interfaces. It also describes power management, the memory system, caches, and the DebugBlock. Information on the programming registers is also provided.

## Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, *r1p2*, where:

*rm* Identifies the major revision of the product, for example, *r1*.

*pn* Identifies the minor revision or modification status of the product, for example, *p2*.

## Intended audience

This manual is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the DSU.

## Using this book

This book is organized into the following chapters:

### **Part A Functional Description**

#### **Chapter A1 Introduction**

This chapter introduces the *DynamIQ Shared Unit* (DSU) and its features.

#### **Chapter A2 Technical Overview**

This chapter describes the structure of the DSU.

#### **Chapter A3 Clocks and Resets**

This chapter describes the clocks and resets of the DSU.

#### **Chapter A4 Power Management**

This chapter describes the power domains and the power modes in the DSU.

#### **Chapter A5 L3 Cache**

This chapter describes the L3 cache.

#### **Chapter A6 ACE Master Interface**

This chapter describes the ACE master memory interface.

#### **Chapter A7 CHI Master Interface**

This chapter describes the AMBA 5 CHI master memory interface.

#### **Chapter A8 ACP Slave Interface**

This chapter describes the ACP slave interface.

#### **Chapter A9 AXI Master Peripheral Port**

This chapter describes the AXI master peripheral port.

### **Part B Register Descriptions**

#### **Chapter B1 Control registers**

This chapter describes the control registers for the DSU.

#### **Chapter B2 Error system Registers**

This chapter describes the ERR1\* error registers for the DSU.

#### **Chapter B3 PMU Registers**

This chapter describes the PMU registers for the DSU.

## Part C Debug

### Chapter C1 Debug

This chapter describes the debug features of the DSU and the associated DebugBlock component.

### Chapter C2 PMU

This chapter describes the *Performance Monitor Unit* (PMU).

### Chapter C3 Debug Registers

This chapter describes the debug registers for the DSU.

### Chapter C4 ROM Table

This chapter describes the CoreSight ROM Table component.

## Part D Appendices

### Appendix A Compatible Core Versions

This appendix lists the permissible combinations of cores.

### Appendix B Signal Descriptions

This appendix describes the DSU signals.

### Appendix C Revisions

This appendix describes the technical changes between released issues of this book.

## Glossary

The ARM® Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM® Glossary* for more information.

## Typographic conventions

### *italic*

Introduces special terminology, denotes cross-references, and citations.

### **bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

### `monospace`

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

### monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

### `monospace italic`

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

### `monospace bold`

Denotes language keywords when used outside example code.

### <and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

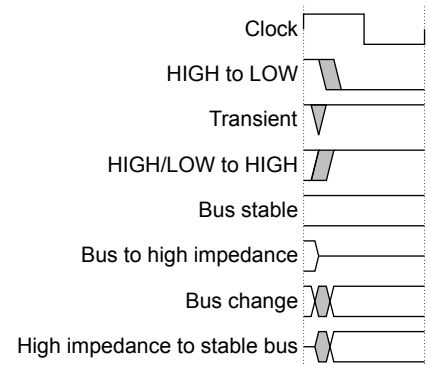
### SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

## Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



**Figure 1 Key to timing diagram conventions**

## Signals

The signal conventions are:

### Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.

Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

### Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

## Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

## ARM publications

- *AMBA® AXT™ and ACE™ Protocol Specification AXI3™, AXI4™, and AXI4-Lite™, ACE and ACE-Lite™* (ARM IHI 0022).
- *AMBA® APB Protocol Version 2.0 Specification* (ARM IHI 0024).
- *AMBA® 4 ATB Protocol Specification* (ARM IHI 0032).
- *ARM® AMBA® CHI Protocol Specification* (ARM IHI 0050).
- *Low Power Interface Specification ARM® Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile* (ARM DDI 0487).
- *ARM® Generic Interrupt Controller Architecture Specification* (ARM IHI 0069).
- *ARM® CoreSight™ Architecture Specification v3.0* (ARM IHI 0029).
- *ARM® CoreSight™ DAP-Lite2 Technical Reference Manual* (ARM 100572) .
- *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480).
- *ARM® Embedded Trace Macrocell Architecture Specification ETMv4* (ARM IHI 0064).
- *ARM® CoreSight™ ELA-500 Embedded Logic Analyzer Technical Reference Manual* (ARM 100127).

The following confidential books are only available to licensees:

- *ARM® DynamIQ™ Shared Unit Configuration and Sign-off Guide* (ARM 100454).
- *ARM® DynamIQ™ Shared Unit Integration Manual* (ARM 100455).

## Other publications

None.

## Feedback

### Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

### Feedback on content

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- The title *ARM DynamIQ Shared Unit Technical Reference Manual*.
- The number ARM 100453\_0002\_00\_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

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## Part A

### **Functional Description**





# Chapter A1

## Introduction

This chapter introduces the *DynamIQ Shared Unit* (DSU) and its features.

It contains the following sections:

- *A1.1 About the DSU* on page A1-18.
- *A1.2 Features* on page A1-20.
- *A1.3 Implementation options* on page A1-21.
- *A1.4 Supported standards and specifications* on page A1-24.
- *A1.5 Test features* on page A1-25.
- *A1.6 Design tasks* on page A1-26.
- *A1.7 Product revisions* on page A1-27.

## A1.1 About the DSU

The *DynamiQ Shared Unit* (DSU) comprises the L3 memory system, control logic, and external interfaces to support a DynamiQ cluster.

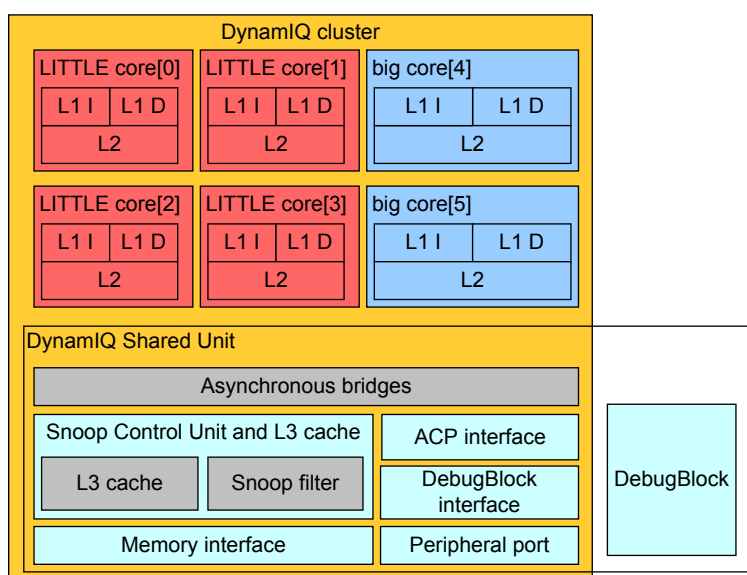
The DynamiQ cluster microarchitecture integrates one or more cores with the DSU to form a cluster that is implemented to a specified configuration.

The cores are selected and configured during macrocell implementation.

A cluster can be implemented in one of two configurations:

- A set of cores having the same microarchitecture.
- Two sets of cores, where each set has a different microarchitecture. This configuration might be used in a DynamiQ big.LITTLE™ cluster.

The following diagram shows a cluster that is composed of two sets of cores in a DynamiQ big.LITTLE configuration.



**Figure A1-1 DynamiQ cluster**

Within the DSU, are the L3 cache, the *Snoop Control Unit* (SCU), internal interfaces to the cores, and external interfaces to the SoC.

- The shared L3 cache simplifies process migration between the cores.

————— **Note** —————

Some cores can be configured without L2 caches. To these cores, the shared L3 cache appears as an L2 cache. The term 'L3 cache' is used throughout this document to describe the shared cache.

- The *Snoop Control Unit* (SCU) maintains coherency between caches in the cores and L3. The SCU includes a Snoop Filter to optimize coherency maintenance operations.
- Internal interfaces to the cores are configured during macrocell implementation and are not directly visible.
- External interfaces are connected to the SoC.

Each core can be configured either to be run synchronously with the DSU, sharing the clock, or asynchronously, with an independent clock.

Microarchitecture features and system control registers that are specific to the implemented cores are described in separate TRMs delivered with the cores.

A DebugBlock is provided with the DSU that integrates an Embedded Cross-Trigger Interface with debugging registers and supports debug over powerdown. The DebugBlock includes all functionality that is required in the debug power domain.

## A1.2 Features

The DSU includes the following features:

- AMBA 5 ACE or AMBA 5 CHI main bus interface.
- Optional 128-bit wide I/O-coherent *Accelerator Coherency Port* (ACP).
- Optional 64-bit wide device peripheral port.
- Support for cores with 40-bit, 44-bit, or 48-bit physical addresses.
- ARMv8.2 debug logic.
- *Reliability, Availability, and Serviceability* (RAS) support.
- Optional unified 16-way set-associative L3 cache.
- 64-byte cache lines throughout.
- Partial L3 cache powerdown support.
- Optional cache protection in the form of *Error Correcting Code* (ECC) on L3 cache RAM instances.
- *Snoop Control Unit* (SCU).
- Cores can be clocked at different frequencies.
- L3 memory system can be clocked at a rate synchronous to the external system interconnect or at integer multiples.

## A1.3 Implementation options

The DynamIQ Shared Unit can be implemented from a range of options. These options are specified during macrocell implementation.

**Table A1-1 Configuration parameters**

Parameter name	Permitted values	Description
NUM_BIG_CORES	0, 1, 2, or 4 cores.	The number of big cores that can be implemented depends on the number of LITTLE cores implemented.
NUM_LITTLE_CORES	0, 1, 2, 3, 4, 6, 7, or 8 cores.	The number of LITTLE cores that can be implemented depends on the number of big cores implemented.
BIG_CORE_TYPE	-	The type of big core you can implement depends on your license.
LITTLE_CORE_TYPE	-	The type of LITTLE core you can implement depends on your license.
MODULE	-	Name of the cluster top-level Verilog file. If you do not specify any top-level module name, then a name is autogenerated based on the number and types of cores present.
MODULE_DEBUG_BLOCK	-	Name of the DebugBlock top-level Verilog file. If you do not specify any DebugBlock module name, then a name is autogenerated based on the top-level module name.
ACE	TRUE, FALSE	Main memory interface. <b>TRUE</b> Implement AMBA 5 ACE. <b>FALSE</b> Implement AMBA 5 CHI.
MASTER_DATA_WIDTH	128 or 256.	Bus width for the main coherent master interface. <b>128</b> 1 x 128-bit wide ACE or CHI. <b>256</b> 2 x 128-bit wide ACE, or 1x 256-bit wide CHI.  ————— <b>Note</b> ————— It is not possible to set MASTER_DATA_WIDTH to 256 when both ACE is TRUE and L3_CACHE_SIZE is 512KB. —————
PORTER_SAM	TRUE, FALSE	<i>System Address Map</i> (SAM). Only applicable if the CHI interface is implemented. <b>TRUE</b> Include support for the CMN-600 interconnect SAM. <b>FALSE</b> Do not include.
ACP	TRUE, FALSE	ACP. <b>TRUE</b> Include ACP. <b>FALSE</b> Do not include ACP.
PERIPH_PORT	TRUE, FALSE	Peripheral port. <b>TRUE</b> Include Peripheral port. <b>FALSE</b> Do not include Peripheral port.

**Table A1-1 Configuration parameters (continued)**

Parameter name	Permitted values	Description
SCU_CACHE_PROTECTION	TRUE, FALSE	<p><i>Error Correcting Code (ECC) support.</i></p> <p><b>TRUE</b> Protect the L3 cache RAMs and snoop filter RAMs with ECC.</p> <p><b>FALSE</b> No ECC on L3 cache RAMs and snoop filter RAMs.</p> <p>————— <b>Note</b> —————</p> <p>The DSU ECC protection implementation is configured in conjunction with the cache protection parameter of your core (CORE_CACHE_PROTECTION). See the documentation for your core for more information.</p> <p>The valid combinations are:</p> <ul style="list-style-type: none"> <li>• CORE_CACHE_PROTECTION = FALSE, SCU_CACHE_PROTECTION = FALSE.</li> <li>• CORE_CACHE_PROTECTION = FALSE, SCU_CACHE_PROTECTION = TRUE.</li> <li>• CORE_CACHE_PROTECTION = TRUE, SCU_CACHE_PROTECTION = TRUE.</li> </ul>
L3_CACHE_SIZE	<ul style="list-style-type: none"> <li>• 512KB.</li> <li>• 1024KB.</li> <li>• 2048KB.</li> <li>• 4096KB.</li> </ul>	L3 cache size.
L3_DATA_WR_LATENCY	1 or 2.	<p>L3 cache data RAM input latency.</p> <ul style="list-style-type: none"> <li>• 1 cycle latency.</li> <li>• 2 cycles latency.</li> </ul>
L3_DATA_RD_LATENCY	2 or 3.	<p>L3 cache data RAM output latency.</p> <ul style="list-style-type: none"> <li>• 2 cycles latency.</li> <li>• 3 cycles latency.</li> </ul>
L3_DATA_RD_SLICE	TRUE, FALSE	<p>L3 cache data RAM output register slice.</p> <p><b>TRUE</b> Include L3 data RAMs output register slice.</p> <p><b>FALSE</b> Do not include register slice.</p>
CORE_REG_SLICE	TRUE, FALSE	<p>For each core, include a register slice between the core and the <i>Snoop Control Unit</i> (SCU).</p> <p>For each core present, starting with core 0, set the value to TRUE or FALSE.</p> <p><b>TRUE</b> Include a register slice between the core and the SCU.</p> <p><b>FALSE</b> Do not include a register slice.</p>
ASYNC_BRIDGE	TRUE, FALSE	<p>For each core, asynchronous bridge on L2 to L3 coherent interface.</p> <p>For each core present, starting with core 0, set the value to TRUE or FALSE.</p> <p><b>TRUE</b> Include an asynchronous bridge for the main bus between L2 and L3.</p> <p><b>FALSE</b> Do not include an asynchronous bridge.</p>
CORE_SYNC_LEVELS	2 or 3.	Number of synchronizer stages in all asynchronous inputs into the core.
SYNC_LEVELS	2 or 3.	Number of synchronizer stages in all asynchronous inputs to the SCU and cluster logic.

**Table A1-1 Configuration parameters (continued)**

Parameter name	Permitted values	Description
LEGACY_V7_DEBUG_MAP	TRUE, FALSE	Legacy v7 debug memory map. Configure v7 or v8 Debug memory map. <b>TRUE</b> v7 Debug memory map. <b>FALSE</b> v8 Debug memory map.
ELA	TRUE, FALSE	Support for integrating the CoreSight ELA-500 Embedded Logic Analyzer. <b>TRUE</b> Include support for integrating the ELA-500. <b>FALSE</b> Do not include support for integrating the ELA-500.  ————— <b>Note</b> ————— If enabled, you must run the uniquify script supplied with the ELA to generate a unique ELA instance for use with the DSU. —————

## A1.4 Supported standards and specifications

The DynamIQ Shared Unit complies with the ARMv8.2 architecture.

**Table A1-2 Compliance with standards and specifications**

Architecture specification or standard	Version
ARM architecture	ARMv8.2.
<i>Advanced Microcontroller Bus Architecture (AMBA)</i>	<ul style="list-style-type: none"> <li>• AMBA 5 ACE.</li> <li>• AMBA 5 CHI (Issue B).</li> </ul>
<i>Performance Monitor Unit (PMU)</i>	PMUv3.
Debug	ARMv8.2.
CoreSight	v3.



## A1.5 Test features

The DSU provides interfaces for manufacturing test.

The following manufacturing test interfaces are supported:

**DFT** For logic testing.

**MBIST** For RAM testing.

## A1.6 Design tasks

The DynamIQ Shared Unit is delivered as a synthesizable Register Transfer Level (RTL) description in the SystemVerilog HDL. Before you can use it, you must implement, integrate, and program it.

A different party can perform each of the following tasks. Each task can include implementation and integration choices that affect the behavior and features of the DSU and its associated cores .

### **Implementation**

The implementer configures and synthesizes the RTL to produce a hard macrocell. This task includes integrating RAMs into the design.

### **Integration**

The integrator connects the macrocell into a SoC. This task includes connecting it to a memory system and peripherals.

### **Programming**

The system programmer develops the software to configure and initialize the DSU and its associated cores and tests the application software.

The operation of the final device depends on the following:

### **Build configuration**

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

### **Configuration inputs**

The integrator configures some features of the DSU by tying inputs to specific values. These configuration settings affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

### **Software configuration**

The programmer configures the DSU by programming particular values into registers. The configuration choices affect the behavior of the DSU and its associated cores.

## A1.7 Product revisions

This section describes the differences in functionality between product revisions.

- r0p0** First release.
- r0p1** CHI and ACP support added.
- r0p2** There are no functional changes in this release.



# Chapter A2

## Technical Overview

This chapter describes the structure of the DSU.

It contains the following sections:

- *A2.1 Components* on page A2-30.
- *A2.2 Interfaces* on page A2-33.
- *A2.3 RAS support* on page A2-36.

## A2.1 Components

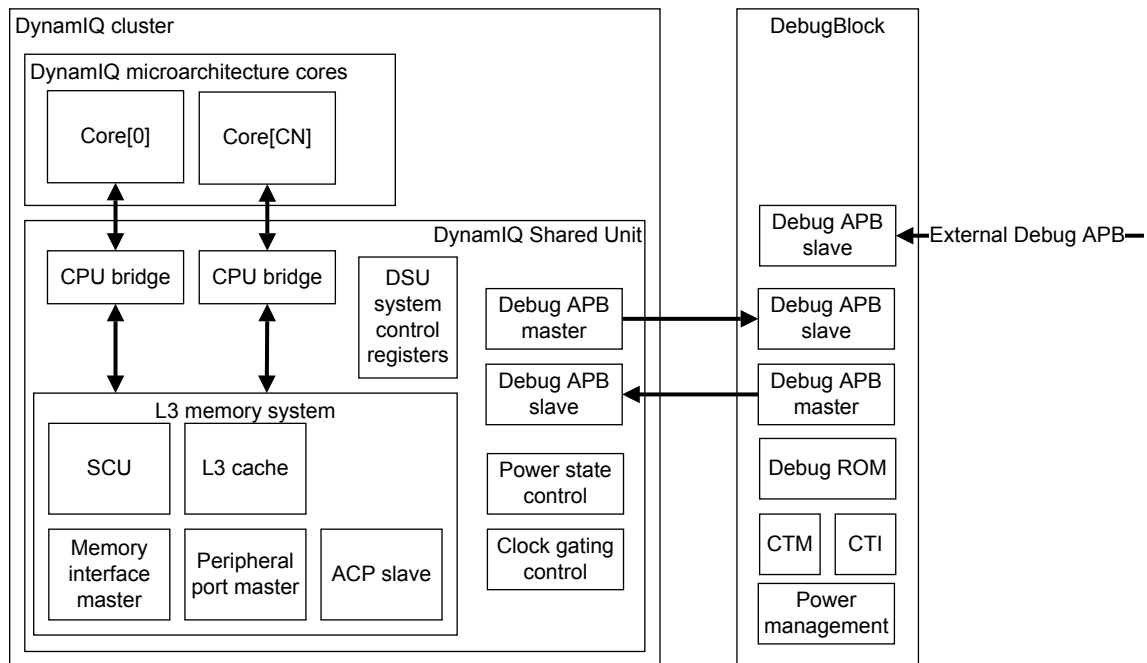
A DynamIQ cluster comprises two top-level modules:

- A module which includes the cores and the *DynamIQ Shared Unit* (DSU).
- The DebugBlock.

In this book, the DynamIQ cluster is referred to as the cluster.

Separating the debug components from the cluster allows the debug components to be implemented in a separate power domain, allowing debug over power down.

The following figure shows the major components in a DynamIQ cluster system.



**Figure A2-1 DynamIQ cluster components**

Throughout this book CN represents a set of cores, where CN has a value of the total number of cores - 1. The ARM architecture allows for cores to be single, or multi-threaded. A *Processing Element* (PE) performs a thread of execution. A single-threaded core has one PE and a multi-threaded core has two or more PEs. Where a reference to a core is made, the core can be a single, or multi-threaded core. Signal names that are associated with PEs use the abbreviation PE, where PE has a value of the total number of PEs - 1.

### DynamIQ™ cluster compatible cores

The core types, and optional features are selected by the macrocell implementer. The cores are described in their respective TRMs. Because the cores are instantiated within the cluster, all interfacing between the cores and the DSU is implemented automatically. All external signal inputs and outputs pass through the DSU. The DSU buffers and resynchronizes many of these signals to allow the cores to be clocked at different speeds. The L2 memory interface of each core is internally connected to the DSU L3 memory system. Where necessary, the DSU implements additional buffering to compensate for different clock rates of the core L2 and DSU L3. Each core implements clock and power control interfaces. These interfaces are routed through the DSU to the respective core external power controller.

### CPU bridges

The CPU bridges control buffering and synchronization between the cores and DSU.

## Snoop Control Unit (SCU)

The SCU maintains coherency between all the data caches in the cluster.

The SCU contains buffers that can handle direct cache-to-cache transfers between cores without having to read or write data to the L3 cache. Cache line migration enables dirty cache lines to be moved between cores, and there is no requirement to write back transferred cache line data to the L3 cache.

## Debug and trace components

Each core includes an *Embedded Trace Macrocell* (ETM) to allow program tracing while debugging.

Trigger events from the cores are combined and output to the Debug APB master. Trigger events to the cores, and debug register accesses, are received on the Debug APB slave.

## Clock and power management

The cluster supports a set of power-saving modes that are controlled by an external power controller. The modes are selected through power-mode requests on P-Channels, for each of the cores, and a separate P-Channel for the DSU.

Clock gating is supported through Q-Channel requests from an external clock controller to the DSU. The Q-Channels allow individual control of the **SCLK**, **PCLK**, **ATCLK**, and **GICCLK** clock inputs.

## L3 memory interfaces

### Main memory master

The main memory interface is implemented as either a CHI master or up to two ACE master interfaces.

### Accelerator Coherency Port

The *Accelerator Coherency Port* (ACP) is an optional slave interface. The ACP provides direct memory access to cacheable memory. The SCU maintains cache coherency by checking ACP accesses for allocation in the core and L3 caches. The ACP implements a subset of the ACE-Lite protocol.

### Peripheral port

The peripheral port is an optional master interface and provides Device accesses to tightly coupled accelerators. The port implements the AXI 4 master interface protocol.

## L3 cache

The cache is 16-way set associative with a 64-byte line length. The cache size is implemented as either 512K, 1MB, 2MB, or 4MB. ECC protection of data and tag RAMs is optionally implemented.

## DSU system control registers

The DSU implements a set of system control registers, which are common to all cores in the cluster. You can access these registers from any core in the cluster. These registers provide:

- Control for power management of the cluster.
- CHI QoS bus control and scheme ID assignment.
- Information about the hardware configuration of the DSU.
- L3 cache hit and miss count information.

## DebugBlock

The debug components are split between two architecturally defined logical power domains, the core power domain and the debug power domain:

- The core power domain comprises one or more physical power domains for the cores and DSU.
- The debug power domain includes the DebugBlock.

The separate power domains allow the cores and the cluster to be powered down while maintaining essential state that is required to continue debugging. Separating the logical power domains into physical domains is optional and might not be available in individual systems.

**Cluster to DebugBlock APB**

Trigger events from the cores are transferred to the DebugBlock as APB writes.

**DebugBlock to cluster APB**

Trigger events to the cores are transferred as APB writes to the DSU. Register accesses from the system debug APB are transferred to the DSU.

**System debug APB**

The system debug APB slave interface connects to external CoreSight components, such as the *Debug Access Port* (DAP).

**CTI and CTM**

The DebugBlock implements an *Embedded Cross-Trigger* (ECT). Each core in the cluster is allocated a *Cross Trigger Interface* (CTI) and the CTIs are interconnected through the *Cross Trigger Matrix* (CTM). A single external channel interface is implemented to allow cross-triggering to be extended to the SoC.

**Debug ROM**

The ROM table contains a list of components in the system. Debuggers can use the ROM table to determine which CoreSight components are implemented.

**Power management and clock gating**

The DebugBlock implements two Q-Channel interfaces, one for requests to gate the **PCLK** clock, and a second for requests to control the debug power domain.

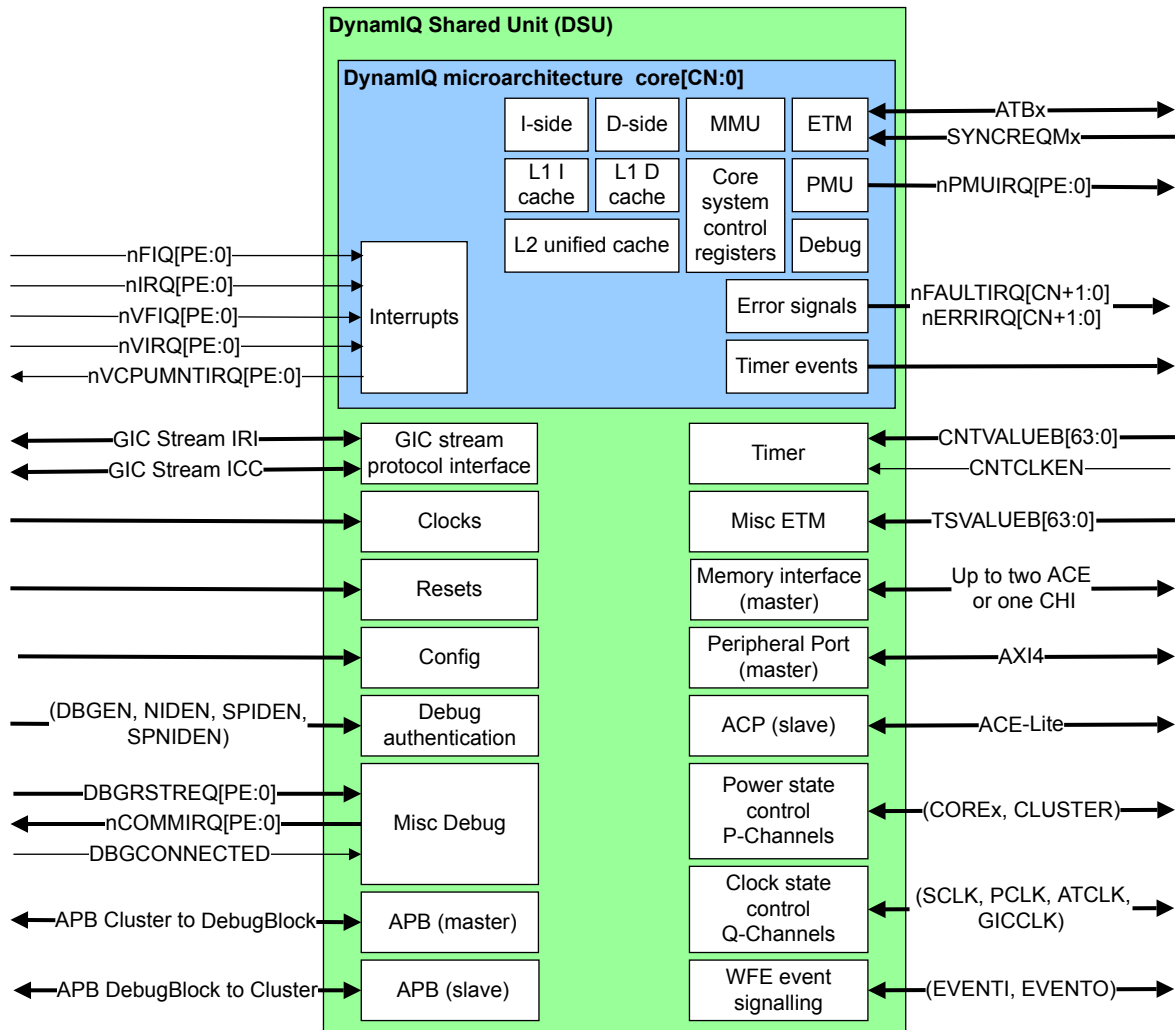


## A2.2 Interfaces

The external interfaces to connect to the SoC system.

### DSU interfaces

The following figure shows the major external interfaces of the *DynamiQ Shared Unit (DSU)*.



**Figure A2-2 DSU interfaces**

The following table describes the major external interfaces.

**Table A2-1 DSU interfaces**

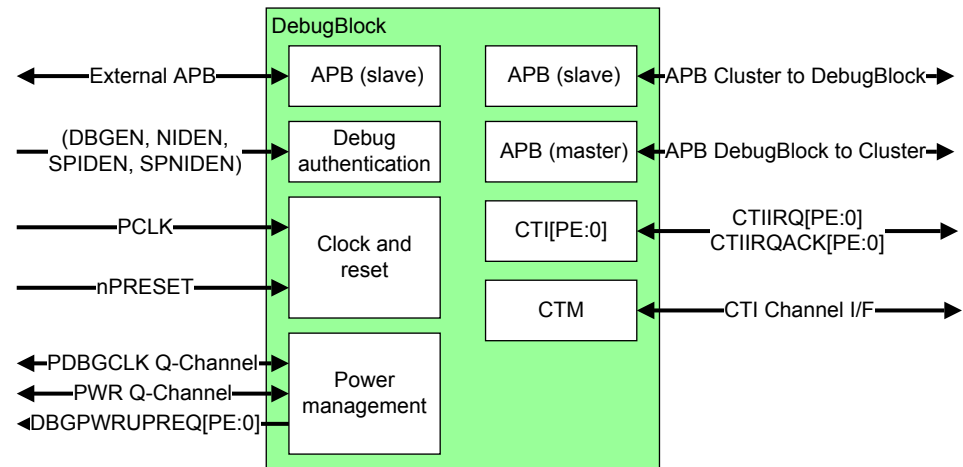
Purpose	Protocol	Notes
Trace	ATB	Master ATB interfaces. Each core, or <i>Processing Element</i> (PE), has an ATB interface to output ETM trace information.
Memory	ACE or CHI	Master interface to main memory. Optionally, one CHI or up to two ACE interfaces.
Accelerator Coherency Port (optional)	ACE-Lite	Slave interface allowing an external master to make coherent requests to cacheable memory.

**Table A2-1 DSU interfaces (continued)**

Purpose	Protocol	Notes
Peripheral port (optional)	AXI	Low-latency master interface to external Device memory.
Debug cluster to DebugBlock	APB	Master and slave APB interfaces to DebugBlock.
Power state control	P-Channel	P-Channels for DSU and core power management.
Clock state control	Q-Channel	Q-Channels for clock gating control.
WFE event signaling	-	Signals for <i>Wait For Event</i> (WFE) wake-up events.
Generic timer	-	Input for the generic time count value. The count value is distributed to all cores. Each core outputs timer events.
GIC interfaces	-	Interrupts to individual cores. A single GIC Stream Protocol interface is shared by all cores.
<i>Design for Test</i> (DFT)	-	Interface to allow access for <i>Automatic Test Pattern Generation</i> (ATPG) scan-path testing.
<i>Memory Built-In Self-Test</i> (MBIST)	ARM MBIST	Internal interface that supports the manufacturing test of the L3 and SCU memories embedded in the DSU. Each core has its own internal MBIST interface.

### DebugBlock interfaces

The following figure shows the major external interfaces.


**Figure A2-3 DebugBlock interfaces**

The following table describes the major external interfaces.

**Table A2-2 DebugBlock interfaces**

Purpose	Protocol	Notes
External debug	APB	Slave interface to external debug component, for example a <i>Debug Access Port</i> (DAP). Allows access to debug registers and resources.
Debug cluster to DebugBlock	APB	Master and slave APB interfaces to DebugBlock.

**Table A2-2 DebugBlock interfaces (continued)**

Purpose	Protocol	Notes
Cross-trigger channel interface	CTI	Allows cross-triggering to be extended to external SoC components.
Power management	Q-Channel	Enables communication to an external power controller. To control clock gating and powerdown.

## A2.3 RAS support

The DSU supports *Reliability, Availability, and Serviceability* (RAS) features.

- Data poisoning on a 64-bit granule is supported in the DSU.

# Chapter A3

## Clocks and Resets

This chapter describes the clocks and resets of the DSU.

It contains the following sections:

- [A3.1 Clocks on page A3-38.](#)
- [A3.2 Resets on page A3-40.](#)

## A3.1 Clocks

The DSU requires clock signals for each of the cores, internal logic, and external interfaces.

The following table describes the clocks.

**Table A3-1 DSU clock signals**

Signal	Description
<b>CORECLK[CN:0]</b>	The per-core clocks for all core logic including L1 and L2 caches.
<b>SCLK</b>	The clock for the SCU and L3 memory system, including the ACE or CHI master interface. <b>SCLK</b> is also used for any cores that are configured to run synchronously to the DSU.
<b>PCLK</b>	<p>The clock for the DebugBlock and DSU debug APB interfaces.</p> <p>————— <b>Note</b> —————</p> <p>The DebugBlock and cluster both have <b>PCLK</b> inputs. You might choose to connect these to the same clock. Alternatively, you might choose to place an asynchronous bridge between the two clock inputs, in which case they might be different clocks.</p> <p>—————</p>
<b>ATCLK</b>	<p>The clock for the ATB trace buses output from the DSU.</p> <p>————— <b>Note</b> —————</p> <p>All ATB buses output from the DSU share the same clock.</p> <p>—————</p>
<b>GICCLK</b>	The clock for the GIC AXI-stream interface between the DSU and an external GIC.
<b>PERIPHCLK</b>	The clock for peripheral logic inside the DSU such as timers, and clock and power management logic.

All clocks can be driven fully asynchronously to each other. The DSU contains all the necessary synchronizing logic for crossing between clock domains. There are no clock dividers and no latches in the design. The entire design is rising edge triggered.

————— **Note** —————

- It is possible to configure some or all the cores to run synchronously with the L3 memory system. If this option is chosen, the corresponding **CORECLK** signals are not present and the synchronous cores run with **SCLK**.
- The DebugBlock can be clocked by a different clock from the DSU **PCLK**. To allow this, the macrocell implementer can choose to add asynchronous bridges between the DSU and the DebugBlock.

Some external interfaces, such as the main ACE or CHI master interface, support a clock enable input to allow the external logic to run at a lower, synchronous, frequency. While there is no functional requirement for the clocks to have any relationship with each other, the DSU is designed with the following expectations to achieve acceptable performance:

- **CORECLK[CN:0]** is dynamically scaled to match the performance requirements of each core.
- **SCLK** frequency affects the L3 hit latency and, therefore, it is important for achieving good performance. For best performance, ARM recommends running **SCLK** as close to **CORECLK[CN:0]** frequency as possible. However to reduce dynamic and leakage power, targeting a lower frequency might be required. Running **SCLK** at least approximately 75% of the **CORECLK[CN:0]** frequency might give an appropriate balance for many systems.
- **SCLK** can run at synchronous 1:1 or 2:1 frequencies with the external interconnect, avoiding the need for an asynchronous bridge between them.

- **PCLK**, **ATCLK**, and **GICCLK** can run at the same frequency as the relevant SoC components that they connect to. This would typically be approximately 25% of the maximum **CORECLK[CN:0]** frequency.
- **PERIPHCLK** contains the architectural timers, and software performance can be impacted if reads to these registers take too long. Therefore, ARM recommends that **PERIPHCLK** is run at least 25% of the maximum **CORECLK[CN:0]** frequency.

## A3.2 Resets

The DSU requires reset signals for each of the cores, internal logic, and external interfaces.

**Table A3-2 DSU reset signals**

Signal	Description
<b>nCPUPORESET[CN:0]</b>	The per-core primary powerup reset signal for all resettable registers in the <b>CORECLK</b> domain including debug registers, ETM registers, and RAS registers
<b>nCORERESET[CN:0]</b>	The per-core Warm reset signal for all resettable registers in the <b>CORECLK</b> domain excluding the debug registers, ETM registers, and RAS registers
<b>nPRESET</b>	A single cluster-wide reset signal for all resettable registers in the <b>PCLK</b> domain
<b>nSPORESET</b>	A single cluster-wide powerup reset signal for all resettable registers in the <b>SCLK</b> domain
<b>nSRESET</b>	A Warm reset signal for all resettable registers in the <b>SCLK</b> domain excluding RAS registers
<b>nATRESET</b>	A single cluster-wide reset signal for all resettable registers in the <b>ATCLK</b> domain
<b>nGICRESET</b>	A single cluster-wide reset signal for all resettable registers in the <b>GICCLK</b> domain
<b>nPERIPHRESET</b>	A single cluster-wide reset signal for all resettable registers in the <b>PERIPHCLK</b> domain
<b>nMBISTRESET</b>	A single cluster-wide reset signal that acts on all resettable registers in the <b>CORECLK</b> and <b>SCLK</b> domains

The **nMBISTRESET** signal is intended for use by an external MBIST controller to avoid the need for it to control the reset logic in the SoC.

All reset inputs can be asserted (HIGH to LOW) and deasserted (LOW to HIGH) asynchronously. Reset synchronization logic inside the DSU ensures that reset deassertion is synchronous for all resettable registers inside those reset domains. The core clock does not need to be present for reset assertion, but it must be present for reset deassertion to ensure reset synchronization.

### AArch32 (EL3) to AArch64 Execution state transition at reset

At *Exception level 3* (EL3), cores can only transition between AArch32 and AArch64 states at reset. The Execution state after reset is controlled by the **AA64nAA32[PE:0]** configuration signals. These signals are only sampled at reset.

To reset a core and change Execution state from software, a Warm reset request can be made by setting the RR bit of the RMR system register (from AArch32) or the RMR\_EL3 register (from AArch64). Following the register write and executing a WFI instruction, the cluster automatically resets the core without requiring any action by the external reset controller. The hardware automatically cleans and invalidates all the caches and safely disconnects the core from cluster before the reset is asserted.

#### Note

Your implementation might include cores that do not support execution in AArch32 state at EL3.



# Chapter A4

## Power Management

This chapter describes the power domains and the power modes in the DSU.

It contains the following sections:

- *A4.1 About DSU power management* on page A4-42.
- *A4.2 Power mode control* on page A4-43.
- *A4.3 Communication with the power controller* on page A4-44.
- *A4.4 L3 RAM power control* on page A4-45.
- *A4.5 Power modes* on page A4-47.
- *A4.6 Power operating requirements* on page A4-52.
- *A4.7 Wait For Interrupt and Wait For Event* on page A4-53.
- *A4.8 Clock, voltage, and power domains* on page A4-54.
- *A4.9 Cluster powerdown* on page A4-56.

## A4.1 About DSU power management

The DSU supports a range of low-power modes and cache RAM powerdown modes.

The DSU supports the following power modes:

### **On**

On mode is the normal mode of operation where all the core and DSU functionality is available. The DSU individually disables internal clocks, and inputs to unused functional blocks. Only the logic that is in use consumes dynamic power.

### **Functional retention**

Functional retention allows the L3 cache and snoop filter RAMs to be put temporarily in to a retention state while the L3 cache is not being accessed. The contents of the cache RAMs are retained.

### **Memory retention**

Memory retention mode allows the L3 cache and snoop filter RAMs to be held in retention while the rest of the cluster is powered down. Keeping the RAMs in retention reduces the energy cost of writing dirty lines back to memory and reduces the cluster response time on powerup. It is not possible to snoop the cache in this mode, so it is important that no other external coherent agents are active (for example, cores external to the cluster, or other coherent devices). In practice, this mode can only be used in a coherent system when the cluster is the only active agent.

### **Off**

In off mode, power is removed completely, and no state is retained. To avoid losing data, the cores within the cluster, and the cluster itself must first be taken out of coherence.

The DSU supports clock, voltage, and power domains that can be controlled by external logic. The cluster, in conjunction with power management software, gives operating requirement hints to an external power controller. The power controller is responsible for coordinating power management with the rest of the SoC, switching and isolating power and voltage domains, and controlling clock gating cells.

## A4.2 Power mode control

Power management control is distributed between power management software, the cluster, and an external power controller.

The cluster supports a set of power operating requirements which act as hints to the external power controller. The operating requirements indicate: the required cache capacity, the RAM retention mode, and whether the cluster logic can be powered up or down. The power controller controls the logic clamps and power switches required to put the RAMs and logic into low-power operation.

Software sets the operating requirements by writing to the following system registers:

*Cluster Power Control Register* (CLUSTERPWRCTLR\_EL1)

To request partial L3 cache powerup or powerdown, and to enable RAM retention capabilities.

*Cluster Powerdown Register* (CLUSTERPWRDN\_EL1)

To request the power mode that the cluster is to enter, after all cores have powered off. For example, memory retention mode.

The operating requirements are signaled to the power controller through the cluster P-channel interface. The power controller responds to a change of operating requirements by sequencing the transition between lower or higher power modes.

Power management algorithms can use *Cluster L3 Hit Counter Register* (CLUSTERL3HIT\_EL1) and *Cluster L3 Miss Counter Register* (CLUSTERL3MISS\_EL1) system registers to determine when to powerup or powerdown cache portions.

The status of the power settings is indicated in the *Cluster Power Status Register* (CLUSTERPWRSTAT\_EL1) system register.

The cluster receives power mode transition requests from the power controller and checks the validity of each transition. If the transition is supported, the cluster accepts the request. If the transition is not supported, the cluster denies the request. If the cluster accepts the request, the power controller can switch power domains on or off as appropriate.

The cluster automatically performs any internal operations required by a mode transition, before accepting the new mode. The internal actions performed by the cluster include: gating clocks, flushing caches, and disabling coherency.

---

**Note**

If L3 RAM retention is not implemented, CLUSTERPWRCTLR\_EL1.L3 data RAM retention control must be left in the reset state.

---

## A4.3 Communication with the power controller

The cluster provides a P-Channel interface to allow the external power controller to set the operating power mode of the cluster, in response to requests from the cluster.

The cluster indicates the operating requirements on the **CLUSTERPACTIVE** bus. The power controller can then request a new power mode. The power controller indicates the requested mode on the **CLUSTERPSTATE** bus and asserts the **CLUSTERPREQ** handshake signal.

When the cluster has performed all the actions that are required in preparation for the power mode transition, the cluster accepts the request by asserting **CLUSTERPACCEPT**. If the request is not valid, the cluster denies the request by asserting **CLUSTERPDENY**. Reasons for denying the request might be, requesting an incorrect mode transition, or the requested mode is no longer appropriate because the L3 operating mode has changed.

At reset, the cluster reads the initial mode set by the power controller on the **CLUSTERPSTATE** bus.

---

**Note**

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ARM recommends that **CLUSTERPREQ** is asserted at reset. If **CLUSTERPREQ** is not asserted at reset, the power controller must wait for 40 **PERIPHCLK** cycles after reset is deasserted before it drives **CLUSTERPREQ** high.

---

## A4.4 L3 RAM power control

Power savings can be made by putting parts, or all, of the L3 control logic and L3 cache RAM into retention modes, or powering down portions of the RAM.

### A4.4.1 L3 cache partial powerdown

Portions of the L3 cache can be independently powered down to reduce RAM leakage power.

When the full L3 cache capacity is not required, for example small memory footprint workloads, the L3 cache size can be reduced by powering down one or more portions.

The L3 cache RAMs are organized to allow separate control of four groups of four cache ways. Power control is applied independently to each group. The operating cache capacity can be selected from: all, 3/4, 1/2, and 1/4.

Although the tag RAMs can be split into four groups, the data RAMs are only split into two groups. Therefore, the 1/4 and 3/4 capacities might not provide significant power savings compared to the 1/2 and full-L3 capacities, respectively.

The following table shows how the cache capacity relates to RAM power enables.

**Table A4-1 L3 Cache capacity and RAM power enables**

Cache capacity	Tag RAM				Data RAM	
	0	1	2	3	0	1
1/4	On	Off			On	Off
1/2	On	Off				On
3/4	On	Off				
All on	On					

The external power controller requests the required L3 cache capacity, through the cluster P-Channel, in response to power management software setting the operating requirements.

**Note**

RAM powerdown requires that logic clamps and power switches are implemented. To confirm that powerdown is supported, contact your implementer.

### A4.4.2 L3 RAM retention

The *DynamIQ Shared Unit* (DSU) supports two retention power modes.

### Functional retention

Functional retention mode (SFONLY FUNC\_RET,  $\frac{1}{4}$ FUNC\_RET,  $\frac{1}{2}$ FUNC\_RET,  $\frac{3}{4}$ FUNC\_RET, or FULL FUNC\_RET mode) allows the L3 cache and snoop filter RAMs to be put temporarily in to retention while the L3 cache is not being accessed.

When the L3 cache has not been accessed for a period of time, the DSU signals to the power controller that the L3 cache RAM can be put into retention. While in functional retention mode, core and snoop requests can still be received. On receiving a request, the DSU signals to the power controller to take the RAMs out of retention. The core or snoop request is stalled until the power controller signals to the DSU to enter an ON mode (SFONLY ON,  $\frac{1}{4}$ ON,  $\frac{1}{2}$ ON,  $\frac{3}{4}$ ON, or FULL ON). When the request is completed, the DSU signals to the power controller that the RAMs can be put back into retention.

The *Cluster Power Control Register* (CLUSTERPWRCTLR) system register determines the duration of inactivity before the DSU requests the RAMs to be put in to retention.

### Memory retention

Memory retention mode ( $\frac{1}{4}$ MEM\_RET,  $\frac{1}{2}$ MEM\_RET,  $\frac{3}{4}$ MEM\_RET, or FULL MEM\_RET mode) allows the L3 cache and snoop filter RAMs to be put into retention and disables the control logic in the DSU.

Memory retention mode can be entered when the DSU is idle and all cores are OFF. In this mode, the L3 cache cannot process ACP or snoop requests.

Software can request the DSU to enter memory retention by setting the CLUSTERPWRDN\_EL1.Memory retention required bit before that core is powered OFF. After all cores have transitioned to the OFF power mode, and the DSU becomes idle, the DSU indicates MEM\_RET on its P-Channel.

Even if CLUSTERPACTIVE indicates MEM\_RET, the DSU can still accept a P-channel request to transition to the OFF mode.

## A4.5 Power modes

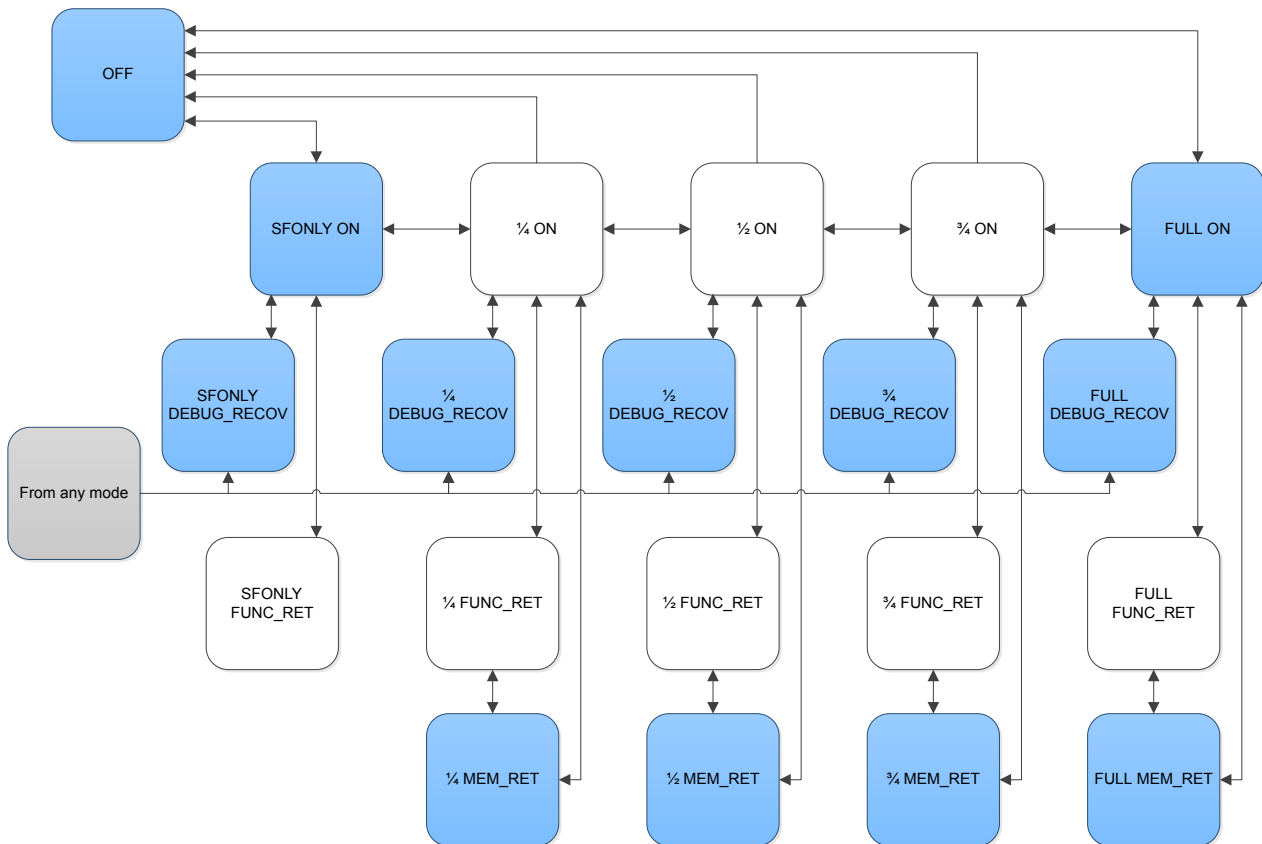
The external power controller can request a new operating power mode in response to the operating requirements indicated by the DSU.

### A4.5.1 Power mode transitions

The *DynamIQ Shared Unit* (DSU) supports a set of power modes. The power controller can request the DSU to transition between modes.

The following diagram shows the supported DSU power modes, and the permitted transitions between them. The blue modes indicate the modes that the DSU can be initialized to at reset. See

[A4.3 Communication with the power controller on page A4-44](#)



**Figure A4-1 DSU power mode transitions**

#### FULL ON

In this mode, all DSU logic, Snoop Filter, and L3 cache RAMs are powered up and fully operational.

The DSU can be initialized into the FULL\_ON mode. In this case, it is treated as an implicit transition from the OFF mode so the L3 cache and Snoop Filter are invalidated. When a transition to the FULL ON mode is completed, the cache and Snoop Filter are accessible and coherent. The L3 cache does not require any configuration from software.

#### SFONLY ON, 1/4ON, 1/2ON, 3/4ON

In these modes, the DSU logic and Snoop Filter RAMs are powered up but some of the L3 cache RAMs remain powered down.

The DSU can be initialized into the SFONLY ON mode. In this case, it is treated as an implicit transition from the OFF mode. When a transition to the SFONLY ON mode is completed, the Snoop Filter is accessible and coherent without needing any configuration from software.

---

**Note**

- Transitions between the ON modes are only allowed in incremental steps. For example, a transition directly from ½ON to FULL ON is not permitted. The **CLUSTERPACTIVE** outputs reflect this, so that **CLUSTERPACTIVE** does not indicate a required mode that cannot be directly reached from the current mode.
  - The SFONLY mode has limited functionality in this release of the DSU. It can be entered when the cluster is idle, but when a transaction attempts to access the L3 cache or snoop filter, the transaction stalls until the DSU has transitioned to the 1/4 ON mode. Therefore, ARM recommends that the SFONLY state is not used.
- 

### SFONLY FUNC\_RET, ¼FUNC\_RET, ½FUNC\_RET, ¾FUNC\_RET, FULL FUNC\_RET

In these modes, the DSU is powered up, the Snoop Filter and L3 cache RAMs are in retention, meaning that the RAMs are inoperable but with state retained.

If a request from a core, or a snoop from the system, is required to be serviced, the request is stalled until the DSU enters one of the ON modes.

When the RAMs are in retention, the clock to the RAMs is automatically gated outside of the retained domain.

### ¼MEM\_RET, ½MEM\_RET, ¾MEM\_RET, FULL MEM\_RET

In these modes, the DSU logic is powered down. The Snoop Filter and L3 cache RAMs are in retention.

All cores in the cluster must be in the OFF mode to allow entry into any one of these modes.

Because the cache contains data that is accessible from the rest of the system, these modes must only be used if there are no other coherent agents in the system that are active and might need to access the data.

### OFF

In this mode, all DSU logic, Snoop Filter, and L3 cache RAMs are powered down.

The DSU can be initialized to this mode on powerup reset.

### Debug Recovery Mode

The debug recovery mode can be used to assist debug of external watchdog-triggered reset events.

By default, the DSU invalidates the cache and snoop filter when there is a transition from OFF to an ON mode. In debug recovery mode, cache invalidation is disabled allowing the contents of the L3 cache that were present before the reset to be observable after the reset. The contents of the L3 cache and snoop filter are retained and are not altered on the transition back to the ON mode.

To enter debug recovery mode, the P-Channel is initialized to DEBUG\_RECOV, and the DSU is cycled through a reset.

To preserve the RAS state and cache contents, a transition to the debug recovery mode can be made from any of the current states. Once in debug recovery mode, a cluster-wide Warm reset must be applied externally. The RAS and cache state are preserved when the core is transitioned to the ON mode.

---

**Note**

- Debug recovery mode is strictly for debug purposes. It must not be used for functional purposes, because correct operation of the cluster is not guaranteed when entering this mode.
- Debug recovery mode can occur at any time with no guarantee of the state of the cluster. A P-Channel request of this type is accepted immediately, therefore its effects on the core, cluster, or the wider system are unpredictable, and a wider system reset might be required. In particular, if there



were outstanding memory system transactions at the time of the reset, then these transactions might complete after the reset when the cluster is not expecting them and cause a system deadlock. If the system sends a snoop to the cluster during this mode, then depending on the cluster state, the snoop might get a response and disturb the contents of the caches, or it might not get a response and cause a system deadlock.

### A4.5.2 Power mode transition behavior

When the power controller requests a transition between power modes, the *DynamIQ Shared Unit* (DSU) automatically performs some actions before accepting the new mode.

Your SoC might implement additional actions. When transitioning from a lower power to higher power mode, these additional actions are performed before the power controller requests a new mode. When transitioning from a higher power to lower power mode, these actions are performed after the DSU accepts the new mode.

The following table shows the permitted mode transitions and behavior that is associated with each transition.

**Table A4-2 Power mode transition behavior**

Start mode	End mode	DSU behavior	Partner implemented behavior
OFF	ON	The L3 cache and snoop filter are initialized. The cluster is brought into coherency with the rest of the system.	Power applied, isolation disabled.
MEM_RET	ON	The cluster is brought into coherency with the rest of the system.	Power applied, isolation disabled.
MEM_RET	FUNC_RET	The cluster is brought into coherency with the rest of the system, but the RAMs remain in retention.	Power applied, clamps and isolation remain enabled.
ON	FUNC_RET	Waits for all memory transactions to complete. The clock to the retention domain is gated. L3 cache and snoop filter RAMs are put into retention.	RAM clamps and isolation enabled.
FUNC_RET	ON	L3 cache and snoop filter RAMs are taken out of retention.	RAM clamps and isolation disabled.
FULL ON	$\frac{3}{4}$ ON	Decreasing available cache ways. Relevant ways in L3 cache are cleaned and invalidated.	RAM clamps and isolation are enabled for relevant ways.
$\frac{3}{4}$ ON	$\frac{1}{2}$ ON		
$\frac{1}{2}$ ON	$\frac{1}{4}$ ON		
$\frac{1}{4}$ ON	SFONLY ON		
SFONLY ON	$\frac{1}{4}$ ON	Increasing available cache ways. Relevant ways in L3 cache are initialized.	RAM clamps and isolation are disabled for relevant ways.
$\frac{1}{4}$ ON	$\frac{1}{2}$ ON		
$\frac{1}{2}$ ON	$\frac{3}{4}$ ON		
$\frac{3}{4}$ ON	FULL ON		
ON	OFF	Waits for all memory transactions to complete. L3 cache allocation is disabled. The L3 cache is cleaned and invalidated. The cluster is removed from system coherency.	DSU clamps and isolation to the rest of the system are enabled.

Table A4-2 Power mode transition behavior (continued)

Start mode	End mode	DSU behavior	Partner implemented behavior
ON or FUNC_RET	MEM_RET	Waits for all memory transactions to complete. The cluster is removed from system coherency. This mode is only useful when the cluster is the only master active.	DSU clamps and isolation to the rest of the system are enabled.
Any	DEBUG_RECOV	-	-
DEBUG_RECOV	ON	The cluster is brought into coherency with the rest of the system.	Reset is applied, clamps and isolation are disabled.

### A4.5.3 Interlocks between core and DSU P-Channels

To ensure that correct operation is maintained, and to allow a cluster powerdown to be abandoned, there are interlocks between the core and DSU P-Channels:

- If a core P-Channel request is made while the DSU is not in an ON or FUNC\_RET mode, the core request stalls until the DSU has reached the appropriate mode.

————— **Note** —————

If the DSU is in the MEM\_RET or OFF mode, the power controller must transition the DSU to the ON mode to avoid deadlock when signaling a core powerup request.

- If the DSU is requested to go to MEM\_RET or OFF while not all cores are OFF, the request is denied.
- If the DSU is in the process of transitioning from ON to OFF (particularly when flushing the L3 cache which can take a long time) and a core is requested to leave the OFF mode, the L3 cache flush is abandoned and the DSU P-Channel request is denied.

### A4.5.4 Power mode encoding

The power mode is encoded on the CLUSTERPSTATE P-channel bus.

The following table shows the encoding of the power mode.

**Table A4-3 Cluster power domain CLUSTERPSTATE values**

Power mode	CLUSTERPSTATE Value	Logic	Snoop filter RAM	L3 RAM ways 0-3	L3 RAM ways 4-7	L3 RAM ways 8-11	L3 RAM ways 12-15
FULL_ON	0b1001000	Powered up	Powered up	Powered up	Powered up	Powered up	Powered up
¾ ON	0b0111000				Powered down	Powered down	Powered down
½ ON	0b0101000						
¼ ON	0b0011000						
SFONLY ON	0b0001000			Powered down	Powered down	Powered down	Powered down
FULL_FUNC_RET	0b1000111		Retention	Retention	Retention	Retention	Retention
¾ FUNC_RET	0b0110111				Powered down	Powered down	Powered down
½ FUNC_RET	0b0100111						
¼ FUNC_RET	0b0010111						
SFONLY FUNC_RET	0b0000101			Powered down	Powered down	Powered down	Powered down
FULL_MEM_RET	0b1000010	Powered down	Retention	Retention	Retention	Retention	Retention
¾ MEM_RET	0b0110010				Powered down	Powered down	Powered down
½ MEM_RET	0b0100010						
¼ MEM_RET	0b0010010						
OFF	0b0000000		Powered down	Powered down	Powered down	Powered down	Powered down
FULL_DEBUG_RECOV	0b1001010	Powered up or down	Powered up or retention	Powered up or retention	Powered up or retention	Powered up or retention	Powered up or retention
¾ DEBUG_RECOV	0b0111010				Powered down	Powered down	Powered down
½ DEBUG_RECOV	0b0101010						
¼ DEBUG_RECOV	0b0011010						
SFONLY_DEBUG_RECOV	0b0001010						

## A4.6 Power operating requirements

The DSU power operating requirements are indicated to the power controller by asserting bits on the **CLUSTERACTIVE** bus.

The meaning of each bit is described in the following table.

**Table A4-4 L3 power domain CLUSTERACTIVE bit positions**

PACTIVE bit	Power operating requirement	Description
[19]	Cache ways 12-15	Indicates the required mode of the cache way RAMs.  <b>0</b> Cache ways are not required and can be requested to power down. <b>1</b> Cache ways are required to be active.
[18]	Cache ways 8-11	
[17]	Cache ways 4-7	
[16]	Cache ways 0-3	
[8]	On	DSU logic and RAMs are required to be powered up.
[7]	Functional retention	DSU logic is active, RAMs can be put into retention.
[2]	Memory retention	DSU logic can be off, RAMs required to be retained.
[0]	Off	DSU logic and RAMs can be powered down.

The following table shows how the **CLUSTERACTIVE** bit combinations are mapped to power modes.

**Table A4-5 L3 memory system power domain requested modes**

PACTIVE bit								Requested mode
[19]	[18]	[17]	[16]	[8]	[7]	[2]	[0]	
Cache ways 12-15	Cache ways 8-11	Cache ways 4-7	Cache ways 0-3	On	Functional retention	Memory retention	Off	
1	X	X	X	1	X	X	X	FULL_ON
0	1	X	X	1	X	X	X	$\frac{3}{4}$ ON
0	0	1	X	1	X	X	X	$\frac{1}{2}$ ON
0	0	0	1	1	X	X	X	$\frac{1}{4}$ ON
0	0	0	0	1	X	X	X	SFONLY ON
1	X	X	X	0	1	X	X	FULL_FUNC_RET
0	1	X	X	0	1	X	X	$\frac{3}{4}$ FUNC_RET
0	0	1	X	0	1	X	X	$\frac{1}{2}$ FUNC_RET
0	0	0	1	0	1	X	X	$\frac{1}{4}$ FUNC_RET
0	0	0	0	0	1	X	X	SFONLY FUNC_RET
1	X	X	X	0	0	1	X	FULL_MEM_RET
0	1	X	X	0	0	1	X	$\frac{3}{4}$ MEM_RET
0	0	1	X	0	0	1	X	$\frac{1}{2}$ MEM_RET
0	0	0	1	0	0	1	X	$\frac{1}{4}$ MEM_RET
X	X	X	X	0	0	0	X	OFF

## A4.7 Wait For Interrupt and Wait For Event

To reduce dynamic power, each core can request entry in to a low-power state using the *Wait-For-Interrupt* (WFI) and *Wait-For-Event* (WFE) instructions.

In the low-power state, most of the clocks in a core are disabled while keeping the core powered up. This reduces the power drawn to the static leakage current, leaving a small clock power overhead to enable the core to wake up.

In addition to the per-core WFI and WFE low-power states, the clock to almost all the SCU and L3 logic is automatically disabled when the cluster is sufficiently idle.

A WFI or WFE instruction completes when:

- All outstanding load instructions are completed.
- All store instructions are completed.
- All cache and TLB maintenance operations are completed.
- All bus traffic to the L3 is completed.

While a core is in the low-power state, the clocks in the core are temporarily enabled under the following conditions:

- A snoop request from L3 that must be serviced by the L1 or L2 data caches.
- A cache or TLB maintenance operation that must be serviced by the core L1 caches or TLB.
- An APB access to the debug or trace registers residing in the core power domain.
- An access request from the GIC distributor to the GIC CPU interface.

While the clocks in the core are temporarily enabled, the core remains in the WFI or WFE low-power state.

### WFE wake-up event signaling

- A *Send Event* (SEV) instruction signals a WFE wake-up event to other clusters by asserting the **EVENTOREQ** output.
- The **EVENTIREQ** input indicates that another cluster or system component has signaled a WFE wake-up event.

### System global exclusive monitor signaling

Any global exclusive monitor in the system must be capable of generating an event when it is cleared. This event must be signaled to the cluster using the **EVENTIREQ** input.

## A4.8 Clock, voltage, and power domains

The DynamIQ cluster microarchitecture supports multiple clock, voltage, and power domains.

The number of domains that are implemented depends on the choices made by the SoC implementer. There might be fewer in your SoC.

The following diagram shows the clock, voltage, and power domains supported by the DSU and cores.

- Voltage domains are indicated by dashed outlines.
- Blocks that are in the same power domain have the same color.

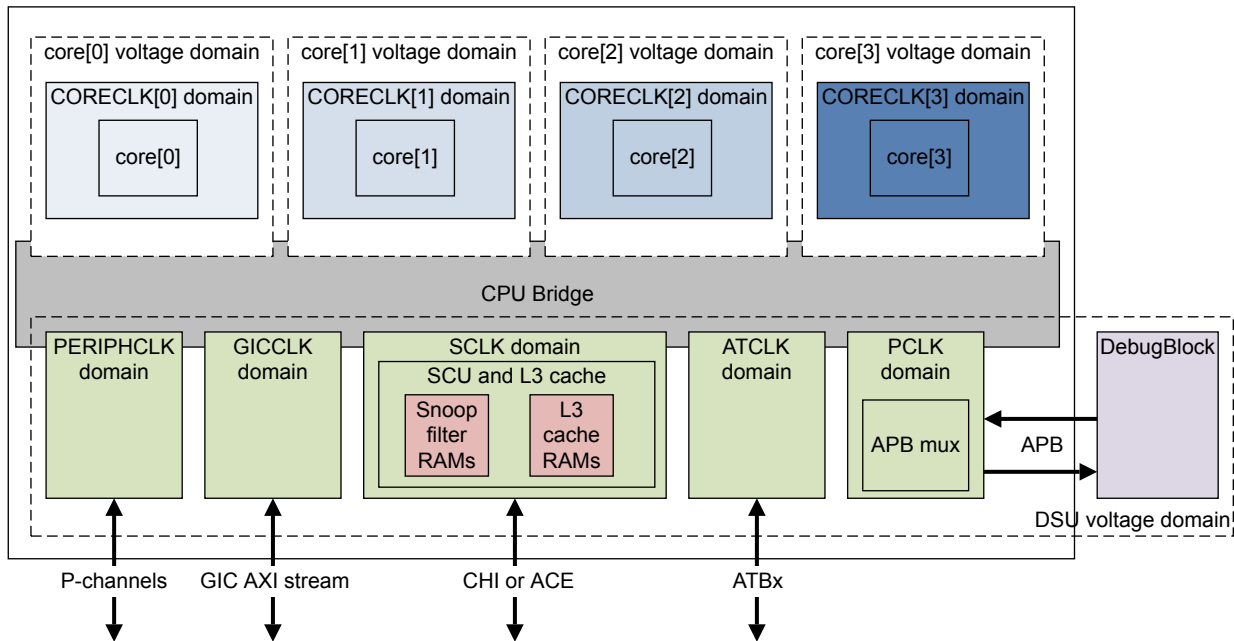


Figure A4-2 DSU Clock, voltage, and power domains

### Clock domains

Each core can be implemented in a separate clock domain. The DSU has multiple clock domains.

The CPU Bridge contains all asynchronous bridges for crossing clock domains, and is split with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. Each core can be implemented with or without an asynchronous bridge. If the asynchronous bridge is not implemented, the core is in the SCLK clock domain.

The DebugBlock can be implemented in the PCLK domain. However, the DebugBlock might be implemented in a different domain. In this case, asynchronous bridges must be implemented on the APB interfaces between the DebugBlock and the cluster.

Each clock domain, except the **PERIPHCLK** domain and **CORECLK** domains, has an associated Q-Channel, which allows the DSU to request the external clock controller to gate the clock on or off.

### Voltage domains

Each core can be implemented in a separate voltage domain. The DSU has a single separate voltage domain, allowing, for example, the DSU to be in the same voltage domain as the SoC interconnect and other system components.

## Power domains

Each core can be implemented in one, or more, separate power domains.

Additional power domains that can be implemented include:

- L3 cache RAM portions.
- SCU.
- DebugBlock.

## A4.9 Cluster powerdown

The cluster is taken out of coherence with the interconnect automatically when it is powered down. No software sequence is required.

After receiving the request to enter power off mode from the power controller, the DSU performs L3 cache flushing, and communication with the interconnect to disable snoops into the cluster. All cores must be in the OFF mode before the cluster is powered down.

### Note

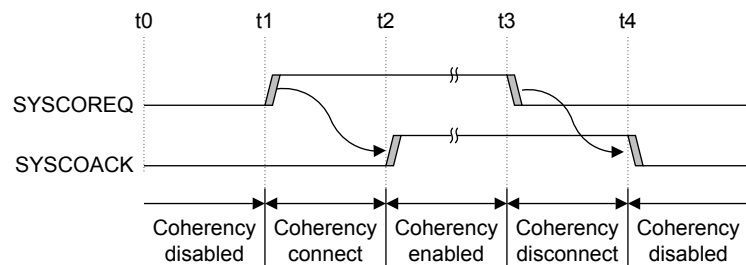
To support automated removal from coherency, the interconnect must support the **SYSCOREQ** and **SYSCOACK** handshake protocol. If not, the SoC is responsible for programming the interconnect to remove the cluster from coherency.

### A4.9.1 Transitioning in and out of coherency

The *DynamIQ Shared Unit* (DSU) provides a hardware mechanism for taking the cluster in and out of coherence with the system interconnect. The cluster enables coherency during powerup and disables it during powerdown.

The system interconnect can use signals, **SYSCOREQ**, and **SYSCOACK**, to take the cluster in and out of coherence. If the system interconnect supports these signals, they can be connected directly. If the system interconnect does not support these signals, ARM recommends that they are connected to the power controller. In this case, the power controller must take any actions necessary to make the transition.

The following diagram shows the timing of **SYSCOREQ**, and **SYSCOACK**.



**Figure A4-3 SYSCOREQ SYSCOACK four-phase coherency handshake**

To enable coherency, the cluster always asserts **SYSCOREQ** during powerup. When the system interconnect has enabled coherency, it asserts **SYSCOACK** and can then start sending snoop requests to the cluster. The cluster accepts snoop requests whenever either signal is asserted.

The cluster disables coherency during powerdown. The cluster deasserts **SYSCOREQ**, and waits for the system interconnect to deassert **SYSCOACK**. The system interconnect must not deassert **SYSCOACK** until it can guarantee that: there are no further snoop requests to be sent, and that all snoop requests it has already sent have fully completed.

The signals must obey the following four-phase handshake rules:

- **SYSCOREQ** can only change when **SYSCOACK** is at the same level.
- **SYSCOACK** can only change when **SYSCOREQ** is at the opposite level.

### Coherency signals naming convention

The *DynamIQ Shared Unit* (DSU) supports a single CHI interface or up to two ACE interfaces. Each set of coherency signals has a unique suffix.

The coherency signals are named as follows:



**CHI**

**SYSCOREQ and SYSCOACK.**

**ACE master 0**

**SYSCOREQM0 and SYSCOACKM0.**

**ACE master 1**

**SYSCOREQM1 and SYSCOACKM1.**



# Chapter A5

## L3 Cache

This chapter describes the L3 cache.

It contains the following sections:

- *A5.1 About the L3 cache* on page A5-60.
- *A5.2 L3 cache allocation policy* on page A5-61.
- *A5.3 Cache stashing* on page A5-62.
- *A5.4 L3 cache ECC and parity* on page A5-63.
- *A5.5 L3 cache data RAM latency* on page A5-66.
- *A5.6 L3 cache slices* on page A5-68.

## A5.1 About the L3 cache

The L3 cache is shared by all the cores in the cluster.

The cache supports stashing requests from the ACP and CHI interfaces.

ECC protection is optionally supported.

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**Note**

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- On powerdown, the DSU automatically performs cache cleaning, eliminating the need for software controlled cache cleaning.
  - The ACE master interface does not support cache stashing.
-

## A5.2 L3 cache allocation policy

The L3 cache data allocation policy changes depending on the pattern of data usage.

Exclusive allocation is used when data is allocated in only one core. Inclusive allocation is used when data is shared between cores.

For example, an initial request from core 0 allocates data in the L1 or L2 caches but is not allocated in the L3 cache. When data is evicted from core 0, the evicted data is allocated in the L3 cache. The allocation policy of this cache line is still exclusive. If core 0 refetches the line, it is allocated in the L1 or L2 caches of core 0 and removed from the L3 cache, keeping the line exclusive. If core 1 then accesses the line for reading, it remains cached in core 0 and is also allocated in both core 1 and L3 caches. In this case, the line has inclusive allocation.

## A5.3 Cache stashing

Cache stashing is the ability of an external agent to request that a line is brought in (or stashed) to a cache in the cluster.

Cache stashing can be performed over the ACP interface, or the CHI master interface. Stash requests target the L3 cache.

On the CHI interface, all types of stash snoops are supported. The cluster always attempts to allocate a stash request. However, if it is heavily loaded and does not have any free buffers, it drops the stash request to avoid a potential system deadlock.

## A5.4 L3 cache ECC and parity

*Error Correcting Code* (ECC) and parity protection is optionally supported on L3 cache RAM instances.

The ECC algorithm that is used is *Single Error Correct, Double Error Detect* (SECCDED). It allows detection and correction of any 1-bit error, and detection of any 2-bit error in all protected RAMs.

If the L3 cache is implemented with ECC, it is applied to the RAMs as follows:

- SECCDED ECC on the L3 data RAMs, per 64-bit.
- SECCDED ECC on the L3 tag RAMs, per entry.
- SECCDED ECC on the snoop filter RAMs, per entry.

Some RAMs, for example the victim selection RAMs, are not protected. In these RAMs errors have no functional effects, only a minor change in performance.

### Error Correction

When a recoverable error is detected in the L3 cache data RAMs, the data is corrected inline before returning to the requestor.

When a recoverable error is detected in the L3 cache tag RAMs or the snoop filter RAMs the following correction mechanism is used:

- The value is corrected and written back to the source address (Read-Correct-Write).
- The lookup is replayed.

The DSU has limited support for hard error correction. A hard error is a physical error in the RAM that prevents the correct value being written. A single hard error can be corrected, but if there are multiple hard errors then in some cases this can cause live-locks as the line could continuously replay.

### Uncorrectable Errors and Data Poisoning

If an error is detected as having two bits in error in a RAM protected by ECC, the error is not correctable. The behavior in the event of an uncorrectable error depends on the type of RAM as follows:

#### Data RAM

When an uncorrectable error is detected in an L3 data RAM, the chunk of data with the error is marked as poisoned. This poison information is then transferred with the data and stored in the cache if the data is allocated back into a cache. The poison is stored per 64 bits of data. If the interconnect supports poisoning, the poison is passed along with the data when the line is evicted or snooped from the cluster. No abort is generated when a line is poisoned, as the abort can be deferred until the point when the poisoned data is consumed by a load or instruction fetch. If a poisoned cache line is evicted or snooped from the cluster, and the interconnect does not support poisoning, the DSU generates an interrupt, **nERRIRQ**, to notify software that data has potentially been lost. Software can indicate if the interconnect supports poisoning or not by setting the Interconnect data poisoning support bit in the cluster Extended Control Register.

#### Data tag RAM

When an uncorrectable error is detected in an L3 tag RAM, then either the address or coherency state of the line is unknown, so the data cannot be poisoned. In this case, the line is invalidated and the DSU generates an interrupt, **nERRIRQ**, to notify software that data has potentially been lost.

## Snoop filter tag RAM

When an uncorrectable error is detected in a snoop filter tag RAM, either the address or coherency state of the line is unknown, so the data cannot be poisoned. In this case, the snoop filter entry is invalidated, but the line remains present in one or more of the cores. The DSU generates an interrupt, **nERRIRQ**, to notify software that data has potentially been lost. Because the core caches and the snoop filter are inconsistent after the error, this can lead to unpredictable behavior. The effect of the error depends on the type of core, but it could result in further data corruption, or deadlocks. Therefore it is generally not possible to cleanly recover from such an error. ARM recommends that, in response to the interrupt, a system reset is performed as soon as possible.

## Error reporting

Any error that is detected is reported in the *Error Record Primary Syndrome Register* (ERXSTATUS\_EL1), and the *Error Record Miscellaneous Register* (EXXMISC0\_EL1). Errors reported include errors that are successfully corrected, and errors that cannot be corrected. If multiple errors occur on the same clock cycle, only one error is reported, but the OF (overflow) bit is set.

There are two error records provided, which can be selected with the ERRSELR\_EL1 register. Record 0 is private to the core, and is updated on any error in the core RAMs including L1 caches, TLB, and L2 cache. Record 1 is for the cluster, and is shared between all cores in the cluster, and records any error in the L3 and snoop filter RAMs.

If enabled in the ERXCTLR\_EL1 register, all errors that are detected cause a fault handling interrupt to be generated on the **nFAULTIRQ[0]** pin (for L3 and snoop filter errors) or on the **nFAULTIRQ[n+1]** pin (for core n L1 and L2 errors).

Errors that cannot be corrected, and therefore might result in data corruption, also cause an abort or error handling interrupt. This allows software to be alerted to an error so that it can either attempt to recover or can restart the system. Some errors can be deferred by poisoning the data. These errors do not cause an abort at the time of the error, but only when the error is consumed.

- Uncorrectable errors in the L3 data RAMs when read by a core might result in a precise or imprecise Data Abort or Prefetch Abort, depending on the implementation of core.
- Uncorrectable errors in the L3 data RAMs when the line is being evicted from a cache, cause the data to be poisoned. The eviction might be because of a natural eviction, a linefill from a higher level of cache, a cache maintenance operation, or a snoop. If the poisoned line is evicted from the cluster for any reason, and the interconnect does not support data poisoning, the **nERRIRQ[0]** pin is asserted.
- Uncorrectable errors in the L1 tag or dirty RAMs, or in the L2 tag RAMs, causes the **nERRIRQ[n+1]** pin to be asserted for core<n>.
- Uncorrectable errors in the L3 tag RAMs or SCU snoop filter RAMs causes the **nERRIRQ[0]** pin to be asserted.

ARM recommends that the **nERRIRQ** pins are connected to the interrupt controller, so that an interrupt or system error is generated when the pin is asserted.

The fault and error interrupt pins can be cleared by writing to the ERXSTATUS(\_EL1) registers.

When a dirty cache line with an error on the data RAMs is evicted from the core, the write on the master interface still takes place. However, if the error is uncorrectable then:

- On ACE, the uncorrected data is written.
- On CHI, the uncorrected data is written but the data poison field indicates that there is a data error.

When a snoop hits on a line with an uncorrectable data error, the data is returned (if the snoop requires the data), and:

- On ACE, the **nERRIRQ[0]** pin is asserted.



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**Note**

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The snoop response does not indicate the error.

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- On CHI, the snoop response indicates that either the data is poisoned (if supported), or that there is an error.

If a snoop hits on a tag that has an uncorrectable error, it is treated as a snoop miss. This is because the error means that it is unknown whether the cache line is valid.

In some cases, it is possible for an error to be counted more than once. For example, multiple accesses might read the location with the error before the line is evicted.

**Related references**

*[Chapter B1 Control registers on page B1-105.](#)*

## A5.5 L3 cache data RAM latency

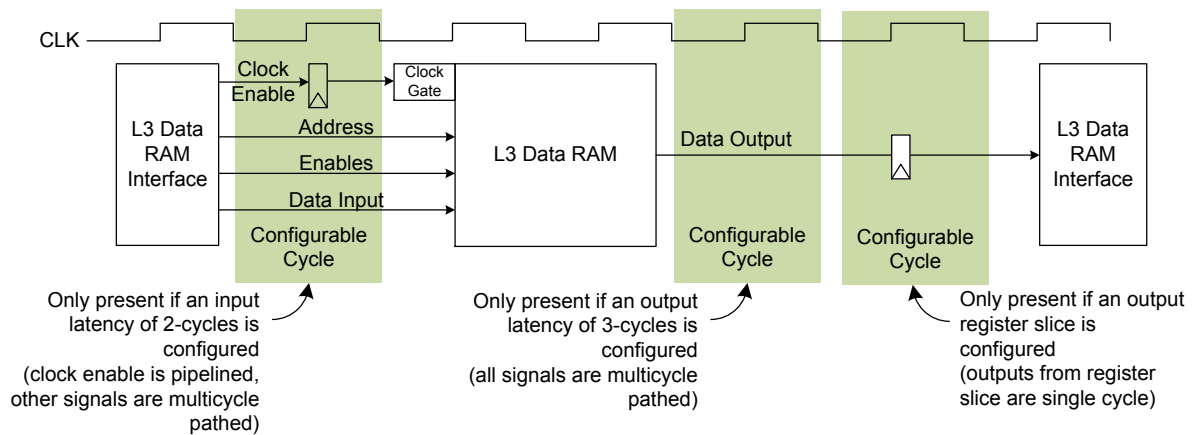
The L3 data RAM interface can be implemented with additional latency on the input and output paths.

The following options are independent of one another:

- Either a 1-cycle (the default) or 2-cycle latency on the input path to the L3 data RAMs.
- Either a 2-cycle (the default) or 3-cycle latency on the output path from the L3 data RAMs.
- An optional register slice on the output of the level-3 data RAMs.

On the input paths, if a 2-cycle latency is requested the RAM clock enable is pipelined and a multicycle path is applied to all other RAM input signals.

The following diagram shows the L3 data RAM timing.



**Figure A5-1 L3 cache data RAM latency**

On the output paths, both a 2-cycle latency and a 3-cycle latency applies a multicycle path to all RAM output signals. The output of the register slice is never multicycle pathed.

The following table describes the impact on L3 data RAM performance with the different latency configurations:

**Table A5-1 L3 data RAM performance with different latency configurations**

Configuration	L3 hit latency cycles	L3 lookup bandwidth
Input, 1-cycle; Output 2-cycles	3	Access every two clock cycles
Input, 1-cycle; Output 3-cycles	4	Access every three clock cycles
Input, 1-cycle; Output 2-cycles; register slice	4	Access every two clock cycles
Input, 1-cycle; Output 3-cycles; register slice	5	Access every three clock cycles
Input, 2-cycles; Output 2-cycles	4	Access every two clock cycles
Input, 2-cycles; Output 3-cycles	5	Access every three clock cycles
Input, 2-cycle; Output 2-cycles; register slice	5	Access every two clock cycles
Input, 2-cycle; Output 3-cycles; register slice	6	Access every three clock cycles

The L1 and L2 cache-miss to L3 cache-hit latency increases with more latency on the RAMs. The additional latency degrades performance. However, if the output latency is set to 3-cycles, the decrease in throughput to one access every three core clock cycles is possibly more significant as the memory system

could begin to back up if there are a series of L3 data RAM accesses close together. The three cycle output latency option should only be used if the RAM cannot meet the timing requirement of two cycles latency. The register slice should be used instead if the wire routing delay from the RAM to the SCU logic cannot meet timing.

## A5.6 L3 cache slices

The L3 cache is implemented in either one or two slices.

When two slices are implemented, there are two sets of tag RAMs and two sets of data RAMs. Requests are allocated to a particular slice based on the address of the request. Splitting the cache into slices improves the physical floorplan when implementing the macrocell, particularly for larger cache sizes, and also gives increased bandwidth because the two slices can be accessed in parallel.

The number of slices implemented is determined by the DSU configuration.

Two slices are implemented when any of the following configuration options are chosen:

- More than four LITTLE cores are configured.
- One or more big cores are configured.
- The L3 cache size is greater than 1MB.
- A second ACE master port is configured.
- A 256-bit CHI master port is configured.

A single slice is implemented for all other configurations.

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**Note**

If a 512KB cache is configured, then a single slice is always used, even if any of the above conditions are chosen.

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# Chapter A6

## ACE Master Interface

This chapter describes the ACE master memory interface.

It contains the following sections:

- *A6.1 About the ACE master interface* on page A6-70.
- *A6.2 ACE configurations* on page A6-71.
- *A6.3 ACE features* on page A6-72.
- *A6.4 ACE master interface attributes* on page A6-73.
- *A6.5 ACE channel properties* on page A6-75.
- *A6.6 ACE transactions* on page A6-76.
- *A6.7 Read response* on page A6-78.
- *A6.8 Write response* on page A6-79.
- *A6.9 Barriers* on page A6-80.
- *A6.10 AXI compatibility mode* on page A6-81.
- *A6.11 ACE privilege information* on page A6-82.

## A6.1 About the ACE master interface

You can configure the DynamIQ Shared Unit to use the ACE protocol for the master memory interface.

### A6.1.1 Dual ACE interfaces

The DSU can be implemented with one or two ACE interfaces. Two interfaces give greater bandwidth for memory transactions.

Transactions generated by the cluster are routed to either interface based on the transaction type, memory type, and transaction address:

- All DVM transactions are routed to interface 0.
- All Device and Normal Non-Cacheable transactions are routed to interface 0.
- All Cacheable transactions use bit [6] of the transaction address to determine which interface is used. If bit [6] is 0, then interface 0 is used, otherwise interface 1 is used.

When the external memory system sends snoops, it must either:

- Send the snoop to both interfaces.
- Send the snoop only to the interface that is relevant for the address of that snoop. This behavior is normal operation for an external memory system that contains a snoop filter. The snoop filter indicates that the line is present in one of the two masters.

The second method is more efficient, and if two masters are implemented, ARM recommends that the external memory system includes a snoop filter.

#### DVM messages

DVM messages can be received on both interfaces, however they are only required on interface 0, and any DVM message sent to interface 1 is treated as a no-op. Therefore for best performance, ARM recommends that, when possible, your interconnect is configured to avoid sending DVM messages to interface 1.

## A6.2 ACE configurations

The following table shows the supported ACE configurations.

**Table A6-1 Supported ACE configurations**

Signal	Feature			
	ACE non-coherent		ACE coherent	
	With no cache or invisible system cache	With visible system cache	With no cache or invisible system cache	With visible system cache
<b>BROADCASTCACHEMAINT</b>	0	1	0	1
<b>BROADCASTOUTER</b>	0	0	1	1

**Note**

- ACE non-coherent mode, no system cache, can be used to connect to an AXI interconnect.
- A visible system cache requires cache maintenance transactions to ensure that a write is visible to all observers.
- An invisible system cache is one that does not require cache maintenance transactions to ensure that a write is visible to all observers. This is true even if those observers use different memory attributes.

The following table shows the key features in each of the supported ACE configurations.

**Table A6-2 Supported features in the ACE configurations**

Features	DSU Configuration		
	ACE non-coherent No system cache	ACE non-coherent System cache	ACE coherent
AXI3 or AXI4 interconnect compliance	Yes	No	No
ACE interconnect compliance	Yes	Yes	Yes
Barriers on AR and AW channels	No	No	No
Cache maintenance requests on AR channel	No	Yes	Yes
Snoops on AC channel	No	No	Yes
Coherent requests on AR or AW channel	No	No	Yes
DVM requests on AR channel	No	No	Yes

## A6.3 ACE features

AMBA defines a set of interface properties for the ACE interconnect. The following table shows which of these properties the DSU supports, or requires the cluster interconnect and system to support.

**Table A6-3 ACE interconnect properties for the DSU**

ACE property	Supported by the DSU	Interconnect support required
Continuous_Cache_Line_Read_Data	Not applicable	Yes
Multi_Copy_Atomicity	Yes	Yes
Ordered_Write_Observation	Not applicable	No
WriteEvict_Transaction	Yes if CLUSTERECTLR Cache UniqueClean eviction control is programmed to 1.	Yes if CLUSTERECTLR Cache UniqueClean eviction control is programmed to 1.
DVM_v8	Yes	Yes if <b>BROADCASTOUTER</b> is HIGH.
Atomic_Transactions	No	No
DVM_v8.1	Yes	Yes if <b>BROADCASTOUTER</b> is HIGH.
Cache_Stash_Transactions	No	No
DeAllocation_Transactions	No	No
Persistent_CMO	No	No
Poison	No	No
Data_Check	No	No
QoS_Accept	No	No
Trace_Signals	No	No
Loopback_Signals	No	No
Low_Power_Signals	Yes	Yes
Untranslated_Transactions	No	No
NSAccess_Identifiers	No	No



## A6.4 ACE master interface attributes

This section describes the read and write issuing capabilities and ID encoding

The following table lists the read and write issuing capabilities.

**Table A6-4 ACE master interface attributes**

Attribute	Value	Comments
Write issuing capability	Configuration dependent	<p>The maximum number of writes is:</p> <ul style="list-style-type: none"> <li>96, if two slices are present.</li> <li>32, if one slice is present.</li> </ul> <p>See <a href="#">A5.6 L3 cache slices on page A5-68</a>.</p> <p>Device and Normal Non-Cacheable transactions are limited to a total of 15 write transactions by default. This value can be used by system components to size buffers when bridging to other interface protocols, for example PCIe. Normal Non-Cacheable transactions can be removed from this limit by setting the control bit in the CLUSTERECTLR. See <a href="#">B1.8 CLUSTERECTLR, Cluster Extended Control Register on page B1-116</a>.</p>
Read issuing capability	Configuration dependent	<p>The maximum number of reads is:</p> <ul style="list-style-type: none"> <li>98, if two slices are present.</li> <li>34, if one slice is present.</li> </ul> <p>————— <b>Note</b> —————</p> <p>Two part <i>Distributed Virtual Memory</i> (DVM) messages use the same ID for both parts, and therefore can have two outstanding transactions on the same ID.</p> <p>—————</p>
Exclusive access thread capability	Number of hardware threads	Each hardware thread can have 1 exclusive access sequence in progress.
Write ID capability	Configuration dependent	<p>The maximum write ID capability is:</p> <ul style="list-style-type: none"> <li>96, if two slices are present.</li> <li>32, if one slice is present.</li> </ul> <p>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</p>
Write ID width	8	The ID encodes the source of the memory transaction. See the Encodings for <b>AWIDM0[7:0]</b> table.
Read ID capability	Configuration dependent	<p>The maximum read ID capability is:</p> <ul style="list-style-type: none"> <li>98, if two slices are present.</li> <li>34, if one slice is present.</li> </ul> <p>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</p> <p>Two part DVMs use the same ID for both parts, and therefore can have two outstanding transactions on the same ID.</p>
Read ID width	9	The ID encodes the source of the memory transaction. See the Encodings for <b>ARIDM0[8:0]</b> table.

The following table shows the encodings for **AWIDM0[7:0]**, **WIDM0[7:0]**. When two ACE masters are configured, the maximum number of reads and writes are unchanged. The reads and writes can be distributed between the two masters, or all send to one of the masters, depending on the memory type and address.

**Table A6-5 Encodings for AWIDM0[7:0] and WIDM0[7:0]**

Attribute	Value	Issuing capability per ID	Comments
Write ID	0b000t0nnn	1	Core nnn <sup>a</sup> , thread t <sup>b</sup> , system domain store exclusives (except for those that are Device non-reorderable).
	0b001t0nnn	15	Core nnn <sup>a</sup> thread t <sup>b</sup> , non-reorderable Device writes.
	0b1xxxxxxx <sup>c</sup>	1	All other types of write.
	Other encodings	-	Not used

The following table shows the Encodings for **ARIDM0[8:0]**.

**Table A6-6 Encodings for ARIDM0[8:0]**

Attribute	Value	Issuing capability per ID	Comments
Read ID	0b0000t0nnn	1	Core nnn <sup>a</sup> , thread t <sup>b</sup> , system domain load exclusives (except for those that are Device non-reorderable).
	0b0001t0nnn	17	Core nnn <sup>a</sup> , thread t <sup>b</sup> , non-reorderable Device reads.
	0b001000000	1	DVM Sync
	0b001000001	256	DVM Complete
	0b01xxxxxxx <sup>c</sup>	1	All other types of read
	0b1xxxxxxx <sup>c</sup>		
	Other encodings	-	Not used

#### Note

These ID and transaction details are provided for information only. ARM strongly recommends that all interconnects and peripherals are designed to support any type and number of transactions on any ID, to ensure compatibility with future products.

For more information about the ACE and AXI signals described in this manual, see the *ARM® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*.

#### Related references

[A5.6 L3 cache slices on page A5-68.](#)

<sup>a</sup> nnn is the core number 0b000-0b111 in binary.  
<sup>b</sup> t is the hardware thread number and is 0 if the core does not support multiple hardware threads.  
<sup>c</sup> x is a do not care value, can be 0 or 1.

## A6.5 ACE channel properties

The following table shows the properties of the ACE channels.

**Table A6-7 ACE channel properties**

Property	Value	Comment
Snoop acceptance capability	9	The SCU can accept and process a maximum of nine snoop requests from the system. It counts requests from the request being accepted on the AC channel to the response being accepted on the CR channel.
Snoop latency	Hit	When there is a hit in L3 cache, the best case for response and data is 10 <b>SCLK</b> cycles. When there is a miss in the L3 cache but a hit in an L1 or L2 cache in a core, then the latency varies depending on the type and configuration of the core.  ————— <b>Note</b> ————— Latencies can be higher if hazards occur or if there are not enough buffers to absorb requests. —————
	Miss	Best case six <b>SCLK</b> cycles when the snoop filter and L3 cache tags indicate the miss.
	DVM	The cluster takes a minimum of six <b>SCLK</b> cycles to provide a response to DVM packets.
Snoop filter	Supported	The cluster provides support for an external snoop filter in an interconnect. It indicates when clean lines are evicted from the cluster by sending Evict transactions on the write channel.  However there are some cases that can prevent an Evict transaction from being sent. Therefore you must ensure that you build any external snoop filter to handle a capacity overflow. When exceeding capacity, the snoop filter should send a back-invalidation to the cluster.  Examples of cases where evicts are not produced include: <ul style="list-style-type: none"> <li>• Linefills that take external aborts.</li> <li>• Store exclusives that fail.</li> <li>• Mis-matched aliases.</li> </ul>
Supported transactions	-	All transactions described by the ACE protocols: <ul style="list-style-type: none"> <li>• Are accepted on the master interface from the system.</li> <li>• Can be produced on the ACE master interface except: <ul style="list-style-type: none"> <li>— Barriers</li> <li>— MakeInvalid</li> <li>— ReadShared</li> <li>— ReadOnceCleanInvalid</li> <li>— ReadOnceMakeInvalid</li> <li>— StashOnceShared</li> <li>— StashOnceUnique</li> <li>— StashTranslation</li> <li>— WriteUniquePtl.</li> <li>— WriteUniqueFull.<sup>d</sup></li> <li>— WriteUniquePtlStash</li> <li>— WriteUniqueFullStash</li> </ul> </li> </ul>

See the *ARM® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite* for more information about the ACE channel.

<sup>d</sup> The AMBA5 ACE transaction types WriteUniqueFull and WriteUniquePtl were known in AMBA4 ACE-Lite as WriteLineUnique and WriteUnique, respectively.

## A6.6 ACE transactions

The DSU does not generate any FIXED bursts and all WRAP bursts fetch a complete cache line starting with the critical word first. A burst does not cross a cache line boundary.

The cache linefill fetch length is always 64 bytes.

The DSU generates only a subset of all possible ACE transactions on the master interface.

For WriteBack cacheable transfers the supported transfers are:

- WRAP 4 128-bit for read transfers (linefills).
- INCR 4 128-bit for write transfers (evictions).
- INCR N (N:1, 2, or 4) 128-bit write transfers.

For Non-cacheable transactions:

- INCR N (N:1, 2, or 4) 128-bit for write transfers.
- INCR N (N:1, 2, or 4) 128-bit for read transfers.
- INCR 1 32-bit, 64-bit, and 128-bit for read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive read transfers.

For Device transactions:

- INCR N (N:1, 2, or 4) 128-bit read transfers.
- INCR N (N:1, 2, or 4) 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive write transfers.

For translation table walk transactions INCR 1 32-bit, and 64-bit read transfers.

The following points apply to ACE transactions:

- WRAP bursts are only 128-bit size.
- INCR 1 can be any size for read or write.
- INCR burst, more than one transfer, are only 128-bit size.
- No transaction is marked as FIXED.
- Write transfers with none, some, or all byte strobes LOW can occur.

The following table shows the ACE transactions that can be generated, and some typical operations that might cause the transactions to be generated. This is not an exhaustive list of ways to generate each type of transaction, because there are many possibilities.

**Table A6-8 ACE transactions**

Transaction	Operation
ReadNoSnoop	Non-cacheable loads or instruction fetches. Linefills of non-shareable cache lines into L1, L2, or L3 caches.
ReadOnce	Cacheable loads that are not allocating into the cache.
ReadClean	Cache data linefills started by a load instruction, or cache linefills started by an instruction fetch.
ReadNotSharedDirty	Cache data linefills started by a load instruction, or cache linefills started by an instruction fetch.
ReadUnique	Data linefills started by a store instruction.
CleanUnique	Store instructions that hit in the cache but the line is not in a unique coherence state. Store instructions that are not allocating into the caches, for example when streaming writes.
MakeUnique	Store instructions of a full cache line of data, that miss in the caches.

**Table A6-8 ACE transactions (continued)**

<b>Transaction</b>	<b>Operation</b>
CleanShared	Cache maintenance instructions.
CleanSharedPersist	Not used.
CleanInvalid	Cache maintenance instructions.
DVM	TLB and instruction cache maintenance instructions.
DVM Complete	DVM Sync snoops received from the interconnect.
WriteNoSnoop	Non-cacheable store instructions. Evictions of non-shareable cache lines from L1, L2, and L3 caches.
WriteBack	Evictions of dirty lines from the L1, L2, or L3 cache, or streaming writes that are not allocating into the cache.
WriteClean	Evictions of dirty lines from the L3 cache, when the line is still present in an L1 or L2 cache. Some cache maintenance instructions.
WriteEvict	Evictions of unique clean lines, when configured in the CLUSTERECTLR.
Evict	Evictions of clean lines, when configured in the CLUSTERECTLR.
Barriers	Not used.
MakeInvalid	Not used.
ReadShared	Not used.
ReadOnceCleanInvalid	Not used.
ReadOnceMakeInvalid	Not used.
StashOnceShared	Not used.
StashOnceUnique	Not used.
StashTranslation	Not used.
WriteUniquePtl	Not used.
WriteUniqueFull <sup>e</sup>	Not used.
WriteUniquePtlStash	Not used.
WriteUniqueFullStash	Not used.

<sup>e</sup> The AMBA5 ACE transaction types WriteUniqueFull and WriteUniquePtl were known in AMBA4 ACE-Lite as WriteLineUnique and WriteUnique, respectively.

## A6.7 Read response

The ACE master can delay accepting a read data channel transfer by holding **RREADY** LOW for an indeterminate number of cycles.

**RREADY** can be deasserted LOW between read data channel transfers that form part of the same transaction.

The ACE master asserts the read acknowledge signal **RACK** HIGH in the **ACLK** cycle following acceptance of the last read data channel transfer for a transaction. **RACK** is asserted in AXI compatibility mode in addition to ACE configurations.

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### Note

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- For interoperability of system components, ARM recommends that components interfacing with the ACE master are fully ACE compliant with no reliance on the subset of permitted **RACK** behavior described for the DSU.
- If the interconnect does not perform hazarding between coherent and non-coherent requests, then, after it has returned the first transfer of read data for a non-coherent read, it must return all the remaining read transfers in the transaction.

The completion of the read transfers must not depend on snoop requests being sent to the core, or the core needing to respond to a snoop request that could be to the same address.

---

## A6.8 Write response

The ACE master requires that the slave does not return a write response until it has received the write address.

The ACE master always accepts write responses without delay by holding **BREADY** HIGH.

The ACE master asserts the write acknowledge signal **WACK** HIGH in the **ACLK** cycle following acceptance of a write response. **WACK** is asserted in AXI compatibility mode in addition to ACE configurations.

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**Note**

For interoperability of system components, ARM recommends that components interfacing with the ACE master are fully ACE compliant with no reliance on the subset of permitted **BREADY** and **WACK** behavior described for the DSU.

---

## A6.9 Barriers

The DSU does not support sending barrier transactions to the interconnect. Barriers are always terminated within the cluster.

You must ensure that your interconnect and any peripherals connected to it do not return a write response for a transaction until that transaction would be considered complete by a later barrier. This means that the write must be observable to all other masters in the system. ARM expects the majority of peripherals to meet this requirement.



## A6.10 AXI compatibility mode

The DSU implements an AXI compatibility mode that enables you to use the DSU in a standalone environment where the AMBA 5 ACE interface is not required.

To enable this mode, you must ensure that the **BROADCASTOUTER**, **BROADCASTCACHEMAIN**, and **BROADCASTPERSIST** input signals are set to LOW.

The AXI3 protocol supports write interleaving which is not used by the DSU. To allow compatibility with AXI3 components, the DSU provides **WIDMx** output signals, which can be connected to an AXI3 device.

If using AXI4 and ACE components, you must leave the **WIDMx** output signals unconnected as these signals do not exist in these protocols.

For single master implementations, **WIDM0** is provided. For dual master implementations, **WIDM0** and **WIDM1** are provided.

### A6.10.1 Additional logic to support AXI compatibility

To support AXI compatibility, the DSU requires additional logic.

The DSU implements a handshake for system coherency using the **SYSCOREQ\*** and **SYSCOACK\*** signals. In AXI compatibility mode, the DSU does not support coherency, but because this interface uses a handshake protocol, transitions on **SYSCOREQ\*** request must be responded to by a corresponding acknowledge on **SYSCOACK\***.

ARM recommends that you implement the following logic in your system:

- Add a single-bit register with the input connected to **SYSCOREQ\***.
- Connect the output of the register to **SYSCOACK\***.
- The register must be reset LOW, and clocked and reset using the clock and reset from your AXI system.

For single ACE master implementations, **SYSCOREQM0** and **SYSCOACKM0** are provided. For dual ACE master implementations, **SYSCOREQM1** and **SYSCOACKM1** are also provided.

## A6.11 ACE privilege information

ACE provides information about the privilege level of accesses on the **ARPROTM[0]** and **AWPROTM[0]** signals. This information is not available from cores within the cluster. Therefore these signals are always driven to HIGH indicating that the access could be a privileged access.

# Chapter A7

## CHI Master Interface

This chapter describes the AMBA 5 CHI master memory interface.

It contains the following sections:

- *A7.1 About the CHI master interface* on page A7-84.
- *A7.2 CHI features* on page A7-85.
- *A7.3 CHI configurations* on page A7-86.
- *A7.4 Attributes of the CHI master interface* on page A7-87.
- *A7.5 CHI channel properties* on page A7-88.
- *A7.6 CHI transactions* on page A7-89.

## A7.1 About the CHI master interface

You can configure the DSU to use the AMBA 5 CHI protocol for the master memory interface.

## A7.2 CHI features

AMBA defines a set of interface properties for the CHI interconnect. The following table shows which of these properties the DSU supports, or requires the interconnect and system to support.

**Table A7-1 CHI interconnect properties for the DSU**

CHI property	Supported by the DSU	Interconnect support required
Atomic_Transactions	Yes if <b>BROADCASTATOMIC</b> is HIGH.	Yes if <b>BROADCASTATOMIC</b> is HIGH.
Cache_Stash_Transactions	Yes	Yes
Direct_Memory_Transfer	Yes	Optional. The DSU supports this feature if it is implemented by the interconnect.
Direct_Cache_Transfer	Yes	Optional. The DSU supports this feature if it is implemented by the interconnect.
Data_Poison	Yes if cache protection (SCU_CACHE_PROTECTION) is enabled.	Yes if cache protection (SCU_CACHE_PROTECTION) is enabled.
Data_Check	No	No
CCF_Wrap_Order	Yes. The DSU always sends Data packets in critical chunk first wrap order.	No
Req_Addr_Width	44. If a core with a 48-bit physical address width is configured inside the cluster, this is 48.	Not applicable
NodeID_Width	11	Not applicable
Data_Width	User configurable: 128 bits or 256 bits.	Not applicable
Barrier_Transactions	No	No. The DSU does not use these transaction types.
Data return from SC state.	Yes	Not applicable
I/O de-allocation transactions (ROMI and ROCI).	No	No. The DSU does not use these transaction types.
ReadNotSharedDirty transactions	Yes	Yes
CleanSharedPersist transactions	Yes if <b>BROADCASTPERSIST</b> is HIGH.	Yes if <b>BROADCASTPERSIST</b> is HIGH.

For more information on these features, see *ARM® AMBA® CHI Protocol Specification*.

## A7.3 CHI configurations

You can change the coherency configurations to suit your system configuration using the **BROADCASTCACHEMAINT** and **BROADCASTOUTER** input signals.

The following table shows the permitted combinations of these signals and the supported configurations in the DSU, with a CHI bus.

**Table A7-2 Supported CHI configurations**

Signal	Feature			
	CHI non-coherent		CHI coherent	
	With no cache or invisible system cache	With visible system cache	With invisible system cache	With visible system cache
<b>BROADCASTCACHEMAINT</b>	0	1	0	1
<b>BROADCASTOUTER</b>	0	0	1	1

**Note**

- A visible system cache requires cache maintenance transactions to ensure that a write is visible to all observers.
- An invisible system cache is one that does not require cache maintenance transactions to ensure that a write is visible to all observers. This is true even if those observers use different memory attributes.

The following table shows the key features in each of the supported CHI configurations.

**Table A7-3 Supported features in the CHI configurations**

Features	Configuration		
	CHI non-coherent		CHI coherent
	With no cache or invisible system cache	With visible system cache	
Cache maintenance requests on TXREQ channel	No	Yes	Yes
Snoops on RXSNP channel	No	No	Yes
Coherent requests on TXREQ channel	No	No	Yes
DVM requests on TXREQ channel	No	No	Yes

## A7.4 Attributes of the CHI master interface

The following table lists the possible values for the read and write issuing capabilities.

**Table A7-4 Attributes of the CHI master memory interface**

Attribute	Value	Comments
Write issuing capability	Configuration dependent	The maximum number of writes is: <ul style="list-style-type: none"> <li>96, if two slices are present.</li> <li>32, if one slice is present.</li> </ul>
Read issuing capability	Configuration dependent	The maximum number of reads is: <ul style="list-style-type: none"> <li>96, if two slices are present.</li> <li>32, if one slice is present.</li> </ul>
Exclusive hardware access thread capability	Number of hardware threads.	Each hardware thread can have one exclusive access sequence in progress.
Transaction ID width	8 bits	There is no fixed mapping between CHI transaction IDs and cores. Transaction IDs can be used for either reads or writes. <p style="text-align: center;"><b>Note</b></p> The source of the transaction is encoded in the LPID field, see <a href="#">Table A7-6 CHI LPID assignment on page A7-89</a> .
Transaction ID capability	Configuration dependent	The ID capability is: <ul style="list-style-type: none"> <li>96, if two slices are present.</li> <li>32, if one slice is present.</li> </ul> <p style="text-align: center;"><b>Note</b></p> Unlike in an AMBA 5 ACE configuration, there is never any ID reuse in CHI implementations, regardless of the memory type.
NodeID widths	11 bits	-
TXREQFLIT.RSVDC	0 bits	-
TXDATFLIT.RSVDC	0 bits	-
TXDATFLIT.DataCheck	0 bits	-

### Related references

[A5.6 L3 cache slices on page A5-68](#).

## A7.5 CHI channel properties

The following table shows the snoop capabilities and other CHI channel properties for the DSU.

**Table A7-5 CHI channel properties**

Property	Value	Comment
Snoop acceptance capability	11	The SCU can accept and process a maximum of eleven snoop requests from the system.
DVM acceptance capability	4	<p>The SCU can accept and process a maximum of four DVM transactions from the system. Each of these four transactions can be a two part DVM message.</p> <p>The interconnect must be configured to never send more than four DVM messages to the cluster, otherwise the system might deadlock.</p>
Snoop latency	Hit	<p>When there is a hit in L3 cache, the best case for response and data is 10 <b>SCLK</b> cycles. When there is a miss in the L3 cache but a hit in an L1 or L2 cache in a core, then the latency varies depending on the type and configuration of that core.</p> <p>Latencies can be higher if hazards occur or if there are not enough buffers to absorb requests.</p>
	Miss	Best case for latency is six <b>SCLK</b> cycles when the snoop filter and L3 cache tags indicate the miss.
	DVM	The cluster takes a minimum of six <b>SCLK</b> cycles to provide a response to DVM packets.
Snoop filter	Supported	<p>The cluster provides support for an external snoop filter in an interconnect. It indicates when clean lines are evicted from the cluster by sending Evict transactions on the CHI write channel.</p> <p>However there are some cases that can prevent an Evict transaction from being sent. Therefore you must ensure that you build any external snoop filter to handle a capacity overflow. When exceeding capacity, the snoop filter should send a back-invalidation to the cluster.</p> <p>Examples of cases where evicts are not produced include:</p> <ul style="list-style-type: none"> <li>• Linefills that take external aborts.</li> <li>• Store exclusives that fail.</li> <li>• Mis-matched aliases.</li> </ul>
Supported transactions	-	<p>All transactions that are described by the CHI protocol:</p> <ul style="list-style-type: none"> <li>• Are accepted on the CHI master interface from the system.</li> <li>• Can be produced on the CHI master interface except: <ul style="list-style-type: none"> <li>— ReadShared.</li> <li>— MakeInvalid.</li> <li>— EOBarrier.</li> <li>— ECTBarrier.</li> <li>— WriteCleanPtl.</li> <li>— WriteUniquePtl.</li> <li>— WriteBackPtl.</li> <li>— WriteUniqueFullStash.</li> <li>— WriteUniquePtlStash.</li> <li>— ReadOnceCleanInvalid.</li> <li>— ReadOnceMakeInvalid.</li> </ul> </li> </ul>



## A7.6 CHI transactions

CHI transactions are sent to a specific node in the interconnect that is based on the following criteria:

- Type of access.
- Address of the access.
- Settings of the System Address Map.

Addresses that map to an HN-F node can be marked as cacheable memory in the translation tables, and can take part in the cache coherency protocol. Addresses that map to an HN-I or MN must be marked as device or non-cacheable memory.

CHI TXREQ transactions include the *Logical Processor ID* (LPID) field. This field uniquely identifies the logical core that generated the request transaction. The following table shows CHI LPID assignment.

**Table A7-6 CHI LPID assignment**

LPID	Description
0x0-0xF	Bits [3:0] are encoded: [0] Thread number. [3:1] CPUID.
0x10-0x1D	Reserved.
0x1E	ACP request.
0x1F	Cache copy back.

**Table A7-7 CHI transaction types**

Transaction	Operation
ReadNoSnp	Non-cacheable loads or instruction fetches. Linefills of Non-shareable cache lines into L1, L2, or L3 caches.
ReadOnce	Cacheable loads that are not allocating into the cache.
ReadClean	Cache data linefills started by a load instruction, or cache linefills started by an instruction fetch.
ReadShared	Not used.
ReadNotSharedDirty	Cache data linefills started by a load instruction, or cache linefills started by an instruction fetch.
ReadUnique	Cache data linefills started by a store instruction.
CleanUnique	Store instructions that hit in the cache but the line is not in a unique coherence state.
MakeUnique	Store instructions of a full cache line of data, that miss in the caches.
CleanShared	Cache maintenance instructions.
CleanSharedPersist	Cache maintenance instructions. This is only generated by the <i>Data Cache Clean to the Point of Persistence</i> (DC CVAP) cache maintenance instruction when the <b>BROADCASTPERSIST</b> input signal is HIGH.
CleanInvalid	Cache maintenance instructions.
MakeInvalid	Not used.
DVMOp	TLB and instruction cache maintenance instructions.
EOBarrier	Not used.
ECBarrier	Not used.
PrefetchTgt	Not used.

**Table A7-7 CHI transaction types (continued)**

Transaction	Operation
StashOnceShared	Cache prefetch when there is no L3 cache present.
StashOnceUnique	Cache prefetch when there is no L3 cache present.
WriteNoSnpPtl	Non-cacheable store instructions.
WriteNoSnpFull	Non-cacheable store instructions, or evictions of Non-shareable cache lines.
WriteUniqueFull	Cacheable writes of a full cache line, that are not allocating into L1, L2, or L3 caches, for example streaming writes.
WriteUniquePtl	Not used.
WriteBackFull	Evictions of dirty lines from the L1, L2, or L3 caches.
WriteBackPtl	Not used.
WriteCleanFull	Evictions of dirty lines from the L3 cache, when the line is still present in an L1 or L2 cache. Some cache maintenance instructions.
WriteCleanPtl	Not used.
WriteEvictFull	Evictions of unique clean lines, when configured in the CLUSTERECTLR.
Evict	Evictions of clean lines, when configured in the CLUSTERECTLR.
AtomicStore	Atomic instruction.
AtomicLoad	Atomic instruction.
AtomicSwap	Atomic instruction.
AtomicCompare	Atomic instruction.
WriteUniqueFullStash	Not used.
WriteUniquePtlStash	Not used.
ReadOnceCleanInvalid	Not used.
ReadOnceMakeInvalid	Not used.

External memory accesses generate the following transactions in an implementation configured with a CHI master interface.

**Table A7-8 CHI transaction usage**

Attributes		CHI transaction				
Memory type	Shareability	SnpAttr	Load	Store	Load exclusive	Store exclusive
Device	Outer Shareable	Non-snooperable	ReadNoSnp	WriteNoSnp	ReadNoSnp and <b>Excl</b> set to HIGH.	WriteNoSnp and <b>Excl</b> set to HIGH.
Normal, Inner Non-cacheable, Outer Non-cacheable	Non-shareable	Non-snooperable	ReadNoSnp	WriteNoSnp	ReadNoSnp and <b>Excl</b> set to HIGH.	WriteNoSnp and <b>Excl</b> set to HIGH.
	Inner Shareable					
	Outer Shareable					

Table A7-8 CHI transaction usage (continued)

Attributes		CHI transaction				
Memory type	Shareability	SnpAttr	Load	Store	Load exclusive	Store exclusive
Normal, Inner Non-cacheable, Outer Write-Back or Write-Through, or Normal, Inner Write-Through, Outer Write-Back, Write-Through or Non-cacheable, or Normal Inner Write-Back Outer Non-cacheable or Write-Through	Non-shareable	Non-snoopable	ReadNoSnp	WriteNoSnp	ReadNoSnp and <b>Excl</b> set to HIGH.	WriteNoSnp and <b>Excl</b> set to HIGH.
	Inner Shareable					
	Outer Shareable					
Normal, Inner Write-Back, Outer Write-Back	Non-shareable	Non-snoopable	ReadNoSnp	WriteNoSnp	ReadNoSnp	WriteNoSnp
	Inner Shareable	Snoopable	ReadNotSharedDirty or ReadClean	ReadUnique, CleanUnique, or MakeUnique if allocating into the cache, then a WriteBackFull when the line is evicted.  WriteUniqueFull or WriteUniquePtl if not allocating into the cache.	ReadNotSharedDirty or ReadClean, with <b>Excl</b> set to HIGH.	CleanUnique with <b>Excl</b> set to HIGH if required, then a WriteBackFull when the line is evicted.
	Outer Shareable	Snoopable				



# Chapter A8

## ACP Slave Interface

This chapter describes the ACP slave interface.

It contains the following sections:

- *A8.1 About the ACP* on page A8-94.
- *A8.2 ACP features* on page A8-95.
- *A8.3 ACP ACE-Lite subset* on page A8-96.
- *A8.4 ACP transaction types* on page A8-97.
- *A8.5 ACP performance* on page A8-98.

## A8.1 About the ACP

The *Accelerator Coherency Port* (ACP) is an optional slave interface, conforming to a subset of the ACE-Lite specification.

The ACP slave interface allows an external master to access memory through the main memory interface of the DSU. Only access to cacheable memory is permitted.

The read and write data buses of the ACP are 128 bits. Accesses are optimized for cache line length.

To maintain cache coherency, accesses are checked in all cached locations in the cluster. That is, the L3 cache, and the data caches in each core.

ACP allocating write accesses are implicit stash requests to the L3 cache.

## A8.2 ACP features

The ACP interface for the DSU supports the following properties.

**Table A8-1 ACP interface properties for the DSU**

ACP property	Supported by the DSU
Port_Type	Accelerator
Continuous_Cache_Line_Read_Data	Yes
Multi_Copy_Atomicity	Yes
Ordered_Write_Observation	No
WriteEvict_Transaction	No
DVM_v8	No
Atomic_Transactions	No
DVM_v8.1	No
Cache_Stash_Transactions	No
DeAllocation_Transactions	No
Persistent_CMO	No
Poison	No
Data_Check	No
QoS_Accept	No
Trace_Signals	No
Loopback_Signals	No
Low_Power_Signals	Yes
Untranslated_Transactions	No
NSAccess_Identifiers	No

## A8.3 ACP ACE-Lite subset

The ACP conforms to a subset of the ACE-Lite specification.

The ACP ACE-Lite subset is described in *AMBA® AXI™ and ACE™ Protocol Specification AXI3™, AXI4™, and AXI4-Lite™, ACE and ACE-Lite™*. The DSU has the following additional restrictions:

- The values of **ARCACHES** and **AWCACHES** are restricted to:
  - 0b0111.
  - 0b1011.
  - 0b1111.
- All transactions can be Secure or Non-secure.
- Exclusive accesses are not supported. **ARLOCK** and **AWLOCK** signals are not present.
- All requests can specify Inner Shareable and Outer Shareable using the **AWDOMAINS** and **ARDOMAINS** signals.
- Barriers are not supported. The **BRESP** response for any write transaction indicates global observability for the transaction.
- **ARSIZE** and **AWSIZE** signals are not present. A value of 4 (16 bytes) is assumed.
- The values of **ARLENS** and **AWLENS** are restricted to:

<b>0</b>	One beat.
<b>3</b>	Four beats.
- **ARBURST** and **AWBURST** signals are not present. A value of 0b01 (INCR) is assumed.
- **ARSNOOP** signals are not present. A value of 0b0000 is assumed.
- **ARQOS** and **AWQOS** signals are not present.



## A8.4 ACP transaction types

The ACP supports transaction types having the following transfer size and length combinations:

- 16-byte INCR read transaction:
  - **ARLENS** is 0 (one beat).
  - Address aligned to 16-byte boundary (**ARADDRS[3:0]** is 0b0000).
- 64-byte INCR read transaction:
  - **ARLENS** is 3 (four beats).
  - Address aligned to 64-byte boundary (**ARADDRS[5:0]** is 0b000000).

The ACP supports the following write transaction transfer size and length combinations:

- 16-byte INCR write transaction:
  - **WSTRBS**, any combination of bytes, including no bytes, are valid.
  - **AWLENS** is 0 (one beat).
  - **AWSNOOPS** is WriteUniquePtl.
  - Address aligned to 16-byte boundary (**AWADDRS[3:0]** is 0b0000).
- 64-byte INCR write transaction:
  - **WSTRBS**, any combination of bytes, including no bytes, are valid.

————— **Note** —————

When **AWSNOOPS** is WriteUniqueFull, all bytes must be valid.

- **AWLENS** is 3 (four beats).
- **AWSNOOPS** is WriteUniquePtl or WriteUniqueFull.
- Address aligned to 64-byte boundary (**AWADDRS[5:0]** is 0b000000).

————— **Note** —————

The AMBA5 ACE-Lite transaction types WriteUniqueFull and WriteUniquePtl were known in AMBA4 ACE-Lite as WriteLineUnique and WriteUnique, respectively.

The ACP supports the following Cache Stash Transaction transfer size and length:

- 64-byte INCR write stash transaction:
  - **WSTRBS**, all bytes are valid.
  - **AWLENS** is 3 (four beats).
  - **AWSNOOPS** is WriteUniqueFullStash.
  - Address aligned to 64-byte boundary (**AWADDRS[5:0]** is 0b000000).

————— **Note** —————

Requests not meeting these restrictions cause a SLVERR response on **RRESPS** or **BRESPS**.

The following table lists the ACP supported transactions:

**Table A8-2 ACP supported transactions**

Transaction	Notes
ReadOnce	-
WriteUniqueFull	-
WriteUniquePtl	-
WriteUniqueFullStash	Identical to WriteUniqueFull

## A8.5 ACP performance

For optimum performance, use the following guidelines for ACP transactions.

The master must avoid sending more than one outstanding transaction on the same AXI ID, to prevent the second transaction stalling the interface until the first has completed. If the master requires explicit ordering between two transactions, ARM recommends that it waits for the response to the first transaction before sending the second transaction.

Writes are higher performance when they contain a full cache line of data.

Writes of less than a full cache line always incur a read-modify write sequence.

Some L3 resources are shared between the ACP interface and the cores, so heavy traffic on the ACP interface might, in some cases, reduce the performance of the cores.

The following table describes the ACP acceptance capabilities.

**Table A8-3 ACP acceptance capabilities**

Attribute	Value	Description
Write acceptance capability	9	The ACP can accept up to 9 write transactions.
Read acceptance capability	9	The ACP can accept up to 9 read transactions.
Combined acceptance capability	10	The ACP can accept up to 10 transactions. There is no performance benefit above 8 outstanding transactions.

# Chapter A9

## AXI Master Peripheral Port

This chapter describes the AXI master peripheral port.

It contains the following sections:

- [A9.1 About the peripheral port](#) on page A9-100.
- [A9.2 Transaction ID encoding](#) on page A9-101.

## A9.1 About the peripheral port

The peripheral port supports Device accesses to tightly coupled accelerators.

The peripheral port can be used for low-latency access to peripherals local to the cluster. It has the same latency as the main master port. However, the overall system latency to devices connected to the main master port is greater because of the higher latency of the system interconnect.

The peripheral port is optionally implemented. It is a 64-bit AXI4 master interface.

The peripheral port supports access to only Device-nGRE, nGnRE, and nGnRnE memory types:

- All accesses must be aligned load or store instructions of 64 bits or less. Unaligned or larger accesses are not supported and generate an external abort.
- Atomic instructions are not supported and generate an external abort.
- Load and store exclusive instructions are not supported. Store exclusive instructions will fail and the result register will reflect this, but the memory location might be updated.

Accesses to the port using other memory types are unpredictable.

The peripheral port address range is defined by two configuration input buses. **ASTARTMP[PA-1:20]** for the start of the address range and **AENDMP[PA-1:20]** for the end of the range, where PA is the largest physical address width of any connected core. The address range is inclusive. These signals are only captured at reset.

## A9.2 Transaction ID encoding

The AXI interface has the following read and write issuing capabilities and ID encoding:

The following table describes the read and write issuing capabilities.

**Table A9-1 AXI issuing capabilities**

Attribute	Value	Comments
Write issuing capability	5	There can be up to 5 outstanding write transactions.
Read issuing capability		There can be up to 5 outstanding read transactions.
Combined issuing capability	10	There can be up to 10 outstanding transactions.
Write ID capability	5	Each ID can have up to 5 outstanding write transactions.
Read ID capability		Each ID can have up to 5 outstanding read transactions.

The following table lists the encoding for AXI transaction IDs.

**Table A9-2 AXI transaction ID encoding**

Attribute	Value	Comments
All IDs	tnnn	Thread t <sup>f</sup> , core nnn <sup>g</sup>

### Note

These ID and transaction details are provided for information only. ARM strongly recommends that all interconnects and peripherals are designed to support any type and number of transactions on any ID, to ensure compatibility with future products.

See the *ARM® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite* for more information about the ACE and AXI signals described in this manual.

<sup>f</sup> t is the hardware thread number and is 0 if the core does not support multiple hardware threads.  
<sup>g</sup> nnn is the core number 0b000-0b111 in binary.



## Part B

### **Register Descriptions**





# Chapter B1

## Control registers

This chapter describes the control registers for the DSU.

It contains the following sections:

- *B1.1 About the control registers on page B1-106.*
- *B1.2 AArch32 control register summary on page B1-107.*
- *B1.3 AArch64 control register summary on page B1-108.*
- *B1.4 CLUSTERACPSID, Cluster ACP Scheme ID Register on page B1-109.*
- *B1.5 CLUSTERACTLR, Cluster Auxiliary Control Register on page B1-110.*
- *B1.6 CLUSTERBUSQOS, Cluster Bus QoS Control Register on page B1-111.*
- *B1.7 CLUSTERCFR, Cluster Configuration Register on page B1-113.*
- *B1.8 CLUSTERECTLR, Cluster Extended Control Register on page B1-116.*
- *B1.9 CLUSTERIDR, Cluster Main Revision ID Register on page B1-119.*
- *B1.10 CLUSTERL3HIT, Cluster L3 Hit Counter Register on page B1-120.*
- *B1.11 CLUSTERL3MISS, Cluster L3 Miss Counter Register on page B1-121.*
- *B1.12 CLUSTERPARTCR, Cluster Partition Control Register on page B1-122.*
- *B1.13 CLUSTERPWRCTRL, Cluster Power Control Register on page B1-123.*
- *B1.14 CLUSTERPWRDN, Cluster Powerdown Register on page B1-125.*
- *B1.15 CLUSTERPWRSTAT, Cluster Power Status Register on page B1-127.*
- *B1.16 CLUSTERREVIDR, Cluster Revision ID Register on page B1-129.*
- *B1.17 CLUSTERSTASHSID, Cluster Stash Scheme ID Register on page B1-130.*
- *B1.18 CLUSTERTHREADSID, Cluster Thread Scheme ID Register on page B1-131.*
- *B1.19 CLUSTERTHREADSIDOVR, Cluster Thread Scheme ID Override Register on page B1-132.*

## B1.1 About the control registers

The DSU contains system control registers in the SCU and L3 logic to control the functionality of the cluster. Most of these registers are shared between all the cores in the cluster, but a few are private to each core.

The chapter is presented as follows:

### **AArch32 control register summary**

This section lists the AArch32 control registers by access encoding.

### **AArch64 control register summary**

This section lists the AArch64 control registers by access encoding.

### **Register descriptions**

The remainder of the chapter provides generic register descriptions, that apply to both AArch32 and AArch64 registers. They are listed in alphabetical order.

## B1.2 AArch32 control register summary

This section lists the AArch32 control registers implemented in the DSU, sorted by access encoding.

**Table B1-1 DynamIQ Shared Unit AArch32 control registers**

Register mnemonic	Copro	CRn	Opc1	CRm	Opc2	Width	Register name and description
CLUSTERCFR	cp15	c15	0	c3	0	32	<i>B1.7 CLUSTERCFR, Cluster Configuration Register on page B1-113</i>
CLUSTERIDR	cp15	c15	0	c3	1	32	<i>B1.9 CLUSTERIDR, Cluster Main Revision ID Register on page B1-119</i>
CLUSTERREVIDR	cp15	c15	0	c3	2	32	<i>B1.16 CLUSTERREVIDR, Cluster Revision ID Register on page B1-129</i>
CLUSTERACTLR	cp15	c15	0	c3	3	32	<i>B1.5 CLUSTERACTLR, Cluster Auxiliary Control Register on page B1-110</i>
CLUSTERECTLR	cp15	c15	0	c3	4	32	<i>B1.8 CLUSTERECTLR, Cluster Extended Control Register on page B1-116</i>
CLUSTERPWRCTLR	cp15	c15	0	c3	5	32	<i>B1.13 CLUSTERPWRCTLR, Cluster Power Control Register on page B1-123</i>
CLUSTERPWRDN	cp15	c15	0	c3	6	32	<i>B1.14 CLUSTERPWRDN, Cluster Powerdown Register on page B1-125</i>
CLUSTERPWRSTAT	cp15	c15	0	c3	7	32	<i>B1.15 CLUSTERPWRSTAT, Cluster Power Status Register on page B1-127</i>
CLUSTERTHREADSID	cp15	c15	0	c4	0	32	<i>B1.18 CLUSTERTHREADSID, Cluster Thread Scheme ID Register on page B1-131</i>
CLUSTERACPSID	cp15	c15	0	c4	1	32	<i>B1.4 CLUSTERACPSID, Cluster ACP Scheme ID Register on page B1-109</i>
CLUSTERSTASHSID	cp15	c15	0	c4	2	32	<i>B1.17 CLUSTERSTASHSID, Cluster Stash Scheme ID Register on page B1-130</i>
CLUSTERPARTCR	cp15	c15	0	c4	3	32	<i>B1.12 CLUSTERPARTCR, Cluster Partition Control Register on page B1-122</i>
CLUSTERBUSQOS	cp15	c15	0	c4	4	32	<i>B1.6 CLUSTERBUSQOS, Cluster Bus QoS Control Register on page B1-111</i>
CLUSTERL3HIT	cp15	c15	0	c4	5	32	<i>B1.10 CLUSTERL3HIT, Cluster L3 Hit Counter Register on page B1-120</i>
CLUSTERL3MISS	cp15	c15	0	c4	6	32	<i>B1.11 CLUSTERL3MISS, Cluster L3 Miss Counter Register on page B1-121</i>
CLUSTERTHREADSIDOVR	cp15	c15	0	c4	7	32	<i>B1.19 CLUSTERTHREADSIDOVR, Cluster Thread Scheme ID Override Register on page B1-132</i>

## B1.3 AArch64 control register summary

This section lists the AArch64 control registers implemented in the DSU, sorted by access encoding.

**Table B1-2 DynamIQ Shared Unit AArch64 control registers**

Register mnemonic	Op0	CRn	Op1	CRm	Op2	Width	Register name and description
CLUSTERCFR_EL1	3	c15	0	c3	0	32	<i>B1.7 CLUSTERCFR, Cluster Configuration Register on page B1-113</i>
CLUSTERIDR_EL1	3	c15	0	c3	1	32	<i>B1.9 CLUSTERIDR, Cluster Main Revision ID Register on page B1-119</i>
CLUSTERREVIDR_EL1	3	c15	0	c3	2	32	<i>B1.16 CLUSTERREVIDR, Cluster Revision ID Register on page B1-129</i>
CLUSTERACTLR_EL1	3	c15	0	c3	3	32	<i>B1.5 CLUSTERACTLR, Cluster Auxiliary Control Register on page B1-110</i>
CLUSTERECTLR_EL1	3	c15	0	c3	4	32	<i>B1.8 CLUSTERECTLR, Cluster Extended Control Register on page B1-116</i>
CLUSTERPWRCTLR_EL1	3	c15	0	c3	5	32	<i>B1.13 CLUSTERPWRCTLR, Cluster Power Control Register on page B1-123</i>
CLUSTERPWRDN_EL1	3	c15	0	c3	6	32	<i>B1.14 CLUSTERPWRDN, Cluster Powerdown Register on page B1-125</i>
CLUSTERPWRSTAT_EL1	3	c15	0	c3	7	32	<i>B1.15 CLUSTERPWRSTAT, Cluster Power Status Register on page B1-127</i>
CLUSTERTHREADSID_EL1	3	c15	0	c4	0	32	<i>B1.18 CLUSTERTHREADSID, Cluster Thread Scheme ID Register on page B1-131</i>
CLUSTERACPSID_EL1	3	c15	0	c4	1	32	<i>B1.4 CLUSTERACPSID, Cluster ACP Scheme ID Register on page B1-109</i>
CLUSTERSTASHSID_EL1	3	c15	0	c4	2	32	<i>B1.17 CLUSTERSTASHSID, Cluster Stash Scheme ID Register on page B1-130</i>
CLUSTERPARTCR_EL1	3	c15	0	c4	3	32	<i>B1.12 CLUSTERPARTCR, Cluster Partition Control Register on page B1-122</i>
CLUSTERBUSQOS_EL1	3	c15	0	c4	4	32	<i>B1.6 CLUSTERBUSQOS, Cluster Bus QoS Control Register on page B1-111</i>
CLUSTERL3HIT_EL1	3	c15	0	c4	5	32	<i>B1.10 CLUSTERL3HIT, Cluster L3 Hit Counter Register on page B1-120</i>
CLUSTERL3MISS_EL1	3	c15	0	c4	6	32	<i>B1.11 CLUSTERL3MISS, Cluster L3 Miss Counter Register on page B1-121</i>
CLUSTERTHREADSIDOVR_EL1	3	c15	0	c4	7	32	<i>B1.19 CLUSTERTHREADSIDOVR, Cluster Thread Scheme ID Override Register on page B1-132</i>

## B1.4 CLUSTERACPSID, Cluster ACP Scheme ID Register

The CLUSTERACPSID register provides the scheme ID for ACP transactions.

This description applies to both the AArch32 (CLUSTERACPSID) and AArch64 (CLUSTERACPSID\_EL1) registers.

### Bit field descriptions

CLUSTERACPSID is a 32-bit register, and is part of SCU and L3 cache configuration registers.

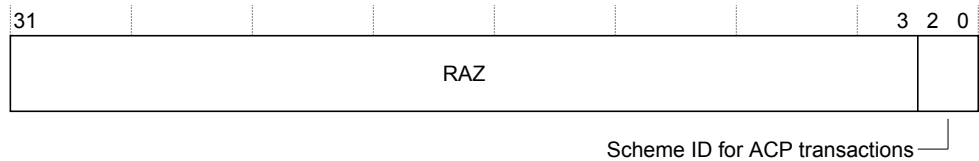


Figure B1-1 CLUSTERACPSID bit assignments

### RAZ, [31:3]

Read-As-Zero.

### Scheme ID for ACP transactions, [2:0]

These bits reset to 0b000.

### Configurations

The AArch32 CLUSTERACPSID register is architecturally mapped to the AArch64 CLUSTERACPSID\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERACPSID	x	x	0	-	RW	n/a	RW
CLUSTERACPSID	x	0	1	-	RW	RW	RW
CLUSTERACPSID	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.SMEN is 1 and ACTLR\_EL2.SMEN is 1, or ACTLR\_EL3.SMEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.5 CLUSTERACTLR, Cluster Auxiliary Control Register

The CLUSTERACTLR register is Reserved.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.ACTLREN is 1 and ACTLR\_EL2.ACTLREN is 1, or ACTLR\_EL3.ACTLREN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).

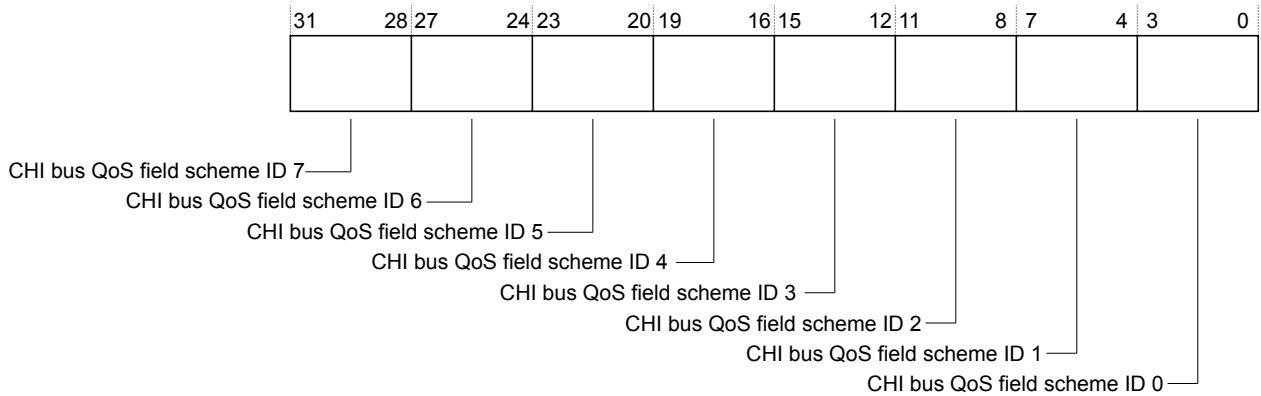
## B1.6 CLUSTERBUSQOS, Cluster Bus QoS Control Register

The CLUSTERBUSQOS provides control for the CHI *Quality of Service* (QoS) fields for different scheme IDs.

This description applies to both the AArch32 (CLUSTERBUSQOS) and AArch64 (CLUSTERBUSQOS\_EL1) registers.

### Bit field descriptions

CLUSTERBUSQOS is a 32-bit register, and is part of SCU and L3 cache configuration registers.



**Figure B1-2 CLUSTERBUSQOS bit assignments**

#### CHI bus QoS field scheme ID 7, [31:28]

Value driven on the CHI bus QoS field for scheme ID 7.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 6, [27:24]

Value driven on the CHI bus QoS field for scheme ID 6.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 5, [23:20]

Value driven on the CHI bus QoS field for scheme ID 5.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 4, [19:16]

Value driven on the CHI bus QoS field for scheme ID 4.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 3, [15:12]

Value driven on the CHI bus QoS field for scheme ID 3.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 2, [11:8]

Value driven on the CHI bus QoS field for scheme ID 2.

These bits reset to 0xE.

#### CHI bus QoS field scheme ID 1, [7:4]

Value driven on the CHI bus QoS field for scheme ID 1.

These bits reset to 0xE.

### CHI bus QoS field scheme ID 0, [3:0]

Value driven on the CHI bus QoS field for scheme ID 0.

These bits reset to 0xE.

### Configurations

The AArch32 CLUSTERBUSQOS register is architecturally mapped to the AArch64 CLUSTERBUSQOS\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERBUSQOS	x	x	0	-	RW	n/a	RW
CLUSTERBUSQOS	x	0	1	-	RW	RW	RW
CLUSTERBUSQOS	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.SMEN is 1 and ACTLR\_EL2.SMEN is 1, or ACTLR\_EL3.SMEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).



## B1.7 CLUSTERCFR, Cluster Configuration Register

The CLUSTERCFR register contains details of the hardware configuration of the cluster. This register is read-only write-ignores RO (WI), and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERCFR) and AArch64 (CLUSTERCFR\_EL1) registers.

### Bit field descriptions

CLUSTERCFR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

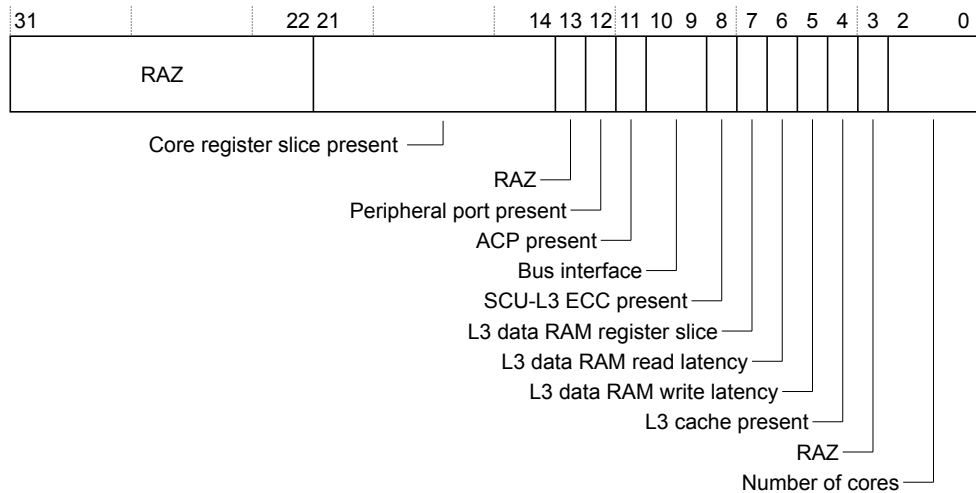


Figure B1-3 CLUSTERCFR bit assignments

### RAZ, [31:22]

Read-As-Zero

### Core register slice present, [21:14]

Core register slice is present. Each bit represents a core, with bit[14] for core 0 up to bit[21] for core 7:

- 0 No register slice is present.
- 1 Register slice is present.

### RAZ, [13]

Read-As-Zero

### Peripheral port present, [12]

Peripheral port is present:

- 0 No peripheral port is present.
- 1 Peripheral port is present.

### ACP present, [11]

ACP interface is present:

- 0 No ACP interface is present.
- 1 ACP interface is present.

### Bus interface, [10:9]

Bus interface configuration:

0b00	Single 128-bit ACE.
0b01	Dual 128-bit ACE.
0b10	Single 128-bit CHI.
0b11	Single 256-bit CHI.

#### SCU-L3 ECC present, [8]

SCU-L3 is configured with ECC:

0	SCU-L3 is not configured with ECC.
1	SCU-L3 is configured with ECC.

#### L3 data RAM register slice, [7]

L3 data RAM read register slice:

0	No register slice is present.
1	Register slice is present.

#### L3 data RAM read latency, [6]

L3 data RAM read latency:

0	Two-cycle output delay from the L3 data RAMs.
1	Three-cycle output delay from L3 data RAMs.

#### L3 data RAM write latency, [5]

L3 data RAM write latency:

0	One cycle input delay from the L3 data RAMs.
1	Two cycle input delay from the L3 data RAMs.

#### L3 cache present, [4]

L3 cache is present:

0	No L3 cache is present.
1	L3 cache is present.

#### RAZ, [3]

Read-As-Zero

#### Number of cores, [2:0]

Number of cores present in the cluster:

0b000	One core, Core0.
0b001	Two cores, Core0-1.
0b010	Three cores, Core0-2.
0b011	Four cores, Core0-3.
0b100	Five cores, Core0-4.
0b101	Six cores, Core0-5.
0b110	Seven cores, Core0-6.
0b111	Eight cores, Core0-7.

#### Configurations

The AArch32 CLUSTERCFR register is architecturally mapped to the AArch64 CLUSTERCFR\_EL1 register.

## Usage Constraints

### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERCFR	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERCFR	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERCFR	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

There are no special traps and enables.

## B1.8 CLUSTERECTLR, Cluster Extended Control Register

The CLUSTERECTLR register provides implementation-specific control of the microarchitecture. It must only be written to as part of the initial system configuration setup following reset. This register is RW, and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERECTLR) and AArch64 (CLUSTERECTLR\_EL1) registers.

### Bit field descriptions

CLUSTERECTLR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

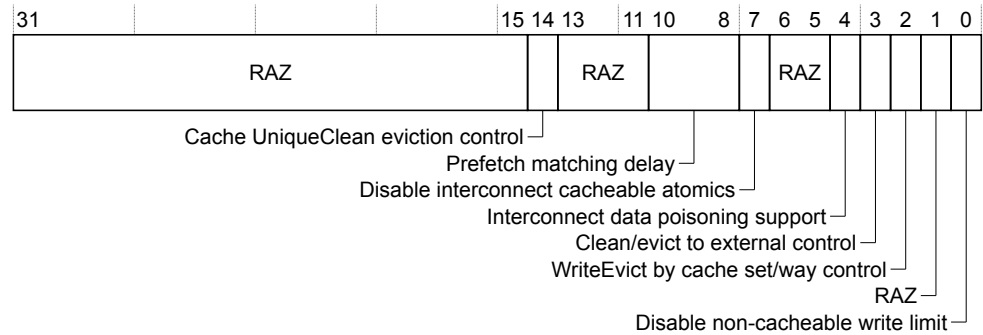


Figure B1-4 CLUSTERECTLR bit assignments

### RAZ, [31:15]

Read-As-Zero

### Cache UniqueClean eviction control, [14]

Enables sending WriteEvict transactions on the ACE/CHI master for UniqueClean evictions. WriteEvict transactions update downstream caches that are outside the cluster. Enable WriteEvict transactions only if there is an L4 or system cache implemented in the system. The possible values are:

- 0 Disables sending data with UniqueClean evictions.
- 1 Enables sending data with UniqueClean evictions.

For ACE, this bit resets to 0.

For CHI, this bit resets to 1.

### RAZ, [13:11]

Read-As-Zero

### Prefetch matching delay, [10:8]

Prefetch matching delay. Controls the amount of time a prefetch waits for a possible match with a later read. Encoded as powers of 2, from 1-128.

These bits reset to 0x5.

### Disable interconnect cacheable atomics, [7]

Disable cacheable atomics being sent to the interconnect. The possible values are:

- 0 If **BROADCASTATOMIC** is set HIGH, cacheable atomics are sent to the interconnect.
- 1 Cacheable atomics are handled inside the cluster.

This bit has no effect for ACE configurations.

This bit resets to 0.

## RAZ, [6:5]

Read-As-Zero

### Interconnect data poisoning support, [4]

Interconnect data poisoning support. This bit is RAZ for ACE configurations. The possible values are:

- 0 Interconnect does not support data poisoning. Therefore **nERRIRQ** is asserted when poisoned data is evicted from the cluster or returned to a snoop.
- 1 Interconnect supports data poisoning. Therefore no error recovery interrupt is generated when poisoned data is evicted from the cluster or returned to a snoop.

For ACE, this bit resets to 0.

For CHI, this bit resets to 1.

### Cache Evict disable, [3]

Disables sending of Evict transactions on the ACE/CHI master for clean cache lines that are evicted from the cluster. Evict transactions are required only if the external interconnect contains a snoop filter that requires notification when the cluster evicts the cache line. The possible values are:

- 0 Enables sending Evict transactions.
- 1 Disables sending Evict transactions.

This bit resets to 0.

### Cache flush UniqueClean eviction control, [2]

Disables the sending of WriteEvict requests on the ACE/CHI master when powering down part or all of the L3 cache. The possible values are:

- 0 Evictions during L3 cache powerdown behave like normal evictions. This is the reset value.
- 1 Disables sending data with UniqueClean evictions caused by powering down the L3 cache.

## RAZ, [6:5]

Read-As-Zero

### Disable non-cacheable write limit, [0]

Disable the limit on the number of non-cacheable writes that are allowed on the ACE interface. Setting this bit might have implications on the behavior of system components for example the CPE-425 Coherent PCIe Extension. The possible values are:

- 0 When ACE is configured, Device and Normal Non-Cacheable writes are limited to 15 outstanding transactions.
- 1 When ACE is configured, only Device writes are limited to 15 outstanding transactions. The limit is removed for Normal Non-Cacheable transactions.

In Dual ACE configurations this bit controls whether Normal Non-Cacheable transactions are sent to interface 0 or to both interfaces. See [A6.1.1 Dual ACE interfaces on page A6-70](#).

If this bit is set to 1, then further writes to this bit are ignored.

For CHI, this bit is Read-As-Zero.

### Configurations

The AArch32 CLUSTERECTLR register is architecturally mapped to the AArch64 CLUSTERECTLR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERECTLR	x	x	0	-	RW	n/a	RW
CLUSTERECTLR	x	0	1	-	RW	RW	RW
CLUSTERECTLR	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

#### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.ECTLREN is 1 and ACTLR\_EL2.ECTLREN is 1, or ACTLR\_EL3.ECTLR\_EN is 1 and SCR.NS is 0.

If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.9 CLUSTERIDR, Cluster Main Revision ID Register

The CLUSTERIDR register contains the revision and patch level of the DSU. This register is read-only write-ignores RO (WI), and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERIDR) and AArch64 (CLUSTERIDR\_EL1) registers.

### Bit field descriptions

CLUSTERIDR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

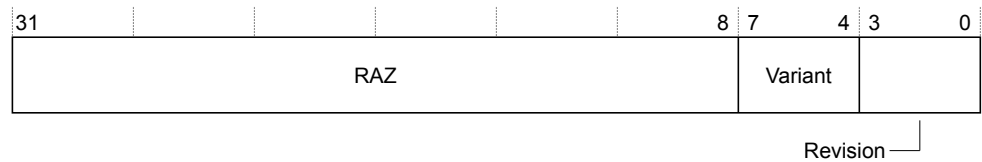


Figure B1-5 CLUSTERIDR bit assignments

### RAZ, [31:8]

Read-As-Zero.

### Variant, [7:4]

Indicates the variant of the DSU. This is the major revision number *x* in the *rx* part of the *rxpy* description of the product revision status. This value is:

0x0      r0

### Revision, [3:0]

Indicates the minor revision number of the DSU. This is the minor revision number *y* in the *py* part of the *rxpy* description of the product revision status. This value is:

0x2      p2

### Configurations

The AArch32 CLUSTERIDR register is architecturally mapped to the AArch64 CLUSTERIDR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERIDR	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERIDR	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERIDR	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

There are no traps and enables that affect this register.

## B1.10 CLUSTERL3HIT, Cluster L3 Hit Counter Register

The CLUSTERL3HIT register contains a count of the L3 cache hits. This register is intended for use in algorithms for determining when to power up or power down portions. This register is RW, and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERL3HIT) and AArch64 (CLUSTERL3HIT\_EL1) registers.

If CLUSTERPMMDCR.SPME == 0, this counter does not trigger for secure transactions.

### Bit field descriptions

CLUSTERL3HIT is a 32-bit register, and is part of SCU and L3 cache configuration registers.

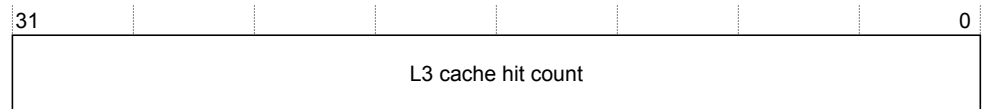


Figure B1-6 CLUSTERL3HIT bit assignments

### L3 cache hit count, [31:0]

Count of number of L3 cache hits, for use in portion control calculations. The counter saturates to its maximum value on overflow.

On a write, CLUSTERL3HIT gets set to the specified value.

These bits reset to 0x00000000.

### Configurations

The AArch32 CLUSTERL3HIT register is architecturally mapped to the AArch64 CLUSTERL3HIT\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERL3HIT	x	x	0	-	RW	n/a	RW
CLUSTERL3HIT	x	0	1	-	RW	RW	RW
CLUSTERL3HIT	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.PWREN is 1 and ACTLR\_EL2.PWREN is 1, or ACTLR\_EL3.PWREN is 1 and SCR.NS is 0.

If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).



## B1.11 CLUSTERL3MISS, Cluster L3 Miss Counter Register

The CLUSTERL3MISS register contains a count of the L3 cache misses. This register is intended for use in algorithms for determining when to power up or power down portions. This register is RW, and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERL3MISS) and AArch64 (CLUSTERL3MISS\_EL1) registers.

If CLUSTERPMMDCR.SPME == 0, this counter does not trigger for secure transactions.

### Bit field descriptions

CLUSTERL3MISS is a 32-bit register, and is part of SCU and L3 cache configuration registers.

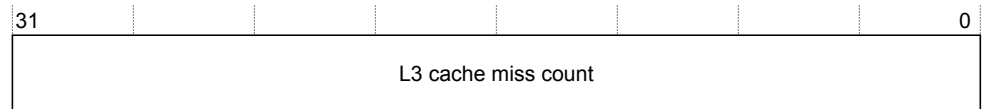


Figure B1-7 CLUSTERL3MISS bit assignments

### L3 cache miss count, [31:0]

Count of number of L3 cache misses, for use in portion control calculations. The counter saturates to its maximum value on overflow.

On a write, CLUSTERL3MISS gets set to the specified value.

These bits reset to 0x00000000.

### Configurations

The AArch32 CLUSTERL3MISS register is architecturally mapped to the AArch64 CLUSTERL3MISS\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERL3MISS	x	x	0	-	RW	n/a	RW
CLUSTERL3MISS	x	0	1	-	RW	RW	RW
CLUSTERL3MISS	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.PWREN is 1 and ACTLR\_EL2.PWREN is 1, or ACTLR\_EL3.PWREN is 1 and SCR.NS is 0.

If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.12 CLUSTERPARTCR, Cluster Partition Control Register

The CLUSTERPARTCR register is unused in this revision of the DSU.

This description applies to both the AArch32 (CLUSTERPARTCR) and AArch64 (CLUSTERPARTCR\_EL1) registers.

### Bit field descriptions

CLUSTERPARTCR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

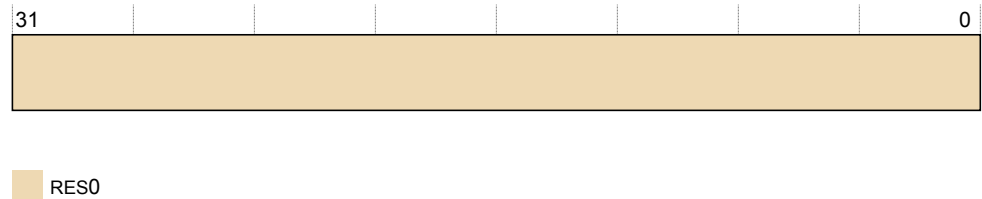


Figure B1-8 CLUSTERPARTCR bit assignments

### RES0, [31:0]

RES0 Reserved.

### Configurations

The AArch32 CLUSTERPARTCR register is architecturally mapped to the AArch64 CLUSTERPARTCR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPARTCR	x	x	0	-	RW	n/a	RW
CLUSTERPARTCR	x	0	1	-	RW	RW	RW
CLUSTERPARTCR	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.SMEN is 1 and ACTLR\_EL2.SMEN is 1, or ACTLR\_EL3.SMEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.13 CLUSTERPWRCTLR, Cluster Power Control Register

The CLUSTERPWRCTLR register controls power features of the cluster. This register is RW, and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERPWRCTLR) and AArch64 (CLUSTERPWRCTLR\_EL1) registers.

### Bit field descriptions

CLUSTERPWRCTLR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

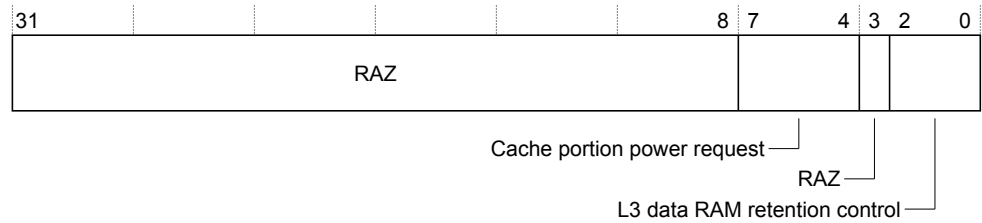


Figure B1-9 CLUSTERPWRCTLR bit assignments

#### RAZ, [31:8]

Read-As-Zero.

#### Cache portion power request, [7:4]

These bits are output on **CLUSTERACTIVE**[19:16] to indicate to the power controller which cache portions must be powered. This is an advisory status to the power controller, and does not cause the p-channel to deny any requests based on this status.

The reset values of these bits depend on the cluster p-channel initialization state.

#### RAZ, [3]

Read-As-Zero.

#### L3 data RAM retention control, [2:0]

L3 data RAM retention control. The possible values of these bits are:

- 0b000 Disable the retention circuit. This is the default condition.
- 0b001 Two Architectural Timer ticks are required before retention entry.
- 0b010 Eight Architectural Timer ticks are required before retention entry.
- 0b011 32 Architectural Timer ticks are required before retention entry.
- 0b100 64 Architectural Timer ticks are required before retention entry.
- 0b101 128 Architectural Timer ticks are required before retention entry.
- 0b110 256 Architectural Timer ticks are required before retention entry.
- 0b111 512 Architectural Timer ticks are required before retention entry.

These bits reset to 0b000.

### Configurations

The AArch32 CLUSTERPWRCTLR register is architecturally mapped to the AArch64 CLUSTERPWRCTLR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPWRCTL	x	x	0	-	RW	n/a	RW
CLUSTERPWRCTL	x	0	1	-	RW	RW	RW
CLUSTERPWRCTL	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

#### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.PWREN is 1 and ACTLR\_EL2.PWREN is 1, or ACTLR\_EL3.PWREN is 1 and SCR.NS is 0.

If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

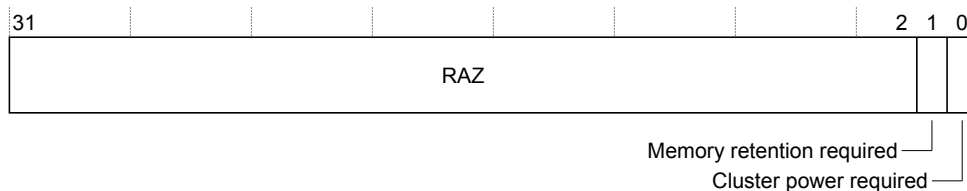
### B1.14 CLUSTERPWRDN, Cluster Powerdown Register

The CLUSTERPWRDN register controls powerdown requirements of the cluster. This register is RW, and is banked for each thread of execution.

This description applies to both the AArch32 (CLUSTERPWRDN) and AArch64 (CLUSTERPWRDN\_EL1) registers.

## Bit field descriptions

CLUSTERPWRDN is a 32-bit register, and is part of SCU and L3 cache configuration registers.



### Figure B1-10 CLUSTERPWRDN bit assignments

**RAZ, [31:2]**

Read-As-Zero.

**Memory retention required, [1]**

The possible values are:

- 0 Indicates on **CLUSTERACTIVE** that memory retention is not required when all cores are powered down.
- 1 Indicates on **CLUSTERACTIVE** that memory retention is required when all cores are powered down.

This signal provides an advisory status to the power controller. It does not deny a p-channel request to powerdown the cluster.

This bit resets to 0.

**Cluster power required, [0]**

The possible values are:

- 0 Indicates on **CLUSTERACTIVE** that cluster power is not required even when all cores are powered down.
- 1 Indicates on **CLUSTERACTIVE** that cluster power is required even when all cores are powered down.

This signal provides an advisory status to the power controller. It does not deny a p-channel request to powerdown the cluster.

This bit resets to 0.

## Configurations

The AArch32 CLUSTERPWRDN register is architecturally mapped to the AArch64 CLUSTERPWRDN\_EL1 register.

## Usage Constraints

## Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPWRDN	x	x	0	-	RW	n/a	RW
CLUSTERPWRDN	x	0	1	-	RW	RW	RW
CLUSTERPWRDN	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

#### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.PWREN is 1 and ACTLR\_EL2.PWREN is 1, or ACTLR\_EL3.PWREN is 1 and SCR.NS is 0. If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.15 CLUSTERPWRSTAT, Cluster Power Status Register

The CLUSTERPWRSTAT register contains the status of the power features. This register is read-only write-ignores RO (WI), and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERPWRSTAT) and AArch64 (CLUSTERPWRSTAT\_EL1) registers.

### Bit field descriptions

CLUSTERPWRSTAT is a 32-bit register, and is part of SCU and L3 cache configuration registers.

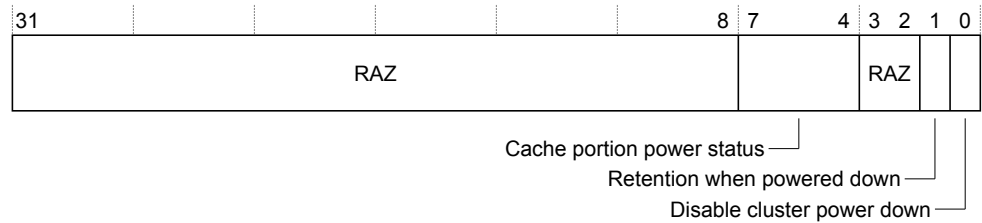


Figure B1-11 CLUSTERPWRSTAT bit assignments

#### RAZ, [31:8]

Read-As-Zero.

#### Cache portion power status, [7:4]

These bits indicate which cache portions are currently powered up and available. These bits can be used to determine when the state requested in bits [7:4] of the CLUSTERPWRCTLR has taken effect. The possible values are:

- 0b1111 Ways 0-15 are powered up.
- 0b0111 Ways 0-11 are powered up.
- 0b0011 Ways 0-7 are powered up.
- 0b0001 Ways 0-3 are powered up.
- 0b0000 No ways are powered up.

The reset value for these bits depends on the p-channel initialization state.

#### RAZ, [3:2]

Read-As-Zero.

#### Retention when powered down, [1]

Enabled memory retention when all cores are powered down. This bit is a combined version of all banked bits for each execution thread from the CLUSTERPWRDN register. The possible values are:

- 0 Disables memory retention when all cores are powered down.
- 1 Enables memory retention when all cores are powered down.

This bit resets to 0.

#### Disable cluster powerdown, [0]

Disabled cluster powerdown when all cores are powered down. This bit is a combined version of all banked per-thread bits from the CLUSTERPWRDN register. The possible values are:

- 0 Enables cluster powerdown when all cores are powered down.
- 1 Disables cluster powerdown when all cores are powered down.

This bit resets to 0.

### Configurations

The AArch32 CLUSTERPWRSTAT register is architecturally mapped to the AArch64 CLUSTERPWRSTAT\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPWRSTAT	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERPWRSTAT	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERPWRSTAT	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

#### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.PWREN is 1 and ACTLR\_EL2.PWREN is 1, or ACTLR\_EL3.PWREN is 1 and SCR.NS is 0. If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).



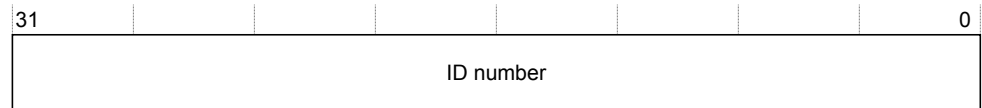
## B1.16 CLUSTERREVIDR, Cluster Revision ID Register

The CLUSTERREVIDR register enables ECO patches applied to the cluster level to be identified by the operating system. This register is read-only write-ignores RO (WI), and is common to all execution threads.

This description applies to both the AArch32 (CLUSTERREVIDR) and AArch64 (CLUSTERREVIDR\_EL1) registers.

### Bit field descriptions

CLUSTERREVIDR is a 32-bit register, and is part of SCU and L3 cache configuration registers.



**Figure B1-12 CLUSTERREVIDR bit assignments**

### ID number, [31:0]

Implementation-specific revision information. The reset value is determined by the specific DSU implementation.

0x00000000

Revision code is zero.

### Configurations

The AArch32 CLUSTERREVIDR register is architecturally mapped to the AArch64 CLUSTERREVIDR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERREVIDR	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERREVIDR	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERREVIDR	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

There are no traps and enables affecting this register.

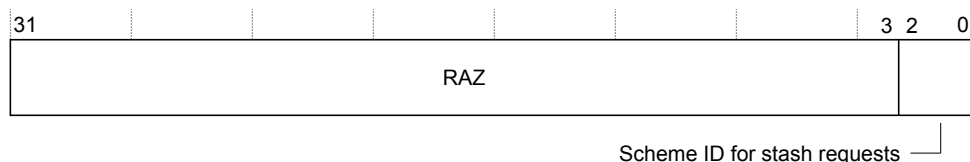
### B1.17 CLUSTERSTASHSID, Cluster Stash Scheme ID Register

The CLUSTERSTASHSID register provides the scheme ID for stash requests received from the interconnect.

This description applies to both the AArch32 (CLUSTERSTASHID) and AArch64 (CLUSTERSTASHID\_EL1) registers.

## Bit field descriptions

CLUSTERSTASHSID is a 32-bit register, and is part of SCU and L3 cache configuration registers.



**Figure B1-13 CLUSTERSTASHSID bit assignments**

**RAZ, [31:3]**

### Read-As-Zero.

**Scheme ID for stash requests, [2:0]**

Scheme ID for stash requests received from the interconnect.

These bits reset to 0b000.

## Configurations

The AArch32 CLUSTERSTASHSID is architecturally mapped to the AArch64 CLUSTERSTASHSID EL1 register.

## Usage Constraints

## Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERSTASHSID	x	x	0	-	RW	n/a	RW
CLUSTERSTASHSID	x	0	1	-	RW	RW	RW
CLUSTERSTASHSID	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

## Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.SMEN is 1 and ACTLR\_EL2.SMEN is 1, or ACTLR\_EL3.SMEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).

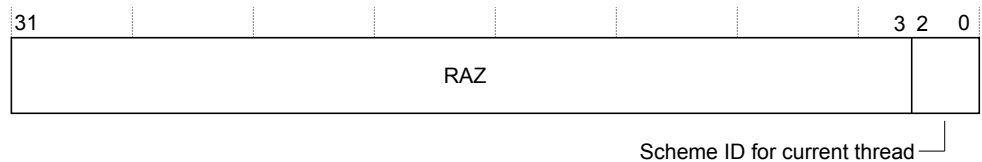
### B1.18 CLUSTERTHREADSID, Cluster Thread Scheme ID Register

The CLUSTERTHREADSID register is banked for each thread of execution. For multi-threaded cores the scheme ID is generated by a logical OR of the thread ID registers for that core.

This description applies to both the AArch32 (CLUSTERTHREADSID) and AArch64 (CLUSTERTHREADSID\_EL1) registers.

## Bit field descriptions

CLUSTERTHREADSID is a 32-bit register, and is part of SCU and L3 cache configuration registers.



**Figure B1-14 CLUSTERTHREADSID bit assignments**

**RAZ, [31:3]**

Read-As-Zero.

**Scheme ID for current thread,[2:0]**

Scheme ID for this thread.

These bits reset to 0b000.

## Configurations

The AArch32 CLUSTERTHREADSID is architecturally mapped to the AArch64 CLUSTERTHREADSID\_EL1 register.

## Usage Constraints

## Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERTHREADSID	x	x	0	-	RW	n/a	RW
CLUSTERTHREADSID	x	0	1	-	RW	RW	RW
CLUSTERTHREADSID	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

## Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.TSIDEN is 1 and ACTLR\_EL2.TSIDEN is 1, or ACTLR\_EL3.TSIDEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B1.19 CLUSTERTHREADSIDOVR, Cluster Thread Scheme ID Override Register

The CLUSTERTHREADSIDOVR register can be used by more privileged software, for example a hypervisor, to partition the scheme IDs. Therefore allowing the less privileged software to use only a subset of scheme IDs. This register is RW.

This description applies to both the AArch32 (CLUSTERTHREADSIDOVR) and AArch64 (CLUSTERTHREADSIDOVR\_EL1) registers.

### Bit field descriptions

CLUSTERTHREADSIDOVR is a 32-bit register, and is part of SCU and L3 cache configuration registers.

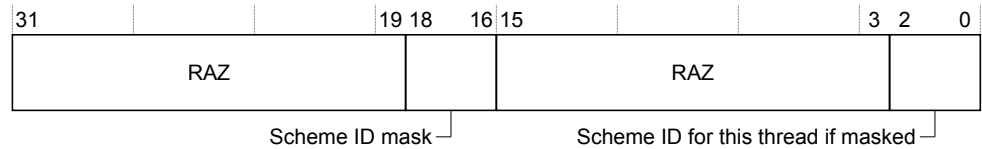


Figure B1-15 CLUSTERTHREADSIDOVR bit assignments

#### RAZ, [31:19]

Read-As-Zero.

#### Scheme ID mask, [18:16]

A bit set in the mask causes the matching bit to be taken from this register rather than from the CLUSTERTHREADSID register.

These bits reset to 0b000.

#### RAZ, [15:3]

Read-As-Zero.

#### Scheme ID for this thread if masked, [2:0]

Scheme ID for this thread if masked.

These bits reset to 0b000.

### Configurations

The AArch32 CLUSTERTHREADSIDOVR register is architecturally mapped to the AArch64 CLUSTERTHREADSIDOVR\_EL1 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERTHREADSIDOVR	x	x	0	-	RW	n/a	RW
CLUSTERTHREADSIDOVR	x	0	1	-	RW	RW	RW
CLUSTERTHREADSIDOVR	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3.SMEN is 1 and ACTLR\_EL2.SMEN is 1, or ACTLR\_EL3.SMEN is 1 and SCR.NS is 0.

If write access not permitted, then Trap to the lowest Exception level that denied access (EL2 or EL3).



# Chapter B2

## Error system Registers

This chapter describes the *ERR1\** error registers for the DSU.

It contains the following sections:

- *B2.1 About the error system registers* on page B2-136.
- *B2.2 Error system register summary* on page B2-137.
- *B2.3 ERR1CTLR, Error Record Control Register* on page B2-138.
- *B2.4 ERR1FR, Error Record Feature Register* on page B2-140.
- *B2.5 ERR1MISC0, Error Record Miscellaneous Register 0* on page B2-142.
- *B2.6 ERR1MISC1, Error Record Miscellaneous Register 1* on page B2-144.
- *B2.7 ERR1PFGCDNR, Error Pseudo Fault Generation Count Down Register* on page B2-145.
- *B2.8 ERR1PFGCTLR, Error Pseudo Fault Generation Control Register* on page B2-146.
- *B2.9 ERR1PFGFR, Error Pseudo Fault Generation Feature Register* on page B2-148.
- *B2.10 ERR1STATUS, Error Record Primary Status Register* on page B2-150.

## B2.1 About the error system registers

The error system registers are accessed by both the AArch32 ERX\* error registers and the AArch64 ERX\* error registers. The ERR1\* registers are agnostic to the architectural state. For example, if `ERRSELR==1` and `ERRSELR_EL1==1`, then `ERR1PFGF` is accessed by both `ERXPFGFR` and `ERXPFGFR_EL1`.

The chapter is presented as follows:

### Error system register summary

This section identifies the ERR1\* error registers and lists the corresponding ERX\* registers that can access them.

### Register descriptions

The remainder of the chapter provides register descriptions. They are listed in alphabetical order.

---

#### Note

The contents of the error system registers are preserved over a Warm reset.

---

See appropriate core Technical Reference Manual for more information about the ERX\* registers.



## B2.2 Error system register summary

This section lists the DSU ERR1\* error record registers that are accessed from the core AArch32 and AArch64 ERX\* error registers.

The ERR1\* registers are agnostic to the architectural state. For example, if ERRSELR==1 and ERRSELR\_EL1==1, then ERR1PFGF is accessed by both ERXPFGFR and ERXPFGFR\_EL1.

For a description of the ERX\* error registers see the related core documentation.

The following table describes the architectural error record registers in the DSU.

**Table B2-1 Architectural error system register summary**

Register mnemonic	Size	Register name and description	Access aliases from AArch32 and AArch64
ERR1CTLR	64	<i>B2.3 ERR1CTLR, Error Record Control Register on page B2-138</i>	ERXCTLR, ERXCTLR2, ERXCTLR_EL1
ERR1FR	64	<i>B2.4 ERR1FR, Error Record Feature Register on page B2-140</i>	ERXFR, ERXFR2, ERXFR_EL1
ERR1MISC0	64	<i>B2.5 ERR1MISC0, Error Record Miscellaneous Register 0 on page B2-142</i>	ERXMISC0, ERXMISC1, ERXMISC0_EL1
ERR1MISC1	64	<i>B2.6 ERR1MISC1, Error Record Miscellaneous Register 1 on page B2-144</i>	ERXMISC2 accesses bits [31:0], ERXMISC3 accesses bits [63:32], ERXMISC1_EL1
ERR1STATUS	32	<i>B2.10 ERR1STATUS, Error Record Primary Status Register on page B2-150</i>	ERXSTATUS, ERXSTATUS_EL1

The following table describes the error record registers that are IMPLEMENTATION DEFINED in the DSU.

**Table B2-2 Implementation defined error system register summary**

Register mnemonic	Size	Register name	Access aliases from AArch32 and AArch64
ERR1PFGCDNR	32	<i>B2.7 ERR1PFGCDNR, Error Pseudo Fault Generation Count Down Register on page B2-145</i>	ERXPFGCDNR, ERXPFGCDNR_EL1
ERR1PFGCTLR	32	<i>B2.8 ERR1PFGCTLR, Error Pseudo Fault Generation Control Register on page B2-146</i>	ERXPFGCTLR, ERXPFGCTLR_EL1
ERR1PFGFR	32	<i>B2.9 ERR1PFGFR, Error Pseudo Fault Generation Feature Register on page B2-148</i>	ERR1PFGFR, ERXPFGFR_EL1

## B2.3 ERR1CTL, Error Record Control Register

The ERR1CTL register contains enable bits for the node that writes to this record:

- Enabling error detection and correction.
- Enabling an error recovery interrupt.
- Enabling a fault handling interrupt.
- Enabling error recovery reporting as a read or write error response.

### Bit field descriptions

ERR1CTL is a 64-bit register and is part of the RAS registers functional group.

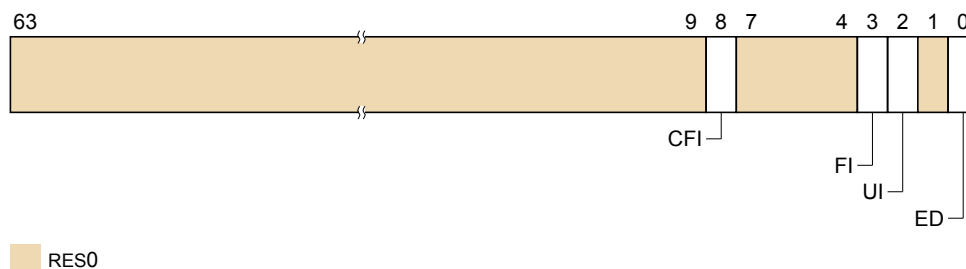


Figure B2-1 ERR1CTL bit assignments

#### RES0, [63:9]

RES0 Reserved.

#### CFI, [8]

Fault handling interrupt for corrected errors enable. The fault handling interrupt is generated when one of the standard CE counters on ERR1MISC0 overflows and the overflow bit is set. The possible values are:

- 0 Fault handling interrupt is not generated for corrected errors.
- 1 Fault handling interrupt is generated for corrected errors.

The interrupt is generated even if the error status is overwritten because the error record already records a higher priority error. If the node does not support this control, this bit is RES0.

#### Note

This condition applies to both reads and writes.

#### RES0, [7:4]

RES0 Reserved.

#### FI, [3]

Fault handling interrupt enable.

The fault handling interrupt is generated for all detected Deferred errors and Uncorrected errors. The possible values are:

- 0 Fault handling interrupt disabled.
- 1 Fault handling interrupt enabled.

#### UI, [2]

Uncorrected error recovery interrupt enable. When enabled, the error recovery interrupt is generated for all detected Uncorrected errors that are not deferred. The possible values are:

- 0 Error recovery interrupt is disabled.
- 1 Error recovery interrupt enabled.

---

**Note**

---

Applies to both reads and writes.

---

**RES0, [1]**

RES0      Reserved.

**ED, [0]**

Error reporting and logging enable. When reporting is disabled, the DSU will not record or signal errors, but it will continue to detect and correct errors. The possible values of this bit are:

- |   |  |
|---|--|
| 0 | Error reporting is disabled. In this state, uncorrectable errors might result in corrupt data being silently propagated. |
| 1 | Error reporting is enabled.  |

Correct error detection and correction codes are written for writes even when reporting is disabled.

**Configurations**

ERR1CTLR resets to 0x0000000000000000.

This register is accessible from the following registers when ERRSELR.SEL==1:

- [31:0]: ERXCTLR.
- [63:32]: ERXCTLR2.
- ERXCTLR\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.4 ERR1FR, Error Record Feature Register

The ERR1FR register defines which of the common architecturally defined features are implemented and, of the implemented features, which are software programmable.

### Bit field descriptions

ERR1FR is a 64-bit register, and is part of the *Reliability, Availability, Serviceability* (RAS) registers functional group.

The register is Read Only.

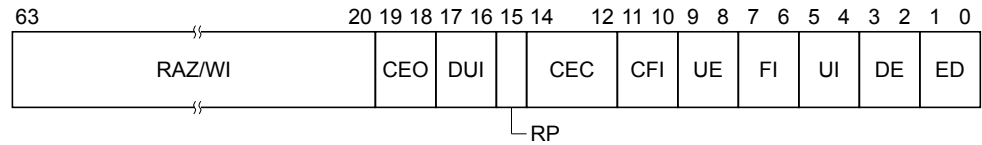


Figure B2-2 ERR1FR bit assignments

#### [63:20]

Read-as-zero/Write ignore.

#### CEO, [19:18]

Corrected Error Overwrite. The value is:

0b00 Counts CE if a counter is implemented and keeps the previous error status. If the counter overflows, or no counter is implemented, ERR0STATUS.OF is set to 1.

#### DUI, [17:16]

Error recovery interrupt for deferred errors. The value is:

0b00 The core or cluster does not support this feature.

#### RP, [15]

Repeat counter. The value is:

1 A first repeat counter and a second other counter are implemented. The repeat counter is the same size as the primary error counter.

#### CEC, [14:12]

Corrected Error Counter. The value is:

0b010 The node implements an 8-bit standard CE counter in ERR0MISC0[39:32].

#### CFI, [11:10]

Fault handling interrupt for corrected errors. The value is:

0b10 The node implements a control for enabling fault handling interrupts on corrected errors.

#### UE, [9:8]

In-band uncorrected error reporting. The value is:

0b01 The node implements in-band uncorrected error reporting, that is external aborts.

#### FI, [7:6]

Fault handling interrupt. The value is:

0b10 The node implements a fault handling interrupt and implements controls for enabling and disabling.

#### UI, [5:4]

Error recovery interrupt for uncorrected errors. The value is:

0b10 The node implements an error recovery interrupt and implements controls for enabling and disabling.

**DE, [3:2]**

Defers Errors enable. The value is:

0b01

Defers Errors are always enabled.

**ED, [1:0]**

Error detection and correction. The value is:

0b10

Error detection is controllable.

**Configurations**

This register is accessible from the following registers when ERRSEL.RSEL==1:

- [31:0]: ERXFR.
- [63:32]: ERXFR2.
- ERXFR\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.5 ERR1MISC0, Error Record Miscellaneous Register 0

The ERR1MISC0 register is an error syndrome register. It contains information on the corrected error count and information to identify where the error was detected. It also contains other state information not present in the corresponding status and address error record registers.

### Bit field descriptions

ERR1MISC0 is a 64-bit register, and is part of the *Reliability, Availability, Serviceability* (RAS) registers functional group.

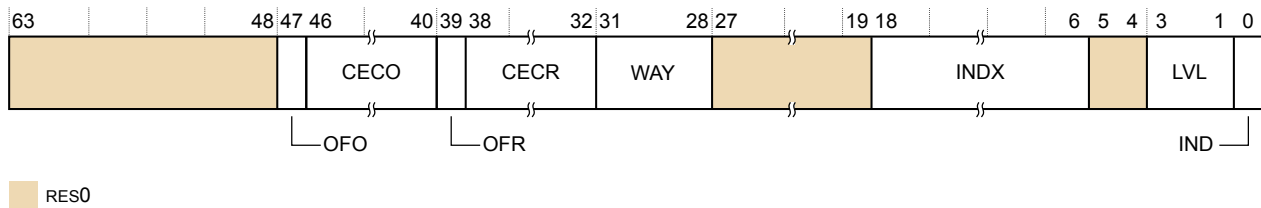


Figure B2-3 ERR1MISC0 bit assignments

#### [63:48]

Reserved, RES0.

#### OFO, [47]

Sticky overflow bit, other. The possible values are:

- 0 Other counter has not overflowed.
- 1 Other counter has overflowed.

The fault handling interrupt is generated when the corrected fault handling interrupt is enabled and either overflow bit is set to 1.

#### CECO, [46:40]

Corrected error count, other. Incremented for each Corrected error that does not match the recorded syndrome.

#### OFR, [39]

Sticky overflow bit, repeat. The possible values are:

- 0 Repeat counter has not overflowed.
- 1 Repeat counter has overflowed.

The fault handling interrupt is generated when the corrected fault handling interrupt is enabled and either overflow bit is set to 1.

#### CECR, [38:32]

Corrected error count, repeat. Incremented for the first recorded error, which also records other syndrome, and then again for each Corrected error that matches the recorded syndrome.

#### WAY, [31:28]

Indicates the way in the L3 tag RAM or snoop filter RAM that contained the error.

- For the L3 tag RAM, all four bits are used.
- For the snoop filter RAM, only bits[30:28] are used and bit[31] is set RES0.

#### [27:19]

Reserved, RES0.

**INDX, [18:6]**

Indicates the index that contained the error.

Upper bits of the index are unused depending on the cache size.

**[5:4]**

Reserved, RES0.

**LVL, [3:1]**

Indicates the level that contained the error. The value is:

0b010                                      Level 3.

**IND, [0]**

Indicates the type of cache that contained the error. The value is:

0                      L3 cache.

**Configurations**

ERR1MISC0 resets to 0x0000000000000000.

This register is accessible from the following registers when ERRSELR.SEL==1:

- [31:0]: ERXMISC0.
- [63:32]: ERXMISC1.
- ERXMISC0\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.6 ERR1MISC1, Error Record Miscellaneous Register 1

The ERR1MISC1 register is not used in the DSU and marked as RES0.

### Configurations

ERR1MISC1 is accessible from the following registers when ERRSELR.SEL==1:

- [31:0]: ERXMISC2.
- [63:32]: ERXMISC3.
- ERXMISC1\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

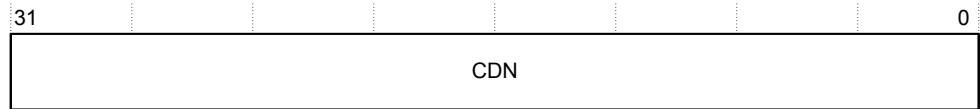


## B2.7 ERR1PFGCDNR, Error Pseudo Fault Generation Count Down Register

ERR1PFGCDNR is the DSU node register that generates one of the errors enabled in the corresponding ERR1PFGCTL register.

### Bit field descriptions

ERR1PFGCDNR is a 32-bit read/write register.



**Figure B2-4 ERR1PFGCDNR bit assignments**

### CDN, [31:0]

Count Down value. The reset value of the Error Generation Counter is used for the countdown.

### Configurations

ERR1PFGCDNR resets to 0x00000000.

There are no configuration options.

ERR1PFGCDNR is accessible from the following registers when ERRSELR.SEL==1:

- ERXPFGCDNR.
- ERXPFGCDNR\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.8 ERR1PFGCTLR, Error Pseudo Fault Generation Control Register

The ERR1PFGCTLR register is the DSU node register that enables controlled fault generation.

### Bit field descriptions

ERR1PFGCTLR is a 32-bit read/write register.

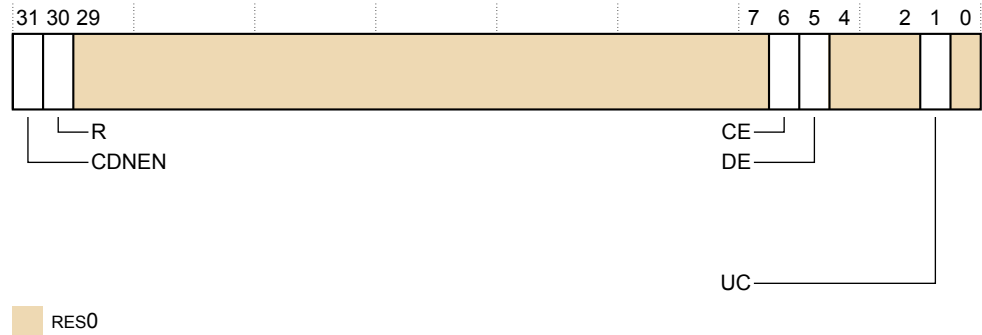


Figure B2-5 ERR1PFGCTLR bit assignments

### CDNEN, [31]

Count down enable. This bit controls transfers from the value that is held in the ERR1PFGCDNR into the Error Generation Counter and enables this counter to start counting down. The possible values are:

- 0 The Error Generation Counter is disabled.
- 1 The value held in the ERR1PFGCDNR register is transferred into the Error Generation Counter. The Error Generation Counter counts down.

### R, [30]

Restartable bit. When it reaches 0, the Error Generation Counter restarts from the ERR1PFGCDNR value or stops. The possible values are:

- 0 When it reaches 0, the counter stops.
- 1 When it reaches 0, the counter reloads the value that is stored in ERR1PFGCDNR and starts counting down again.

### [29:7]

Reserved, RES0.

### CE, [6]

Corrected error generation enable. The possible values are:

- 0 No corrected error is generated.
- 1 A corrected error might be generated when the Error Generation Counter is triggered.

### DE, [5]

Deferred Error generation enable. The possible values are:

- 0 No deferred error is generated.
- 1 A deferred error might be generated when the Error Generation Counter is triggered.

### [4:2]

Reserved, RES0.

### UC, [1]

Uncontainable error generation enable. The possible values are:

- 0 No uncontainable error is generated.

- 1 An uncontainable error might be generated when the Error Generation Counter is triggered.

[0]

Reserved, RES0.

### Configurations

ERR1PFGCTLR resets to 0x00000000.

There are no configuration notes.

ERR1PFGCTLR is accessible from the following registers when ERRSELR.SEL==1:

- ERXPFGCTLR.
- ERXPFGCTLR\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.9 ERR1PFGFR, Error Pseudo Fault Generation Feature Register

The ERR1PFGFR register is the DSU node register that defines which fault generation features are implemented.

### Bit field descriptions

ERR1PFGFR is a 32-bit read-only register.

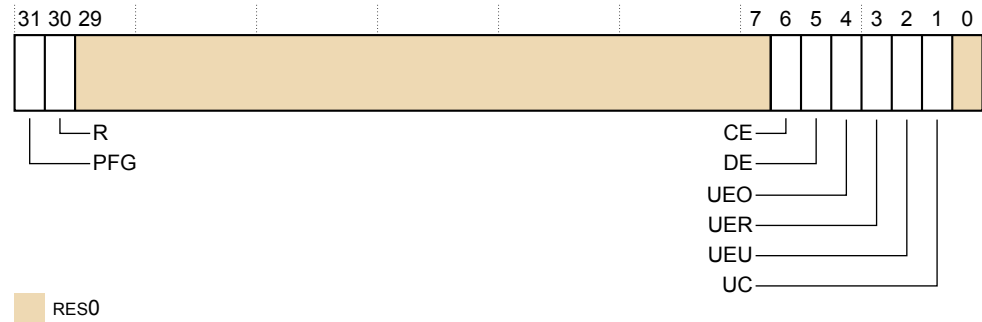


Figure B2-6 ERR1PFGFR bit assignments

#### PFG, [31]

Pseudo Fault Generation. The possible values are:

- 0 The node does not support fault injection.
- 1 The node implements a fault injection mechanism.

#### R, [30]

Restartable bit. When it reaches zero, the Error Generation Counter restarts from the ERR0PFGCDN value or stops. The possible values are:

- 0 The node does not support this feature.
- 1 This feature is controllable.

#### [29:7]

Reserved, RES0.

#### CE, [6]

Corrected Error generation. The possible values are:

- 0 The node does not support this feature.
- 1 This feature is controllable.

#### DE, [5]

Deferred Error generation. The possible values are:

- 0 The node does not support this feature.
- 1 This feature is controllable.

#### UEO, [4]

Latent or Restartable Error generation. The possible values are:

- 0 The node does not support this feature.
- 1 This feature is controllable.

#### UER, [3]

Signaled or Recoverable Error generation. The possible values are:

- 0 The node does not support this feature.

1 This feature is controllable.

**UEU, [2]**

Unrecoverable Error generation. The possible values are:

0 The node does not support this feature.

1 This feature is controllable.

**UC, [1]**

Uncontainable Error generation. The possible values are:

0 The node does not support this feature.

1 This feature is controllable.

**[0]**

Reserved, RES0.

**Configurations**

ERR1PFGFR resets to 0xC0000062.

There are no configuration notes.

ERR1PFGFR is accessible from the following registers when ERRSELR.SEL==1:

- ERXPFGFR.
- ERXPFGFR\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.

## B2.10 ERR1STATUS, Error Record Primary Status Register

The ERR1STATUS register contains the following information about the error record:

- Whether any error has been detected.
- Whether any detected error was not corrected and returned to a master.
- Whether any detected error was not corrected and deferred.
- Whether a second error of the same type was detected before software handled the first error.
- Whether any error has been reported.
- Whether the other error record registers contain valid information.

### Bit field descriptions

ERR1STATUS is a 32-bit register.

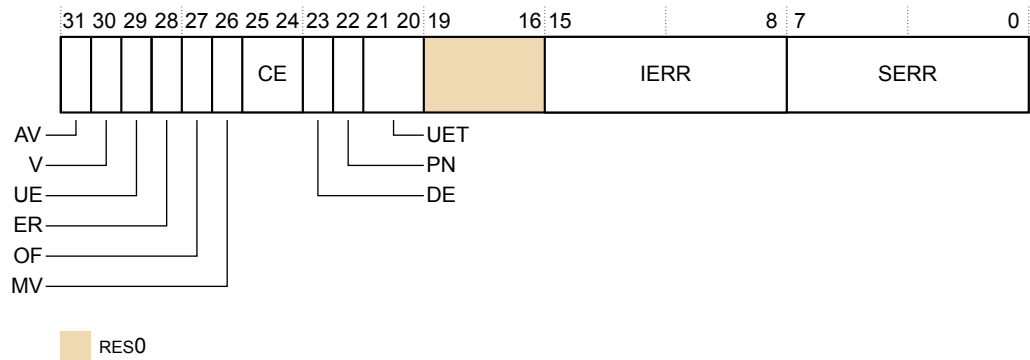


Figure B2-7 ERR1STATUS bit assignments

#### AV, [31]

Address Valid. The value is:

- 0 ERR1ADDR is not valid.

#### V, [30]

Status Register valid. The possible values are:

- 0 ERR1STATUS is not valid.
- 1 ERR1STATUS is valid. At least one error has been recorded.

#### UE, [29]

Uncorrected error. The possible values are:

- 0 No error that could not be corrected or deferred has been detected.
- 1 At least one error that could not be corrected or deferred has been detected. If error recovery interrupts are enabled, then the interrupt signal is asserted until this bit is cleared.

#### ER, [28]

Error reported. The value is:

- 0 No external abort has been reported.

#### OF, [27]

Overflow. The possible values are:

- 0
  - If UE == 1, then no error status for an Uncorrected error has been discarded.
  - If UE == 0 and DE == 1, then no error status for a Deferred error has been discarded.
  - If UE == 0, DE == 0, and CE != 0b00, then:
    - If a Corrected error counter is implemented, it has not overflowed.
    - If no Corrected error counter is implemented, no error status for a Corrected error has been discarded.

- 1 More than one error has occurred and so details of the other error have been discarded.

#### **MV, [26]**

Miscellaneous Registers Valid. The possible values are:

0 ERR1MISC0 and ERR1MISC1 are not valid.

- 1 Indicates that ERR1MISC0 contains additional information about any error recorded that is by this record.

#### **CE, [25:24]**

Corrected error. The possible values are:

0b00 No corrected errors are recorded.

0b10 At least one corrected error recorded.

#### **DE, [23]**

Deferred error. The possible values are:

0 No errors were deferred.

- 1 At least one error was not corrected and deferred by poisoning.

#### **PN, [22]**

Poison. The possible values are:

0 The DSU cannot distinguish a poisoned value from a corrupted value.

- 1 There is an uncorrected error due to data that was earlier poisoned.

#### **UET, [21:20]**

Uncorrected Error Type. The value is:

0b00 Uncontainable.

#### **[19:16]**

RES0.

Reserved.

#### **IERR, [15:8]**

An IMPLEMENTATION DEFINED error code. The possible values are:

0x0 No error, or error on other RAMs.

0x2 Error on a L3 snoop filter RAM.

#### **SERR, [7:0]**

Primary error code. The possible values are:

0x0 No error.

0x2 ECC error from internal data buffer.

0x6 ECC error on cache data RAM.

0x7 ECC error on cache tag or dirty RAM.

0x12 Bus error.

#### **Configurations**

ERR1STATUS resets to 0x00000000.

There are no configuration notes.

ERR1STATUS is accessible from the following registers when ERRSEL.RSEL==1:

- ERXSTATUS.
- ERXSTATUS\_EL1.

See the appropriate core Technical Reference Manual for information about these ERX\* registers.





# Chapter B3

## PMU Registers

This chapter describes the PMU registers for the DSU.

It contains the following sections:

- *B3.1 About the PMU registers on page B3-154.*
- *B3.2 AArch32 PMU register summary on page B3-155.*
- *B3.3 AArch64 PMU register summary on page B3-158.*
- *B3.4 CLUSTERPMCR, Cluster Performance Monitors Control Register on page B3-160.*
- *B3.5 CLUSTERPMMDCR, Cluster Monitor Debug Configuration Register on page B3-162.*
- *B3.6 CLUSTERPMCEID0, Cluster Common Event Identification Register 0 on page B3-163.*
- *B3.7 CLUSTERPMCEID1, Cluster Common Event Identification ID1 register on page B3-165.*
- *B3.8 PMEVTYPERn, Cluster Event Type Register on page B3-167.*

## B3.1 About the PMU registers

The chapter is presented as follows:

### **AArch32 PMU register summary**

This section lists the AArch32 PMU registers by access encoding.

### **AArch64 PMU register summary**

This section lists the AArch64 PMU registers by access encoding.

### **Register descriptions**

The remainder of the chapter provides generic register descriptions, that apply to both AArch32 and AArch64 registers. They are listed in alphabetical order.

## B3.2 AArch32 PMU register summary

This section lists the AArch32 PMU registers implemented in the DSU, sorted by access encoding.

Some of these registers have an equivalent register definition that is given in the PMU architecture. Where this occurs the corresponding register name in PMU architecture is given together with its reference. For example "See the PMCNTENSET register description in the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*".

**Table B3-1 DynaMiq Shared Unit AArch32 32-bit PMU registers**

Register mnemonic	Copro	CRn	Opc1	CRm	Opc2	Width	Register name	Description
CLUSTERPMCR	cp15	c15	0	c5	0	32	Cluster Performance Monitors Control Register	See <a href="#">B3.4 CLUSTERPMCR, Cluster Performance Monitors Control Register</a> on page B3-160
CLUSTERPMCNTENSET	cp15	c15	0	c5	1	32	Cluster Count Enable Set Register	See the PMCNTENSET register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMCNTENCLR	cp15	c15	0	c5	2	32	Cluster Count Enable Clear Register	See the PMCNTENCLR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMOVSSET	cp15	c15	0	c5	3	32	Cluster Overflow Flag Status Set	See the PMOVSSET register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMOVSCLR	cp15	c15	0	c5	4	32	Cluster Overflow Flag Status Clear	See the PMOVSCLR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMSELR	cp15	c15	0	c5	5	32	Cluster Event Counter Selection Register	See the PMSELR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMINTENSET	cp15	c15	0	c5	6	32	Cluster Interrupt Enable Set Register	See the PMINTENSET register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .

**Table B3-1 DynamIQ Shared Unit AArch32 32-bit PMU registers (continued)**

Register mnemonic	Copro	CRn	Opc1	CRm	Opc2	Width	Register name	Description
CLUSTERPMINTENCLR	cp15	c15	0	c5	7	32	Cluster Interrupt Enable Clear Register	See the PMINTENCLR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMCCNTR	cp15	c15	0	c6	0	64-bit register with only bits [31:0] accessible.	Cluster Performance Monitors Cycle Counter	See the PMCCNTR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMXEVTYPER	cp15	c15	0	c6	1	32	Cluster Selected Event Type and Filter Register	See the PMXEVTYPER register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMXVCNTR	cp15	c15	0	c6	2	32	Cluster Selected Event Counter Register	See the PMXVCNTR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMMDCR	cp15	c15	6	c6	3	32	Cluster Monitor Debug Configuration Register	See <a href="#">B3.5 CLUSTERPMMDCR, Cluster Monitor Debug Configuration Register on page B3-162</a>
CLUSTERPMCEID0	cp15	c15	0	c6	4	32	Cluster Common Event Identification ID0 Register	See <a href="#">B3.6 CLUSTERPMCEID0, Cluster Common Event Identification Register 0 on page B3-163</a>
CLUSTERPMCEID1	cp15	c15	0	c6	5	32	Cluster Common Event Identification ID1 Register	See <a href="#">B3.7 CLUSTERPMCEID1, Cluster Common Event Identification ID1 register on page B3-165</a>
CLUSTERPMCLAIMSET	cp15	c15	0	c6	6	32	Cluster Performance Monitor Claim Tag Set Register	See the CLAIMSET register in the <i>ARM® CoreSight™ Architecture Specification v3.0</i> .
CLUSTERPMCLAIMCLR	cp15	c15	0	c6	7	32	Cluster Performance Monitor Claim Tag Clear Register	See the CLAIMCLR register in the <i>ARM® CoreSight™ Architecture Specification v3.0</i> .

The following table describes the DynamIQ Shared Unit AArch32 64-bit PMU register.

**Table B3-2 DynaMlQ Shared Unit AArch32 64-bit PMU register**

Register mnemonic	Copro	Opc1	CRm	Width	Register name	Description
CLUSTERPMCCNTR	cp15	15	c15	64	Cluster Performance Monitors Cycle Counter	See the PMCCNTR register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .

## B3.3 AArch64 PMU register summary

This section lists the AArch64 PMU registers implemented in the DSU, sorted by access encoding.

Some of these registers have an equivalent register definition given in the PMU architecture. Where this occurs the corresponding register name in PMU architecture is given together with its reference. For example "See the PMCNTENSET register description in the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*".

**Table B3-3 DynamIQ Shared Unit AArch64 PMU registers**

Register mnemonic	Op0	CRn	Op1	CRm	Op2	Width	Register name	Description
CLUSTERPMCR_EL1	3	c15	0	c5	0	32	Cluster Performance Monitors Control Register	See <a href="#">B3.4 CLUSTERPMCR, Cluster Performance Monitors Control Register</a> on page B3-160
CLUSTERPMCNTENSET_EL1	3	c15	0	c5	1	32	Cluster Count Enable Set Register	See the PMCNTENSET_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMCNTENCLR_EL1	3	c15	0	c5	2	32	Cluster Count Enable Clear Register	See the PMCNTENCLR_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMOVSSET_EL1	3	c15	0	c5	3	32	Cluster Overflow Flag Status Set	See the PMOVSSET_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMOVSCLR_EL1	3	c15	0	c5	4	32	Cluster Overflow Flag Status Clear	See the PMOVSCLR_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMSELR_EL1	3	c15	0	c5	5	32	Cluster Event Counter Selection Register	See the PMSELR_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMINTENSET_EL1	3	c15	0	c5	6	32	Cluster Interrupt Enable Set Register	See the PMINTENSET_EL1 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMINTENCLR_EL1	3	c15	0	c5	7	32	Cluster Interrupt Enable Clear Register	See the PMINTENCLR_EL1 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .

Table B3-3 DynamIQ Shared Unit AArch64 PMU registers (continued)

Register mnemonic	Op0	CRn	Op1	CRm	Op2	Width	Register name	Description
CLUSTERPMCCNTR_EL1	3	c15	0	c6	0	64	Cluster Performance Monitors Cycle Counter	See the PMCCNTR_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMXEVTYPER_EL1	3	c15	0	c6	1	32	Cluster Selected Event Type and Filter Register	See the PMXEVTYPER_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMXVCNTR_EL1	3	c15	0	c6	2	32	Cluster Selected Event Counter Register	See the PMXVCNTR_EL0 register description in the <i>ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile</i> .
CLUSTERPMMDCR_EL3	3	c15	6	c6	3	32	Cluster Monitor Debug Configuration Register	See <a href="#">B3.5 CLUSTERPMMDCR</a> , <i>Cluster Monitor Debug Configuration Register</i> on page B3-162
CLUSTERPMCEID0_EL1	3	c15	0	c6	4	32	Cluster Common Event Identification ID0 Register	See <a href="#">B3.6 CLUSTERPMCEID0</a> , <i>Cluster Common Event Identification Register 0</i> on page B3-163.
CLUSTERPMCEID1_EL1	3	c15	0	c6	5	32	Cluster Common Event Identification ID1 Register	See <a href="#">B3.7 CLUSTERPMCEID1</a> , <i>Cluster Common Event Identification ID1 register</i> on page B3-165.
CLUSTERPMCLAIMSET_EL1	3	c15	0	c6	6	32	Cluster Performance Monitor Claim Tag Set Register	See the CLAIMSET register in the <i>ARM® CoreSight™ Architecture Specification v3.0</i> .
CLUSTERPMCLAIMCLR_EL1	3	c15	0	c6	7	32	Cluster Performance Monitor Claim Tag Clear Register	See the CLAIMCLR register in the <i>ARM® CoreSight™ Architecture Specification v3.0</i> .

## B3.4 CLUSTERPMCR, Cluster Performance Monitors Control Register

The CLUSTERPMCR register provides details of the Performance Monitors implementation, including the number of counters implemented. CLUSTERPMCR also provides configurations and controls to the counters.

### Bit field descriptions

CLUSTERPMCR is a 32-bit register, and is part of the PMU registers.

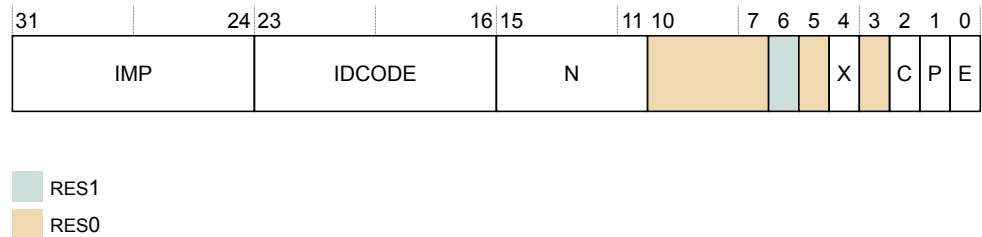


Figure B3-1 CLUSTERPMCR bit assignments

#### IMP, [31:24]

Indicates the implementer code. This value is:

0x41 ASCII character 'A' - implementer is ARM Limited.

This is a read-only field.

#### IDCODE, [23:16]

Identification code. This value is:

0x41

This is a read-only field.

#### N, [15:11]

Identifies the number of event counters implemented. The value is:

0b00110 Six event counters are implemented together with the cycle counter CLUSTERPMCCNTR.

#### RES0, [10:7]

RES0 Reserved.

#### RES1, [6]

RES1 Reserved.

#### RES0, [5]

RES0 Reserved.

#### X, [4]

RAZ/WI Read-As-Zero/Writes ignored.

#### RES0, [3]

RES0 Reserved.

#### C, [2]

Clock counter reset. This bit is WO. The effects of writing to this bit are:

0 No action.

1 Reset all counters, not including CLUSTERPMCCNTR, to zero.



This bit is always RAZ.

#### P, [1]

Event counter reset. This bit is WO. The effects of writing to this bit are:

- 0 No action.
- 1 Reset all event counters, not including CLUSTERPMCCNTR, to zero.

Resetting the event counters does not clear any overflow bits to 0.

This bit is always RAZ.

#### E, [0]

Counters enable. The possible values are:

- 0 All counters including CLUSTERPMCCNTR are disabled.
- 1 All counters are enabled by CLUSTERPMCNTENSET.

#### Configurations

The AArch32 CLUSTERPMCR register is architecturally mapped to the AArch64 CLUSTERPMCR\_EL1 register.

#### Usage Constraints

##### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPMCR	x	x	0	-	RW	n/a	RW
CLUSTERPMCR	x	0	1	-	RW	RW	RW
CLUSTERPMCR	x	1	1	-	n/a	RW	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

#### Traps and enables

This register is write accessible in EL1 if ACTLR\_EL3[12] is 1 and ACTLR\_EL2[12] is 1, or ACTLR\_EL3[12] is 1 and SCR.NS is 0. If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B3.5 CLUSTERPMMDCR, Cluster Monitor Debug Configuration Register

The CLUSTERPMMDCR register defines which common architectural and common microarchitectural feature events are implemented.

### Bit field descriptions

CLUSTERPMMDCR is a 32-bit register, and is part of the PMU registers.

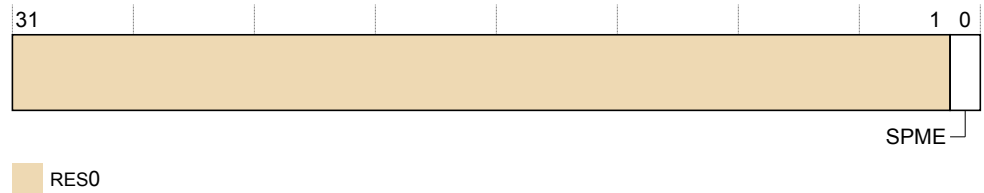


Figure B3-2 CLUSTERPMMDCR bit assignments

### RES0, [31:1]

RES0 Reserved.

### SPME, [0]

Secure Performance Monitors enable. This allows the counting of Secure events. The possible values are:

- 0 Counting of secure events prohibited.
- 1 Counting of secure events allowed.

This bit resets to zero.

### Configurations

The AArch32 CLUSTERPMMDCR register is architecturally mapped to the AArch64 CLUSTERPMMDCR\_EL3 register.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPMMDCR	x	x	0	-	n/a	n/a	RW
CLUSTERPMMDCR	x	0	1	-	n/a	n/a	RW
CLUSTERPMMDCR	x	1	1	-	n/a	n/a	RW

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

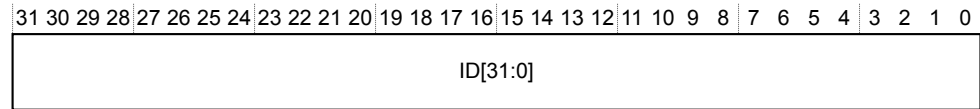
### Traps and enables

This register is only accessible from EL3.

## B3.6 CLUSTERPMCEID0, Cluster Common Event Identification Register 0

The CLUSTERPMCEID0 register defines which common architectural and common microarchitectural feature events are implemented.

### Bit field descriptions



**Figure B3-3 CLUSTERPMCEID0 bit assignments**

See the PMCEID0 register description in the accompanying core for more information.

### CE[31:0], [31:0]

Common architectural and microarchitectural feature events that can be counted by the PMU event counters.

The following table shows the CLUSTERPMCEID0 bit assignments with event implemented or not implemented when the associated bit is set to 1 or 0. See the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile* for more information about these events.

**Table B3-4 PMU events**

Bit	Event number	Event mnemonic	Description
[30]	0x1E	CHAIN	Chain. For odd-numbered counters, counts when for each overflow of the preceding even-numbered counter. For even-numbered counters, does not count: 1 This event is implemented.
[29]	0x1D	BUS_CYCLES	Bus cycle: 1 This event is implemented.
[26]	0x1A	MEMORY_ERROR	Local memory error: 1 This event is implemented.
[25]	0x19	BUS_ACCESS	Bus access: 1 This event is implemented.
[17]	0x11	CPU_CYCLES	Cycle: 1 This event is implemented.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPMCEID0	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERPMCEID0	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERPMCEID0	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

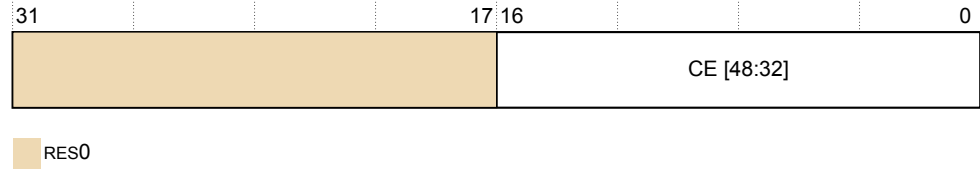
**Traps and enables**

This register is write accessible in EL1 if ACTLR\_EL3[12] is 1 and ACTLR\_EL2[12] is 1, or ACTLR\_EL3[12] is 1 and SCR.NS is 0. If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B3.7 CLUSTERPMCEID1, Cluster Common Event Identification ID1 register

The CLUSTERPMCEID1 register defines which common architectural and common microarchitectural feature events are implemented.

### Bit field descriptions



**Figure B3-4 CLUSTERPMCEID1 bit assignments**

See the PMCEID1 register description in the accompanying core for more information.

### RES0, [31:17]

RES0 Reserved.

### CE[48:32], [16:0]

Common architectural and microarchitectural feature events that can be counted by the PMU event counters.

For each bit described in the following table, the event is implemented if the bit is set to 1, or not implemented if the bit is set to 0.

**Table B3-5 PMU common events**

Bit	Event number	Event mnemonic	Description
[12]	0x2C	L3D_CACHE_WB	Attributable Level 3 data or unified cache writeback. 1 This event is implemented.
[11]	0x2B	L3D_CACHE	Attributable Level 3 data or unified cache access. 1 This event is implemented.
[10]	0x2A	L3D_CACHE_REFILL	Attributable Level 3 data or unified cache refill. 1 This event is implemented.
[9]	0x29	L3D_CACHE_ALLOCATE	Attributable Level 3 data or unified cache allocation without refill. 1 This event is implemented.

### Usage Constraints

#### Accessibility

This register is accessible in software as follows:

<systemreg>	Control			Accessibility			
	E2H	TGE	NS	EL0	EL1	EL2	EL3
CLUSTERPMCEID1	x	x	0	-	RO/WI	n/a	RO/WI
CLUSTERPMCEID1	x	0	1	-	RO/WI	RO/WI	RO/WI
CLUSTERPMCEID1	x	1	1	-	n/a	RO/WI	RO/WI

'n/a' Not accessible. The PE cannot be executing at this Exception level, so this access is not possible.

**Traps and enables**

This register is write accessible in EL1 if ACTLR\_EL3[12] is 1 and ACTLR\_EL2[12] is 1, or ACTLR\_EL3[12] is 1 and SCR.NS is 0. If write access not possible, then Trap to the lowest Exception level that denied access (EL2 or EL3).

## B3.8 PMEVTYPERn, Cluster Event Type Register

The PMEVTYPERn register defines which common architectural and common microarchitectural feature events are implemented.

### Bit field descriptions

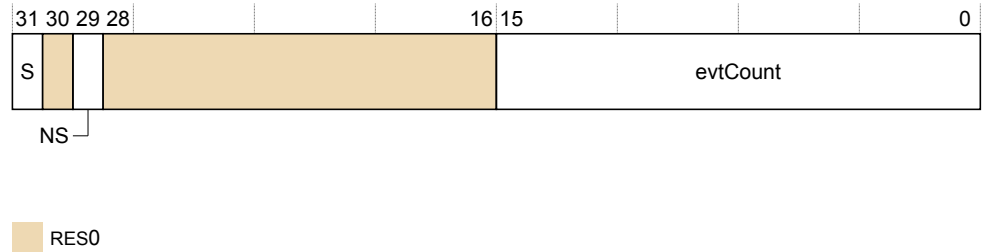


Figure B3-5 PMEVTYPERn bit assignments

#### S, [31]

Secure events filtering bit. Controls counting of events that are generated by Secure transactions. The possible values are:

- 0 Count Secure events.
- 1 Do not count Secure events.

#### RES0, [30]

RES0 Reserved.

#### NS, [29]

Non-secure events filtering bit. Controls counting of events that are generated by Non-secure transactions. The possible values are:

- NS == S If the value of this bit equals the value of S,[31] bit then count Non-secure events.
- NS != S If the value of this bit does not equal the value of S,[31] bit then do not count Non-secure events.

#### RES0, [28:16]

RES0 Reserved.

#### evtCount, [15:0]

Event number. For the list of implemented events, see [C2.3 PMU events on page C2-184](#).

If evtCount is programmed to an event that is not implemented, no events are counted.

### Usage Constraints

#### Accessing the PMEVTYPERn register

This register is accessible using the CLUSTERPMXEVTYPER register. It is not directly accessible as a system or CP15 register.





## Part C

### **Debug**



# Chapter C1

## Debug

This chapter describes the debug features of the DSU and the associated DebugBlock component.

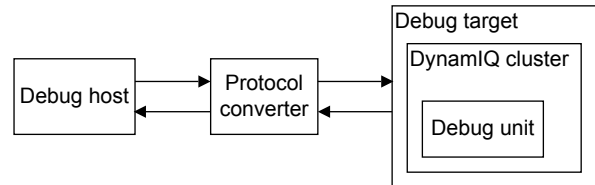
It contains the following sections:

- [C1.1 About debug methods on page C1-172.](#)
- [C1.2 Terminology on page C1-173.](#)
- [C1.3 About the DebugBlock on page C1-174.](#)
- [C1.4 DebugBlock components on page C1-176.](#)
- [C1.5 About the Embedded Cross-Trigger on page C1-177.](#)
- [C1.6 CTI triggers on page C1-179.](#)

## C1.1 About debug methods

The DSU along with its associated cores is part of a debug system that supports both self-hosted and external debug.

The following figure shows a typical external debug system.



**Figure C1-1 External debug system**

### Debug host

A computer, for example a personal computer, that is running a software debugger such as the DS-5 Debugger. With the debug host, you can issue high-level commands, such as setting a breakpoint at a certain location or examining the contents of a memory address.

### Protocol converter

The debug host sends messages to the debug target using an interface such as Ethernet. However, the debug target typically implements a different interface protocol. A device such as DSTREAM is required to convert between the two protocols.

### Debug target

The lowest level of the system implements system support for the protocol converter to access the debug unit using the *Advanced Peripheral Bus* (APB) slave interface. An example of a debug target is a development system with a test chip or a silicon part with a DSU.

### Debug unit

Helps debugging software that is running on the core:

- DSU and external hardware based around the core.
- Operating systems.
- Application software.

With the debug unit, you can:

- Stop program execution.
- Examine and alter process and coprocessor state.
- Examine and alter memory and the state of the input or output peripherals.
- Restart the PE.

For self-hosted debug, the debug target runs additional debug monitor software that runs on the core in the cluster. This way, it does not require expensive interface hardware to connect a second host computer.

## C1.2 Terminology

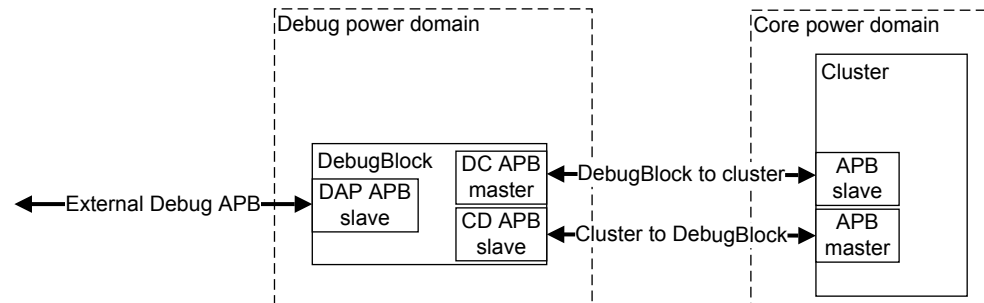
The debug system supports both single and multi-threaded cores.

The ARM architecture allows for cores to be single, or multi-threaded. A *Processing Element* (PE) performs a thread of execution. A single-threaded core has one PE and a multi-threaded core has two or more PEs. Because the debugging system allows individual threads to be debugged, the term PE is used throughout this chapter. Where a reference to a core is made, the core can be a single, or multi-threaded core.

## C1.3 About the DebugBlock

The DebugBlock combines the functions, registers, and interfaces that are required for debug over powerdown. It is provided as a separate component to allow implementation in a separate power domain from the cluster. Having a separate debug power domain allows the connection to a debugger be maintained while the cores and cluster are powered down.

The following diagram shows how the DebugBlock is connected to the cluster.



**Figure C1-2 Debug APB connections**

The DebugBlock has three APB interfaces:

### External Debug APB (DAP APB)

An APB slave interface, allowing communication with an external debugger, for example through a CoreSight *Debug Access Port*(DAP).

All debug register read and write requests from an external debugger are received on this bus.

### DebugBlock to cluster (DC APB)

An APB master interface that is connected to the cluster. It sends all debug register read and write requests to the cluster.

CTI output trigger events are sent to the cluster as trigger requests on this bus.

### Cluster to DebugBlock (CD APB)

An APB slave interface that is connected to the cluster. It receives CTI input trigger event requests from the cluster.

## Debug register reads and writes

The DebugBlock holds all the debug registers that are implemented in the Debug power domain. Registers implemented in the Debug power domain are specified in the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*.

Accesses through the DAP APB interface to Debug domain registers are handled internally by the DebugBlock. Accesses through the DAP APB interface to Core power domain registers are passed on to the cluster through the DC APB interface.

## CTI trigger events

Trigger events are transferred between the DebugBlock and cluster through the CD APB and DC APB interfaces.

### Input trigger events

Input trigger events are sent from the cluster to the CTIs through the CD APB as write transactions.

### Output trigger events

Output trigger events are sent from the CTIs to the cluster through the DC APB as write transactions.

## **DebugBlock power states**

The DebugBlock supports two power modes: ON, and OFF. The DebugBlock sends powerup and powerdown requests to the external power controller on the Q-Channel. In the OFF mode, the DebugBlock does not initiate any APB accesses and all incoming APB accesses to the DebugBlock receive a PSLVERR response.

## C1.4 DebugBlock components

The components are:

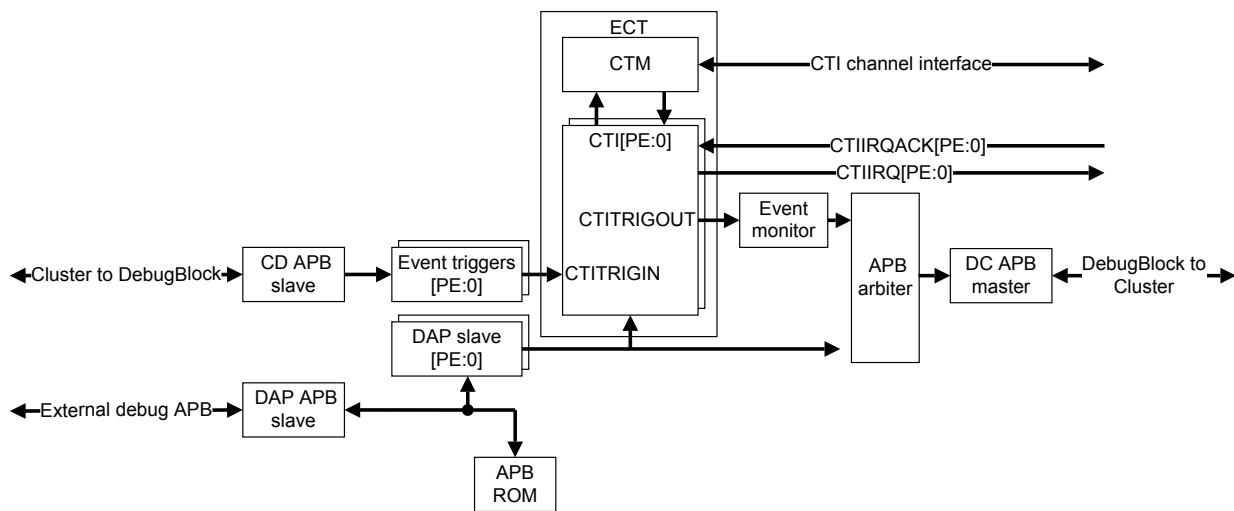


Figure C1-3 DebugBlock block diagram

### ECT

The DebugBlock implements the *Embedded Cross-Trigger (ECT)*.

### APB ROM

The APB ROM table complies with the *ARM® CoreSight™ Architecture Specification v3.0* and holds the address decoding for each debug component in the DebugBlock and the cluster. Both v7 and v8 debug address maps are supported.

### Event monitor

The event monitor converts changes in CTI output triggers to APB write transactions.

### Event triggers

The event triggers convert APB write transactions to CTI input triggers.

### APB arbiter

The DC APB transfers both register accesses and CTI output trigger events. The APB arbiter multiplexes the two sources of transactions.

### DAP slave

The DAP slave holds copies of registers in the debug power domain.

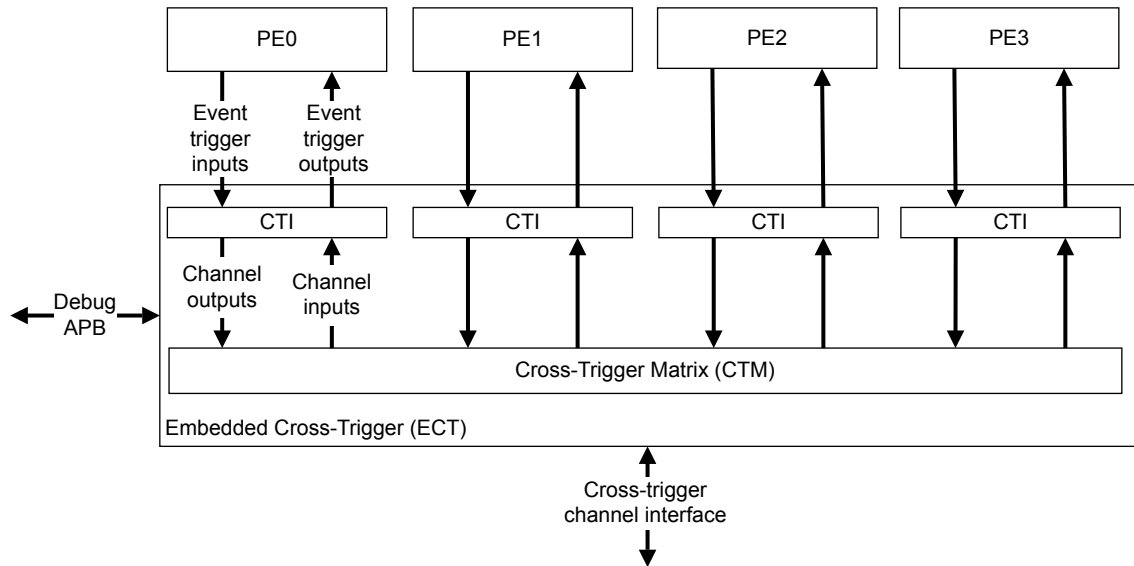


## C1.5 About the Embedded Cross-Trigger

The *Embedded Cross-Trigger* (ECT) allows debug events to be sent between PEs.

The ECT provides a *Cross Trigger Interface* (CTI) for each PE in the cluster. The CTIs are interconnected through a *Cross Trigger Matrix* (CTM) to send debug and trace events between PEs.

The following diagram shows a conceptual view of the trigger event inputs and outputs between the PEs and ECT.



**Figure C1-4 Embedded Cross-Trigger concept**

The CTIs selectively send trigger events to the CTM on their respective channel outputs. The CTIs receive trigger events from the CTM on their channel inputs.

Trigger events are transferred between CTIs over the channel interface. The CTM connects the channel interface to the channel inputs and channel outputs of the CTIs.

### External interfaces

The external cross-trigger channel interface, from the CTM, allows cross-triggering between SoC external devices.

The Debug APB provides access to the CTI registers. This allows an external debugger to configure the trigger event routing, and send events to PEs, for example, to put a PE into Debug state.

### CTI registers

Registers in the CTI:

- Control the mapping of the input trigger events to channel outputs.
- Control the mapping of the channel inputs to output trigger events.
- Capture the state of input and output trigger events.
- Set, clear, or pulse output trigger events.

### C1.5.1 Supported debug and trace trigger events

The CTIs each have eight input and output trigger events that are mapped onto the debug and trace events in the PEs.

The debug and trace trigger events from the CTI are:

**Debug request trigger event**

A trigger event sent from the CTI to the PE to force the PE into Debug state.

**Restart request trigger event**

A trigger event sent from the CTI to the PE to request the PE to exit Debug state.

**Generic CTI interrupt trigger event**

Four trigger events sent from the CTI to the GIC.

**ETM trace input trigger events**

Two trigger events sent from the CTI to the ETM trace in the PE.

The Debug and trace events to the CTI are:

**Cross-halt trigger event**

A trigger event sent from the PE to the CTI when the PE enters Debug state.

**Performance Monitors overflow trigger event**

A trigger event sent from the PE to the CTI when a PMU counter overflows.

**ETM trace output trigger events**

Four trigger events sent from the ETM in the PE to the CTI.

**ELA output trigger events**

Two trigger event sent from the ELA in the core to the CTI.

## C1.6 CTI triggers

Events are mapped onto CTI input and output triggers. All PEs in the cluster have the same mapping.

### CTI input trigger events

The following table shows how events are mapped onto CTI input triggers.

**Table C1-1 Allocation of CTI input trigger events**

Trigger number	Source	Destination	Type	Event description
0	PE	CTI	Pulse	Cross-halt trigger event
1				Performance Monitors Overflow trigger event
2-3	-	-	-	Reserved
4-7	ETM	CTI	Pulse	ETM Trace Output trigger events
8-9	ELA	CTI		ELA <b>CTTRIGOUT</b> [1:0] trigger events

### CTI output trigger events

The following table shows how events are mapped onto CTI output triggers.

**Table C1-2 Allocation of CTI output trigger events**

Trigger number	Source	Destination	Type	Event description
0	CTI	PE	Level	Debug Request trigger event
1			Pulse	Restart Request trigger event
2	CTI	GIC	Pulse	Generic CTI Interrupt trigger event
3	-	-	-	Reserved
4-7	CTI	ETM	Pulse	Generic Trace External Input trigger events
8-9	CTI	ELA	Pulse	ELA <b>CTTRIGIN</b> [1:0] trigger events



# Chapter C2

## PMU

This chapter describes the *Performance Monitor Unit* (PMU).

It contains the following sections:

- [C2.1 About the PMU](#) on page C2-182.
- [C2.2 PMU functional description](#) on page C2-183.
- [C2.3 PMU events](#) on page C2-184.
- [C2.4 PMU interrupts](#) on page C2-187.

## C2.1 About the PMU

The DynamIQ Shared Unit includes performance monitors that enable you to gather various statistics on the operation of the memory of the cluster during runtime. These provide useful information about the behavior of the cluster that you can use when debugging or profiling code.

The PMU provides six counters. Each counter can count any of the events available in the cluster. The absolute counts that are recorded might vary because of pipeline effects. This has negligible effect except in cases where the counters are enabled for a very short time.

## C2.2 PMU functional description

This section describes the functionality of the PMU.

The PMU includes the following interfaces and counters:

### **Event interface**

Events from all other units from across the design are provided to the PMU.

### **System register**

You can program the PMU registers using the system registers.

### **Counters**

The PMU has 32-bit counters that increment when they are enabled, based on events, and a 64-bit cycle counter.

### **PMU register interfaces**

The DynamIQ Shared Unit supports access to the performance monitor registers from the internal system register interface.

### **Related references**

[Chapter B3 PMU Registers on page B3-153.](#)

## C2.3 PMU events

The following table shows the events that are generated and the numbers that the PMU uses to reference the events.

**Table C2-1 PMU events**

PMU event number	Event mnemonic	Event Name	Description
0x0011	CYCLES	Cycle	Cycle counter.
0x0019	BUS_ACCESS	Bus access	Counts every beat of data that is transferred over the data channels between the SCU and the interconnect.  This event counts the sum of BUS_ACCESS_RD and BUS_ACCESS_WR.
0x001A	MEMORY_ERROR	Local memory error	Counts every Correctable or Uncorrectable memory error (ECC or parity) in the protected RAMs.
0x001D	BUS_CYCLES	Bus cycles	ACE or CHI bus cycle counter.
0x001E	CHAIN	Chain	Odd performance counter chain mode.
0x0029	L3D_CACHE_ALLOCATE	Level 3 unified cache allocation without refill	Counts every full cache line write into the L3 cache which does not cause a linefill.
0x002A	L3D_CACHE_REFILL	Level 3 unified cache refill	Counts every cacheable read transaction issued to the interconnect.  This event counts the sum of L3D_CACHE_REFILL_RD and L3D_CACHE_REFILL_WR.
0x002B	L3D_CACHE	Level 3 unified cache access	Counts every cacheable read or write transaction issued to the SCU.  This event counts the sum of L3D_CACHE_RD and L3D_CACHE_WR.
0x002C	L3D_CACHE_WB	Level 3 unified cache write-back	Counts every write-back from the L3 cache.
0x0060	BUS_ACCESS_RD	Bus access, read	Counts every beat of data transferred over the read data channel between the SCU and the interconnect.
0x0061	BUS_ACCESS_WR	Bus access, write	Counts every beat of data transferred over the write data channel between the SCU and the interconnect.
0x0062	BUS_ACCESS_SHARED	Bus access, shared	Counts every beat of shared data transferred over the data channels between the SCU and the interconnect.
0x0063	BUS_ACCESS_NOT_SHARED	Bus access, not shared	Counts every beat of not shared data transferred over the write data channel between the SCU and the interconnect.
0x0064	BUS_ACCESS_NORMAL	Bus access, normal	Counts every beat of normal data transferred over the write data channel between the SCU and the interconnect.
0x0065	BUS_ACCESS_PERIPH	Bus access, periph	Counts every beat of device data transferred over the write data channel between the SCU and the interconnect.



Table C2-1 PMU events (continued)

PMU event number	Event mnemonic	Event Name	Description
0x00A0	L3D_CACHE_RD	Level 3 unified cache access, read	Counts every cacheable read transaction that is issued to the SCU. Prefetches and stashes are not counted.
0x00A1	L3D_CACHE_WR	Level 3 unified cache access, write	Counts every cacheable write transaction issued to the SCU.
0x00A2	L3D_CACHE_REFILL_RD	Level 3 unified cache refill, read	Counts every cacheable read transaction issued to the interconnect caused by a read transaction. Prefetches and stashes are not counted.
0x00A3	L3D_CACHE_REFILL_WR	Level 3 unified cache refill, write	Counts every cacheable read transaction issued to the interconnect caused by a write transaction.
0x0119	ACP_ACCESS	ACP access	Counts every beat of data transferred over the data channels between the SCU and the accelerated coherency port.  This event counts the sum of ACP_ACCESS_RD and ACP_ACCESS_WR.
0x011D	ACP_CYCLES	ACP cycles	ACP cycle counter.
0x0160	ACP_ACCESS_RD	ACP access, read	Counts every beat of data transferred over the read data channel between the SCU and the peripheral port.
0x0161	ACP_ACCESS_WR	ACP access, write	Counts every beat of data transferred over the write data channel between the SCU and the peripheral port.
0x0219	PP_ACCESS	Peripheral port access	Counts every beat of data transferred over the data channels between the SCU and the peripheral port.  This event counts the sum of PP_ACCESS_RD and PP_ACCESS_WR.
0x021D	PP_CYCLES	Peripheral port cycles	Peripheral port cycle counter.
0x0260	PP_ACCESS_RD	Peripheral port access, read	Counts every beat of data transferred over the read data channel between the SCU and the peripheral port.
0x0261	PP_ACCESS_WR	Peripheral port access, write	Counts every beat of data transferred over the write data channel between the SCU and the peripheral port.
0x00C0	SCU_SNP_ACCESS	SNP access	Counts every snoop request.
0x00C1	SCU_SNP_EVICT	SNP evictions	Counts every invalidating snoop request that causes an L3 cache eviction.
0x00C2	SCU_SNP_NO_CPU_SNP	SNP, no CPU snoop	Count for every snoop request that completes without needing to snoop a core.
0x0500	SCU_PFTCH_CPU_ACCESS	Prefetch access, CPU	Counts every stash transaction originating from a core.
0x0501	SCU_PFTCH_CPU_MISS	Prefetch data miss, CPU	Counts every stash transaction originating from a core where data was read in from outside the cluster.
0x0502	SCU_PFTCH_CPU_HIT	Prefetch data hit, CPU	Counts every stash transaction originating from a core where the stash hit in the cluster.

Table C2-1 PMU events (continued)

PMU event number	Event mnemonic	Event Name	Description
0x0503	SCU_PFTCH_CPU_MATCH	Prefetch match, CPU	Counts every completed stash transaction originating from a core that is matched by a compatible read request. This includes one caused by a stash to the core, before the stash times-out and is allocated into the L3 cache.
0x0504	SCU_PFTCH_CPU_KILL	Prefetch terminate, CPU	Counts every killed stash transaction originating from a core that is terminated due to an incompatible match.
0x0510	SCU_STASH_ICN_ACCESS	Stash access, ICN	Counts every stash transaction originating from the interconnect.
0x0511	SCU_STASH_ICN_MISS	Stash data miss, ICN	Counts every stash transaction originating from the interconnect which utilizes a data pull, or is added to the stash queue and later issues a read.
0x0512	SCU_STASH_ICN_HIT	Stash data hit, ICN	Counts every non-invalidating stash transaction originating from the interconnect which hits in the cluster.
0x0513	SCU_STASH_ICN_MATCH	Stash match, ICN	Counts every completed stash transaction originating from the interconnect which is matched by a compatible read request. This includes one caused by a stash to the core, before the stash times out and is allocated into the L3 cache.
0x0514	SCU_STASH_ICN_KILL	Stash terminated, ICN	Counts every killed stash transaction originating from the interconnect that is terminated due to an incompatible match.
0x00D0	SCU_HZD_ADDRESS	Arbitration hazard, address	Counts every flush caused by an address hazard.

## C2.4 PMU interrupts

The DSU asserts the **nCLUSTERPMUIRQ** signal when the PMU generates an interrupt.

You can route this signal to an external interrupt controller for prioritization and masking. This is the only mechanism that signals this interrupt to a core.



# Chapter C3

## Debug Registers

This chapter describes the debug registers for the DSU.

It contains the following sections:

- *C3.1 Debug memory map on page C3-190.*
- *C3.2 CTI register summary on page C3-197.*
- *C3.3 CTIPIDR0, CTI Peripheral Identification Register 0 on page C3-199.*
- *C3.4 CTIPIDR1, CTI Peripheral Identification Register 1 on page C3-200.*
- *C3.5 CTIPIDR2, CTI Peripheral Identification Register 2 on page C3-201.*
- *C3.6 CTIPIDR3, CTI Peripheral Identification Register 3 on page C3-202.*
- *C3.7 CTIPIDR4, CTI Peripheral Identification Register 4 on page C3-203.*
- *C3.8 CTIITCTRL, CTI Integration Mode Control Register on page C3-204.*
- *C3.9 CTIDEVAFF0, Cluster CTI Device Affinity register 0 on page C3-205.*
- *C3.10 CTIDEVID, CTI Device Identification Register on page C3-206.*
- *C3.11 External register access permissions on page C3-208.*

## C3.1 Debug memory map

The debug memory map holds the base addresses for each debug component that is connected to the Debug APB.

Each component in the table requires 4KB, and uses the bottom 4KB of each 64KB region. The remaining 60KB of each region is reserved.

In the tables, individual *Processing Elements* (PE) are identified. For a single-threaded core, the PE number is the same as the core number. Only eight cores are supported.

The following table shows the address mapping for the DSU and the individual core debug APB components when configured for v8 Debug memory map. If an address range is not mapped to a component, it is indicated as reserved. For more information, see *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*.

**Table C3-1 Address mapping for APB components on 64KB pages**

Address	Component
0x000000	ROM table
0x010000	PE0 Debug
0x020000	PE0 CTI
0x030000	PE0 PMU
0x040000	PE0 ETM
0x050000-0x0BFFFF	Reserved, RES0
0x0C0000	PE0 ELA
0x0D0000	Cluster ELA
0x0E0000	Cluster CTI
0x0F0000-0x10FFFF	Reserved, RES0
0x110000	PE1 Debug
0x120000	PE1 CTI
0x130000	PE1 PMU
0x140000	PE1 ETM
0x150000-0x1BFFFF	Reserved, RES0
0x1C0000	PE1 ELA
0x1D0000-0x20FFFF	Reserved, RES0
0x210000	PE2 Debug
0x220000	PE2 CTI
0x230000	PE2 PMU
0x240000	PE2 ETM
0x250000-0x2BFFFF	Reserved, RES0
0x2C0000	PE2 ELA
0x2D0000-0x30FFFF	Reserved, RES0
0x310000	PE3 Debug

**Table C3-1 Address mapping for APB components on 64KB pages (continued)**

Address	Component
0x320000	PE3 CTI
0x330000	PE3 PMU
0x340000	PE3 ETM
0x350000-0x3BFFFF	Reserved, RES0
0x3C0000	PE3 ELA
0x3D0000-0x40FFFF	Reserved, RES0
0x410000	PE4 Debug
0x420000	PE4 CTI
0x430000	PE4 PMU
0x440000	PE4 ETM
0x450000-0x4BFFFF	Reserved, RES0
0x4C0000	PE4 ELA
0x4D0000-0x50FFFF	Reserved, RES0
0x510000	PE5 Debug
0x520000	PE5 CTI
0x530000	PE5 PMU
0x540000	PE5 ETM
0x550000-0x5BFFFF	Reserved, RES0
0x5C0000	PE5 ELA
0x5D0000-0x60FFFF	Reserved, RES0
0x610000	PE6 Debug
0x620000	PE6 CTI
0x630000	PE6 PMU
0x640000	PE6 ETM
0x650000-0x6BFFFF	Reserved, RES0
0x6C0000	PE6 ELA
0x6D0000-0x70FFFF	Reserved, RES0
0x710000	PE7 Debug
0x720000	PE7 CTI
0x730000	PE7 PMU
0x740000	PE7 ETM
0x750000-0x7BFFFF	Reserved, RES0
0x7C0000	PE7 ELA
0x7D0000-0x80FFFF	Reserved, RES0
0x810000	PE8 Debug

**Table C3-1 Address mapping for APB components on 64KB pages (continued)**

Address	Component
0x820000	PE8 CTI
0x830000	PE8 PMU
0x840000	PE8 ETM
0x850000-0x8BFFFF	Reserved, RES0
0x8C0000	PE8 ELA
0x8D0000-0x90FFFF	Reserved, RES0
0x910000	PE9 Debug
0x920000	PE9 CTI
0x930000	PE9 PMU
0x940000	PE9 ETM
0x950000-0x9BFFFF	Reserved, RES0
0x9C0000	PE9 ELA
0x9D0000-0xA0FFFF	Reserved, RES0
0xA10000	PE10 Debug
0xA20000	PE10 CTI
0xA30000	PE10 PMU
0xA40000	PE10 ETM
0xA50000-0xABFFFF	Reserved, RES0
0xAC0000	PE10 ELA
0xAD0000-0xB0FFFF	Reserved, RES0
0xB10000	PE11 Debug
0xB20000	PE11 CTI
0xB30000	PE11 PMU
0xB40000	PE11 ETM
0xB50000-0xBBFFFF	Reserved, RES0
0xBC0000	PE11 ELA
0xBD0000-0xC0FFFF	Reserved, RES0
0xC10000	PE12 Debug
0xC20000	PE12 CTI
0xC30000	PE12 PMU
0xC40000	PE12 ETM
0xC50000-0xCBFFFF	Reserved, RES0
0xCC0000	PE12 ELA
0xCD0000-0xD0FFFF	Reserved, RES0
0xD10000	PE13 Debug



**Table C3-1 Address mapping for APB components on 64KB pages (continued)**

Address	Component
0xD20000	PE13 CTI
0xD30000	PE13 PMU
0xD40000	PE13 ETM
0xD50000-0xDBFFFF	Reserved, RES0
0xDC0000	PE13 ELA
0xDD0000-0xE0FFFF	Reserved, RES0
0xE10000	PE14 Debug
0xE20000	PE14 CTI
0xE30000	PE14 PMU
0xE40000	PE14 ETM
0xE50000-0xEBFFFF	Reserved, RES0
0xEC0000	PE15 ELA
0xED0000-0xF0FFFF	Reserved, RES0
0xF10000	PE15 Debug
0xF20000	PE15 CTI
0xF30000	PE15 PMU
0xF40000	PE15 ETM
0xF50000-0xFBFFFF	Reserved, RES0
0xFC0000	PE15 ELA
0xFD0000-0xFFFFFFF	Reserved, RES0

The following table shows the address mapping for the DSU and the individual core debug APB components when configured for v7 Debug memory map. If an address range is not mapped to a component, it is indicated as reserved.

**Table C3-2 Address mapping for APB components on 4KB pages**

Address	Component
0x000000	ROM table
0x001000	Cluster ELA
0x002000	Cluster CTI
0x003000 - 0x3FFFF	Reserved
0x004000	PE0 Debug
0x005000	PE1 Debug
0x006000	PE2 Debug
0x007000	PE3 Debug
0x008000	PE0 ELA

**Table C3-2 Address mapping for APB components on 4KB pages (continued)**

Address	Component
0x009000	PE1 ELA
0x00A000	PE2 ELA
0x00B000	PE3 ELA
0x00C000	PE0 PMU
0x00D000	PE1 PMU
0x00E000	PE2 PMU
0x00F000	PE3 PMU
0x010000-0x013FFF	Reserved
0x014000	PE0 CTI
0x015000	PE1 CTI
0x016000	PE2 CTI
0x017000	PE3 CTI
0x018000-0x01BFFF	Reserved
0x01C000	PE0 ETM
0x01D000	PE1 ETM
0x01E000	PE2 ETM
0x01F000	PE3 ETM
0x020000-0x023FFF	Reserved
0x024000	PE4 Debug
0x025000	PE5 Debug
0x026000	PE6 Debug
0x027000	PE7 Debug
0x028000	PE4 ELA
0x029000	PE5 ELA
0x02A000	PE6 ELA
0x02B000	PE7 ELA
0x02C000	PE4 PMU
0x02D000	PE5 PMU
0x02E000	PE6 PMU
0x02F000	PE7 PMU
0x030000-0x033FFF	Reserved
0x034000	PE4 CTI
0x035000	PE5 CTI
0x036000	PE6 CTI
0x037000	PE7 CTI

**Table C3-2 Address mapping for APB components on 4KB pages (continued)**

Address	Component
0x038000-0x03BFFF	Reserved
0x03C000	PE4 ETM
0x03D000	PE5 ETM
0x03E000	PE6 ETM
0x03F000	PE7 ETM
0x040000-0x043FFF	Reserved
0x044000	PE8 Debug
0x045000	PE9 Debug
0x046000	PE10 Debug
0x047000	PE11 Debug
0x048000	PE8 ELA
0x049000	PE9 ELA
0x04A000	PE10 ELA
0x04B000	PE11 ELA
0x04C000	PE8 PMU
0x04D000	PE9 PMU
0x04E000	PE10 PMU
0x04F000	PE11 PMU
0x050000-0x053FFF	Reserved
0x054000	PE8 CTI
0x055000	PE9 CTI
0x056000	PE10 CTI
0x057000	PE11 CTI
0x058000-0x05BFFF	Reserved
0x05C000	PE8 ETM
0x05D000	PE9 ETM
0x05E000	PE10 ETM
0x05F000	PE11 ETM
0x060000-0x063FFF	Reserved
0x064000	PE12 Debug
0x065000	PE13 Debug
0x066000	PE14 Debug
0x067000	PE15 Debug
0x068000	PE12 ELA
0x069000	PE13 ELA

**Table C3-2 Address mapping for APB components on 4KB pages (continued)**

Address	Component
0x06A000	PE14 ELA
0x06B000	PE15 ELA
0x06C000	PE12 PMU
0x06D000	PE13 PMU
0x06E000	PE14 PMU
0x06F000	PE15 PMU
0x070000-0x073FFF	Reserved
0x074000	PE12 CTI
0x075000	PE13 CTI
0x076000	PE14 CTI
0x077000	PE15 CTI
0x078000-0x07BFFF	Reserved
0x07C000	PE12 ETM
0x07D000	PE13 ETM
0x07E000	PE14 ETM
0x07F000	PE15 ETM

## C3.2 CTI register summary

This section describes the CTI registers in the *DynamIQ Shared Unit* (DSU). These registers are accessed through the external debug interface.

The following table gives a summary of the CTI registers. For registers that are not described in this chapter, see the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*.

**Table C3-3 CTI register summary**

Offset	CTI	Description
0x000	CTICONTROL	CTI Control register
0x004-0x00C	-	Reserved
0x010	CTIINTACK	CTI Output Trigger Acknowledge Register
0x014	CTIAPPSET	CTI Application Trigger Set Register
0x018	CTIAPPCLEAR	CTI Application Trigger Clear Register
0x01C	CTIAPPULSE	CTI Application Pulse Register
0x020	CTIINEN0	CTI Input Trigger to Output Channel Enable Registers
0x024	CTIINEN1	
0x028	CTIINEN2	
0x02C	CTIINEN3	
0x030	CTIINEN4	
0x034	CTIINEN5	
0x038	CTIINEN6	
0x040	CTIINEN7	
0x044	CTIINEN8	
0x048	CTIINEN9	
0x04C-0x09C	-	Reserved
0x0A0	CTIOUTEN0	CTI Input Channel to Output Trigger Enable Registers
0x0A4	CTIOUTEN1	
0x0A8	CTIOUTEN2	
0x0AC	CTIOUTEN3	
0x0B0	CTIOUTEN4	
0x0B4	CTIOUTEN5	
0x0B8	CTIOUTEN6	
0x0BC	CTIOUTEN7	
0x0C0	CTIOUTEN8	
0x0C4	CTIOUTEN9	
0x0C8-0x12C	-	Reserved
0x130	CTITRIGINSTATUS	CTI Trigger In Status Register

Table C3-3 CTI register summary (continued)

Offset	CTI	Description
0x134	CTITRIGOUTSTATUS	CTI Trigger Out Status Register
0x138	CTICHINSTATUS	CTI Channel In Status Register
0x13C	CTICHOUTSTATUS	CTI Channel Out Status Register
0x140	CTIGATE	CTI Channel Gate Enable Register
0x144-0xF97	-	Reserved
0xFA0	CTICLAIMSET	CTI Claim Tag Set Register
0xFA4	CTICLAIMCLR	CTI Claim Tag Clear Register
0xFA8	CTIDEVAFF0	<a href="#">C3.9 CTIDEVAFF0, Cluster CTI Device Affinity register 0 on page C3-205<sup>h</sup></a>
		CTI Device Affinity Register 0 <sup>i</sup>
0xFAC	CTIDEVAFF1	CTI Device Affinity Register 1
0xFB0-0xFB4	-	Reserved
0xFB8	CTIAUTHSTATUS	CTI Authentication Status Register
0xFBC	CTIDEVARCH	CTI Device Architecture Register
0xFC0	CTIDEVID2	CTI Device Identification Register 2
0xFC4	CTIDEVID1	CTI Device Identification Register 1
0xFC8	CTIDEVID	<a href="#">C3.10 CTIDEVID, CTI Device Identification Register on page C3-206</a>
0xFCC	CTIDEVTYPE	CTI Device Type Register
0xFD0	CTIPIDR4	<a href="#">C3.7 CTIPIDR4, CTI Peripheral Identification Register 4 on page C3-203</a>
0xFD4-0xFDC	-	Reserved
0xFE0	CTIPIDR0	<a href="#">C3.3 CTIPIDR0, CTI Peripheral Identification Register 0 on page C3-199</a>
0xFE4	CTIPIDR1	<a href="#">C3.4 CTIPIDR1, CTI Peripheral Identification Register 1 on page C3-200</a>
0xFE8	CTIPIDR2	<a href="#">C3.5 CTIPIDR2, CTI Peripheral Identification Register 2 on page C3-201</a>
0xFEC	CTIPIDR3	<a href="#">C3.6 CTIPIDR3, CTI Peripheral Identification Register 3 on page C3-202</a>
0xFF0	CTICIDR0	CTI Component Identification Register 0
0xFF4	CTICIDR1	CTI Component Identification Register 1
0xFF8	CTICIDR2	CTI Component Identification Register 2
0xFFC	CTICIDR3	CTI Component Identification Register 3

<sup>h</sup> The CTIDEVAFF0 register for the cluster has a different format.<sup>i</sup> The CTIDEVAFF0 register for the PEs is described in *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*.

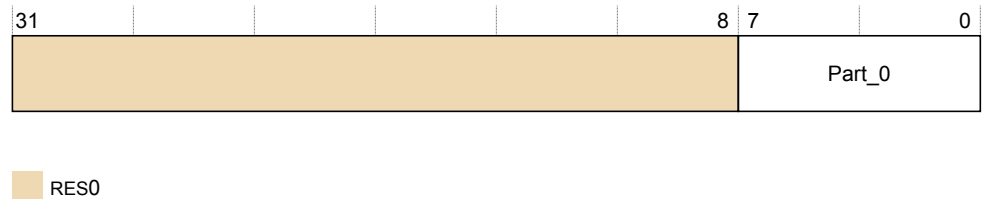
### C3.3 CTIPIDR0, CTI Peripheral Identification Register 0

The CTIPIDR0 register provides information to identify a CTI component.

## Bit field descriptions

CTIPIDR0 is a 32-bit register.

This register is Read Only.



**Figure C3-1 CTIPIDR0 bit assignments**

**RES0, [31:8]**

RES0 Reserved.

**Part\_0, [7:0]**

Least significant byte of the part number.

For the cluster, the value is:

0xE3	If v7 debug memory map is implemented.
------	--

0xE4	If v8 debug memory map is implemented.
------	--

For the PEs, the value is a copy of bits [11:4] of the Main ID Register (MIDR) of the corresponding PE.

## Configurations

The CTIPIDR0 is in the Debug power domain and is optional to implement in the external register interface.

## Usage Constraints

## Accessing the CTIPIDR0

The CTIPIDR0 can be accessed through the external debug interface with offset 0xFE0.

## Accessibility

The accessibility of the CTIPIDR0 by condition code is:

<b>Default</b>
RO

See *C3.11 External register access permissions* on page C3-208 for the condition codes.

### C3.4 CTIPIDR1, CTI Peripheral Identification Register 1

The CTIPIDR1 register provides information to identify a CTI component.

**Bit field descriptions**

CTIPIDR1 is a 32-bit register.

This register is Read Only.

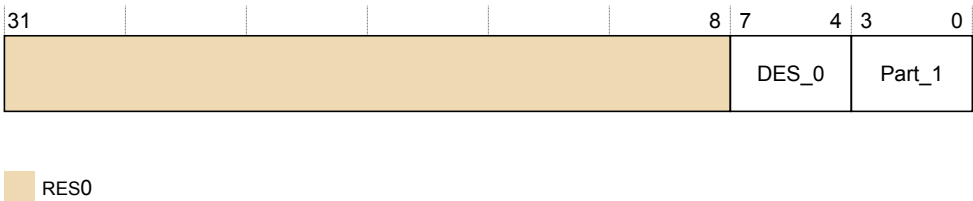


Figure C3-2 CTIPIDR1 bit assignments

**RES0, [31:8]**

RES0                      Reserved.

**DES\_0, [7:4]**

This is the least significant nibble of JEP106 ID code.

0xB                      ARM Limited.

**Part\_1, [3:0]**

Most significant nibble of the part number:

- For the cluster, the value is 0x4.
- For the PEs, the value is a copy of bits [15:12] of the MIDR of the corresponding PE.

**Configurations**

The CTIPIDR1 is in the Debug power domain and is optional to implement in the external register interface.

**Usage Constraints**

**Accessing the CTIPIDR1**

The CTIPIDR1 can be accessed through the external debug interface with offset 0xFE4.

**Accessibility**

The accessibility of the CTIPIDR1 by condition code is:

Default
RO

See [C3.11 External register access permissions](#) on page C3-208 for the condition codes.



### C3.5 CTIPIDR2, CTI Peripheral Identification Register 2

The CTIPIDR2 register provides information to identify a CTI component.

#### Bit field descriptions

CTIPIDR2 is a 32-bit register.

This register is Read Only.

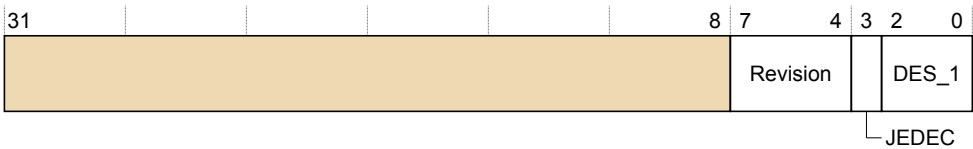


Figure C3-3 CTIPIDR2 bit assignments

#### RES0, [31:8]

RES0 Reserved.

#### Revision, [7:4]

0b0010 r0p2.

#### JEDEC, [3]

1 RES1. Indicates a JEP106 identity code is used.

#### DES\_1, [2:0]

0b011 ARM Limited. This is the most significant nibble of JEP106 ID code.

#### Configurations

The CTIPIDR2 is in the Debug power domain and is optional to implement in the external register interface.

#### Usage Constraints

##### Accessing the CTIPIDR2

The CTIPIDR2 can be accessed through the external debug interface with offset 0xFE8.

##### Accessibility

The accessibility of the CTIPIDR2 by condition code is:

Default
RO

See [C3.11 External register access permissions on page C3-208](#) for the condition codes.

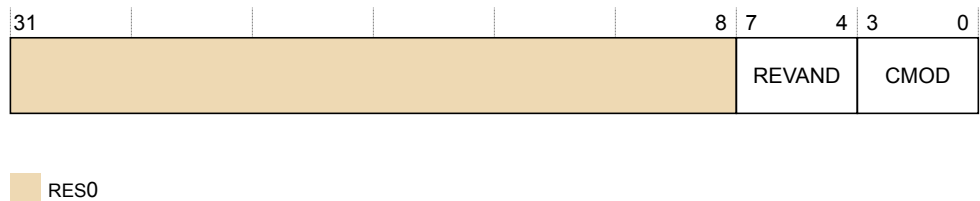
### C3.6 CTIPIDR3, CTI Peripheral Identification Register 3

The CTIPIDR3 register provides information to identify a CTI component.

## Bit field descriptions

CTIPIDR3 is a 32-bit register.

This register is Read Only.



**Figure C3-4 CTIPIDR3 bit assignments**

**RES0, [31:8]**

RES0 Reserved.

**REVAND, [7:4]**

0x0 Part minor revision.

**CMOD, [3:0]**

0x0	Customer modified.
-----	--------------------

## Configurations

The CTIPIDR3 is in the Debug power domain and is optional to implement in the external register interface.

## Usage Constraints

## Accessing the CTIPIDR3

The CTIPIDR3 can be accessed through the external debug interface with offset 0xFEC.

## Accessibility

The accessibility of the CTIPIDR3 by condition code is:

<b>Default</b>
RO

See *C3.11 External register access permissions* on page C3-208 for the condition codes.

C3.7 CTIPIDR4, CTI Peripheral Identification Register 4

The CTIPIDR4 register provides information to identify a CTI component.

Bit field descriptions

CTIPIDR4 is a 32-bit register.

This register is Read Only.

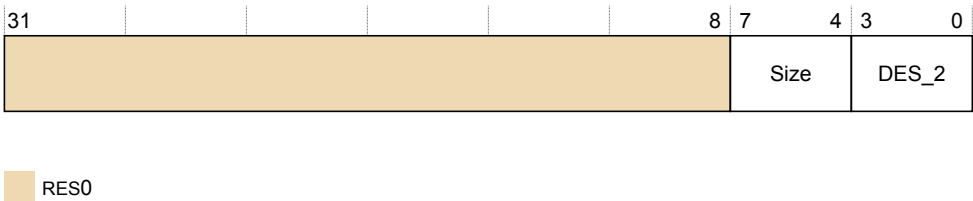


Figure C3-5 CTIPIDR4 bit assignments

RES0, [31:8]

RES0 Reserved.

Size, [7:4]

0x0 Size of the component. Log<sub>2</sub> of the number of 4KB pages from the start of the component to the end of the component ID registers.

DES\_2, [3:0]

0x4 ARM Limited. This is the least significant nibble of the JEP106 continuation code.

Configurations

The CTIPIDR4 is in the Debug power domain and is optional to implement in the external register interface.

Usage Constraints

Accessing the CTIPIDR4

The CTIPIDR4 can be accessed through the external debug interface with offset 0xFD0.

Accessibility

The accessibility of the CTIPIDR4 by condition code is:

Default
RO

See [C3.11 External register access permissions](#) on page C3-208 for the condition codes.

C3.8 CTIITCTRL, CTI Integration Mode Control Register

The CTIITCTRL register shows that the DSU does not implement an integration mode.

Bit field descriptions

CTIPIDR4 is a 32-bit register.

This register is Read Only.

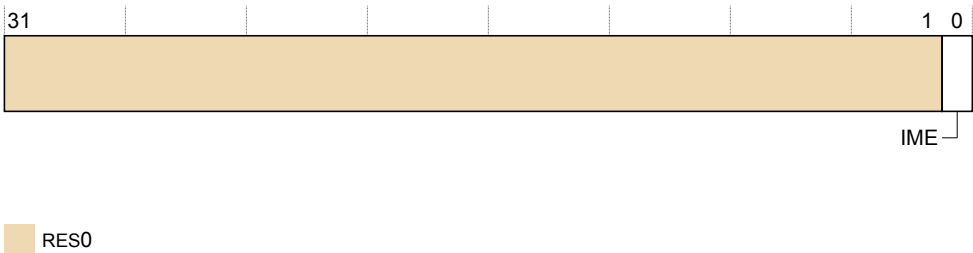


Figure C3-6 CTIITCTRL bit assignments

RES0, [31:1]

RES0 Reserved.

IME, [0]

Integration mode enable. The value is:

0 Normal operation.

Configurations

The CTIITCTRL register is in the Debug power domain.

Usage Constraints

Accessing the CTIITCTRL

The CTIITCTRL register can be accessed through external debug interface with offset 0xF00.

Accessibility

The accessibility of the CTIITCTRL register by condition code is:

Default
RO

See [C3.11 External register access permissions on page C3-208](#) for the condition codes.

## C3.9 CTIDEVAFF0, Cluster CTI Device Affinity register 0

The CTIDEVAFF0 register identifies that the CTI relates to the DSU cluster.

### Bit field descriptions

CTIDEVAFF0 is a 32-bit register.

This register is Read Only.

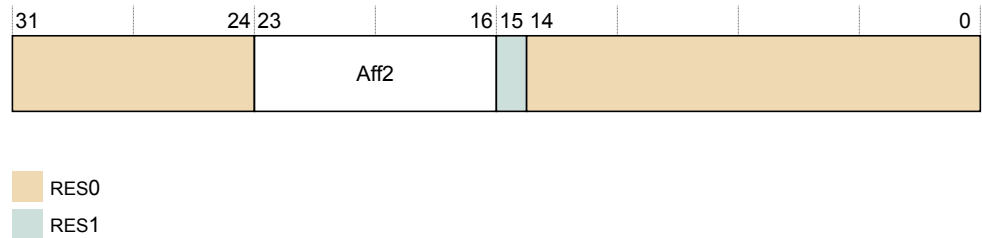


Figure C3-7 CTIDEVAFF0 bit assignments

### RES0, [31:24]

RES0 Reserved.

### Aff2, [23:16]

ClusterID Affinity Level-2 field.

The value is set by the **CLUSTERIDAFF2[7:0]** configuration input bus.

### RES1, [15]

RES1 Reserved.

### RES0, [14:0]

RES0 Reserved.

### Configurations

The CTIDEVAFF0 is in the Debug power domain and is optional to implement in the external register interface.

### Usage Constraints

#### Accessing the CTIDEVAFF0

The CTIDEVAFF0 can be accessed through the external debug interface with offset 0xFA8.

#### Accessibility

The accessibility of the CTIDEVAFF0 by condition code is:

Default
RO

See [C3.11 External register access permissions](#) on page C3-208 for the condition codes.

## C3.10 CTIDEVID, CTI Device Identification Register

The CTIDEVID register describes the CTI component to the debugger.

### Bit field descriptions

CTIDEVID is a 32-bit register.

This register is Read Only.

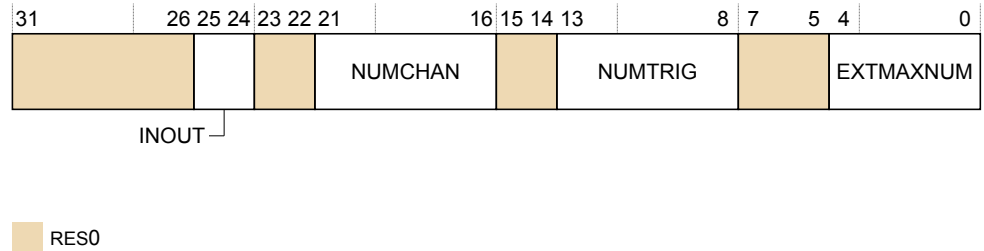


Figure C3-8 CTIDEVID bit assignments

### RES0, [31:26]

RES0 Reserved.

### INOUT, [25:24]

Input and output options. Indicates the presence of an input gate. This value is:

0b01 CTIGATE masks propagation of input events from external channels.

### RES0, [23:22]

RES0 Reserved.

### NUMCHAN, [21:16]

Number of channels implemented. This value is:

0b000100 Four channels implemented.

### RES0, [15:14]

RES0 Reserved.

### NUMTRIG, [13:8]

Number of triggers implemented. This value is:

0b001010 Ten triggers implemented.

### RES0, [7:5]

RES0 Reserved.

### EXTMAXNUM, [4:0]

Maximum number of external triggers implemented. This value is:

0b00000 No external triggers implemented.

### Configurations

The CTIDEVID register is in the Debug power domain.

### Usage Constraints

#### Accessing the CTIDEVID

The CTIDEVID register can be accessed through the external debug interface with offset 0xFC8.

### Accessibility

The accessibility of the CTIDEVID register by condition code is:

Default
RO

See [C3.11 External register access permissions](#) on page C3-208 for the condition codes.

## C3.11 External register access permissions

External access permission to the CTI registers is subject to the conditions at the time of the access. The following table describes the response of the core to accesses through the external debug and memory-mapped interfaces.

**Table C3-4 External register conditions**

Name	Condition	Description
Off	EDPRSR.PU is 0	Core power domain is completely off, or in a low-power state where the core power domain registers cannot be accessed.
DLK	EDPRSR.DLK is 1	OS Double Lock is locked.
OSLK	OSLSR_EL1.OSLK is 1	OS Lock is locked.
EDAD	AllowExternalDebugAccess()==FALSE	External debug access is disabled. When an error is returned because of an EDAD condition code, and this is the highest priority error condition, EDPRSR.SDAD is set to 1. Otherwise EDPRSR.SDAD is unchanged.
Default	-	None of the conditions apply, normal access.

The following table shows an example of external register condition codes for access to a CTI register. To determine the access permission for the register, scan the columns from left to right. Stop at the first column a condition is true, the entry gives the access permission of the register and scanning stops.

**Table C3-5 External register condition code example**

Off	DLK	OSLK	EDAD	Default
-	-	-	-	RO



# Chapter C4

## ROM Table

This chapter describes the CoreSight ROM Table component.

It contains the following sections:

- *C4.1 About the ROM table* on page C4-210.
- *C4.2 ROM table register summary* on page C4-211.

## C4.1 About the ROM table

The ROM table holds the locations of debug components.

The ROM table complies with the *ARM® CoreSight™ Architecture Specification v3.0*. This table contains a list of components such as PE debug units, *Cross Trigger Interfaces* (CTIs), *PE Performance Monitoring Units* (PMUs), and *Embedded Trace Macrocells* (ETMs). Debuggers can use the ROM table to determine which components are implemented.


If a component is not included in your implementation, the corresponding ROM table entry indicates that the component is not present.

## C4.2 ROM table register summary

The ROM table contents are determined by the specific implementation of your macrocell.

The following table shows the offsets from the physical base address of the ROM table. The register formats are described in the *ARM® CoreSight™ Architecture Specification v3.0*.

**Table C4-1 ROM table registers**

Offset	Name	Reset value	Description
0x000-0x144	ROMENTRY0-81		ROM entries
0x148-0x9FC	-	0x00000000	Reserved
0xA00	DBGPCR0	<ul style="list-style-type: none"> <li>0x00000000 if Cluster ELA is not implemented.</li> <li>0x00000001 if Cluster ELA is implemented.</li> </ul>	Debug Power Control Registers
0xA04	DBGPCR1	<ul style="list-style-type: none"> <li>0x00000000 if Core0 ELA is not implemented.</li> <li>0x00000001 if Core0 ELA is implemented.</li> </ul>	
0xA08	DBGPCR2	<ul style="list-style-type: none"> <li>0x00000000 if Core1 ELA is not implemented.</li> <li>0x00000001 if Core1 ELA is implemented.</li> </ul>	
0xA0C	DBGPCR3	<ul style="list-style-type: none"> <li>0x00000000 if Core2 ELA is not implemented.</li> <li>0x00000001 if Core2 ELA is implemented.</li> </ul>	
0xA10	DBGPCR4	<ul style="list-style-type: none"> <li>0x00000000 if Core3 ELA is not implemented.</li> <li>0x00000001 if Core3 ELA is implemented.</li> </ul>	
0xA14	DBGPCR5	<ul style="list-style-type: none"> <li>0x00000000 if Core4 ELA is not implemented.</li> <li>0x00000001 if Core4 ELA is implemented.</li> </ul>	
0xA18	DBGPCR6	<ul style="list-style-type: none"> <li>0x00000000 if Core5 ELA is not implemented.</li> <li>0x00000001 if Core5 ELA is implemented.</li> </ul>	
0xA1C	DBGPCR7	<ul style="list-style-type: none"> <li>0x00000000 if Core6 ELA is not implemented.</li> <li>0x00000001 if Core6 ELA is implemented.</li> </ul>	
0xA20	DBGPCR8	<ul style="list-style-type: none"> <li>0x00000000 if Core7 ELA is not implemented.</li> <li>0x00000001 if Core7 ELA is implemented.</li> </ul>	
0xA24-0xA7C	-	0x00000000	Reserved
0xA80	DBGPSR0	0x00000000	Debug Power Status Registers
0xA84	DBGPSR1	0x00000000	
0xA88	DBGPSR2	0x00000000	
0xA8C	DBGPSR3	0x00000000	
0xA90	DBGPSR4	0x00000000	
0xA94	DBGPSR5	0x00000000	
0xA98	DBGPSR6	0x00000000	
0xA9C	DBGPSR7	0x00000000	
0xAA0	DBGPSR8	0x00000000	
0xAA4-0xBFC	-	0x00000000	Reserved
0xC00	PRIDR0	0x00000001	Power Reset Identification Register 0

**Table C4-1 ROM table registers (continued)**

Offset	Name	Reset value	Description
0xC04-0xFB8	-	0x00000000	Reserved
0xFBC	DEVARCH	0x47700AF7	Device Architecture Register
0xFC0-0xFC4	-	0x00000000	Reserved
0xFC8	DEVID	0x00000020	Device ID Register
0xFCC	DEVTYPE	0x00000000	Device Type Register
0xFD0	PIDR4	0x00000004	Peripheral Identification Register 4
0xFD4-0xFDC	-	0x00000000	Reserved
0xFE0	PIDR0	0x000000E3 <sup>k</sup>	Peripheral Identification Register 0
		0x000000E4 <sup>l</sup>	
0xFE4	PIDR1	0x000000B4	Peripheral Identification Register 1
0xFE8	PIDR2	0x0000002B	Peripheral Identification Register 2
0xFEC	PIDR3	0x00000000	Peripheral Identification Register 3
0xFF0	CIDR0	0x0000000D	Component Identification Register 0
0xFF4	CIDR1	0x00000090	Component Identification Register 1
0xFF8	CIDR2	0x00000005	Component Identification Register 2
0xFFC	CIDR3	0x000000B1	Component Identification Register 3

<sup>j</sup> The ROMENTRY entry values depend on the number and type of cores implemented.  
<sup>k</sup> If v7 debug memory map is implemented.  
<sup>l</sup> If v8 debug memory map is implemented.

## Part D

### **Appendices**



# Appendix A

## Compatible Core Versions

This appendix lists the permissible combinations of cores.

It contains the following section:

- [\*A.1 Compatible core versions on page Appx-A-216.\*](#)

## A.1 Compatible core versions

The number and type of cores that can be combined with the DSU are described in this section.

The following table indicates the combination of core versions that are compatible for the purposes of creating a Coherent Cluster under the terms of the ARM license agreement.

**Table A-1 Compatible core versions**

Products	Core type
MP090 (DSU)	-
MP058 (Cortex-A75)	big
MP070 (Cortex-A55)	LITTLE

---

**Note**

---

Version compatibility between specific product releases are stated in the relevant product release notes and are verified by the DSU configuration script.

---

### Combinations of cores

The following table shows combinations of compatible cores that can be combined with a single instance of the DSU for the purposes of creating a Coherent Cluster under the terms of the ARM license agreement. Only one type of big core and one type of LITTLE core can be combined in a single cluster.

**Table A-2 Combinations of cores**

Number of big cores	Number of LITTLE cores
-	1
-	2
-	4
-	6
-	8
1	-
1	2
1	3
1	4
1	7
2	-
2	2
2	4
2	6
4	-
4	4



# Appendix B

## Signal Descriptions

This appendix describes the DSU signals.

It contains the following sections:

- *B.1 Signal naming convention* on page Appx-B-218.
- *B.2 DSU signals* on page Appx-B-219.
- *B.3 DebugBlock signals* on page Appx-B-237.

## B.1 Signal naming convention

Signals and buses are named using the following convention:

- Some signals or buses are per-core or per-thread. For single-threaded cores, there is a one-to-one mapping between cores and threads.
- Signals specified with a width of [CN:0] (<signal>[CN:0]) have one bit per core, where CN is the number of cores minus 1 (for example, CN=3 for a quad-core system).
- Signals named <signal>x have an instance of the signal per core, where x takes values from 0 to the number of cores minus 1.
- Signals specified with a width of [PE:0] (<signal>[PE:0]) have one bit per thread, where PE is the total number of threads minus one (for example PE=5 for a cluster with two single-threaded cores and two dual-threaded cores).
- Signals named <signal>y have an instance of the signal per thread, where y takes values from 0 to the total number of threads minus 1.

---

### Note

The DSU supports cores that might have different PA widths. The PA width determines how much physical memory the core can access and is a fixed value for each type of core. The DSU supports cores with PA widths of 40 bits, 44 bits, or 48 bits.

There are signals with variable widths that depend on the PA size. In this case, the width is given as [p:0]. If there are different cores in the cluster with different PA widths, then the PA width of the cluster matches the largest PA width of the configured cores. The options are:

- For 40-bit PA, p=39.
- For 44-bit PA, p=43.
- For 48-bit PA, p=47.

The cluster configuration script outputs the maximum core PA width when the --verbose option is used.

---

### Note

In some cases, there are signals with variable widths that depend on configuration. In this case, the width is given as [d:0]. The value of d depends on the configuration. The options are:

- For a 128-bit interface with cache protection, d is 214.
  - For a 256-bit interface with cache protection, d is 360.
  - For a 128-bit interface without cache protection, d is 212.
  - For a 256-bit interface without cache protection, d is 356.
-

## B.2 DSU signals

This section shows the *DynamIQ Shared Unit* (DSU) signals.

This section contains the following subsections:

- [B.2.1 Clock and clock enable signals](#) on page Appx-B-219.
- [B.2.2 Reset signals](#) on page Appx-B-220.
- [B.2.3 Configuration signals](#) on page Appx-B-220.
- [B.2.4 GIC signals](#) on page Appx-B-221.
- [B.2.5 Generic Timer signals](#) on page Appx-B-222.
- [B.2.6 Power management signals](#) on page Appx-B-222.
- [B.2.7 Error signals](#) on page Appx-B-223.
- [B.2.8 ACP interface signals](#) on page Appx-B-224.
- [B.2.9 Peripheral port interface signals](#) on page Appx-B-225.
- [B.2.10 Broadcast signals for the memory interface](#) on page Appx-B-227.
- [B.2.11 ACE interface signals](#) on page Appx-B-228.
- [B.2.12 CHI interface signals](#) on page Appx-B-231.
- [B.2.13 DebugBlock APB interface signals](#) on page Appx-B-233.
- [B.2.14 ATB interface signals](#) on page Appx-B-234.
- [B.2.15 Timestamp signal](#) on page Appx-B-235.
- [B.2.16 PMU interface signals](#) on page Appx-B-235.
- [B.2.17 ELA signal](#) on page Appx-B-235.
- [B.2.18 DFT interface signals](#) on page Appx-B-236.
- [B.2.19 MBIST interface signals](#) on page Appx-B-236.

### B.2.1 Clock and clock enable signals

This section describes the clock and clock enable signals.

**Table B-1 Clock signals**

Signal	Direction	Description
CORECLK[CN:0]	Input	Clock for each core.  ————— <b>Note</b> ————— If a core is synchronous to the cluster, then the corresponding bit of this signal is not present and the core uses <b>SCLK</b> instead. If all cores are synchronous to the cluster, then this signal is not present. —————
SCLK	Input	Clock for the SCU/L3 and the AMBA interface.
PCLK	Input	Clock for the debug APB interface.
ATCLK	Input	Clock for the ATB trace interface.
GICCLK	Input	Clock for the GIC interface.
PERIPHCLK	Input	Clock for the timers, power management, and other miscellaneous logic.

**Table B-2 Clock enable signals**

Signal	Direction	Description
ACLKENM	Input	ACE Master bus clock enable. This pin is only present when the DSU is configured with the ACE interface.
ACLKENMP	Input	AXI Master peripheral port clock enable. This pin is only present when the DSU is configured with the peripheral port interface.
ACLKENS	Input	AXI Slave bus clock enable. This pin is only present when the DSU is configured with the ACP interface.

**Table B-2 Clock enable signals (continued)**

Signal	Direction	Description
CNTCLKEN	Input	Counter clock enable.
SCLKENM	Input	CHI Master bus clock enable. This pin is only present when the DSU is configured with the CHI interface.
TSCCLKEN	Input	Timestamp clock enable.

## B.2.2 Reset signals

This section describes the reset signals.

**Table B-3 Reset signals**

Signal	Direction	Description
nATRESET	Input	Active-LOW reset for all registers in the <b>ATCLK</b> domain.
nCORERESSET[CN:0]	Input	Active-LOW core Warm reset, excluding Debug, RAS, and ETM.
nCPUPORESET[CN:0]	Input	Active-LOW core power-on reset.
nGICRESET	Input	Active-LOW reset for all registers in the <b>GICCLK</b> domain.
nMBISTRESET	Input	Active-LOW reset for all MBIST logic.
nPERIPHRESET	Input	Active-LOW reset for all registers in the <b>PERIPHCLK</b> domain.
nPRESET	Input	Active-LOW reset for all registers in the <b>PCLK</b> domain.
nSPORESET	Input	Active-LOW power-on reset for all registers in the <b>SCLK</b> domain.
nSRESET	Input	Active-LOW Warm reset for all registers in the <b>SCLK</b> domain, excluding RAS registers.

## B.2.3 Configuration signals

This section describes the configuration signals.

**Table B-4 Configuration signals**

Signal	Direction	Description
AA64nAA32[PE:0]	Input	<p>Register width state. The options are:</p> <p><b>0</b>            AArch32</p> <p><b>1</b>            AArch64</p> <p>————— <b>Note</b> —————</p> <p>This signal is only present for cores which support AArch32 execution at EL3. For example, if there are two single-threaded cores, and only core 1 supports executing AArch32 at EL3, then only bit[1] of this signal is present. If none of the cores support AArch32 execution at EL3, this signal is not present.</p> <p>—————</p>
CFGEND[PE:0]	Input	<p>Endianness configuration, controls the reset value of the SCTL_R_EL3/SCTLR EE bit. The options are:</p> <p><b>0</b>            EE bit is LOW.</p> <p><b>1</b>            EE bit is HIGH.</p>

**Table B-4 Configuration signals (continued)**

Signal	Direction	Description
CFGTE[PE:0]	Input	<p>Enable Thumb exceptions, controls the reset value of the SCTLR.TE bit. The options are:</p> <p><b>0</b> TE is LOW.</p> <p><b>1</b> TE is HIGH.</p> <p>————— <b>Note</b> —————</p> <p>This signal is only present for cores which support AArch32 execution at EL3. For example, if there are two single-threaded cores, and only core 1 supports executing AArch32 at EL3, then only bit[1] of this signal is present. If none of the cores support AArch32 execution at EL3, this signal is not present.</p> <p>—————</p>
CLUSTERIDAFF2[7:0]	Input	Value read in ClusterID Affinity Level-2 field, MPIDR bits[23:16].
CLUSTERIDAFF3[7:0]	Input	Value read in ClusterID Affinity Level-3 field, MPIDR bits[39:32].
CRYPTODISABLE	Input	<p>Disables the Cryptographic Extensions.</p> <p>————— <b>Note</b> —————</p> <p>If Cryptographic Extensions are not enabled, this signal is not present.</p> <p>—————</p>
GICCDISABLE	Input	Globally disables the CPU interface logic and routes the external interrupt signals directly to the cores.
RVBARADDRy[p:2]	Input	Reset Vector Base Address for executing in 64-bit state.
VINITHI[PE:0]	Input	<p>Enable high exception vectors, controls the reset value of the SCTLR.V bit. The options are:</p> <p><b>0</b> Starts exceptions vectors at address 0x00000000.</p> <p><b>1</b> Starts exceptions vectors at address 0xFFFF0000.</p> <p>————— <b>Note</b> —————</p> <p>This signal is only present for cores which support AArch32 execution at EL3. For example, if there are two single-threaded cores, and only core 1 supports executing AArch32 at EL3, then only bit[1] of this signal is present. If none of the cores support AArch32 execution at EL3, this signal is not present.</p> <p>—————</p>

## B.2.4 GIC signals

This section describes the GIC and AXI4 Stream Protocol signals.

The following table shows the GIC signals.

**Table B-5 GIC signals**

Signal	Direction	Description
nFIQ[PE:0]	Input	Active-LOW, level-sensitive fast interrupt request.
nIRQ[PE:0]	Input	Active-LOW, level-sensitive interrupt request.
nVFIQ[PE:0]	Input	Active-LOW, level-sensitive virtual fast interrupt request.
nVIRQ[PE:0]	Input	Active-LOW, level-sensitive virtual interrupt request.
nVCPUMNTIRQ[PE:0]	Output	Virtual CPU interface maintenance interrupt PPI output.

The following table shows the AXI4 Stream Protocol signals.

**Table B-6 AXI4 Stream Protocol signals**

Signal	Direction	Description
<b>IRITVALID</b>	Input	Distributor to GIC CPU Interface messages. <b>TVALID</b> indicates that the master is driving a valid transfer.
<b>IRITREADY</b>	Output	Distributor to GIC CPU Interface messages. <b>TREADY</b> indicates that the slave can accept a transfer in the current cycle.
<b>IRITDATA[15:0]</b>	Input	Distributor to GIC CPU Interface messages. <b>TDATA</b> is the primary payload that is used to provide the data that is passing across the interface.
<b>IRITLAST</b>	Input	Distributor to GIC CPU Interface messages. <b>TLAST</b> indicates the boundary of a packet.
<b>IRITDEST[3:0]</b>	Input	Distributor to GIC CPU Interface messages. <b>TDEST</b> provides routing information for the data stream. Depending on the cluster configuration, not all bits of this bus are used. Any unused upper bits should be tied LOW.
<b>IRITWAKEUP</b>	Input	AXI4 stream protocol activity indicator.
<b>ICCTVALID</b>	Output	GIC CPU Interface to distributor messages. <b>TVALID</b> indicates that the master is driving a valid transfer.
<b>ICCTREADY</b>	Input	GIC CPU Interface to distributor messages. <b>TREADY</b> indicates that the slave can accept a transfer in the current cycle.
<b>ICCTDATA[15:0]</b>	Output	GIC CPU Interface to distributor messages. <b>TDATA</b> is the primary payload that is used to provide the data that is passing across the interface
<b>ICCTLAST</b>	Output	GIC CPU Interface to distributor messages. <b>TLAST</b> indicates the boundary of a packet.
<b>ICCTID[3:0]</b>	Output	GIC CPU Interface to distributor. <b>TID</b> is the data stream identifier that indicates different streams of data.
<b>ICCTWAKEUP</b>	Output	AXI4 Stream Protocol activity indicator.

## B.2.5 Generic Timer signals

This section describes the Generic Timer signals.

**Table B-7 Generic Timer signals**

Signal	Direction	Description
<b>nCNTHPIRQ[PE:0]</b>	Output	Hypervisor Physical Timer event.
<b>nCNTSNSIRQ[PE:0]</b>	Output	Non-secure Physical Timer event.
<b>nCNTPSIRQ[PE:0]</b>	Output	Secure Physical Timer event.
<b>nCNTVIRQ[PE:0]</b>	Output	Virtual Timer event.
<b>nCNTHVIRQ[PE:0]</b>	Output	Hypervisor Virtual Timer event.
<b>CNTVALUEB[63:0]</b>	Input	Counter value in binary encoding.

## B.2.6 Power management signals

This section describes the power management signals.

**Table B-8 Power management signals**

Signal	Direction	Description
<b>ATCLKQACCEPTn</b>	Output	Active-LOW signal that indicates that the cluster accepts the clock controller request.
<b>ATCLKQACTIVE</b>	Output	Indicates that the cluster requires <b>ATCLK</b> to be active.
<b>ATCLKQDENY</b>	Output	Active-LOW signal that indicates that the cluster denies the clock controller request.
<b>ATCLKQREQn</b>	Input	Active-LOW signal that indicates that the clock controller wants to gate the clock.
<b>CLUSTERPACCEPT</b>	Output	Indicates that the cluster accepts the power controller request.
<b>CLUSTERPACTIVE[19:0]</b>	Output	Indicates if the cluster is active in various power states.
<b>CLUSTERPDENY</b>	Output	Indicates that the cluster denies the power controller request.
<b>CLUSTERPREQ</b>	Input	Indicates that the power controller wants the cluster to move to a new power state.
<b>CLUSTERPSTATE[6:0]</b>	Input	Power state that the power controller requires the cluster to move to.
<b>COREPACCEPTx</b>	Output	Indicates that the referenced core accepts the power controller request.
<b>COREPACTIVEx[17:0]</b>	Output	Indicates if the referenced core is active in various power states.
<b>COREPDENYx</b>	Output	Indicates that the referenced core denies the power controller request.
<b>COREPREQx</b>	Input	Indicates that the power controller wants the referenced core to move to a new power state.
<b>COREPSTATEx[5:0]</b>	Input	Power state that the power controller requires the core to move to.
<b>EVENTIACK</b>	Output	Event input request acknowledge. It is not asserted until <b>EVENTIREQ</b> is high, and then remains asserted until after <b>EVENTIREQ</b> goes low.
<b>EVENTIREQ</b>	Input	Event input request for wake-up from WFE state. It must remain asserted until <b>EVENTIACK</b> is asserted, and must not be re-asserted until <b>EVENTIACK</b> is low.
<b>EVENTOACK</b>	Input	Event output request acknowledge. It must not be asserted until <b>EVENTOREQ</b> is high, and then must remain asserted until after <b>EVENTOREQ</b> goes low.
<b>EVENTOREQ</b>	Output	Event output request for wake-up, triggered by SEV instruction. It is only asserted when <b>EVENTOACK</b> is low, and then remains high until after <b>EVENTOACK</b> goes high.
<b>GICCLKQACCEPTn</b>	Output	Active-LOW signal that indicates that the cluster accepts the clock controller request.
<b>GICCLKQACTIVE</b>	Output	Indicates that the cluster requires <b>GICCLK</b> to be active.
<b>GICCLKQDENY</b>	Output	Indicates that the cluster denies the clock controller request.
<b>GICCLKQREQn</b>	Input	Active-LOW signal that indicates that the clock controller wants the gate the clock.
<b>PCLKQACCEPTn</b>	Output	Active-LOW signal that indicates that the cluster accepts the clock controller request.
<b>PCLKQACTIVE</b>	Output	Indicates that the cluster requires <b>PCLK</b> to be active.
<b>PCLKQDENY</b>	Output	Indicates that the cluster denies the clock controller request.
<b>PCLKQREQn</b>	Input	Active-LOW signals that indicate that the clock controller wants the gate the clock.
<b>SCLKQACCEPTn</b>	Output	Active-LOW signal that indicates that the cluster accepts the clock controller request.
<b>SCLKQACTIVE</b>	Output	Indicates that the cluster requires <b>SCLK</b> to be active.
<b>SCLKQDENY</b>	Output	Indicates that the cluster denies the clock controller request.
<b>SCLKQREQn</b>	Input	Active-LOW signal that indicates that the clock controller wants the gate the clock.

## B.2.7 Error signals

This section describes the error signals.

**Table B-9 Timing constraints for the error signals**

Signal	Direction	Description
<b>nFAULTIRQ</b> [CN+1:1]	Output	Fault indicator for a detected 1-bit or 2-bit ECC or Parity error in the RAMs. Bits [CN+1:1] are for the L1 and L2 RAMs in each core. The bits are output from the <b>PERIPHCLK</b> domain.
<b>nFAULTIRQ</b> [0]	Output	Fault indicator for a detected 1-bit or 2-bit ECC or Parity error in the RAMs. Bit [0] is for L3 or snoop filter RAMs. It is output from the <b>SCLK</b> domain.
<b>nERRIRQ</b> [CN+1:1]	Output	Error indicator for an ECC error that causes potential data corruption or loss of coherency. Bits [CN+1:1] are for the L1 and L2 RAMs in each core. The bits are output from the <b>PERIPHCLK</b> domain.
<b>nERRIRQ</b> [0]	Output	Error indicator for an ECC error that causes potential data corruption or loss of coherency. Bit [0] is for L3 or snoop filter RAMs or ACE/CHI write transactions with a write response condition. It is output from the <b>SCLK</b> domain.

### B.2.8 ACP interface signals

This interface exists only if the DSU is configured to have the ACP interface.

**Table B-10 ACP wakeup signal**

Signal	Direction	Description
<b>AWAKEUPS</b>	Input	AXI Slave activity indicator.

**Table B-11 ACP write address channel signals**

Signal	Direction	Description
<b>AWREADYS</b>	Output	Write address ready.
<b>AWVALIDS</b>	Input	Write address valid.
<b>AWIDS</b> [7:0]	Input	Write address ID.
<b>AWADDRS</b> [p:0]	Input	Write address.
<b>AWLENS</b> [7:0]	Input	Write burst length.
<b>AWCACHES</b> [3:0]	Input	Write cache type.
<b>AWDOMAINS</b> [1:0]	Input	Write attributes.
<b>AWSNOOPS</b> [3:0]	Input	Write request type.
<b>AWPROTS</b> [2:0]	Input	Write protection type.
<b>AWSTASHLPIDS</b> [3:0]	Input	Write stash target core.
<b>AWSTASHLPIDENS</b>	Input	Write stash target enable.

**Table B-12 ACP write data channel signals**

Signal	Direction	Description
<b>WREADYS</b>	Output	Write data ready.
<b>WVALIDS</b>	Input	Write data valid.
<b>WDATAS</b> [127:0]	Input	Write data.



**Table B-12 ACP write data channel signals (continued)**

Signal	Direction	Description
<b>WSTRBS[15:0]</b>	Input	Write byte-lane strobes.
<b>WLASTS</b>	Input	Write data last transfer indication.

**Table B-13 ACP write response channel signals**

Signal	Direction	Description
<b>BREADYS</b>	Input	Write response ready.
<b>BVALIDS</b>	Output	Write response valid.
<b>BIDS[7:0]</b>	Output	Write response ID.
<b>BRESPS[1:0]</b>	Output	Write response.

**Table B-14 ACP read address channel signals**

Signal	Direction	Description
<b>ARREADYS</b>	Output	Read address ready.
<b>ARVALIDS</b>	Input	Read address valid.
<b>ARIDS[7:0]</b>	Input	Read address ID.
<b>ARADDRS[p:0]</b>	Input	Read address.
<b>ARLENS[7:0]</b>	Input	Read burst length.
<b>ARCAHES[3:0]</b>	Input	Read cache type.
<b>ARDOMAINS[1:0]</b>	Input	Read attributes.
<b>ARPROTS[2:0]</b>	Input	Read protection type.

**Table B-15 ACP read data channel signals**

Signal	Direction	Description
<b>RREADYS</b>	Input	Read data ready.
<b>RVALIDS</b>	Output	Read data valid.
<b>RIDS[7:0]</b>	Output	Read data ID.
<b>RDATAS[127:0]</b>	Output	Read data.
<b>RRESPS[1:0]</b>	Output	Read data response.
<b>RLASTS</b>	Output	Read data last transfer indication.

## B.2.9 Peripheral port interface signals

This interface exists only if the DSU is configured to have a peripheral port interface.

**Table B-16 Peripheral port wakeup signals**

Signal	Direction	Description
<b>AWAKEUPMP</b>	Output	AXI activity indicator.

**Table B-17 Peripheral port configuration signals**

Signal	Direction	Description
<b>ASTARTMP[p:20]</b>	Input	Start address for peripheral port address range.
<b>AENDMP[p:20]</b>	Input	End address for peripheral port address range.

**Table B-18 Peripheral port write address channel signals**

Signal	Direction	Description
<b>AWREADYMP</b>	Input	Write address ready.
<b>AWVALIDMP</b>	Output	Write address valid.
<b>AWIDMP[3:0]</b>	Output	Write address ID.
<b>AWADDRMP[p:0]</b>	Output	Write address.
<b>AWCACHEMP[3:0]</b>	Output	Write cache type.
<b>AWDOMAINMP[1:0]</b>	Output	Write protection type.
<b>AWPROTMP[2:0]</b>	Output	Write size.
<b>AWSIZEMP[2:0]</b>	Output	Write attributes.

**Table B-19 Peripheral port write data channel signals**

Signal	Direction	Description
<b>WREADYMP</b>	Input	Write data ready.
<b>WVALIDMP</b>	Output	Write data valid.
<b>WDATAMP[63:0]</b>	Output	Write data.
<b>WSTRBMP[7:0]</b>	Output	Write byte-lane strobes.
<b>WLASTMP</b>	Output	Write data last transfer indication.

**Table B-20 Peripheral port write response channel signals**

Signal	Direction	Description
<b>BREADYMP</b>	Output	Write response ready.
<b>BVALIDMP</b>	Input	Write response valid.
<b>BIDMP[3:0]</b>	Input	Write response ID.
<b>BRESPMP[1:0]</b>	Input	Write response.

**Table B-21 Peripheral port read address channel signals**

Signal	Direction	Description
<b>ARREADYMP</b>	Input	Read address ready.
<b>ARVALIDMP</b>	Output	Read address valid.
<b>ARIDMP[3:0]</b>	Output	Read address ID.
<b>ARADDRMP[p:0]</b>	Output	Read address.
<b>ARCACHEMP[3:0]</b>	Output	Read cache type.

**Table B-21 Peripheral port read address channel signals (continued)**

Signal	Direction	Description
ARPROTMP[2:0]	Output	Read protection type.
ARSIZEEMP[2:0]	Output	Read size.
ARDOMAINMP[1:0]	Output	Read attributes.

**Table B-22 Peripheral port read data channel signals**

Signal	Direction	Description
RREADYMP	Output	Read data ready.
RVALIDMP	Input	Read data valid.
RIDMP[3:0]	Input	Read data ID.
RDATAMP[63:0]	Input	Read data.
RRESPMP[1:0]	Input	Read data response.

### B.2.10 Broadcast signals for the memory interface

The signals in the following table are common to the memory interface, irrespective of whether the ACE or CHI protocol is used.

**Table B-23 Broadcast signals**

Signal	Direction	Description
BROADCASTCACHEMAINT	Input	Enable broadcasting of cache maintenance operations to downstream caches. The options are: <b>0</b> Cache maintenance operations are not broadcast to downstream caches. <b>1</b> Cache maintenance operations are broadcast to downstream caches.
BROADCASTCACHEMAINTPOU	Input	Enable broadcasting of cache maintenance operations to the point of unification. The options are: <b>0</b> Cache maintenance operations DCCMVAU and DC CVAU are not broadcast to other clusters. This is more efficient if all other clusters are ARM Cortex processors. <b>1</b> Cache maintenance operations DCCMVAU and DC CVAU are broadcast to other clusters.

**Table B-23 Broadcast signals (continued)**

Signal	Direction	Description
<b>BROADCASTPERSIST</b>	Input	Enable broadcasting of cache clean to the point of persistence operations. The options are:  <b>0</b> DC CVAP instructions are treated the same as DC CVAC. <b>1</b> DC CVAP instructions are sent as a clean to the point of persistence transaction externally.
<b>BROADCASTOUTER</b>	Input	Enable broadcasting of Outer Shareable transactions. The options are:  <b>0</b> Outer Shareable transactions are not broadcast externally. <b>1</b> Outer Shareable transactions are broadcast externally.  <p style="text-align: center;">————— <b>Note</b> —————</p> <p>Within the cluster, Inner Shareable and Outer Shareable memory are treated identically. Therefore, this signal also controls the broadcast of Inner Shareable transactions.</p>

### B.2.11 ACE interface signals

This interface exists only if the DSU is configured to have the ACE master interface.

The following tables show the signals present when one ACE interface is implemented. The signals have a suffix of M0. If a second ACE interface is implemented, an additional set of ACE signals is present suffixed by M1.

**Table B-24 ACE write address channel signals**

Signal	Direction	Description
<b>AWADDRM0[q:0]<sup>m</sup></b>	Output	Write address.
<b>AWBURSTM0[1:0]</b>	Output	Write burst type.
<b>AWCACHM0[3:0]</b>	Output	Write cache type.
<b>AWDOMAINM0[1:0]</b>	Output	Write shareability domain type.
<b>AWIDM0[7:0]</b>	Output	Write address ID.
<b>AWLENM0[7:0]</b>	Output	Write burst length.
<b>AWLOCKM0</b>	Output	Write lock type.
<b>AWPROTM0[2:0]</b>	Output	Write protection type.
<b>AWREADYM0</b>	Input	Write address ready.
<b>AWSIZEM0[2:0]</b>	Output	Write burst size.
<b>AWSNOOPM0[2:0]</b>	Output	Write snoop request type.
<b>AWUNIQUEM0</b>	Output	For WriteBack, WriteClean and WriteBackUC transactions. Indicates that the write is Unique (0b1) or shared (0b0).
<b>AWVALIDM0</b>	Output	Write address valid.

<sup>m</sup> The value of q is 43 when p is 39. For any other value of p, q is the same as p.

**Table B-25 ACE write data channel signals**

Signal	Direction	Description
<b>WDATAM0[127:0]</b>	Output	Write data.
<b>WIDM0[7:0]</b>	Output	Write data ID. Only used when connecting to an AXI3 interconnect.
<b>WLASTM0</b>	Output	Write data last transfer indication.
<b>WREADYM0</b>	Input	Write data ready.
<b>WSTRBM0[15:0]</b>	Output	Write byte-lane strobes.
<b>WVALIDM0</b>	Output	Write data valid.

**Table B-26 ACE write data response channel signals**

Signal	Direction	Description
<b>BIDM0[7:0]</b>	Input	Write response ID.
<b>BREADYM0</b>	Output	Write response valid.
<b>BRESPM0[1:0]</b>	Input	Write response.
<b>BVALIDM0</b>	Input	Write response valid.

**Table B-27 ACE read address channel signals**

Signal	Direction	Description
<b>ARADDRM0[q:0]<sup>m</sup></b>	Output	Read address.
<b>ARBURSTM0[1:0]</b>	Output	Read burst type.
<b>ARCACHEM0[3:0]</b>	Output	Read cache type.
<b>ARDOMAINM0[1:0]</b>	Output	Read shareability domain type.
<b>ARIDM0[8:0]</b>	Output	Read address ID.
<b>ARLENM0[7:0]</b>	Output	Read burst length.
<b>ARLOCKM0</b>	Output	Read lock type.
<b>ARPROTM0[2:0]</b>	Output	Read protection type.
<b>ARREADYM0</b>	Input	Read address ready.
<b>ARSIZEM0[2:0]</b>	Output	Read burst size.
<b>ARSNOOPM0[3:0]</b>	Output	Read snoop request type.
<b>ARVALIDM0</b>	Output	Read address valid.
<b>ARVMIDEXTM0[3:0]</b>	Output	Additional VMID bits for DVM messages.

**Table B-28 ACE read data channel signals**

Signal	Direction	Description
<b>RDATAM0[127:0]</b>	Input	Read data.
<b>RIDM0[8:0]</b>	Input	Read data ID.
<b>RLASTM0</b>	Input	Read data last transfer indication.

**Table B-28 ACE read data channel signals (continued)**

Signal	Direction	Description
<b>RREADYM0</b>	Output	Read data ready.
<b>RRESPM0[3:0]</b>	Input	Read data response.
<b>RVALIDM0</b>	Input	Read data valid.

**Table B-29 ACE coherency address channel signals**

Signal	Direction	Description
<b>ACADDRM0[q:0]<sup>m</sup></b>	Input	Snoop address.
<b>ACPROTM0[2:0]</b>	Input	Snoop protection type.
<b>ACREADYM0</b>	Output	Master ready to accept snoop address.
<b>ACVMIDEXTM0[3:0]</b>	Input	Additional VMID bits for DVM messages.
<b>ACSNOOPM0[3:0]</b>	Input	Snoop request type.
<b>ACVALIDM0</b>	Input	Snoop address valid.

**Table B-30 ACE coherency response channel signals**

Signal	Direction	Description
<b>CRREADYM0</b>	Input	Slave ready to accept snoop response.
<b>CRVALIDM0</b>	Output	Snoop response valid.
<b>CRRESPM0[4:0]</b>	Output	Snoop response.

**Table B-31 ACE coherency data channel handshake signals**

Signal	Direction	Description
<b>CDDATAM0[127:0]</b>	Output	Snoop data.
<b>CDLASTM0</b>	Output	Snoop data last transfer.
<b>CDREADYM0</b>	Input	Slave ready to accept snoop data.
<b>CDVALIDM0</b>	Output	Snoop data valid.

**Table B-32 ACE read and write acknowledge signals**

Signal	Direction	Description
<b>RACKM0</b>	Output	Read acknowledge.
<b>WACKM0</b>	Output	Write acknowledge.

**Table B-33 ACE low-power wakeup signals**

Signal	Direction	Description
<b>AWAKEUPM0</b>	Output	ACE pending activity indicator.
<b>ACWAKEUPM0</b>	Input	ACE snoop activity indicator.

**Table B-34 ACE coherency signals**

Signal	Direction	Description
<b>SYSCOREQM0</b>	Output	The cluster requests to be part of the coherency domain and can safely receive snoops.
<b>SYSCOACKM0</b>	Input	The system might send snoops to the cluster.

## B.2.12 CHI interface signals

This interface exists only if the DSU is configured to have the CHI master interface.

**Table B-35 CHI configuration signals**

Signal	Direction	Description
<b>BROADCASTATOMIC<sup>n</sup></b>	Input	Enable broadcasting of atomic transactions. The options are: <b>0</b> Atomic transactions are not sent externally. <b>1</b> Atomic transactions are sent externally.
<b>NODEID[10:0]</b>	Input	DSU cluster CHI Node Identifier.

**Table B-36 CHI activity signals**

Signal	Direction	Description
<b>RXSACTIVE</b>	Input	Receive pending activity indicator.
<b>TXSACTIVE</b>	Output	Transmit pending activity indicator.
<b>RXLINKACTIVEREQ</b>	Input	Receive link active request.
<b>RXLINKACTIVEACK</b>	Output	Receive link active acknowledge.
<b>TXLINKACTIVEREQ</b>	Output	Transmit link active request.
<b>TXLINKACTIVEACK</b>	Input	Transmit link active acknowledge.

**Table B-37 CHI transmit request virtual channel signals**

Signal	Direction	Description
<b>TXREQFLITPEND</b>	Output	Transmit Request Flit pending.
<b>TXREQFLITV</b>	Output	Transmit Request Flit valid.
<b>TXREQFLIT[85+p:0]</b>	Output	Transmit Request Flit payload.
<b>TXREQLCRDV</b>	Input	Transmit Request link-layer credit valid.

**Table B-38 CHI transmit response virtual channel signals**

Signal	Direction	Description
<b>TXRSPFLITPEND</b>	Output	Transmit response flit pending.
<b>TXRSPFLITV</b>	Output	Transmit response flit valid.
<b>TXRSPFLIT[58:0]</b>	Output	Transmit response flit.
<b>TXRSPLCRDV</b>	Input	Transmit response link-layer credit valid.

<sup>n</sup> This signal is sampled on reset like the other broadcast signals listed in [B.2.10 Broadcast signals for the memory interface](#) on page Appx-B-227

**Table B-39 CHI transmit data virtual channel signals**

Signal	Direction	Description
<b>TXDATFLITPEND</b>	Output	Transmit Data Flit pending.
<b>TXDATFLITV</b>	Output	Transmit Data Flit valid.
<b>TXDATFLIT[d:0]</b>	Output	Transmit Data Flit.
<b>TXDATLCRDV</b>	Input	Transmit Data link-layer credit valid.

**Table B-40 CHI receive response virtual channel signals**

Signal	Direction	Description
<b>RXRSPFLITPEND</b>	Input	Receive Response Flit pending.
<b>RXRSPFLITV</b>	Input	Receive Response Flit valid.
<b>RXRSPFLIT[58:0]</b>	Input	Receive Response Flit.
<b>RXRSPLCRDV</b>	Output	Receive Response link-layer credit valid.

**Table B-41 CHI receive snoop virtual channel signals**

Signal	Direction	Description
<b>RXSNPFLITPEND</b>	Input	Receive Snoop Flit pending.
<b>RXSNPFLITV</b>	Input	Receive Snoop Flit valid.
<b>RXSNPFLIT[48+p:0]</b>	Input	Receive Snoop Flit.
<b>RXSNPLCRDV</b>	Output	Receive Snoop link-layer credit valid.

**Table B-42 CHI receive data virtual channel signals**

Signal	Direction	Description
<b>RXDATFLITPEND</b>	Input	Receive Data Flit pending.
<b>RXDATFLITV</b>	Input	Receive Data Flit valid.
<b>RXDATFLIT[d:0]</b>	Input	Receive Data Flit.
<b>RXDATLCRDV</b>	Output	Receive Data link-layer credit valid.

**Table B-43 CHI coherency signals**

Signal	Direction	Description
<b>SYSCOREQ</b>	Output	The cluster requests to be part of the coherency domain and can safely receive snoops.
<b>SYSCOACK</b>	Input	The system might send snoops to the cluster.

### System address map signals

This interface exists only if the DSU is configured to have the CHI interface and the CMN-600 SAM option is enabled.



**Table B-44 CHI system address map signals**

Signal	Direction	Description
RXPUBCFGACTIVE	Input	SAM configuration pending activity indicator.
RXPUBFLITPEND	Input	Receive Data Flit pending.
RXPUBFLITV	Input	Receive Data Flit valid.
RXPUBFLIT[34:0]	Input	Receive Data Flit.
RXPUBLICRDV_RP1	Output	Receive Data link-layer credit valid.
RXPUBLINKACTIVEREQ	Input	Receive link active request.
RXPUBLINKACTIVEACK	Output	Receive link active acknowledge.
RXPUBLINKFLIT	Input	Receive link-layer flit.
TXPUBFLITPEND	Output	Transmit Data Flit pending.
TXPUBFLITV	Output	Transmit Data Flit valid.
TXPUBFLIT[34:0]	Output	Transmit Data Flit.
TXPUBLCRDV_RP1	Input	Transmit Data link-layer credit valid.
TXPUBLINKACTIVEREQ	Output	Transmit link active request.
TXPUBLINKACTIVEACK	Input	Transmit link active acknowledge.
TXPUBLINKFLIT	Output	Transmit link-layer flit.

**Table B-45 CHI system address map configuration signals**

Signal	Direction	Description
RNSAM_CFGM_DESTID[15:0]	Input	CMN-600 CFG master destination ID.
RNSAM_CFGS_NODEID[15:0]	Input	Source ID for the cluster CFG slave.
RNSAM_DEFAULT_TGTID[10:0]	Input	Default target ID of the boot node.
RNSAM_DN_TGTID[10:0]	Input	Target ID for the DN that handles DVMs.
RNSAM_PGMED_RDY	Input	Reset value of the Programmed Ready bit.

### B.2.13 DebugBlock APB interface signals

The interface between the DebugBlock and the cluster consists of a pair of APB interfaces, one in each direction. The signals on the cluster interface should be connected to the equivalently named signal on the DebugBlock.

The following table shows the signals between the cluster APB master and the DebugBlock APB slave.

**Table B-46 Cluster to DebugBlock APB interface signals**

Signal	Direction	Description
PSELCD	Output	APB bus access.
PADDRCD[8:2]	Output	APB address.
PENABLECD	Output	Cluster to DebugBlock APB transfer complete flag.
PWDATACD[7:0]	Output	APB write data.
PREADYCD	Input	APB slave ready, used to extend a transfer.

**Table B-46 Cluster to DebugBlock APB interface signals (continued)**

Signal	Direction	Description
<b>PSLVERRCD</b>	Input	APB slave transfer error.
<b>PWAKEUPCD</b>	Output	APB activity indicator.

The following table shows the signals between the DebugBlock APB master and the cluster APB slave.

**Table B-47 DebugBlock to cluster APB interface signals**

Signal	Direction	Description
<b>PSELDC</b>	Input	DebugBlock to cluster bus access.
<b>PADDRDC[19:2]</b>	Input	APB address.
<b>PENABLEDC</b>	Input	APB transfer complete flag.
<b>PWRITEDC</b>	Input	APB read/write indicator.
<b>PWDATADC[31:0]</b>	Input	APB write data.
<b>PRDATADC[31:0]</b>	Output	APB read data.
<b>PREADYDC</b>	Output	APB slave ready, used to extend a transfer.
<b>PSLVERRDC</b>	Output	APB slave transfer error.
<b>PWAKEUPDC</b>	Input	APB activity indicator.

The following table shows the miscellaneous debug signals.

**Table B-48 Miscellaneous debug signals**

Signal	Direction	Description
<b>DBGRSTREQ[PE:0]</b>	Output	Debug reset request.
<b>nCOMMIRQ[PE:0]</b>	Output	Active-LOW comms channel receive or transmit interrupt request.
<b>DBGGEN</b>	Input	Invasive debug enable.
<b>NIDEN</b>	Input	Non-invasive debug enable.
<b>SPIDEN</b>	Input	Secure privilege invasive debug enable.
<b>SPNIDEN</b>	Input	Secure privilege non-invasive debug enable.
<b>DBGCONNECTED</b>	Input	A debugger is connected and so the DebugBlock can be accessed on boot.

## B.2.14 ATB interface signals

The following table shows the ATB interface signals.

**Table B-49 ATB interface signals**

Signal	Direction	Description
<b>ATREADYMx</b>	Input	ATB device ready.
<b>AFVALIDMx</b>	Input	FIFO flush request.
<b>ATDATAMx[31:0]</b>	Output	Data.
<b>ATVALIDMx</b>	Output	Data valid.

**Table B-49 ATB interface signals (continued)**

Signal	Direction	Description
ATBYTESMx[1:0]	Output	Data size.
AFREADYMx	Output	FIFO flush finished
ATIDMx[6:0]	Output	Trace source ID.
ATWAKEUPMx	Output	ATB activity indicator.
SYNCREQMx	Input	Synchronization request.

### B.2.15 Timestamp signal

This section describes the timestamp signal.

**Table B-50 Timestamp signal**

Signal	Direction	Description
TSVALUEB[63:0]	Input	Timestamp in binary encoding.

### B.2.16 PMU interface signals

This section describes the PMU interface signals.

**Table B-51 PMU interface signals**

Signal	Direction	Description
COREINSTRRET[PE:0]	Output	Indicates that a core has retired at least one instruction recently. This signal is output from the <b>PERIPHCLK</b> domain.
COREINSTRRUN[PE:0]	Output	Indicates that a core is in a running state (powered up and not in WFI or WFE low-power states). This signal is output from the <b>PERIPHCLK</b> domain.
nCLUSTERPMUIRQ	Output	Cluster PMU interrupt request. This signal is output from the <b>SCLK</b> domain.
nPMBIRQ[PE:0]	Output	SPE interrupt request. This signal only exists for cores that support the architectural <i>Statistical Profiling Extension</i> (SPE). This signal is output from the <b>PERIPHCLK</b> domain.
nPMUIRQ[PE:0]	Output	PMU interrupt request.
PMUSNAPSHOTACK	Output	Acknowledge a snapshot request. This signal forms a four phase handshake with <b>PMUSNAPSHOTREQ</b> .
PMUSNAPSHOTREQ	Input	Request for a snapshot of the PMU counters. Once asserted, this signal must remain high until <b>PMUSNAPSHOTACK</b> is asserted. It must not be reasserted until <b>PMUSNAPSHOTACK</b> is deasserted.

### B.2.17 ELA signal

This signal is present only if ELA-500 support is configured.

**Table B-52 ELA signal**

Signal	Direction	Description
STOPCLOCK	Output	ELA request for the system to stop the clocks. This signal is generated from multiple clock domains and must be synchronized in the system before use.

## B.2.18 DFT interface signals

This section describes the DFT signals.

**Table B-53 DFT interface signals**

Signal	Direction	Description
<b>DFTRAMHOLD</b>	Input	Disables the RAM chip select during scan shift.
<b>DFTRSTDISABLE[1:0]</b>	Input	Disables internal synchronized reset during scan shift.
<b>DFTCGEN</b>	Input	Forces on the clock gates during scan shift.
<b>DFTMCPHOLD</b>	Input	Disables Multicycle Paths on RAM interfaces.
<b>DFTCORECLKDISABLE[CN:0]</b>	Input	Disables specific <b>CORECLK</b> signals from toggling during scan, to reduce test power if only part of the design is being scanned.

## B.2.19 MBIST interface signals

This section describes the MBIST interface signals.

**Table B-54 MBIST interface signals**

Signal	Direction	Description
<b>MBISTREQ</b>	Input	MBIST test request.

## B.3 DebugBlock signals

This section shows the DebugBlock signals.

This section contains the following subsections:

- [B.3.1 Clock signal on page Appx-B-237.](#)
- [B.3.2 Reset signal on page Appx-B-237.](#)
- [B.3.3 Power and clock gate control signals on page Appx-B-237.](#)
- [B.3.4 Configuration signals on page Appx-B-238.](#)
- [B.3.5 Debug signals on page Appx-B-238.](#)
- [B.3.6 CTI interface signals on page Appx-B-239.](#)
- [B.3.7 DFT signals on page Appx-B-240.](#)

### B.3.1 Clock signal

The following table shows the clock signal.

Table B-55 Clock signal

Signal	Direction	Description
<b>PCLK</b>	Input	Clock for the DebugBlock and APB interface.

### B.3.2 Reset signal

The following table shows the reset signal.

Table B-56 Reset signal

Signal	Direction	Description
<b>nPRESET</b>	Input	Reset for all registers in the DebugBlock.

### B.3.3 Power and clock gate control signals

The following table shows the power and clock gate control signals.

Table B-57 Power and clock gate signals

Signal	Direction	Description
<b>PDBGCLKQREQn</b>	Input	Active-LOW signal that indicates that the clock controller wants to gate the clock.
<b>PWRQREQn</b>	Input	Active-LOW signal that indicates that the power controller wants to power down the DebugBlock.
<b>PDBGCLKQACTIVE</b>	Output	Indicates that the DebugBlock requires <b>PCLK</b> to be active.
<b>PDBGCLKQACCEPTn</b>	Output	Active-LOW signal that indicates that the DebugBlock accepts the clock controller request.
<b>PDBGCLKQDENY</b>	Output	Indicates that the DebugBlock denies the clock controller request.
<b>PWRQACTIVE</b>	Output	Indicates that the DebugBlock requires power.
<b>PWRQACCEPTn</b>	Output	Active-LOW signal that indicates that the DebugBlock accepts the power controller request. It causes all future APB accesses to the DebugBlock to receive a <b>PSLVERR</b> response.
<b>PWRQDENY</b>	Output	Indicates that the DebugBlock denies the power controller request because of an ongoing transaction.

### B.3.4 Configuration signals

The following table shows the configuration signals. All these configuration pins are sampled only on reset.

————— **Note** —————

The following signals must be tied to the same values as the corresponding cluster signals.

**Table B-58 Configuration signals**

Signal	Direction	Description
<b>CLUSTERIDAFF2[7:0]</b>	Input	Value read in ClusterID Affinity Level-2 field, MPIDR bits[23:16].
<b>CLUSTERIDAFF3[7:0]</b>	Input	Value read in ClusterID Affinity Level-3 field, MPIDR bits[39:32].
<b>ELADISABLE</b>	Input	Disables the ELA logic in the cluster. This signal is not present if ELA support is not implemented.  ————— <b>Note</b> ————— The ELA is intended only for silicon debug of sample devices. The ELADISABLE pin must be driven HIGH in any production devices.  —————
<b>GICCDISABLE</b>	Input	Globally disables the CPU interface logic and routes the external signals directly to the cores.

### B.3.5 Debug signals

This section describes the debug interface signals.

The following table shows the external debug APB interface signals.

**Table B-59 External debug APB interface signals**

Signal	Direction	Description
<b>PSELDBG</b>	Input	Debug bus access.
<b>PADDRDBG[23:2]</b>	Input	APB address.
<b>PADDRDBG31</b>	Input	APB address bit[31]. Controls the ETM OS Lock mechanism.  ————— <b>Note</b> ————— Software lock is not supported.  —————
<b>PENABLEDBG</b>	Input	APB transfer complete flag.
<b>PWRITEDBG</b>	Input	APB read/write indicator.
<b>PWDATADBG[31:0]</b>	Input	APB write data.
<b>PWAKEUPDBG</b>	Input	APB activity indicator.
<b>PRDATADBG[31:0]</b>	Output	APB read data.
<b>PREADYDBG</b>	Output	APB slave ready, used to extend a transfer.
<b>PSLVERRDBG</b>	Output	APB slave transfer error.

The following table shows the debug authentication signals.

**Table B-60 Debug authentication signals**

Signal	Direction	Description
<b>DBGEN</b>	Input	Invasive debug enable.
<b>NIDEN</b>	Input	Non-invasive debug enable.
<b>SPIDEN</b>	Input	Secure privilege invasive debug enable.
<b>SPNIDEN</b>	Input	Secure privilege non-invasive debug enable.
<b>DBGPWRUPREQ[PE:0]</b>	Output	Request to power up a PE for debug.
<b>CLUSTERDBGPWRUPREQ</b>	Output	Request power to the cluster domain. Supports the powerup of Cluster-level ELA from the external debugger.

The following table shows the signals between the cluster APB master and the DebugBlock APB slave.

**Table B-61 Cluster to DebugBlock APB signals**

Signal	Direction	Description
<b>PADDRCD[8:2]</b>	Input	APB address.
<b>PENABLECD</b>	Input	APB transfer complete flag.
<b>PREADYCD</b>	Output	APB slave ready, used to extend a transfer.
<b>PSELCD</b>	Input	DebugBlock to Cluster bus access.
<b>PSLVERRCD</b>	Output	APB slave transfer error.
<b>PWAKEUPCD</b>	Input	APB activity indicator.
<b>PWDATACD[7:0]</b>	Input	APB write data.

The following table shows the signals between the DebugBlock APB master and the cluster APB slave.

**Table B-62 DebugBlock to cluster APB signals**

Signal	Direction	Description
<b>PADDRDC[19:2]</b>	Output	APB address.
<b>PENABLEDC</b>	Output	APB transfer complete flag.
<b>PRDATADC[31:0]</b>	Input	APB read data.
<b>PREADYDC</b>	Input	APB slave ready, used to extend a transfer.
<b>PSELDC</b>	Output	DebugBlock to Cluster bus access.
<b>PSLVERRDC</b>	Input	APB slave transfer error.
<b>PWAKEUPDC</b>	Output	APB activity indicator.
<b>PWDATADC[31:0]</b>	Output	APB write data.
<b>PWRITEDC</b>	Output	APB read/write indicator.

### B.3.6 CTI interface signals

This section describes the CTI interface signals

**Table B-63 CTI interface signals**

Signal	Direction	Description
CTICHIN[3:0]	Input	Channel In.
CTICHOUTACK[3:0]	Input	Channel Out acknowledge.
CTICHOUT[3:0]	Output	Channel Out.
CTICHINACK[3:0]	Output	Channel In acknowledge.
CISBYPASS	Input	Channel interface sync bypass.
CIHSBYPASS[3:0]	Input	Channel interface H/S bypass.
CTIIRQ[PE:0]	Output	Active-HIGH CTI interrupt.
CTIIRQACK[PE:0]	Input	CTI interrupt acknowledge.

### B.3.7 DFT signals

The following table shows the DFT signals.

**Table B-64 DFT interface signals**

Signal	Direction	Description
DFTCGEN	Input	Forces on the clock gates during scan shift.
DFTRSTDISABLE	Input	Disables internal synchronized reset during scan shift.



# Appendix C

## Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- [C.1 Revisions on page Appx-C-242](#).

## C.1 Revisions

This section describes the technical changes between released issues of this document.

**Table C-1 Issue 0000-00**

Change	Location	Affects
First release	-	-

**Table C-2 Differences between issue 0000-00 and issue 0001-00**

Change	Location	Affects
Added support for ACE and CHI.	The whole document	r0p1

**Table C-3 Differences between issue 0001-00 and issue 0002-00**

Change	Location	Affects
Change of terminology, <i>Flexible Cluster Microarchitecture</i> (FCM) to <i>DynamIQ Shared Unit</i> (DSU)	The whole document	All revisions
Updated CLUSTERPSTATE value	<a href="#">Table A4-3 Cluster power domain CLUSTERPSTATE values on page A4-51</a>	r0p2
Added description of error protection of snoop filter tag RAMs	<a href="#">A5.4 L3 cache ECC and parity on page A5-63</a>	
Added traps and enables descriptions to AARCH64 registers	<a href="#">Chapter B1 Control registers on page B1-105</a>	
Updated register description	<a href="#">B2.3 ERRICTLR, Error Record Control Register on page B2-138</a>	
Updated revision field	<a href="#">C3.5 CTIPIDR2, CTI Peripheral Identification Register 2 on page C3-201</a>	
Updated ROM table Peripheral Identification Register 2 address	<a href="#">C4.2 ROM table register summary on page C4-211</a>	