

# ARM® CoreLink™ GIC-600 Generic Interrupt Controller

Revision: r0p2

## Technical Reference Manual



# ARM® CoreLink™ GIC-600 Generic Interrupt Controller

## Technical Reference Manual

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### Release Information

### Document History

Issue	Date	Confidentiality	Change
0000-00	29 July 2016	Confidential	First release for r0p0
0000-01	26 October 2016	Confidential	Second release for r0p0
0001-00	31 March 2017	Confidential	First release for r0p1
0002-00	07 June 2017	Confidential	First release for r0p2
0002-01	15 June 2017	Non-Confidential	Second release for r0p2

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LES-PRE-20349

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**Product Status**

The information in this document is Final, that is for a developed product.

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# Preface

This preface introduces the *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Technical Reference Manual*.

It contains the following:

- *About this book* on page 7.
- *Feedback* on page 10.

## About this book

This book is for the ARM® CoreLink™ GIC-600 Generic Interrupt Controller.

### Product revision status

The *rm**pn* identifier indicates the revision status of the product described in this book, for example, r1p2, where:

*rm* Identifies the major revision of the product, for example, r1.

*pn* Identifies the minor revision or modification status of the product, for example, p2.

### Intended audience

This book is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the GIC-600.

### Using this book

This book is organized into the following chapters:

#### **Chapter 1 Introduction**

Read this for an introduction to the GIC-600 and its features.

#### **Chapter 2 Components and configuration**

Read this for a description of the major components of the GIC-600.

#### **Chapter 3 Single-chip operation**

Read this for an operational description of the GIC-600 that is configured in a single-chip system.

#### **Chapter 4 Programmers model**

Read this for a description of the memory map and registers, and for information about programming the device.

#### **Appendix A Signal descriptions**

Read this for a description of the input and output signals.

#### **Appendix B Implementation-defined features**

Read this for a description of the IMPLEMENTATION-DEFINED features.

#### **Appendix C Revisions**

Read this for a description of changes between released issues of this book.

### Glossary

The ARM® Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the [ARM® Glossary](#) for more information.

### Typographic conventions

*italic*

Introduces special terminology, denotes cross-references, and citations.

**bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

#### **monospace**

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

#### ***monospace italic***

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

#### ****monospace bold****

Denotes language keywords when used outside example code.

#### **<and>**

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

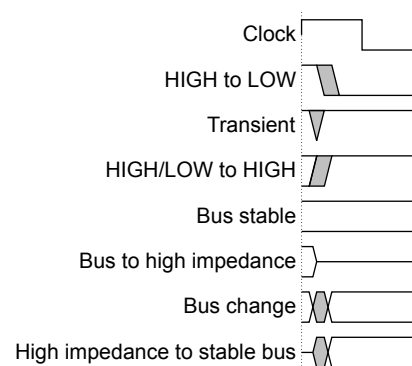
#### **SMALL CAPITALS**

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

## **Timing diagrams**

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



**Figure 1 Key to timing diagram conventions**

## **Signals**

The signal conventions are:

### **Signal level**

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

### **Lowercase n**

At the start or end of a signal name denotes an active-LOW signal.

## **Additional reading**

This section lists publications by ARM and by third parties.

See *Infocenter* <http://infocenter.arm.com>, for access to ARM documentation.



## ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *ARM® AMBA® AXI and ACE Protocol Specification* (ARM IHI 0022).
- *ARM® AMBA® 4 AXI4-Stream Protocol Specification* (ARM IHI 0051).
- *AMBA® Low Power Interface Specification, ARM® Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* (ARM IHI 0069).
- *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile* (ARM DDI 0487).
- *ARM® GICv3 and GICv4 Software Overview* (ARM DAI 0492).

The following confidential books are only available to licensees:

- *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual* (ARM 100337).
- *ARM® Reliability, Availability, and Serviceability (RAS) Architecture Extension* (ARM PRD03-PRDC-010953).
- *ARM® CoreLink™ ADB-400 AMBA® Domain Bridge User Guide* (ARM DUI 0615).

## Feedback

### Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

### Feedback on content

If you have comments on content then send an e-mail to [errata@arm.com](mailto:errata@arm.com). Give:

- The title *ARM CoreLink GIC-600 Generic Interrupt Controller Technical Reference Manual*.
- The number ARM 100336\_0002\_01\_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

————— **Note** —————

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# Chapter 1

## Introduction

Read this for an introduction to the GIC-600 and its features.

It contains the following sections:

- [1.1 About the GIC-600 on page 1-12.](#)
- [1.2 Components on page 1-13.](#)
- [1.3 Compliance on page 1-17.](#)
- [1.4 Features on page 1-18.](#)
- [1.5 Test features on page 1-19.](#)
- [1.6 Product documentation on page 1-20.](#)
- [1.7 Product revisions on page 1-21.](#)

## 1.1 About the GIC-600

The GIC-600 is a generic interrupt controller that handles interrupts from peripherals to the cores and between cores. The GIC-600 supports a distributed microarchitecture containing several individual blocks that are used to provide a flexible GIC implementation.

The GIC-600 supports the GICv3 architecture, see *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

The microarchitecture scales from a single core to coherent, unified, and consistent, multichip environments containing up to 16 chips of up to 512 cores each.

---

### Note

This manual defines a *chip* as a SoC that is integrated with the GIC-600. A single-chip system has one SoC. A multichip system can have several SoCs that are connected externally, or a SoC comprising several SoCs connected inside a single physical package. In all cases, each SoC is integrated with the GIC-600.

---

All the GIC-600 blocks communicate through fully credited AXI4-Stream interface channels. Channels can be routed over dedicated AXI4-Stream buses, or over any available free-flowing transport layer in the system. A channel is described as free-flowing if all transactions on that channel complete without a non-transient dependency on any other transaction.

The GIC-600 includes build scripts that can create appropriate levels of hierarchy for any particular configuration. In small configurations, the distribution can be hidden and internally optimized.

---

### Note

The microarchitecture for product versions r0p0, r0p1, and r0p2 is limited to a maximum of 16 cores on a single chip.

---

## 1.2 Components

The GIC-600 comprises several significant blocks that work in combination to create a single architecturally compliant GICv3 implementation within the system. The GIC-600 top level can have one of several optional structures.

The GIC-600 consists of the following blocks:

### Distributor

The Distributor is the hub of all the GIC communications and contains the functionality for all *Shared Peripheral Interrupts* (SPIs) and *Locality-specific Peripheral Interrupts* (LPIs). It is responsible for the entire GIC programmers model, except for the GITS\_TRANSLATER register, which is hosted in the *Interrupt Translation Service* (ITS) block.

---

#### Note

The LPI functionality for all cores on a chip is combined into a single cache in the Distributor.

---

See [2.1 Distributor on page 2-23](#).

### Redistributor

The Redistributor maintains the *Private Peripheral Interrupts* (PPIs) and *Software Generated Interrupts* (SGIs) for a particular core set. A Redistributor can scale from 1-128 cores and is best placed next to the processors that it is servicing to reduce wiring to the cores.

A Redistributor is also referred to as a PPI block.

The GICv3 architecture specifies a Redistributor address space containing two pages per core. The SGI page functionality is contained in the GIC-600 Redistributor. However, the command and control page for all cores is contained in the Distributor.

The GIC-600 supports powering down the Redistributors and the associated cores.

See [2.2 Redistributor on page 2-29](#).

### Interrupt Translation Service

The ITS translates message-based interrupts, *Message-Signaled Interrupts* (MSI/MSIx), from *PCI Express* (PCIe) or other sources. The ITS also manages LPIs during core power management.

The GIC-600 supports up to 16 ITS blocks per chip.

See [2.3 ITS on page 2-32](#).

For more information about the ITS, see *ARM® GICv3 and GICv4 Software Overview*.

### MSI-64 Encapsulator

The MSI-64 Encapsulator is a small block that combines the *DeviceID* (DID), required by writes to the GITS\_TRANSLATER register, into a single memory access.

See [2.4 MSI-64 Encapsulator on page 2-37](#).

### SPI Collator

The GIC-600 supports up to 960 SPIs that are spread across the system. The SPI Collator enables SPIs to be converted into messages remotely from the Distributor. This enables hierarchical clock-gating of the Distributor and the use of other more aggressive low-power states.

See [2.5 SPI Collator on page 2-40](#).

### Wake Request

The Wake Request contains all the architecturally defined **wake\_request** signals for each core on the chip. It is a separate block that can be positioned remotely from the Distributor, such as next to a system control processor if necessary.

See [2.6 Wake Request on page 2-42](#).

### GIC Interconnect

The GIC Interconnect is a set of components that can be used for routing the AXI4-Stream interfaces between the different blocks.

See [2.7 Interconnect on page 2-43](#).

### Top level

The top level has no specific interfaces but combines the interfaces of other blocks within the domain to reduce the number of domain bridges. The GIC-600 build scripts enable you to build the GIC from a single combined block or a set of individual blocks that are interconnected using your own transport layer.

See [2.8 Top-level interfaces on page 2-44](#).

These blocks can be combined in different ways:

- In systems where there is an available free-flowing transport layer in place, existing buses can be used to route the GIC traffic.
- The GIC-600 includes a narrow, 16-bit, AXI4-Stream interconnect that can be used for routing internal traffic.

The following figure shows a GIC-600 with a free-flowing interconnect in an example system.

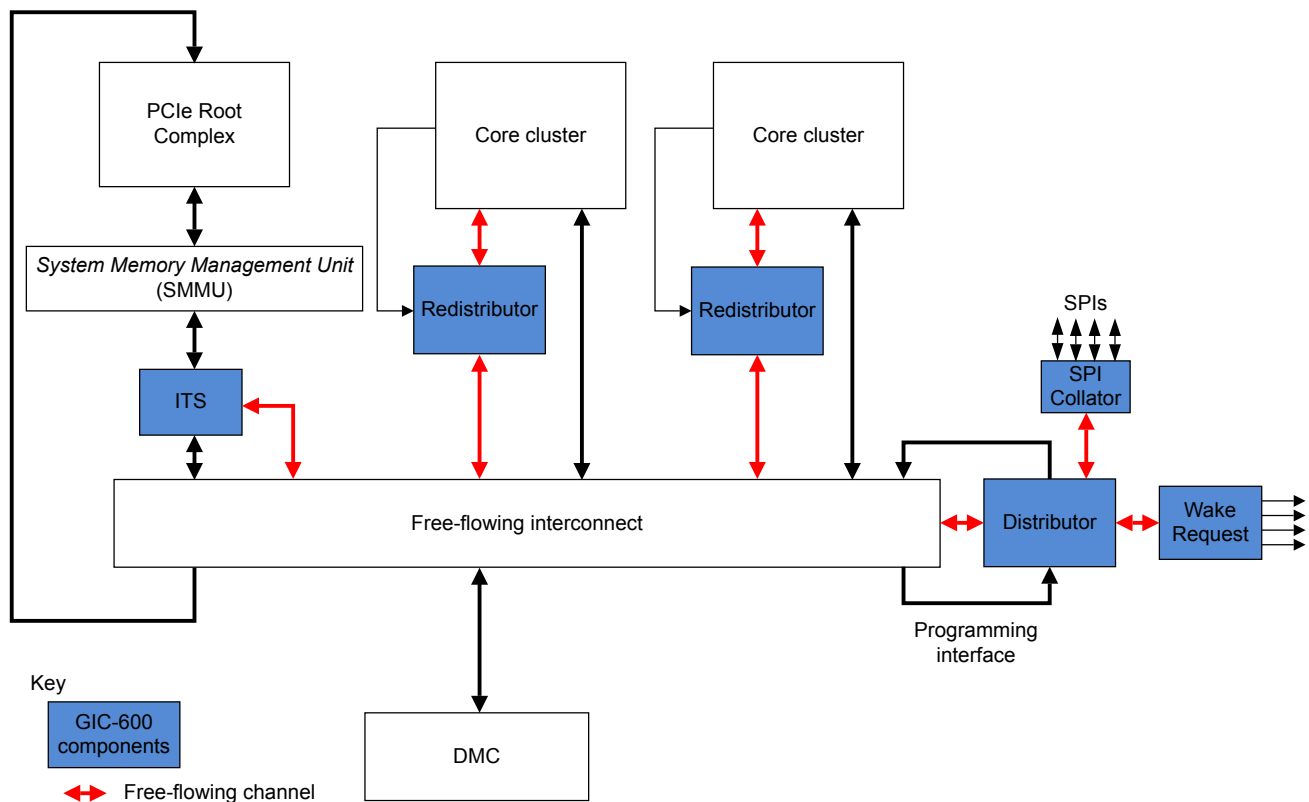
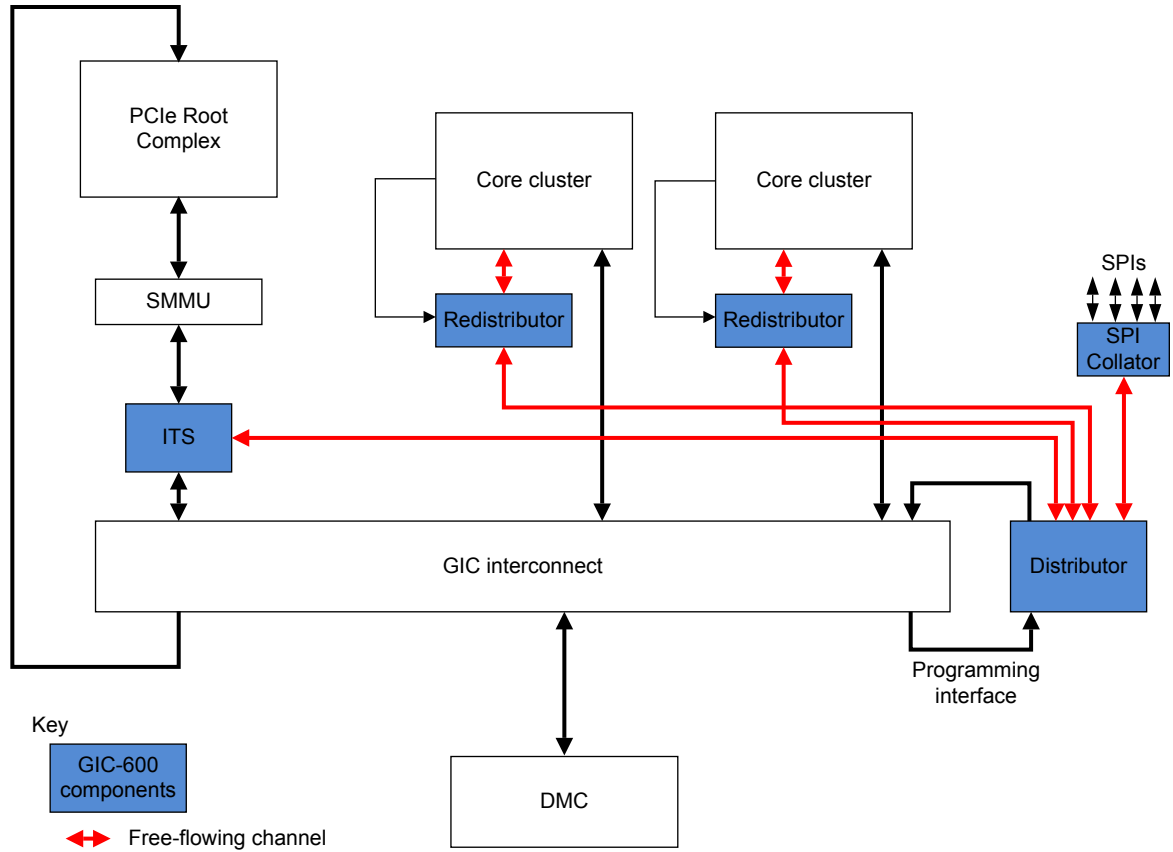


Figure 1-1 GIC-600 with free-flowing interconnect in an example system

**Note**

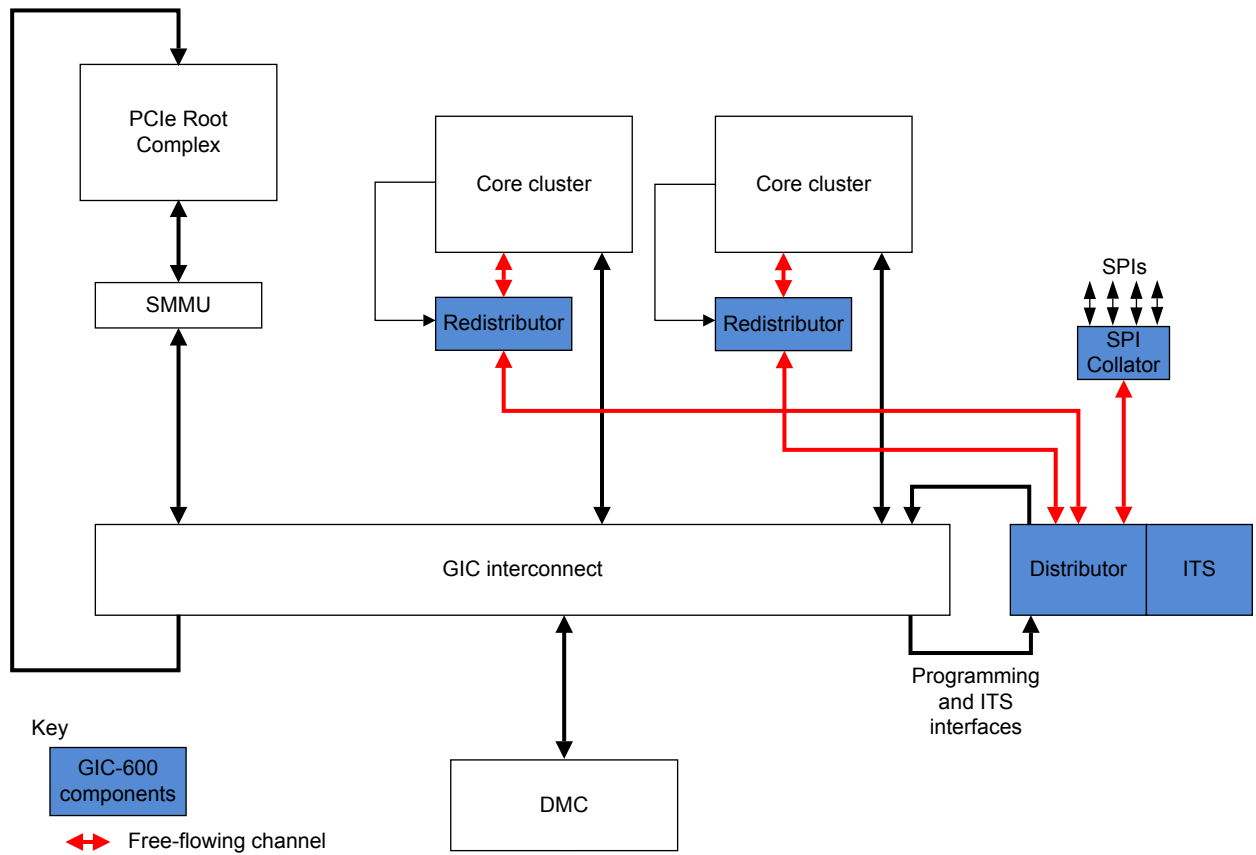
A free-flowing channel is clear to transmit a transaction that arrives at its destination without any non-transient dependencies on other transactions.

The following figure shows a GIC-600 with interconnect in an example system.



The following figure shows a monolithic GIC-600 with interconnect in an example system.

**Figure 1-2 GIC-600 with interconnect in an example system**



**Figure 1-3 Monolithic GIC-600 with interconnect in an example system**

**Note**

If the GIC supports LPIs, there must be free-flowing access to main memory. This requirement is irrespective of the interconnect that is used for routing the AXI4-Stream interfaces. For more information, see *Chapter 3, Key integration points* of the *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual*.

The GIC-600 supports cores that implement only the ARMv8 architecture, and later versions, and the GIC CPU interface with the standard GIC AXI4-Stream protocol interface. The GIC-600 implements version 3.0 of the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*, to enable support for:

- ARMv8 cores and later versions.
- Physical interrupt signals.
- SGIs.
- Interrupts that are generated by writing to the ACE-Lite slave port, and are known as message-based interrupts.
- Multiple distributed ITS that provides ID translation and core migration for message-based interrupts.



## 1.3 Compliance

The GIC-600 interfaces are compliant with ARM specifications and protocols.

The GIC-600 is compliant with:

- The AMBA AXI4-Stream protocol. See *ARM® AMBA® AXI and ACE Protocol Specification*.
- Version 3.0 of the ARM GIC architecture specification. See *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

The GIC Stream protocol is based on the following specifications:

- The AMBA AXI4-Stream protocol. See *ARM® AMBA® 4 AXI4-Stream Protocol Specification*.
- The GIC Stream Protocol Interface. See *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### Related information

*ARM® AMBA® AXI and ACE Protocol Specification.*

*ARM® Generic Interrupt Controller Architecture Specification, version 3.0 and version 4.0.*

## 1.4 Features

The GIC-600 provides interrupt services and masking, registers and programming, interrupt Exception level grouping, security, performance monitoring, and error correction.

Interrupt services and masking:

- Support for the following interrupt types:
  - Up to 56000 LPis. A peripheral generates these interrupts by writing to a memory-mapped register in the GIC-600. See [2.1.6 Distributor configuration on page 2-27](#).
  - Up to 960 SPIs in groups of 32. See [2.1.6 Distributor configuration on page 2-27](#).
  - Up to 16 PPIs that are independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts. See [2.2.6 Redistributor configuration on page 2-31](#).
  - Up to 16 SGIs that are generated either by using software to write to the GICD\_SGIR register, which controls the generation of SGIs, or through the GIC CPU interface of a core.
- Up to 16 ITS modules that provide device isolation and ID translation for message-based interrupts and enable virtual machines to program devices directly.
- Interrupt masking and prioritization with 32 priority levels, five bits per interrupt.

Registers and programming:

- Flexible affinity routing, using the *Multiprocessor Identification Register* (MPIDR) addresses, including support for all four affinity levels.
- Single ACE-Lite slave port on each chip for programming of all *GIC Distributor* (GICD) registers, *GIC Interrupt Translation Service* (GITS) registers, and *GIC Redistributor* (GICR) registers. Each ITS has an optional ACE-Lite slave port for programming the GITS\_TRANSLATER register.

---

### Note

For more information about Exception levels, see the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*.

---

Security:

- A global *Disable Security* (DS) bit. This bit enables support for systems with and without security.
- The following interrupt groups allow interrupts to target different Exception levels:
  - Group 0.
  - Non-secure Group 1.
  - Secure Group 1.

See [3.2.7 Security on page 3-56](#) for more information about security and groupings.

Performance monitoring. *Performance Monitoring Unit* (PMU) counters with snapshot functionality.

Error correction:

- ARMv8.2 *Reliability Accessibility Serviceability* (RAS) architecture-compliant error reporting for:
  - Software access errors.
  - ITS command errors.
  - ECC errors.

## 1.5 Test features

The GIC-600 provides *Design for Test* (DFT) signals for test mode.

### Related references

[A.1 Common control signals](#) on page Appx-A-153.

## 1.6 Product documentation

Documentation that is provided with this product includes a *Technical Reference Manual* (TRM) and a *Configuration and Integration Manual* (CIM), together with architecture and protocol information.

For relevant protocol and architectural information that relates to this product, see [Additional reading on page 8](#).

The GIC-600 documentation is as follows:

### Technical Reference Manual

The TRM describes the functionality and the effects of functional options on the behavior of the GIC-600. It is required at all stages of the design flow. The choices that are made in the design flow can mean that some behaviors that the TRM describes are not relevant. If you are programming the GIC-600, contact:

- The implementer to determine:
  - The build configuration of the implementation.
  - What integration, if any, was performed before implementing the GIC-600.
- The integrator to determine the signal configuration of the device that you use.

The TRM complements architecture and protocol specifications and relevant external standards. It does not duplicate information from these sources.

### Configuration and Integration Manual

The CIM describes:

- The available build configuration options.
- How to configure the *Register Transfer Level* (RTL) with the build configuration options.
- How to integrate the GIC-600 into a SoC.
- How to implement the GIC-600 into your design.
- The processes to validate the configured design.

The ARM product deliverables include reference scripts and information about using them to implement your design.

The CIM is a confidential book that is only available to licensees.

## 1.7 Product revisions

This section describes the differences in functionality between product revisions:

<b>r0p0</b>	First release.
<b>r0p0-r0p1</b>	Functional changes are: <ul style="list-style-type: none"><li>• Bug fixes.</li></ul>
<b>r0p1-r0p2</b>	Functional changes are: <ul style="list-style-type: none"><li>• Bug fixes.</li></ul>

# Chapter 2

## Components and configuration

Read this for a description of the major components of the GIC-600.

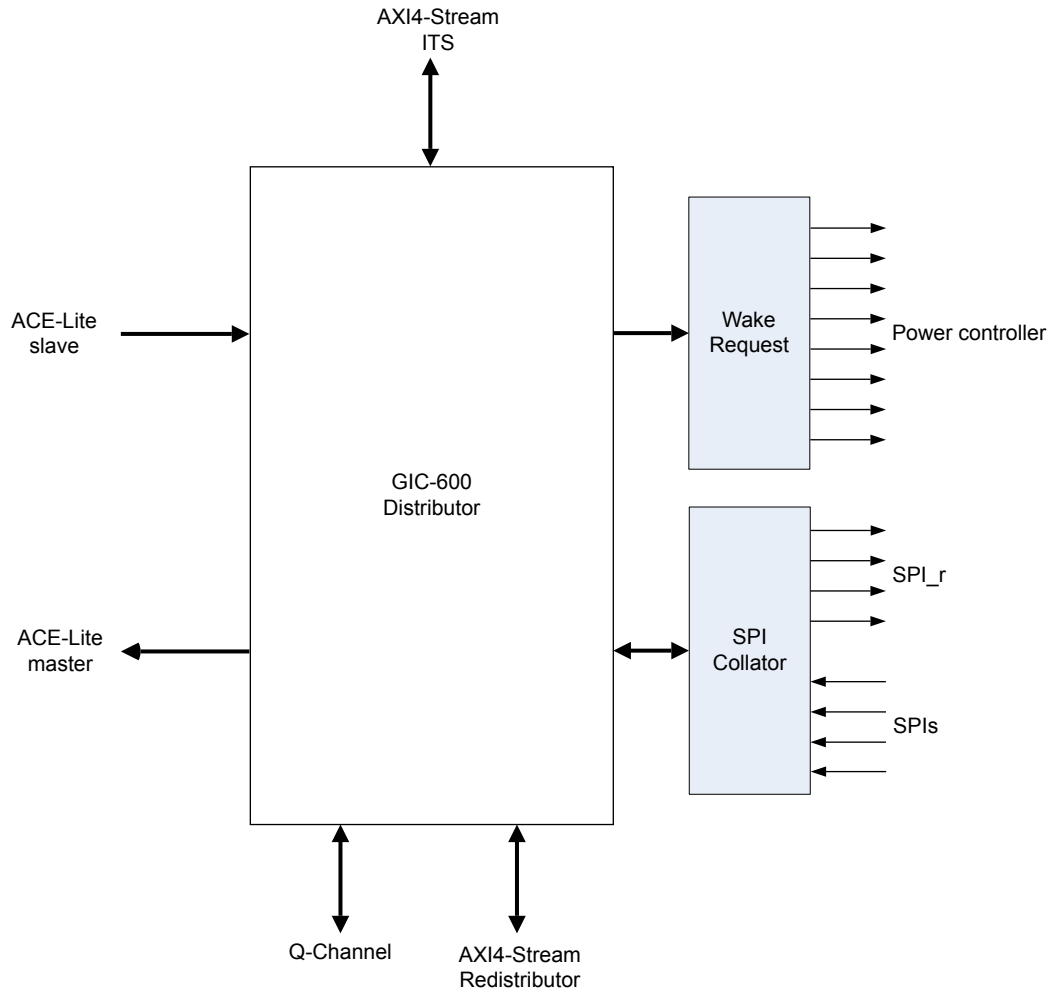
It contains the following sections:

- [2.1 Distributor on page 2-23.](#)
- [2.2 Redistributor on page 2-29.](#)
- [2.3 ITS on page 2-32.](#)
- [2.4 MSI-64 Encapsulator on page 2-37.](#)
- [2.5 SPI Collator on page 2-40.](#)
- [2.6 Wake Request on page 2-42.](#)
- [2.7 Interconnect on page 2-43.](#)
- [2.8 Top-level interfaces on page 2-44.](#)
- [2.9 Top-level configuration on page 2-46.](#)

## 2.1 Distributor

The Distributor is the main communication point between all GIC-600 blocks. It performs SPI and LPI caching, and all communications with other blocks and chips.

The following figure shows the Distributor and its interfaces.



**Figure 2-1 GIC-600 Distributor**

The Distributor is the main hub of the GIC and it implements most of the GICv3 architecture including:

- Programming, forwarding, and prioritization of SPIs, see [3.1.3 SPIs on page 3-48](#).
- Caching and forwarding of LPIs, see [3.1.4 LPIs on page 3-49](#).
- SGI routing and forwarding.
- Register programming of all registers apart from GITS\_TRANSLATER.
- Power control of cores and Redistributor blocks.

This section contains the following subsections:

- [2.1.1 Distributor AXI4-Stream interfaces on page 2-24](#).
- [2.1.2 Distributor ACE-Lite slave interface on page 2-24](#).
- [2.1.3 Distributor ACE-Lite master interface on page 2-25](#).
- [2.1.4 Distributor Q-Channels on page 2-26](#).
- [2.1.5 Distributor miscellaneous signals on page 2-26](#).
- [2.1.6 Distributor configuration on page 2-27](#).

### 2.1.1 Distributor AXI4-Stream interfaces

The GIC-600 uses AXI4-Stream interfaces to communicate between blocks.

These interfaces are fully credited, therefore they never exert anything other than transient backpressure on their **ic<xy>dtready** signals. This enables packets to be routed over any available free-flowing interconnect.

————— **Note** —————

- **ic<xy>** can be **cd**, **pd**, **id**, **dp**, **di**.
- Packets must not be reordered between endpoints, for example, between the Distributor and a single Redistributor block, irrespective of the interconnect that is used. Packets must never be interleaved.

For information about AXI4-Stream signals, see the *ARM® AMBA® 4 AXI4-Stream Protocol Specification*.

The following table lists the AXI4-Stream input interfaces.

**Table 2-1 AXI4-Stream input interface descriptions**

Bus	Destination	Width	ic<xy>dtdest
ICID	ITS to Distributor	16-bit or 64-bit	ITS number
ICPD	Redistributor to Distributor	16-bit, 32-bit, or 64-bit	Redistributor number
ICCD	SPI Collator to Distributor	16-bit	0

The following table lists the AXI4-Stream output interfaces.

**Table 2-2 AXI4-Stream output interface descriptions**

Bus	Destination	Width	ic<xy>dtid
ICDI	Distributor to ITS	16-bit or 64-bit	ITS number
ICDP	Distributor to Redistributor	16-bit, 32-bit, or 64-bit	Redistributor number
ICDC	Distributor to SPI Collator	16-bit	0
ICDW	Distributor to Wake Request block	16-bit	-

Each bus has an associated **ic<xy>twakeup** signal that requests wakeup through the **qactive** signals when the Distributor, or destination block, is hierarchically clock-gated through the Q-Channel. The **ic<xy>twakeup** input signal must be driven from a cleanly registered version of the **ic<xy>dtvalid** signal to prevent spurious wakeups caused by signal glitches.

To ease integration, an arbitrary set of these stream interfaces can be combined into a single port. In this case, an **ic<xy>dtdest** value for the inputs and an **ic<xy>dtid** for the outputs is assigned with a number that increments in the same order as the rows shown in the interface description tables.

### 2.1.2 Distributor ACE-Lite slave interface

The ACE-Lite slave port on the GIC-600 Distributor provides access to the entire register map except for the GITS\_TRANSLATER registers. The interface supports either 64-bit, 128-bit, or 256-bit data widths.

The GIC-600 only accepts single beat accesses of the sizes for each register that are shown in the Programmers model, see [Chapter 4 Programmers model on page 4-83](#). All other accesses are rejected and given either an *OK* or *SLVERR* response that is based on the GICT\_ERR0CTLR.UE bit.



When the GIC-600 is a monolithic configuration, the Distributor and ITS both share an ACE-Lite slave port, and the DeviceID for the ITS translation is taken from **awuser\_s[DEVICE\_ID\_WIDTH+2:3]**. See [2.3 ITS on page 2-32](#), for more information about the ITS.

---

**Note**

---

The **a<x>user\_s[2:0]** signals are not used and must be tied to 0.

---

**Table 2-3 Acceptance capabilities**

Attribute	Capability
Combined acceptance capability	3
Read acceptance capability	2
Read data reorder depth	1
Write acceptance capability	2

The GIC-600 uses **a<x>cache\_s**, **a<x>domain\_s**, and **a<x>bar\_s** signals to detect cache maintenance operations and barrier transactions that are responded to in a protocol-compliant manner but are otherwise ignored. The GIC-600 also ignores other cachability, shareability, and protection settings except Security, **a<x>prot\_s[1]**.

If you are connecting to an AXI3 or AXI4 port, signals **a<x>domain\_s**, **a<x>bar\_s** and, for AXI3, **a<x>len[7:4]** must all be tied to 0.

The GIC-600 has a separate **awakeup\_s** signal to force the GIC to wakeup when it is hierarchically clock-gated through the Q-Channel. The **awakeup\_s** signal must be connected to a cleanly registered version of (**awvalid\_s** | **arvalid\_s**) to ensure that the GIC does not request to be woken up due to incoming signal glitches.

The GIC-600 address map can have several pages. The number of pages depends on your configuration. See [4.1.1 Register map pages on page 4-84](#).

You must set up the system address map so that each core accesses the GICD page on its local chip at the same address. All other pages must be globally accessible, although access of pages on a remote chip by a core is expected to be rare.

In most configurations, the GIC-600 ignores address bits above ceiling ( $\log_2(\text{page\_count}) + 15$ ). For example, a configuration that uses 11 pages ignores address bits above 19, and any address bits of the form 0xFFFFX00000 is accepted to access the GICD page of the memory map. However, in monolithic configurations, where the Distributor and ITS share the ACE-Lite slave port, there are two address tie-offs that specify the full page address of the GICD and GITS\_TRANSLATER pages. The page address comprises address bits[x:16]. For example, if the GICD page is at 32-bit address 0xFFFF0000, the tie-off is 16-bit 0xFFFF. See [2.1.5 Distributor miscellaneous signals on page 2-26](#) for information about the Distributor miscellaneous signals.

### Related references

[4.1.1 Register map pages on page 4-84](#).

## 2.1.3 Distributor ACE-Lite master interface

The GICD uses the ACE-Lite master interface to access LPI Property and Pending tables. If LPIs are not supported, then this interface is not present.

The interface can be configured to be 64-bit, 128-bit, or 256-bit wide.

The following table shows the master port issuing capabilities.

Table 2-4 Issuing capabilities

Attribute	Capability		
	Read	Write	Combined
256-bit aligned read and writes to any Pending table	3	3	3
8-bit read and writes to any Pending table	1	1	1
256-bit aligned reads to the Property table	1	0	1
8-bit reads to the Property table	4	0	4

Each transaction uses a unique transaction ID, and properties come from either the GICR\_PROPBASER or GICR\_PENDBASER registers according to the destination. There is one copy of the attribute fields for all GICR\_PROPBASER registers and another for all GICR\_PENDBASER registers, so software must program these registers to a consistent value in all Redistributors.

The ACE-Lite master port cannot issue barriers or *Cache Maintenance Operations* CMOs. However, it can issue shareable, *ReadOnce* and *WriteUnique*, transactions if programmed to do so.

See [3.2.11 Memory access and attributes on page 3-60](#) for more information.

The **a<x>user\_m** signal outputs the GICR\_TYPER.ProcessorNumber of the core that is associated with each transaction, but it can be ignored and it is not necessary to route it anywhere else.

---

**Note**

See [2.8 Top-level interfaces on page 2-44](#) for changes that occur if this port is shared with an ITS ACE-lite master port.

---

## 2.1.4 Distributor Q-Channels

There is a single Q-Channel for clock gating the GIC-600 Distributor. The Q-Channel interface denies access if the Distributor block is busy processing interrupts.

The Distributor also has a separate Q-Channel that enables power control for each configured ITS. The Q-Channel reads GITS\_CTLR.Quiescent to check whether the ITS is fully disabled. If the Quiescent bit is set, the Q-Channel **qacceptn\_its** signal is asserted, and the GIC guarantees that the bus to the relevant ITS is idle in both directions and that the ITS can be powered down.

---

**Note**

The **qreqn\*** signals are synchronized internally, and can be driven asynchronously. See [A.2 Power control signals on page Appx-A-155](#).

---

## 2.1.5 Distributor miscellaneous signals

The Distributor generates or processes several signals, such as tie-offs, interrupts, and handshakes.

The following table shows the Distributor miscellaneous signals.

**Table 2-5 Distributor miscellaneous signals**

Signal	Direction	Description
chip_id	Input	Tie off this signal to identify the chip in the system. Only present if there is more than one chip in the system.
fault_int	Output	These fault handling and error reporting interrupts are defined in <i>ARM® Reliability, Availability, and Serviceability (RAS) Architecture Extension</i> . The GIC-600 can deliver these interrupts internally but the outputs are provided for any other device such as a system control processor that does not receive normal interrupts from the GIC.  See <a href="#">3.2.15 Reliability, Accessibility, and Serviceability</a> on page 3-64.
err_int	Output	
pmu_int	Output	The PMU counter overflow interrupt. This interrupt can be routed internally but is provided as an external output to trigger an external agent to service the GIC, for example, to read out the PMU counter snapshot registers.  See <a href="#">3.2.14 Performance Monitoring Unit</a> on page 3-63.
sample_req	Input	This 4-phase handshake provides a hardware mechanism to snapshot the PMU counters and has the same effect as writing to the GICP_CAPR register.
sample_ack	Output	
gict_allow_ns	Input	From reset, these tie-off signals control whether Non-secure software can access the GICT RAS, and the GICP PMU, pages. Secure software can override the values at any time.
gicp_allow_ns	Input	
gicd_page_offset	Input	This tie-off signal is used to set the page address bits[x:16] of the GICD page. Only present in monolithic configurations.

### 2.1.6 Distributor configuration

You can configure several options that relate to the operation of the Distributor block.

**Table 2-6 Configurable options for the Distributor**

Feature	Range of options
Affinity0 width	0-8
Affinity1 width	0-8
Affinity2 width	0-8
Affinity3 width	0-8
LPI support	True, False
LPI cache size (entries / 2)	8, 16, 32, 64, 128, 256, 512.
LPI Lock support	True, False
Number of ITS	0-16
Number of Redistributors on chip	1-512
Number of message-based SPIs permitted in system	32-960, in blocks of 32

**Table 2-6 Configurable options for the Distributor (continued)**

Feature	Range of options
Number of SPI wires on chip for wire-based SPIs	0-960
Security support	<p>Options include:</p> <ul style="list-style-type: none"> <li>• Security support programmable. Resets to support security.</li> <li>• Security support always present.</li> <li>• Security support not present.</li> </ul> <p>————— <b>Note</b> —————</p> <p>See <i>Security model</i> in <i>ARM® GICv3 and GICv4 Software Overview</i> for information about the implications of setting Security support to not present.</p> <p>—————</p>

See *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual* for more information.

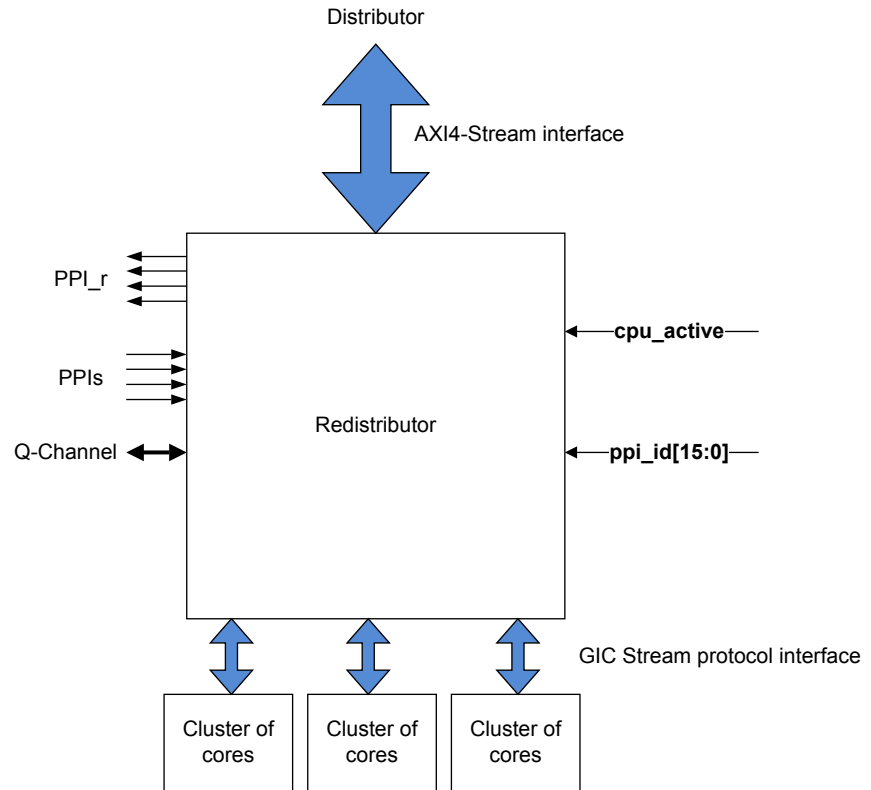
**Related information**

[\*ARM® GICv3 and GICv4 Software Overview.\*](#)

## 2.2 Redistributor

The Redistributor is responsible for PPIs and SGIs that are associated with its related cluster or group of cores. A Redistributor is also referred to as a PPI block.

The following figure shows the Redistributor block.



**Figure 2-2 GIC-600 Redistributor**

The Redistributor performs the following functions:

- Maintaining the SGI and PPI programming.
- Monitoring, and if necessary, synchronizing the PPI wires.
- Prioritizing SGIs, PPIs, and any other interrupts that are sent from the Distributor, and forwarding them to the core.
- Maintaining the GIC Stream protocol and communicating with the cluster.

There can be multiple Redistributors in a configuration and they can be sized to match your system. For example, if you have two clusters of eight cores, then you can have one Redistributor positioned next to each cluster. You can use a Redistributor for each cluster to reduce the PPI wiring and enable the Redistributor to be powered down with the cores for extra power savings. Alternatively, for a small system, combining all cores into one Redistributor block might be the best solution.

### Note

The Redistributor (GICR) registers are programmed through the Distributor ACE-Lite slave port. The Distributor also contains the architectural LPI functionality.

This section contains the following subsections:

- [2.2.1 Redistributor AXI4-Stream interface on page 2-30.](#)
- [2.2.2 Redistributor GIC Stream protocol interface on page 2-30.](#)
- [2.2.3 Redistributor Q-Channel on page 2-30.](#)
- [2.2.4 Redistributor PPI signals on page 2-30.](#)

- [2.2.5 Redistributor miscellaneous input signals](#) on page 2-31.
- [2.2.6 Redistributor configuration](#) on page 2-31.

### 2.2.1 Redistributor AXI4-Stream interface

Each Redistributor has an upstream and downstream AXI4-Stream port for communicating with the Distributor. This interface is either 16-bit or 64-bit wide and uses a fully credited protocol.

### 2.2.2 Redistributor GIC Stream protocol interface

The GIC Stream protocol interface has a pair of 16-bit wide AXI4-Stream interfaces, one upstream interface, and one downstream interface. The GIC-600 uses these interfaces to send interrupts to the core and receive notifications when the core activates interrupts.

The GIC Stream protocol interface, also referred to as the GIC Stream interface, uses the GIC Stream protocol to pass interrupts and responses to the CPU interface inside each core.

**Table 2-7 GIC Stream protocol interface signals**

Signal name	Description
<b>iri</b>	Prefix which identifies the names of the downstream interface signals. These signals are sent by the GIC Stream master. On this interface, the Redistributor is the master and the CPU interface is the slave.
<b>icc</b>	Prefix which identifies the names of the upstream interface signals. These signals are sent by the GIC Stream slave. On this interface, the CPU interface is the master and the Redistributor is the slave.
<b>iritdest</b>	The GIC Stream master interface uses this signal to direct packets to one core within the cluster.
<b>iccdtid</b>	The GIC Stream slave interface uses this signal to determine which core within the cluster sent a packet.

Both the **iritdest** and **iccdtid** can support up to 16 cores that use packed binary encoding, as opposed to one-hot encoding. They can also be divided down using an AXI4-Stream crossbar to support clusters of an arbitrary number of cores from 1-16.

The necessary crossbar is generated as part of the render process.

### 2.2.3 Redistributor Q-Channel

The Redistributor has a single Q-Channel input that is used to ensure that the Redistributor can be clock-gated hierarchically, and safely.

If the Redistributor is busy, actively processing interrupts or sending messages up or downstream, the Q-Channel denies a quiescence request, **qreqn**, by asserting the **qdeny** signal. For more information, see the *AMBA® Low Power Interface Specification, ARM® Q-Channel and P-Channel Interfaces*.

#### Note

The **qreqn** input is synchronized to the Redistributor.

The **qactive** signal is connected to the PPI wires directly, and must be considered as an asynchronous output.

#### Related references

[A.2 Power control signals](#) on page Appx-A-155.

### 2.2.4 Redistributor PPI signals

GIC-600 supports 8, 12, or 16 PPIs, and return wires, for each core. The number of PPIs and return wires must be the same for all cores sharing a Redistributor.

Level-sensitive PPI signals are active-LOW by default, as with previous ARM GIC implementations. However, individual PPI signals can be inverted and synchronized using parameters `GIC600_<config_name>_PPI<ppi_id>_<cpu_number>_<ppi_number>_<INV/SYNC>`.

Every wire has a corresponding wire from after the synchronizer or capture flop. These can be used to create pulse extenders for edge-triggered interrupts that cross clock domains.

**Note**

If you plan to use edge-triggered PPIs and the Q-Channel to clock gate the Redistributor hierarchically, you must use pulse extenders to ensure that interrupts are not missed while the clock is restarted.

### 2.2.5 Redistributor miscellaneous input signals

The Redistributor receives signals that identify the status of each core. It also has a tie-off signal that provides the Redistributor with a unique identifier.

**Table 2-8 Redistributor miscellaneous input signals**

Signal	Direction	Description
cpu_active	Input	This signal indicates if the core is active and not in a low-power state such as retention. The GIC can decide to target only active cores for 1 of N SPIs. See <a href="#">3.2.14 Performance Monitoring Unit</a> on page 3-63.
ppi_id[15:0]	Input	This tie-off signal provides the Redistributor with a unique identifier that is used primarily to ensure that the GIC is correctly integrated into the system.

**Related concepts**

[3.2.5 Power management](#) on page 3-53.

### 2.2.6 Redistributor configuration

You can configure several options that relate to the operation of the Redistributor block.

**Table 2-9 Configurable options for the Redistributor**

Feature	Range of options
Number of cores downstream	1-16
PPIs per core	8, 12, 16
ECC support <sup>a</sup>	True, False
Bus data width	16 or 32
GIC Stream bus structure	Flexible buses and domains

See the *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual* for more information.

**Related information**

[ARM® GICv3 and GICv4 Software Overview](#).

<sup>a</sup> See [3.2.15 Reliability, Accessibility, and Serviceability](#) on page 3-64 for more information.

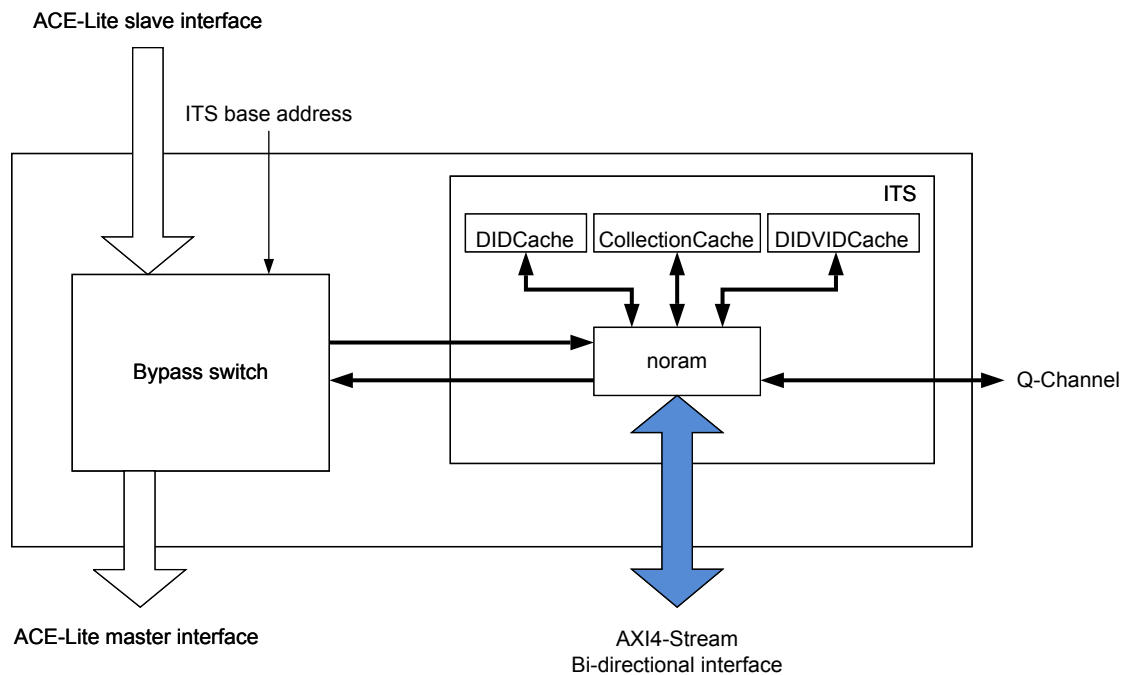
## 2.3 ITS

The ITS provides a software mechanism for translating message-based interrupts into LPIs. The ITS is supported optionally in configurations that support LPIs.

A peripheral generates an LPI by writing to the GITS\_TRANSLATER in the ITS. The write provides the ITS with the following information:

- *EventID* (VID). A value written to GITS\_TRANSLATER. The EventID identifies which interrupt the peripheral is sending. Each interrupt source is identified by an *Interrupt Identifier* (INTID). The EventID might be the same as the INTID, or it might be translated by the ITS into the INTID.
- *DeviceID* (DID). The DeviceID is a unique identifier that identifies the peripheral.

The following figure shows the ITS block.



**Figure 2-3 ITS block**

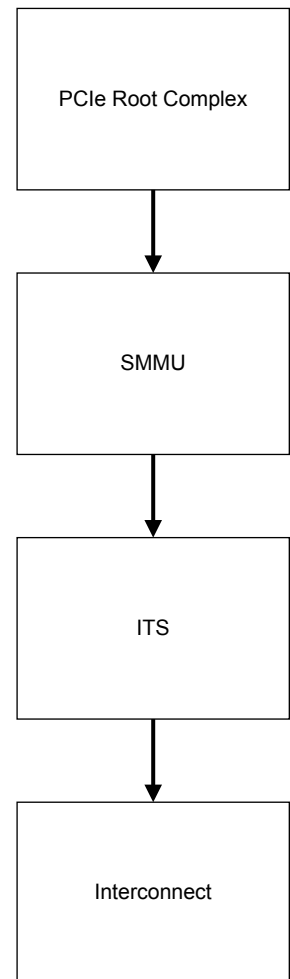
The ITS is an implementation of the GICv3 Interrupt Translation Service as described in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*. The ITS translates MSI requests to the required LPI and target. It also has a set of commands for managing LPIs for core power management.

A main use of the ITS is the translation of MSI/MSIx messages from a PCIe *Root Complex* (RC). To complete the translation, the ITS must be supplied with a DeviceID that is derived from the PCIe RequestorID. To reduce the distance that the DeviceID is transferred and to enable better compartmentalization between RCs, the ITS is best placed next to the RC. To ease integration, the ITS has an optional bypass switch as shown in the ITS block diagram. If the bypass switch is not configured, the ACE\_Lite slave and master ports connect to the ITS directly. See [2.3.1 ITS ACE-Lite slave interface on page 2-33](#) and [2.3.2 ITS ACE-Lite master interface on page 2-34](#).

See [3.2.9 Interrupt translation service \(ITS\) on page 3-57](#) for more information.

The following figure provides an example of the ITS integration process.





**Figure 2-4 ITS integration**

An ITS can be placed anywhere in the system so that it is seen by devices that want to send MSIs. However, the system is responsible for ensuring that the DeviceID reaching each ITS is not spoofed by rogue software using either **a<x>user** signals or MSI-64. See [2.4 MSI-64 Encapsulator on page 2-37](#).

If the ITS is placed downstream of an ACE interconnect, care must be taken to avoid system deadlock. See *Chapter 3, Key integration points of the ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual*.

See [3.2.9 Interrupt translation service \(ITS\) on page 3-57](#) for more information about each inner block.

This section contains the following subsections:

- [2.3.1 ITS ACE-Lite slave interface on page 2-33](#).
- [2.3.2 ITS ACE-Lite master interface on page 2-34](#).
- [2.3.3 ITS AXI4-Stream interface on page 2-35](#).
- [2.3.4 ITS Q-Channel on page 2-35](#).
- [2.3.5 ITS miscellaneous signals on page 2-36](#).
- [2.3.6 ITS configuration on page 2-36](#).

### 2.3.1 ITS ACE-Lite slave interface

The ITS AMBA AXI4 ACE-Lite slave interface has a configurable width of 64 bits, 128 bits, or 256 bits. The slave, master, and address data widths must match.

The ITS ACE-Lite slave port contains only the GITS\_TRANSLATER register. See the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* for more information.

If the bypass switch configuration option is selected, the port accepts all ACE-Lite traffic, and filters accesses to the ITS based on an address match set by the ITS base address tie-off **its\_page\_offset [ADDR\_WIDTH:16]**. Without the bypass switch, the upper bits of the address, 16 and above, are ignored, and the system address decoders must ensure that only relevant ITS writes arrive at the ITS.

The ACE-Lite slave interface ignores all **a<x>snoop**, **a<x>cache**, **a<x>domain**, and **a<x>prot** information other than to filter CMOs and Barriers to ensure that it replies in a protocol-compliant manner.

To generate an LPI, the ITS requires the DeviceID of the issuing master. For PCIe, the DeviceID is derived from the RequestorID.

The GIC-600 supports two different methods for deriving the DeviceID:

- When using the MSI-64 config parameter, the write to GITS\_TRANSLATER is converted to 64-bit accesses at an unmapped system address and the DeviceID is transferred in the upper 32 bits of the access. In this case, only burst length 1, 64-bit ACE-Lite writes are accepted.
- When not using MSI-64, the DeviceID is transported on the **AWUSER** bus with the address (AW) phase of the register access. In this case, burst length 1, 32-bit or 16-bit writes are accepted.

The DeviceID must be transferred using a method that cannot be spoofed by malicious software.

---

**Note**

---

These two modes must not be mixed on a single ITS.

---

The following table shows the attribute configurations.

**Table 2-10 Attribute configurations**

Attribute	With bypass switch	Without bypass switch
Combined acceptance capability	256	3
Read acceptance capability	128	1
Read data reorder depth	128	1
Write acceptance capability	128	2

If the bypass switch is configured, the switch ensures that responses are received from all outstanding writes before routing an MSI to the ITS. This ensures that PCIe ordering requirements are met.

---

**Note**

---

If the bypass switch is configured, the slave and master ports must both have the same data width and the same address width.

If the Distributor and ITS both share the ACE-Lite slave port, some of these properties are changed. See [2.8 Top-level interfaces on page 2-44](#) for more information.

---

The ITS ACE-Lite slave interface has an associated **awakeup** signal. To ensure that incoming traffic wakes the ITS correctly when it is clock gated hierarchically through the Q-Channel, **awakeup** must be driven from a registered version of **awvalid** and **arvalid**. To prevent spurious wake events, ensure that the **awakeup** signal is registered cleanly.

### 2.3.2 ITS ACE-Lite master interface

The ITS AMBA AXI4 ACE-Lite master interface has a configurable width of 64 bits, 128 bits, or 256 bits. If the bypass switch is not included, the ID width is 4 bits. If the bypass switch is included, the ID width is one more than the ID width of the corresponding input channel. The slave, master, and address data widths must match.

The ACE-Lite master port issues accesses to the ITS private tables and Command queue. If the bypass switch is configured, the port also forwards transactions from the slave interface. The ACE-Lite bus can issue I/O coherent transactions, therefore you can place these tables in shared memory if required.

---

**Note**

- When heavily loaded, the ITS creates a necessary dependency between writes on its slave port and reads on its master port. You must ensure that any writes that back up to the slave port do not prevent the free-flow of both reads and writes to the memory.
  - In an ACE system, you must ensure that the write channel from any core cache that could be snooped is not blocked by accesses to the ITS slave port. If the write channel is blocked, and the snoop is prevented from completing its task, a potential deadlock can result.
- 

ARM strongly recommends that if you place the ITS downstream of an ACE interconnect, then you must not place tables in shareable memory.

If the bypass switch is included, apart from transactions that are forwarded from the slave port, the ITS can issue the following transaction types:

- 256-bit aligned read to the Command queue.
- 64-bit aligned read and write to the Device table.
- 32-bit aligned read and write to the *Interrupt Translation Table* (ITT).
- 16-bit aligned read and write to the Collection table.

ITS issued transactions output the DeviceID on the **a<x>user\_** signals. The DeviceID is used for information and does not have to be routed anywhere if it is not required. If the bypass switch is included, ITS issued transactions are identified by a value of 0 on the top bit of the **a<x>id**.

---

**Note**

The ITS supports only one outstanding transaction per ID. This gives a maximum of one outstanding write and five outstanding reads, excluding any transactions from the slave port. If this port is combined with the Distributor ACE-Lite master port, some of these properties are changed. See [2.8 Top-level interfaces on page 2-44](#) for more information.

---

### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 2.3.3 ITS AXI4-Stream interface

The ITS AXI4-Stream interface is a bi-directional AXI4-Stream interface of either 16-bit or 64-bit width for communication between the ITS and the GIC Distributor components on the same chip.

ARM expects a typical distributed system to be 16 bits wide. When a pre-existing wide interconnect is used, the 64-bit option allows messages to be efficiently packed.

The interface is fully credited so all messages can be accepted without dependency on any other ports.

## 2.3.4 ITS Q-Channel

The ITS has a Q-Channel interface which controls requests from an external clock gating source.

If the ITS is busy, the Q-Channel interface asserts the **qdeny** signal to deny an external request to gate its clock. When an external request occurs, the interface requests a wakeup by asserting **qactive**.

---

**Note**

Software-initiated RAM scrub requests, set by GITS\_FCTLR.SIP, also cause the interface to reject requests.

---

The **qreqn** input is synchronized to the ITS. See [A.2 Power control signals on page Appx-A-155](#).

**Related references**

[A.2 Power control signals on page Appx-A-155.](#)

**2.3.5 ITS miscellaneous signals**

The ITS generates or processes several signals, such as an ID tie-off, and the ITS page offset.

**Table 2-11 ITS miscellaneous signals**

Signal	Direction	Description
<b>its_page_offset</b> [ADDR_WIDTH-16:0]	Input	Modifies the address map to ensure only writes to the correct location trigger MSI requests. Only present when the bypass switch is configured.  Specifies the 64K page address that includes the GITS_TRANSLATER register address, and is matched against <b>axaddr</b> [ADDR_WIDTH-16:1].
<b>its_id</b>	Input	This is an ID tie-off. It must be tied to the <b>ic&lt;x&gt;dtdest</b> value used to read the ITS on the AXI4-Stream interface. This ID value feeds into the GITS_CFGID register and is used to check that the GIC system is correctly interconnected. If top-level stitching is used, which creates a hierarchical level from the other components, this signal is not visible.
<b>its_transr_page_offset</b>	Input	This tie-off signal is used to set the page address of the GITS_TRANSLATER register. Only present in monolithic configurations.

**2.3.6 ITS configuration**

You can configure several options that relate to the operation of the ITS block.

**Table 2-12 Configurable options for the ITS**

Feature	Range of options
DeviceID <sup>b</sup>	1-16
EventID size <sup>b</sup>	1-32
Bypass_ports	1 or 0
ACE-Lite data width	64, 128, or 256
MSI-64 support	True or False
ACE-Lite read ID width	1-32
ACE-Lite write ID width	1-32
ECC support <sup>c</sup>	True or False
DID cache size	2, 4, 8, 16, 32, 64, or 128
DID and VID cache size	2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, or 2048
Collection cache size	2, 4, 8, 16, 32, 64, 128, 256, or 512
Domain <sup>d</sup>	Any legal domain identifier

**Related information**

[ARM® GICv3 and GICv4 Software Overview.](#)

<sup>b</sup> See [2.3 ITS on page 2-32](#) for more information.

<sup>c</sup> See [3.2.15 Reliability, Accessibility, and Serviceability on page 3-64](#) for more information.

<sup>d</sup> See [2.8 Top-level interfaces on page 2-44](#).

## 2.4 MSI-64 Encapsulator

The MSI-64 Encapsulator reduces system wiring by combining the DeviceID onto the Data bus for writes to the GITS\_TRANSLATER register.

The following figure shows an overview of the MSI-64 Encapsulator process.

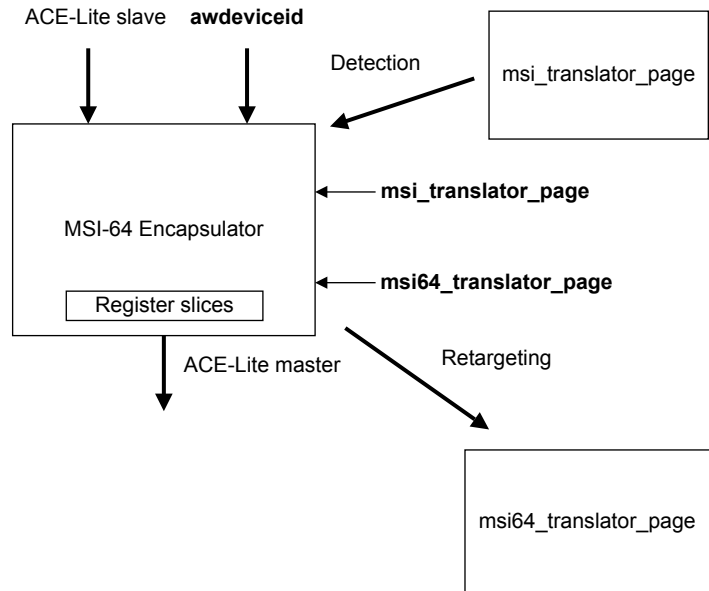


Figure 2-5 MSI-64 Encapsulator

The MSI-64 Encapsulator detects translations that are targeted at the target page address of the GITS\_TRANSLATER register, set by the **msi\_translator\_page** tie-off. It then converts accesses to 64-bit writes with the **awdeviceid** in the upper 32 bits of the data and retargets them to the **msi64\_translator\_page**. This avoids having to use wires to transfer a DeviceID to the GITS\_TRANSLATER register for translation.

See [3.2.12 MSI-64](#) on page 3-62 for more information.

This section contains the following subsections:

- [2.4.1 MSI-64 ACE-Lite interfaces](#) on page 2-37.
- [2.4.2 MSI-64 miscellaneous signals](#) on page 2-38.
- [2.4.3 MSI-64 Encapsulator configuration](#) on page 2-38.

### 2.4.1 MSI-64 ACE-Lite interfaces

The MSI-64 Encapsulator has an ACE-Lite slave interface and an ACE-Lite master interface.

#### MSI-64 ACE-Lite slave interface with awdeviceid

This interface is a full ACE-Lite slave port with an extra **awdeviceid** input signal, which is valid, and must remain stable with **awvalid**.

#### MSI-64 ACE-Lite master interface

This interface is a full ACE-Lite master port.

The following table shows the transaction acceptance capabilities of both slave and master ports.

Table 2-13 Transaction acceptance

Transaction type	Maximum number of transactions allowed
Read	128
Write	128
Combined	256

Any leading **wdata** is registered and held until the **awaddr** signal arrives. These signals are described in [A.5 ACE interface signals on page Appx-A-158](#).

---

**Note**

---

- The MSI-64 Encapsulator requires a data bus that has a width of 64 bits or greater.
  - The ACE-Lite master port never issues more than two addresses before signal **wlast** is asserted.
- 

## 2.4.2 MSI-64 miscellaneous signals

The MSI-64 receives target address signals for the GITS\_TRANSLATER registers, and an ACE-Lite sideband signal.

Table 2-14 MSI-64 miscellaneous signals

Signal	Direction	Description
<b>msi_translator_page</b>	Input	The target page address of the GITS_TRANSLATER register. The MSI-64 Encapsulator does not support a <b>msi_translator_page</b> value of 0.
<b>msi64_translator_page</b>	Input	The target address of the 64-bit GITS_TRANSLATER register.
<b>awdeviceid</b>	Input	The ACE-Lite AW sideband signal that reports the DeviceID for writes to GITS_TRANSLATER. The value is ignored for non-MSI writes.

## 2.4.3 MSI-64 Encapsulator configuration

The MSI-64 Encapsulator does not have any configurable options at design time. However, if this block is generated in your RTL design, it has several parameter options that you can configure.

The MSI-64 Encapsulator is generated as part of any GIC configuration that includes an MSI-64 enabled ITS.

The following table shows the parameter options for the MSI-64 Encapsulator that you can configure at build time.

Table 2-15 Configurable options for the MSI-64 Encapsulator

RTL parameter	Function	Range of options
DATA_WIDTH	Specifies the width of data signals <b>rdata</b> and <b>wdata</b>	64, 128, 256
ADDR_WIDTH	Specifies the width of address signals <b>araddr</b> and <b>awaddr</b>	17-48
AWUSER_WIDTH	Specifies the width of signal <b>awuser</b>	1-128
ARUSER_WIDTH	Specifies the width of signal <b>aruser</b>	1-128
RUSER_WIDTH	Specifies the width of signal <b>ruser</b>	1-128
WUSER_WIDTH	Specifies the width of signal <b>wuser</b>	1-128
BUSER_WIDTH	Specifies the width of signal <b>buser</b>	1-128
DEVICEID_WIDTH	Specifies the width of the DeviceID.	1-20

**Table 2-15 Configurable options for the MSI-64 Encapsulator (continued)**

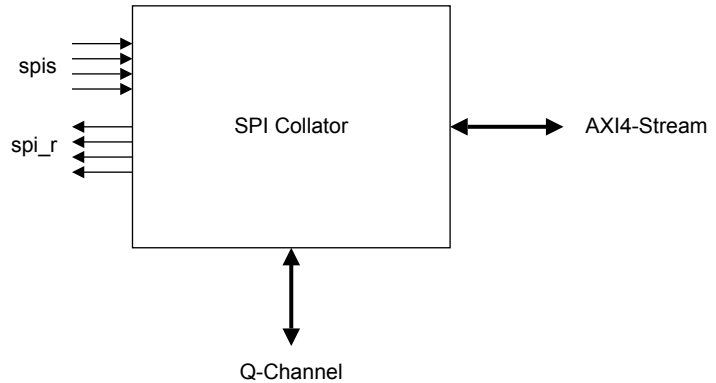
RTL parameter	Function	Range of options
WID_WIDTH	Specifies the width of signal <b>wid</b>	1-32
RID_WIDTH	Specifies the width of signal <b>rid</b>	1-32
FWD_REG_TYPE	Register slice type on forward AW, AR, and W channels.	0 = None 1 = Reverse 2 = Forward 3 = Full
REV_REG_TYPE	Register slice type on reverse AW, AR, and W channels.	0 = None 1 = Reverse 2 = Forward 3 = Full
REV_REG_TYPE	Register slice type on B and R channels	0 = None 1 = Reverse 2 = Forward 3 = Full

The signal width options have the format <AXI\_signal>[RTL parameter - 1:0], for example, **awuser**[AWUSER\_WIDTH - 1:0].

## 2.5 SPI Collator

The SPI Collator converts SPI wires into messages to be sent to the Distributor.

The following figure shows the SPI Collator block.



**Figure 2-6 SPI Collator**

Individual SPIs can be synchronized into the SPI Collator, or the SPI Collator can be placed in the same domain as the interrupt sources and the messages that are synchronized into the Distributor.

Placing the SPI Collator in an always On domain that is remote from the GIC Distributor enables more aggressive power saving because the GIC Distributor can be clock gated hierarchically.

**spi\_r** wires are SPI outputs after synchronization and edge detection. They can be used for cross-domain pulse detection.

This section contains the following subsections:

- [2.5.1 SPI Collator AXI4-Stream interface on page 2-40.](#)
- [2.5.2 SPI Collator wires on page 2-40.](#)
- [2.5.3 SPI Collator Q-Channel on page 2-40.](#)
- [2.5.4 SPI collator configuration on page 2-41.](#)

### 2.5.1 SPI Collator AXI4-Stream interface

The AXI4-Stream interface enables communication between the SPI Collator and the Distributor.

The AXI4-Stream ports apply only transient backpressure to the AXI4-Stream interface.

### 2.5.2 SPI Collator wires

The SPI Collator wires can be extended to create other functions.

By default, the asserted level of a SPI is active-HIGH, as with previous ARM GIC implementations. However, each SPI can be either inverted or synchronized, or both, using the parameters `gic600_<config_name>_SPI_INV[n]` and `gic600_<config_name>_SPI_SYNC[n]`, where:

- `SPI_INV[n] == 1` = inverter enabled.
- `SPI_SYNC[n] == 1` = synchronizer enabled.
- `[n] = SPI_ID - 32`.

Each SPI Collator wire has corresponding wires after the synchronizer or capture flop that can be used to create pulse extenders for edge-triggered interrupts that cross clock domains.

### 2.5.3 SPI Collator Q-Channel

The SPI Collator has a Q-Channel interface that controls requests from an external clock gating source.



When signal **qactive\_col** is LOW, it indicates that all SPIs to the SPI Collator are in their normal state of either 0 (edge-triggered, or active HIGH), or 1 (edge-triggered, or active LOW), and therefore all messages are sent to the Distributor.

If **qactive\_col** is HIGH, the SPI Collator rejects any attempt to enter a low-power mode.

If **qreqn\_col** is LOW and is accepted, the SPI Collator enters low-power mode and the AXI4-Stream channels to the Distributor are flushed out to ensure that there are no messages in progress, enabling the Distributor to be powered down.

---

**Note**

---

In low-power mode, it is only safe to stop the Collator clock if all edge-triggered interrupts into the SPI Collator are pulse extended to ensure that edges are not missed.

---

## 2.5.4 SPI collator configuration

You can configure several options that relate to the operation of the SPI Collator block.

**Table 2-16 Configurable options for the SPI Collator**

Feature	Description
NUM_SPIS	The number of wires.
SPI_BASE	The ID of the first group of 32 SPIs.
SPI_INV	A wide vector of one bit for each SPI indicating the interrupt must be inverted.
SPI_SYNC	A wide vector of one bit for each SPI indicating the interrupt must be synchronized.

### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 2.6 Wake Request

The Wake Request block converts AXI4-Stream wake requests into one **wake\_request** wire for each core. Each **wake\_request** connects to the power controller.

The following figure shows the Wake Request block.



Figure 2-7 Wake Request

The level of the asserted **wake\_request** signal drops only when the core is woken by clearing GICR\_WAKER.ProcessorSleep, or when the Distributor leaves reset.

This section contains the following subsections:

- [2.6.1 Wake Request AXI4-Stream interface on page 2-42.](#)
- [2.6.2 Wake Request miscellaneous signals on page 2-42.](#)
- [2.6.3 Wake Request configuration on page 2-42.](#)

### 2.6.1 Wake Request AXI4-Stream interface

The AXI4-Stream interface enables the Wake Request block to communicate with the Distributor.

The AXI4-Stream interface is fully credited.

### 2.6.2 Wake Request miscellaneous signals

The Wake Request block generates the **wake\_request[<num\_cpus - 1:0>]** signal.

Table 2-17 Wake Request miscellaneous signals

Signal	Description
<b>wake_request[&lt;num_cpus - 1:0&gt;]</b>	This output signal indicates to the power controller that an interrupt is targeting this core and that the core must be woken. When asserted, the <b>wake_request</b> is sticky unless the Distributor is put into the gated state.

### 2.6.3 Wake Request configuration

The configuration of the Wake Request block is based on the number of cores in the system. There are no options to configure.

#### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 2.7 Interconnect

The GIC-600 uses AXI4-Stream interfaces for communication between some blocks.

These blocks are:

- Distributor to and from ITS.
- Distributor to and from Redistributors.
- Distributor to Distributor for cross-chip communications.
- Distributor to and from the SPI Collator.
- Distributor to and from the Wake Request block.

All these interfaces use fully credited schemes where all messages are guaranteed to be accepted without dependency on any other port.

Apart from the cross-chip communications, GIC-600 provides an AXI4-Stream interconnect for transporting messages. However, messages can be sent over an existing interconnect provided the interconnect is free-flowing.

The key requirements of the interconnect are as follows:

- The Distributor must appear at the same address on each chip. This is to maintain the view of a single Distributor across the system.
- Free-flowing access from the ITS and Distributor to memory.
- All AXI4-Stream messages must be free-flowing.
- Accesses to GITS\_TRANSLATER at the ITS must occur at the correct offsets, that is, the subsequent 64K page to the related ITS control registers.

This section contains the following subsection:

- [2.7.1 Interconnect configuration on page 2-43](#).

### 2.7.1 Interconnect configuration

The internal interconnect is configured automatically in accordance with the number of cores and ITS blocks in the system. The configuration produces a balanced tree structure with minimum clock domain crossings.

## 2.8 Top-level interfaces

The top level adds no specific interfaces, but combines the interfaces of other blocks within the domain to reduce the number of domain bridges.

The following figure shows the top-level options.

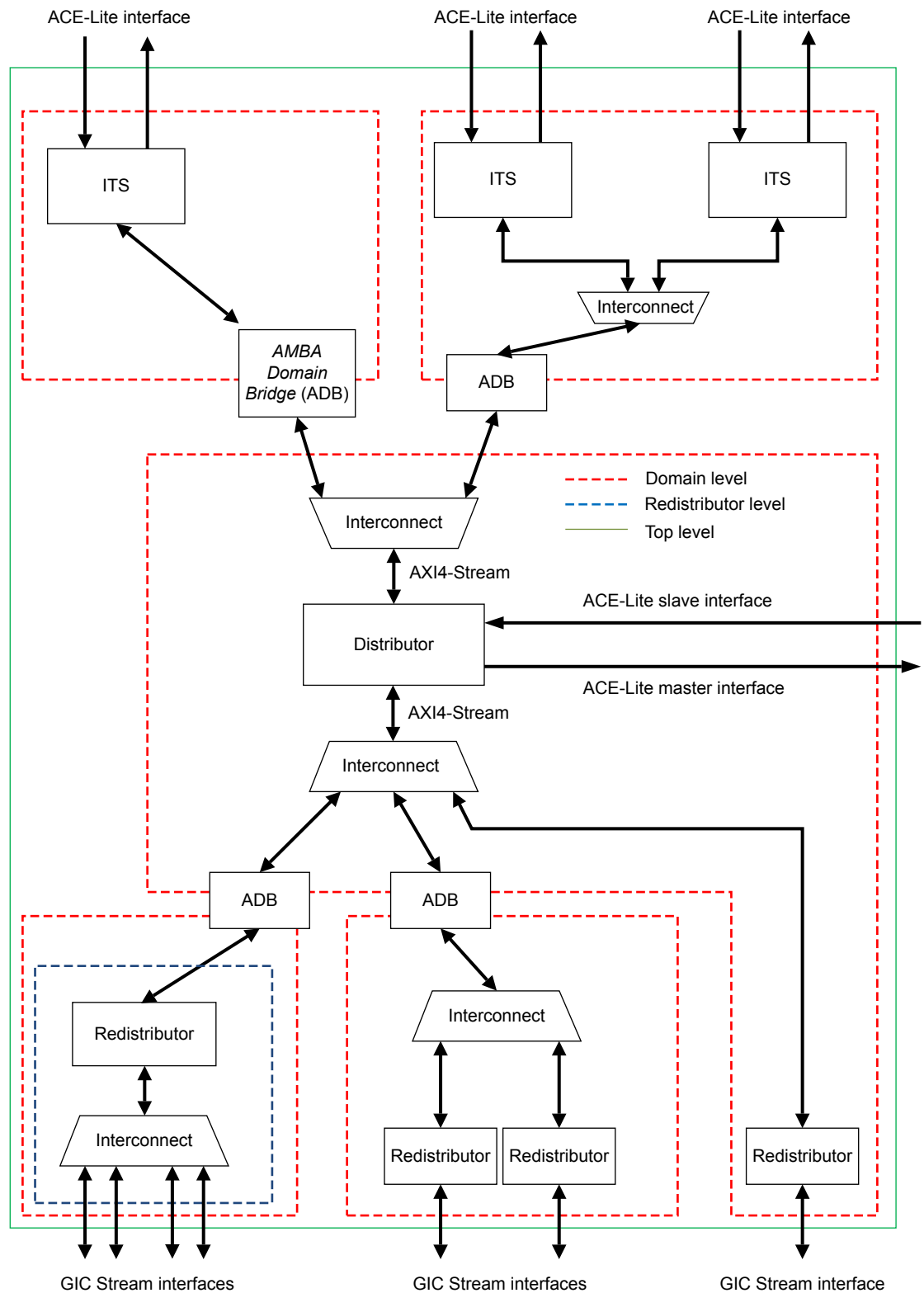


Figure 2-8 GIC top-level structure options

## 2.9 Top-level configuration

The GIC-600 is a distributed system that supports a range of top-level options that are based on the system structure.

**Table 2-18 Top-level configurable options**

Feature	Range of options
Number of chips	1-16
Affinity level that is used for chip selection	2, 3
LPI support	True, False
Number of ITS on chip	0-16 <hr/> <b>Note</b> If there are no ITS blocks in the whole multichip system, then the GIC-600 can optionally support the register-based setting of LPIs. See <i>GICR_SETLPIR</i> register in the <i>ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0</i> . <hr/>
Number of clusters per chip	1-512
Number of cores per chip	1-512

## Chapter 3

# Single-chip operation

Read this for an operational description of the GIC-600 that is configured in a single-chip system.

It contains the following sections:

- [3.1 Interrupt types on page 3-48.](#)
- [3.2 Single chip operation on page 3-50.](#)

## 3.1 Interrupt types

The GIC-600 manages SPIs, SGIs, PPIs, and LPIs.

This section contains the following subsections:

- [3.1.1 SGIs on page 3-48.](#)
- [3.1.2 PPIs on page 3-48.](#)
- [3.1.3 SPIs on page 3-48.](#)
- [3.1.4 LPIs on page 3-49.](#)
- [3.1.5 Choosing between LPIs and SPIs on page 3-49.](#)

### 3.1.1 SGIs

SGIs are inter-processor interrupts, that is, interrupts generated from one core and sent to other cores.

Each core in the system processes an SGI independently of the other cores. The priority of an SGI, and other settings, are also independent for each core.

SGIs are generated by writing to system registers in the CPU interface of the core that generates the interrupt. SGI signals are edge triggered.

Up to 16 SGIs can be recorded for each target core, where each SGI has a different INTID in the range ID0-ID15.

### 3.1.2 PPIs

PPIs are typically used for peripherals that are tightly coupled to a particular core.

Interrupts that are connected to the PPI inputs associated with one core, are only sent to that core. Each core processes a PPI independently of other cores. The settings of a PPI are also independent for each core.

Each PPI has an INTID that identifies its source. A PPI is unique to one core. However, the PPIs to other cores can have the same INTID. Up to 16 PPIs can be recorded for each target core, where each PPI has a different INTID in the range ID16-ID31.

PPI signals are active-LOW level-sensitive by default. However, you can set a PPI signal to be either level-sensitive or edge-triggered using GICR\_ICFGR1, see *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*. You can also set a level-sensitive PPI signal to be active HIGH, see [2.2.4 Redistributor PPI signals on page 2-30](#) for more information. The GIC-600 provides an option, through a parameter, to include one or both a synchronizer and inverter on each PPI interrupt wire.

### 3.1.3 SPIs

SPIs are typically used for peripherals that are not tightly coupled to a specific core.

You can program each SPI to target either a particular core or any core. Activating a SPI on one core activates the SPI for all cores. That is, the GIC-600 allows at most one core to activate a SPI. The settings for each SPI are also shared between all cores.

SPIs are generated either by wire inputs or by writes to the ACE-Lite slave programming interface. The GIC-600 can support up to 960 SPIs corresponding to the external **spi** signal on the SPI Collator. The number of SPIs available depends on the implemented configuration. The permitted values are 32-960, in steps of 32. The first SPI has an ID number of 32.

You can configure whether each SPI is triggered on a rising edge or is active-HIGH level-sensitive. The GIC-600 provides an option, through a parameter, to include one or both a synchronizer and inverter on each SPI interrupt wire.



The GIC-600 uses the SPI Collator to convert wire-based interrupts into messages to reduce system wiring, and to allow more aggressive clock gating of the GIC to reduce power consumption. See [2.5 SPI Collator on page 2-40](#) for more information.

SPIs are programmed through the GICD register space.

You can add a pending state to a valid SPI using GICD\_SETSPI\_NSR or GICD\_SETSPI\_SR, see *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### 3.1.4 LPIs

LPIs are always message-based, and can be from a peripheral, or from a PCIe root complex.

An LPI targets only one core. LPIs are generated when the peripheral writes to the ITS. The ITS contains the registers to control the generation and maintenance of LPIs. The ITS provides INTID translation, allowing peripherals to be owned directly by a virtual machine if an SMMU is also present for those peripherals.

#### Note

- The ITS enables interrupts to be translated to the ID space of the hypervisor instead of directly to a virtual machine.
- Instead of using an ITS, registers can be used to configure the GIC-600 to generate and control LPIs. For more information, see *GICR\_SETLPIR register* in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### 3.1.5 Choosing between LPIs and SPIs

Message-based interrupts can be either LPIs or SPIs.

The decision to use an LPI or SPI for an interrupt can be made by software, and depends on whether there are spare SPIs and if the GIC-600 has ITS support. This can be achieved by either making the peripheral write to a different GIC-600 address, or by changing the address translation for the interrupt write in the SMMU. Changing only the SMMU is possible because the registers for Non-secure message-based interrupts, GICD\_SETSPI\_NSR and GITS\_TRANSLATER, or GICD\_SETLPIR for configurations without LPI support, are at the same address offset in different pages.

The following factors can help you to decide which interrupt type is most appropriate:

- Only the ITS provides INTID translation, therefore LPIs are preferable for peripherals that are owned by a virtual machine. This is because the hypervisor can let the virtual machine program the peripheral directly, and the ITS convert the IDs of interrupts used by the virtual machine to unique physical IDs.
- LPIs are always Group 1 Non-secure, so message-based interrupts that target Secure software must use SPIs.
- Only SPIs are able to target all cores, which means that the GIC-600 attempts to automatically balance the interrupt load to cores that are active but not handling other interrupts.
- The GIC-600 can provide a greater number of LPIs than SPIs.
- You might decide not to include LPI support in a small system where the features of the ITS are not required and there are few message-based interrupts.
- SPIs usually have a better worst-case interrupt latency than LPIs. This is because SPIs have all their settings stored internally to the GIC-600, whereas LPIs that are not cached require external memory accesses. The cache hit rate is expected to be higher for the LPIs that occur more frequently. Therefore, ARM recommends that SPIs are used for any latency-sensitive interrupts that are expected to occur infrequently.

#### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 3.2 Single chip operation

This section describes the operation of a single chip GIC-600.

This section contains the following subsections:

- [3.2.1 Interrupt groups on page 3-50.](#)
- [3.2.2 Interrupt signals \(PPIs and SPIs\) on page 3-50.](#)
- [3.2.3 Affinity routing and assignment on page 3-51.](#)
- [3.2.4 1 of N SPI interrupt selection on page 3-52.](#)
- [3.2.5 Power management on page 3-53.](#)
- [3.2.6 Getting started on page 3-56.](#)
- [3.2.7 Security on page 3-56.](#)
- [3.2.8 Backwards compatibility on page 3-57.](#)
- [3.2.9 Interrupt translation service \(ITS\) on page 3-57.](#)
- [3.2.10 LPI caching on page 3-60.](#)
- [3.2.11 Memory access and attributes on page 3-60.](#)
- [3.2.12 MSI-64 on page 3-62.](#)
- [3.2.13 RAM on page 3-62.](#)
- [3.2.14 Performance Monitoring Unit on page 3-63.](#)
- [3.2.15 Reliability, Accessibility, and Serviceability on page 3-64.](#)

### 3.2.1 Interrupt groups

The GIC-600 configures the interrupts that it receives into one of three groups. Each group determines the security status of an interrupt and how it is routed.

- GICD\_IGROUPRn.
- GICD\_IGRPMODRn.
- GICR\_IGROUPR0.
- GICR\_IGRPMODR0.

These registers control whether each interrupt is configured as:

- Group 0.
- Group 1 Secure.
- Group 1 Non-secure.

Each interrupt is programmed to belong to an interrupt group. Each interrupt group:

- Determines the security state for interrupts in that group, depending on the Exception level of the core.
- Has separate enable bits that control whether interrupts in that group can be forwarded to the core.
- Has an impact on later routing decisions in the core interfaces.

When the GIC-600 is set to security disabled, the meaning and number of interrupt groups are affected.

You can specify GIC-600 security by setting the configuration parameter `ds_value` to either 0, 1 or P, where 0 = Security enabled (fixed), 1 = Security disabled (fixed), P = Security is programmable by software during the boot sequence using GICD\_CTLR.DS.

See the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* for more information.

#### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

### 3.2.2 Interrupt signals (PPIs and SPIs)

The GIC-600 supports two types of physical interrupt signal.

The two types of physical interrupt signal are:

### Level-sensitive

The interrupt is pending while the interrupt input is asserted. As with previous ARM GICs, PPIs are active-LOW, whereas SPIs are active-HIGH by default. However, you can change these default settings, see [3.1 Interrupt types on page 3-48](#) for more information.

### Edge-triggered

A rising-edge on the interrupt input causes the interrupt to become pending. The pending bit is cleared later when the interrupt is activated by the CPU interface.

To set the correct settings for the system, you must program the GICD\_ICFGRn and GICR\_ICFGR1 registers.

The GIC-600 provides optional synchronizers on every interrupt wire input and also return signals, to enable pulse extenders when sending edge-triggered interrupts across domain boundaries, see [2.5.2 SPI Collator wires on page 2-40](#).

### Related information

[ARM® GICv3 and GICv4 Software Overview](#).

## 3.2.3 Affinity routing and assignment

The GIC-600 uses affinity routing, a hierarchical scheme, to identify connected cores and for routing interrupts to specific cores.

The ARM architecture defines a register in a core that identifies the logical address of the core in the system. This register, which is known as the *Multiprocessor Identification Register* (MPIDR), has a hierarchical format. Each level of the hierarchy is known as an affinity level, with the highest affinity level specified first:

- For 32-bit ARMv8 processors, the MPIDR defines three levels of affinity, with an implicit affinity level 3 value of 0.
- For 64-bit ARMv8 processors, the MPIDR defines four levels of affinity.

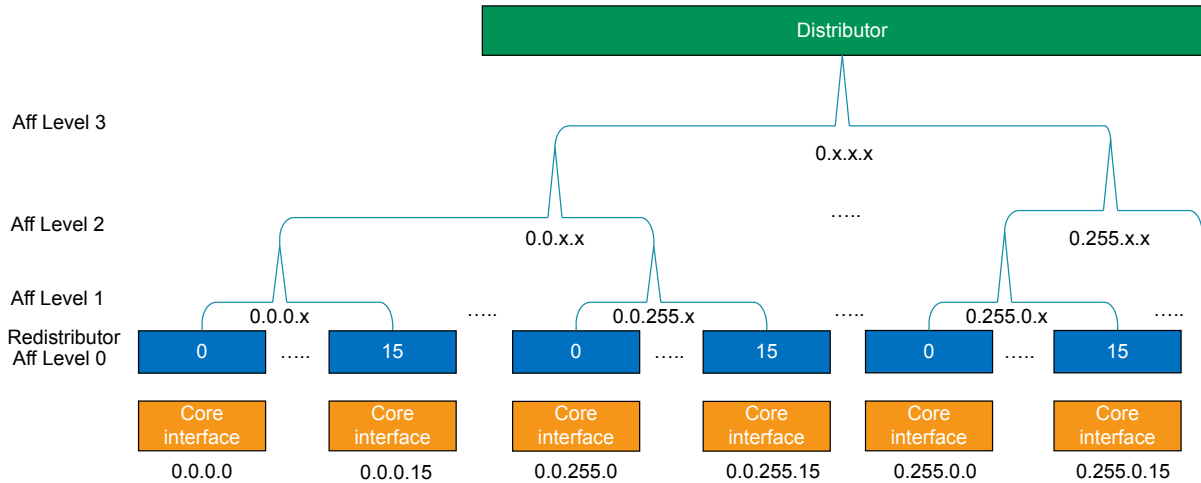
#### Note

The GIC-600 regards each hardware thread of a processor that supports multiple hardware threads as a single independent core.

The affinity of a core is represented by four 8-bit fields using dot-decimal notation, <Aff3>.<Aff2>.<Aff1>.<Aff0>, where Affn is a value for affinity level n. An example of an identification for a specific core would be 0.255.0.15.

The affinity scheme matches the format of the MPIDR\_EL1 register in ARMv8-A. System designers must ensure that the ID reported by the core of the MPIDR\_EL1 register matches how the core is connected to the interrupt controller.

The following figure shows the affinity hierarchical structure.



**Figure 3-1 Affinity routing**

There can be up to 256 nodes at level 3, with each node able to host 256 child level 2 nodes. Similarly each level 2 node can host 256 level 1 nodes. However, level 1 nodes can only host 16 child level 0 nodes.

At affinity level 0, there is a Redistributor. Each Redistributor connects to a single core interface. The Redistributor is used to configure SGIs, PPIs, and LPIs.

The GIC-600 allows fully flexible allocation of MPIDR. However, it has two built-in default assignments that are based on the `aff0_thread` configuration parameter, see *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual*.

- When `aff0_thread == 1`, the four fields are mapped to `0.<cluster>.<core>.<thread>`.
- When `aff0_thread == 0`, the four fields are mapped to `0.0.<cluster>.<core>`.

For more information about affinity routing, see the *ARM® GICv3 and GICv4 Software Overview*.

### 3.2.4 1 of N SPI interrupt selection

The GIC-600 supports 1 of N selection of SPI interrupts.

When the relevant `GICD_IROUTERn.Interrupt_Routing_Mode == 1`, the GIC selects the appropriate core for a SPI.

When `GICD_IROUTERn.Interrupt_Routing_Mode == 0`, the SPI is routed to the core specified by the remaining fields of `GICD_IROUTERn`.

The selections that the GIC-600 makes can be controlled or influenced by several 1 of N features:

#### **cpu\_active**

A **cpu\_active** signal is an input to a Redistributor that corresponds to a particular core. It indicates to the GIC that a core is in a transparent low-power state, such as retention, and that it must be selected as a target for a SPI if there are no other options possible.

A **cpu\_active** signal is typically generated by a power controller, or by power control logic. If this signal is not available in the system, the input must be tied to 1.

#### **Note**

The **cpu\_active** provides an indication only, it cannot stop selection of the core or stop the GIC sending messages to the core.

### **GICR\_CTLR.DPGxx (Disabled Processor Group)**

Setting a DPG bit prevents 1 of N interrupts of a particular group being sent to that core. Any interrupts that have not reached a core at the time of the change are recalled and reprioritized by the GIC. For details of the DPG bits, see *GICR\_CTLR, Redistributor Control Register* in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### **Processor and GICD Group enables and GICR\_WAKER.ProcessorSleep**

A 1 of N interrupt is not sent to a core if the interrupt group is either enabled by the processor and GICD\_CTLR group, or it is asleep as indicated by GICR\_WAKER.ProcessorSleep.

### **Interrupt class**

This is a new IMPLEMENTATION-DEFINED feature introduced with the GIC-600. Each core can be assigned to either class 0 or class 1 by writing to the relevant GICR\_CLASS register. A SPI, programmed as 1 of N, by GICD\_IROUTERn.Interrupt\_Routing\_Mode, can be programmed to target either class 0, class 1, or both classes by the GICD\_ICLARn register. By default, all 1 of N SPIs can go to both classes, therefore the interrupt class feature is disabled by default. The system can use this partitioning for any purpose, for example in a big.LITTLE™ system, all the big cores can be in class 1 and little cores in class 0, allowing 1 of N SPIs to be partitioned according to the amount of processing they require.

### **GICD\_CTLR.E1NWF**

The GICD\_CTLR register E1NWF bit controls whether the GIC-600 wakes a core if there are no other possible targets for a 1 of N SPI.

The GIC tries to wake the minimum of cores possible and only wakes a core if there is no other possible target awake that is able to accept the 1 of N interrupt. To do this, the GIC reads the DPG bits to determine if any core is awake that can accept the interrupt. If a suitable core is not awake, the GIC then wakes a core.

ARM strongly recommends that if you use GICD\_CTLR.E1NWF, you must also set the DPGx bits of register GICR\_CTLR to specify whether a core is likely to accept a particular interrupt group in a timely manner. The GIC does not continue to wake cores until one is found. The GIC-600 uses two passes to try to find the best place for a 1 of N interrupt, by using a round\_robin arbiter between:

- Any core that has **cpu\_active** set, is fully enabled for the interrupt, and has no other pending interrupts.
- Any core that is fully enabled for the interrupt and has no interrupts of a higher priority than the 1 of N interrupt.

If neither option is available to the 1 of N, the interrupt is assigned to any legal target and regularly re-evaluated to ensure that it is not excluded from other SPIs of the same priority.

## **3.2.5 Power management**

The GIC-600 can be powered down by the system power controller, and supports the cores that it services that are also being powered down by the power controller. The GICR\_WAKER and the IMPLEMENTATION-DEFINED GICR\_PWRR registers provide bits to control functions that are associated with power management.

### **Redistributor power management**

At Reset, the Redistributors are considered to be powered down. To power up the Redistributors, software must use the GICR\_PWRR register.

#### **Note**

This is true for all GIC-600 configurations.

The GICR\_PWRR register can control Redistributor power management either by operating through the core, or through the Redistributor.

If operating through the core, each core must program its `GIC_PWRR.RDPD = 0` and `GIC_PWRR.RDAG = 0` to ensure that the Redistributor powers up. Alternatively, a single core can power up the Redistributor for all cores connected to the same Redistributor by writing `GIC_PWRR.RDPD = 0` and `GIC_PWRR.RDAG = 1`.

You can use `GIC_PWRR.RDG` to identify which core shares a Redistributor.

### Processor core power management

The GIC architecture defines the programming sequence to safely power down a core that is connected to the GIC-600.

The powerdown programming sequence uses the `GIC_WAKER.ProcessorSleep` bit. When all cores within a cluster are powered down using the architectural sequence, you can power gate the GIC Stream interface for that cluster.

Before a core is powered down, you must set the `GIC_WAKER.ProcessorSleep` bit to 1. The core must then poll the `GIC_WAKER.ChildrenAsleep` bit to ensure that there are no outstanding transactions on the GIC Stream interface of the core.

To ensure that there are no interrupts during the powerdown of the core, in a typical powerdown sequence you must:

1. Mask interrupts on the core.
2. Clear the CPU interface enables.
3. Set the interrupt bypass disable on the CPU interface.

---

#### Note

The core powerdown sequence that you use must match the core powerdown sequence that is described in the Technical Reference Manual for your processor.

---

When a core is powered down and the `GIC_WAKER.ProcessorSleep` bit is set to 1, if the GIC-600 receives an interrupt that targets only that core, it attempts to wake the core by asserting the **wake\_request** signal that corresponds to that core. The **wake\_request** signal is asserted by the Wake Request block and must be connected to the system power controller.

See [Other core signals on page 3-56](#) for more information about the **wake\_request** signals.

You must not set the `GIC_WAKER.ProcessorSleep` bit to 1 unless the core enters a power state where the GIC-600 uses the power controller to wake the core instead of the GIC Stream interface. For example, with Cortex®-A53 and Cortex-A57, if the core enters a low-power state that is based on the *Wait For Interrupt* (WFI) or *Wait For Event* (WFE) instructions, such as retention, you must not set the `GIC_WAKER.ProcessorSleep` bit to 1.

Software is not required to reprogram the GIC-600 for the core to enter these low-power states.

These interrupts can cause the core to leave the low-power state, entered by executing a WFI or WFE instruction, as defined in the *ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*. The system integrator can use the **cpu\_active** signal to ensure that interrupts that can target multiple cores are much less likely to target cores in certain low-power states. In such a system, software has more control of the conditions under which cores leave low-power states.

---

#### Note

Interrupts that target only one core are unaffected by **cpu\_active** and are always sent to that core. Moreover, if the `GIC_WAKER.ProcessorSleep` bit for that core is set, the **wake\_request** signal is asserted for that core. See [Other core signals on page 3-56](#) for more information about the **cpu\_active** signals.

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See the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* for information about power management, and about wakeup signals and their relation to the core outputs.

## Other power management

The GIC-600 can be powered up and powered down using IMPLEMENTATION-DEFINED protocols.

When powering down the GIC-600, software must preserve the state of the GIC-600, except for any LPI pending interrupts that are preserved in pending tables, as defined in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

You can preserve the LPI pending bits by using the IMPLEMENTATION-DEFINED powerdown sequence, which ensures that the memory pointed to by each GICR\_PENDBASER contains the updated pending information for the LPIs. This powerdown sequence:

1. Completes the powerdown sequence for all cores.
2. Sets GICR\_WAKER.Sleep to 1.
3. Polls GICR\_WAKER until GICR\_WAKER.Quiescent is set.

### Note

- GICR\_WAKER.Sleep can only be set to 1 when:
  - All Redistributors have GICR\_WAKER.ProcessorSleep == 1.
  - All Redistributors have GICR\_WAKER.ChildrenAsleep == 1.
- GICR\_WAKER.ProcessorSleep can only be set to 0 when:
  - GICR\_WAKER.Sleep == 0.
  - GICR\_WAKER.Quiescent == 0.
- Software must not clear GICR\_WAKER.Sleep until GICR\_WAKER.Quiescent is set because the Write is ignored.
- There is only one GICR\_WAKER.Sleep and one GICR\_WAKER.Quiescent bit that can be read and written through the GICR\_WAKER register of any Redistributor.

This sequence ensures that all LPIs that are acknowledged by a write response to the write GITS\_TRANSLATER are saved to the Pending tables. Any interrupt that arrives when the Sleep bit is set to 1 is ignored, and the ACE-Lite transaction completes in accordance with the ACE protocol.

ARM recommends that you disable any interrupt sources before setting GICR\_WAKER.Sleep. However, if you require wake-on-interrupt behavior, the Write to GITS\_TRANSLATER must be gated upstream at a location that enables software to reprogram and enable the GIC-600 without deadlock.

When the GICR\_WAKER.Quiescent bit is set, it is safe to power down the GIC-600. However, you must provide custom mechanisms to wake the GIC-600 if any interrupts arrive that must not be ignored.

When the GIC-600 next powers up, you can program the GICR\_PENDBASER registers to point to the same memory to reload the LPI pending status. If there is no requirement to reload the pending LPIs, ARM recommends that you speed up the initialization of the GIC-600 as follows:

1. Zero the Pending table.
2. Set the GICR\_PENDBASER.PTZ bit to 1.

### Note

GICR\_PENDBASER registers can only be modified before the GICR\_CTLR.Enable\_LPIs bit is set, or when bits GICR\_WAKER.Sleep and GICR\_WAKER.Quiescent are both set.

## Related references

[4.4.3 Power Management Control Register, GICR\\_WAKER on page 4-102.](#)



## Other core signals

The signals **wake\_request** and **cpu\_active** can be used to control how a core is selected to receive interrupts.

Before a core is powered-down, it must set the GICR\_WAKER.ProcessorSleep bit to 1 to disable sending packets over the GIC Stream interface, and wait until the GICR\_WAKER.ChildrenAsleep bit is set to 1. After that is completed, an interrupt that is targeted at that core causes the **wake\_request** signal for that core to be asserted. ARM recommends that you connect this signal to the power controller to cause that core to power up.

When the core wakes, it must set the GICR\_WAKER.ProcessorSleep bit to 0 to resume communications over the GIC Stream interface and to enable its group enables so that the interrupt is delivered to the core.

The GIC-600 uses the **cpu\_active** signal to decide which cores are preferred for SPIs that target multiple cores. The signal does not affect the operation of any other type of interrupt, and has no effect if GICR\_WAKER.ProcessorSleep is set to 1 for those cores.

SPIs that target multiple cores are never sent to cores that have GICR\_WAKER.ProcessorSleep set to 1. ARM recommends that you deassert **cpu\_active** when a core is in a certain software-transparent sleep state that is entered during a WFI or WFE instruction, such as retention. When **cpu\_active** deasserts, the core is less likely to handle SPIs that target multiple cores, and the amount of time that a core spends in these sleep states can increase. If you use this method when **cpu\_active** is deasserted, software must not rely on SPIs that target multiple cores to make a core leave WFI or WFE. Instead, software must use another mechanism to ensure this, such as an SGI, or a SPI targeted at only the core in question.

## Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

### 3.2.6 Getting started

There are some basic tasks that you must complete before you can start to use the GIC-600.

The Redistributor(s) must be powered on using the GICR\_PWRR register to enable the Redistributor(s) to be accessed, see [Redistributor power management on page 3-53](#) for more information.

When the GIC-600 is powered up, it must be programmed as described in the *ARM® GICv3 and GICv4 Software Overview*.

### 3.2.7 Security

The GIC-600 supports the ARM TrustZone technology. Each INTID must be assigned a group and security setting.

The GIC-600 supports the three interrupt groups that are shown in the following table.

**Table 3-1 Security and groupings**

Interrupt type	Example use
Secure Group 0	Interrupts for EL3 (Secure firmware)
Secure Group 1	Interrupts for Secure EL1 (Trusted OS)
Non-secure Group 1	Interrupts for the Non-secure state (OS and the Hypervisor, or one of both)

The following table shows the interrupt signals that are used for each interrupt group, security state, and Exception level.



**Table 3-2 Interrupt signals, security states and Exception levels**

Core Exception level and Security state	Group 0	Group 1	
		Secure	Non-secure
Secure EL0, EL1	FIQ	IRQ	FIQ
Non-secure EL0, EL1, EL2	FIQ	FIQ	IRQ
EL3	FIQ	FIQ	FIQ

Setting the *Disable Security* (DS) bit to 1 in the GICD\_CTLR register removes the security support of the GIC-600. It can be set by Secure software during the boot sequence or configured to be always set when you configure the design using the parameter `ds_value`. When the system has no concept of security, you must set GICD\_CTLR.DS to allow access to important registers.

If you set GICD\_CTLR.DS to 1, only a single security state is supported, in which a system core can be configured as either Secure or Non-secure. In a single security state, register access, and the behavior and number of interrupt groups supported are affected. For more information, see *Interrupt grouping*, and *Interrupt grouping and security* in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

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**Note**

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ARM recommends that you only set GICD\_CTLR.DS if either your system does not support security, or the only software you run does not use security. See *Security model* in GICv3 and GICv4 Software Overview for more information about the implications of setting GICD\_CTLR.DS to 1.

---

If you run software without security awareness on a system that supports security, the Secure boot code can set DS before switching to a Non-secure Exception level to run the software. This enables you to program the GIC-600 from any Exception level and use two interrupt groups, Group 0 and Group 1, so that interrupts can target both the FIQ and IRQ handlers on a core.

Group 0 is always Secure in systems with security. If you decide to write security-unaware software using Group 0, it might not be portable to systems with a concept of security. Security-unaware software is most portable when written using Group 1.

If a system has a concept of security but one or more cores do not, then you must not set DS. Instead each core is only able to enable the interrupt groups corresponding to the security states that it supports.

In security aware systems, secure software can prevent the DS bit from being written by writing to Disable Security Lock bit (GICD\_SAC.DSL). Once set, the DSL bit is cleared only by a hardware reset.

If you know that your system is always security aware, then ARM recommends configuring the GIC-600 without DS support.

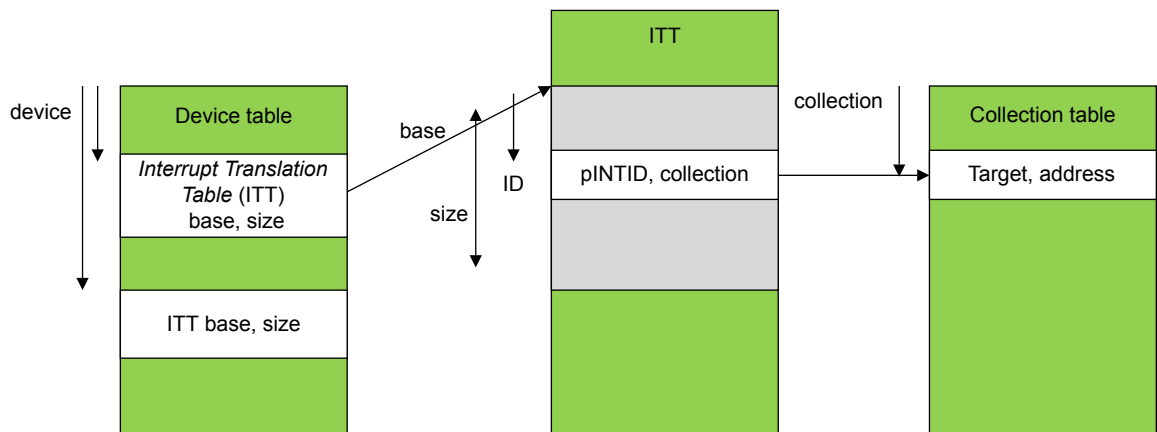
### 3.2.8 Backwards compatibility

The GIC-600 does not support legacy operation, that is, when GICD\_CTLR.ARE\_S or GICD\_CTLR.NS == 0.

### 3.2.9 Interrupt translation service (ITS)

The GIC-600 supports up to 32 ITS blocks in the system with a limit of 16 per chip. Each ITS is responsible for translating message-based interrupts from peripherals into LPIs.

Each ITS is compliant with the GICv3 architecture and is responsible for mapping translation requests with an EventID and DeviceID through to the *physical INTID* (pINTID) and Collection, a group of interrupts, and finally to the target core. The following figure shows the ITS process.



**Figure 3-2 ITS process**

To reduce memory traffic and keep interrupt latency to a minimum, GIC-600 has three two-way set associative caches in each ITS:

- DeviceID to ITT base address.
- DeviceID and EventID to collection.
- Collection to target core.

In small configurations, these caches might be too small to be worth the overhead of implementing them as SRAM. If *Error Correcting Code* (ECC) protection is not required for a cache implemented as an array of flops, and to reduce RAM area, you can remove ECC from each RAM individually, see *Setting configuration options* section in the *ARM® CoreLink™ GIC-600 Generic Interrupt Controller Configuration and Integration Manual*.

It is common for the DeviceID to be a non-contiguous number that is derived from the PCIe RequestorID. To ensure that this does not result in a sparse DeviceID table and wasted memory, the GIC-600 supports indirect Device tables (GITS\_BASERn.Indirect = 1) where the first-level table points at subtables that can be allocated at runtime. See the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* for more details.

The GIC-600 uses memory-backed collections only, which means that before the ITS is enabled by writing to GITS\_CTLR.Enabled, memory must be allocated for the Device table, the Collection table, and the ITS Command queue. Inline with the architecture, these tables must be pre-cleared to 0 by software, apart from pointers to cleared level-two Device tables, unless the tables were previously populated by the GIC-600.

The GIC-600 ITS supports all GICv3 commands as described in the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

GITS\_TYPER.PTA is 0 for all configurations, which means that all references to processor cores in ITS commands are implemented through the GICR\_TYPER.ProcessorNumber field.

Command and translation errors are reported through the RAS registers. See [3.2.15 Reliability, Accessibility, and Serviceability on page 3-64](#).

For details on how to program and use the ITS, see the *ARM® GICv3 and GICv4 Software Overview*.

### ITS cache control, locking, and test

The GIC-600 can lock certain interrupts to the ITS and LPI caches, or to one of either.

If an LPI or translation is missed in a cache, several memory reads can be required to obtain the data necessary from memory. This can result in a range of latency that might not be acceptable for some LPIs.

The GIC-600 can lock certain interrupts to the ITS and, or LPI caches, with the following guarantees:

- Interrupts that are locked in ITS caches always hit and never need any translation.
- Interrupts that are locked in the LPI cache always hit.

Interrupts that are locked in the ITS cache and also locked in the LPI cache, create a virtual channel that ensures those interrupts are never held behind any memory accesses, unless those interrupts are invalidated.

The ITS caches are automatically managed and invalidated as necessary when the GITS\_BASERn registers are updated. Therefore, software intervention is not required. However, to aid debug and integration testing, you can force invalidation of the appropriate cache by setting the relevant bit in the GITS\_FCTLR register.

A forced invalidation of the Event cache abandons all locked entries.

The GITS\_OPR and GITS\_OPSR registers control cache locking, which is DEVICE\_ID, EVENT\_ID, and the correct GITS\_OPR.LOCK\_TYPE (ITS = 2, LPI = 6). The GIC attempts to perform the lock, and reports in GITS\_OPSR. If the lock succeeds, GITS\_OPSR.REQUEST\_COMPLETE == 1 and GITS\_OPSR.REQUEST\_PASS == 1.

Each cache set is two-way set associative. Only one entry can be locked in each cache set. Any attempt to lock a cache set both ways, or a cache set that does not support locking, report as failed in GITS\_OPSR. You can also use the GITS\_OPSR register to unlock entries that are locked.

The GITS\_OPSR register has two test features:

- Trial: Tests the mapping by writing a DeviceID and EventID to GITS\_OPR with GITS\_OPR.LOCK\_TYPE = 1 (TRIAL). This causes the ITS to translate the supplied DeviceID and, or EventID pair, and report the generated target and *physical ID* (PID) in GITS\_OPSR. It also reports if the translation fails, GITS\_OPSR.REQUEST\_PASS == 0, or if it hit a locked entry, GITS\_OPSR.ENTRY\_LOCKED. The interrupt is not set to pending.
- Track: Can be used to detect the arrival of a certain EventID and, or DeviceID pair, which is reported by setting GITS\_OPSR.REQUEST\_COMPLETE.

While any GITS\_OPR operation is in progress, the GITS\_OPSR.REQUEST\_IN\_PROGRESS bit is set and no further updates are accepted by GITS\_OPR until the previous operation completes. To ensure that the operation is accepted, ARM recommends that the GITS\_OPR value is read after writing. You can abort Track operation by writing GITS\_OPR.LOCK\_TYPE == Track\_abort, however, you must allow all other requests to complete.

### ITS commands and errors

Each ITS detects a wide range of command errors and translation errors, and reports them in ARMv8.2 RAS architecture-compliant error records.

The ITS record error syndromes comprise four groups that each have separate enables in the GITS\_FCTLR register. See [Error record classification on page 3-64](#) for information about all the detected syndromes.

**Table 3-3 ITS record error syndrome groups**

Group	Control
ACE-Lite slave Write translation errors. Only when the ITS has a separate ACE-Lite slave port.	GITS_FCTLR.AEE (Access Error Enable)
Translation errors on incoming writes to GITS_TRANSLATOR.	GITS_FCTLR.UEE (Unmapped Error Enable)
Errors during commands.	GITS_FCTLR.CEE (Command Error Enable)
Other errors, such as, memory system, or memory allocation errors.	None

ITS commands must be written by software before they are executed.

The ITS Command queue operates a stall mechanism on any error, irrespective of the GITS\_FCTLR.CEE value. To execute commands, software writes to a Command queue in memory and

then updates the `GITS_CWRITER.Offset` to indicate that there are commands to run. See [3.2.6 Getting started on page 3-56](#) for more information. Normally, the `GITS_CREADR.Offset` increments until it matches the `GITS_CWRITER.Offset`, wrapping as necessary, to indicate that the Command queue has completed.

If an error occurs, `GITS_CREADR.Stalled` is set, which indicates that processing has stopped and software intervention is required. If `GITS_FCTLR.CEE` is set, at least one error is reported in the relevant error record to aid software debug. You can correct the command identified by `GITS_CREADR` and resume the Command queue by writing to `GITS_CWRITER.Retry`. If the command is no longer required, you must rewrite it as a `SYNC` command before you resume.

To determine when Command queue execution has completed, you can use either one of two methods:

- Polling `GITS_CREADR.Offset` until it matches `GITS_CWRITER.Offset`.
- Putting an `INT` command in the queue and waiting for that interrupt to arrive.

For the second method, ARM recommends that you enable `GITS_FCTLR.CEE` and that you configure the `fault_handling`, or `error_recovery` interrupt to be delivered to a core that can resolve Command queue issues. See [3.2.15 Reliability, Accessibility, and Serviceability on page 3-64](#) for more information.

### 3.2.10 LPI caching

If LPI support is configured, the GIC-600 supports a single LPI cache per chip.

The LPI cache is two-way set associative based on the lowest bits of the LPI `INTID`, and stores LPI properties from the LPI Property table. The relevant set is checked for valid properties as each LPI arrives in the system.

The cache is fully associative for pending LPIs, which means that the LPI system fills almost all lines in the cache before sending anything to the Pending tables. The GIC-600 is not optimized for collating LPIs that have the same `INTID`. However the system is designed to reorder and sort the cache over time. In some circumstances, this can cause duplicated interrupts to not be collated efficiently. However, the reduced use of the Pending table, results in better latency bounds under load.

This method of caching means that priorities are associated with an incoming LPI and remain with it until it is serviced. Changes in the LPI Property table are not accepted by the GIC until the relevant `INV` and `SYNC` commands are executed through an `ITS`, `GICR_INVLPIR` or `GICR_INVALLR`.

The GIC-600 considers priority and enable when choosing data to retain in the cache. However, pending interrupts always take priority over interrupts that are not pending, so there is no guarantee that the highest priority interrupt data always remains stored in the cache.

To ensure the lowest possible latency for a small subset of LPIs, the GIC offers a cache-locking option in the LPI cache. If the same interrupt is locked in both the `ITS` and LPI caches, when accepted by the `ITS`, the interrupt follows a virtual channel through the GIC. This guarantees that the interrupt reaches all necessary caches before it reaches the core, and is not blocked by memory accesses from other interrupts.

#### Note

A locked interrupt must remain the highest priority and fully enabled to guarantee that it is delivered to the core before any other interrupt.

The type of cache lock is set by the `GITS_OPR` register, see [4.6.4 Operations Register, `GITS\_OPR` on page 4-118](#).

### Related references

[2.1.6 Distributor configuration on page 2-27](#).

### 3.2.11 Memory access and attributes

The LPI and `ITS` transactions are located in memory tables whose locations are defined in registers that specify their base address, size, and access attributes.

The **a<x>cache** and **a<x>domain** mappings for memory transactions generated by the GIC are shown in the following table.

**Table 3-4 Memory access registers**

Access type	Register	Mapping control bit <sup>e</sup>
LPI Property table	GICR_PROPBASER	GICD_FCTLR.DCC
LPI Pending table	GICR_PENDBASER	
ITS Device table	GITS_BASER0	
ITS Translation table	GITS_BASER0	
ITS Collection table	GITS_BASER1	
ITS Command queue	GITS_CBASER	

The main cacheability value is derived from the \*BASER\*.OuterCache field, unless it is zero, in which case the cacheability value is a value that is shown in the following table.

**Table 3-5 Cacheability values**

Main cacheability value (*BASER*.OuterCache field)	Other cacheability value (*BASER*.InnerCache field)	ARCCACHE	AWCCACHE	ARCCACHE (DCC = 1)	AWCCACHE (DCC = 1)
0b000, Device-nGnRnE	-	0b0010	0b0010	0b0010	0b0010
0b001, Normal Non-cacheable	Match	0b0011	0b0011	0b0011	0b0011
0b001, Normal Non-cacheable	No match	0b0011	0b0011	0b0011	0b0011
0b010, Normal cacheable RA Write-Through	Match	0b0011	0b0011	0b1110	0b0110
0b010, Normal cacheable RA Write-Through	No match	0b0011	0b0011	0b1110	0b0110
0b011, Normal cacheable RA Write-Back	Match	0b1111	0b0111	0b1111	0b0111
0b011, Normal cacheable RA Write-Back	No match	0b0011	0b0011	0b1111	0b0111
0b100, Normal cacheable WA Write-Through	Match	0b0011	0b0011	0b1010	0b1110
0b100, Normal cacheable WA Write-Through	No match	0b0011	0b0011	0b1010	0b1110
0b101, Normal cacheable WA Write-Back	Match	0b1011	0b1111	0b1011	0b1111
0b101, Normal cacheable WA Write-Back	No match	0b0011	0b0011	0b1011	0b1111
0b110, Normal cacheable WA RA Write-Through	Match	0b0011	0b0011	0b1110	0b1110
0b110, Normal cacheable WA RA Write-Through	No match	0b0011	0b0011	0b1110	0b1110

<sup>e</sup> The mappings are designed for the ARMv8 and ARMv8.2 generation of cores. However, setting this bit converts the GIC-600 to full featured mapping.

Table 3-5 Cacheability values (continued)

Main cacheability value (*BASER*.OuterCache field)	Other cacheability value (*BASER*.InnerCache field)	ARCCACHE	AWCACHE	ARCCACHE (DCC = 1)	AWCACHE (DCC = 1)
0b111, Normal cacheable WA RA Write-Back	Match	0b1111	0b1111	0b1111	0b1111
0b111, Normal cacheable WA RA Write-Back	No match	0b0011	0b0011	0b1111	0b1111

Signal **a<x>domain** is driven according to the \*BASER\*.Shareability field unless the resultant cacheability is Device, or Non-cacheable, in which case it becomes 0b11, system Shareable in accordance with the *ARM® AMBA® AXI and ACE Protocol Specification*.

### 3.2.12 MSI-64

The MSI-64 Encapsulator can be used to combine the DeviceID into single memory access writes to the GITS\_TRANSLATER register in the ITS.

The ITS translates DeviceID/EventID pairs into LPI physical INTIDs.

A normal MSI/MSI64 write contains the EventID in the lower 16 bits or 32 bits of data. However, the DeviceID must be transported using a different method. The DeviceID is often derived directly from a PCIe RequestorID or *System Memory Management Unit* (SMMU) StreamID.

The GIC-600 ITS supports two mechanisms:

#### awuser\_its[\_<num>]\_s

The DeviceID arrives on sideband user signals. The system integrator must ensure that rogue software cannot directly or indirectly, perform an access to the GITS\_TRANSLATER register with a DeviceID that matches a real device.

#### MSI-64

When configured to support MSI-64, the ITS expects the DeviceID to be in the upper 32 bits of a 64-bit write to the GITS\_TRANSLATER register.

To prevent rogue software accessing the GITS\_TRANSLATER register and spoofing any device, ARM recommends that the GITS\_TRANSLATER registers are moved to an arbitrary page that is protected by the Hypervisor.

The GIC-600 uses two methods to support this:

- The MSI-64 Encapsulator modifies the page address of accesses to the architectural GITS\_TRANSLATER address, set by the **msi\_translator\_page** tie-off, to the system-defined page set by **msi64\_translator\_page**.
- When the ITS shares an ACE-Lite slave port, a separate page address tie-off **gits\_translator\_page**, allows the GITS\_TRANSLATER register page to be moved to anywhere in the address map to match the **msi64\_translator\_page** value that is independent of the GICD address map reset.

#### Note

The **msi64\_translator\_page** must not be on top of any other GIC register page.

To ensure that this method of mapping is hidden from software, all accesses to the **msi64\_translator\_page** must pass through an Encapsulator, or similar embedded functionality. See [2.4 MSI-64 Encapsulator on page 2-37](#) for more information about the MSI-64 Encapsulator.

### 3.2.13 RAM

The GIC-600 uses multiple RAMs to store a range of states for all types of interrupt.

In typical operation, the RAMs are transparent to software.

A RAM is protected from errors using an ECC with *Single Error Correction and Double Error Detection* (SECCDED). If single or double errors are detected, they are reported in the software visible error records, see [3.2.15 Reliability, Accessibility, and Serviceability on page 3-64](#) for more information.

### 3.2.14 Performance Monitoring Unit

The GIC-600 contains a PMU for counting key GIC events from both the Distributor and any configured ITS blocks on the same chip.

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#### Note

Redistributor events are not tracked by the PMU. The delivery of PPI and SGI interrupts can be counted by recording calls to the core interrupt service routine.

---

The PMU has five counters with snapshot capability and overflow interrupt.

Secure software must enable Non-secure access to the GICP, PMU register space, and ensure that Secure and Non-secure interrupts are counted together. This can be done by programming the GICD\_SAC.GICPNS bit, or by integrating the GIC with the **gicp\_allow\_ns** tie-off set HIGH.

---

#### Note

If GICD\_CTLR.DS == 1, the GICP register space is accessible to all software.

---

### Count configuration

Each PMU counter can be programmed individually to count a range of events.

To configure a counter:

1. Program the counter GICP\_EVCNTRn to a known value. This could be 0 to count events, or a higher number to trigger an overflow after a known number of events.
2. Program the associated GICP\_EVTYPERN to count the required event.
3. Program the required filter type for the event by programming GICP\_FRn.
4. Enable the counter by programming the corresponding bit in GICP\_CNTENSET0.
5. Repeat the previous steps for all counters that are required.
6. Enable the global count enable in GICP\_CR.E.

---

#### Note

PMU registers, other than enables, do not have resets and must be programmed before use.

---

### Count filtering

#### Overflow interrupt

The overflow interrupt can be enabled on a per counter basis by enabling the relevant bit of GICP\_INTENSET0, where bit0 enables GICP\_EVCNTR0, bit1 enables GICP\_EVCNTR1, and so on. Similarly, the overflow interrupt enable can be disabled by corresponding Writes to GICP\_INTENCLR0.

When enabled, the interrupt activates at any of these events:

- A write to a GICP\_OVSSET0 for any counter.
- An overflow on any enabled counter.

The GICP\_OVSSET0 and GICP\_OVSCLR0 can be used for save and restore operations and for testing the correct integration of the **pmu\_int** interrupt.

The **pmu\_int** can be used to trigger external logic, for example, to trigger a Read of the captured data.



## Snapshot

Each PMU counter GICP\_EVCNTRn has a corresponding GICP\_SVNn snapshot register. On a snapshot event, all five counters are copied to their backup registers so that all consistent data is copied out over a longer period.

The snapshot events are:

- A handshake on the four phase **sample\_req/sample\_ack** external handshake.
- A write of 1 to the GICP\_CAPR register CAPTURE field.
- An overflow of an enabled counter when GICP\_EVTYPERN.OVFCAP is set.

### Note

There is only one set of snapshot registers, therefore data is replaced in multiple capture events.

## 3.2.15 Reliability, Accessibility, and Serviceability

RAM is protected with SECDED and ECC, and can be checked by software to determine valid entries. RAM and software errors are reported in records and can be assigned to fault handling or error recovery interrupts.

### Non-secure access

You can control whether Non-secure software has access to the register space by using GICD\_SAC.GICTNS. Its reset value is set by the **gic\_allow\_ns** tie-off signal.

In the case of an error, and if the GICD\_CTLR.DS == 0, all SPIs, PPIs, and SGIs, resort to a secure group. Therefore, interrupt programming is not revealed to the Non-secure side. See [Software error record 0 on page 3-66](#) to [ITS software error records 13+ on page 3-75](#) for more information.

### Scrub

The GIC-600 holds many states including all associated interrupt types in RAM that is protected by the scrub system.

RAM is protected with SECDED, and ECC. However, the contents of some RAM is expected to be static over long periods of time. There is a potential for errors to accumulate if a particular address is not accessed after a period. To prevent this, software can trigger a low\_priority scrub through GITS\_FCTLR.SIP, GICR\_FCTLR.SIP, and GICD\_FCTLR.SIP. This process triggers a check and if necessary, a Write-Back, of all valid RAM entries.

### Error record classification

The GIC reports errors in ARMv8.2 RAS architecture-compliant error records.

There are four classes of error records:

- Correctable ECC errors.
- Uncorrectable ECC errors.
- ITS command errors.
- Software access errors.

The error records have a separate reset so that they can be read after a main GIC reset to determine any problems.

### ECC error reporting and recovery

When an ECC error is detected, the GIC-600 attempts to contain the error and ensure it cannot propagate further.

You can program the GIC-600 to trigger a SPI as a fault\_handling interrupt. The following table shows the ECC error reporting of components by RAM.



**Table 3-6 ECC error reporting**

RAM	Action
ITS caches	All ITS caches are memory that is backed. The contents are reloaded from memory. However, if entries are locked in the cache, the lock is lost. Locked entries are the highest priority for reporting in the error record.
SPI	All information about the SPI is reported and the interrupt is returned to its reset values. The SPIs that are in the error state can also be determined by reading the GICD_IERRRn register. This SPI is not reused until it is reprogrammed and re-enabled.
LPI	<p>All information from the RAM entry is reported. Software can determine the set of interrupts that might have errors, based on the reported ID, to check priority, and to target information.</p> <p>If a <i>Double Error Detect</i> (DED) error occurs on a locked entry, the lock is lost.</p> <p>————— <b>Note</b> —————</p> <p>Repeated double errors in the LPI cache cause an overflow of the error record, which means subsequent information is lost. ARM recommends that a high priority SPI is used to trigger a core to clear the error record as fast as possible.</p> <p>—————</p>
Redistributor RAM	<p>In the Redistributor, only group and priority are maintained in the RAM. If an error occurs, this information becomes UNKNOWN for four interrupts. Pending and Active states are maintained but the enable is cleared so that the interrupt is not forwarded.</p> <p>You can determine the interrupts that are in error by reading the GICR_IERRV register.</p> <p>————— <b>Note</b> —————</p> <p>Because the group is UNKNOWN, it is assumed to be Secure, and therefore interrupt deactivates can be ignored. Software must consider this as part of the recovery sequence.</p> <p>—————</p> <p>It is also possible for a GenerateSGI packet to become corrupted. In this case, the GenerateSGI is reported as bad, and software can read the remaining data to determine how to recover.</p> <p>For more information about Pending and Active PPI states, see <i>ARM® GICv3 and GICv4 Software Overview</i>.</p>
SGI	The SGI RAM holds group and <i>Non-Secure Access Control</i> (NSACR) information for all cores. It is used to enable wakeup of the Redistributor as required. If an error occurs in the RAM, then all SGIs for that core are considered to be Secure. This prevents Non-secure masters from raising Secure interrupts incorrectly.

## Error recovery and fault handling interrupts

You can assign a recorded correctable ECC error to the fault\_handling interrupt by setting GICT\_ERR<n>CTLR.CFI.

All correctable ECC errors have error counters, therefore, the interrupt only fires when the counter in the associated GICT\_ERR<c>MISC0 register overflows. You can preset the counter in GICT\_ERR<c>MISC0 bits 32-40 to any value by Writing to GICT\_ERR<c>MISC0. For example, to fire an interrupt on any correctable error, Write 0xFF, or to fire an interrupt on every second correctable error, Write 0xFE.

You can assign a recorded uncorrectable ECC error either to the fault\_handling interrupt, **fault\_int**, by setting GICT\_ERR<n>CTLR.FI, or to the error recovery interrupt, **err\_int**, by setting GICT\_ERR<n>CTLR.UI. The interrupt fires on every uncorrectable interrupt occurrence irrespective of the counter value.

You can route interrupts **fault\_int** and **err\_int** out as interrupt wires for situations where error recovery is handled by a core that does not receive interrupts directly from the GIC, such as a central system control processor. Alternatively, you can drive each interrupt internally by programming the associated GICT\_ERRIRQCR<x> register.

Each GICT\_ERRIRQCR<n> register contains an ID field that must be programmed to 0 if internal routing is not required, or if internal routing is required, to a legally supported SPI ID. If the programmed

ID is below 32, out of range, or for multichip configurations, not owned on chip, the register updates to 0 and no internal delivery occurs.

The interrupt active bit is stored in RAM. This allows the *Interrupt Service Routine* (ISR) to cope with instances where there is a DED error on the SPI programming and the current active status is ignored, or in rare circumstances, the interrupt might be delivered while the ISR is active.

ARM recommends that if the **err\_int** and **fault\_int** are internally routed, the target interrupts must not have SPI Collator wires, or if they are present, are tied off. This prevents software checking for the same ID at multiple destinations.

The **err\_int** and **fault\_int** do not have direct test enable registers. You can test connectivity using error record 0 and triggering an error, such as an illegal AXI access to a non-existent register.

### Error handling records

The GIC-600 has several ARMv8.2 RAS architecture-compliant error records. The range of error handling records that are available depends on the configuration of the GIC-600.

The GIC-600 error handling records are listed in the following table.

**Table 3-7 Error handling records**

Record	Description
0	Uncorrected software error in the Distributor.
1	Corrected SPI RAM error.
2	Uncorrected SPI RAM error.
3	Corrected SGI RAM error.
4	Uncorrected SGI RAM error.
5	Corrected <i>Target</i> (TGT) cache error. Not used if there are less than 16 cores.
6	Corrected TGT cache error. Not used if there are less than 16 cores.
7	Corrected PPI RAM error.
8	Uncorrected PPI RAM error.
9	Corrected LPI RAM error. Not present if there is no LPI support.
10	Uncorrected LPI RAM error. Not present if there is no LPI support.
11	Corrected error from ITS RAM. Not present if an ITS is not present.
12	Uncorrected error from ITS RAM. Not present if an ITS is not present.
13+	Uncorrected software error in ITS. One record per ITS on the chip. Not present if an ITS is not present.

The details, events, and recovery sequences of each record are described in [Software error record 0](#) on page 3-66 to [ITS software error records 13+](#) on page 3-75.

### Software error record 0

Software error record 0 records software errors that are uncorrectable.

Record 0 contains software programming errors from a wide range of sources within the GIC-600. In general, these errors are contained. For uncorrected errors, the information that is provided gives enough information to enable recovery without significant loss of functionality.

ARM recommends that record 0 is connected to a high priority interrupt. This prevents the record from overflowing if it receives more errors than it is able to process with the possible loss of information

required for recovery. See [Error recovery and fault handling interrupts on page 3-65](#) for more information.

The following table describes the syndromes that are recorded in record 0, the reported information, and recovery instructions.

**Table 3-8 Record 0 software errors**

IERR	SERR	GICT_ERR<n>MISC0.Data	Recovery, Prevention
0x00, SYN_ACE_BAD Illegal ACE-Lite Slave Access.	0xE	AccessRnW, bit[12] AccessSparse, bit[11] AccessSize, bits[10:8] AccessLength, bits[7:0]	Repeat illegal access, with appropriate size and properties.  Full access address is given in GICT_ERR0ADDR.
0x01, SYN_PPI_PWRDWN Attempt to access a powered down Redistributor.	0xF	Redistributor, bits[24:16] Core, bits[8:0]	Ensure that the Redistributor is powered up before accessing. See <a href="#">4.4.5 Power Register, GICR_PWRR on page 4-104</a> .  Attempt was made by the core reported in MISC0.
0x02, SYN_PPI_PWRCHANGE Attempt to power down Redistributor rejected.	0xF	Redistributor, bits[24:16] Core, bits[8:0]	Ensure that the core accessing the register, or all cores with the same GICR_PWRR.RDG if GICR_PWRR.RDAG is set, has completed the GICR_WAKER.ProcessorSleep handshake.
0x03, SYN_GICR_ARE Attempt to access GICR or GICD registers in mode that cannot work.	0xF	Core, bits[8:0]	Repeat the access to the specified core accessing the correct register space. That is, if ARE_S and ARE_NS == 1 then PPI and SGI registers must be accessed through the GICRx instead of GICD register space.
0x04, SYN_PROPBASE_ACC Attempt to reprogram PROPBASE registers to a value that is not accepted because another value is already in use.	0xF	Core, bits[8:0]	GICR_PROPBASER is shared between all cores on a chip. Once any GICR_CTLR.Enable_LPIs bit is set, the value is locked and cannot be updated unless a complete GICR_WAKER.Sleep handshake is complete.  See <a href="#">A.2 Power control signals on page Appx-A-155</a> .
0x05, SYN_PENDBASE_ACC Attempt to reprogram PENDBASE registers to a value that is not accepted because another value is already in use.	0xF	Core, bits[8:0]	Once any GICR_CTLR.Enable_LPIs bit is set, the Shareability, InnerCache, and OuterCache fields are locked for the whole chip. They can only be changed by completing the GICR_WAKER.Sleep handshake.  See <a href="#">A.2 Power control signals on page Appx-A-155</a> . Otherwise, repeat the register access using the current global values.

**Table 3-8 Record 0 software errors (continued)**

<b>IERR</b>	<b>SERR</b>	<b>GICT_ERR&lt;n&gt;MISC0.Data</b>	<b>Recovery, Prevention</b>
<b>0x06, SYN_LPI_CLR</b>  Attempt to reprogram ENABLE_LPI when not enabled and not asleep.	0xF	Core, bits[8:0]	ARM recommends that you do not clear the Enable_LPIs bit. Instead, interrupts must be unmapped using an ITS. If you must clear, then you must flush the LPI cache using the GICR_WAKER.Sleep handshake.  See <a href="#">A.2 Power control signals</a> on page Appx-A-155.
<b>0x07, SYN_WAKER_CHANGE</b>  Attempt to change GICR_WAKER abandoned due to handshake rules.	0xF	Core, bits[8:0]	GICR_WAKER.ProcessorSleep and GICR_WAKER.ChildrenAsleep form a four-phase handshake. The attempt to change state must be repeated when the previous transition has completed.
<b>0x08, SYN_SLEEP_FAIL</b>  Attempt to put GIC to sleep failed as cores are not fully asleep	0xF	Core, bits[8:0]	All cores must be asleep, using the GICR_WAKER.ProcessorSleep handshake, before you flush the LPI cache using GICR_WAKER.Sleep.
<b>0x09, SYN_PGE_ON QUIESCE</b>  Core put to sleep before its Group enables were cleared.	0xF	Core, bits[8:0]	The core must disable its group enables before it toggles the GICR_WAKER.ProcessorSleep handshake, otherwise, the GIC clears its record of the group enables, causing a mismatch between the GIC and the core.
<b>0x0A, SYN_GICD_CTLR</b>  Attempt to update GICD_CTLR was prevented due to <i>Register Write Pending</i> (RWP) or Group enable restrictions.	0xF	Data, bits[7:0]	Software must wait for GICD_CTLR.RWP to be 0 before repeating the GICD_CTLR Write. The data represents the target value.
<b>0x10, SYN_SGI_NO_TGT</b>  SGI sent with no valid destinations.	0xE	Core, bits[8:0]	If the SGI is required, software must repeat the SGI from the reported core with a valid target list.  If this level of RAS functionality is required, the software must track generated SGIs externally.
<b>0x11, SYN_SGI_CORRUPTED</b>  SGI was corrupted and has not taken effect.	0x6	Core, bits[8:0]	An SGI is corrupted due to a RAM error in the PPI RAM. The RAM error details are reported separately in record 8. The GIC ignores the SGI generated from the recorded core. If you want software to recover from this, it must use an external record of the generated SGI.
<b>0x12, SYN_GICR_CORRUPTED</b>  Data was read from GICR register space that has encountered an uncorrectable error.	0x6	GITS_ERR0ADDR is populated	Software has tried to read corrupted data stored in SGI RAM or PPI RAM. Check records 4 and 8, and perform a recovery sequence for those interrupts.

**Table 3-8 Record 0 software errors (continued)**

<b>IERR</b>	<b>SERR</b>	<b>GICT_ERR&lt;n&gt;MISC0.Data</b>	<b>Recovery, Prevention</b>
<b>0x13, SYN_GICD_CORRUPTED</b> Data was read from GICD register space that has encountered an uncorrectable error.	0x6	GICT_ERR0ADDR is populated	Software has tried to read corrupted data stored in SPI RAM. Check record 2 and perform a recovery sequence for those interrupts.
<b>0x14, SYN_ITS_OFF</b> Data was read from an ITS that was powered down.	0xF	GITS_ERR0ADDR is populated	Ensure that the <b>qreqn_its&lt;x&gt;</b> power control Q-Channel is in the RUN state before accessing the relevant ITS.
<b>0x19, SYN_SPI_OOR</b> Access to a non-implemented SPI using (SET CLR)SPI.	0xE	ID, bits[9:0]	Reprogram the issuing device to send a supported SPI ID.
<b>0x1A, SYN_SPI_NO_DEST_TGT</b> A SPI has no legal target destinations.	0xF	ID, bits[9:0]	Before enabling the specified SPI, reprogram the SPI to target an existing core.
<b>0x1B, SYN_SPI_NO_DEST_1OFN</b> A 1 of N SPI cannot be delivered due to bad DPG/GICR_CLASS programming.	0xF	ID, bits[9:0]	Ensure that there is at least one valid target for the specified 1 of N interrupt, that is, ensure that at least one core has acceptable DPG and CLASSR settings to enable delivery.
<b>0x1C, SYN_COL_OOR</b> A collator message is received for a non-implemented SPI, or is larger than the number of owned SPIs in a multichip configuration.	0xF	ID, bits[9:0]	In a multichip configuration, ensure that there are enough owned SPIs to support all SPI wires that are used. Any unsupported interrupts must be disabled at the source.
<b>0x1D, SYN_DEACT_IN</b> A Deactivate to a non-existent SPI, or with incorrect groups set. Deactivates to LPI and non-existent PPI are not reported.	0xE	None	A Deactivate occurred to a non-existent SPI, or that SPI group prevented the Deactivate occurring. Software must check the active states of SPIs.
<b>0x1E, SYN_SPI_CHIP_OFFLINE</b> An attempt was made to send a SPI to an offline chip.	0xF	ID, bits[9:0]	Software must disable or retarget interrupts that are targeted at offline cores.
<b>0x20, SYN_PUP_REJ</b> A multichip power update was rejected.	0xF	None	Software must wait for a previous chip power transition to complete before attempting to start another one.
<b>0x28, SYN_ITS_REG_SET_OOR</b> An attempt was made to set an OOR interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16] Data, bits[15:0]	Software must reprogram the source device to only create legal LPI IDs.
<b>0x29, SYN_ITS_REG_CLR_OOR</b> An attempt was made to clear an OOR interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16] Data, bits[15:0]	Software must not attempt to clear non-existent LPIs.

**Table 3-8 Record 0 software errors (continued)**

<b>IERR</b>	<b>SERR</b>	<b>GICT_ERR&lt;n&gt;MISC0.Data</b>	<b>Recovery, Prevention</b>
<b>0x2A, SYN_ITS_REG_INV_OOR</b> An attempt was made to invalidate an OOR interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16] Data, bits[15:0]	Software must not attempt to clear non-existent LPIs.
<b>0x2B, SYN_ITS_REG_SET_ENB</b> An attempt was made to set an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16] Data, bits[15:0]	Software must follow architectural steps to enable LPIs on the specified core before enabling the core to send interrupts.
<b>0x2C, SYN_ITS_REG_CLR_ENB</b> An attempt was made to clear an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16] Data, bits[15:0]	Software must not try to clear LPIs on a core that does not have LPIs enabled using GICR_CTLR.Enable_LPIs.
<b>0x2D, SYN_ITS_REG_INV_ENB</b> An attempt was made to invalidate an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16] Data, bits[15:0]	Software must not try to invalidate LPIs on a core that does not have LPIs enabled using GICR_CTLR.Enable_LPIs.
<b>0x40, SYN_LPI_PROP_READ_FAIL</b> An attempt was made to read properties for a single interrupt, where an error response was received with the data.	0x12	Target, bits[31:16] ID, bits[15:0]	Software must reprogram the LPI Property table for the specified ID with error-free data and then issue an INV command through the ITS. If an overflow occurred, an INVAL command must be issued to all cores.
<b>0x41, SYN_PT_PROP_READ_FAIL</b> An attempt was made to read properties for a block of interrupts, where an error response was received with the data.	0x12	Target, bits[31:16] ID, bits[15:0]	Software must reprogram the LPI Property table for the specified ID with error-free data and then issue an INV command through the ITS. If an overflow occurred, an INVAL command must be issued to all cores.
<b>0x42, SYN_PT_COARSE_MAP_READ_FAIL</b> An attempt was made to read the coarse map for a target, where an error response was received with the data.	0x12	Target, bits[31:16]	No recovery is necessary because the GIC assumes that the coarse map is full. After a period, software tries to determine the reason for the error.
<b>0x43, SYN_PT_COARSE_MAP_WRITE_FAIL</b> An attempt was made to write the coarse map for a target, with an error received with the Write response.	0x12	Target, bits[31:16]	The GIC attempts to continue, however this error indicates issues with the memory system, and operation might be UNPREDICTABLE.
<b>0x44, SYN_PT_TABLE_READ_FAIL</b> An attempt was made to read a block of interrupts from a Pending table, where an error response was received with the data.	0x12	Target, bits[31:16] ID, bits[15:0]	Software must determine the reason for the pending error Read fail. The GIC uses the data supplied, however, it is possible for the LPI interrupt to be lost around the specified LPI.

**Table 3-8 Record 0 software errors (continued)**

IERR	SERR	GICT_ERR<n>MISC0.Data	Recovery, Prevention
<b>0x45, SYN_PT_TABLE_WRITE_FAIL</b>  An attempt was made to write back a block of interrupts from a Pending table, with an error received with the write response.	0x12	Target, bits[31:16]  ID, bits[15:0]	The GIC tries to continue, however, this error indicates issues with the memory system, and operation might be UNPREDICTABLE.
<b>0x46, SYN_PT_SUB_TABLE_READ_FAIL</b>  An attempt was made to read a sub-block of interrupts from a Pending table, where an error response was received with the data.	0x12	Target, bits[31:16]  ID, bits[15:0]	Software must determine the reason for the pending error read fail. The GIC uses the data supplied, however, it is possible for the LPI interrupt to be lost around the specified LPI.
<b>0x47, SYN_PT_TABLE_WRITE_FAIL_BYTE</b>  An attempt was made to write back a sub-block of interrupts from a Pending table, with an error received with the write response.	0x12	Target, bits[31:16]  ID, bits[15:0]	The GIC tries to continue, however, this error indicates issues with the memory system, and operation might be UNPREDICTABLE.

### SPI RAM error records 1-2

SPI RAM error record 1 records RAM ECC errors that are correctable. SPI RAM error record 2 records RAM ECC errors that are uncorrectable. Each error generates a SPI interrupt.

SPI RAM error records 1-2 are present if SPI RAM ECC is configured.

The GIC-600 has two SPI RAM, SPI0 and SPI1 that contain the programming for SPIs. SPI0 contains SPIs that have even-numbered IDs, and SPI1 contains SPIs that have odd-numbered IDs.

If a correctable error is detected in SPI RAM, it is corrected and the error is reported in error record 1. See [Error recovery and fault handling interrupts on page 3-65](#) for information about the error counters and interrupt generation options.

Correctable errors do not require software to take any action within the GIC. However, the GIC can choose to track error locations in case a RAM row or column can be repaired, if the RAM has repair capability.

The GICT\_ERR1MISC0 reports data for SPI error records 1-2 shown in the following table.

**Table 3-9 SPI RAM error reported data**

Record	GICT_ERR1MISC0.Data
1 = Correctable	Bit location, bits[log <sub>2</sub> (SPI)+]
2 = Uncorrectable	ID, bits[log <sub>2</sub> (SPI) - 1:0]

The RAM address can be determined from the ID >> 1. ID[0] specifies the SPI RAM number.

If a SPI has an uncorrectable error, GICD\_IERRRn identifies the SPI. While in this error state, the interrupt reverts to a disabled, secure group 0, edge-triggered SPI, and Non-secure access is controlled by GICD\_FCTLR.NSACR. This enables secure software to control whether Non-secure accesses can set the interrupt to pending while in the errored state.

For uncorrectable errors, software is required to perform the following recovery sequence:

1. Read the error record to determine if an uncorrectable error has occurred.
2. Clear the error record to enable future errors to be tracked.
3. Read all GICD\_IERRRn registers to identify SPIs that have errors. The GICR\_IERRRn registers must be read from the secure side.<sup>f</sup>

4. If required, read out any of the current programmed states. This includes programmed data that is corrupted and generates an error, unless GICT\_ERR0CTRL.UE is disabled. ARM recommends that intended programming is stored in memory so that this step is not required.
5. Write to GICD\_ICENABLERn to disable all interrupts that have errors.
6. Write 1 to GICD\_IERRRn to clear all interrupts that have errors and revert \_GROUP, \_GRPMOD, \_ICFG and \_NSACR to their default values.
7. Reprogram the interrupt to the intended settings.
8. If the interrupt is reprogrammed to be level-sensitive, write to GICD\_ICPENDRn to ensure that any level-sensitive pending bits are cleared.
9. If the interrupt is edge-triggered, ARM recommends that software checks the device, if possible, in case an edge is lost.
10. Ensure that the active bit is set correctly depending on whether it is being processed. Clear the active bit using GICD\_ICACTIVE to ensure that the interrupt is delivered when it is set to pending in the future. However, if the interrupt is being processed in a core, the interrupt might be delivered again before it is deactivated.
11. Re-enable the reprogrammed interrupts by writing to GICD\_ISENABLER.
12. Recheck the error record to ensure that no more errors are reported, if necessary, repeat step 2.

### SGI RAM error records 3-4

SGI RAM error record 3 records RAM ECC errors that are correctable. SGI RAM error record 4 records RAM ECC errors that are uncorrectable. Each error generates an SGI interrupt.

SGI RAM error records 3-4 are present if SGI RAM ECC is configured.

The Distributor records a subset of the SGI programming, and stores this information in the SGI RAM, to ensure that it can make the correct routing decisions for SGIs.

If a correctable error is detected in SGI RAM, the error is corrected and the error is reported in error record 3. See [Error recovery and fault handling interrupts on page 3-65](#) for information about the error counters and interrupt generation options.

Correctable errors do not require software to take an action within the GIC. However, the GIC can choose to track error locations in case it can repair a RAM row or column.

The GICT\_ERR<n>MISC0 reports data for SGI error records 3-4 shown in the following table.

**Table 3-10 SGI RAM error reported data**

Record	GICT_ERR<n>MISC0.Data
3 = Correctable	Bit location, $\log_2(\text{width})$ Address, bits[ceiling(core / 16) × 16+]
4 = Uncorrectable	Address, bits[ceiling(core / 16) × 16 - 1:0]

The RAM stores information for the same SGI for up to 16 cores on a single row.

GICR\_SGIDR contains default values for GRP, GRPMOD, and NSACR for each SGI.

When SGI programming that is in error, is taken from GICR\_SGIDR, the corrupted SGI number is given by address × 16 on cores (address - (address × 16)) to (address - (address × 16)) + 15.

For uncorrectable errors that occur in either the PPI or SGI RAM, software is required to perform the following recovery sequence:

1. Read the error record to determine if an uncorrectable error has occurred.
2. Clear the error record to enable future errors to be tracked.
3. Read all GICR\_IERRV registers to identify SGIs and PPIs that have errors. The GICR\_IERRV registers must be read from the secure side.

<sup>f</sup> If the error record reports only one error, the block that contains the error can be determined using the ID in the GICT\_ERR2MISC register, by calculating the block number as 1 + (ID / 32). However, in the case of an overflow, all GICD\_IERRRn registers must be checked.



4. If required, read out any of the current programmed states.<sup>g</sup> This includes programmed data that is corrupted and generates an error, unless GICT\_ERR0CTRL.UE is disabled. ARM recommends that intended programming is stored in memory so that this step is not required.
5. Write to GICR\_ICENABLER<sub>n</sub> to disable all interrupts that have errors.
6. Write 1 to the interrupts that have errors in the relevant GICR\_IERRV register to clear the interrupts that have errors and revert \_GROUP, \_GRPMOD, and \_NSACR to their default values. The values of PPIs are not changed.
7. Reprogram the interrupt to the intended settings.
8. Re-enable the reprogrammed interrupts by writing to the relevant GICR\_ISENABLER<sub>0</sub>.
9. Recheck the error record to ensure that no more errors are reported, if necessary, repeat step 2.

### PPI RAM error records 7-8

PPI RAM error record 7 records RAM ECC errors that are correctable. PPI RAM error record 8 records RAM ECC errors that are uncorrectable. Each error generates a PPI interrupt.

PPI RAM error records 7-8 are present if PPI RAM ECC is configured.

Error records 7-8 record the errors from PPI RAM that contain GRP, GRPMOD, and priority information for PPIs and SGIs. PPI RAM also contains a buffer that stores generated SGIs when backpressure occurs.

The GICT\_ERR<n>MISC0 reports data for PPI error records 7-8 shown in the following table.

**Table 3-11 PPI RAM error reported data**

Record	MISC0
7 = Correctable	PPI block, bits[18+] Bit location, bits[17:12] Offset, bits[11:8] SGI/Int, bit[7] Core, bits[6:0]
8 = Uncorrectable	PPI block, bits[12:+] Offset, bits[11:8] SGI/Int, bit[7] Core, bits[6:0]

### LPI RAM error records 9-10

LPI RAM error record 9 records RAM ECC errors that are correctable. LPI RAM error record 10 records RAM ECC errors that are uncorrectable. Each error generates an LPI interrupt.

LPI RAM error records 9-10 are present if LPI RAM ECC is configured.

Error records 9-10 record errors from the main LPI cache.

The GICT\_ERR<n>MISC0 reports data for LPI error records 9-10 shown in the following table.

<sup>g</sup> The GICR\_NSACR is overwritten when an error occurs, therefore, the pre-error value cannot be read back at this stage.

**Table 3-12 LPI RAM error reported data**

Record	MISC0
9 = Correctable	Bit location, bits[15+] Lock, bit[14] Pending <sup>h</sup> , bits[13:12] Channel <sup>i</sup> , bits[11:10] Address, bits[9:0]
10 = Uncorrectable	Lock <sup>j</sup> , bit[14] Pending, bits[13:12] Channel, bits[11:10] Address, bits[9:0]

When an uncorrectable error occurs, the data shown in the table is stored and the GICT\_ERR10MISC1 register is updated to contain the RAM contents of the corrupted line. The line in RAM is dropped, and any pending interrupts that it might contain are lost.

If required, software can use the data in the GICT\_ERR10MISC1 register to check several interrupt sources, such as the corrupted INTID. This ID is never more than two bits away from the recorded ID.

#### ITS RAM error records 11-12

ITS RAM error record 11 records ITS RAM ECC errors that are correctable. ITS RAM error record 12 records ITS RAM ECC errors that are uncorrectable.

ITS RAM error records 11-12 are present if an ITS is configured.

Error records 11-12 record the errors from ITS RAM.

All ITS tables are memory backed allowing uncorrectable errors to be read from RAM again without software intervention. These records are used for tracking RAM errors and for possible RAM maintenance.

The GICT\_ERR<n>MISC0 reports data for ITS RAM error records 11-12 shown in the following table.

**Table 3-13 ITS RAM error reported data**

Record	MISC0
11 = Correctable	Bit location, bit[8] Address, bit[12] RAM, bit[2] ITS, log <sub>2</sub> (ITS)
12 = Uncorrectable	Address, bit[12] RAM, bit[3] ITS, log <sub>2</sub> (ITS)

GICT\_ERR<n>MISC0 gives information relating to the corrupted ITS, RAM, and RAM address. The bit location of a correctable error is also given. The RAM encoding is shown in the following table.

<sup>h</sup> Pending bits[13:12] indicate if there were pending interrupts in the cache at the time of the corruption.  
<sup>i</sup> Channel bits[11:10] indicate the banked LPI cache and are always 0 for r0p0.  
<sup>j</sup> The Lock bit indicates if the error occurred on a locked line in the LPI cache, for more information, see [3.2.10 LPI caching on page 3-60](#).

**Table 3-14 RAM encoding**

RAM	Record 11	Record 12
0	None	None
1	Device cache	Device cache
2	Collection cache	Collection cache
3	Event cache	Event cache
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Event cache, locked

### ITS software error records 13+

ITS software error record 13+ records uncorrectable software errors in an ITS.

The ITS software error records 13+ record software errors from each configured ITS.

The ITS software records capture software events so that the operation of software can be tracked.

The ITS software records capture software errors that are only uncorrectable contained errors that require software to correct the command and to restart.

The GICT\_ERR<n>STATUS.IERR field indicates if an error is either related to the architecture (0) or is IMPLEMENTATION DEFINED (1). In both cases, the full 24-bit syndrome is reported in GICT\_ERR<n>MISC0. Extra data is reported in GICT\_ERR<n>MISC1.

The data captured for each ITS software syndrome is shown in the following table.

**Table 3-15 Captured data for each ITS software syndrome**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
MOVALL_TGT_OOR	0x010E20	1	0	-	MOVALL from a core that does not exist. Command is ignored.
MOVALL_DST_TGT_OOR	0x010E21	1	0	-	MOVALL to a core that does not exist. LPIs on MOVALL source are dropped.
MOVALL_DST_CHIP_OFFLINE_OOR	0x010E22	1	0	-	MOVALL to a chip that is offline. LPIs on MOVALL source are dropped.
MOVALL_ENABLE_LPI_OFF	0x010E23	1	0	-	MOVALL from a core where GICR_CTLR.Enable_LPIs is 0. Command is ignored.
MOVALL_DST_ENABLE_LPI_OFF	0x010E24	1	0	-	MOVALL from a core where GICR_CTLR.Enable_LPIs is 0. LPIs on MOVALL source are dropped.

**Table 3-15 Captured data for each ITS software syndrome (continued)**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
INT_PHYSICALID_OOR	0x010326	1	0	-	INT received with a physical ID that is beyond the range specified in GICR_PROPBASER.IDbits.  Software must correct mappings.  Interrupt is dropped.  ID is reported in GICT_ERR<n>MISC1.
INT_TGT_OOR	0x010320	1	0	-	INT received for a core that does not exist.  Software must correct mappings.  Interrupt is dropped and TGT is reported in GICT_ERR<n>MISC1.
INT_CHIP_OFFLINE_OOR	0x010322	1	0	-	INT received for a chip that is offline.  Software must either correct mappings or take chip online.  Interrupt is dropped and TGT is reported in GICT_ERR<n>MISC1.
INT_LPI_OFF	0x010323	1	0	-	INT received for TGT with GICR_CTLR.Enable_LPis disabled.  Software must either enable LPI or correct mappings.  TGT is reported in GICT_ERR<n>MISC1.
LOCK_PHYSICALID_OOR	0x010F26	1	0	-	An attempt was made to lock a cache entry for a physical ID that is not supported.  Fail is reported in GITS_OPR. <sup>k</sup>
LOCK_TGT_OOR	0x010F20	1	0	-	An attempt was made to lock a cache entry for a core that does not exist.  Fail is reported in GITS_OPR. <sup>k</sup>
LOCK_LPI_OFF	0x010F23	1	0	-	An attempt was made to lock a cache entry for a core with GICR_CTLR.Enable_LPis set to 0.  Fail is reported in GITS_OPR. <sup>k</sup>
MAPD_DEVICE_OOR	0x010801	0	1	CEE	A MAPD command has tried to map a device with a DeviceID that is outside the range supported, or that is beyond the memory allocated.
MAPD_ITTSIZE_OOR	0x010802	0	1	CEE	A command has tried to allocate an ITT table that is larger than the supported EventID size.
MAPC_COLLECTION_OOR	0x010903	0	1	CEE	A MAPC command has tried to map a CollectionID that is not supported. <sup>l</sup>

<sup>k</sup> See ITS cache control, locking, and test on page 3-58.

<sup>l</sup> See 4.6.2 Interrupt Controller Type Register; GITS\_TYPER on page 4-115.

Table 3-15 Captured data for each ITS software syndrome (continued)

Error mnemonic	Encoding	IERR	Stall	Mask	Description
MAPC_TGT_OOR	0x010920	1	1/0	CEE	<p>A MAPC command has tried to map to a core that does not exist.</p> <p>If the core is within the maximum range supported by the ITS, the command stalls.</p> <p>If the command is detected in the destination Distributor, the command is ignored and the core is reported in GICT_ERR&lt;n&gt;MISC1.</p> <p>————— <b>Note</b> —————</p> <p>If the value in GICT_ERR&lt;n&gt;MISC1 is 0, the location of the detected error is in the ITS.</p> <p>—————</p> <p>CEE applies to errors detected in the ITS only.</p>
MAPC_LPI_OFF	0x010923	1	0	-	<p>A MAPC command has tried to map a collection to a core that does not have LPIs enabled.</p> <p>Software must correct the mapping, or it must first enable LPIs using GICR_CTLR.Enable_LPIs.</p> <p>The core is reported in GICT_ERR&lt;n&gt;MISC1.</p>
MAPC_CHIP_OFFLINE_OOR	0x010922	1	0	-	<p>A MAPC command has targeted a core in an offline chip.</p> <p>Software must correct the mapping or take the target chip online.</p>
MAPI_DEVICE_OOR	0x010B01	0	1	CEE	<p>A MAPI has tried to map a DeviceID that is not supported.</p> <p>See <i>GITS_BASER0</i> in <sup>m</sup>, and for information about the range that is supported, <sup>1</sup>.</p>
MAPI_COLLECTION_OOR	0x010B03	0	1	CEE	<p>A MAPI has tried to map to a collection that is not supported.</p> <p>See <i>GITS_BASER1</i> in <sup>m</sup> and for information about the range that is supported, <sup>1</sup>.</p>
MAPI_ID_OOR	0x010B05	0	1	CEE	<p>A MAPI has tried to map to an EventID size that is not supported.</p> <p>The size that is supported is reported in <i>GITS_TYPER</i>, but might be reduced depending on the MAPD command for the specified DeviceID.</p>
MAPI_UNMAPPED_DEVICE	0x010B04	0	1	CEE	<p>A MAPI has tried to map an interrupt to a device that is not mapped.</p>
MAPVI_DEVICE_OOR	0x010A01	0	1	CEE	<p>A MAPVI has tried to map a device supported by the ITS that is out-of-range.</p> <p>See <i>GITS_BASER0</i> in <sup>m</sup>, and for information about the range that is supported, <sup>1</sup>.</p>

<sup>m</sup> ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0.

**Table 3-15 Captured data for each ITS software syndrome (continued)**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
MAPVI_COLLECTION_OOR	0x010A03	0	1	CEE	A MAPVI has tried to map to a collection that is outside the range supported by the ITS.  See <i>GITS_BASER1</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
MAPVI_UNMAPPED_DEVICE	0x010A04	0	1	CEE	A MAPVI has tried to map an interrupt to a device that is not mapped.
MAPVI_ID_OOR	0x010A05	0	1	CEE	A MAPVI has tried to use an EventID that is outside the size supported by the corresponding MAPD command.
MAPVI_PHYSICALID_OOR	0x010A06	0	1	CEE	A MAPVI is received that has a physical ID outside the range supported.  The supported range is >16-<8096 bits.
MOVI_DEVICE_OOR	0x010101	0	1	CEE	A MAPVI has tried to map a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
MOVI_COLLECTION_OOR	0x010103	0	1	CEE	A MOVI has tried to use a collection that is outside the range supported by the ITS.  See <i>GITS_BASER1</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
MOVI_UNMAPPED_DEVICE	0x010104	0	1	CEE	A MOVI has tried to move an interrupt from a device that is not mapped.
MOVI_ID_OOR	0x010105	0	1	CEE	A MOVI has tried to use an EventID that is outside the size supported by the corresponding MAPD command.
MOVI_UNMAPPED_INTERRUPT	0x010107	0	1	CEE	A MOVI command has tried to operate on an interrupt that is not mapped.
MOVI_UNMAPPED_COLLECTION	0x010109	0	1	CEE	A MOVI command has tried to operate on a collection that is not mapped.
DISCARD_DEVICE_OOR	0x010F01	0	1	CEE	A DISCARD has tried to use a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
DISCARD_UNMAPPED_DEVICE	0x010F04	0	1	CEE	A DISCARD has tried to drop an interrupt from a device that is not mapped.
DISCARD_ID_OOR	0x010F05	0	1	CEE	A DISCARD command has tried to use an EventID that is outside the size supported by the corresponding MAPD command.
DISCARD_UNMAPPED_INTERRUPT	0x010F07	0	1	CEE	A MOVI command has tried to operate on an interrupt that is not mapped.
DISCARD_ITE_INVALID	0x010F10	0	1	CEE	A MOVI command has tried to operate on an EventID that is not supported by the corresponding MAPD command.

**Table 3-15 Captured data for each ITS software syndrome (continued)**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
INV_DEVICE_OOR	0x010C01	0	1	CEE	An INV has tried to use a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
INV_UNMAPPED_DEVICE	0x010C04	0	1	CEE	An INV has tried to invalidate an interrupt from a device that is not mapped.
INV_ID_OOR	0x010C05	0	1	CEE	An INV has tried to use an EventID that is outside the size supported by the corresponding MAPD command.
INV_UNMAPPED_INTERRUPT	0x010C07	0	1	CEE	An INV has tried to invalidate an interrupt that is not mapped.
INV_ITE_INVALID	0x010C10	0	1	CEE	An INV has tried to invalidate an interrupt with an EventID that is invalid.
INV_PHYSICALID_OOR	0x010C26	1	1	CEE	An INV has tried to invalidate an interrupt with a physical ID that is larger than that supported by the target.  See <i>GICR_PROPBASER.IDbits</i> in <sup>m</sup> .
INV_TGT_OOR	0x010C20	1	1	CEE	An INV has tried to invalidate an interrupt that is mapped to an invalid target.
INV_LPI_OFF	0x010C23	1	1	CEE	An INV has tried to invalidate an interrupt that is mapped to a target that does not have LPis enabled.  See <i>GICR_CTLR.Enable_LPis</i> in <sup>m</sup> .
INV_CHIP_OFFLINE_OOR	0x010C22	1	1	CEE	An INV has tried to invalidate an interrupt that is mapped to a chip that is offline.
INVALL_COLLECTION_OOR	0x010D03	0	1	CEE	An INVALL has tried to invalidate an OOR collection. <sup>1</sup>
INVALL_UNMAPPED_COLLECTION	0x010D09	0	1	CEE	An INVALL has tried to invalidate a collection that is not mapped.
INVALL_TGT_OOR	0x010D20	1	1	CEE	An INVALL has been sent to an illegal target.
INVALL_LPI_OFF	0x010D23	1	1	CEE	An INVALL has been sent to a target that has LPis turned off.
INVALL_CHIP_OFFLINE_OOR	0x010D22	1	1	CEE	An INVALL has tried to invalidate an interrupt from a device that is not mapped.
INT_DEVICE_OOR	0x010301	0	1	UEE	An incoming translation has attempted to use a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>1</sup> .
INT_UNMAPPED_DEVICE	0x010304	0	1	UEE	An incoming translation has tried to invalidate an interrupt from a device that is not mapped.
INT_ID_OOR	0x010305	0	1	UEE	An INT has tried to use an EventID that is outside the size supported by the corresponding MAPD command.

**Table 3-15 Captured data for each ITS software syndrome (continued)**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
INT_UNMAPPED_INTERRUPT	0x010307	0	1	UEE	An INT command has tried to raise an interrupt that is not mapped.
INT_ITE_INVALID	0x010310	0	1	UEE	An INT command has tried to raise an interrupt with an EventID that is not supported by the corresponding MAPD command.
CLEAR_DEVICE_OOR	0x010501	0	1	CEE	A CLEAR has attempted to use a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>l</sup> .
CLEAR_UNMAPPED_DEVICE	0x010504	0	1	CEE	A CLEAR has tried to drop an interrupt from a device that is not mapped.
CLEAR_ID_OOR	0x010505	0	1	CEE	A CLEAR has tried to drop an interrupt from an EventID that is not supported by the corresponding MAPD command.
CLEAR_UNMAPPED_INTERRUPT	0x010507	0	1	CEE	A CLEAR has attempted to drop an interrupt that is not mapped.
CLEAR_ITE_INVALID	0x010510	0	1	CEE	A CLEAR has tried to drop an interrupt from an EventID that is not supported by the corresponding MAPD command.
CLEAR_PHYSICALID_OOR	0x010526	1	1	CEE	A CLEAR has tried to drop an interrupt, which has a physical ID that is not supported by the target.
CLEAR_TGT_OOR	0x010520	1	1	CEE	A CLEAR has been sent to an illegal target.
CLEAR_LPI_OFF	0x010523	1	1	CEE	A CLEAR has been sent to a target that does not have LPis enabled.
CLEAR_CHIP_OFFLINE_OOR	0x010522	1	1	CEE	A CLEAR has been sent to a target on a chip that is offline.
OPR_DEVICE_OOR	0x010A01	1	-	-	Software has tried an operation through GITS_OPR using a device that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>l</sup> .
OPR_UNMAPPED_COLLECTION	0x010A03	1	-	-	Software has tried an operation through GITS_OPR using a collection that is outside the range supported by the ITS.  See <i>GITS_BASER0</i> in <sup>m</sup> , and for information about the range that is supported, <sup>l</sup> .
OPR_ID_OOR	0x010A05	1	-	-	Software has tried to lock an interrupt using an EventID that is larger than that supported by the specified device.  The GITS_OPSR reports a fail.



**Table 3-15 Captured data for each ITS software syndrome (continued)**

Error mnemonic	Encoding	IERR	Stall	Mask	Description
OPR_UNMAPPED_DEVICE	0x010A04	1	-	-	Software has tried to lock an interrupt from a device that is not mapped through GITS_OPR. The GITS_OPR reports a fail.
OPR_UNMAPPED_INTERRUPT	0x010A07	1	-	-	Software has tried to lock an interrupt that is not mapped through GITS_OPR. The GITS_OPSR reports a fail.
OPR_SET_LOCKED	0x010A10	1	-	-	Software has tried to lock an interrupt into the LPI cache but the set already contains a locked interrupt. The GITS_OPSR reports a fail.
INVALID_ML_DEV_TABLE_ENTRY	0x010B04	1	1	CEE	Software is using a two-level Device table and the first-level table entry has not completed. Software must allocate and clear a new second-level table, update the first-level entry, and repeat the command.
ACE_LITE_ACCESS_FAILURE	0x010B01	1	-	-	An access issued by the ITS received an <i>SLVERR</i> or <i>DECODE</i> error. The address is given in GICT_ERR<n>MISC1. This error can occur from multiple sources. Software must determine whether the Command queue is stalled by checking GITS_OPR. If the Command queue has stalled, the command might not have occurred.
ACE_LITE_TRANS_FAILURE	0x010B03	1	-	AEE	An unknown source in the system has written to the slave port with an access that is not a legal GITS_TRANSLATER access. The full address of the access is given in GICT_ERR<n>MISC1. If the address matches GITS_TRANSLATER, either the size, length, strobes, or access type is wrong. <b>Note</b> Read accesses are not tracked.
ACE_LITE_ADDR_OOR	0x010B05	1	-	-	ITS programming has tried to create an access to the address specified in GICT_ERR<n>MISC1 that is larger than the address space supported.
INVALID_COMMAND	0x010F00	1	-	CEE	An Invalid command has been detected in the Command queue. Software must correct this and then resume.

### Clearing error records

After reading a GICT\_ERR<n>\_STATUS register, software must clear the valid register bits so that any new errors are recorded.

During this period, a new error might overwrite the syndrome for the error read previously. If the register is Read or Write, the previous error is lost.

To prevent this, most bits use a modified version of write-1-to-clear:

- Writes to the bits of ERR<n>STATUS.UE (uncorrectable error records) or ERR<n>STATUS.CE (correctable error records) are ignored if ERR<n>STATUS.OF is set and is not being cleared.
- Writes to other fields in the ERR<n>STATUS register are ignored if either bits ERR<n>STATUS.UE or ERR<n>STATUS.CE are set and are not being cleared.

Similarly, ERR<n>MISC<x> cannot be Written, except the counter fields, if the corresponding ERR<n>STATUS.MV bit is set, and ERR<n>ADDR cannot be Written if ERR<n>STATUS.AV is set.

Recommended recovery sequences are described for each error record in [Software error record 0 on page 3-66](#) to [ITS software error records 13+ on page 3-75](#).

## Bus errors

ACE-Lite bus error syndromes such as bad transactions, and corrupted RAM data reads can be made to enable *SLVERR*.

The GICT\_ERR0CTLR.UE bit can be used to enable ACE-Lite bus error, *External AXI Slave Error (SLVERR)* for the syndromes shown in the following table.

**Table 3-16 Bus error syndromes**

Syndrome	Description	Direction
SYN_ACE_BAD	ACE-Lite transactions are either bad or unrecognized	Read and Write
SYN_GICR_CORRUPTED	Data read from SPI RAM is corrupted	Read only
SYN_GICD_CORRUPTED	Data read from SGI or PPI RAM is corrupted	Read only
SYN_ITS_OFF	Access to ITS attempted when powered down	Read and Write

# Chapter 4

## Programmers model

Read this for a description of the memory map and registers, and for information about programming the device.

It contains the following sections:

- [4.1 The GIC-600 registers on page 4-84.](#)
- [4.2 Distributor registers \(GICD/GICDA\) summary on page 4-86.](#)
- [4.3 Distributor registers \(GICA\) for message-based SPIs summary on page 4-97.](#)
- [4.4 Redistributor registers for control and physical LPIs summary on page 4-98.](#)
- [4.5 Redistributor registers for SGIs and PPIs summary on page 4-107.](#)
- [4.6 ITS control register summary on page 4-113.](#)
- [4.7 ITS translation register summary on page 4-122.](#)
- [4.8 GICT register summary on page 4-123.](#)
- [4.9 GICP register summary on page 4-138.](#)

## 4.1 The GIC-600 registers

All the GIC-600 registers have names constructed of mnemonics that indicate the logical block that the register belongs to and the register function.

The following information applies to the GIC-600 registers:

- The GIC-600 implements only memory-mapped registers.
- The GIC-600 has a single base address, except for the GITS\_TRANSLATER register. The base address is not fixed and can be different for each particular system implementation.
- The offset of each register from the base address is fixed.
- Accesses to reserved or unused address locations might result in a bus error that is based on GICT\_ERR0CTRL.UE.
- Unless otherwise stated in the accompanying text:
  - Do not modify reserved register bits.
  - Ignore reserved register bits on reads.
  - A system reset or a powerup reset resets all register bits to zero.
- The GIC-600 ACE-Lite slave port can be 64 bits, 128 bits, or 256 bits wide, depending on the configuration. The *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0* defines the permitted sizes of access.

### ————— Note —————

The GIC-600 guarantees single-copy atomicity for doubleword accesses.

- The GIC-600 supports data only in little-endian format.
- The access types for the GIC-600 are as follows:

**RO**      Read only.  
**RW**      Read and write.  
**WO**      Write only, reads return as UNKNOWN.

This section contains the following subsections:

- [4.1.1 Register map pages on page 4-84.](#)
- [4.1.2 Discovery on page 4-85.](#)
- [4.1.3 GIC-600 register access and banking on page 4-85.](#)

### 4.1.1 Register map pages

The register map is separated into several pages.

The register map pages are defined in the following table.

**Table 4-1 Register map pages**

Offset[x:16]	Page	Description
0	GICD	GICD main page
1	GICA	GICD message-based interrupts alias
2	GICT	GIC trace and debug page
3	GICP	GIC PMU
4 + (ITSnum x 2)	GITSn	ITS address page
5 + (ITSnum x 2)	GITSn translate	ITS translation page
4 + (2 x ITSnum) + (RDnum x 2)	GICR (LPI)	GICR LPI registers
5 + (2 x ITSnum) + (RDnum x 2)	GICR (SGI)	GICR SPI + SGI registers
4 + (2 x ITSnum) + (RDnum x 2)	GICDA	Alias to GICD (page after last GICR page)

## Related information

*ARM® Generic Interrupt Controller Architecture Specification, version 3.0 and version 4.0.*

### 4.1.2 Discovery

ARM recommends that the operating system is provided with pointers to the start of the Distributor, every ITS, and the first Redistributor page on each chip.

To verify that the pages are of GIC registers, these pointers can be checked against the discovery registers, which start at offset 0xFFD0 for each GIC page. These registers allow discovery of the architecture version and, for GIC-600, whether the page contains the Distributor, ITS, or Redistributor registers. When this information is known, additional information can be obtained from registers specific to each page.

For Redistributors, ARM recommends that you examine GICR\_TYPER to determine:

- Whether the implementation has two or four pages per Redistributor that are based on the features implemented. It can be inferred that GIC-600 has only two pages for each Redistributor because the feature bits in that register indicate that it does not support virtual LPIs.
- Whether it is the last Redistributor in the series of pages.
- Which core the Redistributor is for, based on affinity values.

This information allows you to iteratively search through all Redistributors in a discovery process.

The GITS\_TYPER register in the GIC-600 indicates that you must program the ITS with unique ProcessorNumbers, instead of physical target addresses. The GICR\_TYPER contains the unique ProcessorNumber that you must use to reference a Redistributor when programming the ITS.

#### Note

In a multichip configuration, the ProcessorNumber upper bits are derived from the **chip\_id** tie-off. Therefore, make sure that the **chip\_id** value is defined before the registers are read.

## Related information

*ARM® GICv3 and GICv4 Software Overview.*

### 4.1.3 GIC-600 register access and banking

The GIC-600 uses an access and banking scheme for its registers.

#### Note

For information about the register access and banking scheme, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

The key characteristics of the scheme are:

- Some registers, such as the *Distributor Control Register*, GICD\_CTLR, and the *Redistributor Control Register*, GICR\_CTLR, are banked by security that provides separate Secure and Non-secure copies of the registers. A Secure access to the address accesses the Secure copy of the register. A Non-secure access to the address accesses the Non-secure copy.
- Some registers, such as the *Interrupt Group Registers*, GICD\_IGROUPRn, are only accessible using Secure accesses.
- Non-secure accesses to registers, or parts of a register, which are only accessible to Secure accesses are *Read-As-Zero* and *Writes Ignored* (RAZ/WI).

## Related information

*ARM® Generic Interrupt Controller Architecture Specification, version 3.0 and version 4.0.*

## 4.2 Distributor registers (GICD/GICDA) summary

The GIC-600 Distributor functions are controlled through the Distributor registers identified with the prefix GICD. The Distributor Alias registers are identified with the prefix GICDA.

The following table lists the Distributor registers in base offset order and provides a reference to the register description that is described in either this book or the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

Address offsets are relative to the Distributor base address defined by the system memory map.

Offsets that are not shown are Reserved and RAZ/WI.

**Table 4-2 Distributor registers (GICD/GICDA) summary**

Offset	Name	Type	Width	Reset	Description
0x0000	GICD_CTLR	RW	32	0x00000000 <sup>n</sup>	Distributor Control Register
0x0004	GICD_TYPER	RO	32	Configuration dependent	<a href="#">4.2.1 Interrupt Controller Type Register, GICD_TYPER</a> on page 4-88
0x0008	GICD_IIDR	RO	32	Configuration dependent	<a href="#">4.2.2 Distributor Implementer Identification Register, GICD_IIDR</a> on page 4-89
0x000C-0x001C	-	-	-	-	Reserved
0x0020	GICD_FCTLR	RW	32	0x00000000	<a href="#">4.2.3 Function Control Register, GICD_FCTLR</a> on page 4-90
0x0024	GICD_SAC	RW	32	0x00000000 <sup>o</sup>	<a href="#">4.2.4 Secure Access Control Register, GICD_SAC</a> on page 4-92
0x0028-0x003C	-	-	-	-	Reserved
0x0040	GICD_SETSPI_NSR	WO	32	-	Non-secure SPI Set Register
0x0044	-	-	-	-	Reserved
0x0048	GICD_CLRSPI_NSR	WO	32	-	Non-secure SPI Clear Register
0x004C	-	-	-	-	Reserved
0x0050	GICD_SETSPI_SR <sup>p</sup>	WO	32	-	Secure SPI Set Register <sup>q</sup>
0x0054	-	-	-	-	Reserved
0x0058	GICD_CLRSPI_SR <sup>p</sup>	WO	32	-	Secure SPI Clear Register <sup>q</sup>
0x005C-0x007C	-	-	-	-	Reserved
0x0080-0x00FC	GICD_IGROUPRn	RW	32	0x00000000	Interrupt Group Registers <sup>q</sup>
0x0184-0x01F8	-	-	-	-	Reserved
0x0200-0x027C	GICD_ISPENDRn <sup>r</sup>	RW	32	0x00000000	Interrupt Set-Pending Registers
0x0280-0x02FC	GICD_ICPENDRn <sup>r</sup>	RW	32	0x00000000	Interrupt Clear-Pending Registers
0x0300-0x037C	GICD_ISACTIVERn <sup>r</sup>	RW	32	0x00000000	Interrupt Set-Active Registers
0x0380-0x03FC	GICD_ICACTIVERn <sup>r</sup>	RW	32	0x00000000	Interrupt Clear-Active Registers

<sup>n</sup> The reset value is 0x00000040 if the GIC is configured to support a single security state only.

<sup>o</sup> The reset values of GICD\_SAC.GICTNS and GICD\_SAC.GICPNS are controlled by the **gicp\_allow\_ns** and **gicd\_allow\_ns** tie-off signals respectively.

<sup>p</sup> The existence of this register depends on the configuration of the GIC-600. If Security support is not included, then this register does not exist.

<sup>q</sup> This register is only accessible from a Secure access.

<sup>r</sup> The first one of these registers does not exist.

Table 4-2 Distributor registers (GICD/GICDA) summary (continued)

Offset	Name	Type	Width	Reset	Description
0x0400-0x07F8	GICD_IPRIORITYRn <sup>s</sup>	RW	32	0x00000000	Interrupt Priority Registers
0x0800-0x0BF8	GICD_ITARGETSRn <sup>t</sup>	RW	32	0x00000000	Interrupt Processor Targets Registers
0x0D00-0x0D7C	GICD_IGRPMODRn <sup>u</sup>	RW	32	0x00000000	Interrupt Group Modifier Registers
0x0E00-0x0EFC	GICD_NSACRn <sup>p</sup>	RW	32	0x00000000	Non-secure Access Control Registers
0x0F20-0x0F2C	GICD_SPENDSGIRn <sup>v</sup>	RW	32	0x00000000	SGI Set-Pending Registers
0x0F30-0x5FFC	-	-	-	-	Reserved
0x6000-0x7FD8	GICD_IROUTERn	RW	64	0x0000000080000000	Interrupt Routing Registers See <i>ARM® GICv3 and GICv4 Software Overview</i> .  <div style="border: 1px solid black; padding: 5px; margin: 5px 0;"> <p style="text-align: center;"><b>Note</b></p> <p>The reset value of all GICD_IROUTERn registers is determined by Interrupt_Routing_Mode == 1.</p> </div>
0x7FDC-0xBFFC	-	-	-	-	Reserved
0xC088-0xDFFC	-	-	-	-	Reserved
0xE000-0xE0FC	GICD_ICLARn	RW	32	0x00000000	<a href="#">4.2.5 Interrupt Class Registers, GICD_ICLARn</a> on page 4-92
0xE100-0xE17C	GICD_IERRRn	RW	32	0x00000000	<a href="#">4.2.6 Interrupt Error Registers, GICD_IERRRn</a> on page 4-93
0xE180-0xEFFC	-	-	-	-	Reserved
0xF000	GICD_CFGID	RO	64	Configuration dependent	<a href="#">4.2.7 Configuration ID Register, GICD_CFGID</a> on page 4-94
0xF008-0xFFCC	-	-	-	-	Reserved
0xFFD0	GICD_PIDR4	RO	32	0x00000044	Peripheral ID 4 Register
0xFFD4	GICD_PIDR5	RO	32	0x00000000	Peripheral ID 5 Register
0xFFD8	GICD_PIDR6	RO	32	0x00000000	Peripheral ID 6 Register
0xFFDC	GICD_PIDR7	RO	32	0x00000000	Peripheral ID 7 Register
0xFFE0	GICD_PIDR0	RO	32	0x00000092	Peripheral ID 0 Register
0xFFE4	GICD_PIDR1	RO	32	0x000000B4	Peripheral ID 1 Register
0xFFF8	GICD_PIDR2	RO	32	0x0000003B	<a href="#">4.2.8 Peripheral ID2 register, GICD_PIDR2</a> on page 4-95
0xFFEC	GICD_PIDR3	RO	32	0x00000000	Peripheral ID 3 Register
0xFFFF0	GICD_CIDR0	RO	32	0x0000000D	Component ID 0 Register
0xFFFF4	GICD_CIDR1	RO	32	0x000000F0	Component ID 1 Register

<sup>s</sup> The first eight of these registers do not exist.  
<sup>t</sup> When ARE is set, this register is replaced by GICD\_IROUTERn.  
<sup>u</sup> When ARE = 0, these bits are RES0.  
<sup>v</sup> When ARE is set, this register is replaced by GICR\_ISPENDR0.

**Table 4-2 Distributor registers (GICD/GICDA) summary (continued)**

Offset	Name	Type	Width	Reset	Description
0xFFF8	GICD_CIDR2	RO	32	0x00000005	Component ID 2 Register
0xFFFC	GICD_CIDR3	RO	32	0x000000B1	Component ID 3 Register

This section contains the following subsections:

- [4.2.1 Interrupt Controller Type Register; GICD\\_TYPER](#) on page 4-88.
- [4.2.2 Distributor Implementer Identification Register; GICD\\_IIDR](#) on page 4-89.
- [4.2.3 Function Control Register; GICD\\_FCTLR](#) on page 4-90.
- [4.2.4 Secure Access Control Register; GICD\\_SAC](#) on page 4-92.
- [4.2.5 Interrupt Class Registers; GICD\\_ICLARn](#) on page 4-92.
- [4.2.6 Interrupt Error Registers; GICD\\_IERRRn](#) on page 4-93.
- [4.2.7 Configuration ID Register; GICD\\_CFGID](#) on page 4-94.
- [4.2.8 Peripheral ID2 register; GICD\\_PIDR2](#) on page 4-95.

#### 4.2.1 Interrupt Controller Type Register, GICD\_TYPER

This register returns information about the configuration of the GIC-600. You can use this register to determine the number of security states, the number of INTIDs, and the number of processor cores that the GIC supports.

The GICD\_TYPER characteristics are:

##### Usage constraints

There are no usage constraints.

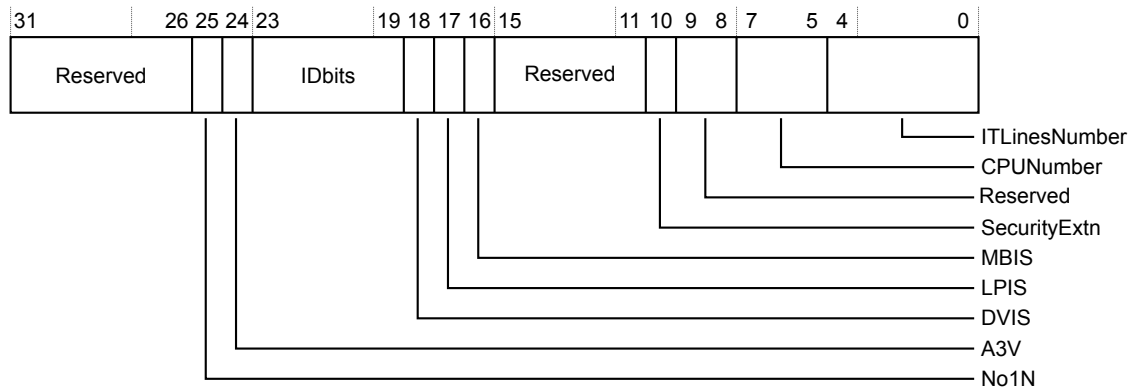
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.



**Figure 4-1 GICD\_TYPER bit assignments**

The following table shows the bit assignments.

**Table 4-3 GICD\_TYPER bit assignments**

Bits	Name	Function
[31:26]	-	Reserved, returns 0b000000.
[25]	No1N	1 of N SPI: 0 = The GIC-600 supports 1 of N SPI interrupts.



**Table 4-3 GICD\_TYPER bit assignments (continued)**

Bits	Name	Function
[24]	A3V	Affinity level 3 values. Depending on the configuration, returns either: 0 = The GIC-600 Distributor only supports zero values of Affinity level 3. 1 = The GIC-600 Distributor supports nonzero values of Affinity level 3.
[23:19]	IDbits	Interrupt identifier bits: 0b01111 = The GIC-600 supports 16 interrupt identifier bits.
[18]	DVIS	Direct Virtual LPI injection support: 0 = The GIC-600 does not support Direct Virtual LPI injection. See <i>ARM® GICv3 and GICv4 Software Overview</i> .
[17]	LPIS	Locked SPI support: 0 = Locked SPIs are not supported.
[16]	MBIS	Message-based interrupt support: 1 = The GIC-600 supports message-based interrupts.
[15:11]	-	Reserved, returns 0b00000.
[10]	SecurityExtn	Security state support. Depending on the configuration, returns either: 0 = The GIC-600 supports only a single Security state. 1 = The GIC-600 supports two Security states. When GICD_CTLR.DS == 1, this field is RAZ.
[9:8]	-	Reserved, returns 0b00.
[7:5]	CPUNumber	Number of cores in system minus one. Returns the number of cores in the system, saturated to eight, minus one. The permitted values for this field are 0-8. If GICD_CTLR.ARE_S or GICD_CTLR.ARE_NS = 0, modes are not supported and this field reads as 0.
[4:0]	ITLinesNumber	Number of SPIs divided by 32. Returns the number of SPIs divided by 32. The permitted values for this field are 0-30 (992 SPIs maximum).

#### 4.2.2 Distributor Implementer Identification Register, GICD\_IIDR

This register provides information about the implementer and revision of the Distributor.

The GICD\_IIDR characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.

31	24	23	20	19	16	15	12	11	0
ProductID				Reserved	Variant		Revision		Implementer

Figure 4-2 GICD\_IIDR bit assignments

The following table shows the bit assignments.

Table 4-4 GICD\_IID bit assignments

Bits	Name	Function
[31:24]	ProductID	Indicates the product ID: $0x02 = \text{GIC-600}$ .
[23:20]	-	Reserved, RAZ.
[19:16]	Variant	Indicates the major revision or variant of the product for the <i>rmprn</i> identifier: $0x0 = r0$ .
[15:12]	Revision	Indicates the minor revision of the product for the <i>rmprn</i> identifier: $0x1 = p0$ . $0x3 = p1$ . $0x4 = p2$ .
[11:0]	Implementer	Identifies the implementer: $0x43B = \text{ARM}$ .

### 4.2.3 Function Control Register, GICD\_FCTLR

This register controls the scrubbing of all RAMs in the local Distributor. The register is not distributed and only acts on the local chip.

The GICD\_FCTLR characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary on page 4-86](#).

The following figure shows the bit assignments.

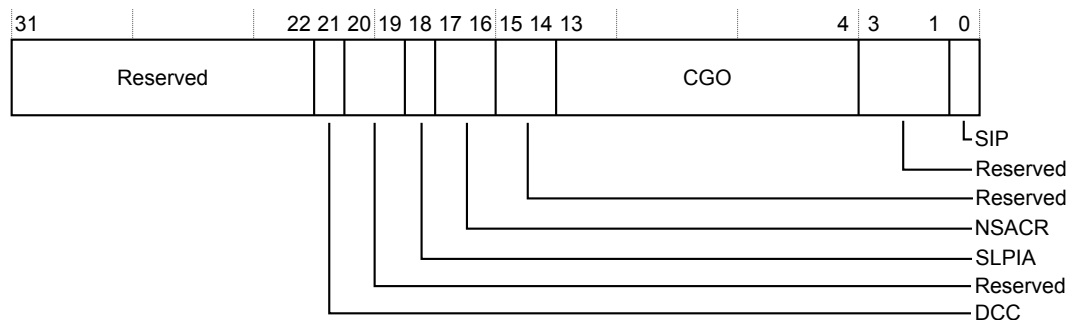


Figure 4-3 GICD\_FCTLR bit assignments

The following table shows the bit assignments.

**Table 4-5 GICD\_FCTLR bit assignments**

Bits	Name	Function
[31:22]	-	Reserved, returns 0b000000.
[21]	DCC	<i>Disable Cache Conversion</i> (DCC). Disable cache conversion on memory accesses.
[20:19]	-	Reserved, returns 0b000000.
[18]	SLPIA	<i>Strict LPI Allocation</i> (SLPIA). Controls whether LPI reverts to a fixed index behavior. This bit can only be written when in full sleep (quiescent). RES0. Resets to 0b0.
[17:16]	NSACR	Non-secure Access Control. Values are as described in the GICD_NSACR register. This is the value that is used if a SPI has an error. Secure access only. Resets to 0b00.
[15:14]	-	Reserved, returns 0b00.
[13:4]	CGO	One bit per clock gate: 1 = Leave clock running. 0 = Use full clock gating. Clock gate bit assignments are specified in <a href="#">Table 4-6 CGO field bit assignments</a> on page 4-91.
[3:1]	-	Reserved, returns 0b000.
[0]	SIP	Scrub in progress: 1 = Scrub in progress. 0 = No scrub in progress. This bit is read and written by software. When a scrub is complete, the GIC clears the bit to 0.

**Table 4-6 CGO field bit assignments**

Value	Clock gate
0x0	CPU communications block
0x1	SPI registers and search
0x2	ACE-Lite slave interface
0x3	ACE-Lite master interface
0x4	LPI cache and search
0x5	SGI and GICR registers
0x6	Trace & debug
0x7	Pending table search and control
0x8	ITS communications block

#### 4.2.4 Secure Access Control Register, GICD\_SAC

This register allows Secure software to control Non-secure access to GIC-600 Secure features by other software.

The GICD\_SAC characteristics are:

**Usage constraints**

Only accessible by Secure accesses.

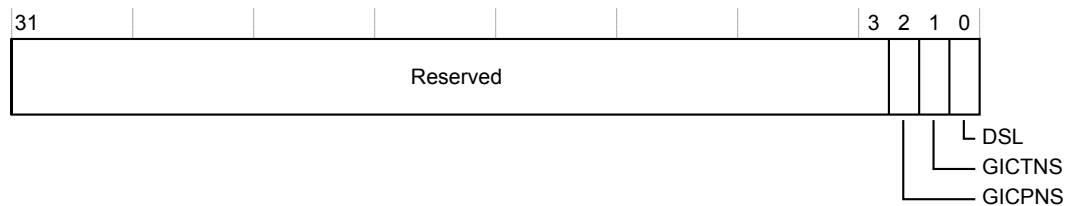
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.



**Figure 4-4 GICD\_SAC bit assignments**

The following table shows the bit assignments.

**Table 4-7 GICD\_SAC bit assignments**

Bits	Name	Function
[31:3]	-	Reserved, returns zero.
[2]	GICPNS	1 = Allow Non-secure access to the GICP registers. This enables Non-secure access to Secure PMU data. 0 = Secure access only. The <b>gicp_allow_ns</b> tie-off signal controls the reset value on a per-chip basis.
[1]	GICTNS	1 = Allow Non-secure access to the GICT registers. This enables Non-secure access to Secure trace data. 0 = Secure access only. The <b>gict_allow_ns</b> tie-off signal controls the reset value on a per-chip basis.
[0]	DSL	Disable Security Lock. <i>WriteOnce</i> (WO): 1 = WO bit to lock GICD_CTLR.DS to be WO at its current value. 0 = No effect. When set to 1, this value is only returned by reset.

#### 4.2.5 Interrupt Class Registers, GICD\_ICLARn

These registers control whether a 1 of N SPI can target a core that is assigned to class 0 or class 1 group. Each register controls 16 SPIs and the GIC-600 has 60 registers, GICD\_ICLAR2-GICD\_ICLAR61.

The GICD\_ICLARn characteristics are:

**Usage constraints**

The Distributor provides up to 60 registers to support 960 SPIs. If you configure the GIC-600 to use fewer than 960 SPIs, then it reduces the number of registers accordingly. For locations where interrupts are not implemented, the register is RAZ/WI.

### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.

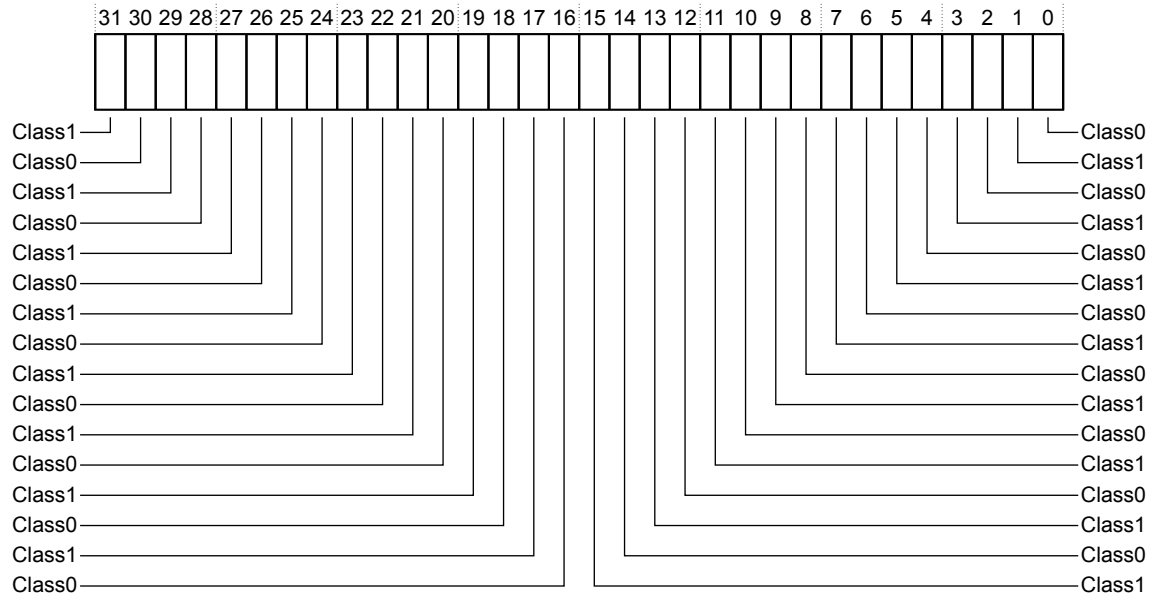


Figure 4-5 GICD\_ICLARN bit assignments

The following table shows the bit assignments.

Table 4-8 GICD\_ICLARN bit assignments

Bits	Name	Function
[31,29,27,25,23,21,19,17,15,13,11,9,7,5,3,1]	Class1	Controls whether the 1 of N SPI can target a core that is assigned to class 1: 0 = The SPI can target a core that is assigned to class 1 group. 1 = The SPI cannot target a core that is assigned to class 1 group.  ————— <b>Note</b> ————— The SPI that a bit refers to depends on its bit position and the base address offset of the GICD_ICLARN.
[30,28,26,24,22,20,18,16,14,12,10,8,6,4,2,0]	Class0	Controls whether the 1 of N SPI can target a core that is assigned to class 0: 0 = The SPI can target a core that is assigned to class 0 group. 1 = The SPI cannot target a core that is assigned to class 0 group.  ————— <b>Note</b> ————— The SPI that a bit refers to depends on its bit position and the base address offset of the GICD_ICLARN.

## 4.2.6 Interrupt Error Registers, GICD\_IERRRn

These registers indicate the error status of a SPI. Each register monitors 32 SPIs and the GIC-600 has 30 registers, GICD\_IERRR1-GICD\_IERRR30.

The GICD\_IERRRn characteristics are:

#### Usage constraints

The Distributor provides up to 30 registers to support 960 SPIs. If you configure the GIC-600 to use fewer than 960 SPIs, it reduces the number of registers accordingly. For locations where interrupts are not implemented, the register is RAZ/WI.

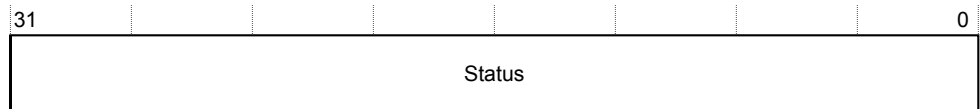
#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.



**Figure 4-6 GICD\_IERRRn bit assignments**

The following table shows the bit assignments.

**Table 4-9 GICD\_IERRRn bit assignments**

Bits	Name	Function
[31:0]	Status	<p>Indicates whether a SPI is in an error state:</p> <p>0 = The SPI is not in an error state and programming is valid.</p> <p>1 = The SPI is in an error state and programming is not valid.</p> <p><b>Note</b></p> <p>The SPI that a bit refers to depends on its bit position and the base address offset of the GICD_IERRRn.</p>

### 4.2.7 Configuration ID Register, GICD\_CFGID

This register contains information that enables test software to determine if the GIC-600 system is compatible. There is one register per configured chip. The offset determines the chip number.

The GICD\_CFGID characteristics are:

#### Usage constraints

There are no usage constraints.

#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.

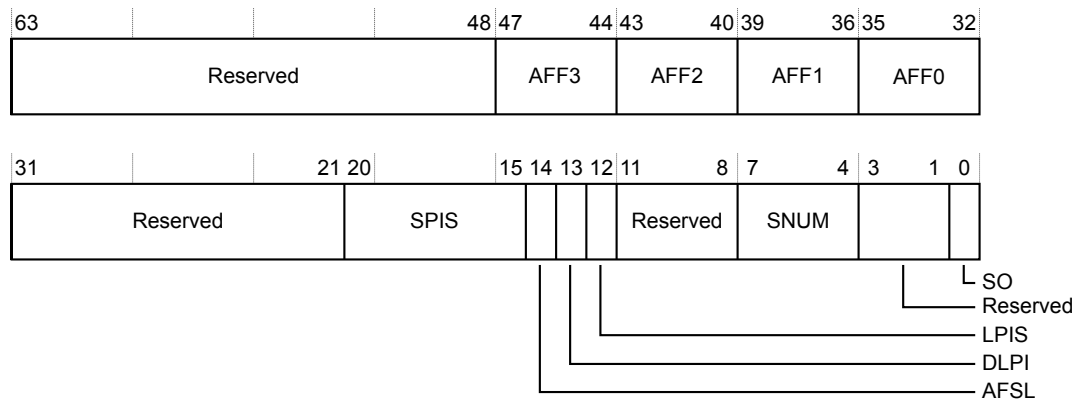


Figure 4-7 GICD\_CFGID bit assignments

The following table shows the bit assignments.

Table 4-10 GICD\_CFGID bit assignments

Bits	Name	Function
[63:48]	-	Reserved, returns zero
[47:44]	AFF3	Returns the Affinity3 bits
[43:40]	AFF2	Returns the Affinity2 bits
[39:36]	AFF1	Returns the Affinity1 bits
[35:32]	AFF0	Returns the Affinity0 bits
[31:21]	-	Reserved, returns zero
[20:15]	SPIS	SPI Groups
[14]	AFSL	Chip affinity selection level
[13]	DLPI	Direct LPI registers supported
[12]	LPIS	LPI supported
[11:8]	-	Reserved, returns zero
[7:4]	SNUM	Chip number
[3:1]	-	Reserved, returns zero
[0]	SO	Chip offline

#### 4.2.8 Peripheral ID2 register, GICD\_PIDR2

This register defines the GIC architecture version with which the GIC-600 complies.

The GICD\_PIDR2 characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.2 Distributor registers \(GICD/GICDA\) summary](#) on page 4-86.

The following figure shows the bit assignments.

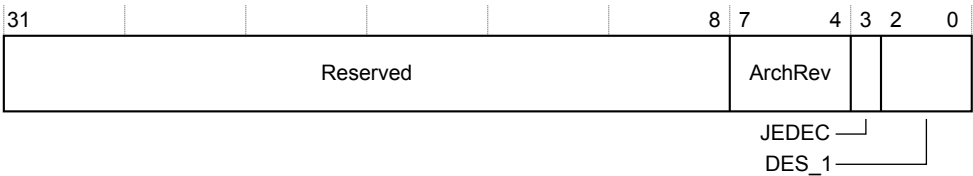


Figure 4-8 GICD\_PIDR2 bit assignments

The following table shows the bit assignments.

Table 4-11 GICD\_PIDR2 bit assignments

Bits	Name	Function
[31:8]	-	Reserved, RAZ.
[7:4]	ArchRev	Identifies the version of the GIC architecture with which the GIC-600 complies: <ul style="list-style-type: none"><li>• 0x03 = GICv3.</li></ul>
[3]	JEDEC	Indicates that a JEDEC-assigned JEP106 identity code is used.
[2:0]	DES_1	Bits[6:4] of the JEP106 identity code. Bits[3:0] of the JEP106 identity code are assigned to GICD_PIDR1.



## 4.3 Distributor registers (GICA) for message-based SPIs summary

The functions for the GIC-600 message-based SPIs are controlled through the Distributor registers identified with the prefix GICA.

The following table lists the message-based SPI registers. All registers are 32 bits wide.

**Table 4-12 Distributor registers (GICA) for message-based SPIs summary**

Offset	Name	Type	Reset	Description <sup>w</sup>
0x0000-0x003C	-	-	-	Reserved
0x0040	GICA_SETSPI_NSR	WO	-	Aliased Non-secure SPI Set Register
0x0044	-	-	-	Reserved
0x0048	GICA_CLRSPI_NSR	WO	-	Aliased Non-secure SPI Clear Register
0x004C	-	-	-	Reserved
0x0050	GICA_SETSPI_SR <sup>x</sup>	WO	-	Aliased Secure SPI Set Register <sup>y</sup>
0x0054	-	-	-	Reserved
0x0058	GICA_CLRSPI_SR <sup>x</sup>	WO	-	Aliased Secure SPI Clear Register <sup>y</sup>
0x005C-0xFFFC	-	-	-	Reserved

<sup>w</sup> For the description of the registers that are not specific to the GIC-600, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

<sup>x</sup> The existence of this register depends on the configuration of the GIC-600. If Security support is not included, this register does not exist.

<sup>y</sup> This register is only accessible from a Secure access.

## 4.4 Redistributor registers for control and physical LPIs summary

The functions for the GIC-600 physical LPIs are controlled through the Redistributor registers identified with the prefix GICR. In GICv3, these registers start from the base address.

For more information about LPIs, see *ARM® GICv3 and GICv4 Software Overview*.

For the description of the registers that are not specific to the GIC-600, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

**Table 4-13 Redistributor registers for control and physical LPIs summary**

Offset	Name	Type	Width	Reset	Description
0x0000	GICR_CTLR	RW	32	0x00000000	Redistributor Control Register
0x0004	GICR_IIDR	RO	32	0x0001043B	<a href="#">4.4.1 Redistributor Implementation Identification Register, GICR_IIDR</a> on page 4-99
0x0008	GICR_TYPER	RO	64	Configuration dependent	<a href="#">4.4.2 Interrupt Controller Type Register, GICR_TYPER</a> on page 4-100
0x0010	-	-	-	-	Reserved
0x0014	GICR_WAKER	RW	32	0x00000003	<a href="#">4.4.3 Power Management Control Register, GICR_WAKER</a> on page 4-102
0x0018-0x001C	-	-	-	-	Reserved
0x0020	GICR_FCTLR	RW	32	0x00000000	<a href="#">4.4.4 Function Control Register, GICR_FCTLR</a> on page 4-103
0x0024	GICR_PWRR	RW	32	0x00000000	<a href="#">4.4.5 Power Register, GICR_PWRR</a> on page 4-104
0x0028	GICR_CLASS	RW	32	0x00000000	<a href="#">4.4.6 Class Register, GICR_CLASS</a> on page 4-105
0x002C-0x003C	-	-	-	-	Reserved
0x0040	GICR_SETLPIR	WO	64	-	64-bit accesses only. Data contains the physical ID. Not present if any ITS is in the system.
0x0048	GICR_CLRLPIR	WO	64	-	64-bit accesses only. Data contains the physical ID. Not present if any ITS is in the system.
0x0050-0x006C	-	-	-	-	Reserved
0x0070	GICR_PROPBASER <sup>z</sup>	RW	64	0x0000000000000000	Redistributor Properties Base Address Register
0x0078	GICR_PENDBASER <sup>z</sup> <sup>aa</sup>	RW	64	0x0000000000000000	Redistributor LPI Pending Table Base Address Register <sup>ab</sup>
0x00A0	GICR_INVLPIR	WO	64	-	64-bit accesses only. Data contains the physical ID. Not present if any ITS is in the system.

<sup>z</sup> The existence of this register depends on the configuration of the GIC-600. If ITS and LPI support is not included, this register does not exist.

<sup>aa</sup> ARM recommends that if possible, you set the GICR\_PENDBASER Pending Table Zero bit to one. This reduces the power and time that is taken during initialization.

<sup>ab</sup> This register is only accessible from a Secure access.

**Table 4-13 Redistributor registers for control and physical LPIs summary (continued)**

Offset	Name	Type	Width	Reset	Description
0x00A8-0x00AC	-	-	-	-	Reserved
0x00B0	GICR_INVALLR	WO	64	-	64-bit accesses only. Not present if any ITS is in the system.
0x00B8-0x00BC	-	-	-	-	Reserved
0x00C0	GICR_SYNCR	RO	32	0x00000000	64-bit accesses only. Not present if any ITS is in the system.
0x00C8-0xFFFC	-	-	-	-	Reserved
0xFFD0	GICR_PIDR4	RO	32	0x00000044	Peripheral ID 4 Register
0xFFD4	GICR_PIDR5	RO	32	0x00000000	Peripheral ID 5 Register
0xFFD8	GICR_PIDR6	RO	32	0x00000000	Peripheral ID 6 Register
0xFFDC	GICR_PIDR7	RO	32	0x00000000	Peripheral ID 7 Register
0xFFE0	GICR_PIDR0	RO	32	0x00000093	Peripheral ID 0 Register
0xFFE4	GICR_PIDR1	RO	32	0x000000B4	Peripheral ID 1 Register
0xFFE8	GICR_PIDR2	RO	32	0x0000003B	<a href="#">4.4.7 Peripheral ID2 Register; GICR_PIDR2 on page 4-106</a>
0xFFEC	GICR_PIDR3	RO	32	0x00000000	Peripheral ID 3 Register
0xFFF0	GICR_CIDR0	RO	32	0x0000000D	Peripheral ID 0 Register
0xFFF4	GICR_CIDR1	RO	32	0x000000F0	Peripheral ID 1 Register
0xFFF8	GICR_CIDR2	RO	32	0x00000005	Peripheral ID 2 Register
0xFFFC	GICR_CIDR3	RO	32	0x000000B1	Peripheral ID 3 Register

This section contains the following subsections:

- [4.4.1 Redistributor Implementation Identification Register; GICR\\_IIDR on page 4-99.](#)
- [4.4.2 Interrupt Controller Type Register; GICR\\_TYPER on page 4-100.](#)
- [4.4.3 Power Management Control Register; GICR\\_WAKER on page 4-102.](#)
- [4.4.4 Function Control Register; GICR\\_FCTLR on page 4-103.](#)
- [4.4.5 Power Register; GICR\\_PWRR on page 4-104.](#)
- [4.4.6 Class Register; GICR\\_CLASS on page 4-105.](#)
- [4.4.7 Peripheral ID2 Register; GICR\\_PIDR2 on page 4-106.](#)

#### 4.4.1 Redistributor Implementation Identification Register, GICR\_IIDR

This register provides information about the implementer and revision of the Redistributor.

The GICR\_IIDR characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See [4.4 Redistributor registers for control and physical LPIs summary on page 4-98.](#)

The following figure shows the bit assignments.

31	24	23	20	19	16	15	12	11			0
ProductID		Reserved		Variant		Revision		Implementer			

**Figure 4-9 GICR\_IIDR bit assignments**

The following table shows the bit assignments.

**Table 4-14 GICR\_IIDR bit assignments**

Bits	Name	Function
[31:24]	ProductID	Indicates the product ID: $0 \times 02 = \text{GIC-600}$ .
[23:20]	-	Reserved, RAZ
[19:16]	Variant	Indicates the major revision or variant of the product for the <i>rmprn</i> identifier: $0 \times 0 = r0$ .
[15:12]	Revision	Indicates the minor revision of the product for the <i>rmprn</i> identifier: $0 \times 1 = p0$ . $0 \times 3 = p1$ . $0 \times 4 = p2$ .
[11:0]	Implementer	Identifies the implementer: $0 \times 43B = \text{ARM}$ .

#### 4.4.2 Interrupt Controller Type Register, GICR\_TYPER

This register returns information about the configuration of the GIC-600.

The GICR\_TYPER characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.4 Redistributor registers for control and physical LPIs summary on page 4-98](#).

The following figure shows the bit assignments.

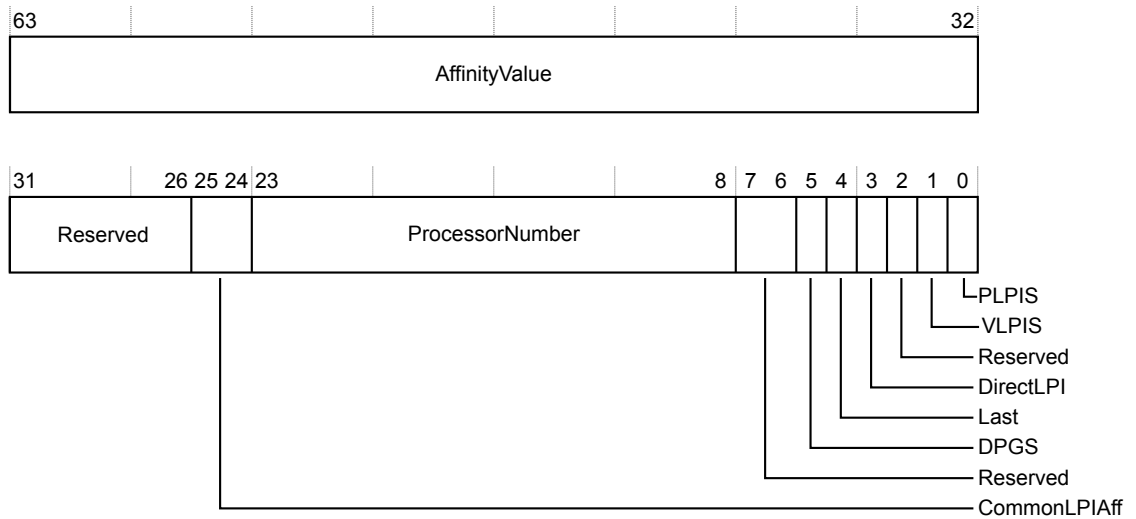


Figure 4-10 GIC\_TYPER bit assignments

The following table shows the bit assignments.

Table 4-15 GIC\_TYPER bit assignments

Bits	Name	Function
[63:32]	AffinityValue	Affinity level value for this Redistributor: AF3, bits[63:56], Affinity level 3 value. AF2, bits[55:48], the Affinity level 2 value. AF1, bits[47:40], the Affinity level 1 value. AF0, bits[39:32], the Affinity level 0 value.
[31:26]	-	Reserved, returns 0b000000.
[25:24]	CommonLPIAff	Returns: 00 = Single core configuration. 01 = If chip set by AF3. 10 = If chip set by AF2. 11 = Reserved.
[23:8]	ProcessorNumber	Returns the core number and chip number that uniquely identifies this core in the system.
[7:6]	-	Reserved, returns 0b00.
[5]	DPGS	Disable Processor Group Selections: 1 = The GIC-600 supports DPG. See <i>ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0</i> .
[4]	Last	Last Redistributor: 0 = This Redistributor is not the last Redistributor on the chip. 1 = This Redistributor is the last Redistributor on the chip.

**Table 4-15 GIC\_TYPER bit assignments (continued)**

Bits	Name	Function
[3]	DirectLPI	Direct injection of LPIs: 0 = The GIC-600 does not support LPIs. 1 = The GIC-600 supports LPIs and there is no ITS in the system.
[2]	-	Reserved, returns 0.
[1]	VLPIS	Virtual LPI support: 0 = The GIC-600 does not support Virtual LPIs. See <i>ARM® GICv3 and GICv4 Software Overview</i> .
[0]	PLPIS	Physical LPI support: 0 = The GIC-600 does not support LPIs. 1 = The GIC-600 supports LPIs.

#### 4.4.3 Power Management Control Register, GICR\_WAKER

This register controls whether the GIC-600 can be powered down.

The GICR\_WAKER characteristics are:

##### Usage constraints

There are no usage constraints.

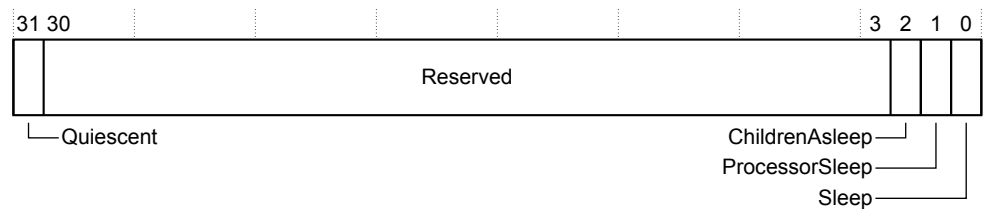
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See [4.4 Redistributor registers for control and physical LPIs summary](#) on page 4-98.

The following figure shows the bit assignments.



**Figure 4-11 GICR\_WAKER bit assignments**

The following table shows the bit assignments.

**Table 4-16 GICR\_WAKER bit assignments**

Bits	Name	Function
[31]	Quiescent	Indicates that the GIC-600 is idle and can be powered down if necessary.
[30:3]	-	Reserved, RAZ.
[2]	ChildrenAsleep	Indicates that the bus between the CPU interface and this Redistributor is quiescent.

**Table 4-16 GICR\_WAKER bit assignments (continued)**

Bits	Name	Function
[1]	ProcessorSleep	Indicates:  0 = This Redistributor never asserts <b>wake_request</b> .  1 = This Redistributor must assert a <b>wake_request</b> if there is a pending interrupt targeted at the connected core. See <a href="#">Processor core power management on page 3-54</a> .
[0]	Sleep	Indicates the sleep state:  0 = Normal operation.  1 = The GIC-600 ensures that all the caches are consistent with external memory and that it is safe to power down. See <a href="#">Other power management on page 3-55</a> .

#### Related references

[Other power management on page 3-55](#).

#### 4.4.4 Function Control Register, GICR\_FCTLR

This register controls the scrubbing of all RAMs in the associated Redistributor.

The GICR\_FCTLR characteristics are:

##### Usage constraints

There are no usage constraints.

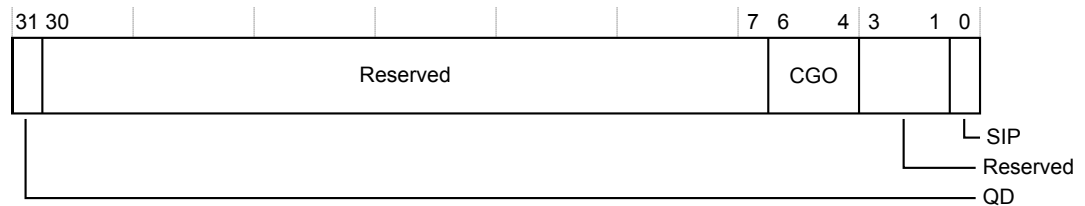
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.4 Redistributor registers for control and physical LPIs summary on page 4-98](#).

The following figure shows the bit assignments.



**Figure 4-12 GICR\_FCTLR bit assignments**

The following table shows the bit assignments.

**Table 4-17 GICR\_FCTLR bit assignments**

Bits	Name	Function
[31]	QD	Q-Channel deny:  0 = Allow Q-Channel accesses.  1 = Deny Q-Channel accesses.
[30:7]	-	Reserved, RAZ/WI.
[6:4]	CGO	One bit per clock gate:  0 = Use full clock gating.  1 = Leave clock running.

Bits	Name	Function
[3:1]	-	Reserved, RAZ/WI.
[0]	SIP	<p>Scrub in progress:</p> <p>0 = No scrub in progress.</p> <p>1 = Scrub in progress.</p> <p>This bit is read and written by software. When a scrub is complete, the GIC clears the bit to 0.</p>

#### 4.4.5 Power Register, GICR\_PWRR

This register controls the powerup sequence of the Redistributors. Software must write to this register during the powerup sequence.

The GICR\_PWRR characteristics are:

## Usage constraints

There are no usage constraints.

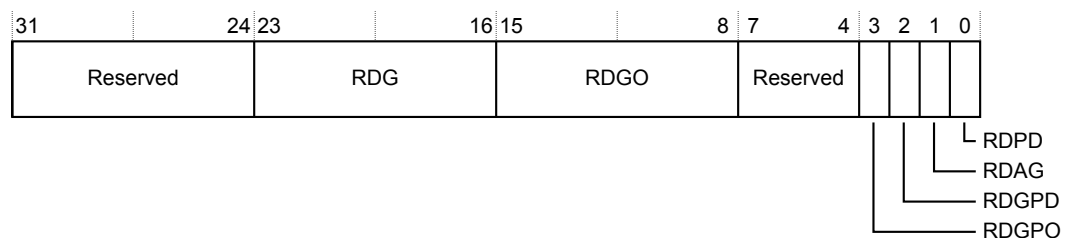
## Configurations

Available in all GIC-600 configurations.

## Attributes

See *4.4 Redistributor registers for control and physical LPIs summary* on page 4-98.

The following figure shows the bit assignments.



**Figure 4-13 GICR\_PWRR bit assignments**

The following table shows the bit assignments.

### Table 4-18 GICR\_PWRR bit assignments

Bits	Name	Function
[31:24]	-	Reserved, RAZ.
[23:16]	RDG	RDGroup. This read-only field indicates the number of the current Redistributor. Must be packed from 0.
[15:8]	RDGO	RDGroupOffset. This read-only field indicates the offset of the current core that is connected to the current Redistributor. Must be packed from 0 but does not necessarily map to a single cluster because the AXI4-Stream bus can be subdivided.
[7:4]	-	Reserved, RAZ.
[3]	RDGPO	RDGroupPoweredOff. This read-only bit indicates:  0 = Redistributor is powered up and can be accessed.  1 = It is safe to power down the Redistributor.



Bits	Name	Function
[2]	RDGPD	RDGroupPowerDown. This read-only bit indicates the intentional power state of the Redistributor:  0 = Intend to power up.  1 = Intend to power down.  The Redistributor has reached its intentional power state when RDGPD = RDGPO.
[1]	RDAG	RDApplyGroup. This write-only bit applies the RDPD value to all Redistributors in the group.  If the RDPD value cannot be applied to all cores in the group, then the GIC ignores this request.
[0]	RDPD	RDPowerDown:  0 = Redistributor is powered up and can be accessed.  1 = The core permits the Redistributor to be powered down.  Writes to 1 ignored if GICR_WAKER.ProcessorSleep != 1.  Writes ignored if RDGPD != RDGPO and changing to not match RDGPD.  If all other cores in the Redistributor group have RDPD == 1, then setting this bit to 1 also sets RDGPD = 1.

#### 4.4.6 Class Register, GICR\_CLASS

This register controls the assignment of interrupts to either class 0 or class 1.

The GICR\_CLASS characteristics are:

## Usage constraints

There are no usage constraints.

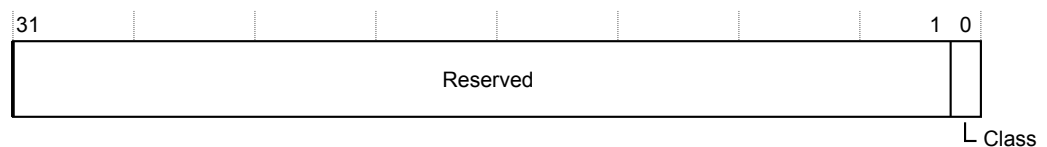
## Configurations

Available in all GIC-600 configurations.

## Attributes

See the *4.4 Redistributor registers for control and physical LPIs summary* on page 4-98.

The following figure shows the bit assignments.



**Figure 4-14 GICR\_CLASS bit assignments**

The following table shows the bit assignments.

### Table 4-19 GICR\_CLASS bit assignments

Bits	Name	Function
[31:1]	-	Reserved, RAZ/WI.
[0]	Class	Interrupt class: 0 = Class 0. 1 = Class 1.

4.4.7 Peripheral ID2 Register, GICR\_PIDR2

This register defines the GIC architecture version with which the GIC-600 complies.

The GICR\_PIDR2 characteristics are:

Usage constraints

There are no usage constraints.

Configurations

Available in all GIC-600 configurations.

Attributes

See [4.4 Redistributor registers for control and physical LPIs summary](#) on page 4-98.

The following figure shows the bit assignments.

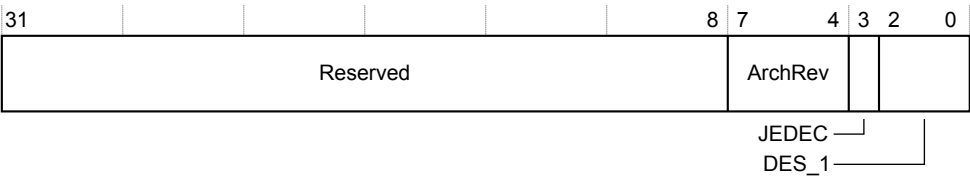


Figure 4-15 GICR\_PIDR2 bit assignments

The following table shows the bit assignments.

Table 4-20 GICR\_PIDR2 bit assignments

Bits	Name	Function
[31:8]	-	Reserved, RAZ.
[7:4]	ArchRev	Identifies the version of the GIC architecture with which the GIC-600 complies: <ul style="list-style-type: none"><li>0x03 = GICv3.</li></ul>
[3]	JEDEC	Indicates that a JEDEC-assigned JEP106 identity code is used.
[2:0]	DES_1	Bits[6:4] of the JEP106 identity code. Bits[3:0] of the JEP106 identity code are assigned to GICR_PIDR1.

Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 4.5 Redistributor registers for SGIs and PPIs summary

The functions for the GIC-600 SGIs and PPIs are controlled through the Redistributor registers identified with the prefix GICR.

For a description of the registers that are not specific to the GIC-600, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

**Table 4-21 Redistributor registers for SGIs and PPIs summary**

Offset	Name	Type	Width	Reset	Description
0x0000-0x007C	-	-	-	-	Reserved
0x0080	GICR_IGROUPR0	RW	32	0x00000000	Interrupt Group Register
0x0084-0x0FFC	-	-	-	-	Reserved
0x0100	GICR_ISENABLER0	RW	32	0x00000000	Interrupt Set-Enable Register
0x0104-0x017C	-	-	-	-	Reserved
0x0180	GICR_ICENABLER0	RW	32	0x00000000	Interrupt Clear-Enable Register
0x0184-0x01FC	-	-	-	-	Reserved
0x0200	GICR_ISPENDR0	RW	32	0x00000000	Interrupt Set-Pending Register
0x0204-0x027C	-	-	-	-	Reserved
0x0280	GICR_ICPENDR0	RW	32	0x00000000	Peripheral Clear Pending Register
0x0284-0x02FC	-	-	-	-	Reserved
0x0300	GICR_ISACTIVER0	RW	32	0x00000000	Interrupt Set-Active Register
0x0304-0x037C	-	-	-	-	Reserved
0x0380	GICR_ICACTIVER0	RW	32	0x00000000	Interrupt Clear-Active Register
0x0384-0x03FC	-	-	-	-	Reserved
0x0400-0x041C	GICR_IPRIORITYRn	RW	32	0x00000000	Interrupt Priority Registers
0x0420-0x0BFC	-	-	-	-	Reserved
0x0C00-0x0C04	GICR_ICFGRn	RO	32	0xAAAAAAAA <sup>ac</sup>	Peripheral ID 3 Registers
0x0C08-0x0CFC	-	-	-	-	Reserved
0x0D00	GICR_IGRPMODR0	RW	32	0x00000000	Interrupt Group Modifier Register
0x0D04-0x0DFC	-	-	-	-	Reserved
0x0E00	GICR_NSACR	RW	32	0x00000000	Non-secure Access Control Register
0x0E04-0xBFFC	-	-	-	-	Reserved
0xC000	GICR_MISCTATUSR	RO	32	0x00000000	<a href="#">4.5.1 Miscellaneous Status Register, GICR_MISCTATUSR on page 4-108</a>
0xC004	-	-	-	-	Reserved
0xC008	GICR_IERRVR	RO	32	0x00000000	<a href="#">4.5.2 Interrupt Error Valid Register, GICR_IERRV on page 4-109</a>
0xC00C	-	-	-	-	Reserved

<sup>ac</sup> When GIC-600 is configured to have GICD\_CTLR.ARE\_S or GICD\_CTLR.ARE\_NS as programmable, if ARE is 0 for the security state of the SGI, this register is Reserved and RAZ/WI.

**Table 4-21 Redistributor registers for SGIs and PPIs summary (continued)**

Offset	Name	Type	Width	Reset	Description
0xC010-0xC014	GICR_SGIDR	RW	64	-	<a href="#">4.5.3 SGI Default Register; GICR_SGIDR on page 4-110</a>
0xC018-0xEFFC	-	-	-	-	Reserved
0xF000	GICR_CFGID0	RO	32	-	<a href="#">4.5.4 Configuration ID0 Register; GICR_CFGID0 on page 4-110</a>
0xF004	GICR_CFGID1	RO	32	-	<a href="#">4.5.5 Configuration ID1 Register; GICR_CFGID1 on page 4-111</a>

This section contains the following subsections:

- [4.5.1 Miscellaneous Status Register; GICR\\_MISCSTATUSR on page 4-108.](#)
- [4.5.2 Interrupt Error Valid Register; GICR\\_IERRV on page 4-109.](#)
- [4.5.3 SGI Default Register; GICR\\_SGIDR on page 4-110.](#)
- [4.5.4 Configuration ID0 Register; GICR\\_CFGID0 on page 4-110.](#)
- [4.5.5 Configuration ID1 Register; GICR\\_CFGID1 on page 4-111.](#)

#### 4.5.1 Miscellaneous Status Register, GICR\_MISCSTATUSR

Use this register to test the integration of the **cpu\_active** input signals and to debug the CPU interface enables as seen by the GIC-600.

The GICR\_MISCSTATUSR characteristics are:

##### Usage constraints

There are no usage constraints.

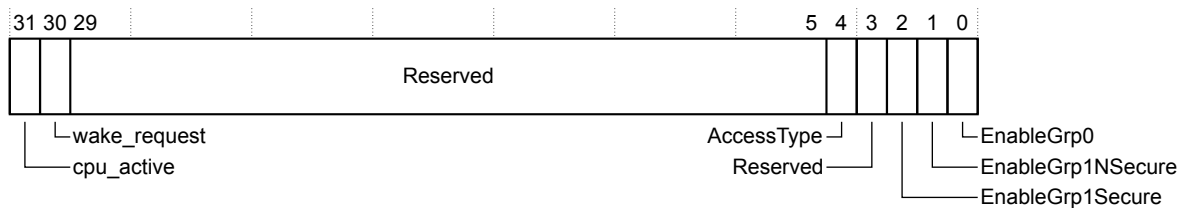
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.5 Redistributor registers for SGIs and PPIs summary on page 4-107.](#)

The following figure shows the bit assignments.



**Figure 4-16 GICR\_MISCSTATUSR bit assignments**

The following table shows the bit assignments.

**Table 4-22 GICR\_MISCTATUSR bit assignments**

Bits	Name	Function
[31]	cpu_active	Returns the status of the <b>cpu_active</b> signal for the core corresponding to the Redistributor whose register is being read:  0 = <b>cpu_active</b> input signal not active.  1 = <b>cpu_active</b> input signal active.  This bit is UNDEFINED when ProcessorSleep or ChildrenAsleep is set for a core, because the core is presumed to be powered down.
[30]	wake_request	0 = <b>wake_request</b> not active.  1 = <b>wake_request</b> asserted.
[29:5]	-	Reserved.
[4]	AccessType	0 = Secure access.  1 = Non-secure access.
[3]	-	Reserved.
[2] <sup>ad</sup>	EnableGrp1Secure	In systems with two Security states enabled, when GICD_CTLR.DS == 0, then: <ul style="list-style-type: none"> <li>For Secure reads, returns the Group 1 Secure CPU interface enable.</li> <li>For Non-secure reads, returns zero.</li> </ul> In systems with only a single Security state enabled, when GICD_CTLR.DS == 1, then this bit returns zero.
[1] <sup>ad</sup>	EnableGrp1NSecure	In systems with two Security states enabled, when GICD_CTLR.DS == 0, then: <ul style="list-style-type: none"> <li>For Secure reads, this bit returns the Group 1 Non-secure CPU interface enable.</li> <li>For Non-secure reads, when GICD_CTLR.ARE_NS == 1, this bit returns the Group 1 Non-secure CPU interface enable.</li> <li>For Non-secure reads when GICD_CTLR.ARE_NS == 0, this bit returns zero.</li> </ul> In systems with only a single Security state enabled, when GICD_CTLR.DS == 1, this bit returns the Group 1 CPU interface enable.
[0] <sup>ad</sup>	EnableGrp0	In systems with two Security states enabled, when GICD_CTLR.DS == 0, then: <ul style="list-style-type: none"> <li>For Secure reads, this bit returns the Group 0 CPU interface enable.</li> <li>For Non-secure reads when GICD_CTLR.ARE_NS == 0, this bit returns the Group 1 Non-secure CPU interface enable.</li> <li>For Non-secure reads when GICD_CTLR.ARE_NS == 1, this bit returns zero.</li> </ul> In systems with only a single Security state enabled, when GICD_CTLR.DS == 1, this bit returns the Group 0 CPU interface enable.

#### 4.5.2 Interrupt Error Valid Register, GICR\_IERRV

This register indicates if the SGI or PPI data has been corrupted in SRAM.

The GICR\_IERRV characteristics are:

##### Usage constraints

There are no usage constraints.

<sup>ad</sup> These bits are a copy of the CPU interface group enables for the core corresponding to this Redistributor. These copies are UNDEFINED when ProcessorSleep or ChildrenSleep is set for a core, because the core is presumed to be powered down. Upstream Write packets maintain these copies that can de-synchronize after an incorrect powerdown sequence. This register enables you to debug this scenario. For more information, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.5 Redistributor registers for SGIs and PPIs summary](#) on page 4-107.

The following table shows the bit assignments.

**Table 4-23 GICR\_IERRV bit assignments**

Bits	Name	Function
[0] + n	valid<n>	0 = No error on interrupt n.
	n = 0-31	1 = There is an error on interrupt n so the interrupt is not delivered.

### 4.5.3 SGI Default Register, GICR\_SGIDR

This register controls the default value of SGI settings, for use in the case of a *DEDERR*.

The GICR\_SGIDR characteristics are:

### Usage constraints

Only accessible by Secure accesses.

### Configurations

Available in all GIC-600 configurations. If SGI ECC is not enabled, then this register is RES0.

### Attributes

See the [4.5 Redistributor registers for SGIs and PPIs summary](#) on page 4-107.

The following table shows the bit assignments.

**Table 4-24 GICR\_SGIDR bit assignments**

Bits	Name	Function
[3] + 4n: [63, 59, 55, 51, 47, 43, 39, 35, 31, 27, 23, 19, 15, 11, 7, 3]	-	Reserved, RAZ.
[2] + 4n: [62, 58, 54, 50, 46, 42, 38, 34, 30, 26, 22, 18, 14, 10, 6, 2]	GRPMOD	As GRPMOD register.
[1] + 4n: [61, 57, 53, 49, 45, 41, 37, 33, 29, 25, 21, 17, 13, 9, 5, 1]	GRP	As GRP register.
[0] + 4n: [60, 56, 52, 48, 44, 40, 36, 32, 28, 24, 20, 16, 12, 8, 4, 0]	nsacr	1 = Allow Non-secure access to interrupt <n>.

### 4.5.4 Configuration ID0 Register, GICR\_CFGID0

This register returns information about the configuration of the Redistributors.

The GICR\_CFGID0 characteristics are:

### Usage constraints

There are no usage constraints.

### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.5 Redistributor registers for SGIs and PPIs summary](#) on page 4-107.

The following figure shows the bit assignments.

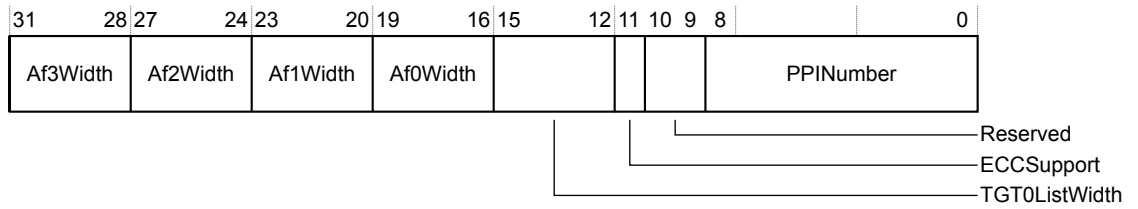


Figure 4-17 GICR\_CFGID0 bit assignments

The following table shows the bit assignments.

Table 4-25 GICR\_CFGID0 bit assignments

Bits	Name	Function
[31:28]	Af3Width	Affinity 3 width.
[27:24]	Af2Width	Affinity 2 width.
[23:20]	Af1Width	Affinity 1 width.
[19:16]	Af0Width	Affinity 0 width.
[15:12]	TGT0ListWidth	The Target0 list width - 1.
[11]	ECCSupport	1 = ECC is supported.
[10:9]	-	Reserved, RAZ.
[8:0]	PPINumber	RedistributorID. The <b>ppi_id[15:0]</b> tie-off signal sets the value of the ID. Each Redistributor must have a unique ID.

#### Related references

[A.6 Miscellaneous signals on page Appx-A-163.](#)

#### 4.5.5 Configuration ID1 Register, GICR\_CFGID1

This register returns information about the configuration of the Redistributors.

The GICR\_CFGID1 characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.5 Redistributor registers for SGIs and PPIs summary on page 4-107](#).

The following figure shows the bit assignments.

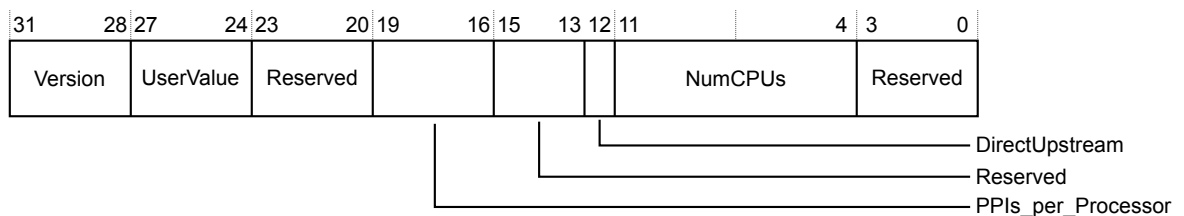


Figure 4-18 GICR\_CFGID1 bit assignments

The following table shows the bit assignments.

**Table 4-26 GICR\_CFGID1 bit assignments**

Bits	Name	Function
[31:28]	Version	Identifies the major and minor revisions, and product quality status of the GIC-600: 0x1 = version 0 (r0p0). 0x3 = version 1 (r0p1). 0x4 = version 2 (r0p2).
[27:24]	UserValue	Modification value that you can set.
[23:20]	-	Reserved, RAZ.
[19:16]	PPIs_per_Processor	The number of Redistributors that each core supports - 1.
[15:13]	-	Reserved.
[12]	DirectUpstream	Indicates a direct upstream connection.
[11:4]	NumCPUs	The number of cores that are integrated in this Redistributor.
[3:0]	-	Reserved, RAZ.



## 4.6 ITS control register summary

The GIC-600 Interrupt Translation Service functions are controlled through registers identified with the prefix GITS.

For a description of the registers that are not specific to the GIC-600, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

### Note

This page does not exist in GIC-600 configurations that do not support LPis or that do not have an ITS.

**Table 4-27 ITS control register summary**

Offset	Name	Type	Width	Reset	Description
0x0000	GITS_CTLR	RW	32	0x80000000	ITS Control Register
0x0004	GITS_IIDR	RO	32	0x0001043B	<a href="#">4.6.1 ITS Implementer Identification Register, GITS_IIDR on page 4-114</a>
0x0008	GITS_TYPER	RO	64	Configuration dependent	<a href="#">4.6.2 Interrupt Controller Type Register, GITS_TYPER on page 4-115</a>
0x0010-0x001C	-	-	32	-	Reserved
0x0020	GITS_FCTLR	RW	32	0x00000000	<a href="#">4.6.3 Function Control Register, GITS_FCTLR on page 4-116</a>
0x0024	-	-	-	-	Reserved
0x0028	GITS_OPR	RW	64	0x0000000000000000	<a href="#">4.6.4 Operations Register, GITS_OPR on page 4-118</a>
0x0030-0x0034	GITS_OPSR	RO	64	0x0000000000000000	<a href="#">4.6.5 Operation Status Register, GITS_OPSR on page 4-119</a>
0x0038-0x007C	-	-	-	-	Reserved
0x0080-0x0084	GITS_CBASER	RW	64	0x0000000000000000	Command Queue Control Register See <i>ARM® GICv3 and GICv4 Software Overview</i>
0x0088-0x008C	GITS_CWRITER	RW	64	0x0000000000000000	Command Queue Write Pointer Register
0x0090-0x0094	GITS_CREADR	RO	64	0x0000000000000000	Command Queue Read Pointer Register
0x0098-0x00FC	-	-	-	-	Reserved
0x0100-0x0104	GITS_BASER0	RW	64	0x0107000000000000	ITS Translation Table Descriptor Register0
0x0108-0x010C	GITS_BASER1	RW	64	0x0000000000000000	ITS Translation Table Descriptor Register1
0x0108-0xEFFC	-	-	-	-	Reserved
0xF000	GITS_CFGID	RO	32	0x00000000	<a href="#">4.6.6 Configuration ID Register, GITS_CFGID on page 4-120</a>
0xF004-0xFFCC	-	-	-	-	Reserved
0xFFD0	GITS_PIDR4	RO	32	0x00000044	Peripheral ID 4 Register
0xFFD4	GITS_PIDR5	RO	32	0x00000000	Peripheral ID 5 Register
0xFFD8	GITS_PIDR6	RO	32	0x00000000	Peripheral ID 6 Register
0xFFDC	GITS_PIDR7	RO	32	0x00000000	Peripheral ID 7 Register

**Table 4-27 ITS control register summary (continued)**

Offset	Name	Type	Width	Reset	Description
0xFFE0	GITS_PIDR0	RO	32	0x00000094	Peripheral ID 0 Register
0xFFE4	GITS_PIDR1	RO	32	0x000000B4	Peripheral ID 1 Register
0xFFE8	GITS_PIDR2	RO	32	0x0000003B	<a href="#">4.6.7 Peripheral ID2 Register; GITS_PIDR2 on page 4-121</a>
0xFFEC	GITS_PIDR3	RO	32	0x00000000	Peripheral ID 3 Register
0xFFF0	GITS_CIDR0	RO	32	0x0000000D	Component ID 0 Register
0xFFF4	GITS_CIDR1	RO	32	0x000000F0	Component ID 1 Register
0xFFF8	GITS_CIDR2	RO	32	0x00000005	Component ID 2 Register
0xFFFC	GITS_CIDR3	RO	32	0x000000B1	Component ID 3 Register

This section contains the following subsections:

- [4.6.1 ITS Implementer Identification Register; GITS\\_IIDR on page 4-114.](#)
- [4.6.2 Interrupt Controller Type Register; GITS\\_TYPER on page 4-115.](#)
- [4.6.3 Function Control Register; GITS\\_FCTLR on page 4-116.](#)
- [4.6.4 Operations Register; GITS\\_OPR on page 4-118.](#)
- [4.6.5 Operation Status Register; GITS\\_OPSR on page 4-119.](#)
- [4.6.6 Configuration ID Register; GITS\\_CFGID on page 4-120.](#)
- [4.6.7 Peripheral ID2 Register; GITS\\_PIDR2 on page 4-121.](#)

#### 4.6.1 ITS Implementer Identification Register, GITS\_IIDR

This register provides information about the implementer and revision of the ITS.

The GITS\_IIDR characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.6 ITS control register summary on page 4-113.](#)

The following figure shows the bit assignments.

31	24	23	20	19	16	15	12	11		0
ProductID				Reserved	Variant		Revision		Implementer	

**Figure 4-19 GITS\_IIDR bit assignments**

The following table shows the bit assignments.

**Table 4-28 GITS\_IIDR bit assignments**

Bits	Name	Function
[31:24]	ProductID	Indicates the product ID: 0x02 = GIC-600.
[23:20]	-	Reserved, RAZ.

Table 4-28 GITS\_IIDR bit assignments (continued)

Bits	Name	Function
[19:16]	Variant	Indicates the major revision or variant of the product for the rmpn identifier: $0 \times 0 = r0$ .
[15:12]	Revision	Indicates the minor revision of the product for the rmpn identifier: $0 \times 1 = p0$ . $0 \times 3 = p1$ . $0 \times 4 = p2$ .
[11:0]	Implementer	Identifies the implementer: $0 \times 43B = ARM$ .

#### 4.6.2 Interrupt Controller Type Register, GITS\_TYPER

This register returns information about the configuration of the GIC-600.

The GITS\_TYPER characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.6 ITS control register summary on page 4-113](#).

The following figure shows the bit assignments.

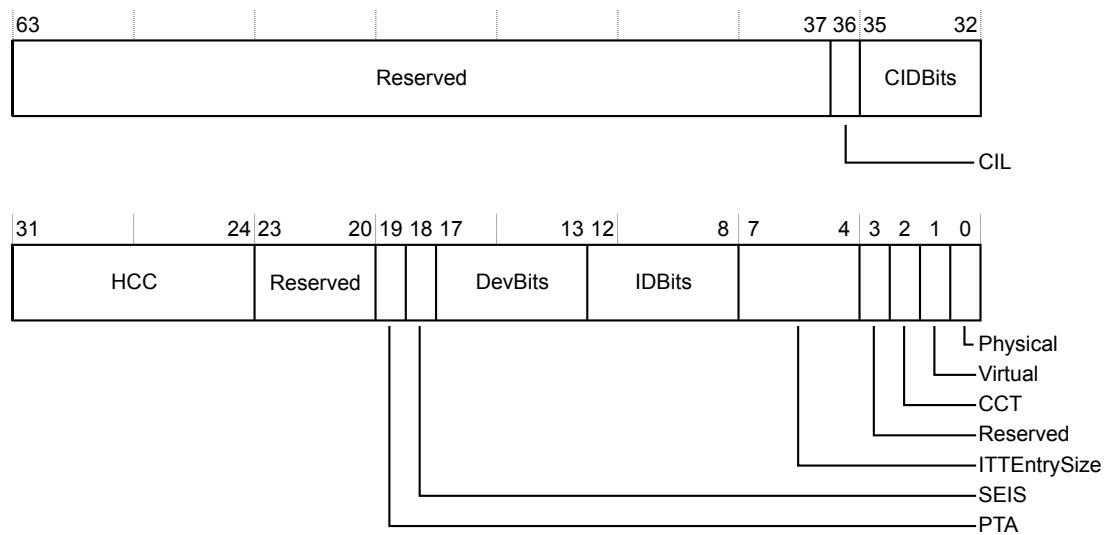


Figure 4-20 GITS\_TYPER bit assignments

The following table shows the bit assignments.

**Table 4-29 GITS\_TYPER bit assignments**

Bits	Name	Function
[63:37]	-	Reserved, RAZ.
[36]	CIL	CollectionID limit: 1 = The GIC-600 supports CIL.
[35:32]	CIDBits	The number of CollectionID bits, minus one. Set by the <code>col_width</code> configuration parameter.
[31:24]	HCC	Hardware collection count: 0 = All memory backed.
[23:20]	-	Reserved, returns 0.
[19]	PTA	Physical target addresses: 0 = The GIC-600 does not support physical target addresses.
[18]	SEIS	System error interrupts: 0 = The GIC-600 does not support locally generated System Error interrupts.
[17:13]	Devbits	The number of device identifier bits implemented, minus one. Set by the <code>did_width</code> configuration parameter.
[12:8]	IDBits	The number of interrupt identifier bits implemented, minus one. Set by the <code>vid_width</code> configuration parameter.
[7:4]	ITT Entry size	The number of bytes per entry, minus one: 0x3 = The GIC-600 supports a 4-byte ITT entry size.
[3]	-	Reserved.
[2]	CCT	Cumulative collection tables: 0 = Total number of supported collections is determined by the number of collections that are held in memory only.
[1]	Virtual	Virtual LPIs: 0 = The GIC-600 does not support Virtual LPIs. See <i>ARM® GICv3 and GICv4 Software Overview</i> .
[0]	Physical	Physical LPIs: 1 = The GIC-600 supports physical LPIs.

### 4.6.3 Function Control Register, GITS\_FCTL

This register controls the scrubbing of all RAMs in the local GITS. The register is not distributed and only acts on the local chip.

The GITS\_FCTL characteristics are:

#### Usage constraints

There are no usage constraints.

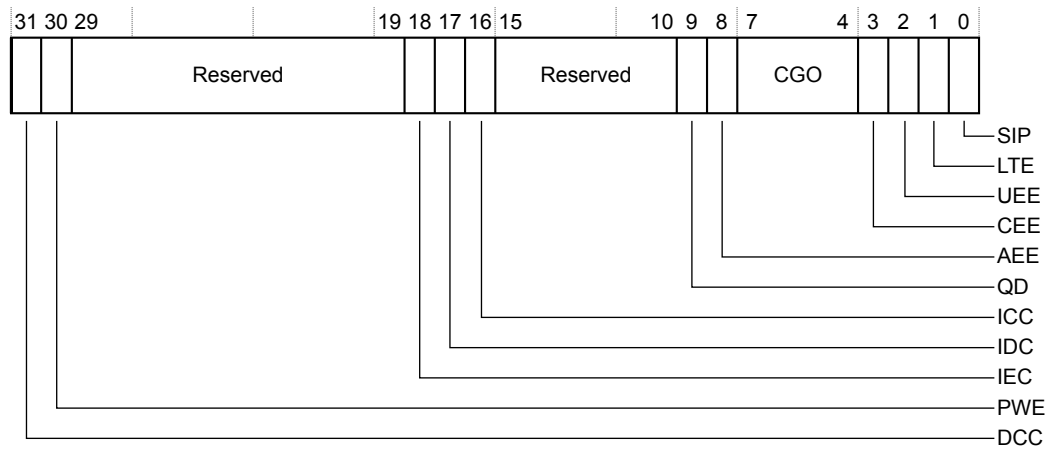
#### Configurations

Available in all GIC-600 configurations.

## Attributes

See the [4.6 ITS control register summary](#) on page 4-113.

The following figure shows the bit assignments.



**Figure 4-21 GITS\_FCTLR bit assignments**

The following table shows the bit assignments.

**Table 4-30 GITS\_FCTLR bit assignments**

Bits	Name	Function
[31]	DCC	Disable Cache Conversion: 0 = Use SMMU attribute for AMBA mapping. 1 = Use Direct attribute for AMBA mapping.
[30]	PWE	Powerdown While Enabled: 0 = Requests GITS_CTLR.Quiescent to indicate ITS is quiescent and can be powered down. 1 = Do not request GITS_CTLR.Quiescent to indicate ITS is quiescent.
[29:19]	-	Reserved, RAZ/WI.
[18]	IEC	Invalidate Event Cache: 1 = Invalidate event cache enabled. 0 = Invalidate event cache disabled.
[17]	IDC	Invalidate Device Cache: 1 = Invalidate Device cache enabled. 0 = Invalidate Device cache disabled.
[16]	ICC	Invalidate Collection cache: 1 = Invalidate Collection cache enabled. 0 = Invalidate Collection cache disabled.
[15:8]	-	Reserved, RAZ/WI.
[9]	QD	Q Deny: 1 = Always deny Q-Channel requests. 0 = Do not deny Q-Channel requests.

**Table 4-30 GITS\_FCTLR bit assignments (continued)**

Bits	Name	Function
[8]	AEE	Access Error Enable: 1 = Enable reporting of slave access errors. 0 = Do not enable reporting of slave access errors.
[7:4]	CGO	One bit per clock gate: 0 = Use full clock gating. 1 = Leave clock running.
[3]	CEE	Command error enable: 0 = Command errors are disabled. 1 = Command errors are enabled.
[2]	UEE	Unmapped error enable: 0 = Unmapped interrupt errors are disabled. 1 = Unmapped interrupt errors are enabled.
[1]	LTE	Latency tracking enable: 0 = Latency tracking of interrupts is disabled. 1 = Latency tracking of interrupts is enabled.
[0]	SIP	Scrub in progress: 0 = No scrub in progress. 1 = Scrub in progress. This bit is read and written by software. When a scrub is complete, the GIC clears the bit to 0.

#### 4.6.4 Operations Register, GITS\_OPR

This register controls cache lock.

The GITS\_OPR characteristics are:

##### Usage constraints

There are no usage constraints.

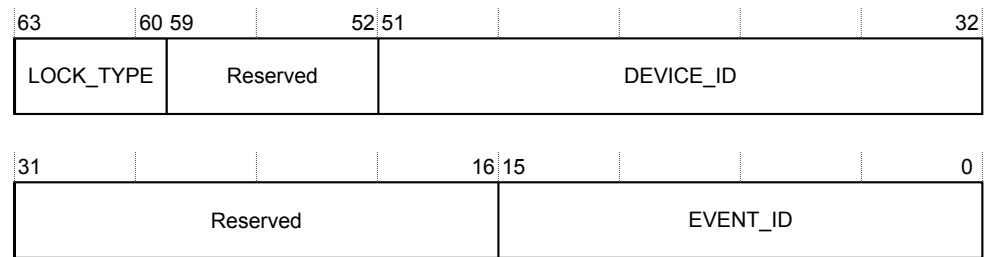
##### Configurations

Available in all GIC-600 configurations. However, for single-chip configurations this register is RAZ/WI.

##### Attributes

See the [4.6 ITS control register summary on page 4-113](#).

The following figure shows the bit assignments.



**Figure 4-22 GITS\_OPR bit assignments**

The following table shows the bit assignments.

**Table 4-31 GITS\_OPR bit assignments**

Bits	Name	Function
[63:60]	LOCK_TYPE	Lock type supported: 0 = Track. 1 = Trial. 2 = ITS lock. 3 = ITS unlock. 4 = Track abort. 6 = LPI lock. 7 = LPI unlock. 8 = ITS unlock all.
[59:52]	-	Reserved.
[51:32]	DEVICE_ID	0-maximum DeviceID supported.
[31:16]	-	Reserved.
[15:0]	EVENT_ID	8192-maximum EventID supported.

#### 4.6.5 Operation Status Register, GITS\_OPSR

This register indicates cache lock status.

The GITS\_OPSR characteristics are:

##### Usage constraints

There are no usage constraints.

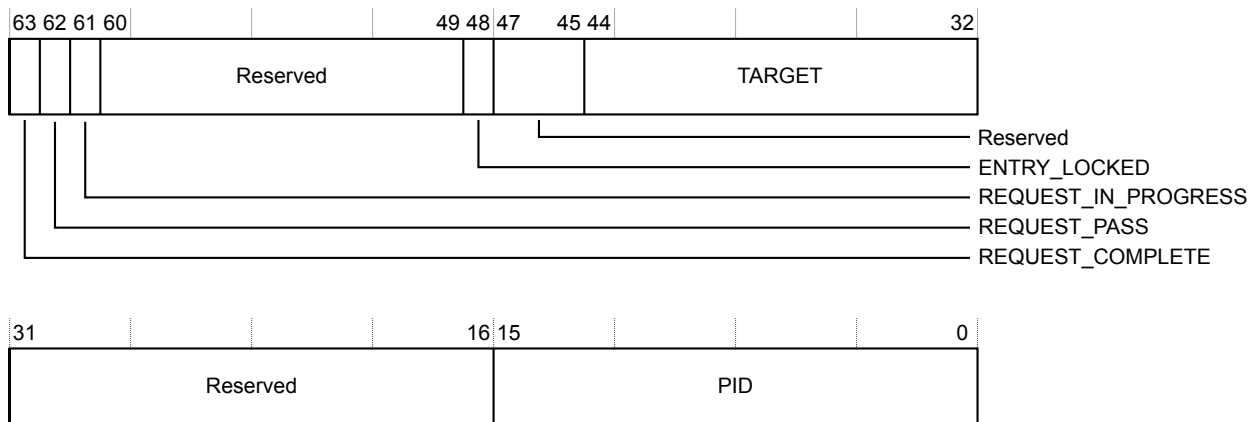
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.6 ITS control register summary on page 4-113](#).

The following figure shows the bit assignments.



**Figure 4-23 GITS\_OPSR bit assignments**

The following table shows the bit assignments.

**Table 4-32 GITS\_OPSR bit assignments**

Bits	Name	Function
[63]	REQUEST_COMPLETE	Request to GITS_OPR completed.
[62]	REQUEST_PASS	Request to GITS_OPR completed without error.
[61]	REQUEST_IN_PROGRESS	Translation in progress.
[60:49]	-	Reserved.
[48]	ENTRY_LOCKED	Locked entry in cache corresponds to request.
[47:45]	-	Reserved.
[44:32]	TARGET	Target of interrupt requested.
[31:16]	-	Reserved.
[15:0]	PID	Physical ID of interrupt requested.

#### 4.6.6 Configuration ID Register, GITS\_CFGID

This register returns the ID number of the ITS block.

The GITS\_CFGID characteristics are:

##### Usage constraints

There are no usage constraints.

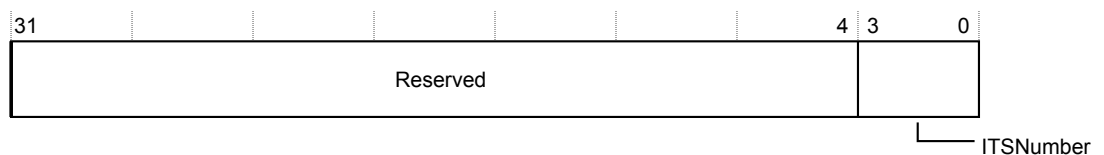
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.6 ITS control register summary on page 4-113](#).

The following figure shows the bit assignments.



**Figure 4-24 GITS\_CFGID bit assignments**

The following table shows the bit assignments.



**Table 4-33 GITS\_CFGID bit assignments**

Bits	Name	Function
[31:4]	-	Reserved.
[3:0]	ITSNumber	Returns the ITS block ID. The <code>its_id[7:0]</code> tie-off signal controls the ID value. Each ITS block must have a unique ID.

#### Related references

[A.6 Miscellaneous signals on page Appx-A-163.](#)

### 4.6.7 Peripheral ID2 Register, GITS\_PIDR2

This register defines the GIC architecture version with which the GIC-600 complies.

The GITS\_PIDR2 characteristics are:

#### Usage constraints

There are no usage constraints.

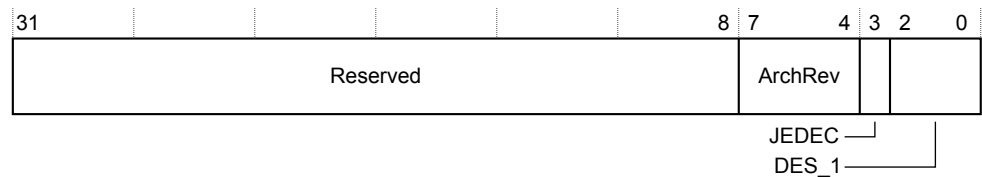
#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.6 ITS control register summary on page 4-113](#).

The following figure shows the bit assignments.



**Figure 4-25 GITS\_PIDR2 bit assignments**

The following table shows the bit assignments.

**Table 4-34 GITS\_PIDR2 bit assignments**

Bits	Name	Function
[31:8]	-	Reserved, RAZ.
[7:4]	ArchRev	Identifies the version of the GIC architecture with which the GIC-600 complies: <ul style="list-style-type: none"> <li>0x03 = GICv3.</li> </ul>
[3]	JEDEC	Indicates that a JEDEC-assigned JEP106 identity code is used.
[2:0]	DES_1	Bits[6:4] of the JEP106 identity code. Bits[3:0] of the JEP106 identity code are assigned to GITS_PIDR1.

#### Related information

[ARM® GICv3 and GICv4 Software Overview.](#)

## 4.7 ITS translation register summary

Interrupts to be translated by the GIC-600 Interrupt Translation Service are identified by EventIDs that are written to the ITS translation register GITS\_TRANSLATER.

For a description of the registers that are not specific to the GIC-600, see the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

---

**Note**

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This page does not exist in GIC-600 configurations that do not support LPis or that do not have an ITS.

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**Table 4-35 ITS translation register summary**

Offset	Name	Type	Reset	Description
0x0000-0x003C	-	-	-	Reserved
0x0040	GITS_TRANSLATER	WO	0x0001043B	ITS Translation Register
0x0044-0xFFFC	-	-	-	Reserved

## 4.8 GICT register summary

The GIC-600 trace and debug functions are controlled through registers identified with the prefix GICT.

### Note

The GICD\_SAC.GICTNS bit controls whether Non-secure software can access the GICT registers.

**Table 4-36 GICT register summary**

Offset	Name	Type	Width	Reset	Description
0x0000+n×64	GICT_ERR<n>FR	RO	64	64	<a href="#">4.8.1 Error Record Feature Register, GICT_ERR&lt;n&gt;FR on page 4-125</a>
0x0008+n×64	GICT_ERR<n>CTLR	RW	64	64	<a href="#">4.8.2 Error Record Control Register, GICT_ERR&lt;n&gt;CTLR on page 4-126</a>
0x0010+n×64	GICT_ERR<n>STATUS	RW	64	64	<a href="#">4.8.3 Error Record Primary Status Register, GICT_ERR&lt;n&gt;STATUS on page 4-127</a>
0x0018+n×64	GICT_ERR<n>ADDR	RW	64	64	<a href="#">4.8.4 Error Record Address Register, GICT_ERR&lt;n&gt;ADDR on page 4-128</a>
0x0020+n×64	GICT_ERR<n>MISC0	RW	64	64	<a href="#">4.8.5 Error Record Miscellaneous Register 0, GICT_ERR&lt;n&gt;MISC0 on page 4-129</a>
0x0028+n×64	GICT_ERR<n>MISC1	RW	64	64	<a href="#">4.8.6 Error Record Miscellaneous Register 1, GICT_ERR&lt;n&gt;MISC1 on page 4-135</a>
0xE000	GICT_ERRGSR	RO	64	64	Group Status Register
0xE008-0xE7FC	-	-	-	-	Reserved, RAZ/WI
0xE808-0xFFB8	-	-	-	-	Reserved, RAZ/WI
0xFFBC	GICT_ERRDEVARCH	RO	32	32	Device Architecture register
0xFFC0-0xFFC4	-	-	-	-	Reserved, RAZ/WI
0xFFC8	GICT_ERRIDR	RO	32	32	<a href="#">4.8.7 Error Record ID Register, GICT_ERRIDR on page 4-136</a>
0xFFCC	-	-	-	-	Reserved, RAZ/WI
0xFFD0	GICT_PIDR4	RO	32	0x00000044	Peripheral ID 4 Register
0xFFD4	GICT_PIDR5	RO	32	0x00000000	Peripheral ID 5 Register
0xFFD8	GICT_PIDR6	RO	32	0x00000000	Peripheral ID 6 Register
0xFFDC	GICT_PIDR7	RO	32	0x00000000	Peripheral ID 7 Register
0xFFE0	GICT_PIDR0	RO	32	0x00000095	Peripheral ID 0 Register
0xFFE4	GICT_PIDR1	RO	32	0x000000B4	Peripheral ID 1 Register
0xFFE8	GICT_PIDR2	RO	32	0x0000003B	<a href="#">4.8.8 Peripheral ID2 Register, GICT_PIDR2 on page 4-137</a>
0xFFEC	GICT_PIDR3	RO	32	0x00000000	Peripheral ID 3 Register
0xFFF0	GICT_CIDR0	RO	32	0x0000000D	Component ID 0 Register
0xFFF4	GICT_CIDR1	RO	32	0x000000F0	Component ID 1 Register

**Table 4-36 GICT register summary (continued)**

Offset	Name	Type	Width	Reset	Description
0xFFF8	GICT_CIDR2	RO	32	0x00000005	Component ID 2 Register
0xFFFC	GICT_CIDR3	RO	32	0x000000B1	Component ID 3 Register

The following table lists the error records for the various error conditions.

**Table 4-37 Error records**

Record	Description	Type	Syndrome	Syndrome data (GICT_ERR<n>MISC0.Data)
0	Software error in GICD programming	UEO <sup>ae</sup>	14, Illegal Access	Address, security, size, and direction
1	Correctable SPI RAM errors	CE <sup>af</sup>	7, Data value from associative memory	Counter, SPI number, bit
2	Uncorrectable SPI RAM errors	UER <sup>ag</sup>	7, Data value from associative memory	Counter, SPI number
3	Correctable SGI RAM errors	CE <sup>af</sup>	7, Control value from associative memory	Counter, core number, bit
4	Uncorrectable SGI RAM errors	UER <sup>ag</sup>	7, Control value from associative memory	Counter, core number
5	Correctable TGT cache errors	CE <sup>af</sup>	7, Control value from associative memory	Counter, core number, bit, and slot
6	Correctable TGT cache errors	UER <sup>ag</sup>	7, Control value from associative memory	Counter, core number, slot
7	Correctable PPI RAM errors	CE <sup>af</sup>	7, Control value from associative memory	Counter, core number, lowest PPI number, 0 for SGI, bit
8	Uncorrectable PPI RAM errors	UER <sup>ag</sup>	7, Control value from associative memory	Counter, core number, lowest PPI number, 0 for SGI
9	Correctable LPI RAM errors	CE <sup>af</sup>	7, Control value from associative memory	Counter, RAM, address, bit
10	Uncorrectable LPI RAM errors	UER <sup>ag</sup>	7, Control value from associative memory	Counter, RAM, address, bit
11	Correctable error from ITS RAM	CE <sup>af</sup>	6, Data value from associative memory	Counter, ITS, RAM, row, bit
12	Uncorrectable error from ITS RAM	UEO <sup>ae</sup>	6, Data value from associative memory	Counter, ITS, RAM, row
13 + ITSnum	Software error in ITS	UER <sup>ag</sup>	14, Illegal Access	As supplied by ITS 24-bit syndrome.

This section contains the following subsections:

- [4.8.1 Error Record Feature Register, GICT\\_ERR<n>FR on page 4-125.](#)
- [4.8.2 Error Record Control Register, GICT\\_ERR<n>CTLR on page 4-126.](#)
- [4.8.3 Error Record Primary Status Register, GICT\\_ERR<n>STATUS on page 4-127.](#)

<sup>ae</sup> Restartable error and contained.  
<sup>af</sup> Correctable error.  
<sup>ag</sup> Recoverable error.

- 4.8.4 Error Record Address Register, *GICT\_ERR<n>ADDR* on page 4-128.
- 4.8.5 Error Record Miscellaneous Register 0, *GICT\_ERR<n>MISC0* on page 4-129.
- 4.8.6 Error Record Miscellaneous Register 1, *GICT\_ERR<n>MISC1* on page 4-135.
- 4.8.7 Error Record ID Register, *GICT\_ERRIDR* on page 4-136.
- 4.8.8 Peripheral ID2 Register, *GICT\_PIDR2* on page 4-137.

#### 4.8.1 Error Record Feature Register, *GICT\_ERR<n>FR*

This register returns information about the ARMv8.2 RAS features that the GIC-600 implements.

The *GICT\_ERR<n>FR* characteristics are:

##### Usage constraints

If *GICD\_SAC.GICTNS* == 0, then only Secure software can access the contents of this register.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.

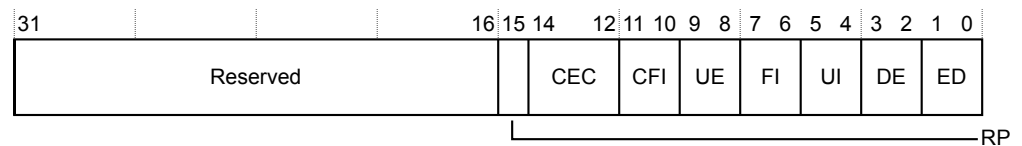


Figure 4-26 *GICT\_ERR<n>FR* bit assignments

The following table shows the bit assignments.

Table 4-38 *GICT\_ERR<n>FR* bit assignments

Bits	Name	Function
[31:16]	-	Reserved, RAZ.
[15]	RP	Repeat corrected error count: 0 = The GIC-600 does not implement a repeat corrected error counter.
[14:12]	CEC	Corrected error count: 0b000 = The GIC-600 does not implement a standard Corrected error counter in <i>GICT_ERR&lt;n&gt;MISC0</i> .
[11:10]	CFI	Corrected errors fault interrupt. Depending on the configuration, returns either: 0b00 = The GIC-600 does not provide a fault handling interrupt for corrected errors. 0b10 = The GIC-600 provides a controllable fault handling interrupt for corrected errors.
[9:8]	UE	Uncorrected error. Depending on the configuration, returns either: 0b00 = The GIC-600 does not provide an in-band uncorrected error reporting. 0b10 = The GIC-600 provides a controllable in-band uncorrected error reporting.
[7:6]	FI	Fault handling interrupt for uncorrected errors. Depending on the configuration, returns either: 0b00 = The GIC-600 does not provide a fault handling interrupt. 0b10 = The GIC-600 provides a controllable fault handling interrupt.

Table 4-38 GICT\_ERR<n>FR bit assignments (continued)

Bits	Name	Function
[5:4]	UI	Error recovery interrupt for uncorrected errors. Depending on the configuration, returns either: 0b00 = The GIC-600 does not provide an error recovery interrupt for uncorrected errors. 0b10 = The GIC-600 provides a controllable error recovery interrupt for uncorrected errors.
[3:2]	DE	Deferring of errors support: 0b00 = The GIC-600 does not support the deferring of errors.
[1:0]	ED	Uncorrected error reporting: 0b01 = Uncorrected error reporting is always enabled.

#### 4.8.2 Error Record Control Register, GICT\_ERR<n>CTLR

This register controls how interrupts are handled.

The GICT\_ERR<n>CTLR characteristics are:

##### Usage constraints

If GICD\_SAC.GICTNS == 0, then only Secure software can access the functions of this register.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.

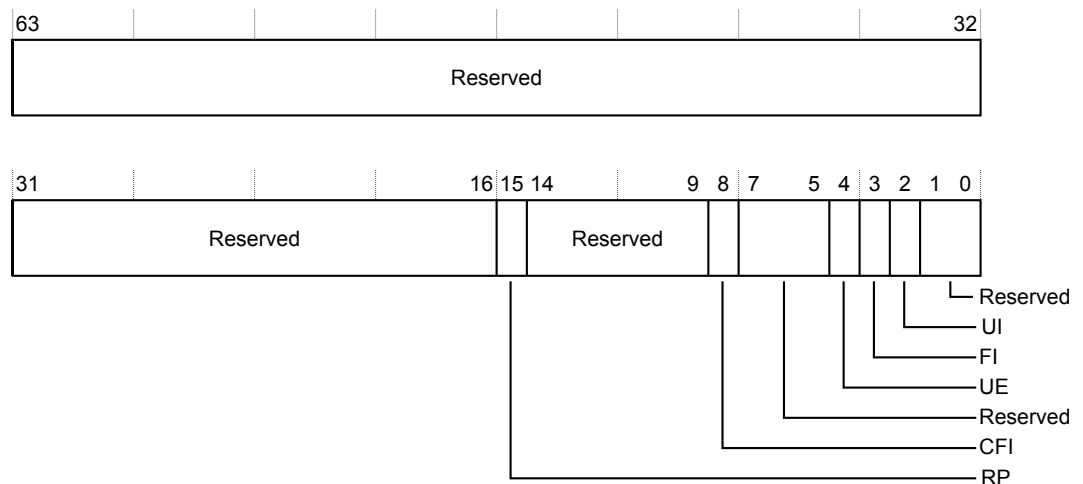


Figure 4-27 GICT\_ERR<n>CTLR bit assignments

The following table shows the bit assignments.

Table 4-39 GICT\_ERR<n>CTLR bit assignments

Bits	Name	Function
[63:16]	-	Reserved, RAZ.
[15]	RP	0 = An error response to a transaction is reported.
[14:9]	-	Reserved, RAZ.

**Table 4-39 GICT\_ERR<n>CTLR bit assignments (continued)**

Bits	Name	Function
[8]	CFI	Controls whether a corrected error generates a fault handling interrupt: 0 = The GIC-600 does not assert a fault handling interrupt for corrected errors. 1 = The GIC-600 asserts a fault handling interrupt when a corrected error occurs.
[7:5]	-	Reserved, RAZ.
[4]	UE	Uncorrected error. RAZ/WI for all records except GICT error record (0) else: 1 = Send external abort with transaction. 2 = Do not send external abort with transaction.
[3]	FI	Fault handling interrupt. SBZ on <i>Correctable Error</i> (CE) records else: 0 = Fault handling interrupt is not generated on any error. 1 = Fault handling interrupt is generated on all uncorrectable errors.
[2]	UI	Error recovery interrupt for uncorrected error. SBZ on CE records else: 0 = Error recovery interrupt is not generated on any error. 1 = Error recovery interrupt is generated on all uncorrectable errors.
[1:0]	-	Reserved, RAZ.

### 4.8.3 Error Record Primary Status Register, GICT\_ERR<n>STATUS

This register indicates information of recorded errors.

The GICT\_ERR<n>STATUS characteristics are:

#### Usage constraints

If GICD\_SAC.GICTNS == 0, then only Secure software can access the functions of this register.

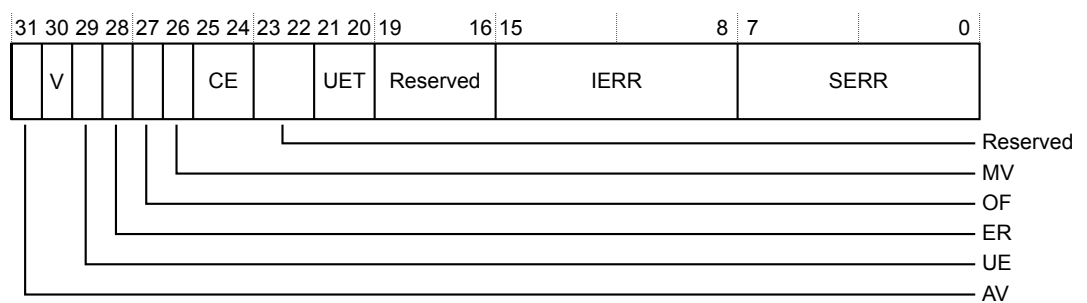
#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.



**Figure 4-28 GICT\_ERR<n>STATUS bit assignments**

The following table shows the bit assignments.

**Table 4-40 GICT\_ERR<n>STATUS bit assignments**

Bits	Name	Function
[31]	AV	Indicates if the address is valid: 0 = GICT_ERR<n>ADDR is not valid. 1 = GICT_ERR<n>ADDR contains an address that is associated with the highest priority error that this record stores. Only present in record 0.
[30]	V	Indicates if this register is valid: 0 = GICT_ERR<n>STATUS is not valid. 1 = GICT_ERR<n>STATUS is valid. One or more errors are recorded.
[29]	UE	Uncorrectable error bit. SBZ in <i>Correctable Error</i> (CE) records.
[28]	ER	Indicates that at least one error has been reported over ACE-Lite. Set for record 0 only, and only for accesses to corrupted data, and bad incoming access.
[27]	OF	Record has overflowed.
[26]	MV	Indicates if the GICT miscellaneous registers are valid: 0 = GICT_ERR<n>MISC0 and GICT_ERR<n>MISC1 are not valid. 1 = GICT_ERR<n>MISC0 and GICT_ERR<n>MISC1 are valid.
[25:24]	CE	Only in <i>Correctable Error</i> (CE) records: 0b00 = No CE recorded. 0b10 = At least one CE recorded.
[23:22]	-	Reserved, RAZ/WI.
[21:20]	UET	RES0 unless UE == 1, in which case: 0b10 = UEO. 0b11 = UER.
[19:16]	-	Reserved, RAZ/WI.
[15:8]	IERR	IMPLEMENTATION-DEFINED error code: This field is RO if one value is specified. Returns the summary table information.
[7:0]	SERR	Architecturally-defined primary error code: This field is RO if one value is specified. Returns the summary table information.

#### 4.8.4 Error Record Address Register, GICT\_ERR<n>ADDR

This register contains the address and security status of the write. This register is only present for GICT software record 0.

The GICT\_ERR<n>ADDR characteristics are:



**Usage constraints**

If GICD\_SAC.GICTNS == 0, then only Secure software can access the functions of this register.

Ignores writes if ERR<n>STATUS.AV == 1.

All bits are RAZ/WI if GICT\_ERR<n>STATUS.IERR = 0, 12, or 13.

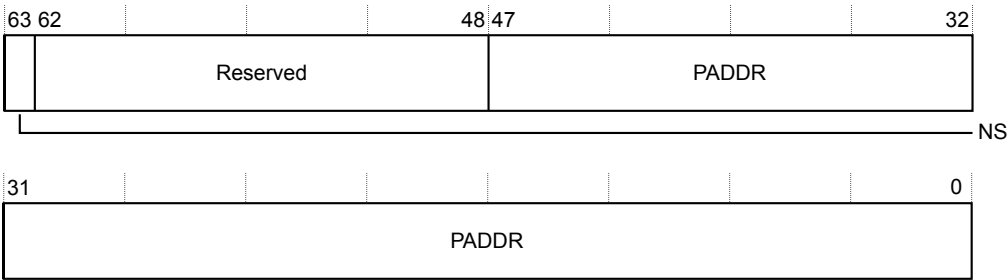
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.



**Figure 4-29** GICT\_ERR<n>ADDR bit assignments

The following table shows the bit assignments.

**Table 4-41** GICT\_ERR<n>ADDR bit assignments

Bits	Name	Function
[63]	NS	Non-secure attribute: 0 = The address is Secure. 1 = The address is Non-secure.
[62:48]	-	Reserved, RAZ/WI.
[47:0]	PADDR	The error address.

**4.8.5 Error Record Miscellaneous Register 0, GICT\_ERR<n>MISC0**

This register contains the Corrected error counter and information that assists with identifying the RAM in which the error was detected.

The GICT\_ERR<n>MISC0 characteristics are:

**Usage constraints**

If GICD\_SAC.GICTNS == 0, then only Secure software can access the functions of this register. If GICT\_ERR<n>STATUS.MV == 1, then the GICT\_ERR<n>MISC0 ignores writes to the Data field.

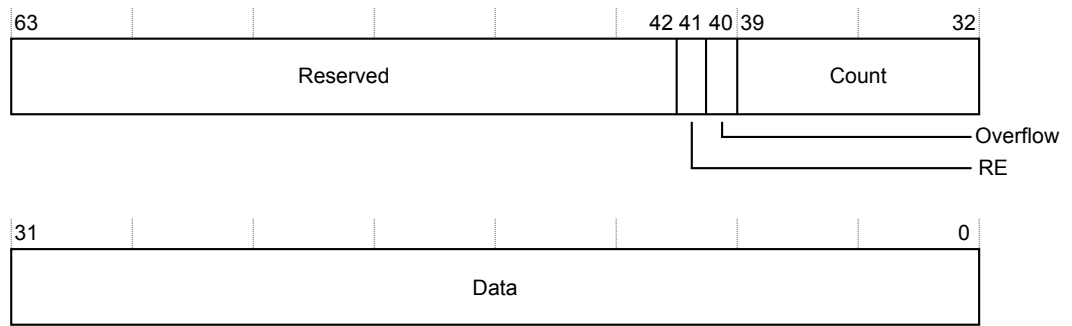
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.



**Figure 4-30 GICT\_ERR<n>MISC0 bit assignments**

The following table shows the bit assignments.

**Table 4-42 GICT\_ERR<n>MISC0 bit assignments**

Bits	Name	Function
[63:42]	-	Reserved, RAZ.
[41]	RE	Rounding Error. The Rounding Error counter is under-reporting.
[40]	Overflow	Sticky overflow bit: 0 = Counter has not overflowed. 1 = Counter has overflowed. If the corrected fault handling interrupt is enabled, then the GIC-600 generates a fault handling interrupt.
[39:32]	Count	Corrected error count. Error counter is not 0 or is more than 134. Incremented for each corrected error that does not match the recorded syndrome.
[31:0]	Data	Information associated with the error. See the following table.

The following table shows the Data field encoding for each error record and syndrome.

**Table 4-43 Data field encoding**

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Software Error (0)	0x00, SYN_ACE_BAD Illegal ACE-Lite Slave Access.	0xE	AccessRnW, bit[12] AccessSparse, bit[11] AccessSize, bits[10:8] AccessLength, bits[7:0]
Software Error (0)	0x01, SYN_PPI_PWRDWN Attempt to access a powered down Redistributor.	0xF	Redistributor, bits[24:16] Core, bits[8:0]

**Table 4-43 Data field encoding (continued)**

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Software Error (0)	0x02, SYN_PPI_PWRCHANGE  Attempt to power down Redistributor rejected.	0xF	Redistributor, bits[24:16]  Core, bits[8:0]
Software Error (0)	0x03, SYN_GICR_ARE  Attempt to access GICR or GICD registers in mode that cannot work.	0xF	Core, bits[8:0]
Software Error (0)	0x04, sdsd_ACC  Attempt to reprogram PROPBASE registers to a value that is not accepted because another value is already in use.	0xF	Core, bits[8:0]
Software Error (0)	0x05, SYN_PENDBASE_ACC  Attempt to reprogram PENDBASE registers to a value that is not accepted because another value is already in use.	0xF	Core, bits[8:0]
Software Error (0)	0x06, SYN_LPI_CLR  Attempt to reprogram ENABLE_LPI when not already enabled and not asleep.	0xF	Core, bits[8:0]
Software Error (0)	0x07, SYN_WAKER_CHANGE  Attempt to change GICR_WAKER abandoned due to handshake rules.	0xF	Core, bits[8:0]
Software Error (0)	0x08, SYN_SLEEP_FAIL  Attempt to put GIC to sleep failed because cores are not fully asleep.	0xF	Core, bits[8:0]
Software Error (0)	0x09, SYN_PGE_ON_QUIESCE  Core put to sleep before its Group enables were cleared.	0xF	Core, bits[8:0]
Software Error (0)	0x0A, SYN_GICD_CTLR  Attempt to update GICD_CTLR was prevented due to RWP or Group enable restrictions.	0xF	Data, bits[7:0]
Software Error (0)	0x10, SYN_SGI_NO_TGT  SGI sent with no valid destinations.	0xE	Core, bits[8:0]
Software Error (0)	0x11, SYN_SGI_CORRUPTED  SGI was corrupted and has not taken effect.	0x6	Core, bits[8:0]

Table 4-43 Data field encoding (continued)

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Software Error (0)	0x12, SYN_GICR_CORRUPTED  Data was read from the GICR register space that has encountered an uncorrectable error.	0x6	GITS_ERR0ADDR is populated.
Software Error (0)	0x13, SYN_GICD_CORRUPTED  Data was read from the GICD register space that has encountered an uncorrectable error.	0x6	GITS_ERR0ADDR is populated.
Software Error (0)	0x14, SYN_ITS_OFF  Data was read from an ITS that was powered down.	0xF	GITS_ERR0ADDR is populated.
Software Error (0)	0x19, SYN_SPI_OOR  Access to a non-implemented SPI using (SET CLR)SPI.	0xE	ID, bits[9:0]
Software Error (0)	0x1A, SYN_SPI_NO_DEST_TGT  A SPI has no legal target destinations.	0xF	ID, bits[9:0]
Software Error (0)	0x1B, SYN_SPI_NO_DEST_1OFN  A 1 of N SPI cannot be delivered due to bad DPG/GICR_CLASS programming.	0xF	ID, bits[9:0]
Software Error (0)	0x1C, SYN_COL_OOR  A collator message is received for a non-implemented SPI, or is larger than the number of owned SPIs in a multichip configuration.	0xF	ID, bits[9:0]
Software Error (0)	0x1D, SYN_DEACT_IN  A Deactivate to a non-existent SPI, or with incorrect groups set. Deactivates to LPI and non-existent PPI are not reported.	0xE	None
Software Error (0)	0x1E, SYN_SPI_CHIP_OFFLINE  An attempt was made to send a SPI to an offline chip.	0xF	ID, bits[9:0]
Software Error (0)	0x20, SYN_PUP_REJ  A multichip power update was rejected.	0xF	None
Software Error (0)	0x28, SYN_ITS_REG_SET_OOR  An attempt was made to set an <i>Out Of Range</i> (OOR) interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16] Data, bits[15:0]

**Table 4-43 Data field encoding (continued)**

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Software Error (0)	0x29, SYN_ITS_REG_CLR_OOR  An attempt was made to clear an OOR interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16]  Data, bits[15:0]
Software Error (0)	0x2A, SYN_ITS_REG_INV_OOR  An attempt was made to invalidate an OOR interrupt. Only valid when GICR LPI injection registers are supported.	0xE	Core, bits[24:16]  Data, bits[15:0]
Software Error (0)	0x2B, SYN_ITS_REG_SET_ENB  An attempt was made to set an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16]  Data, bits[15:0]
Software Error (0)	0x2C, SYN_ITS_REG_CLR_ENB  An attempt was made to clear an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16]  Data, bits[15:0]
Software Error (0)	0x2D, SYN_ITS_REG_INV_ENB  An attempt was made to invalidate an interrupt when LPIs are not enabled. Only valid when GICR LPI injection registers are supported.	0xF	Core, bits[24:16]  Data, bits[15:0]
Software Error (0)	0x40, SYN_LPI_PROP_READ_FAIL  An attempt was made to read properties for a single interrupt where an error response was received with the data.	0x12	Target, bits[31:16]  ID, bits[15:0]
Software Error (0)	0x41, SYN_PT_PROP_READ_FAIL  An attempt was made to read properties for a block of interrupts where an error response was received with the data.	0x12	Target, bits[31:16]  ID, bits[15:0]
Software Error (0)	0x42, SYN_PT_COARSE_MAP_READ_FAIL  An attempt was made to read the coarse map for a target where an error response was received with the data.	0x12	Target, bits[31:16]

**Table 4-43 Data field encoding (continued)**

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Software Error (0)	0x43, SYN_PT_COARSE_MAP_WRITE_FAIL  An attempt was made to write the coarse map for a target with an error received with the write response.	0x12	Target, bits[31:16]
Software Error (0)	0x44, SYN_PT_TABLE_READ_FAIL  An attempt was made to read a block of interrupts from a Pending table where an error response was received with the data.	0x12	Target, bits[31:16] ID, bits[15:0]
Software Error (0)	0x45, SYN_PT_TABLE_WRITE_FAIL  An attempt was made to write back a block of interrupts from a Pending table with an error received with the write response.	0x12	Target, bits[31:16] ID, bits[15:0]
Software Error (0)	0x46, SYN_PT_SUB_TABLE_READ_FAIL  An attempt was made to read a sub-block of interrupts from a Pending table where an error response was received with the data.	0x12	Target, bits[31:16] ID, bits[15:0]
Software Error (0)	0x47, SYN_PT_TABLE_WRITE_FAIL_BYTE  An attempt was made to write back a sub- block of interrupts from a Pending table with an error received with the write response.	0x12	Target, bits[31:16] ID, bits[15:0]
Correctable SPI RAM errors (1)	0x00	0x7	Bit location, $\log_2(\text{width})$ ID, $[\log_2(\text{SPI}) - 1:0]$
Uncorrectable SPI RAM errors (2)	0x00	0x7	ID, $\log_2(\text{SPI}) - 1:0]$
Correctable SGI RAM errors (3)	0x00	0x7	Bit location, $\log_2(\text{width})$ Address, $\text{ceiling}(\text{core} / 16) \times 16$
Uncorrectable SGI RAM errors (4)	0x00	0x7	Address - $\text{ceiling}(\text{core} / 16) \times 16$
Correctable PPI RAM errors (7)	0x00	0x7	Bit location – $\log_2(\text{width})$ Address, $\text{ceiling}(\text{core} / 16) \times 16$

**Table 4-43 Data field encoding (continued)**

Record	GICT_ERR<n>STATUS.IERR (syndrome)	GICT_ERR<n>STATUS.SERR	Value and description of GICT_ERR<n>MISC0.Data (Other bits RES0)  Always packed from 0 (lowest = 0)
Uncorrectable PPI RAM errors (8)	0x00	0x7	Address, ceiling(core / 16) × 16
Correctable LPI RAM errors (9)	0x00	0x7	Bit location, bit[15+] Lock, bit[14] Pending, bits[13:12] Channel, bits[11:10] Address, bits[9:0]
Uncorrectable LPI RAM errors (10)	0x00	0x7	Lock, bit[14] Pending, bits[13:12] Channel, bits[11:10] Address, bits[9:0]  The corresponding data is stored in GICT_ERR<n>MISC1.
Correctable error from ITS RAM (11)	0x00	0x6	Bit location, bit[8] Address, bit[12] RAM, bit[2] ITS, log <sub>2</sub> (ITS)
Uncorrectable error from ITS RAM (12)	0x00	0x6	Address, bit[12] RAM, bit[3] ITS, log <sub>2</sub> (ITS)
Software error in ITS (13+)	0x00, Architectural 0x01, NonArchitectural	0xE	ITS 24-bit syndrome

#### 4.8.6 Error Record Miscellaneous Register 1, GICT\_ERR<n>MISC1

This register contains the data value of an uncorrectable error in the LPI RAM, or ITS software information for one of 13, or more, error records. The GIC-600 only supports a single MISC1 register, so n = 10, and therefore this register is identified as GICT\_ERR10MISC1.

The GICT\_ERR10MISC1 characteristics are:

##### Usage constraints

If GICD\_SAC.GICTNS = 0, then only Secure software can access the functions of this register.

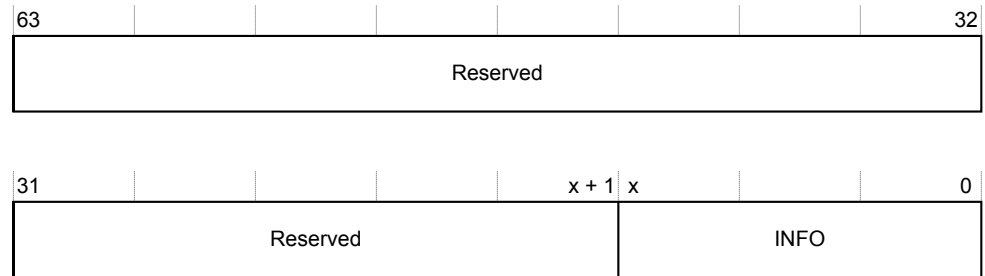
If GICT\_ERR10STATUS.MV = 1, then GICT\_ERR10MISC1 ignores writes.

### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.8 GICT register summary on page 4-123](#).



**Figure 4-31 GICT\_ERR10MISC1 bit assignments**

The following table shows the bit assignments.

**Table 4-44 GICT\_ERR10MISC1 bit assignments**

Bits	Name	Function
[63:x + 1]	-	Reserved, RAZ.
[x:0]	INFO	Value represents either data that is written to the LPI RAM when an uncorrectable error is detected, or ITS software information for one of 13, or more, error records. The value x depends on the width of the LPI RAM, which is set during configuration of the GIC-600.

### 4.8.7 Error Record ID Register, GICT\_ERRIDR

This register returns information about the configuration of the GIC-600 GICT such as whether an LPI or ITS is available.

The GICT\_ERRIDR characteristics are:

#### Usage constraints

If GICD\_SAC.GICTNS == 0, then only Secure software can read this register.

### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.8 GICT register summary on page 4-123](#).

The following table shows the bit assignments.

**Table 4-45 GICT\_ERRIDR bit assignments**

Bits	Name	Function
[31:16]	-	Reserved, RAZ.
[15:0]	NUM	Identifies the device configuration: 10 = No LPI available. 12 = LPI available but no ITS. 14 = LPI available and 1 × ITS. 15 = LPI available and 2 × ITS. 16 = LPI available and 3 × ITS.



4.8.8 Peripheral ID2 Register, GICT\_PIDR2

This register defines the GIC architecture version with which the GIC-600 complies.

The GICT\_PIDR2 characteristics are:

Usage constraints

There are no usage constraints.

Configurations

Available in all GIC-600 configurations.

Attributes

See the [4.8 GICT register summary on page 4-123](#).

The following figure shows the bit assignments.

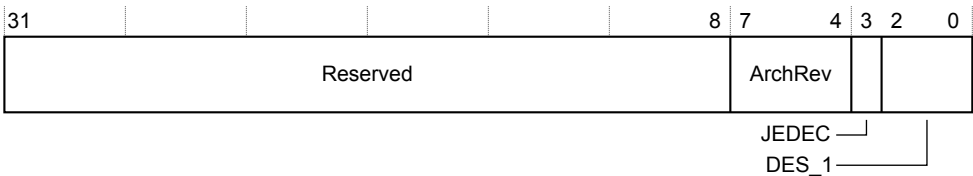


Figure 4-32 GICT\_PIDR2\_bit assignments

The following table shows the bit assignments.

Table 4-46 GICT\_PIDR2 bit assignments

Bits	Name	Function
[31:8]	-	Reserved, RAZ.
[7:4]	ArchRev	Identifies the version of the GIC architecture with which the GIC-600 complies: <ul style="list-style-type: none"><li>0x03 = GICv3.</li></ul>
[3]	JEDEC	Indicates that a JEDEC-assigned JEP106 identity code is used.
[2:0]	DES_1	Bits[6:4] of the JEP106 identity code. Bits[3:0] of the JEP106 identity code are assigned to GICT_PIDR1.

## 4.9 GICP register summary

The GIC-600 Performance Monitoring Unit functions are controlled through registers identified with the prefix GICP.

**Table 4-47 GICP register summary**

Offset	Name	Type	Width	Reset	Description
$0x000 + (n \times 4)$	GICP_EVCNTR <sub>n</sub>	RW	32	UNKNOWN	<a href="#">4.9.1 Event Counter Registers, GICP_EVCNTR<sub>n</sub> on page 4-139</a>
$0x400 + (n \times 4)$	GICP_EVTYPEN <sub>n</sub> <sup>ah</sup>	RW	32	UNKNOWN	<a href="#">4.9.2 Event Type Configuration Registers, GICP_EVTYPEN<sub>n</sub> on page 4-139</a>
$0x600 + (n \times 4)$	GICP_SVR <sub>n</sub> <sup>ah</sup>	RO	32	UNKNOWN	<a href="#">4.9.3 Shadow Value Registers, GICP_SVR<sub>n</sub> on page 4-143</a>
$0xA00 + (n \times 4)$	GICP_FR <sub>n</sub> <sup>ah</sup>	RW	32	UNKNOWN	<a href="#">4.9.4 Filter Registers, GICP_FR<sub>n</sub> on page 4-143</a>
0xC00	GICP_CNTENSET0	RW	64	0	<a href="#">4.9.5 Counter Enable Set Register, GICP_CNTENSET0 on page 4-144</a>
0xC20	GICP_CNTENCLR0	RW	64	0	<a href="#">4.9.6 Counter Enable Clear Register 0, GICP_CNTENCLR0 on page 4-145</a>
0xC40	GICP_INTENSET0	RW	64	0	<a href="#">4.9.7 Interrupt Contribution Enable Set Register 0, GICP_INTENSET0 on page 4-145</a>
0xC60	GICP_INTENCLR0	RW	64	0	<a href="#">4.9.8 Interrupt Contribution Enable Clear Register 0, GICP_INTENCLR0 on page 4-146</a>
0xC80	GICP_OVSCLR0	RW	64	0	<a href="#">4.9.9 Overflow Status Clear Register 0, GICP_OVSCLR0 on page 4-147</a>
0xCC0	GICP_OVSSET0	RW	64	0	<a href="#">4.9.10 Overflow Status Set Register 0, GICP_OVSSET0 on page 4-147</a>
0xD88	GICP_CAPR	WO	32	-	<a href="#">4.9.11 Counter Shadow Value Capture Register, GICP_CAPR on page 4-148</a>
0xE00	GICP_CFGR	RO	32	0x00401F04	<a href="#">4.9.12 Configuration Information Register, GICP_CFGR on page 4-149</a>
0xE04	GICP_CR	RW	32	0	<a href="#">4.9.13 Control Register, GICP_CR on page 4-149</a>
0xFCC	GICP_PMDEVTYPE	RO	32	0x00000056	-
0xFD0	GICP_PIDR4	RO	32	0x00000044	Peripheral ID 4 Register
0xFD4	GICP_PIDR5	RO	32	0x00000000	Peripheral ID 5 Register
0xFD8	GICP_PIDR6	RO	32	0x00000000	Peripheral ID 6 Register
0xFDC	GICP_PIDR7	RO	32	0x00000000	Peripheral ID 7 Register
0xFE0	GICP_PIDR0	RO	32	0x00000096	Peripheral ID 0 Register
0xFE4	GICP_PIDR1	RO	32	0x000000B4	Peripheral ID 1 Register
0xFE8	GICP_PIDR2	RO	32	0x0000003B	<a href="#">4.9.14 Peripheral ID2 Register, GICP_PIDR2 on page 4-150</a>
0xFEC	GICP_PIDR3	RO	32	0x00000000	Peripheral ID 3 Register
0xFF0	GICP_CIDR0	RO	32	0x0000000D	Component ID 0 Register

<sup>ah</sup> n = 0-4.

**Table 4-47 GICP register summary (continued)**

Offset	Name	Type	Width	Reset	Description
0xFF4	GICP_CIDR1	RO	32	0x00000090	Component ID 1 Register
0xFF8	GICP_CIDR2	RO	32	0x00000005	Component ID 2 Register
0xFFC	GICP_CIDR3	RO	32	0x000000B1	Component ID 3 Register

This section contains the following subsections:

- [4.9.1 Event Counter Registers, GICP\\_EVCNTRn](#) on page 4-139.
- [4.9.2 Event Type Configuration Registers, GICP\\_EVTYPERN](#) on page 4-139.
- [4.9.3 Shadow Value Registers, GICP\\_SVRn](#) on page 4-143.
- [4.9.4 Filter Registers, GICP\\_FRn](#) on page 4-143.
- [4.9.5 Counter Enable Set Register, GICP\\_CNTENSET0](#) on page 4-144.
- [4.9.6 Counter Enable Clear Register 0, GICP\\_CNTENCLR0](#) on page 4-145.
- [4.9.7 Interrupt Contribution Enable Set Register 0, GICP\\_INTENSET0](#) on page 4-145.
- [4.9.8 Interrupt Contribution Enable Clear Register 0, GICP\\_INTENCLR0](#) on page 4-146.
- [4.9.9 Overflow Status Clear Register 0, GICP\\_OVSCLR0](#) on page 4-147.
- [4.9.10 Overflow Status Set Register 0, GICP\\_OVSSET0](#) on page 4-147.
- [4.9.11 Counter Shadow Value Capture Register, GICP\\_CAPR](#) on page 4-148.
- [4.9.12 Configuration Information Register, GICP\\_CFGR](#) on page 4-149.
- [4.9.13 Control Register, GICP\\_CR](#) on page 4-149.
- [4.9.14 Peripheral ID2 Register, GICP\\_PIDR2](#) on page 4-150.

#### 4.9.1 Event Counter Registers, GICP\_EVCNTRn

These registers contain the values of event counter n. The GIC-600 supports five counters, n = 0-4.

The GICP\_EVCNTRn characteristics are:

##### Usage constraints

There are no usage constraints.

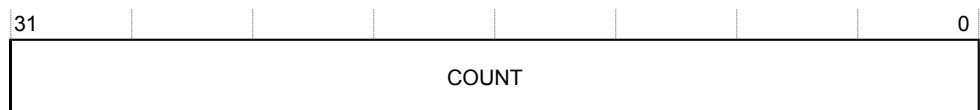
##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.9 GICP register summary](#) on page 4-138.

The following figure shows the bit assignments.



**Figure 4-33 GICP\_EVCNTRn bit assignments**

The following table shows the bit assignments.

**Table 4-48 GICP\_EVCNTRn bit assignments**

Bits	Name	Function
[31:0]	COUNT	Counter value. If the counter is enabled, the counter value increments when an event matching GICP_EVTYPERN.EVENT occurs.

#### 4.9.2 Event Type Configuration Registers, GICP\_EVTYPERN

These registers configure which events are counted by the event counter n. The GIC-600 supports five counters, n = 0-4.

The GICP\_EVTYPERN characteristics are:

**Usage constraints**

There are no usage constraints.

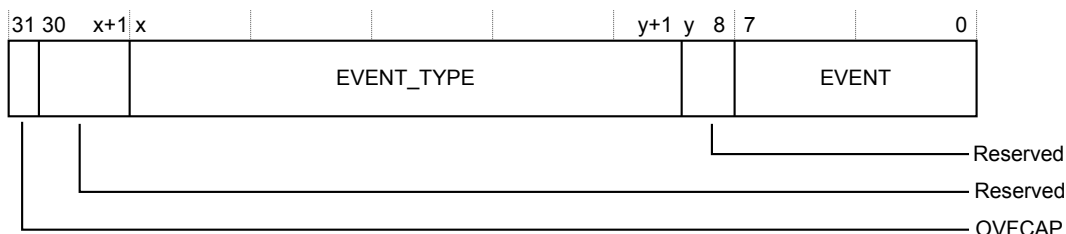
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary](#) on page 4-138.

The following figure shows the bit assignments.



**Figure 4-34 GICP\_EVTYPERN bit assignments**

The following table shows the bit assignments.

**Table 4-49 GICP\_EVTYPERN bit assignments**

Bits	Name	Function
[31]	OVFCAP	When set to 1, an overflow of counter n triggers a capture if GICP_CAPR.CAPTURE is set.
[30:x + 1]	-	Reserved.
[x:y + 1]	EVENT_TYPE	Event tracking type: 0b00 = Count events. 0b01 = AccumulateEvent. 0b10 = MaximumEvent. 0b11 = Reserved.
[y:8]	-	Reserved.
[7:0]	EVENT	Event identifier. All events reset to an UNKNOWN value. Registers corresponding to unimplemented counters are RES0. See the following table.

The following table shows the events that the GIC can count.

**Table 4-50 EVENT field encoding**

Event	Description	EventID	Filter
CLK	Clock cycle.	0x0	None
CLK_NG	Clock cycle that prevents Q-Channel clock gating.	0x1	None
-	Reserved.	0x2-0x3	-
DN_MSG	Downstream message to core excluding PPIs.	0x4	Target
DN_SET	Set to core SPIs and LPIs.	0x5	Target/ID range

**Table 4-50 EVENT field encoding (continued)**

Event	Description	EventID	Filter
DN_SET1OFN	Set to core, which is a 1 of N interrupts.	0x6	Target/ID range
-	Reserved.	0x7	-
UP_MSG	Upstream message from core.	0x8	Target
UP_ACT	Upstream Activate.	0x9	Target/ID range
UP_REL	Upstream Release.	0xA	Target/ID range
UP_ACTREL	Upstream Activate or Release.	0xB	Target/ID range
UP_SET_COMP	A Set followed by Activate. This counts the set and then decrements on Release.	0xC	Target/ID range
UP_DEACT	Upstream Deactivate. SPIs only.	0xD	Target/ID range
SGI_BRD	Broadcast SGI messages. Target = source.	0x10	Target/ID range
SGI_TAR	Targeted SGI messages. Target = source.	0x11	Target/ID range
SGI_ALL	All SGI messages. Target = source.	0x12	Target/ID range
SGI_ACC	Accepted SGI. Target = source.	0x13	Target/ID range
SGI_BRD_CC_IN	Broadcast SGI message from cross-chip.	0x14	ID range
SGI_TAR_CC_IN	Targeted SGI Message from cross-chip.	0x15	ID range
SGI_TAR_CC_OUT	Targeted SGI sent cross-chip.	0x16	Chip/ID range
ITS_NLL_LPI	Incoming LPI.	0x20	Target/ID range/ITS
ITS_LL_LPI	Incoming low latency LPI.	0x21	Target/ID range/ITS
ITS_LPI	Incoming LPI (or low latency).	0x22	Target/ID range/ITS
ITS_LPI_CMD	Incoming LPI command.	0x23	Target/ID range/ITS
ITS_DID_MISS	Number of DeviceID cache misses.	0x24	Target/ID range/ITS
ITS_VID_MISS	Number of EventID cache misses.	0x25	Target/ID range/ITS
ITS_COL_MISS	Number of Collection cache misses.	0x26	Target/ID range/ITS
ITS_LAT	Latency of the ITS transaction.	0x27	Target/ID range/ITS
ITS_MPFA	Number of free slots during translation.	0x28	Target/ID range/ITS
LPI_CC_OUT	LPI sent cross-chip.	0x29	ID range/Chip
LPI_CMD_CC_OUT	LPI command sent cross-chip.	0x2A	ID range/Chip
LPI_CC_IN	LPI coming in from cross-chip.	0x2B	Target/ID range/Chip
LPI_CMD_CC_IN	LPI command coming in from cross-chip.	0x2C	Target/ID range/Chip
LPI_OWN_STORED	LPI stored in own location.	0x30	-
LPI_OOL_STORED	LPI stored out of location.	0x31	-
LPI_HIT_EN	LPI property read cache hit enabled. Uses the filter from counter 0 only.	0x32	Target/ID range
LPI_HIT_DIS	LPI property read cache hit disabled. Uses the filter from counter 0 only.	0x33	Target/ID range
LPI_HIT	LPI property read cache hit. Uses the filter from counter 0 only.	0x34	Target/ID range

**Table 4-50 EVENT field encoding (continued)**

Event	Description	EventID	Filter
LPI_MATCH	LPI coalesced. Uses the filter from counter 0 only.	0x35	Target/ID range
LPI_FAS	Number of slots free on new LPI.	0x36	None
LPI_PROP_EN	Enabled LPI property fetch. Uses the filter from counter 0.	0x37	Target/ID range
LPI_PROP_DIS	Disabled LPI property fetch. Uses the filter from counter 0.	0x38	Target/ID range
LPI_PROP	LPI property fetch. Uses the filter from counter 0.	0x39	Target/ID range
LPI_COMP_INC_MERGE	Indicates that an LPI has completed. Uses the filter from counter 0.	0x3A	Target/ID range
SPI_COL_MSG	New message from SPI Collator.	0x50	ID range
SPI_ENABLED	SPI enabled (new SPI or register access if pending).	0x51	ID range
SPI_DISABLED	SPI disabled (new SPI that is disabled or register access if pending).	0x52	ID range
SPI_PENDING_SET	New SPI pending valid.	0x53	ID range
SPI_PENDING_CLR	SPI pending bit cleared.	0x54	ID range
SPI_MATCH	Collated edge-based SPI. Excludes collation in the collator.	0x55	ID range
SPI_COMP	Indicates completion of a SPI either by an accepted set, or being disabled.	0x56	ID range
SPI_CC_IN	SPI from remote chip.	0x57	ID range
SPI_CC_OUT	SPI sent to remote chip.	0x58	ID range
SPI_CC_DEACT	SPI deactivate message sent.	0x5A	ID range
PT_IN_EN	Enabled interrupt written to Pending table.	0x60	Target/ID range
PT_IN_DIS	Disabled interrupt written to Pending table.	0x61	Target/ID range
PT_PRI	Priority of interrupt written to Pending table.	0x62	Target/ID range
PT_IN	Interrupt written to Pending table.	0x63	Target/ID range
PT_MATCH	Interrupt already set in Pending table.	0x64	Target/ID range
PT_OUT_EN	Enabled interrupt taken out of Pending table (also covered PT_MATCH when enabled).	0x65	Target/ID range
PT_OUT_DIS	Disabled interrupt taken out of Pending table (also covered PT_MATCH when disabled).	0x66	Target/ID range
PT_OUT	Disabled interrupt taken out of Pending table (also covered PT_MATCH).	0x67	Target/ID range
PT_BLOCK_SENT_CC	Pending table block that is sent as part of MOVALL.	0x68	None
SPI_CC_LATENCY	SPIs outstanding.	0x70	Chip
SPI_CC_LAT_WAIT	SPIs waiting to be sent.	0x71	Chip
LPI_CC_LATENCY	LPIs outstanding.	0x72	Chip
LPI_CC_LAT_WAIT	LPI waiting to be sent.	0x73	Chip
SGI_CC_LATENCY	SGIs outstanding.	0x74	Chip
SGI_LAT_WAIT	SGIs waiting to be sent.	0x75	Chip

**Table 4-50 EVENT field encoding (continued)**

Event	Description	EventID	Filter
ACC	Accumulate Counter(n - 2) - Counter(n - 1) every cycle. Prevents clock gating.	0x80	None
OFLOW	Overflow of Counter n - 1.	0x81	None

### 4.9.3 Shadow Value Registers, GICP\_SVRn

These registers contain the shadow value of event counter n. The GIC-600 supports five counters, n = 0-4.

The GICP\_SVRn characteristics are:

## Usage constraints

There are no usage constraints.

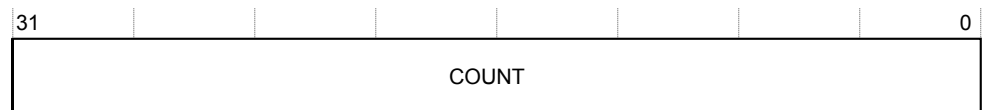
## Configurations

Available in all GIC-600 configurations.

## Attributes

See the [4.9 GICP register summary](#) on page 4-138.

The following figure shows the bit assignments.



**Figure 4-35 GLCP\_SVRn bit assignments**

The following table shows the bit assignments.

### Table 4-51 GICP\_SVRn bit assignments

Bits	Name	Function
[31:0]	COUNT	<p>Captured counter value.</p> <p>This field holds the captured counter values of the corresponding entry in GICP_EVCNTRn.</p>

#### 4.9.4 Filter Registers, GICP\_FRn

These registers configure the filtering of event counter  $n$ . The GIC-600 supports five counters,  $n = 0-4$ .

The GICP FRn characteristics are:

## Usage constraints

There are no usage constraints.

## Configurations

Available in all GIC-600 configurations.

## Attributes

See the *4.9 GICP register summary* on page 4-138.

The following figure shows the bit assignments.

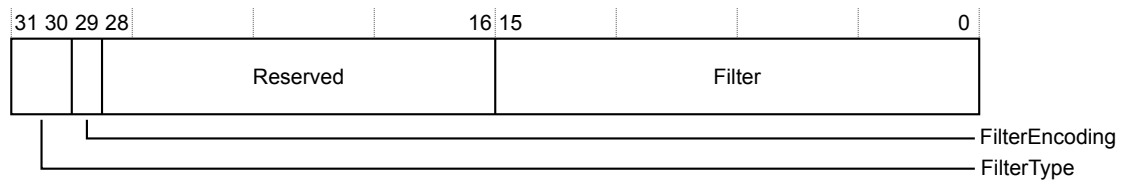


Figure 4-36 GICP\_FRn bit assignments

The following table shows the bit assignments.

Table 4-52 GICP\_FRn bit assignments

Bits	Name	Function
[31:30]	FilterType	Filter type: 0b00 = Filter on core. 0b01 = Filter on INTID. 0b10 = Filter on chip or ITS. 0b11 = Reserved, no effect.
[29]	FilterEncoding	0 = Filter on range. 1 = Filter on an exact match.
[28:16]	-	Reserved.
[15:0]	Filter	If the corresponding GICP_EVTYPERn.EVENT indicates an event that cannot be filtered, then the value in this register is ignored.  When the corresponding FilterEncoding == 1, counter n counts events that are only associated with an exact match of the FilterType.  When FilterEncoding == 0, this field is encoded so that the least-significant bit0 indicates the uppermost of a contiguous span of least-significant FilterType bits that are ignored for the purposes of matching.

#### 4.9.5 Counter Enable Set Register, GICP\_CNTENSET0

These registers contain the enables for each event counter. The GIC-600 supports five event counters.

The GICP\_CNTENSET0 characteristics are:

##### Usage constraints

There are no usage constraints.

##### Configurations

Available in all GIC-600 configurations.

##### Attributes

See the [4.9 GICP register summary](#) on page 4-138.

The following figure shows the bit assignments.

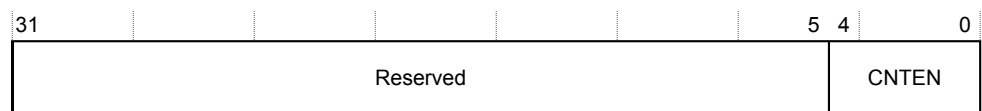


Figure 4-37 GICP\_CNTENSET0 bit assignments

The following table shows the bit assignments.



### Table 4-53 GICP\_CNTENSET0 bit assignments

Bits	Name	Function
[31:5]	-	Reserved, RAZ
[4:0]	CNTEN	<p>Counter enable.</p> <p>The CNTEN[n] bit is the enable for counter n. This field resets to an UNKNOWN value.</p> <p>Writing 1 to a bit location sets the enable for the associated counter.</p> <p>Writing 0 to a bit location has no effect. To disable a counter, use the GICP_CNTENCLR0 register.</p> <p>Reads return the state of the counter enables.</p> <p>Counter n is enabled when CNTEN[n] == 1 and GICP_CR.E == 1.</p>

#### 4.9.6 Counter Enable Clear Register 0, GICP\_CNTENCLR0

This register contains the disables for each event counter. The GIC-600 supports five event counters.

The GICP\_CNTENCLR0 characteristics are:

## Usage constraints

There are no usage constraints.

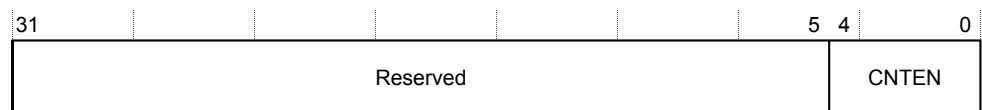
## Configurations

Available in all GIC-600 configurations.

## Attributes

See the *4.9 GICP register summary* on page 4-138.

The following figure shows the bit assignments.



**Figure 4-38 GICP\_CNTENCLR0 bit assignments**

The following table shows the bit assignments.

#### Table 4-54 GICP\_CNTLCLR0 bit assignments

Bits	Name	Function
[31:5]	-	Reserved, RAZ
[4:0]	CNTEN	Counter disable. The CNTEN[n] bit is the disable for counter n. This field resets to an UNKNOWN value. Writing 1 to a bit location clears the enable for the associated counter. Writing 0 to a bit location has no effect. To enable a counter, use the GICP_CNTENSET0 register. Reads return the state of the counter enables. Counter n is disabled when CNTEN[n] == 0 or GICP_CR.E == 1.

#### 4.9.7 Interrupt Contribution Enable Set Register 0, GICP\_INTENSET0

This register contains the set mechanism for the counter interrupt contribution enables. The GIC-600 supports five counters, n = 0-4.

The GICP INTENSET0 characteristics are:

## Usage constraints

There are no usage constraints.

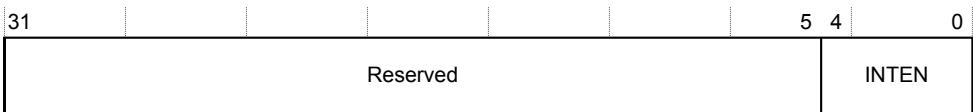
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-39 GICP\_INTENSET0 bit assignments**

The following table shows the bit assignments.

**Table 4-55 GICP\_INTENSET0 bit assignments**

Bits	Name	Function
[31:5]	-	Reserved, RAZ
[4:0]	INTEN	<p>Interrupt enable. The INTEN[n] bit is the interrupt enable for counter n. This field resets to an UNKNOWN value.</p> <p>Writing 1 to a bit location sets the interrupt enable for the associated counter.</p> <p>Writing 0 to a bit location has no effect. To disable a counter interrupt enable, use the GICP_INTENCLR0 register.</p> <p>Reads return the state of the interrupt enables.</p> <p>The interrupt enable for counter n is enabled when INTEN[n] == 1 and GICP_CR.E == 1.</p> <p>Overflow of counter n sets GICP_OVSSET0.OVS[n] to 1 and that triggers the PMU interrupt if INTEN[n] == 1.</p>

### 4.9.8 Interrupt Contribution Enable Clear Register 0, GICP\_INTENCLR0

This register contains the clear mechanism for the counter interrupt contribution enables. The GIC-600 supports five counters, n = 0-4.

The GICP\_INTENCLR0 characteristics are:

**Usage constraints**

There are no usage constraints.

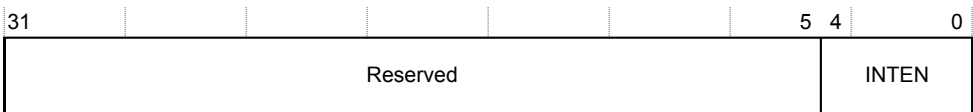
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-40 GICP\_INTENCLR0 bit assignments**

The following table shows the bit assignments.

**Table 4-56 GICP\_INTENCLR0 bit assignments**

Bits	Name	Function
[31:5]	-	Reserved, RAZ.
[4:0]	INTEN	<p>Interrupt enable. The INTEN[n] bit is the interrupt disable for counter n. This field resets to an UNKNOWN value.</p> <p>Writing 1 to a bit location clears the interrupt enable for the associated counter.</p> <p>Writing 0 to a bit location has no effect. To enable a counter interrupt enable, use the GICP_INTENSET0 register.</p> <p>Reads return the state of the interrupt enables.</p>

#### 4.9.9 Overflow Status Clear Register 0, GICP\_OVSCLR0

This register provides the clear mechanism for the counter overflow status bits and provides read access to the counter overflow status bit values. The GIC-600 supports five counters, n = 0-4.

The GICP\_OVSCLR0 characteristics are:

**Usage constraints**

There are no usage constraints.

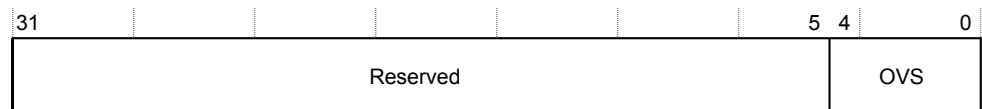
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-41 GICP\_OVSCLR0 bit assignments**

The following table shows the bit assignments.

**Table 4-57 GICP\_OVSCLR0 bit assignments**

Bits	Name	Function
[31:5]	-	Reserved, RAZ.
[4:0]	OVS	<p>Overflow status. The OVS[n] bit is the overflow clear for counter n. This field resets to zero.</p> <p>Writing 1 to a bit location clears the overflow status for the associated counter.</p> <p>Writing 0 to a bit location has no effect. To set a counter overflow status, use the GICP_OVSSET0 register.</p> <p>Reads return the state of the overflow status bits.</p> <p>Overflow of counter n, that is a transition past the maximum unsigned value of the counter that causes the value to wrap and become zero, and sets the corresponding OVS bit. In addition, this event can trigger the PMU interrupt and cause a capture of the PMU counter values, see <a href="#">4.9.2 Event Type Configuration Registers, GICP_EVTYPERN on page 4-139</a>.</p>

#### 4.9.10 Overflow Status Set Register 0, GICP\_OVSSET0

This register provides the set mechanism for the counter overflow status bits and provides read access to the counter overflow status bit values. The GIC-600 supports five counters, n = 0-4.

The GICP\_OVSSET0 characteristics are:

**Usage constraints**

There are no usage constraints.

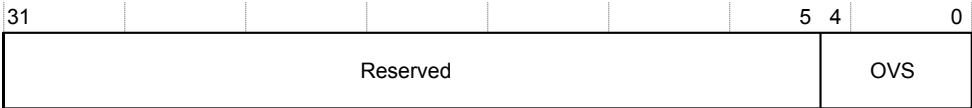
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-42 GICP\_OVSSET0 bit assignments**

The following table shows the bit assignments.

**Table 4-58 GICP\_OVSSET0 bit assignments**

Bits	Name	Function
[31:5]	-	Reserved, RAZ.
[4:0]	OVS	<p>Overflow status. The OVS[n] bit is the overflow set for counter n. This field resets to zero.</p> <p>Writing 1 to a bit location sets the overflow status for the associated counter.</p> <p>Writing 0 to a bit location has no effect. To clear a counter overflow status, use the GICP_OVSCLR0 register.</p> <p>Reads return the state of the overflow status bits.</p> <p>When the agent controlling the GIC-600 sets an OVS bit, it is similar to an OVS bit being set because of a counter overflow. However, it is IMPLEMENTATION DEFINED whether the overflow triggers the PMU interrupt or performs a capture of the PMU counter values.</p> <p>Setting the OVS bit triggers the overflow interrupt if it is enabled.</p>

**4.9.11 Counter Shadow Value Capture Register, GICP\_CAPR**

This register controls the counter shadow value capture mechanism.

The GICP\_CAPR characteristics are:

**Usage constraints**

There are no usage constraints.

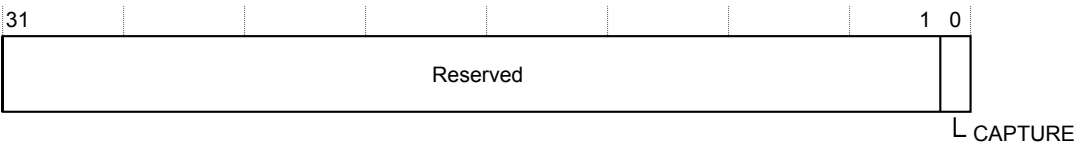
**Configurations**

Available in all GIC-600 configurations.

**Attributes**

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-43 GICP\_CAPR bit assignments**

The following table shows the bit assignments.

**Table 4-59 GICP\_CAPR bit assignments**

Bits	Name	Function
[31:1]	-	Reserved.
[0]	CAPTURE	When GICP_CFGR.CAPTURE == 1, a write of 1 to this bit triggers a capture of all values within the PMU into their respective shadow registers. When GICP_CFGR.CAPTURE == 0, this bit is zero.

#### Related references

[A.6 Miscellaneous signals on page Appx-A-163.](#)

### 4.9.12 Configuration Information Register, GICP\_CFGR

This register returns information about the PMU implementation.

The GICP\_CFGR characteristics are:

#### Usage constraints

There are no usage constraints.

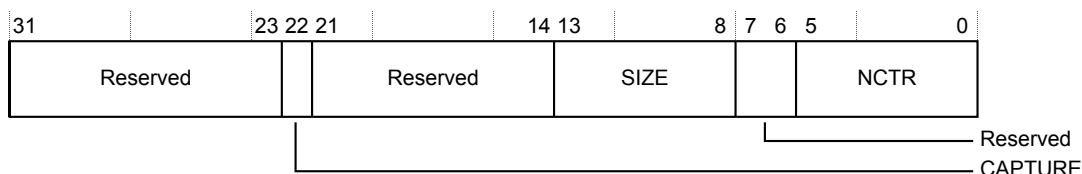
#### Configurations

Available in all GIC-600 configurations.

#### Attributes

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-44 GICP\_CFGR bit assignments**

The following table shows the bit assignments.

**Table 4-60 GICP\_CFGR bit assignments**

Bits	Name	Function
[31:23]	-	Reserved, RAZ.
[22]	CAPTURE	Set to 1, to indicate that the GIC supports capture.
[21:14]	-	Reserved, RAZ.
[13:8]	SIZE	Set to 31, to indicate that the GIC supports 32-bit counters.
[7:6]	-	Reserved, RAZ.
[5:0]	NCTR	Set to 4, to indicate that the GIC provides five counters.

### 4.9.13 Control Register, GICP\_CR

This register controls whether all counters are enabled or disabled.

The GICP\_CR characteristics are:

#### Usage constraints

There are no usage constraints.

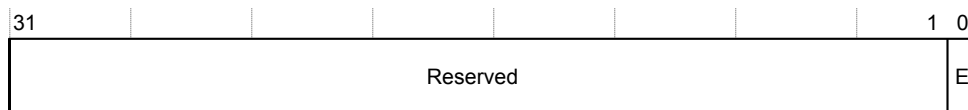
### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-45 GICP\_CR bit assignments**

The following table shows the bit assignments.

**Table 4-61 GICP\_CR bit assignments**

Bits	Name	Function
[31:1]	-	Reserved.
[0]	E	Global counter enable: 0 = No events are counted and values in the GICP_EVCNTRn registers do not change. 1 = The counters are enabled.  This bit takes precedence over the GICP_CNTENSET0.CNTEN bits.

### 4.9.14 Peripheral ID2 Register, GICP\_PIDR2

This register defines the GIC architecture version with which the GIC-600 complies.

The GICP\_PIDR2 characteristics are:

### Usage constraints

There are no usage constraints.

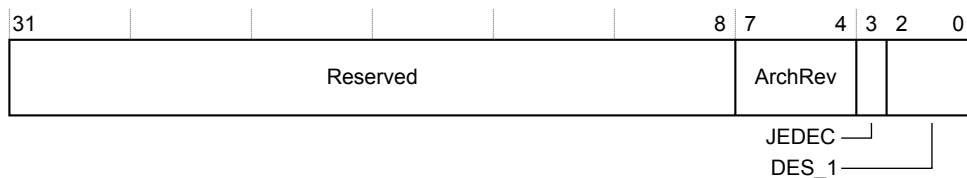
### Configurations

Available in all GIC-600 configurations.

### Attributes

See the [4.9 GICP register summary on page 4-138](#).

The following figure shows the bit assignments.



**Figure 4-46 GICP\_PIDR2\_bit assignments**

The following table shows the bit assignments.

**Table 4-62 GICP\_PIDR2 bit assignments**

Bits	Name	Function
[31:8]	-	Reserved, RAZ.
[7:4]	ArchRev	Identifies the version of the GIC architecture with which the GIC-600 complies: • 0x03 = GICv3.

**Table 4-62 GICP\_PIDR2 bit assignments (continued)**

Bits	Name	Function
[3]	JEDEC	Indicates that a JEDEC-assigned JEP106 identity code is used.
[2:0]	DES_1	Bits[6:4] of the JEP106 identity code. Bits[3:0] of the JEP106 identity code are assigned to GICP_PIDR1.

# Appendix A

## Signal descriptions

Read this for a description of the input and output signals.

It contains the following sections:

- *A.1 Common control signals* on page Appx-A-153.
- *A.2 Power control signals* on page Appx-A-155.
- *A.3 Interrupt signals* on page Appx-A-156.
- *A.4 CPU interface signals* on page Appx-A-157.
- *A.5 ACE interface signals* on page Appx-A-158.
- *A.6 Miscellaneous signals* on page Appx-A-163.
- *A.7 Interblock signals* on page Appx-A-164.
- *A.8 Interdomain signals* on page Appx-A-166.



## A.1 Common control signals

The following table shows the GIC-600 common control signal set.

**Table A-1 Common control signals**

Signal name	Type	Source or destination	Description
[<domain>]clk	Input	Clock source	Clock input.
[<domain>]reset_n	Input	Reset source	Active-LOW reset. Minimum of one cycle.
dbg_[<domain>]reset_n	Input	Reset source	Active-LOW reset for the PMU and error records.  Only present for domain containing the Distributor.
Test signals			
dftrstdisable	Input	DFT control logic	Reset disable. Disables the external reset input for test mode. When this signal is HIGH, it forces the internal active-LOW reset HIGH, bypassing the reset synchronizer.
dftse	Input		Scan enable. Disables clock gates for test mode.
dftcgen	Input		Clock gate enable. When this signal is HIGH, it forces all the clock gates on so that all internal clocks always run.
dftramhold	Input		RAM hold. When this signal is HIGH, it forces all the RAM chip selects LOW, preventing accesses to the RAMs.
MBIST controller signals			
[<domain>]mbistack	Output	MBIST controller	MBIST mode ready.  GIC-600 acknowledges that it is ready for MBIST testing.
[<domain>]mbistreq	Input		MBIST mode request.  Request to GIC-600 to enable MBIST testing. This signal must be tied LOW during functional operation.
[<domain>]nmbistreset	Input		Resets MBIST logic.  Resets functional logic to enable MBIST operation by an Active-LOW signal. This signal must be tied HIGH during functional operation.

Table A-1 Common control signals (continued)

Signal name	Type	Source or destination	Description
[<domain>_]mbistaddr[variable:0] <sup>ai</sup>	Input	MBIST controller	Logical address.  The width is based on the RAM with the largest number of words. You must drive the most significant bits to zero when accessing RAMs with fewer address bits.
[<domain>_]mbistindata[variable:0] <sup>ai</sup>	Input		Data in.  Write data. Width that is based on the RAM with the largest number of data bits.
[<domain>_]mbistoutdata[variable:0] <sup>ai</sup>	Output		Data out.  Read data. Width that is based on the RAM with the largest number of data bits.
[<domain>_]mbistwriteen	Input		Write control ( <b>mbistwriteen</b> ) and read control ( <b>mbistreaden</b> ). No access occurs if both enables are off. It is illegal to activate both enables simultaneously.
[<domain>_]mbistreaden	Input		
[<domain>_]mbistarray[variable:0] <sup>ai</sup>	Input		Array selector.  This controls which RAM array is accessed. For the single RAM configuration, this port is unused.  This signal is not present on a block containing only one RAM.
[<domain>_]mbistcfg	Input		MBIST ALL enable.  When enabled, allows simultaneous access to all RAM arrays for maximum array power consumption.  This signal is not present on a block containing only one RAM.

<sup>ai</sup> The variable is configuration-dependent.

## A.2 Power control signals

The following table shows the GIC-600 power control signals.

**Table A-2 Power control signals**

Signal name	Type	Source or destination	Description
<b>cpu_active</b> [<ppi_block>] [<bus>][<num_cpus - 1:0>]	Input	Power controller	Indicates if the core is active and not in a low-power state such as retention. This is used for lowering the priority of selection for 1 of N SPIs. There is one bit per core on the ICC bus.
<b>wake_request</b> [<num_cpus - 1:0>]	Output	Power controller	Wake request signal to power controller indicating that an interrupt is targeting this core and it must be woken. When asserted the <b>wake_request</b> is sticky unless the Distributor is put into the gated state.
<b>qreqn_col</b>	Input	Low-power interface	Low-power interface to flush out the path between the SPI Collator and the Distributor to aid in power down. When asserted, messages are not sent to the Distributor until low-power state is exited.  ————— <b>Note</b> ————— It is only safe to stop the Collator clock if all interrupts are level sensitive, or if edge-triggered, pulse extended into the SPI Collator. —————
<b>qacceptn_col</b>	Output		
<b>qdeny_col</b>	Output		
<b>qactive_col</b>	Output		
<b>qreqn_its</b> [<its>]	Input	Low-power interface <sup>aj</sup>	Required to flush out the path between the ITS and the Distributor.  There is one Q-Channel for each ITS.  All Distributor ITS Q-Channels are combined as a single set of vectored signals, <b>qreqn_its</b> [num_ITS - 1:0].
<b>qacceptn_its</b> [<its>]	Output		
<b>qdeny_its</b> [<its>]	Output		
<b>qactive_its</b> [<its>]	Output		
[<domain_>]clkqreqn	Input	Clock controller	Low-power interface for clock gating of everything in the domain.  [<domain_>]clkqreqn is synchronized into the GIC-600.  This bus must be treated asynchronously.
[<domain_>]clkqacceptn	Output		
[<domain_>]clkqdeny	Output		
[<domain_>]clkqactive	Output		
[<domain_>]pwrqreqn	Input	Power controller	ADB power interface within the domain.  See the <i>ARM® CoreLink™ ADB-400 AMBA® Domain Bridge User Guide</i> .
[<domain_>]pwrqacceptn	Output		
[<domain_>]pwrqdeny	Output		
[<domain_>]pwrqactive	Output		

<sup>aj</sup> These signals are not present in monolithic configurations where the Distributor and ITS share ACE-Lite ports.

## A.3 Interrupt signals

The following table shows the GIC-600 interrupt signal set.

**Table A-3 Interrupt signals**

Signal name	Type	Source or destination	Description
<b>ppi</b> <n><[_<ppi_block>] [_<bus>][_<num_cpus - 1:0>]	Input	Interrupt source	PPI input wires for interrupt <n>. One bit per core.  n is 16-31 if the number of PPIs per core is 16.  n is 20-31 if the number of PPIs per core is 12.  n is 22-27, 29, 30 if number of PPIs per core is 8.
<b>ppi</b> <n>_r[_<ppi_block>] [_<bus>]	Output	Interrupt source	PPI output after synchronization and edge detection. You can use it for cross-domain pulse detection.
<b>spi</b> [variable:0]	Input	Interrupt source	This is the number of SPI wires that are supported by the GIC.  ————— <b>Note</b> —————  This is not the same as the number of SPIs supported because they could be message-based only or be on another chip.  —————
<b>spi_r</b> [variable:0]	Output	Interrupt source	SPI output after synchronization and edge detection. Can be used for cross-domain pulse detection.

### Related concepts

[2.2.4 Redistributor PPI signals on page 2-30.](#)

[2.5 SPI Collator on page 2-40.](#)

## A.4 CPU interface signals

The following table shows the GIC-600 CPU interface signal set.

**Table A-4 CPU interface signals**

Signal name	Type	Source or destination	Description
<b>iccttready</b> [_<ppi_num>] [_<bus>]	Output	Core block	<p>GIC Stream-compliant bus for communication from the core block to the Redistributor. It is fully credited and can be sent over any free-flowing interconnect.</p> <p>See the <i>Redistributor to downstream CPU interface table</i> in the <i>GIC Stream Redistributor to downstream CPU interface Appendix</i> of the <i>ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0</i>.</p> <p>IDs <b>iccttid</b> values of &lt;num_cpus - 1:0&gt; are used. Issuing other values is UNPREDICTABLE.</p>
<b>iccttvalid</b> [_<ppi_num>] [_<bus>]	Input		
<b>icctdata</b> [_<ppi_num>] [_<bus>][15:0]	Input		
<b>iccttid</b> [_<ppi_num>] [_<bus>][variable:0] <sup>ak</sup>	Input		
<b>iccttlast</b> [_<ppi_num>] [_<bus>]	Input		
<b>iccttwakeup</b> [_<ppi_num>] [_<bus>]	Input		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>icc</b> bus. Signals <b>iccttvalid</b> and <b>iccttready</b> control data transfer.
<b>iritready</b> [_<ppi_num>] [_<bus>]	Input	Core block	<p>GIC Stream-compliant bus for communication from the Redistributor to the core block. It is fully credited and can be sent over any free-flowing interconnect.</p> <p>See the <i>Redistributor to downstream CPU interface table</i> in the <i>GIC Stream Redistributor to downstream CPU interface Appendix</i> of the <i>ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0</i>.</p> <p>IDs <b>iritdest</b> values of &lt;num_cpus - 1:0&gt; are used.</p>
<b>iritvalid</b> [_<ppi_num>] [_<bus>]	Output		
<b>iritdata</b> [_<ppi_num>] [_<bus>][15:0]	Output		
<b>iritdest</b> [_<ppi_num>] [_<bus>][variable:0] <sup>ak</sup>	Output		
<b>iritlast</b> [_<ppi_num>] [_<bus>]	Output		
<b>iritwakeup</b> [_<ppi_num>] [_<bus>]	Output		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>iri</b> bus. Signals <b>iritvalid</b> and <b>iritready</b> control data transfer.

<sup>ak</sup> The variable is configuration-dependent.

## A.5 ACE interface signals

The following table shows the GIC-600 ACE signal set.

**Table A-5 ACE interface signals**

Signal name	Type	Description
Write address channel signals → Slave		
There are multiple versions of this bus. Buses that have <code>_its[_&lt;num&gt;]</code> are dedicated ITS slave ports for GITS_TRANSLATER only. There is always one port that has no <code>_its</code> suffix that is used for all registers except GITS_TRANSLATER. This port is used for all registers in monolithic configurations.		
<code>awuser[_its[_&lt;num&gt;]]_s[<b>did_width:0</b>]</code> <sup>al</sup>	Input	Optional user-defined signal in the write address channel. Supported only in AXI4.  Indicates the <i>DeviceID</i> of writes to GITS_TRANSLATER if MSI_64 is not configured.
<code>awaddr[_its[_&lt;num&gt;]]_s[<b>variable:0</b>]</code> <sup>al</sup>	Input	The write address gives the address of the first transfer in a write burst transaction.
<code>awid[_its[_&lt;num&gt;]]_s[<b>variable:0</b>]</code> <sup>al</sup>	Input	This signal is the identification tag for the write address group of signals.
<code>awlen[_its[_&lt;num&gt;]]_s[7:0]</code>	Input	The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
<code>awsize[_its[_&lt;num&gt;]]_s[2:0]</code>	Input	This signal indicates the size of each transfer in the burst.
<code>awburst[_its[_&lt;num&gt;]]_s[1:0]</code>	Input	The burst type and the size information, determine how the address for each transfer within the burst is calculated.
<code>awprot[_its[_&lt;num&gt;]]_s[2:0]</code>	Input	This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
<code>awvalid[_its[_&lt;num&gt;]]_s</code>	Input	This signal indicates that the channel is signaling valid write address and control information.
<code>awready[_its[_&lt;num&gt;]]_s</code>	Output	This signal indicates that the slave is ready to accept an address and associated control signals.
<code>awcache[_its[_&lt;num&gt;]]_s[3:0]</code>	Input	This signal indicates how transactions are required to progress through a system.
<code>awdomain[_its[_&lt;num&gt;]]_s[1:0]</code>	Input	This signal indicates the shareability domain of a write transaction.
<code>awsnoop[_its[_&lt;num&gt;]]_s[2:0]</code>	Input	This signal indicates the transaction type for Shareable write transactions.
<code>awbar[_its[_&lt;num&gt;]]_s[1:0]</code>	Input	This signal indicates a write barrier transaction.
Write data channel signals → Slave		
<code>wstrb[_its[_&lt;num&gt;]]_s[<b>variable:0</b>]</code> <sup>al</sup>	Input	This signal indicates which byte lanes hold valid data. There is one write strobe bit for every eight bits of the write data bus.
<code>wdata[_its[_&lt;num&gt;]]_s[<b>variable:0</b>]</code> <sup>al</sup>	Input	Write data.
<code>wvalid[_its[_&lt;num&gt;]]_s</code>	Input	This signal indicates that valid write data and strobes are available.

**Table A-5 ACE interface signals (continued)**

Signal name	Type	Description
<b>wready_</b> [its[_<num>]]_s	Output	This signal indicates that the slave can accept the write data.
<b>wlast_</b> [its[_<num>]]_s	Input	This signal indicates the last transfer in a write burst.
Write response channel signals → Slave		
<b>bid_</b> [its[_<num>]]_s[variable:0] <sup>al</sup>	Output	This signal is the ID tag of the write response.
<b>bvalid_</b> [its[_<num>]]_s	Output	This signal indicates that the channel is signaling a valid write response.
<b>bready_</b> [its[_<num>]]_s	Input	This signal indicates that the master can accept a write response.
<b>bresp_</b> [its[_<num>]]_s[1:0]	Output	This signal indicates the status of the write transaction.
Read address channel signals → Slave		
<b>arcache_</b> [its[_<num>]]_s[3:0]	Input	This signal indicates how transactions are required to progress through a system.
<b>arbar_</b> [its[_<num>]]_s[1:0]	Input	This signal indicates a read barrier transaction.
<b>arsnoop_</b> [its[_<num>]]_s[3:0]	Input	This signal indicates the transaction type for Shareable read transactions.
<b>ardomain_</b> [its[_<num>]]_s[1:0]	Input	This signal indicates the shareability domain of a read transaction.
<b>araddr_</b> [its[_<num>]]_s[variable:0] <sup>al</sup>	Input	The read address gives the address of the first transfer in a read burst transaction.
<b>arid_</b> [its[_<num>]]_s[variable:0] <sup>al</sup>	Input	This signal is the identification tag for the read address group of signals.
<b>arlen_</b> [its[_<num>]]_s[7:0]	Input	This signal indicates the exact number of transfers in a burst. This changes between AXI3 and AXI4.
<b>arsize_</b> [its[_<num>]]_s[2:0]	Input	This signal indicates the size of each transfer in the burst.
<b>aruser_</b> [its[_<num>]]_s[2:0]	Input	This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or instruction access.
<b>arburst_</b> [its[_<num>]]_s[1:0]	Input	The burst type and the size information determine how the address for each transfer within the burst is calculated.
<b>arprot_</b> [its[_<num>]]_s[2:0]	Input	This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
<b>arvalid_</b> [its[_<num>]]_s	Input	This signal indicates that the channel is signaling valid read address and control information.
<b>arready_</b> [its[_<num>]]_s	Output	This signal indicates that the slave is ready to accept an address and associated control signals.
Read data channel signals → Slave		
<b>rid_</b> [its[_<num>]]_s[variable:0] <sup>al</sup>	Output	This signal is the identification tag for the read data group of signals generated by the slave.
<b>rdata_</b> [its[_<num>]]_s[variable:0] <sup>al</sup>	Output	Read data.
<b>rresp_</b> [its[_<num>]]_s[1:0]	Output	This signal indicates the status of the read transfer.

**Table A-5 ACE interface signals (continued)**

Signal name	Type	Description
<b>rlast</b> [_its[_<num>]]_s	Output	This signal indicates the last transfer in a read burst.
<b>rvalid</b> [_its[_<num>]]_s	Output	This signal indicates that the channel is signaling the required read data.
<b>rready</b> [_its[_<num>]]_s	Input	This signal indicates that the master can accept the read data and response information.
Write address channel signals → Master. Only present if LPI support is configured.		
Buses containing <b>_its[_&lt;num&gt;]</b> are used by the specific ITS for read/writes to the private tables and Command queue. Buses without an <b>_its</b> suffix are used for accesses to the LPI Pending and Property tables. This port performs all accesses in monolithic configurations.		
<b>awaddr</b> [_its[_<num>]]_m[variable:0] <sup>al</sup>	Output	The write address gives the address of the first transfer in a write burst transaction.
<b>awid</b> [_its[_<num>]]_m[variable:0] <sup>al</sup>	Output	This signal is the identification tag for the write address group of signals.
<b>awlen</b> [_its[_<num>]]_m[7:0]	Output	The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
<b>awsize</b> [_its[_<num>]]_m[2:0]	Output	This signal indicates the size of each transfer in the burst.
<b>awburst</b> [_its[_<num>]]_m[1:0]	Output	The burst type and size information determine how the address for each transfer within the burst is calculated.
<b>awprot</b> [_its[_<num>]]_m[2:0]	Output	This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
<b>awvalid</b> [_its[_<num>]]_m	Output	This signal indicates that the channel is signaling valid write address and control information.
<b>awready</b> [_its[_<num>]]_m	Input	This signal indicates that the channel is signaling valid write address and control information.
<b>awcache</b> [_its[_<num>]]_m[3:0]	Output	This signal indicates how transactions are required to progress through a system.
<b>awdomain</b> [_its[_<num>]]_m[1:0]	Output	This signal indicates the shareability domain of a write transaction.
<b>awsnoop</b> [_its[_<num>]]_m[2:0]	Output	This signal indicates the transaction type for Shareable write transactions.
<b>awbar</b> [_its[_<num>]]_m[1:0]	Output	This signal indicates a write barrier transaction.
<b>awuser</b> _m[variable:0] <sup>al</sup>	Output	Optional user-defined signal in the write address channel.
Write data channel signals → Master. Only present if LPI support is configured.		
<b>wstrb</b> [_its[_<num>]]_m[variable:0] <sup>al</sup>	Output	This signal indicates which byte lanes hold valid data. There is one write strobe bit for every eight bits of the write data bus.
<b>wdata</b> [_its[_<num>]]_m[variable:0] <sup>al</sup>	Output	Write data.
<b>wvalid</b> [_its[_<num>]]_m	Output	This signal indicates that valid write data and strobes are available.
<b>wready</b> [_its[_<num>]]_m	Input	This signal indicates that the slave can accept the write data.



**Table A-5 ACE interface signals (continued)**

Signal name	Type	Description
<b>wlast</b> _[its[_<num>]]_m	Output	This signal indicates the last transfer in a write burst.
Write response channel signals → Master. Only present if LPI support is configured.		
<b>bid</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Input	This signal is the ID tag of the write response.
<b>bvalid</b> _[its[_<num>]]_m	Input	This signal indicates that valid write data and strobes are available.
<b>bready</b> _[its[_<num>]]_m	Output	This signal indicates that the channel is signaling a valid write response.
<b>bresp</b> _[its[_<num>]]_m[1:0]	Input	This signal indicates the status of the write transaction.
Read address channel signals → Master. Only present if LPI support is configured.		
<b>araddr</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Output	The read address gives the address of the first transfer in a read burst transaction.
<b>arid</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Output	This signal is the identification tag for the read address group of signals.
<b>arlen</b> _[its[_<num>]]_m[7:0]	Output	This signal indicates the exact number of transfers in a burst. This changes between AXI3 and AXI4.
<b>arsize</b> _[its[_<num>]]_m[2:0]	Output	This signal indicates the size of each transfer in the burst.
<b>arburst</b> _[its[_<num>]]_m[1:0]	Input	The burst type and the size information determine how the address for each transfer within the burst is calculated.
<b>arprot</b> _[its[_<num>]]_m[2:0]	Output	This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
<b>arvalid</b> _[its[_<num>]]_m	Output	The signal indicates that the channel is signaling valid read address and control information.
<b>arready</b> _[its[_<num>]]_m	Input	This signal indicates that the slave is ready to accept an address and associated control signals.
<b>arcache</b> _[its[_<num>]]_m[3:0]	Output	This signal indicates how transactions are required to progress through a system.
<b>ardomain</b> _[its[_<num>]]_m[1:0]	Output	This signal indicates the shareability domain of a read transaction.
<b>arsnoop</b> _[its[_<num>]]_m[3:0]	Output	This signal indicates the transaction type for Shareable read transactions.
<b>arbar</b> _[its[_<num>]]_m[1:0]	Output	This signal indicates a read barrier transaction.
<b>aruser</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Output	Optional user-defined signal in the read address channel. Supported only in AXI4.
Read data channel signals → Master. Only present if LPI support is configured.		
<b>rid</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Input	This signal is the identification tag for the read data group of signals generated by the slave.
<b>rada</b> _[its[_<num>]]_m[variable:0] <sup>al</sup>	Input	Read data.
<b>rresp</b> _[its[_<num>]]_m[1:0]	Input	This signal indicates the status of the read transfer.
<b>rlast</b> _[its[_<num>]]_m	Input	This signal indicates the last transfer in a read burst.

**Table A-5 ACE interface signals (continued)**

Signal name	Type	Description
<b>rvalid_[its[_&lt;num&gt;]]_m</b>	Input	This signal indicates that the channel is signaling the required read data.
<b>rready_[its[_&lt;num&gt;]]_m</b>	Output	This signal indicates that the master can accept the read data and response information.

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<sup>a1</sup> The variable is configuration-dependent.

## A.6 Miscellaneous signals

The following table shows the GIC-600 miscellaneous signals.

**Table A-6 Miscellaneous signals**

Signal name	Type	Source or destination	Description
<b>ppi_id[15:0]</b>	Input	Interrupt source	RedistributorID number that is used for system identification only. Software can read the GICR_CFGID0 register to access the value of this signal.
<b>its_id[7:0]</b>	Input	ITS block	ID number that is used for system identification only. Software can read the GITS_CFGID register to access the value of this signal.
<b>sample_req</b>	Input	Debug controller	Request to sample PMU. Equivalent to writing to the GICP_CAPR register.
<b>sample_ack</b>	Output	Debug controller	<b>sample_req</b> accept.
<b>fault_int</b>	Output	System control processor	Fault handling interrupt.
<b>err_int</b>	Output	System control processor	Error handling interrupt.
<b>pmu_int</b>	Output	Debug controller	PMU overflow length.
<b>gict_allow_ns</b>	Input	Tie-off	Allow Non-secure access to error record registers.
<b>gicp_allow_ns</b>	Input	Tie-off	Allow Non-secure access to PMU registers.

### Related references

[4.5.4 Configuration ID0 Register; GICR\\_CFGID0](#) on page 4-110.

[4.6.6 Configuration ID Register; GITS\\_CFGID](#) on page 4-120.

[4.9.11 Counter Shadow Value Capture Register; GICP\\_CAPR](#) on page 4-148.

## A.7 Interblock signals

The following table shows the GIC-600 interblock signals.

**Table A-7 Interblock signals**

Signal name	Forward or reverse	Source or destination	Description
icdptready	Reverse	Redistributor → Distributor	AXI4-Stream compliant bus for communication between the Distributor and a Redistributor. It is fully credited and must never backpressure. It can be sent over any free-flowing interconnect.
icdptvalid	Forward	Distributor → Redistributor	
icdptdata[variable] <sup>am</sup>	Forward		
icdptlast	Forward		
icdptwakeup	Forward		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>icdp</b> bus. Signals <b>icdptvalid</b> and <b>icdptready</b> control data transfer.
icpdtready	Reverse	Distributor → Redistributor	AXI4-Stream compliant bus for communication between the Redistributor and the Distributor. It is fully credited and can be sent over any free-flowing interconnect.
icpdtvalid	Forward	Redistributor → Distributor	
icpdtdata[variable:0]	Forward		
icpdtlast	Forward		
icpdtwakeup	Forward		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>icpd</b> bus. Signals <b>icpdtvalid</b> and <b>icpdtready</b> control data transfer.
icditready	Reverse	ITS → Distributor	AXI4-Stream compliant bus for communication from the Distributor to the ITS. It is fully credited and can be sent over any free-flowing interconnect.
icditvalid	Forward	Distributor → ITS	
icditdata[variable:0] <sup>am</sup>	Forward		
icditlast	Forward		
icditwakeup	Forward		Indicates that a message is arriving or is about to arrive on the <b>icdi</b> bus. Signals <b>icditvalid</b> and <b>icditready</b> control data transfer.
icidtready	Reverse	Distributor → ITS	AXI4-Stream compliant bus for communication from the ITS to the Distributor. It is fully credited and can be sent over any free-flowing interconnect.
icidtvalid	Forward	ITS → Distributor	
icidtdata[variable:0] <sup>am</sup>	Forward		
icidtkeep[variable:0]	Forward		
icidtlast	Forward		
icidtawakeup	Forward	Registered wake signal	Indicates that a message is arriving or is about to arrive on the <b>icid</b> bus. Signals <b>icidtvalid</b> and <b>icidtready</b> control data transfer.

<sup>am</sup> The variable is configuration-dependent.

**Table A-7 Interblock signals (continued)**

Signal name	Forward or reverse	Source or destination	Description
<b>icdwtready</b>	Reverse	Wake Request → Distributor	AXI4-Stream compliant bus for communication from the Distributor to the Wake Request block.
<b>icdwtvalid</b>	Forward	Distributor → Wake Request	It is fully credited and can be sent over any free-flowing interconnect.
<b>icdwtdata[15:0]</b>	Forward		This bus is not exposed when the top level is stitched.
<b>icdwtwakeup</b>	Forward		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>icdw</b> bus. Signals <b>icdwtvalid</b> and <b>icdwtready</b> control data transfer.  This signal is not exposed when the top level is stitched.
<b>icdctready</b>	Reverse	SPI Collator → Distributor	AXI4-Stream compliant bus for communication between the Distributor and the SPI Collator. It is fully credited and must never backpressure. It can be sent over any free-flowing interconnect.
<b>icdctvalid</b>	Forward	Distributor → SPI Collator	
<b>icdctdata[15:0]</b>	Forward		
<b>icdctlst</b>	Forward		
<b>icdctwakeup</b>	Forward		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>icdc</b> bus. Signals <b>icdctvalid</b> and <b>icdctready</b> control data transfer.
<b>iccdtready</b>	Reverse	Distributor → SPI Collator	AXI4-Stream compliant bus for communication between the SPI Collator and the Distributor. It is fully credited and must never backpressure. It can be sent over any free-flowing interconnect.
<b>iccdtvalid</b>	Forward	SPI Collator → Distributor	
<b>iccdtdata[15:0]</b>	Forward		
<b>iccdtlst</b>	Forward		
<b>iccdtwakeup</b>	Forward		Registered wake signal to indicate that a message is arriving or is about to arrive on the <b>iccd</b> bus. Signals <b>iccdtvalid</b> and <b>iccdtready</b> control data transfer.

## A.8 Interdomain signals

Interdomain signals are routed between domains.

The following table shows the interdomain signals.

**Table A-8 Interdomain signals**

Signal name
wakeup_sm_*
wakeup_ms_*
*_async_*

If you instantiate domain levels, you must ensure that matching input and output pairs of interdomain signals connect together directly, and are not separated by synchronizers.

## Appendix B

# Implementation-defined features

Read this for a description of the IMPLEMENTATION-DEFINED features.

It contains the following section:

- [\*B.1 Implementation-defined features reference\*](#) on page Appx-B-168.

## B.1 Implementation-defined features reference

The GIC-600 implements features that are defined in the GICv3 Architecture. Many of these features are configurable at build time.

The following table describes each feature with reference to the *ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0*.

**Table B-1 Declared implementation-defined features**

Implementation-defined features	Architectural specification reference		Description
	Chapter	Section	
1 of N model	Introduction	Models for handling interrupts	See <a href="#">3.2.4 1 of N SPI interrupt selection on page 3-52</a> .
Direct LPI support	GIC partitioning	The GIC logical components	Direct LPI support is by configuration if there are no LPIs in the system.
ITS to Redistributor communications	GIC partitioning Locality-specific peripheral interrupts and the ITS	The GIC logical components LPIs	This is done over a fully credited AXI4-Stream.
INTIDs	Distributed and routing of interrupts	INTIDs	16-bit width when supporting LPIs, otherwise the width is set to support the number of SPIs and SGIs.
All error cases	-	Pseudocode throughout the document	All errors are reported through error records, see <a href="#">3.2.15 Reliability, Accessibility, and Serviceability on page 3-64</a> .
Message-based SPIs	Physical interrupt handling and prioritization	Shared peripheral interrupts	Pending bits for level sensitive SPIs that are set by writes to GICD_SETSPI_* or GICA_SETSPI_* are not affected by writes to GICD_ICPENDR. Writes to GICD_CLRSPI_* or GICA_CLRSPI_* have no effect on pending bits set by GICD_ISPENDR.
Interrupt grouping	Physical interrupt handling and prioritization	Interrupt grouping	All implemented SPIs, SGIs, and PPIs have programmable groups.
Interrupt enables	Physical interrupt handling and prioritization	Enabling individual interrupts	All SGIs have a programmable enable.
Interrupt prioritization	Physical interrupt handling and prioritization	Interaction of group and individual interrupt enables	Interrupts that are disabled through the GICC_CTLR register or the ICC_CTLR_* registers are not considered in the selection of the highest pending interrupt and do not block fully enabled interrupts of a lower priority.
		Interrupt prioritization	GIC-600 supports 32 priority levels, 16 for LPIs that are always Non-secure.
Effects of disabling interrupts	Physical interrupt handling and prioritization	Effects of disabling interrupts	Interrupts are set pending irrespective of the GICD_CTLR.EnableGrp* settings.



**Table B-1 Declared implementation-defined features (continued)**

Implementation-defined features	Architectural specification reference		Description
	Chapter	Section	
Changing priority	Physical interrupt handling and prioritization	Interrupt prioritization.  Changing the priority of enabled PPIs, SGIs, and SPIs.	Reprogramming an IPRIORITYRn register does not change the priority of an active interrupt but causes a pending and not active interrupt to be recalled from the CPU interface so that the new value can be applied.
Direct LPI registers	Locality-specific peripheral interrupts and the ITS	LPIs	The GICR_SETLPIR, GICR_CLRLPIR, GICR_INVLPIR, GICR_INVALLR, and GICR_SYNCR are supported in configurations that support LPIs but have no ITS anywhere in the system. If there is an ITS, these registers, and their locations, are RAZ/WI.
LPI caching	Locality-specific peripheral interrupts and the ITS	LPIs	See <a href="#">3.2.10 LPI caching on page 3-60</a> and <a href="#">3.2.9 Interrupt translation service (ITS) on page 3-57</a> .
LPI configuration tables	Locality-specific peripheral interrupts and the ITS	LPI configuration tables	The GIC-600 has one GICR_PROPBASER register for all cores on a chip and therefore points at a single table. Each chip in a multichip configuration can point to a copy of the table in local memory. See <i>GICR_TYPER.CommonLPIAff</i> in <a href="#">4.2.1 Interrupt Controller Type Register; GICD_TYPER on page 4-88</a> for more information.  When interrupts are sent between chips, they keep the properties associated with them until the next invalidate. All property fetches are always from the offset specified in the GICR_PROPBASER of the issuing chip.
LPI Pending tables	Locality-specific peripheral interrupts and the ITS	LPI Pending tables	See <i>LPI Pending tables</i> in the <i>ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0</i> .

# Appendix C

## Revisions

Read this for a description of changes between released issues of this book.

It contains the following section:

- [C.1 Revisions on page Appx-C-171](#).

## C.1 Revisions

This appendix describes changes between released issues of this book.

**Table C-1 Issue 0000-00**

Change	Location	Affects
First release	-	-

**Table C-2 Differences between issue 0000-00 and issue 0000-01**

Change	Location	Affects
Added note	<i>1.1 About the GIC-600 on page 1-12</i>	r0p0
Added figure	<i>Figure 1-3 Monolithic GIC-600 with interconnect in an example system on page 1-16</i>	r0p0
Added note	<i>Top level on page 1-14</i>	r0p0
Updated section	<i>1.4 Features on page 1-18</i>	r0p0
Updated section	<i>2.1.1 Distributor AXI4-Stream interfaces on page 2-24</i>	r0p0
Updated section	<i>2.1.2 Distributor ACE-Lite slave interface on page 2-24</i>	r0p0
Updated section	<i>2.1.3 Distributor ACE-Lite master interface on page 2-25</i>	r0p0
Updated section	<i>2.1.4 Distributor Q-Channels on page 2-26</i>	r0p0
Updated table	<i>Table 2-6 Configurable options for the Distributor on page 2-27</i>	r0p0
Updated section	<i>2.2.2 Redistributor GIC Stream protocol interface on page 2-30</i>	r0p0
Updated section	<i>2.2.3 Redistributor Q-Channel on page 2-30</i>	r0p0
Updated table	<i>Table 2-8 Redistributor miscellaneous input signals on page 2-31</i>	r0p0
Updated section	<i>2.3.1 ITS ACE-Lite slave interface on page 2-33</i>	r0p0
Updated section	<i>2.3.3 ITS AXI4-Stream interface on page 2-35</i>	r0p0
Updated table	<i>Table 2-11 ITS miscellaneous signals on page 2-36</i>	r0p0
Updated table	<i>Table 2-12 Configurable options for the ITS on page 2-36</i>	r0p0
Updated section	<i>2.4.1 MSI-64 ACE-Lite interfaces on page 2-37</i>	r0p0
Updated table	<i>Table 2-14 MSI-64 miscellaneous signals on page 2-38</i>	r0p0
Updated table	<i>Table 2-15 Configurable options for the MSI-64 Encapsulator on page 2-38</i>	r0p0
Updated section	<i>2.5.2 SPI Collator wires on page 2-40</i>	r0p0
Updated section	<i>2.6.2 Wake Request miscellaneous signals on page 2-42</i>	r0p0
Updated section	<i>2.6.3 Wake Request configuration on page 2-42</i>	r0p0
Updated section	<i>2.7.1 Interconnect configuration on page 2-43</i>	r0p0
Changed note	<i>3.1.4 LPIs on page 3-49</i>	r0p0
Updated section	<i>3.1.5 Choosing between LPIs and SPIs on page 3-49</i>	r0p0
Updated section	<i>3.2.2 Interrupt signals (PPIs and SPIs) on page 3-50</i>	r0p0
Updated section	<i>3.2.3 Affinity routing and assignment on page 3-51</i>	r0p0
Added section	<i>3.2.4 1 of N SPI interrupt selection on page 3-52</i>	r0p0

**Table C-2 Differences between issue 0000-00 and issue 0000-01 (continued)**

Change	Location	Affects
Updated section	<a href="#">3.2.8 Backwards compatibility</a> on page 3-57	r0p0
Updated section	<a href="#">3.2.10 LPI caching</a> on page 3-60	r0p0
Updated section	<a href="#">3.2.11 Memory access and attributes</a> on page 3-60	r0p0
Updated section	<a href="#">3.2.12 MSI-64</a> on page 3-62	r0p0
Updated section	<a href="#">3.2.13 RAM</a> on page 3-62	r0p0
Updated section	<a href="#">3.2.14 Performance Monitoring Unit</a> on page 3-63	r0p0
Updated table	<a href="#">Table 3-6 ECC error reporting</a> on page 3-65	r0p0
Updated section	<a href="#">1.1 About the GIC-600</a> on page 1-12	r0p0
Added section	<a href="#">4.1.1 Register map pages</a> on page 4-84	r0p0
Updated section	<a href="#">4.1.3 GIC-600 register access and banking</a> on page 4-85	r0p0
Updated table	<a href="#">Table 4-2 Distributor registers (GICD/GICDA) summary</a> on page 4-86	r0p0
Updated table	<a href="#">Table 4-3 GICD_TYPER bit assignments</a> on page 4-88	r0p0
Updated table	<a href="#">Table 4-5 GICD_FCTLR bit assignments</a> on page 4-91	r0p0
Updated table	<a href="#">Table 4-7 GICD_SAC bit assignments</a> on page 4-92	r0p0
Updated table	<a href="#">Table 4-12 Distributor registers (GICA) for message-based SPIs summary</a> on page 4-97	r0p0
Updated table	<a href="#">Table 4-13 Redistributor registers for control and physical LPIs summary</a> on page 4-98	r0p0
Updated table	<a href="#">Table 4-14 GICR_IIDR bit assignments</a> on page 4-100	r0p0
Updated table	<a href="#">Table 4-15 GICR_TYPER bit assignments</a> on page 4-101	r0p0
Updated table	<a href="#">Table 4-17 GICR_FCTLR bit assignments</a> on page 4-103	r0p0
Updated table	<a href="#">Table 4-18 GICR_PWRR bit assignments</a> on page 4-104	r0p0
Updated table	<a href="#">Table 4-22 GICR_MISCSTATUSR bit assignments</a> on page 4-109	r0p0
Updated table	<a href="#">Table 4-26 GICR_CFGID1 bit assignments</a> on page 4-112	r0p0
Updated table	<a href="#">Table 4-27 ITS control register summary</a> on page 4-113	r0p0
Updated table	<a href="#">Table 4-31 GITS_OPR bit assignments</a> on page 4-119	r0p0
Updated table	<a href="#">Table 4-36 GICT register summary</a> on page 4-123	r0p0
Updated table	<a href="#">Table 4-39 GICT_ERR&lt;n&gt;CTLR bit assignments</a> on page 4-126	r0p0
Updated table	<a href="#">Table 4-40 GICT_ERR&lt;n&gt;STATUS bit assignments</a> on page 4-128	r0p0
Updated table	<a href="#">Table 4-42 GICT_ERR&lt;n&gt;MISC0 bit assignments</a> on page 4-130	r0p0
Updated table	<a href="#">Table 4-43 Data field encoding</a> on page 4-130	r0p0
Added section	<a href="#">4.8.8 Peripheral ID2 Register; GICT_PIDR2</a> on page 4-137	r0p0
Updated table	<a href="#">Table 4-47 GICP register summary</a> on page 4-138	r0p0
Updated table	<a href="#">Table 4-49 GICP_EVTYPERN bit assignments</a> on page 4-140	r0p0
Updated table	<a href="#">Table 4-50 EVENT field encoding</a> on page 4-140	r0p0
Updated table	<a href="#">Table 4-53 GICP_CNTENSET0 bit assignments</a> on page 4-145	r0p0
Updated table	<a href="#">Table 4-54 GICP_CNTENCLR0 bit assignments</a> on page 4-145	r0p0

**Table C-2 Differences between issue 0000-00 and issue 0000-01 (continued)**

Change	Location	Affects
Updated table	<a href="#">Table 4-55 GICP_INTENSET0 bit assignments</a> on page 4-146	r0p0
Added section	<a href="#">4.9.14 Peripheral ID2 Register; GICP_PIDR2</a> on page 4-150	r0p0
Updated section	<a href="#">A.2 Power control signals</a> on page Appx-A-155	r0p0
Updated section	<a href="#">A.3 Interrupt signals</a> on page Appx-A-156	r0p0
Updated section	<a href="#">A.4 CPU interface signals</a> on page Appx-A-157	r0p0
Updated section	<a href="#">A.7 Interblock signals</a> on page Appx-A-164	r0p0
Updated section	<a href="#">B.1 Implementation-defined features reference</a> on page Appx-B-168	r0p0

**Table C-3 Differences between issue 0000-01 and issue 0002-00**

Change	Location	Affects
Updated section	<a href="#">1.1 About the GIC-600</a> on page 1-12	All releases
Updated section	<a href="#">1.2 Components</a> on page 1-13	All releases
Updated Figure	<a href="#">Figure 1-1 GIC-600 with free-flowing interconnect in an example system</a> on page 1-14	All releases
Updated Figure	<a href="#">Figure 1-2 GIC-600 with interconnect in an example system</a> on page 1-15	All releases
Updated Figure	<a href="#">Figure 1-3 Monolithic GIC-600 with interconnect in an example system</a> on page 1-16	All releases
Updated section	<a href="#">1.3 Compliance</a> on page 1-17	All releases
Updated section	<a href="#">1.4 Features</a> on page 1-18	All releases
Updated Figure	<a href="#">Figure 2-1 GIC-600 Distributor</a> on page 2-23	All releases
Updated section	<a href="#">2.1.1 Distributor AXI4-Stream interfaces</a> on page 2-24	All releases
Updated section	<a href="#">2.1.2 Distributor ACE-Lite slave interface</a> on page 2-24	All releases
Updated section	<a href="#">2.1.3 Distributor ACE-Lite master interface</a> on page 2-25	All releases
Updated section	<a href="#">2.1.4 Distributor Q-Channels</a> on page 2-26	All releases
Updated table	<a href="#">2.1.5 Distributor miscellaneous signals</a> on page 2-26	All releases
Updated table	<a href="#">Table 2-6 Configurable options for the Distributor</a> on page 2-27	All releases
Updated section	<a href="#">2.2 Redistributor</a> on page 2-29	All releases
Updated section	<a href="#">2.2.2 Redistributor GIC Stream protocol interface</a> on page 2-30	All releases
Added table	<a href="#">Table 2-7 GIC Stream protocol interface signals</a> on page 2-30	All releases
Updated section	<a href="#">2.2.4 Redistributor PPI signals</a> on page 2-30	All releases
Updated section	<a href="#">2.2.5 Redistributor miscellaneous input signals</a> on page 2-31	All releases
Updated section	<a href="#">2.3 ITS</a> on page 2-32	All releases
Updated section	<a href="#">2.3.1 ITS ACE-Lite slave interface</a> on page 2-33	All releases
Updated section	<a href="#">2.3.4 ITS Q-Channel</a> on page 2-35	All releases
Updated table	<a href="#">Table 2-11 ITS miscellaneous signals</a> on page 2-36	All releases
Updated section	<a href="#">2.4 MSI-64 Encapsulator</a> on page 2-37	All releases
Updated section	<a href="#">2.4.2 MSI-64 miscellaneous signals</a> on page 2-38	All releases

**Table C-3 Differences between issue 0000-01 and issue 0002-00 (continued)**

<b>Change</b>	<b>Location</b>	<b>Affects</b>
Updated section	<a href="#">2.4.3 MSI-64 Encapsulator configuration on page 2-38</a>	All releases
Updated section	<a href="#">2.5 SPI Collator on page 2-40</a>	All releases
Updated section	<a href="#">2.5.1 SPI Collator AXI4-Stream interface on page 2-40</a>	All releases
Updated section	<a href="#">2.5.2 SPI Collator wires on page 2-40</a>	All releases
Updated section	<a href="#">2.5.3 SPI Collator Q-Channel on page 2-40</a>	All releases
Updated section	<a href="#">2.6 Wake Request on page 2-42</a>	All releases
Updated section	<a href="#">2.6.3 Wake Request configuration on page 2-42</a>	All releases
Updated section	<a href="#">2.8 Top-level interfaces on page 2-44</a>	All releases
Updated Figure	<a href="#">Figure 2-8 GIC top-level structure options on page 2-45</a>	All releases
Renamed Chapter 3	<a href="#">Chapter 3 Single-chip operation on page 3-47</a>	All releases
Updated section	<a href="#">3.1.1 SGIs on page 3-48</a>	All releases
Updated section	<a href="#">3.1.2 PPIs on page 3-48</a>	All releases
Updated section	<a href="#">3.1.3 SPIs on page 3-48</a>	All releases
Updated section	<a href="#">3.1.4 LPIs on page 3-49</a>	All releases
Updated section	<a href="#">3.2.1 Interrupt groups on page 3-50</a>	All releases
Updated section	<a href="#">3.2.2 Interrupt signals (PPIs and SPIs) on page 3-50</a>	All releases
Updated section	<a href="#">3.2.3 Affinity routing and assignment on page 3-51</a>	All releases
Updated section	<a href="#">3.2.4 1 of N SPI interrupt selection on page 3-52</a>	All releases
Updated section	<a href="#">3.2.5 Power management on page 3-53</a>	All releases
Updated section	<a href="#">3.2.7 Security on page 3-56</a>	All releases
Updated section	<a href="#">3.2.8 Backwards compatibility on page 3-57</a>	All releases
Updated section	<a href="#">3.2.9 Interrupt translation service (ITS) on page 3-57</a>	All releases
Updated section	<a href="#">3.2.11 Memory access and attributes on page 3-60</a>	All releases
Updated headings in Table	<a href="#">Table 3-5 Cacheability values on page 3-61</a>	All releases
Updated section	<a href="#">3.2.12 MSI-64 on page 3-62</a>	All releases
Updated section	<a href="#">3.2.13 RAM on page 3-62</a>	All releases
Updated section	<a href="#">3.2.15 Reliability, Accessibility, and Serviceability on page 3-64</a>	All releases
Updated section	<a href="#">4.1.2 Discovery on page 4-85</a>	All releases
Updated section	<a href="#">4.2 Distributor registers (GICD/GICDA) summary on page 4-86</a>	All releases
Updated section	<a href="#">4.2.5 Interrupt Class Registers, GICD_ICLARn on page 4-92</a>	All releases
Updated table	<a href="#">Table 4-24 GICR_SGIDR bit assignments on page 4-110</a>	All releases
Updated table	<a href="#">Table 4-25 GICR_CFGID0 bit assignments on page 4-111</a>	All releases
Updated table	<a href="#">Table 4-26 GICR_CFGID1 bit assignments on page 4-112</a>	All releases
Updated table	<a href="#">Table 4-30 GITS_FCTLR bit assignments on page 4-117</a>	All releases
Updated section	<a href="#">4.6.5 Operation Status Register, GITS_OPSR on page 4-119</a>	All releases

**Table C-3 Differences between issue 0000-01 and issue 0002-00 (continued)**

Change	Location	Affects
Updated table	<a href="#">Table 4-32 GITS_OPSR bit assignments</a> on page 4-120	All releases
Updated section	<a href="#">4.7 ITS translation register summary</a> on page 4-122	All releases
Updated table	<a href="#">Table 4-40 GICT_ERR&lt;n&gt;STATUS bit assignments</a> on page 4-128	All releases
Updated section	<a href="#">4.8.4 Error Record Address Register, GICT_ERR&lt;n&gt;ADDR</a> on page 4-128	All releases
Updated section	<a href="#">4.8.5 Error Record Miscellaneous Register 0, GICT_ERR&lt;n&gt;MISC0</a> on page 4-129	All releases
Updated table	<a href="#">Table 4-42 GICT_ERR&lt;n&gt;MISC0 bit assignments</a> on page 4-130	All releases
Updated table	<a href="#">Table 4-43 Data field encoding</a> on page 4-130	All releases
Updated section	<a href="#">4.8.6 Error Record Miscellaneous Register 1, GICT_ERR&lt;n&gt;MISC1</a> on page 4-135	All releases
Updated table	<a href="#">Table 4-44 GICT_ERR10MISC1 bit assignments</a> on page 4-136	All releases
Updated section	<a href="#">4.9.2 Event Type Configuration Registers, GICP_EVTYPEn</a> on page 4-139	All releases
Updated tables	<a href="#">GICP_EVTYPEn bit assignments</a> on page 4-140 and <a href="#">Table 4-50 EVENT field encoding</a> on page 4-140	All releases
Updated section	<a href="#">A.2 Power control signals</a> on page Appx-A-155	All releases
Updated section	<a href="#">A.4 CPU interface signals</a> on page Appx-A-157	All releases
Updated section	<a href="#">A.5 ACE interface signals</a> on page Appx-A-158	All releases
Updated section	<a href="#">A.6 Miscellaneous signals</a> on page Appx-A-163	All releases
Updated section	<a href="#">A.7 Interblock signals</a> on page Appx-A-164	All releases
Added section	<a href="#">A.8 Interdomain signals</a> on page Appx-A-166	All releases
Updated section	<a href="#">B.1 Implementation-defined features reference</a> on page Appx-B-168	All releases

**Table C-4 Differences between issue 0002-00 and issue 0002-01**

Change	Location	Affects
No technical changes	-	-