ARM® CoreLink™ DMC-520 Dynamic Memory Controller

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Technical Reference Manual

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ARM® CoreLink™ DMC-520 Dynamic Memory Controller

Technical Reference Manual

Release information

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Product status

The information in this document is Final, that is for a developed product.

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Preface

This preface introduces the *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Technical Reference Manual*.

It contains the following:

- *About this book* on page 7.
- *Feedback* on page 10.

About this book

This book is for the ARM® CoreLink™ DMC-520 Dynamic Memory Controller.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced engineers who want to integrate the delivered ARM DMC-520 product in a *System on Chip* (SoC) design.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter describes the DMC-520.

Chapter 2 Functional Description
This chapter describes how the DMC-520 operates.

Chapter 3 Programmers Model
This chapter describes the programmers model of the DMC-520.

Appendix A Signal Descriptions
This appendix describes the DMC-520 signals.

Appendix B Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

<and>
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

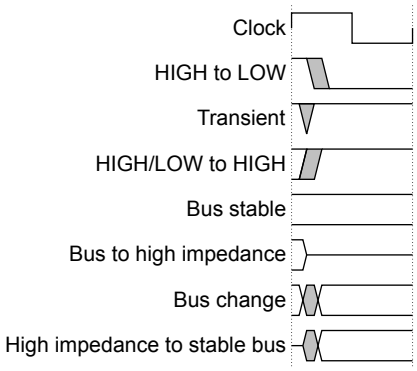

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n
: At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

ARM publications

- *ARM® AMBA® APB Protocol Specification* (ARM IHI 0024).
- *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *Principles of ARM® Memory Maps White Paper* (ARM DEN 0001).

The following confidential books are only available to licensees:

- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Design Manual* (ARM 100001).
- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Integration Manual* (ARM 100003).
- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Implementation Guide* (ARM 100002).
- *ARM® AMBA® 5 CHI Architecture Specification* (ARM IHI 0050).
- *ARM® CoreLink™ CCN-504 Cache Coherent Network Technical Reference Manual* (ARM 100017).

Other publications

- *JEDEC STANDARD DDR3 SDRAM Specification*, JESD79-3D, *http://www.jedec.org*.
- *JEDEC STANDARD DDR3L SDRAM Specification*, JESD79-3-1A, *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 SDRAM Specification*, JESD79-4, *http://www.jedec.org*.
- *JEDEC STANDARD DDR3 RDIMM Specification*, JESD82-29, *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 RDIMM Common Design Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 LRDIMM Common Design Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 RCD Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 DB Specification*, (pre-release), *http://www.jedec.org*.
- *DDR PHY Interface DFI 3.1 Specification*, *http://ddr-phy.org/*.

Note

See the *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Release Note* for the actual versions of the specifications that ARM used when designing the device.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Technical Reference Manual*.
- The number ARM 100000_0202_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

ARM tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter describes the DMC-520.

It contains the following sections:

- *1.1 About the product* on page 1-12.
- *1.2 DMC-520 compliance* on page 1-13.
- *1.3 Features* on page 1-14.
- *1.4 Interfaces* on page 1-15.
- *1.5 Configurable options* on page 1-16.
- *1.6 Test features* on page 1-17.
- *1.7 Product documentation and design flow* on page 1-18.
- *1.8 Product revisions* on page 1-20.

1.1 About the product

This is a high-level overview of the DMC-520.

The DMC-520 is an ARM AMBA 5 CHI SoC peripheral developed, tested, and licensed by ARM. It is a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol. It supports the following memory devices:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

The following figure shows an example system.

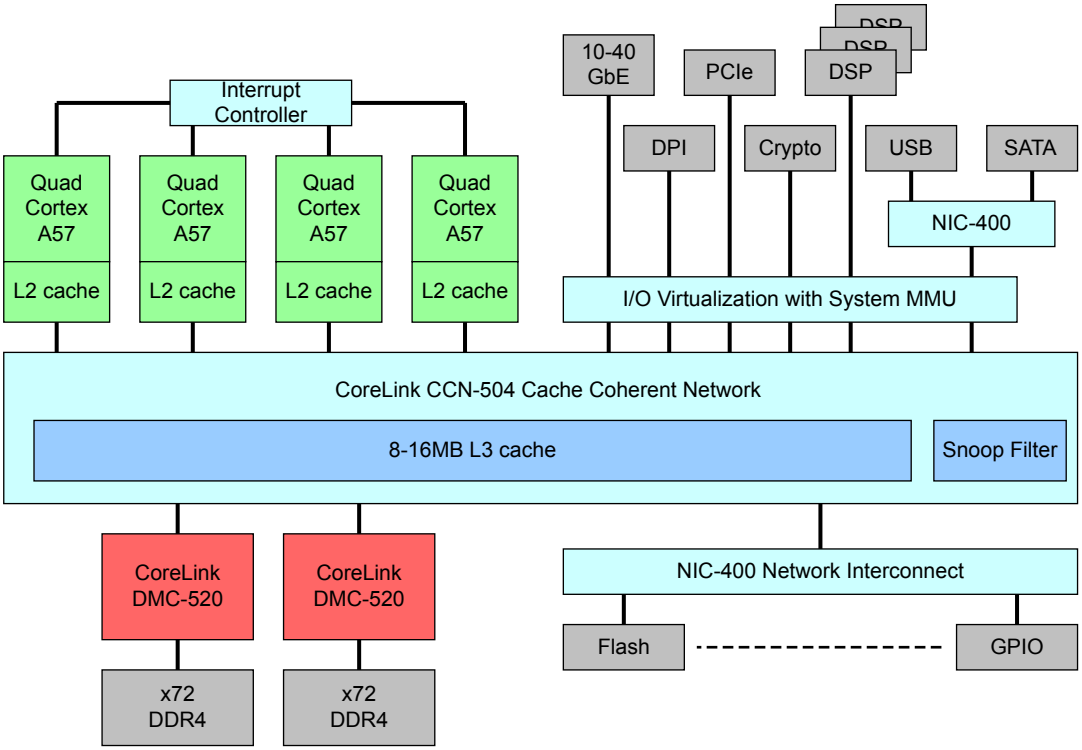

Figure 1-1 Example system

The DMC-520 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface and to a processor through the programmers APB3 interface to program the DMC-520. It connects to the SDRAM devices through its memory interface block and the *DDR PHY Interface* (DFI).

1.2 DMC-520 compliance

The DMC-520 is compatible with the following protocol specifications and standards:

- AMBA 5 CHI protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR4 Memory Buffer Spec Proposal.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- DFI 3.1.

1.3 Features

The DMC-520 supports DDR3 and DDR4 SDRAMs. It also supports error checking, reliability, availability, and serviceability features. In addition, *Quality of Service* (QoS) features and ARM TrustZone® architecture security extensions are built in throughout the controller.

The system interface provides a CHI interface for connection to a CoreLink *Cache Coherent Network* (CCN), an APB3 interface for configuration and initialization purposes, and an external performance event interface for connecting to CoreSight™ on-chip debug and trace technology.

The DMC-520 has the following features:

- Profiling signals that enable performance profiling to be performed in the system.
- TrustZone architecture security extensions.
- Buffering to optimize read and write turnaround and to maximize bandwidth.
- A system interface that provides:
  - A CHI interface to connect to a CCN.
  - An APB3 interface for configuration and initialization purposes.
- A *Memory Interface* (MI) that provides:
  - A DFI interface to a PHY that supports DDR3, DDR3L, and DDR4.
  - Support for DFI 1:1, 1:2, and 1:4 DFI frequency ratio modes.
  - Support for either a 32-bit wide data SDRAM interface or a 64-bit wide data SDRAM interface.
- Low-power operation through programmable SDRAM power modes.
- *Reliability, Availability, Serviceability* (RAS):
  - *Single Error Correcting, Double Error Detecting* (SECDED) *Error-Correcting Code* (ECC) for off-chip DRAM.
  - Symbol-based ECC, to correct memory chip and data-lane failures.
  - SECDED ECC for on-chip RAM protection.
  - Hardware *Read-Modify-Write* (RMW) for systems supporting sparse writes.
  - *Command-Address* (CA) parity checks for DDR3 and DDR4 link errors.
  - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling and automated recovery.
- Refresh Control Logic for memory banks.
- Power Control Logic that generates powerdown requests to the SDRAM, and manages power enables for the PHY logic.

1.4 Interfaces

This section lists the interfaces in the DMC-520.

The DMC-520 has the following external interfaces:

- A system interface to provide read and write access to or from a master that supports the CHI protocol.
- An APB3 programmers interface to program and control the DMC-520.
- A DFI-compatible PHY interface to transfer data to and from the external memory.
- A profile and debug interface.
- A low-power clock control interface that uses the Q-Channel protocol. See *Q-Channel interface* on page 2-27.
- An abort interface that is a 4-phase request and acknowledge handshake that you can use to recover from a livelock that is caused by DRAM or PHY failure.
- User I/O ports.
- A set of interrupts that are used to report operational events and detected faults.

1.5 Configurable options

The DMC-520 has the following configurable options:

The different DFI frequency ratios that the DMC can support are defined in the *DFI* specification. The DMC supports the following options:

- 1:1 Frequency Ratio Mode where **dfi_clk** = SDRAM CLK.
- 1:2 Frequency Ratio Mode where **dfi_clk** = ½×SDRAM CLK.
- 1:4 Frequency Ratio Mode where **dfi_clk** = ¼×SDRAM CLK.

——— **Note** ———

The DFI Frequency Ratio is the only configurable option for the DMC-520.

———————————

1.6 Test features

The DMC-520 provides the following test features:

- Integration test logic for integration testing.
- A debug and profile interface to enable you to monitor transaction events.

1.7 Product documentation and design flow

This section describes the DMC-520 books and how they relate to the design flow.

Documentation

The DMC-520 documentation is as follows:

Technical Reference Manual
The *Technical Reference Manual* (TRM) summarizes the functionality of the DMC, and describes its signals.

Design Manual
The *Design Manual* (DM) describes the functionality and the effects of functional options on the behavior of the DMC. It is required at all stages of the design flow. The choices that are made in the design flow can mean that some behavior described in the DM is not relevant. If you are programming the DMC, then contact:

- The implementer to determine what integration, if any, was performed before implementing the DMC.
- The integrator to determine the pin configuration of the device that you are using.

The DM is a confidential book that is only available to licensees.

Implementation Guide
The *Implementation Guide* (IG) describes:

- How to synthesize the *Register Transfer Level* (RTL).
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Contact your EDA vendor for EDA tool support.

The IG is a confidential book that is only available to licensees.

Integration Manual
The *Integration Manual* (IM) describes how to integrate the DMC into a SoC. It includes a description of the pins that the integrator must tie off to connect the DMC into an SoC design or to other IP.

The IM is a confidential book that is only available to licensees.

Design flow

The DMC-520 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation
The implementer synthesizes the RTL to produce a hard macrocell. This includes integrating RAMs into the design.

Integration
The integrator connects the implemented design into a SoC. This includes connecting it to a memory system.

Programming
This is the last process. The system programmer develops the software that is required to initialize the DMC, and tests the required application software.

Each process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the DMC.

The operation of the final device depends on:

Configuration inputs
: The integrator configures some features of the DMC by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software programming
: The programmer configures the DMC by programming particular values into registers. This affects the behavior of the DMC.

——— **Note** ———

This manual refers to implementation-defined features. Reference to a feature that is included means that the appropriate signal configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

———————————

1.8 Product revisions

This section describes the differences in functionality between product revisions of the DMC-520.

r0p0 First release.

r0p0-r0p1
- Updated DIMM support.
- Updated address mode.
- Updated the scrub engine operation.
- Added an optimized 2-cycle preamble bus turnaround function.
- Added update interrupts and DCI update options.
- Added rank mask capability.
- Added pwakeup.
- Updated DFT signals to latest standard.

r0p1-r1p0 Added 32-bit memory interface support.

r1p0-r2p0 Added configurable support for 1:1, 1:2, and 1:4 DFI frequency ratio modes.

r2p0-r2p1
- Added the phy_request_cs_remap, phy_rdwrdata_cs_mask_31_00, and phy_rdwrdata_cs_mask_63_32 registers.
- Added the sparse_3ds_cs bit to the feature_config register.

r2p1-r2p2
- Updated the functionality of ODT.

Chapter 2
Functional Description

This chapter describes how the DMC-520 operates.

It contains the following sections:

- *2.1 About the functions* on page 2-22.
- *2.2 Clocking and resets* on page 2-24.
- *2.3 Interfaces* on page 2-25.
- *2.4 Constraints and limitations of use* on page 2-29.

2.1 About the functions

This section gives a brief description of all the functions of the device.

The following figure shows a block diagram of the functions of the DMC-520. The colors show the different categories of functions:

- Blue indicates the blocks that are associated with data flow. The System interface is an example.
- Green indicates the blocks that are associated with programming. The Programming interface is an example.
- Orange indicates the blocks that are associated with the quality and efficiency of the communication to its external memory. The QoS engine is an example.

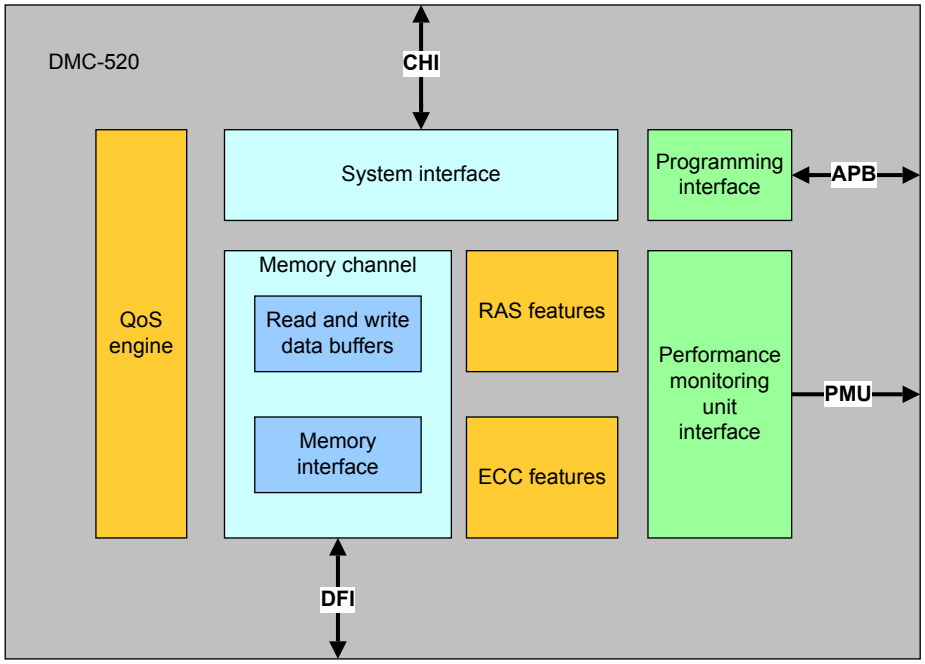

Figure 2-1 DMC functional block diagram

System interface

The DMC-520 interfaces to the rest of the SoC through the System interface. This interface connects to a CHI *Slave Node* (SN-F) interface. For any attempted accesses that the system makes outside of the programmed address range of the DMC-520, the System interface responds with a *Non-data Error* (NDERR) response. Depending on how you program the DMC-520, it converts the system access information to the correct rank, bank, column, and row access of the external SDRAM that connects to it. The System interface supports TrustZone features to regulate Secure and Non-secure accesses to both Secure and Non-secure regions of memory.

The DMC monitors queue occupancies and dictates whether system requests of any given QoS are accepted. Prefetched and Dynamic P-Credit requests are allocated based on a threshold setting, which is derived from register settings.

Note

There is no support for exclusive access in the DMC because the CoreLink CCN-5xx product family supports exclusive access requests in the *Home Node* (HN-F).

Memory channel

Through this interface, the DMC-520 conducts its data transactions with the SDRAM and regulates the power consumption of the SDRAM. The DMC-520 uses the ECC information that it receives from the SDRAM to maximize the reliability from these devices.

Programming interface

Through this interface, a master in the system programs the DMC-520. You can define the Secure and Non-secure regions of external memory and also define how the DMC-520 addresses the external memory, from the address that the system provides on its system interface. You can also make direct accesses to the SDRAM, for example to initialize it.

Performance Monitoring Unit interface

You can use the *Performance Monitoring Unit* (PMU) interface to monitor the performance and power settings for your specific application. This interface allows you to monitor the inner workings of the device and so enables additional information to be viewed.

QoS engine

The DMC-520 provides controls to enable you to adjust its arbitration scheme for your system to maximize the availability of your external memory devices. It provides buffers to re-order system transaction requests. It uses an advanced scheduling algorithm to ensure that traffic going to one memory bank causes minimal disruption to traffic going to a different memory bank. It also schedules transaction requests according to the availability of the destination memory bank. For system access requests to different available memory banks, the DMC-520 arbitrates these requests using the QoS priority initially and then the temporal priority. These memory access requests all compete for control of the external SDRAM bus and SDRAM bank availability.

RAS

RAS features include support for the following:

- SECDED ECC and symbol-based ECC for external DRAM. The symbol-based ECC performs quad-symbol correct and multi-symbol detect.
- SECDED ECC of on-chip SRAM buffers within the DMC-520.
- An automated retry of failed read transactions.
- Write-back of corrected errors.
- To improve containment of faults, the DMC-520 supports:
  - Link error protection for the memory interface, including automated hardware recovery for system memory access, training, and other hardware operations.
  - Programmable data scrubbing. The DMC-520 periodically detects and corrects data errors in the memory autonomously.

2.2 Clocking and resets

The DMC-520 normally operates as one synchronous clock domain between the interconnect and the external DDR interface. However, the programming interface can operate asynchronously to this.

This section shows the clock and reset signals that the DMC-520 requires.

Clocks

There are either two or three clock inputs depending on the DFI frequency ratio configuration:

- **clk**. This is the main DMC clock that runs at SDRAM clock frequency. It must run synchronous to, and at the same frequency, as the CHI interface. If the CHI interface is not running at SDRAM clock frequency, then a *Device Source Synchronous Bridge* (DSSB), which is part of the CCN product must be used. When in a 1:1 DFI frequency ratio mode, this clock also serves as the **dfi clk**.
- **dfi_clk**. This clock port only exists if the DMC is in 1:2 or 1:4 mode. The clock runs the DFI interface and connects to both the DMC and the PHY. It must be edge synchronous to **clk**, and run at half the **clk** frequency if it is in the 1:2 configuration or one quarter the **clk** frequency when in the 1:4 configuration.
- **pclk**. This can run asynchronously to **clk** and **dfi clk**.

Reset

Resets must be applied for a minimum duration of 16 clock cycles for each clock domain.

There are two reset inputs. **RESETn** resets both **clk** and **dfi clk** registers and **PRESETn** resets **pclk** registers. The **pclk** domain must be brought out of reset prior to the **clk** and **dfi clk** domains.

Note

- To assert any DMC-520 reset signal, you must set it LOW.
- To perform a DMC-520 reset, you must assert both reset signals.

Related references

Appendix A Signal Descriptions on page Appx-A-144.

2.3 Interfaces

This section describes the interfaces of the DMC-520, as the following figure shows.

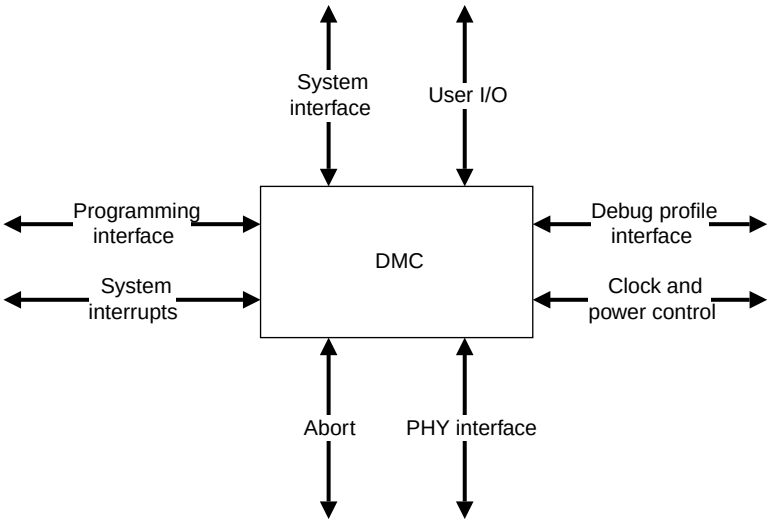

Figure 2-2 Interfaces of the DMC-520

This section contains the following subsections:

- *2.3.1 System interface* on page 2-25.
- *2.3.2 Programming interface* on page 2-25.
- *2.3.3 PHY interface* on page 2-25.
- *2.3.4 Profile and debug interface* on page 2-26.
- *2.3.5 Low-power clock control interface* on page 2-26.
- *2.3.6 Abort interface* on page 2-28.

2.3.1 System interface

This section describes the function of the System interface.

The System Interface provides protocol conversion between CHI and internal read/write requests. Because CHI is packet-based and a slave node only supports read and write semantics, this translation is straightforward at a transaction level because no transformation function is performed.

2.3.2 Programming interface

This section describes the APB3 interface, used for programming the DMC-520.

The AMBA APB3 slave interface allows software to configure the controller and to initialize the memory devices. The APB3 programming interface also provides a means of performing architectural state transitions in addition to querying certain debug and profile information. The interface is a memory-mapped register interface.

2.3.3 PHY interface

The PHY interface provides command scheduling and arbitration, including the generation of any required SDRAM prepare commands, for example, ACTIVATE and PRECHARGE.

The PHY interface is compatible with the DDR standards for DDR4 and DDR3 (including DDR3L). It provides:

- Command scheduling and arbitration, including generation of any required SDRAM prepare commands, for example, ACTIVATE or PRECHARGE.
- Automated AUTOREFRESH command generation.

- SDRAM interface link protection including automated retries for failed commands to ensure the correct ordering of those retried commands to SDRAM.
- Automated SDRAM and PHY logic power control.
- Profile and debug information.
- Support for DFI 1:1, 1:2, and 1:4 frequency ratio modes.

2.3.4 Profile and debug interface

This section describes the profile and debug interface in the DMC-520.

The DMC-520 provides programmable features that allow system designers and software developers to fine-tune performance and power settings for their applications. A number of events can be monitored and the statistics used to fine-tune the performance of the controller by statically, or dynamically, altering the programmed state.

The information is made available through output pins that the system integrator must connect to an external monitoring unit.

The following events are monitored:
- Channel utilization.
- Channel and chip power state information.
- Bank utilization.
- Bank distribution.
- Activation rate.
- Read and write turnaround frequency.
- Read and write buffer fill status and the frequency of full events.
- Thresholding asserting back pressure.
- Arbitration decisions made where QoS is prioritized over efficiency.
- *Read-Modify-Write* (RMW) frequency.
- Timeouts and deadline events.

Each event is implemented as a pair of signals, VALID, and either PAYLOAD or a permanently valid PAYLOAD signal.

The Profile and Debug event interface can be connected to a generic event counter block, where any combination of the signals can be logged and tracked, depending on your system requirements.

2.3.5 Low-power clock control interface

This section describes the clock requirements for the DMC-520.

The DMC-520 provides a low-power control interface using the Q-Channel protocol. This is used to place the DMC into its low-power state, in which state the clock can be removed. The system can use the APB interface to put the DMC into its low-power state, and take it out of its low-power state.

SDRAM provides a number of power-saving states, as distinct from those of the DMC-520:

1. Idle-ready.
2. Clock stop.
3. Active power down.
4. Precharge power down.
5. *Self-Refresh* (SR).
6. *Maximum Power Down* (MPD) for DDR4.

All states prohibit commands apart from Idle-ready. From states 2-6, the energy saving increases, but so does the exit latency from that state. Some SDRAMs do not support dynamic clock stopping or MPD. Specific commands, together with the clock-enable **CKE** signal, are used to control states 2-5. Individual **CKE** pins are required for each chip that requires separate power control.

The features of the DMC-520 include:

- Separate clock and **CKE** controls for each chip select, with a set of multiplexer options to support standard DIMM configurations.
- Automated power control of SDRAM power modes based on an enable and timer. See *3.3.8 low_power_control_next* on page 3-46.
- Clock stop functionality that differs between memory devices. A programmable register controls this behavior. See *3.3.8 low_power_control_next* on page 3-46.
- Auto powerdown with minimal or no latency penalty on wakeup.
- Auto self-refresh functionality. The time delay before entry to self-refresh can be timed in refresh periods. When in self-refresh, a chip only comes out of self-refresh in response to system commands.
- Software-controlled low-power entry through the APB programming interface.
- A Q-Channel interface for hardware to control entry into the SR states. See *Q-Channel interface* on page 2-27.
- A separate low-power interface to allow clock stopping of the programming interface.

  ——— **Note** ———

  The DMC-520 does not allow multiple methods of low-power entry, either software or hardware, that are used at the same time. This is a restriction imposed on the system design.

  ———————————

The PHY logic consumes power in standby mode. If the controller is using SDRAM low-power modes, then it indicates to the PHY that it can power down. The wakeup value that the DMC signals to the PHY with the powerdown request determines the level of power state that the PHY enters. The wakeup value is determined from a programmed value that is associated with each SDRAM power-saving state. These states are:

- Configuration.
- Idle.
- Power-down.
- Self-refresh.
- MPD.

——— **Note** ———

The DMC can also indicate that the PHY must power down in the following ways:

- As a direct command from software, with a software-defined wakeup value.
- As part of a Q-Channel sequence, with a tie-off defined wakeup value.

———————————

Q-Channel interface

The DMC has a Q-Channel interface that allows an external power controller to place the DMC into a low-power state.

It is a standard Q-Channel interface as defined in the *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* using the following 4 signals.

- **qactive**.
- **qreqn**.
- **qacceptn**.
- **qdeny**.

When the DMC receives a request, it puts the DRAM into self_refresh before asserting **qacceptn** to accept the request that indicates the clk can be stopped.

DMC denies requests to power down using the Q-Channel when geardown_mode is enabled. In this case low-power mode can still be entered using the APB interface.

There is a separate Q-Channel interface for the **pclk** using the following signals:

- **qactive_apb**.
- **qreqn_apb**.

- **qacceptn_apb**.
- **qdeny_apb**.

The DMC never denies a request to power down the APB clock although it might be delayed based on APB activity.

Note

These two interfaces are interrelated and a change on one can cause **qactive** on the other to be asserted. If this occurs then the powerup request must be responded to in a timely fashion to allow the request to be serviced.

See *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces*.

2.3.6 Abort interface

When a fault is detected on the DFI interface, it causes repeated retries of commands on the memory interface. The abort interface is a 4-phase request and acknowledge handshake that the DMC can use to recover from a livelock caused by a DRAM failure or a PHY failure.

The following diagram shows the request, acknowledge handshake.

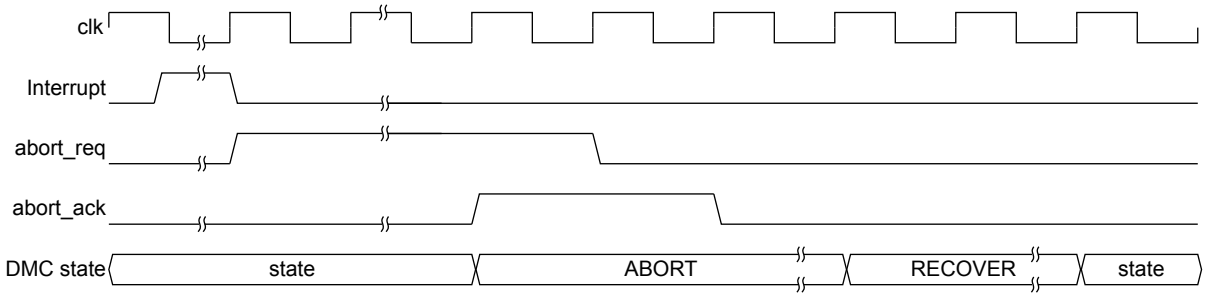

Figure 2-3 Abort interface timing diagram

The system can issue an abort at any time, which puts the DMC into the ABORT architectural state. Software must then restore the memory state. All current system transactions are retried after software restores the memory state and puts the DMC back into the Ready state.

2.4 Constraints and limitations of use

The constraints and limitations of the DMC-520 depend on the SDRAMs used, and the interoperability within the PHYs. This, in turn, depends on the *DDR Physical Interface* (DFI) parameters.

The SDRAMs supported by the DMC-520 are:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

——— **Note** ———

These devices are described in the JEDEC specifications that are global standards for the microelectronics industry.

———————————

The DIMMs supported by the DMC-520 are:

- DDR3 UDIMM.
- DDR3 RDIMM.
- DDR4 UDIMM.
- DDR4 RDIMM.
- DDR4 LRDIMM.
- DDR4 3DS. DIMMs utilizing 3DS parts are supported.

Chapter 3
Programmers Model

This chapter describes the programmers model of the DMC-520.

It contains the following sections:

- *3.1 About this programmers model* on page 3-31.
- *3.2 Register summary* on page 3-32.
- *3.3 Register descriptions* on page 3-44.

3.1 About this programmers model

The following information applies to the dmc520 registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to the reset value specified in the *3.2 Register summary* on page 3-32
- Access type is described as follows:

  RW Read and write.

  RO Read only.

  WO Write only.

3.2 Register summary

The following table shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000	memc_status	RO	0x00000000	32	*3.3.1 memc_status* on page 3-44
0x004	memc_config	RO	0x00000000	32	*3.3.2 memc_config* on page 3-44
0x008	memc_cmd	WO	0x00000000	32	*3.3.3 memc_cmd* on page 3-44
0x010	address_control_next	RW	0x00030202	32	*3.3.4 address_control_next* on page 3-45
0x014	decode_control_next	RW	0x00000000	32	*3.3.5 decode_control_next* on page 3-45
0x018	format_control	RW	0x22000213	32	*3.3.6 format_control* on page 3-45
0x01C	address_map_next	RW	0x00000000	32	*3.3.7 address_map_next* on page 3-45
0x020	low_power_control_next	RW	0x00000020	32	*3.3.8 low_power_control_next* on page 3-46
0x028	turnaround_control_next	RW	0x0F0F0F0F	32	*3.3.9 turnaround_control_next* on page 3-46
0x02C	hit_turnaround_control_next	RW	0x08909FBF	32	*3.3.10 hit_turnaround_control_next* on page 3-46
0x030	qos_class_control_next	RW	0x00000FC8	32	*3.3.11 qos_class_control_next* on page 3-47
0x034	escalation_control_next	RW	0x00080F03	32	*3.3.12 escalation_control_next* on page 3-47
0x038	qv_control_31_00_next	RW	0x76543210	32	*3.3.13 qv_control_31_00_next* on page 3-47
0x03C	qv_control_63_32_next	RW	0xFEDCBA98	32	*3.3.14 qv_control_63_32_next* on page 3-47
0x040	rt_control_31_00_next	RW	0x00000000	32	*3.3.15 rt_control_31_00_next* on page 3-48
0x044	rt_control_63_32_next	RW	0x00000000	32	*3.3.16 rt_control_63_32_next* on page 3-48
0x048	timeout_control_next	RW	0x00000001	32	*3.3.17 timeout_control_next* on page 3-48
0x04C	credit_control_next	RW	0x00000F03	32	*3.3.18 credit_control_next* on page 3-49
0x050	write_priority_control_31_00_next	RW	0x00000000	32	*3.3.19 write_priority_control_31_00_next* on page 3-49
0x054	write_priority_control_63_32_next	RW	0x00000000	32	*3.3.20 write_priority_control_63_32_next* on page 3-49
0x060	queue_threshold_control_31_00_next	RW	0x00000000	32	*3.3.21 queue_threshold_control_31_00_next* on page 3-49
0x064	queue_threshold_control_63_32_next	RW	0x00000000	32	*3.3.22 queue_threshold_control_63_32_next* on page 3-50
0x078	memory_address_max_31_00_next	RW	0x00000010	32	*3.3.23 memory_address_max_31_00_next* on page 3-50
0x07C	memory_address_max_43_32_next	RW	0x00000000	32	*3.3.24 memory_address_max_43_32_next* on page 3-50
0x080	access_address_min0_31_00_next	RW	0x00000000	32	*3.3.25 access_address_min0_31_00_next* on page 3-51
0x084	access_address_min0_43_32_next	RW	0x00000000	32	*3.3.26 access_address_min0_43_32_next* on page 3-51

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x088	access_address_max0_31_00_next	RW	0x00000000	32	*3.3.27 access_address_max0_31_00_next* on page 3-51
0x08C	access_address_max0_43_32_next	RW	0x00000000	32	*3.3.28 access_address_max0_43_32_next* on page 3-51
0x090	access_address_min1_31_00_next	RW	0x00000000	32	*3.3.29 access_address_min1_31_00_next* on page 3-52
0x094	access_address_min1_43_32_next	RW	0x00000000	32	*3.3.30 access_address_min1_43_32_next* on page 3-52
0x098	access_address_max1_31_00_next	RW	0x00000000	32	*3.3.31 access_address_max1_31_00_next* on page 3-52
0x09C	access_address_max1_43_32_next	RW	0x00000000	32	*3.3.32 access_address_max1_43_32_next* on page 3-53
0x0A0	access_address_min2_31_00_next	RW	0x00000000	32	*3.3.33 access_address_min2_31_00_next* on page 3-53
0x0A4	access_address_min2_43_32_next	RW	0x00000000	32	*3.3.34 access_address_min2_43_32_next* on page 3-53
0x0A8	access_address_max2_31_00_next	RW	0x00000000	32	*3.3.35 access_address_max2_31_00_next* on page 3-53
0x0AC	access_address_max2_43_32_next	RW	0x00000000	32	*3.3.36 access_address_max2_43_32_next* on page 3-54
0x0B0	access_address_min3_31_00_next	RW	0x00000000	32	*3.3.37 access_address_min3_31_00_next* on page 3-54
0x0B4	access_address_min3_43_32_next	RW	0x00000000	32	*3.3.38 access_address_min3_43_32_next* on page 3-54
0x0B8	access_address_max3_31_00_next	RW	0x00000000	32	*3.3.39 access_address_max3_31_00_next* on page 3-55
0x0BC	access_address_max3_43_32_next	RW	0x00000000	32	*3.3.40 access_address_max3_43_32_next* on page 3-55
0x0C0	access_address_min4_31_00_next	RW	0x00000000	32	*3.3.41 access_address_min4_31_00_next* on page 3-55
0x0C4	access_address_min4_43_32_next	RW	0x00000000	32	*3.3.42 access_address_min4_43_32_next* on page 3-55
0x0C8	access_address_max4_31_00_next	RW	0x00000000	32	*3.3.43 access_address_max4_31_00_next* on page 3-56
0x0CC	access_address_max4_43_32_next	RW	0x00000000	32	*3.3.44 access_address_max4_43_32_next* on page 3-56
0x0D0	access_address_min5_31_00_next	RW	0x00000000	32	*3.3.45 access_address_min5_31_00_next* on page 3-56
0x0D4	access_address_min5_43_32_next	RW	0x00000000	32	*3.3.46 access_address_min5_43_32_next* on page 3-57
0x0D8	access_address_max5_31_00_next	RW	0x00000000	32	*3.3.47 access_address_max5_31_00_next* on page 3-57

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0DC	access_address_max5_43_32_next	RW	0x00000000	32	*3.3.48 access_address_max5_43_32_next* on page 3-57
0x0E0	access_address_min6_31_00_next	RW	0x00000000	32	*3.3.49 access_address_min6_31_00_next* on page 3-57
0x0E4	access_address_min6_43_32_next	RW	0x00000000	32	*3.3.50 access_address_min6_43_32_next* on page 3-58
0x0E8	access_address_max6_31_00_next	RW	0x00000000	32	*3.3.51 access_address_max6_31_00_next* on page 3-58
0x0EC	access_address_max6_43_32_next	RW	0x00000000	32	*3.3.52 access_address_max6_43_32_next* on page 3-58
0x0F0	access_address_min7_31_00_next	RW	0x00000000	32	*3.3.53 access_address_min7_31_00_next* on page 3-59
0x0F4	access_address_min7_43_32_next	RW	0x00000000	32	*3.3.54 access_address_min7_43_32_next* on page 3-59
0x0F8	access_address_max7_31_00_next	RW	0x00000000	32	*3.3.55 access_address_max7_31_00_next* on page 3-59
0x0FC	access_address_max7_43_32_next	RW	0x00000000	32	*3.3.56 access_address_max7_43_32_next* on page 3-59
0x100	channel_status	RO	0x00000003	32	*3.3.57 channel_status* on page 3-60
0x108	direct_addr	RW	0x00000000	32	*3.3.58 direct_addr* on page 3-60
0x10C	direct_cmd	WO	0x00000000	32	*3.3.59 direct_cmd* on page 3-60
0x110	dci_replay_type_next	RW	0x00000002	32	*3.3.60 dci_replay_type_next* on page 3-61
0x118	dci_strb	RW	0x0000000F	32	*3.3.61 dci_strb* on page 3-61
0x11C	dci_data	RW	0x00000000	32	*3.3.62 dci_data* on page 3-61
0x120	refresh_control_next	RW	0x00000000	32	*3.3.63 refresh_control_next* on page 3-61
0x128	memory_type_next	RW	0x00000101	32	*3.3.64 memory_type_next* on page 3-62
0x130	feature_config	RW	0x000000F0	32	*3.3.65 feature_config* on page 3-62
0x138	nibble_failed_031_000	RW	0x00000000	32	*3.3.66 nibble_failed_031_000* on page 3-62
0x13C	nibble_failed_063_032	RW	0x00000000	32	*3.3.67 nibble_failed_063_032* on page 3-63
0x140	nibble_failed_095_064	RW	0x00000000	32	*3.3.68 nibble_failed_095_064* on page 3-63
0x144	nibble_failed_127_096	RW	0x00000000	32	*3.3.69 nibble_failed_127_096* on page 3-63
0x148	queue_allocate_control_031_000	RW	0xFFFFFFFF	32	*3.3.70 queue_allocate_control_031_000* on page 3-63
0x14C	queue_allocate_control_063_032	RW	0xFFFFFFFF	32	*3.3.71 queue_allocate_control_063_032* on page 3-64
0x150	queue_allocate_control_095_064	RW	0xFFFFFFFF	32	*3.3.72 queue_allocate_control_095_064* on page 3-64
0x154	queue_allocate_control_127_096	RW	0xFFFFFFFF	32	*3.3.73 queue_allocate_control_127_096* on page 3-64

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x158	ecc_errc_count_31_00	RW	0x00000000	32	*3.3.74 ecc_errc_count_31_00* on page 3-65
0x15C	ecc_errc_count_63_32	RW	0x00000000	32	*3.3.75 ecc_errc_count_63_32* on page 3-65
0x160	ecc_errd_count_31_00	RW	0x00000000	32	*3.3.76 ecc_errd_count_31_00* on page 3-65
0x164	ecc_errd_count_63_32	RW	0x00000000	32	*3.3.77 ecc_errd_count_63_32* on page 3-66
0x168	ram_err_count	RW	0x00000000	32	*3.3.78 ram_err_count* on page 3-66
0x16C	link_err_count	RW	0x00000000	32	*3.3.79 link_err_count* on page 3-66
0x170	scrub_control0_next	RW	0x1F000000	32	*3.3.80 scrub_control0_next* on page 3-66
0x174	scrub_address_min0_next	RW	0x00000000	32	*3.3.81 scrub_address_min0_next* on page 3-67
0x178	scrub_address_max0_next	RW	0x00000000	32	*3.3.82 scrub_address_max0_next* on page 3-67
0x180	scrub_control1_next	RW	0x1F000000	32	*3.3.83 scrub_control1_next* on page 3-67
0x184	scrub_address_min1_next	RW	0x00000000	32	*3.3.84 scrub_address_min1_next* on page 3-68
0x188	scrub_address_max1_next	RW	0x00000000	32	*3.3.85 scrub_address_max1_next* on page 3-68
0x190	scrub_control2_next	RW	0x1F000000	32	*3.3.86 scrub_control2_next* on page 3-68
0x194	scrub_address_min2_next	RW	0x00000000	32	*3.3.87 scrub_address_min2_next* on page 3-68
0x198	scrub_address_max2_next	RW	0x00000000	32	*3.3.88 scrub_address_max2_next* on page 3-69
0x1A0	scrub_control3_next	RW	0x1F000000	32	*3.3.89 scrub_control3_next* on page 3-69
0x1A4	scrub_address_min3_next	RW	0x00000000	32	*3.3.90 scrub_address_min3_next* on page 3-69
0x1A8	scrub_address_max3_next	RW	0x00000000	32	*3.3.91 scrub_address_max3_next* on page 3-70
0x1B0	scrub_control4_next	RW	0x1F000000	32	*3.3.92 scrub_control4_next* on page 3-70
0x1B4	scrub_address_min4_next	RW	0x00000000	32	*3.3.93 scrub_address_min4_next* on page 3-70
0x1B8	scrub_address_max4_next	RW	0x00000000	32	*3.3.94 scrub_address_max4_next* on page 3-70
0x1C0	scrub_control5_next	RW	0x1F000000	32	*3.3.95 scrub_control5_next* on page 3-71
0x1C4	scrub_address_min5_next	RW	0x00000000	32	*3.3.96 scrub_address_min5_next* on page 3-71
0x1C8	scrub_address_max5_next	RW	0x00000000	32	*3.3.97 scrub_address_max5_next* on page 3-71
0x1D0	scrub_control6_next	RW	0x1F000000	32	*3.3.98 scrub_control6_next* on page 3-72
0x1D4	scrub_address_min6_next	RW	0x00000000	32	*3.3.99 scrub_address_min6_next* on page 3-72
0x1D8	scrub_address_max6_next	RW	0x00000000	32	*3.3.100 scrub_address_max6_next* on page 3-72
0x1E0	scrub_control7_next	RW	0x1F000000	32	*3.3.101 scrub_control7_next* on page 3-72
0x1E4	scrub_address_min7_next	RW	0x00000000	32	*3.3.102 scrub_address_min7_next* on page 3-73
0x1E8	scrub_address_max7_next	RW	0x00000000	32	*3.3.103 scrub_address_max7_next* on page 3-73
0x1F0	feature_control_next	RW	0x0AA00000	32	*3.3.104 feature_control_next* on page 3-73
0x1F4	mux_control_next	RW	0x00000000	32	*3.3.105 mux_control_next* on page 3-74
0x1F8	rank_remap_control_next	RW	0x76543210	32	*3.3.106 rank_remap_control_next* on page 3-74
0x1FC	scrub_control_next	RW	0x00001F00	32	*3.3.107 scrub_control_next* on page 3-74
0x200	t_refi_next	RW	0x00090100	32	*3.3.108 t_refi_next* on page 3-74

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x204	t_rfc_next	RW	0x00008C23	32	*3.3.109 t_rfc_next* on page 3-75
0x208	t_mrr_next	RW	0x00000002	32	*3.3.110 t_mrr_next* on page 3-75
0x20C	t_mrw_next	RW	0x0000000C	32	*3.3.111 t_mrw_next* on page 3-75
0x210	t_rdpden_next	RW	0x0000000A	32	*3.3.112 t_rdpden_next* on page 3-76
0x218	t_rcd_next	RW	0x00000005	32	*3.3.113 t_rcd_next* on page 3-76
0x21C	t_ras_next	RW	0x0000000E	32	*3.3.114 t_ras_next* on page 3-76
0x220	t_rp_next	RW	0x00000005	32	*3.3.115 t_rp_next* on page 3-77
0x224	t_rpall_next	RW	0x00000005	32	*3.3.116 t_rpall_next* on page 3-77
0x228	t_rrd_next	RW	0x00000404	32	*3.3.117 t_rrd_next* on page 3-77
0x22C	t_act_window_next	RW	0x03560014	32	*3.3.118 t_act_window_next* on page 3-77
0x234	t_rtr_next	RW	0x00060404	32	*3.3.119 t_rtr_next* on page 3-78
0x238	t_rtw_next	RW	0x00060606	32	*3.3.120 t_rtw_next* on page 3-78
0x23C	t_rtp_next	RW	0x00000004	32	*3.3.121 t_rtp_next* on page 3-78
0x244	t_wr_next	RW	0x00000005	32	*3.3.122 t_wr_next* on page 3-79
0x248	t_wtr_next	RW	0x00040505	32	*3.3.123 t_wtr_next* on page 3-79
0x24C	t_wtw_next	RW	0x00060404	32	*3.3.124 t_wtw_next* on page 3-79
0x254	t_xmpd_next	RW	0x000003FF	32	*3.3.125 t_xmpd_next* on page 3-80
0x258	t_ep_next	RW	0x00000002	32	*3.3.126 t_ep_next* on page 3-80
0x25C	t_xp_next	RW	0x00060002	32	*3.3.127 t_xp_next* on page 3-80
0x260	t_esr_next	RW	0x0000000E	32	*3.3.128 t_esr_next* on page 3-80
0x264	t_xsr_next	RW	0x05120100	32	*3.3.129 t_xsr_next* on page 3-81
0x268	t_esrck_next	RW	0x00000005	32	*3.3.130 t_esrck_next* on page 3-81
0x26C	t_ckxsr_next	RW	0x00000001	32	*3.3.131 t_ckxsr_next* on page 3-81
0x270	t_cmd_next	RW	0x00000000	32	*3.3.132 t_cmd_next* on page 3-82
0x274	t_parity_next	RW	0x00000900	32	*3.3.133 t_parity_next* on page 3-82
0x278	t_zqcs_next	RW	0x00000040	32	*3.3.134 t_zqcs_next* on page 3-82
0x300	t_rddata_en_next	RW	0x00000001	32	*3.3.135 t_rddata_en_next* on page 3-83
0x304	t_phyrdlat_next	RW	0x00000000	32	*3.3.136 t_phyrdlat_next* on page 3-83
0x308	t_phywrlat_next	RW	0x00000001	32	*3.3.137 t_phywrlat_next* on page 3-83
0x310	rdlvl_control_next	RW	0x00001080	32	*3.3.138 rdlvl_control_next* on page 3-83
0x314	rdlvl_mrs_next	RW	0x00000004	32	*3.3.139 rdlvl_mrs_next* on page 3-84
0x318	t_rdlvl_en_next	RW	0x00000000	32	*3.3.140 t_rdlvl_en_next* on page 3-84
0x31C	t_rdlvl_rr_next	RW	0x00000000	32	*3.3.141 t_rdlvl_rr_next* on page 3-84
0x320	wrlvl_control_next	RW	0x00001000	32	*3.3.142 wrlvl_control_next* on page 3-85
0x324	wrlvl_mrs_next	RW	0x00000086	32	*3.3.143 wrlvl_mrs_next* on page 3-85

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x328	t_wrlvl_en_next	RW	0x00000000	32	*3.3.144 t_wrlvl_en_next* on page 3-85
0x32C	t_wrlvl_ww_next	RW	0x00000000	32	*3.3.145 t_wrlvl_ww_next* on page 3-86
0x348	phy_power_control_next	RW	0x00000000	32	*3.3.146 phy_power_control_next* on page 3-86
0x34C	t_lpresp_next	RW	0x00000000	32	*3.3.147 t_lpresp_next* on page 3-86
0x350	phy_update_control_next	RW	0x0FE00000	32	*3.3.148 phy_update_control_next* on page 3-87
0x358	odt_timing_next	RW	0x06000600	32	*3.3.149 odt_timing_next* on page 3-87
0x360	odt_wr_control_31_00_next	RW	0x08040201	32	*3.3.150 odt_wr_control_31_00_next* on page 3-87
0x364	odt_wr_control_63_32_next	RW	0x80402010	32	*3.3.151 odt_wr_control_63_32_next* on page 3-87
0x368	odt_rd_control_31_00_next	RW	0x00000000	32	*3.3.152 odt_rd_control_31_00_next* on page 3-88
0x36C	odt_rd_control_63_32_next	RW	0x00000000	32	*3.3.153 odt_rd_control_63_32_next* on page 3-88
0x370	temperature_readout	RO	0x00000000	32	*3.3.154 temperature_readout* on page 3-88
0x378	training_status	RO	0x00000000	32	*3.3.155 training_status* on page 3-89
0x37C	update_status	RO	0x00000000	32	*3.3.156 update_status* on page 3-89
0x380	dq_map_control_15_00_next	RW	0x00000000	32	*3.3.157 dq_map_control_15_00_next* on page 3-89
0x384	dq_map_control_31_16_next	RW	0x00000000	32	*3.3.158 dq_map_control_31_16_next* on page 3-89
0x388	dq_map_control_47_32_next	RW	0x00000000	32	*3.3.159 dq_map_control_47_32_next* on page 3-90
0x38C	dq_map_control_63_48_next	RW	0x00000000	32	*3.3.160 dq_map_control_63_48_next* on page 3-90
0x390	dq_map_control_71_64_next	RW	0x00000000	32	*3.3.161 dq_map_control_71_64_next* on page 3-90
0x398	rank_status	RO	0x00000000	32	*3.3.162 rank_status* on page 3-91
0x39C	mode_change_status	RO	0x00000000	32	*3.3.163 mode_change_status* on page 3-91
0x400	user_status	RO	0x00000000	32	*3.3.164 user_status* on page 3-91
0x408	user_config0_next	RW	0x00000000	32	*3.3.165 user_config0_next* on page 3-92
0x40C	user_config1_next	RW	0x00000000	32	*3.3.166 user_config1_next* on page 3-92
0x410	user_config2	RW	0x00000000	32	*3.3.167 user_config2* on page 3-92
0x414	user_config3	RW	0x00000000	32	*3.3.168 user_config3* on page 3-92
0x500	interrupt_control	RW	0x00000000	32	*3.3.169 interrupt_control* on page 3-93
0x508	interrupt_clr	WO	0x00000000	32	*3.3.170 interrupt_clr* on page 3-93
0x510	interrupt_status	RO	0x00000000	32	*3.3.171 interrupt_status* on page 3-93
0x518	ram_ecc_errc_int_info_31_00	RO	0x00000000	32	*3.3.172 ram_ecc_errc_int_info_31_00* on page 3-94
0x51C	ram_ecc_errc_int_info_63_32	RO	0x00000000	32	*3.3.173 ram_ecc_errc_int_info_63_32* on page 3-94
0x520	ram_ecc_errd_int_info_31_00	RO	0x00000000	32	*3.3.174 ram_ecc_errd_int_info_31_00* on page 3-94
0x524	ram_ecc_errd_int_info_63_32	RO	0x00000000	32	*3.3.175 ram_ecc_errd_int_info_63_32* on page 3-94
0x528	dram_ecc_errc_int_info_31_00	RO	0x00000000	32	*3.3.176 dram_ecc_errc_int_info_31_00* on page 3-95

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x52C	dram_ecc_errc_int_info_63_32	RO	0x00000000	32	*3.3.177 dram_ecc_errc_int_info_63_32* on page 3-95
0x530	dram_ecc_errd_int_info_31_00	RO	0x00000000	32	*3.3.178 dram_ecc_errd_int_info_31_00* on page 3-95
0x534	dram_ecc_errd_int_info_63_32	RO	0x00000000	32	*3.3.179 dram_ecc_errd_int_info_63_32* on page 3-96
0x538	failed_access_int_info_31_00	RO	0x00000000	32	*3.3.180 failed_access_int_info_31_00* on page 3-96
0x53C	failed_access_int_info_63_32	RO	0x00000000	32	*3.3.181 failed_access_int_info_63_32* on page 3-96
0x540	failed_prog_int_info_31_00	RO	0x00000000	32	*3.3.182 failed_prog_int_info_31_00* on page 3-96
0x544	failed_prog_int_info_63_32	RO	0x00000000	32	*3.3.183 failed_prog_int_info_63_32* on page 3-97
0x548	link_err_int_info_31_00	RO	0x00000000	32	*3.3.184 link_err_int_info_31_00* on page 3-97
0x54C	link_err_int_info_63_32	RO	0x00000000	32	*3.3.185 link_err_int_info_63_32* on page 3-97
0x550	arch_fsm_int_info_31_00	RO	0x00000000	32	*3.3.186 arch_fsm_int_info_31_00* on page 3-98
0x554	arch_fsm_int_info_63_32	RO	0x00000000	32	*3.3.187 arch_fsm_int_info_63_32* on page 3-98
0xE00	integ_cfg	RW	0x00000000	32	*3.3.188 integ_cfg* on page 3-98
0xE08	integ_outputs	WO	0x00000000	32	*3.3.189 integ_outputs* on page 3-98
0x1010	address_control_now	RO	0x00030202	32	*3.3.190 address_control_now* on page 3-99
0x1014	decode_control_now	RO	0x00000000	32	*3.3.191 decode_control_now* on page 3-99
0x101C	address_map_now	RO	0x00000000	32	*3.3.192 address_map_now* on page 3-99
0x1020	low_power_control_now	RO	0x00000020	32	*3.3.193 low_power_control_now* on page 3-100
0x1028	turnaround_control_now	RO	0x0F0F0F0F	32	*3.3.194 turnaround_control_now* on page 3-100
0x102C	hit_turnaround_control_now	RO	0x08909FBF	32	*3.3.195 hit_turnaround_control_now* on page 3-100
0x1030	qos_class_control_now	RO	0x00000FC8	32	*3.3.196 qos_class_control_now* on page 3-101
0x1034	escalation_control_now	RO	0x00080F03	32	*3.3.197 escalation_control_now* on page 3-101
0x1038	qv_control_31_00_now	RO	0x76543210	32	*3.3.198 qv_control_31_00_now* on page 3-101
0x103C	qv_control_63_32_now	RO	0xFEDCBA98	32	*3.3.199 qv_control_63_32_now* on page 3-101
0x1040	rt_control_31_00_now	RO	0x00000000	32	*3.3.200 rt_control_31_00_now* on page 3-102
0x1044	rt_control_63_32_now	RO	0x00000000	32	*3.3.201 rt_control_63_32_now* on page 3-102
0x1048	timeout_control_now	RO	0x00000001	32	*3.3.202 timeout_control_now* on page 3-102
0x104C	credit_control_now	RO	0x00000F03	32	*3.3.203 credit_control_now* on page 3-103
0x1050	write_priority_control_31_00_now	RO	0x00000000	32	*3.3.204 write_priority_control_31_00_now* on page 3-103
0x1054	write_priority_control_63_32_now	RO	0x00000000	32	*3.3.205 write_priority_control_63_32_now* on page 3-103
0x1060	queue_threshold_control_31_00_now	RO	0x00000000	32	*3.3.206 queue_threshold_control_31_00_now* on page 3-104

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1064	queue_threshold_control_63_32_now	RO	0x00000000	32	*3.3.207 queue_threshold_control_63_32_now* on page 3-104
0x1078	memory_address_max_31_00_now	RO	0x00000010	32	*3.3.208 memory_address_max_31_00_now* on page 3-104
0x107C	memory_address_max_43_32_now	RO	0x00000000	32	*3.3.209 memory_address_max_43_32_now* on page 3-104
0x1080	access_address_min0_31_00_now	RO	0x00000000	32	*3.3.210 access_address_min0_31_00_now* on page 3-105
0x1084	access_address_min0_43_32_now	RO	0x00000000	32	*3.3.211 access_address_min0_43_32_now* on page 3-105
0x1088	access_address_max0_31_00_now	RO	0x00000000	32	*3.3.212 access_address_max0_31_00_now* on page 3-105
0x108C	access_address_max0_43_32_now	RO	0x00000000	32	*3.3.213 access_address_max0_43_32_now* on page 3-106
0x1090	access_address_min1_31_00_now	RO	0x00000000	32	*3.3.214 access_address_min1_31_00_now* on page 3-106
0x1094	access_address_min1_43_32_now	RO	0x00000000	32	*3.3.215 access_address_min1_43_32_now* on page 3-106
0x1098	access_address_max1_31_00_now	RO	0x00000000	32	*3.3.216 access_address_max1_31_00_now* on page 3-107
0x109C	access_address_max1_43_32_now	RO	0x00000000	32	*3.3.217 access_address_max1_43_32_now* on page 3-107
0x10A0	access_address_min2_31_00_now	RO	0x00000000	32	*3.3.218 access_address_min2_31_00_now* on page 3-107
0x10A4	access_address_min2_43_32_now	RO	0x00000000	32	*3.3.219 access_address_min2_43_32_now* on page 3-107
0x10A8	access_address_max2_31_00_now	RO	0x00000000	32	*3.3.220 access_address_max2_31_00_now* on page 3-108
0x10AC	access_address_max2_43_32_now	RO	0x00000000	32	*3.3.221 access_address_max2_43_32_now* on page 3-108
0x10B0	access_address_min3_31_00_now	RO	0x00000000	32	*3.3.222 access_address_min3_31_00_now* on page 3-108
0x10B4	access_address_min3_43_32_now	RO	0x00000000	32	*3.3.223 access_address_min3_43_32_now* on page 3-109
0x10B8	access_address_max3_31_00_now	RO	0x00000000	32	*3.3.224 access_address_max3_31_00_now* on page 3-109
0x10BC	access_address_max3_43_32_now	RO	0x00000000	32	*3.3.225 access_address_max3_43_32_now* on page 3-109
0x10C0	access_address_min4_31_00_now	RO	0x00000000	32	*3.3.226 access_address_min4_31_00_now* on page 3-110
0x10C4	access_address_min4_43_32_now	RO	0x00000000	32	*3.3.227 access_address_min4_43_32_now* on page 3-110

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x10C8	access_address_max4_31_00_now	RO	0x00000000	32	*3.3.228 access_address_max4_31_00_now* on page 3-110
0x10CC	access_address_max4_43_32_now	RO	0x00000000	32	*3.3.229 access_address_max4_43_32_now* on page 3-110
0x10D0	access_address_min5_31_00_now	RO	0x00000000	32	*3.3.230 access_address_min5_31_00_now* on page 3-111
0x10D4	access_address_min5_43_32_now	RO	0x00000000	32	*3.3.231 access_address_min5_43_32_now* on page 3-111
0x10D8	access_address_max5_31_00_now	RO	0x00000000	32	*3.3.232 access_address_max5_31_00_now* on page 3-111
0x10DC	access_address_max5_43_32_now	RO	0x00000000	32	*3.3.233 access_address_max5_43_32_now* on page 3-112
0x10E0	access_address_min6_31_00_now	RO	0x00000000	32	*3.3.234 access_address_min6_31_00_now* on page 3-112
0x10E4	access_address_min6_43_32_now	RO	0x00000000	32	*3.3.235 access_address_min6_43_32_now* on page 3-112
0x10E8	access_address_max6_31_00_now	RO	0x00000000	32	*3.3.236 access_address_max6_31_00_now* on page 3-113
0x10EC	access_address_max6_43_32_now	RO	0x00000000	32	*3.3.237 access_address_max6_43_32_now* on page 3-113
0x10F0	access_address_min7_31_00_now	RO	0x00000000	32	*3.3.238 access_address_min7_31_00_now* on page 3-113
0x10F4	access_address_min7_43_32_now	RO	0x00000000	32	*3.3.239 access_address_min7_43_32_now* on page 3-113
0x10F8	access_address_max7_31_00_now	RO	0x00000000	32	*3.3.240 access_address_max7_31_00_now* on page 3-114
0x10FC	access_address_max7_43_32_now	RO	0x00000000	32	*3.3.241 access_address_max7_43_32_now* on page 3-114
0x1110	dci_replay_type_now	RO	0x00000002	32	*3.3.242 dci_replay_type_now* on page 3-114
0x1120	refresh_control_now	RO	0x00000000	32	*3.3.243 refresh_control_now* on page 3-115
0x1128	memory_type_now	RO	0x00000101	32	*3.3.244 memory_type_now* on page 3-115
0x1170	scrub_control0_now	RO	0x1F000000	32	*3.3.245 scrub_control0_now* on page 3-115
0x1174	scrub_address_min0_now	RO	0x00000000	32	*3.3.246 scrub_address_min0_now* on page 3-116
0x1178	scrub_address_max0_now	RO	0x00000000	32	*3.3.247 scrub_address_max0_now* on page 3-116
0x1180	scrub_control1_now	RO	0x1F000000	32	*3.3.248 scrub_control1_now* on page 3-116
0x1184	scrub_address_min1_now	RO	0x00000000	32	*3.3.249 scrub_address_min1_now* on page 3-116
0x1188	scrub_address_max1_now	RO	0x00000000	32	*3.3.250 scrub_address_max1_now* on page 3-117
0x1190	scrub_control2_now	RO	0x1F000000	32	*3.3.251 scrub_control2_now* on page 3-117
0x1194	scrub_address_min2_now	RO	0x00000000	32	*3.3.252 scrub_address_min2_now* on page 3-117

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1198	scrub_address_max2_now	RO	0x00000000	32	*3.3.253 scrub_address_max2_now* on page 3-118
0x11A0	scrub_control3_now	RO	0x1F000000	32	*3.3.254 scrub_control3_now* on page 3-118
0x11A4	scrub_address_min3_now	RO	0x00000000	32	*3.3.255 scrub_address_min3_now* on page 3-118
0x11A8	scrub_address_max3_now	RO	0x00000000	32	*3.3.256 scrub_address_max3_now* on page 3-119
0x11B0	scrub_control4_now	RO	0x1F000000	32	*3.3.257 scrub_control4_now* on page 3-119
0x11B4	scrub_address_min4_now	RO	0x00000000	32	*3.3.258 scrub_address_min4_now* on page 3-119
0x11B8	scrub_address_max4_now	RO	0x00000000	32	*3.3.259 scrub_address_max4_now* on page 3-119
0x11C0	scrub_control5_now	RO	0x1F000000	32	*3.3.260 scrub_control5_now* on page 3-120
0x11C4	scrub_address_min5_now	RO	0x00000000	32	*3.3.261 scrub_address_min5_now* on page 3-120
0x11C8	scrub_address_max5_now	RO	0x00000000	32	*3.3.262 scrub_address_max5_now* on page 3-120
0x11D0	scrub_control6_now	RO	0x1F000000	32	*3.3.263 scrub_control6_now* on page 3-121
0x11D4	scrub_address_min6_now	RO	0x00000000	32	*3.3.264 scrub_address_min6_now* on page 3-121
0x11D8	scrub_address_max6_now	RO	0x00000000	32	*3.3.265 scrub_address_max6_now* on page 3-121
0x11E0	scrub_control7_now	RO	0x1F000000	32	*3.3.266 scrub_control7_now* on page 3-122
0x11E4	scrub_address_min7_now	RO	0x00000000	32	*3.3.267 scrub_address_min7_now* on page 3-122
0x11E8	scrub_address_max7_now	RO	0x00000000	32	*3.3.268 scrub_address_max7_now* on page 3-122
0x11F0	feature_control_now	RO	0x0AA00000	32	*3.3.269 feature_control_now* on page 3-122
0x11F4	mux_control_now	RO	0x00000000	32	*3.3.270 mux_control_now* on page 3-123
0x11F8	rank_remap_control_now	RO	0x76543210	32	*3.3.271 rank_remap_control_now* on page 3-123
0x11FC	scrub_control_now	RO	0x00001F00	32	*3.3.272 scrub_control_now* on page 3-123
0x1200	t_refi_now	RO	0x00090100	32	*3.3.273 t_refi_now* on page 3-124
0x1204	t_rfc_now	RO	0x00008C23	32	*3.3.274 t_rfc_now* on page 3-124
0x1208	t_mrr_now	RO	0x00000002	32	*3.3.275 t_mrr_now* on page 3-124
0x120C	t_mrw_now	RO	0x0000000C	32	*3.3.276 t_mrw_now* on page 3-125
0x1210	t_rdpden_now	RO	0x0000000A	32	*3.3.277 t_rdpden_now* on page 3-125
0x1218	t_rcd_now	RO	0x00000005	32	*3.3.278 t_rcd_now* on page 3-125
0x121C	t_ras_now	RO	0x0000000E	32	*3.3.279 t_ras_now* on page 3-126
0x1220	t_rp_now	RO	0x00000005	32	*3.3.280 t_rp_now* on page 3-126
0x1224	t_rpall_now	RO	0x00000005	32	*3.3.281 t_rpall_now* on page 3-126
0x1228	t_rrd_now	RO	0x00000404	32	*3.3.282 t_rrd_now* on page 3-127
0x122C	t_act_window_now	RO	0x03560014	32	*3.3.283 t_act_window_now* on page 3-127
0x1234	t_rtr_now	RO	0x00060404	32	*3.3.284 t_rtr_now* on page 3-127
0x1238	t_rtw_now	RO	0x00060606	32	*3.3.285 t_rtw_now* on page 3-128
0x123C	t_rtp_now	RO	0x00000004	32	*3.3.286 t_rtp_now* on page 3-128
0x1244	t_wr_now	RO	0x00000005	32	*3.3.287 t_wr_now* on page 3-128

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1248	t_wtr_now	RO	0x00040505	32	*3.3.288 t_wtr_now* on page 3-129
0x124C	t_wtw_now	RO	0x00060404	32	*3.3.289 t_wtw_now* on page 3-129
0x1254	t_xmpd_now	RO	0x000003FF	32	*3.3.290 t_xmpd_now* on page 3-129
0x1258	t_ep_now	RO	0x00000002	32	*3.3.291 t_ep_now* on page 3-130
0x125C	t_xp_now	RO	0x00060002	32	*3.3.292 t_xp_now* on page 3-130
0x1260	t_esr_now	RO	0x0000000E	32	*3.3.293 t_esr_now* on page 3-130
0x1264	t_xsr_now	RO	0x05120100	32	*3.3.294 t_xsr_now* on page 3-131
0x1268	t_esrck_now	RO	0x00000005	32	*3.3.295 t_esrck_now* on page 3-131
0x126C	t_ckxsr_now	RO	0x00000001	32	*3.3.296 t_ckxsr_now* on page 3-131
0x1270	t_cmd_now	RO	0x00000000	32	*3.3.297 t_cmd_now* on page 3-131
0x1274	t_parity_now	RO	0x00000900	32	*3.3.298 t_parity_now* on page 3-132
0x1278	t_zqcs_now	RO	0x00000040	32	*3.3.299 t_zqcs_now* on page 3-132
0x1300	t_rddata_en_now	RO	0x00000001	32	*3.3.300 t_rddata_en_now* on page 3-132
0x1304	t_phyrdlat_now	RO	0x00000000	32	*3.3.301 t_phyrdlat_now* on page 3-133
0x1308	t_phywrlat_now	RO	0x00000001	32	*3.3.302 t_phywrlat_now* on page 3-133
0x1310	rdlvl_control_now	RO	0x00001080	32	*3.3.303 rdlvl_control_now* on page 3-133
0x1314	rdlvl_mrs_now	RO	0x00000004	32	*3.3.304 rdlvl_mrs_now* on page 3-134
0x1318	t_rdlvl_en_now	RO	0x00000000	32	*3.3.305 t_rdlvl_en_now* on page 3-134
0x131C	t_rdlvl_rr_now	RO	0x00000000	32	*3.3.306 t_rdlvl_rr_now* on page 3-134
0x1320	wrlvl_control_now	RO	0x00001000	32	*3.3.307 wrlvl_control_now* on page 3-135
0x1324	wrlvl_mrs_now	RO	0x00000086	32	*3.3.308 wrlvl_mrs_now* on page 3-135
0x1328	t_wrlvl_en_now	RO	0x00000000	32	*3.3.309 t_wrlvl_en_now* on page 3-135
0x132C	t_wrlvl_ww_now	RO	0x00000000	32	*3.3.310 t_wrlvl_ww_now* on page 3-136
0x1348	phy_power_control_now	RO	0x00000000	32	*3.3.311 phy_power_control_now* on page 3-136
0x134C	t_lpresp_now	RO	0x00000000	32	*3.3.312 t_lpresp_now* on page 3-136
0x1350	phy_update_control_now	RO	0x0FE00000	32	*3.3.313 phy_update_control_now* on page 3-137
0x1358	odt_timing_now	RO	0x06000600	32	*3.3.314 odt_timing_now* on page 3-137
0x1360	odt_wr_control_31_00_now	RO	0x08040201	32	*3.3.315 odt_wr_control_31_00_now* on page 3-137
0x1364	odt_wr_control_63_32_now	RO	0x80402010	32	*3.3.316 odt_wr_control_63_32_now* on page 3-138
0x1368	odt_rd_control_31_00_now	RO	0x00000000	32	*3.3.317 odt_rd_control_31_00_now* on page 3-138
0x136C	odt_rd_control_63_32_now	RO	0x00000000	32	*3.3.318 odt_rd_control_63_32_now* on page 3-138
0x1380	dq_map_control_15_00_now	RO	0x00000000	32	*3.3.319 dq_map_control_15_00_now* on page 3-138
0x1384	dq_map_control_31_16_now	RO	0x00000000	32	*3.3.320 dq_map_control_31_16_now* on page 3-139
0x1388	dq_map_control_47_32_now	RO	0x00000000	32	*3.3.321 dq_map_control_47_32_now* on page 3-139
0x138C	dq_map_control_63_48_now	RO	0x00000000	32	*3.3.322 dq_map_control_63_48_now* on page 3-140

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1390	dq_map_control_71_64_now	RO	0x00000000	32	*3.3.323 dq_map_control_71_64_now* on page 3-140
0x1408	user_config0_now	RO	0x00000000	32	*3.3.324 user_config0_now* on page 3-140
0x140C	user_config1_now	RO	0x00000000	32	*3.3.325 user_config1_now* on page 3-141
0x1FD0	periph_id_4	RO	0x00000014	32	*3.3.326 periph_id_4* on page 3-141
0x1FE0	periph_id_0	RO	0x00000052	32	*3.3.327 periph_id_0* on page 3-141
0x1FE4	periph_id_1	RO	0x000000B4	32	*3.3.328 periph_id_1* on page 3-141
0x1FE8	periph_id_2	RO	0x0000003B	32	*3.3.329 periph_id_2* on page 3-142
0x1FEC	periph_id_3	RO	0x00000000	32	*3.3.330 periph_id_3* on page 3-142
0x1FF0	component_id_0	RO	0x0000000D	32	*3.3.331 component_id_0* on page 3-142
0x1FF4	component_id_1	RO	0x000000F0	32	*3.3.332 component_id_1* on page 3-143
0x1FF8	component_id_2	RO	0x00000005	32	*3.3.333 component_id_2* on page 3-143
0x1FFC	component_id_3	RO	0x000000B1	32	*3.3.334 component_id_3* on page 3-143

3.3 Register descriptions

This section describes the dmc520 registers.

3.2 Register summary on page 3-32 provides cross references to individual registers.

3.3.1 memc_status

Holds the architectural status of the DMC.

The memc_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x000`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.2 memc_config

Holds the configuration data for the DMC.

The memc_config register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x004`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.3 memc_cmd

Used to change the architectural state of the DMC, or execute queued manager operations.

The memc_cmd register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x008`
Type	Write-only
Reset	`0x00000000`
Width	32

3.3.4 address_control_next

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values.

The address_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x010`

Type Read-write

Reset `0x00030202`

Width 32

3.3.5 decode_control_next

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, bank, row address, and the column address.

The decode_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x014`

Type Read-write

Reset `0x00000000`

Width 32

3.3.6 format_control

Configures the memory burst access parameters.

The format_control register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x018`

Type Read-write

Reset `0x22000213`

Width 32

3.3.7 address_map_next

Configures the system address mapping options.

The address_map_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x01C
Type Read-write
Reset 0x00000000
Width 32

3.3.8 low_power_control_next

Configures the low-power features of the DMC.

The low_power_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x020
Type Read-write
Reset 0x00000020
Width 32

3.3.9 turnaround_control_next

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus.

The turnaround_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x028
Type Read-write
Reset 0x0F0F0F0F
Width 32

3.3.10 hit_turnaround_control_next

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams.

The hit_turnaround_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x02C
Type Read-write
Reset 0x08909FBF

Width 32

3.3.11 qos_class_control_next

Configures the priority class for each QoS encoding.

The qos_class_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x030`

Type Read-write

Reset `0x00000FC8`

Width 32

3.3.12 escalation_control_next

Configures the settings for escalating the priority of entries in the queue.

The escalation_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x034`

Type Read-write

Reset `0x00080F03`

Width 32

3.3.13 qv_control_31_00_next

Configures the priority settings for each QoS encoding.

The qv_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x038`

Type Read-write

Reset `0x76543210`

Width 32

3.3.14 qv_control_63_32_next

Configures the priority settings for each QoS encoding.

The qv_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x03C
Type	Read-write
Reset	0xFEDCBA98
Width	32

3.3.15 rt_control_31_00_next

Configures the timeout settings for each QoS encoding.

The rt_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x040
Type	Read-write
Reset	0x00000000
Width	32

3.3.16 rt_control_63_32_next

Configures the timeout settings for each QoS encoding.

The rt_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x044
Type	Read-write
Reset	0x00000000
Width	32

3.3.17 timeout_control_next

Configures the prescaler applied to timeout values.

The timeout_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x048
Type	Read-write
Reset	0x00000001
Width	32

3.3.18 credit_control_next

Configures the settings for preventing starvation of CHI protocol retries.

The credit_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x04C`
Type	Read-write
Reset	`0x00000F03`
Width	32

3.3.19 write_priority_control_31_00_next

Configures the priority settings for write requests within the DMC

The write_priority_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x050`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.20 write_priority_control_63_32_next

Configures the priority settings for write requests within the DMC.

The write_priority_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x054`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.21 queue_threshold_control_31_00_next

Configures the threshold settings for requests in the DMC

The queue_threshold_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x060
Type Read-write
Reset 0x00000000
Width 32

3.3.22 queue_threshold_control_63_32_next

Configures the threshold settings for requests in the DMC

The queue_threshold_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x064
Type Read-write
Reset 0x00000000
Width 32

3.3.23 memory_address_max_31_00_next

Configures the address space control for the DMC default region.

The memory_address_max_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x078
Type Read-write
Reset 0x00000010
Width 32

3.3.24 memory_address_max_43_32_next

Configures the address space control for the DMC default region.

The memory_address_max_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x07C
Type Read-write
Reset 0x00000000
Width 32

3.3.25 access_address_min0_31_00_next

Configures the address space control for address region 0.

The access_address_min0_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x080`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.26 access_address_min0_43_32_next

Configures the address space control for address region 0.

The access_address_min0_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x084`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.27 access_address_max0_31_00_next

Configures the address space control for address region 0.

The access_address_max0_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x088`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.28 access_address_max0_43_32_next

Configures the address space control for address region 0.

The access_address_max0_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x08C
Type Read-write
Reset 0x00000000
Width 32

3.3.29 access_address_min1_31_00_next

Configures the address space control for address region 1.

The access_address_min1_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x090
Type Read-write
Reset 0x00000000
Width 32

3.3.30 access_address_min1_43_32_next

Configures the address space control for address region 1.

The access_address_min1_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x094
Type Read-write
Reset 0x00000000
Width 32

3.3.31 access_address_max1_31_00_next

Configures the address space control for address region 1.

The access_address_max1_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x098
Type Read-write
Reset 0x00000000
Width 32

3.3.32 access_address_max1_43_32_next

Configures the address space control for address region 1.

The access_address_max1_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x09C`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.33 access_address_min2_31_00_next

Configures the address space control for address region 2.

The access_address_min2_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0A0`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.34 access_address_min2_43_32_next

Configures the address space control for address region 2.

The access_address_min2_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0A4`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.35 access_address_max2_31_00_next

Configures the address space control for address region 2.

The access_address_max2_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x0A8

Type Read-write

Reset 0x00000000

Width 32

3.3.36 access_address_max2_43_32_next

Configures the address space control for address region 2.

The access_address_max2_43_32_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0AC

Type Read-write

Reset 0x00000000

Width 32

3.3.37 access_address_min3_31_00_next

Configures the address space control for address region 3.

The access_address_min3_31_00_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0B0

Type Read-write

Reset 0x00000000

Width 32

3.3.38 access_address_min3_43_32_next

Configures the address space control for address region 3.

The access_address_min3_43_32_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0B4

Type Read-write

Reset 0x00000000

Width 32

3.3.39 access_address_max3_31_00_next

Configures the address space control for address region 3.

The access_address_max3_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0B8`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.40 access_address_max3_43_32_next

Configures the address space control for address region 3.

The access_address_max3_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0BC`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.41 access_address_min4_31_00_next

Configures the address space control for address region 4.

The access_address_min4_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0C0`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.42 access_address_min4_43_32_next

Configures the address space control for address region 4.

The access_address_min4_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x0C4

Type Read-write

Reset 0x00000000

Width 32

3.3.43 access_address_max4_31_00_next

Configures the address space control for address region 4.

The access_address_max4_31_00_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0C8

Type Read-write

Reset 0x00000000

Width 32

3.3.44 access_address_max4_43_32_next

Configures the address space control for address region 4.

The access_address_max4_43_32_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0CC

Type Read-write

Reset 0x00000000

Width 32

3.3.45 access_address_min5_31_00_next

Configures the address space control for address region 5.

The access_address_min5_31_00_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x0D0

Type Read-write

Reset 0x00000000

Width 32

3.3.46 access_address_min5_43_32_next

Configures the address space control for address region 5.

The access_address_min5_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0D4`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.47 access_address_max5_31_00_next

Configures the address space control for address region 5.

The access_address_max5_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0D8`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.48 access_address_max5_43_32_next

Configures the address space control for address region 5.

The access_address_max5_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0DC`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.49 access_address_min6_31_00_next

Configures the address space control for address region 6.

The access_address_min6_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x0E0
Type Read-write
Reset 0x00000000
Width 32

3.3.50 access_address_min6_43_32_next

Configures the address space control for address region 6.

The access_address_min6_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x0E4
Type Read-write
Reset 0x00000000
Width 32

3.3.51 access_address_max6_31_00_next

Configures the address space control for address region 6.

The access_address_max6_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x0E8
Type Read-write
Reset 0x00000000
Width 32

3.3.52 access_address_max6_43_32_next

Configures the address space control for address region 6.

The access_address_max6_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x0EC
Type Read-write
Reset 0x00000000
Width 32

3.3.53 access_address_min7_31_00_next

Configures the address space control for address region 7.

The access_address_min7_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0F0`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.54 access_address_min7_43_32_next

Configures the address space control for address region 7.

The access_address_min7_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0F4`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.55 access_address_max7_31_00_next

Configures the address space control for address region 7.

The access_address_max7_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0F8`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.56 access_address_max7_43_32_next

Configures the address space control for the address region 7.

The access_address_max7_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x0FC
Type Read-write
Reset 0x00000000
Width 32

3.3.57 channel_status

Holds the current status of the memory channel.

The channel_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x100
Type Read-only
Reset 0x00000003
Width 32

3.3.58 direct_addr

Sets the direct command address field for direct commands.

The direct_addr register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x108
Type Read-write
Reset 0x00000000
Width 32

3.3.59 direct_cmd

Generates direct commands from the manager.

The direct_cmd register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10C
Type Write-only
Reset 0x00000000
Width 32

3.3.60 dci_replay_type_next

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command.

The dci_replay_type_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x110`
Type	Read-write
Reset	`0x00000002`
Width	32

3.3.61 dci_strb

Configures the write data strobe values used during direct_cmd WRITE operations.

The dci_strb register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x118`
Type	Read-write
Reset	`0x0000000F`
Width	32

3.3.62 dci_data

Reading from this register location returns read data received a result of a READ command. Writing to this register location sets the data to be used for direct_cmd WRITE commands. You must read or write once for each 32-bit data word of a DRAM burst.

The dci_data register characteristics are:

Usage constraints
Can be read from when in CONFIG, PAUSED or READY states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11C`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.63 refresh_control_next

Configures the type of refresh commands issued by the DMC.

The refresh_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x120`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.64 memory_type_next

Configures the DMC for the attached memory type.

The memory_type_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x128`
Type	Read-write
Reset	`0x00000101`
Width	32

3.3.65 feature_config

Control register for DMC features.

The feature_config register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x130`
Type	Read-write
Reset	`0x000000F0`
Width	32

3.3.66 nibble_failed_031_000

Used to inform the DMC that a particular nibble has failed.

The nibble_failed_031_000 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x138`
Type	Read-write

Reset 0x00000000
Width 32

3.3.67 nibble_failed_063_032

Used to inform the DMC that a particular nibble has failed.

The nibble_failed_063_032 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x13C
Type Read-write
Reset 0x00000000
Width 32

3.3.68 nibble_failed_095_064

Used to inform the DMC that a particular nibble has failed.

The nibble_failed_095_064 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x140
Type Read-write
Reset 0x00000000
Width 32

3.3.69 nibble_failed_127_096

Used to inform the DMC that a particular nibble has failed.

The nibble_failed_127_096 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x144
Type Read-write
Reset 0x00000000
Width 32

3.3.70 queue_allocate_control_031_000

Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation.

The queue_allocate_control_031_000 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x148`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

3.3.71 queue_allocate_control_063_032

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_063_032 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x14C`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

3.3.72 queue_allocate_control_095_064

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_095_064 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x150`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

3.3.73 queue_allocate_control_127_096

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_127_096 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x154
Type	Read-write
Reset	0xFFFFFFFF
Width	32

3.3.74 ecc_errc_count_31_00

Counter register for the DRAM ECC functionality.

The ecc_errc_count_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x158
Type	Read-write
Reset	0x00000000
Width	32

3.3.75 ecc_errc_count_63_32

Counter register for the DRAM ECC functionality.

The ecc_errc_count_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x15C
Type	Read-write
Reset	0x00000000
Width	32

3.3.76 ecc_errd_count_31_00

Counter register for the DRAM ECC functionality.

The ecc_errd_count_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x160
Type	Read-write
Reset	0x00000000
Width	32

3.3.77 ecc_errd_count_63_32

Counter register for the DRAM ECC functionality.

The ecc_errd_count_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x164`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.78 ram_err_count

Counter register for the RAM ECC functionality.

The ram_err_count register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x168`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.79 link_err_count

Counter register for link errors. The counter increments on detection of a new link error (dfi_alert_n or dfi_err).

The link_err_count register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x16C`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.80 scrub_control0_next

Scrub engine channel control register.

The scrub_control0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x170`
Type	Read-write
Reset	`0x1F000000`
Width	32

3.3.81 scrub_address_min0_next

Configures the address space control for the scrub engine channel.

The scrub_address_min0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x174`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.82 scrub_address_max0_next

Configures the address space control for the scrub engine channel.

The scrub_address_max0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x178`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.83 scrub_control1_next

Scrub engine channel control register.

The scrub_control1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x180`
Type	Read-write
Reset	`0x1F000000`
Width	32

3.3.84 scrub_address_min1_next

Configures the address space control for the scrub engine channel.

The scrub_address_min1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x184`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.85 scrub_address_max1_next

Configures the address space control for the scrub engine channel.

The scrub_address_max1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x188`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.86 scrub_control2_next

Scrub engine channel control register.

The scrub_control2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x190`
Type	Read-write
Reset	`0x1F000000`
Width	32

3.3.87 scrub_address_min2_next

Configures the address space control for the scrub engine channel.

The scrub_address_min2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x194
Type Read-write
Reset 0x00000000
Width 32

3.3.88 scrub_address_max2_next

Configures the address space control for the scrub engine channel.

The scrub_address_max2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x198
Type Read-write
Reset 0x00000000
Width 32

3.3.89 scrub_control3_next

Scrub engine channel control register.

The scrub_control3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1A0
Type Read-write
Reset 0x1F000000
Width 32

3.3.90 scrub_address_min3_next

Configures the address space control for the scrub engine channel.

The scrub_address_min3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1A4
Type Read-write
Reset 0x00000000
Width 32

3.3.91 scrub_address_max3_next

Configures the address space control for the scrub engine channel.

The scrub_address_max3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1A8`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.92 scrub_control4_next

Scrub engine channel control register.

The scrub_control4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1B0`
Type	Read-write
Reset	`0x1F000000`
Width	32

3.3.93 scrub_address_min4_next

Configures the address space control for the scrub engine channel.

The scrub_address_min4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1B4`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.94 scrub_address_max4_next

Configures the address space control for the scrub engine channel.

The scrub_address_max4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1B8
Type Read-write
Reset 0x00000000
Width 32

3.3.95 scrub_control5_next

Scrub engine channel control register.

The scrub_control5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1C0
Type Read-write
Reset 0x1F000000
Width 32

3.3.96 scrub_address_min5_next

Configures the address space control for the scrub engine channel.

The scrub_address_min5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1C4
Type Read-write
Reset 0x00000000
Width 32

3.3.97 scrub_address_max5_next

Configures the address space control for the scrub engine channel.

The scrub_address_max5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1C8
Type Read-write
Reset 0x00000000
Width 32

3.3.98 scrub_control6_next

Scrub engine channel control register.

The scrub_control6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1D0`

Type Read-write

Reset `0x1F000000`

Width 32

3.3.99 scrub_address_min6_next

Configures the address space control for the scrub engine channel.

The scrub_address_min6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1D4`

Type Read-write

Reset `0x00000000`

Width 32

3.3.100 scrub_address_max6_next

Configures the address space control for the scrub engine channel.

The scrub_address_max6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1D8`

Type Read-write

Reset `0x00000000`

Width 32

3.3.101 scrub_control7_next

Scrub engine channel control register.

The scrub_control7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1E0
Type Read-write
Reset 0x1F000000
Width 32

3.3.102 scrub_address_min7_next

Configures the address space control for the scrub engine channel.

The scrub_address_min7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1E4
Type Read-write
Reset 0x00000000
Width 32

3.3.103 scrub_address_max7_next

Configures the address space control for the scrub engine channel.

The scrub_address_max7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1E8
Type Read-write
Reset 0x00000000
Width 32

3.3.104 feature_control_next

Control register for DMC features.

The feature_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1F0
Type Read-write
Reset 0x0AA00000
Width 32

3.3.105 mux_control_next

Control muxing options for the DMC.

The mux_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1F4`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.106 rank_remap_control_next

Control register for rank remap.

The rank_remap_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1F8`
Type	Read-write
Reset	`0x76543210`
Width	32

3.3.107 scrub_control_next

Scrub engine channel control register.

The scrub_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FC`
Type	Read-write
Reset	`0x00001F00`
Width	32

3.3.108 t_refi_next

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8.

The t_refi_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.
Attributes

Offset	0x200
Type	Read-write
Reset	0x00090100
Width	32

3.3.109 t_rfc_next

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank.

The t_rfc_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x204
Type	Read-write
Reset	0x00008C23
Width	32

3.3.110 t_mrr_next

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank.

The t_mrr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x208
Type	Read-write
Reset	0x00000002
Width	32

3.3.111 t_mrw_next

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank.

The t_mrw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x20C

Type Read-write
Reset 0x0000000C
Width 32

3.3.112 t_rdpden_next

Configures the tRDPDEN timing parameter. This determines the delay applied after a Read command before a power down command can be issued to the same rank.

The t_rdpden_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x210
Type Read-write
Reset 0x0000000A
Width 32

3.3.113 t_rcd_next

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank.

The t_rcd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x218
Type Read-write
Reset 0x00000005
Width 32

3.3.114 t_ras_next

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank.

The t_ras_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x21C
Type Read-write
Reset 0x0000000E
Width 32

3.3.115 t_rp_next

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank.

The t_rp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x220`
Type	Read-write
Reset	`0x00000005`
Width	32

3.3.116 t_rpall_next

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank.

The t_rpall_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x224`
Type	Read-write
Reset	`0x00000005`
Width	32

3.3.117 t_rrd_next

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, and a different bank group, respectively, as described in the DDR4 specification.

The t_rrd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x228`
Type	Read-write
Reset	`0x00000404`
Width	32

3.3.118 t_act_window_next

Configures the tFAW and tMAWi timing parameters.

The t_act_window_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x22C`
Type	Read-write
Reset	`0x03560014`
Width	32

3.3.119 t_rtr_next

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), and different chip-selects (t_rtr_cs).

The t_rtr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x234`
Type	Read-write
Reset	`0x00060404`
Width	32

3.3.120 t_rtw_next

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs).

The t_rtw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x238`
Type	Read-write
Reset	`0x00060606`
Width	32

3.3.121 t_rtp_next

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank.

The t_rtp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x23C
Type Read-write
Reset 0x00000004
Width 32

3.3.122 t_wr_next

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank.

The t_wr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x244
Type Read-write
Reset 0x00000005
Width 32

3.3.123 t_wtr_next

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs).

The t_wtr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x248
Type Read-write
Reset 0x00040505
Width 32

3.3.124 t_wtw_next

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes.

The t_wtw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x24C
Type Read-write
Reset 0x00060404

Width 32

3.3.125 t_xmpd_next

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank.

The t_xmpd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x254`

Type Read-write

Reset `0x000003FF`

Width 32

3.3.126 t_ep_next

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank.

The t_ep_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x258`

Type Read-write

Reset `0x00000002`

Width 32

3.3.127 t_xp_next

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL).

The t_xp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x25C`

Type Read-write

Reset `0x00060002`

Width 32

3.3.128 t_esr_next

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank.

The t_esr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x260`
Type	Read-write
Reset	`0x0000000E`
Width	32

3.3.129 t_xsr_next

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank.

The t_xsr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x264`
Type	Read-write
Reset	`0x05120100`
Width	32

3.3.130 t_esrck_next

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state.

The t_esrck_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x268`
Type	Read-write
Reset	`0x00000005`
Width	32

3.3.131 t_ckxsr_next

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state.

The t_ckxsr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x26C
Type	Read-write
Reset	0x00000001
Width	32

3.3.132 t_cmd_next

Configures command signaling timing.

The t_cmd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x270
Type	Read-write
Reset	0x00000000
Width	32

3.3.133 t_parity_next

Parity latencies t_parinlat and t_completion.

The t_parity_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x274
Type	Read-write
Reset	0x00000900
Width	32

3.3.134 t_zqcs_next

Configures the delay to apply following a ZQC-Short calibration command.

The t_zqcs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x278
Type	Read-write
Reset	0x00000040
Width	32

3.3.135 t_rddata_en_next

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal.

The t_rddata_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x300`
Type	Read-write
Reset	`0x00000001`
Width	32

3.3.136 t_phyrdlat_next

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY.

The t_phyrdlat_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x304`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.137 t_phywrlat_next

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en, dfi_wrdata_cs and dfi_wrdata signals.

The t_phywrlat_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x308`
Type	Read-write
Reset	`0x00000001`
Width	32

3.3.138 rdlvl_control_next

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training.

The rdlvl_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x310`
Type	Read-write
Reset	`0x00001080`
Width	32

3.3.139 rdlvl_mrs_next

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration Manual for more information on PHY training.

The rdlvl_mrs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x314`
Type	Read-write
Reset	`0x00000004`
Width	32

3.3.140 t_rdlvl_en_next

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training.

The t_rdlvl_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x318`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.141 t_rdlvl_rr_next

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp.

The t_rdlvl_rr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x31C
Type	Read-write
Reset	0x00000000
Width	32

3.3.142 wrlvl_control_next

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training.

The wrlvl_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x320
Type	Read-write
Reset	0x00001000
Width	32

3.3.143 wrlvl_mrs_next

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information.

The wrlvl_mrs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x324
Type	Read-write
Reset	0x00000086
Width	32

3.3.144 t_wrlvl_en_next

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training.

The t_wrlvl_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x328
Type Read-write
Reset 0x00000000
Width 32

3.3.145 t_wrlvl_ww_next

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp.

The t_wrlvl_ww_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x32C
Type Read-write
Reset 0x00000000
Width 32

3.3.146 phy_power_control_next

Configures the low-power requests made to the PHY for the different channel states.

The phy_power_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x348
Type Read-write
Reset 0x00000000
Width 32

3.3.147 t_lpresp_next

Configures the minimum cycle delay to apply for PHY low-power handshakes.

The t_lpresp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x34C
Type Read-write
Reset 0x00000000
Width 32

3.3.148 phy_update_control_next

Configures the update mechanism to use in response to PHY training requests.

The phy_update_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x350`
Type	Read-write
Reset	`0x0FE00000`
Width	32

3.3.149 odt_timing_next

Configures the ODT on and off timing.

The odt_timing_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x358`
Type	Read-write
Reset	`0x06000600`
Width	32

3.3.150 odt_wr_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x360`
Type	Read-write
Reset	`0x08040201`
Width	32

3.3.151 odt_wr_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x364
Type Read-write
Reset 0x80402010
Width 32

3.3.152 odt_rd_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x368
Type Read-write
Reset 0x00000000
Width 32

3.3.153 odt_rd_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x36C
Type Read-write
Reset 0x00000000
Width 32

3.3.154 temperature_readout

Holds the status of the temperature information. Reading the register returns the current temperature from the most recent automated temperature poll.

The temperature_readout register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x370
Type Read-only
Reset 0x00000000
Width 32

3.3.155 training_status

Shows information relating to the training request status of the DMC.

The training_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x378`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.156 update_status

Shows information relating to the update request status of the DMC.

The update_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x37C`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.157 dq_map_control_15_00_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_15_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x380`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.158 dq_map_control_31_16_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_31_16_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x384

Type Read-write

Reset 0x00000000

Width 32

3.3.159 dq_map_control_47_32_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_47_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x388

Type Read-write

Reset 0x00000000

Width 32

3.3.160 dq_map_control_63_48_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_63_48_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x38C

Type Read-write

Reset 0x00000000

Width 32

3.3.161 dq_map_control_71_64_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation.

The dq_map_control_71_64_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x390`

Type Read-write

Reset `0x00000000`

Width 32

3.3.162 rank_status

Shows the current status of geardown, MPD and CAL.

The rank_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x398`

Type Read-only

Reset `0x00000000`

Width 32

3.3.163 mode_change_status

Shows the current status of the sequence that is currently being processed.

The mode_change_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x39C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.164 user_status

Shows the value of the input user_status signals.

The user_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x400`

Type Read-only
Reset 0x00000000
Width 32

3.3.165 user_config0_next

Drives the output user_config0 signal.

The user_config0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x408
Type Read-write
Reset 0x00000000
Width 32

3.3.166 user_config1_next

Drives the output user_config1 signal.

The user_config1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x40C
Type Read-write
Reset 0x00000000
Width 32

3.3.167 user_config2

Drives the output user_config2 signal.

The user_config2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x410
Type Read-write
Reset 0x00000000
Width 32

3.3.168 user_config3

Drives the output user_config3 signal.

The user_config3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x414`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.169 interrupt_control

Configures interrupt behavior.

The interrupt_control register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x500`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.170 interrupt_clr

Clear register for interrupts.

The interrupt_clr register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x508`
Type	Write-only
Reset	`0x00000000`
Width	32

3.3.171 interrupt_status

Status register for interrupts (pre-mask).

The interrupt_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x510`
Type	Read-only
Reset	`0x00000000`

Width 32

3.3.172 ram_ecc_errc_int_info_31_00

Shows information relating to the interrupt

The ram_ecc_errc_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x518`

Type Read-only

Reset `0x00000000`

Width 32

3.3.173 ram_ecc_errc_int_info_63_32

Shows information relating to the interrupt

The ram_ecc_errc_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x51C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.174 ram_ecc_errd_int_info_31_00

Shows information relating to the interrupt

The ram_ecc_errd_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x520`

Type Read-only

Reset `0x00000000`

Width 32

3.3.175 ram_ecc_errd_int_info_63_32

Shows information relating to the interrupt

The ram_ecc_errd_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.
Attributes

Offset	0x524
Type	Read-only
Reset	0x00000000
Width	32

3.3.176 dram_ecc_errc_int_info_31_00

Shows information relating to the interrupt

The dram_ecc_errc_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x528
Type	Read-only
Reset	0x00000000
Width	32

3.3.177 dram_ecc_errc_int_info_63_32

Shows information relating to the interrupt

The dram_ecc_errc_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x52C
Type	Read-only
Reset	0x00000000
Width	32

3.3.178 dram_ecc_errd_int_info_31_00

Shows information relating to the interrupt

The dram_ecc_errd_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x530
Type	Read-only
Reset	0x00000000
Width	32

3.3.179 dram_ecc_errd_int_info_63_32

Shows information relating to the interrupt

The dram_ecc_errd_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x534`

Type Read-only

Reset `0x00000000`

Width 32

3.3.180 failed_access_int_info_31_00

Shows information relating to the interrupt

The failed_access_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x538`

Type Read-only

Reset `0x00000000`

Width 32

3.3.181 failed_access_int_info_63_32

Shows information relating to the interrupt

The failed_access_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x53C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.182 failed_prog_int_info_31_00

Shows information relating to the interrupt

The failed_prog_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x540
Type Read-only
Reset 0x00000000
Width 32

3.3.183 failed_prog_int_info_63_32

Shows information relating to the interrupt

The failed_prog_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x544
Type Read-only
Reset 0x00000000
Width 32

3.3.184 link_err_int_info_31_00

Shows information relating to the interrupt

The link_err_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x548
Type Read-only
Reset 0x00000000
Width 32

3.3.185 link_err_int_info_63_32

Shows information relating to the interrupt

The link_err_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x54C
Type Read-only
Reset 0x00000000
Width 32

3.3.186 arch_fsm_int_info_31_00

Shows information relating to the interrupt

The arch_fsm_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x550`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.187 arch_fsm_int_info_63_32

Shows information relating to the interrupt

The arch_fsm_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x554`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.188 integ_cfg

Integration test register to enable integration test mode.

The integ_cfg register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0xE00`
Type	Read-write
Reset	`0x00000000`
Width	32

3.3.189 integ_outputs

Drives the value of outputs when in integration test mode.

The integ_outputs register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.
Attributes

Offset	`0xE08`
Type	Write-only
Reset	`0x00000000`
Width	32

3.3.190 address_control_now

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values.

The address_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1010`
Type	Read-only
Reset	`0x00030202`
Width	32

3.3.191 decode_control_now

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, bank, row address, and the column address.

The decode_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1014`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.192 address_map_now

Configures the system address mapping options.

The address_map_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x101C
Type Read-only
Reset 0x00000000
Width 32

3.3.193 low_power_control_now

Configures the low-power features of the DMC.

The low_power_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1020
Type Read-only
Reset 0x00000020
Width 32

3.3.194 turnaround_control_now

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus.

The turnaround_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1028
Type Read-only
Reset 0x0F0F0F0F
Width 32

3.3.195 hit_turnaround_control_now

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams.

The hit_turnaround_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x102C
Type Read-only
Reset 0x08909FBF
Width 32

3.3.196 qos_class_control_now

Configures the priority class for each QoS encoding.

The qos_class_control_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1030`

Type Read-only

Reset `0x00000FC8`

Width 32

3.3.197 escalation_control_now

Configures the settings for escalating the priority of entries in the queue.

The escalation_control_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1034`

Type Read-only

Reset `0x00080F03`

Width 32

3.3.198 qv_control_31_00_now

Configures the priority settings for each QoS encoding.

The qv_control_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1038`

Type Read-only

Reset `0x76543210`

Width 32

3.3.199 qv_control_63_32_now

Configures the priority settings for each QoS encoding.

The qv_control_63_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x103C`

Type Read-only

Reset `0xFEDCBA98`

Width 32

3.3.200 rt_control_31_00_now

Configures the timeout settings for each QoS encoding.

The rt_control_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1040`

Type Read-only

Reset `0x00000000`

Width 32

3.3.201 rt_control_63_32_now

Configures the timeout settings for each QoS encoding.

The rt_control_63_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1044`

Type Read-only

Reset `0x00000000`

Width 32

3.3.202 timeout_control_now

Configures the prescaler applied to timeout values.

The timeout_control_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1048
Type Read-only
Reset 0x00000001
Width 32

3.3.203 credit_control_now

Configures the settings for preventing starvation of CHI protocol retries.

The credit_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x104C
Type Read-only
Reset 0x00000F03
Width 32

3.3.204 write_priority_control_31_00_now

Configures the priority settings for write requests within the DMC

The write_priority_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1050
Type Read-only
Reset 0x00000000
Width 32

3.3.205 write_priority_control_63_32_now

Configures the priority settings for write requests within the DMC.

The write_priority_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1054
Type Read-only
Reset 0x00000000
Width 32

3.3.206 queue_threshold_control_31_00_now

Configures the threshold settings for requests in the DMC

The queue_threshold_control_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1060`

Type Read-only

Reset `0x00000000`

Width 32

3.3.207 queue_threshold_control_63_32_now

Configures the threshold settings for requests in the DMC

The queue_threshold_control_63_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1064`

Type Read-only

Reset `0x00000000`

Width 32

3.3.208 memory_address_max_31_00_now

Configures the address space control for the DMC default region.

The memory_address_max_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1078`

Type Read-only

Reset `0x00000010`

Width 32

3.3.209 memory_address_max_43_32_now

Configures the address space control for the DMC default region.

The memory_address_max_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x107C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.210 access_address_min0_31_00_now

Configures the address space control for address region 0.

The access_address_min0_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1080`

Type Read-only

Reset `0x00000000`

Width 32

3.3.211 access_address_min0_43_32_now

Configures the address space control for address region 0.

The access_address_min0_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1084`

Type Read-only

Reset `0x00000000`

Width 32

3.3.212 access_address_max0_31_00_now

Configures the address space control for address region 0.

The access_address_max0_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1088
Type Read-only
Reset 0x00000000
Width 32

3.3.213 access_address_max0_43_32_now

Configures the address space control for address region 0.

The access_address_max0_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x108C
Type Read-only
Reset 0x00000000
Width 32

3.3.214 access_address_min1_31_00_now

Configures the address space control for address region 1.

The access_address_min1_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1090
Type Read-only
Reset 0x00000000
Width 32

3.3.215 access_address_min1_43_32_now

Configures the address space control for address region 1.

The access_address_min1_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1094
Type Read-only
Reset 0x00000000
Width 32

3.3.216 access_address_max1_31_00_now

Configures the address space control for address region 1.

The access_address_max1_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1098`

Type Read-only

Reset `0x00000000`

Width 32

3.3.217 access_address_max1_43_32_now

Configures the address space control for address region 1.

The access_address_max1_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x109C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.218 access_address_min2_31_00_now

Configures the address space control for address region 2.

The access_address_min2_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10A0`

Type Read-only

Reset `0x00000000`

Width 32

3.3.219 access_address_min2_43_32_now

Configures the address space control for address region 2.

The access_address_min2_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10A4`

Type Read-only

Reset `0x00000000`

Width 32

3.3.220 access_address_max2_31_00_now

Configures the address space control for address region 2.

The access_address_max2_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10A8`

Type Read-only

Reset `0x00000000`

Width 32

3.3.221 access_address_max2_43_32_now

Configures the address space control for address region 2.

The access_address_max2_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10AC`

Type Read-only

Reset `0x00000000`

Width 32

3.3.222 access_address_min3_31_00_now

Configures the address space control for address region 3.

The access_address_min3_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10B0
Type Read-only
Reset 0x00000000
Width 32

3.3.223 access_address_min3_43_32_now

Configures the address space control for address region 3.

The access_address_min3_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10B4
Type Read-only
Reset 0x00000000
Width 32

3.3.224 access_address_max3_31_00_now

Configures the address space control for address region 3.

The access_address_max3_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10B8
Type Read-only
Reset 0x00000000
Width 32

3.3.225 access_address_max3_43_32_now

Configures the address space control for address region 3.

The access_address_max3_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10BC
Type Read-only
Reset 0x00000000
Width 32

3.3.226 access_address_min4_31_00_now

Configures the address space control for address region 4.

The access_address_min4_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10C0`

Type Read-only

Reset `0x00000000`

Width 32

3.3.227 access_address_min4_43_32_now

Configures the address space control for address region 4.

The access_address_min4_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10C4`

Type Read-only

Reset `0x00000000`

Width 32

3.3.228 access_address_max4_31_00_now

Configures the address space control for address region 4.

The access_address_max4_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10C8`

Type Read-only

Reset `0x00000000`

Width 32

3.3.229 access_address_max4_43_32_now

Configures the address space control for address region 4.

The access_address_max4_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10CC`

Type Read-only

Reset `0x00000000`

Width 32

3.3.230 access_address_min5_31_00_now

Configures the address space control for address region 5.

The access_address_min5_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10D0`

Type Read-only

Reset `0x00000000`

Width 32

3.3.231 access_address_min5_43_32_now

Configures the address space control for address region 5.

The access_address_min5_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10D4`

Type Read-only

Reset `0x00000000`

Width 32

3.3.232 access_address_max5_31_00_now

Configures the address space control for address region 5.

The access_address_max5_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10D8
Type Read-only
Reset 0x00000000
Width 32

3.3.233 access_address_max5_43_32_now

Configures the address space control for address region 5.

The access_address_max5_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10DC
Type Read-only
Reset 0x00000000
Width 32

3.3.234 access_address_min6_31_00_now

Configures the address space control for address region 6.

The access_address_min6_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10E0
Type Read-only
Reset 0x00000000
Width 32

3.3.235 access_address_min6_43_32_now

Configures the address space control for address region 6.

The access_address_min6_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10E4
Type Read-only
Reset 0x00000000
Width 32

3.3.236 access_address_max6_31_00_now

Configures the address space control for address region 6.

The access_address_max6_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10E8`

Type Read-only

Reset `0x00000000`

Width 32

3.3.237 access_address_max6_43_32_now

Configures the address space control for address region 6.

The access_address_max6_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10EC`

Type Read-only

Reset `0x00000000`

Width 32

3.3.238 access_address_min7_31_00_now

Configures the address space control for address region 7.

The access_address_min7_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10F0`

Type Read-only

Reset `0x00000000`

Width 32

3.3.239 access_address_min7_43_32_now

Configures the address space control for address region 7.

The access_address_min7_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10F4`

Type Read-only

Reset `0x00000000`

Width 32

3.3.240 access_address_max7_31_00_now

Configures the address space control for address region 7.

The access_address_max7_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10F8`

Type Read-only

Reset `0x00000000`

Width 32

3.3.241 access_address_max7_43_32_now

Configures the address space control for the address region 7.

The access_address_max7_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10FC`

Type Read-only

Reset `0x00000000`

Width 32

3.3.242 dci_replay_type_now

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command.

The dci_replay_type_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1110
Type Read-only
Reset 0x00000002
Width 32

3.3.243 refresh_control_now

Configures the type of refresh commands issued by the DMC.

The refresh_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1120
Type Read-only
Reset 0x00000000
Width 32

3.3.244 memory_type_now

Configures the DMC for the attached memory type.

The memory_type_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1128
Type Read-only
Reset 0x00000101
Width 32

3.3.245 scrub_control0_now

Scrub engine channel control register.

The scrub_control0_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1170
Type Read-only
Reset 0x1F000000

Width 32

3.3.246 scrub_address_min0_now

Configures the address space control for the scrub engine channel.

The scrub_address_min0_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1174`

Type Read-only

Reset `0x00000000`

Width 32

3.3.247 scrub_address_max0_now

Configures the address space control for the scrub engine channel.

The scrub_address_max0_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1178`

Type Read-only

Reset `0x00000000`

Width 32

3.3.248 scrub_control1_now

Scrub engine channel control register.

The scrub_control1_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1180`

Type Read-only

Reset `0x1F000000`

Width 32

3.3.249 scrub_address_min1_now

Configures the address space control for the scrub engine channel.

The scrub_address_min1_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1184`

Type Read-only

Reset `0x00000000`

Width 32

3.3.250 scrub_address_max1_now

Configures the address space control for the scrub engine channel.

The scrub_address_max1_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1188`

Type Read-only

Reset `0x00000000`

Width 32

3.3.251 scrub_control2_now

Scrub engine channel control register.

The scrub_control2_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1190`

Type Read-only

Reset `0x1F000000`

Width 32

3.3.252 scrub_address_min2_now

Configures the address space control for the scrub engine channel.

The scrub_address_min2_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1194
Type Read-only
Reset 0x00000000
Width 32

3.3.253 scrub_address_max2_now

Configures the address space control for the scrub engine channel.

The scrub_address_max2_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1198
Type Read-only
Reset 0x00000000
Width 32

3.3.254 scrub_control3_now

Scrub engine channel control register.

The scrub_control3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11A0
Type Read-only
Reset 0x1F000000
Width 32

3.3.255 scrub_address_min3_now

Configures the address space control for the scrub engine channel.

The scrub_address_min3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11A4
Type Read-only
Reset 0x00000000
Width 32

3.3.256 scrub_address_max3_now

Configures the address space control for the scrub engine channel.

The scrub_address_max3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11A8`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.257 scrub_control4_now

Scrub engine channel control register.

The scrub_control4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11B0`
Type	Read-only
Reset	`0x1F000000`
Width	32

3.3.258 scrub_address_min4_now

Configures the address space control for the scrub engine channel.

The scrub_address_min4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11B4`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.259 scrub_address_max4_now

Configures the address space control for the scrub engine channel.

The scrub_address_max4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11B8`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.260 scrub_control5_now

Scrub engine channel control register.

The scrub_control5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11C0`
Type	Read-only
Reset	`0x1F000000`
Width	32

3.3.261 scrub_address_min5_now

Configures the address space control for the scrub engine channel.

The scrub_address_min5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11C4`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.262 scrub_address_max5_now

Configures the address space control for the scrub engine channel.

The scrub_address_max5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11C8
Type Read-only
Reset 0x00000000
Width 32

3.3.263 scrub_control6_now

Scrub engine channel control register.

The scrub_control6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11D0
Type Read-only
Reset 0x1F000000
Width 32

3.3.264 scrub_address_min6_now

Configures the address space control for the scrub engine channel.

The scrub_address_min6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11D4
Type Read-only
Reset 0x00000000
Width 32

3.3.265 scrub_address_max6_now

Configures the address space control for the scrub engine channel.

The scrub_address_max6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11D8
Type Read-only
Reset 0x00000000
Width 32

3.3.266 scrub_control7_now

Scrub engine channel control register.

The scrub_control7_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x11E0`

Type Read-only

Reset `0x1F000000`

Width 32

3.3.267 scrub_address_min7_now

Configures the address space control for the scrub engine channel.

The scrub_address_min7_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x11E4`

Type Read-only

Reset `0x00000000`

Width 32

3.3.268 scrub_address_max7_now

Configures the address space control for the scrub engine channel.

The scrub_address_max7_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x11E8`

Type Read-only

Reset `0x00000000`

Width 32

3.3.269 feature_control_now

Control register for DMC features.

The feature_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11F0`
Type	Read-only
Reset	`0x0AA00000`
Width	32

3.3.270 mux_control_now

Control muxing options for the DMC.

The mux_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11F4`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.271 rank_remap_control_now

Control register for rank remap.

The rank_remap_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11F8`
Type	Read-only
Reset	`0x76543210`
Width	32

3.3.272 scrub_control_now

Scrub engine channel control register.

The scrub_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11FC
Type Read-only
Reset 0x00001F00
Width 32

3.3.273 t_refi_now

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8.

The t_refi_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1200
Type Read-only
Reset 0x00090100
Width 32

3.3.274 t_rfc_now

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank.

The t_rfc_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1204
Type Read-only
Reset 0x00008C23
Width 32

3.3.275 t_mrr_now

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank.

The t_mrr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1208
Type Read-only

Reset 0x00000002
Width 32

3.3.276 t_mrw_now

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank.

The t_mrw_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x120C
Type Read-only
Reset 0x0000000C
Width 32

3.3.277 t_rdpden_now

Configures the tRDPDEN timing parameter. This determines the delay applied after a Read command before a power down command can be issued to the same rank.

The t_rdpden_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1210
Type Read-only
Reset 0x0000000A
Width 32

3.3.278 t_rcd_now

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank.

The t_rcd_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1218
Type Read-only
Reset 0x00000005

Width 32

3.3.279 t_ras_now

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank.

The t_ras_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x121C`

Type Read-only

Reset `0x0000000E`

Width 32

3.3.280 t_rp_now

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank.

The t_rp_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1220`

Type Read-only

Reset `0x00000005`

Width 32

3.3.281 t_rpall_now

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank.

The t_rpall_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1224`

Type Read-only

Reset `0x00000005`

Width 32

3.3.282 t_rrd_now

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, and a different bank group, respectively, as described in the DDR4 specification.

The t_rrd_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1228`

Type Read-only

Reset `0x00000404`

Width 32

3.3.283 t_act_window_now

Configures the tFAW and tMAWi timing parameters.

The t_act_window_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x122C`

Type Read-only

Reset `0x03560014`

Width 32

3.3.284 t_rtr_now

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), and different chip-selects (t_rtr_cs).

The t_rtr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1234`

Type Read-only

Reset `0x00060404`

Width 32

3.3.285 t_rtw_now

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs).

The t_rtw_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1238`

Type Read-only

Reset `0x00060606`

Width 32

3.3.286 t_rtp_now

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank.

The t_rtp_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x123C`

Type Read-only

Reset `0x00000004`

Width 32

3.3.287 t_wr_now

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank.

The t_wr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1244`

Type Read-only

Reset `0x00000005`

Width 32

3.3.288 t_wtr_now

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs).

The t_wtr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1248`

Type Read-only

Reset `0x00040505`

Width 32

3.3.289 t_wtw_now

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes.

The t_wtw_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x124C`

Type Read-only

Reset `0x00060404`

Width 32

3.3.290 t_xmpd_now

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank.

The t_xmpd_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1254`

Type Read-only

Reset `0x000003FF`

Width 32

3.3.291 t_ep_now

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank.

The t_ep_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1258`

Type Read-only

Reset `0x00000002`

Width 32

3.3.292 t_xp_now

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL).

The t_xp_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x125C`

Type Read-only

Reset `0x00060002`

Width 32

3.3.293 t_esr_now

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank.

The t_esr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1260`

Type Read-only

Reset `0x0000000E`

Width 32

3.3.294 t_xsr_now

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank.

The t_xsr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1264`

Type Read-only

Reset `0x05120100`

Width 32

3.3.295 t_esrck_now

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state.

The t_esrck_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1268`

Type Read-only

Reset `0x00000005`

Width 32

3.3.296 t_ckxsr_now

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state.

The t_ckxsr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x126C`

Type Read-only

Reset `0x00000001`

Width 32

3.3.297 t_cmd_now

Configures command signaling timing.

The t_cmd_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1270`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.298 t_parity_now

Parity latencies t_parinlat and t_completion.

The t_parity_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1274`
Type	Read-only
Reset	`0x00000900`
Width	32

3.3.299 t_zqcs_now

Configures the delay to apply following a ZQC-Short calibration command.

The t_zqcs_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1278`
Type	Read-only
Reset	`0x00000040`
Width	32

3.3.300 t_rddata_en_now

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal.

The t_rddata_en_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1300`
Type	Read-only
Reset	`0x00000001`
Width	32

3.3.301 t_phyrdlat_now

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY.

The t_phyrdlat_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1304`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.302 t_phywrlat_now

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en, dfi_wrdata_cs and dfi_wrdata signals.

The t_phywrlat_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1308`
Type	Read-only
Reset	`0x00000001`
Width	32

3.3.303 rdlvl_control_now

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training.

The rdlvl_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1310
Type Read-only
Reset 0x00001080
Width 32

3.3.304 rdlvl_mrs_now

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration Manual for more information on PHY training.

The rdlvl_mrs_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1314
Type Read-only
Reset 0x00000004
Width 32

3.3.305 t_rdlvl_en_now

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training.

The t_rdlvl_en_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1318
Type Read-only
Reset 0x00000000
Width 32

3.3.306 t_rdlvl_rr_now

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp.

The t_rdlvl_rr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x131C
Type Read-only
Reset 0x00000000
Width 32

3.3.307 wrlvl_control_now

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training.

The wrlvl_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1320
Type Read-only
Reset 0x00001000
Width 32

3.3.308 wrlvl_mrs_now

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information.

The wrlvl_mrs_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1324
Type Read-only
Reset 0x00000086
Width 32

3.3.309 t_wrlvl_en_now

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training.

The t_wrlvl_en_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1328`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.310 t_wrlvl_ww_now

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp.

The t_wrlvl_ww_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x132C`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.311 phy_power_control_now

Configures the low-power requests made to the PHY for the different channel states.

The phy_power_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1348`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.312 t_lpresp_now

Configures the minimum cycle delay to apply for PHY low-power handshakes.

The t_lpresp_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x134C
Type Read-only
Reset 0x00000000
Width 32

3.3.313 phy_update_control_now

Configures the update mechanism to use in response to PHY training requests.

The phy_update_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1350
Type Read-only
Reset 0x0FE00000
Width 32

3.3.314 odt_timing_now

Configures the ODT on and off timing.

The odt_timing_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1358
Type Read-only
Reset 0x06000600
Width 32

3.3.315 odt_wr_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1360
Type Read-only
Reset 0x08040201
Width 32

3.3.316 odt_wr_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_63_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1364`

Type Read-only

Reset `0x80402010`

Width 32

3.3.317 odt_rd_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1368`

Type Read-only

Reset `0x00000000`

Width 32

3.3.318 odt_rd_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_63_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x136C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.319 dq_map_control_15_00_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_15_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1380`

Type Read-only

Reset `0x00000000`

Width 32

3.3.320 dq_map_control_31_16_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_31_16_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1384`

Type Read-only

Reset `0x00000000`

Width 32

3.3.321 dq_map_control_47_32_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_47_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1388`

Type Read-only

Reset `0x00000000`

Width 32

3.3.322 dq_map_control_63_48_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_63_48_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x138C`

Type Read-only

Reset `0x00000000`

Width 32

3.3.323 dq_map_control_71_64_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation.

The dq_map_control_71_64_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1390`

Type Read-only

Reset `0x00000000`

Width 32

3.3.324 user_config0_now

Drives the output user_config0 signal.

The user_config0_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1408`

Type Read-only

Reset `0x00000000`

Width 32

3.3.325 user_config1_now

Drives the output user_config1 signal.

The user_config1_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x140C`
Type	Read-only
Reset	`0x00000000`
Width	32

3.3.326 periph_id_4

Peripheral ID register.

The periph_id_4 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FD0`
Type	Read-only
Reset	`0x00000014`
Width	32

3.3.327 periph_id_0

Peripheral ID register.

The periph_id_0 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FE0`
Type	Read-only
Reset	`0x00000052`
Width	32

3.3.328 periph_id_1

Peripheral ID register.

The periph_id_1 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FE4
Type	Read-only
Reset	0x000000B4
Width	32

3.3.329 periph_id_2

Peripheral ID register.

The periph_id_2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FE8
Type	Read-only
Reset	0x0000003B
Width	32

3.3.330 periph_id_3

Peripheral ID register.

The periph_id_3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FEC
Type	Read-only
Reset	0x00000000
Width	32

3.3.331 component_id_0

Component ID register.

The component_id_0 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FF0
Type	Read-only
Reset	0x0000000D
Width	32

3.3.332 component_id_1

Component ID register.

The component_id_1 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FF4`
Type	Read-only
Reset	`0x000000F0`
Width	32

3.3.333 component_id_2

Component ID register.

The component_id_2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FF8`
Type	Read-only
Reset	`0x00000005`
Width	32

3.3.334 component_id_3

Component ID register.

The component_id_3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FFC`
Type	Read-only
Reset	`0x000000B1`
Width	32

Appendix A
Signal Descriptions

This appendix describes the DMC-520 signals.

It contains the following sections:

- *A.1 Signals list* on page Appx-A-145.

A.1 Signals list

DMC signals list that excludes bus interface signals. The bus interface signals are defined by their own bus protocol standard.

The following table shows the Primary clock and reset signals list of the DMC.

Table A-1 DMC Primary clock and reset signals list

Signal	Type	Width	Description
clk	Input	1	Primary DMC clock
dfi_clk	Input	1	DFI clock
resetn	Input	1	Primary DMC reset

The following table shows the APB clock and reset signals list of the DMC.

Table A-2 DMC APB clock and reset signals list

Signal	Type	Width	Description
pclk	Input	1	APB clock
presetn	Input	1	APB reset

The following table shows the User I/O with APB access list of the DMC.

Table A-3 DMC User I/O with APB access list

Signal	Type	Width	Description
user_status	Input	32	User defined inputs
user_config0	Output	32	User defined outputs
user_config1	Output	32	User defined outputs
user_config2	Output	32	User defined outputs
user_config3	Output	32	User defined outputs
user_periph_id_3	Input	8	Tie-off value to set the value of CMOD in the periph_id_3 bitfield

The following table shows the Events list of the DMC.

Table A-4 DMC Events list

Signal	Type	Width	Description
scrub_event_in0	Input	1	Scrub event 0 trigger.
scrub_event_in1	Input	1	Scrub event 1 trigger.
scrub_event_in2	Input	1	Scrub event 2 trigger.
scrub_event_in3	Input	1	Scrub event 3 trigger.
scrub_event_in4	Input	1	Scrub event 4 trigger.
scrub_event_in5	Input	1	Scrub event 5 trigger.
scrub_event_in6	Input	1	Scrub event 6 trigger.

Table A-4 DMC Events list (continued)

Signal	Type	Width	Description
scrub_event_in7	Input	1	Scrub event 7 trigger.
scrub_event_out0	Output	1	Scrub event 0 triggered.
scrub_event_out1	Output	1	Scrub event 1 triggered.
scrub_event_out2	Output	1	Scrub event 2 triggered.
scrub_event_out3	Output	1	Scrub event 3 triggered.
scrub_event_out4	Output	1	Scrub event 4 triggered.
scrub_event_out5	Output	1	Scrub event 5 triggered.
scrub_event_out6	Output	1	Scrub event 6 triggered.
scrub_event_out7	Output	1	Scrub event 7 triggered.
direct_cmd_event_in0	Input	1	Direct cmd event 0 trigger.
direct_cmd_event_in1	Input	1	Direct cmd event 1 trigger.
direct_cmd_event_in2	Input	1	Direct cmd event 2 trigger.
direct_cmd_event_in3	Input	1	Direct cmd event 3 trigger.
direct_cmd_event_out0	Output	1	Direct cmd event 0 triggered.
direct_cmd_event_out1	Output	1	Direct cmd event 1 triggered.
direct_cmd_event_out2	Output	1	Direct cmd event 2 triggered.
direct_cmd_event_out3	Output	1	Direct cmd event 3 triggered.

The following table shows the Scan Signals list of the DMC.

Table A-5 DMC Scan Signals list

Signal	Type	Width	Description
dftse	Input	1	DFT scan enable
dftclkcgen	Input	1	DFT clk clock gate enable
dftclkdiv2cgen	Input	1	DFT clkdiv2 clock gate enable
dftpclkcgen	Input	1	DFT pclk clock gate enable
dftrstdisable	Input	1	DFT reset synchronizer disable
dftramhold	Input	1	DFT on-chip RAM hold
dftmcphold	Input	1	DFT multi-cycle path hold

The following table shows the PMU Signals list of the DMC.

Table A-6 DMC PMU Signals list

Signal	Type	Width	Description
ev_request_valid_valid	Output	1	Indicates that ev_request_valid_payload is valid
ev_request_tzfail_valid	Output	1	Indicates that ev_request_tzfail_payload is valid
ev_request_retry_valid	Output	1	Indicates that ev_request_retry_payload is valid

Table A-6 DMC PMU Signals list (continued)

Signal	Type	Width	Description
ev_retry_grant_valid	Output	1	Indicates that ev_retry_grant_payload is valid
ev_request_valid_payload	Output	27	A request enters the DMC
ev_request_tzfail_payload	Output	22	A request fails an address translation or TrustZone permissions check
ev_request_retry_payload	Output	25	A request is retried
ev_retry_grant_payload	Output	15	Indicates that a P-credit has been granted.
ev_queue_fill_status_payload	Output	8	Count of entries in the DMC
ev_queued_reads_payload	Output	8	Count of read entries in the DMC
ev_queued_writes_payload	Output	8	Count of write entries in the DMC
ev_enqueued_reads_payload	Output	8	Count of read entries in the queue
ev_enqueued_writes_payload	Output	8	Count of write entries in the queue
ev_arbitrated_reads_payload	Output	8	Count of read entries in the arbitrated, without data state
ev_arbitrated_writes_payload	Output	8	Count of write entries in the arbitrated, not clean state
ev_read_backlog_payload	Output	8	Count of read entries in the backlog queue
ev_enqueue_backlog_payload	Output	8	Count of entries that are waiting to get enqueued
ev_hazard_resolution_backlog_payload	Output	8	Count of entries that are ready to be merged
ev_queue_allocation_backlog_payload	Output	8	Count of entries that in allocation backlog
ev_enqueue_valid	Output	1	Indicates that ev_enqueue_payload is valid
ev_arbitrate_valid	Output	1	Indicates that ev_arbitrate_payload is valid
ev_rank_targetted_valid	Output	RANKS_PER_CHANNEL	A rank is targeted by an enqueued entry
ev_enqueue_payload	Output	34	A request is enqueued in the arbitration queue
ev_arbitrate_payload	Output	12	A request is arbitrated from the arbitration queue
ev_allocate_valid	Output	1	Indicates that ev_allocate_payload is valid
ev_allocate_payload	Output	22	Maps sysid to allocated tag ID on entry to the DCB
ev_request_hazard_valid	Output	1	Indicates that ev_request_hazard_payload is valid
ev_request_hazard_payload	Output	2	A request forms a data hazard on an existing entry
ev_request_partial_valid	Output	1	A request is partial (not a complete burst)
ev_request_rmw_valid	Output	1	A request requires a read-modify-write
ev_ram_err_detect_valid	Output	9	Indicates that ev_ram_err_detect_payload is valid
ev_ram_err_detect_payload	Output	42	See ram_ecc_errd_int description
ev_ram_err_correct_valid	Output	9	Indicates that ev_ram_err_correct_payload is valid
ev_ram_err_correct_payload	Output	42	See ram_ecc_errc_int description
ev_dram_err_detect_valid	Output	1	Indicates that ev_dram_err_detect_payload is valid
ev_dram_err_detect_payload	Output	35	See dram_ecc_errd_int description

Table A-6 DMC PMU Signals list (continued)

Signal	Type	Width	Description
ev_dram_err_correct_valid	Output	1	Indicates that ev_dram_err_correct_payload is valid
ev_dram_err_correct_payload	Output	59	See dram_ecc_errc_int description
ev_turnaround_valid	Output	1	Indicates that ev_rank_turnaround_payload is valid
ev_activate_valid	Output	1	Indicates that ev_activate_payload is valid
ev_rdwr_valid	Output	1	Indicates that ev_rdwr_payload is valid
ev_precharge_valid	Output	1	Indicates that ev_precharge_payload is valid
ev_refresh_valid	Output	1	Indicates that ev_refresh_payload is valid
ev_turnaround_payload	Output	9	A turnaround has occurred
ev_activate_payload	Output	29	An ACTIVATE command has been sent
ev_rdwr_payload	Output	15	A READ/WRITE command has been sent
ev_precharge_payload	Output	9	A PRECHARGE command has been sent
ev_refresh_payload	Output	3	A REFRESH command has been sent
ev_pwr_state_active_valid	Output	MEMORY_CHIP_SELECTS	The rank is active
ev_pwr_state_idle_valid	Output	MEMORY_CHIP_SELECTS	The rank is idle
ev_pwr_state_pd_valid	Output	MEMORY_CHIP_SELECTS	The rank is in a POWER DOWN state
ev_pwr_state_sref_valid	Output	MEMORY_CHIP_SELECTS	The rank is in a SELF_REFRESH state
ev_bank_active_valid	Output	BANKS_PER_CHANNEL	A bank is active (has a row open)
ev_bank_busy_valid	Output	BANKS_PER_CHANNEL	A bank is busy (one or more timing parameters is being measured following an access)
ev_phy_update_req_valid	Output	1	Indicates that ev_phy_update_req_payload is valid
ev_phy_update_valid	Output	1	Indicates that ev_phy_update_payload is valid
ev_phy_update_req_payload	Output	4	A PHY update request has been received (update or training)
ev_phy_update_payload	Output	4	A PHY update request is in progress (update or training)
ev_phy_update_complete_valid	Output	1	A PHY update request has been completed (update or training)
ev_link_err_valid	Output	1	A link error has been detected
ev_tmac_limit_reached_valid	Output	1	Indicates that a bank row has reached the tMAC threshold for triggering a Target Row Refresh
ev_tmaw_tracker_full_valid	Output	1	Indicates that tMAC/tMAW tracking resource is full

The following table shows the Misc. signals list of the DMC.

Table A-7 DMC Misc. signals list

Signal	Type	Width	Description
memory_type	Output	3	An external output of the value of the memory_type register bitfield.

The following table shows the Tie-off signals list of the DMC.

Table A-8 DMC Tie-off signals list

Signal	Type	Width	Description
t_rddata_en_diff_tie_off	Input	6	Tie-off value for reset of register bitfield t_rddata_en_diff
t_phyrdcslat_tie_off	Input	5	Tie-off value for reset of register bitfield t_phyrdcslat
t_phyrdlat_tie_off	Input	7	Tie-off value for reset of register bitfield t_phyrdlat
t_phywrlat_diff_tie_off	Input	5	Tie-off value for reset of register bitfield t_phywrlat_diff
t_phywrcslat_tie_off	Input	5	Tie-off value for reset of register bitfield t_phywrcslat
t_phywrdata_tie_off	Input	1	Tie-off value for reset of register bitfield t_phywrdata
refresh_dur_rdlvl_tie_off	Input	1	Tie-off value for reset of register bitfield refresh_dur_rdlvl
t_rdlvl_en_tie_off	Input	6	Tie-off value for reset of register bitfield t_rdlvl_en
t_rdlvl_rr_tie_off	Input	10	Tie-off value for reset of register bitfield t_rdlvl_rr
refresh_dur_wrlvl_tie_off	Input	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl
t_wrlvl_en_tie_off	Input	6	Tie-off value for reset of register bitfield t_wrlvl_en
t_wrlvl_ww_tie_off	Input	10	Tie-off value for reset of register bitfield t_wrlvl_ww
t_lpresp_tie_off	Input	6	Tie-off value for reset of register bitfield t_lpresp
user_config0_tie_off	Input	32	Tie-off value for reset of register bitfield user_config0
user_config1_tie_off	Input	32	Tie-off value for reset of register bitfield user_config1
user_config2_tie_off	Input	32	Tie-off value for reset of register bitfield user_config2
user_config3_tie_off	Input	32	Tie-off value for reset of register bitfield user_config3

The following table shows the Tie-off values for AMBA5 CHI list of the DMC.

Table A-9 DMC Tie-off values for AMBA5 CHI list

Signal	Type	Width	Description
system_id	Input	SKY_RSP_FLIT_SRCID_WIDTH	Tie-off value to set the physical node ID of the DMC
home_node_id	Input	(SKY_REQ_FLIT_SRCID_WIDTH*SYSTEM_REQUESTORS)	Tie off value to specify the concatenated physical node IDs of up to 8 Home Nodes that are permitted to access the DMC

The following table shows the APB Interface bus list of the DMC.

Table A-10 DMC APB Interface list

Name	Width	Description
paddr	32	APB address
psel		APB select
penable		APB enable
pwrite		APB write
pwdata	32	APB write data

Table A-10 DMC APB Interface list (continued)

Name	Width	Description
pready		APB ready
prdata	32	APB read data
pslverr		APB error signal

The following table shows the DFI Interface bus list of the DMC.

Table A-11 DMC DFI Interface list

Name	Width	Description
dfi_address_p0	18	Address to DDR3 PHY
dfi_address_p1	18	Address to DDR3 PHY
dfi_address_p2	18	Address to DDR3 PHY
dfi_address_p3	18	Address to DDR3 PHY
dfi_bank_p0	3	Bank Address to PHY
dfi_bank_p1	3	Bank Address to PHY
dfi_bank_p2	3	Bank Address to PHY
dfi_bank_p3	3	Bank Address to PHY
dfi_ras_n_p0	1	Row address strobe to PHY
dfi_ras_n_p1	1	Row address strobe to PHY
dfi_ras_n_p2	1	Row address strobe to PHY
dfi_ras_n_p3	1	Row address strobe to PHY
dfi_cas_n_p0	1	Column address strobe to PHY
dfi_cas_n_p1	1	Column address strobe to PHY
dfi_cas_n_p2	1	Column address strobe to PHY
dfi_cas_n_p3	1	Column address strobe to PHY
dfi_we_n_p0	1	Write enable to PHY
dfi_we_n_p1	1	Write enable to PHY
dfi_we_n_p2	1	Write enable to PHY
dfi_we_n_p3	1	Write enable to PHY
dfi_cs_n_p0	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_cs_n_p1	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_cs_n_p2	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_cs_n_p3	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_act_n_p0	1	Activate to PHY
dfi_act_n_p1	1	Activate to PHY
dfi_act_n_p2	1	Activate to PHY
dfi_act_n_p3	1	Activate to PHY

Table A-11 DMC DFI Interface list (continued)

Name	Width	Description
dfi_bg_p0	2	Bank group address to PHY
dfi_bg_p1	2	Bank group address to PHY
dfi_bg_p2	2	Bank group address to PHY
dfi_bg_p3	2	Bank group address to PHY
dfi_cid_p0	3	Chip ID to PHY
dfi_cid_p1	3	Chip ID to PHY
dfi_cid_p2	3	Chip ID to PHY
dfi_cid_p3	3	Chip ID to PHY
dfi_cke_p0	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_cke_p1	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_cke_p2	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_cke_p3	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_odt_p0	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_odt_p1	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_odt_p2	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_odt_p3	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_reset_n_p0	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_reset_n_p1	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_reset_n_p2	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_reset_n_p3	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_parity_in_p0	1	Command parity to PHY
dfi_parity_in_p1	1	Command parity to PHY
dfi_parity_in_p2	1	Command parity to PHY
dfi_parity_in_p3	1	Command parity to PHY
dfi_wrdata_en_p0	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_en_p1	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_en_p2	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_en_p3	(DFI_DATA_SLICES)	Write data enable PHY
dfi_wrdata_p0	(DFI_DATA_BITS)	Write data to PHY
dfi_wrdata_p1	(DFI_DATA_BITS)	Write data to PHY
dfi_wrdata_p2	(DFI_DATA_BITS)	Write data to PHY
dfi_wrdata_p3	(DFI_DATA_BITS)	Write data to PHY
dfi_wrdata_cs_n_p0	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_cs_n_p1	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_cs_n_p2	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY

Table A-11 DMC DFI Interface list (continued)

Name	Width	Description
dfi_wrdata_cs_n_p3	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_mask_p0	(DFI_DATA_BYTES)	Write data mask PHY
dfi_wrdata_mask_p1	(DFI_DATA_BYTES)	Write data mask PHY
dfi_wrdata_mask_p2	(DFI_DATA_BYTES)	Write data mask PHY
dfi_wrdata_mask_p3	(DFI_DATA_BYTES)	Write data mask PHY
dfi_rddata_en_p0	(DFI_DATA_SLICES)	Enable for read data
dfi_rddata_en_p1	(DFI_DATA_SLICES)	Enable for read data
dfi_rddata_en_p2	(DFI_DATA_SLICES)	Enable for read data
dfi_rddata_en_p3	(DFI_DATA_SLICES)	Enable for read data
dfi_rddata_p0	(DFI_DATA_BITS)	Read data input from PHY
dfi_rddata_p1	(DFI_DATA_BITS)	Read data input from PHY
dfi_rddata_p2	(DFI_DATA_BITS)	Read data input from PHY
dfi_rddata_p3	(DFI_DATA_BITS)	Read data input from PHY
dfi_rddata_dbi_n_p0	(DFI_DATA_BYTES) * 2	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal should be tied to 'b1.
dfi_rddata_dbi_n_p1	(DFI_DATA_BYTES) * 2	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal should be tied to 'b1.
dfi_rddata_dbi_n_p2	(DFI_DATA_BYTES) * 2	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal should be tied to 'b1.
dfi_rddata_dbi_n_p3	(DFI_DATA_BYTES) * 2	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal should be tied to 'b1.
dfi_rddata_valid_p0	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_valid_p1	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_valid_p2	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_valid_p3	(DFI_DATA_SLICES)	Indicates read data valid
dfi_rddata_cs_n_p0	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_rddata_cs_n_p1	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_rddata_cs_n_p2	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_rddata_cs_n_p3	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_ctrlupd_req	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_ctrlupd_ack	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_phyupd_req	1	DFI PHY-initiated update request
dfi_phyupd_ack	1	DFI PHY-initiated update acknowledge
dfi_phyupd_type	2	DFI PHY-initiated update type
dfi_data_byte_disable	(DFI_DATA_BYTES)	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_dram_clk_disable	MEMORY_CHIP_SELECTS	DRAM clock disable to PHY

Table A-11 DMC DFI Interface list (continued)

Name	Width	Description
dfi_init_start	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_init_complete	1	Indicates PHY initialization complete
dfi_alert_n_p0	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_alert_n_p1	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_alert_n_p2	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_alert_n_p3	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_err	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_err_info	4	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_phylvl_req_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_phylvl_ack_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_rdlvl_req	1	DFI read data eye training request
dfi_rdlvl_cs_n	MEMORY_CHIP_SELECTS	DFI read data eye training request target chip-select
dfi_rdlvl_periodic	1	DFI read data eye training request periodic
dfi_rdlvl_en	1	DFI read data eye training enable
dfi_rdlvl_resp	1	DFI read data eye training response
dfi_rdlvl_gate_req	1	DFI read gate training request
dfi_rdlvl_gate_cs_n	MEMORY_CHIP_SELECTS	DFI read gate training request target chip-select
dfi_rdlvl_gate_periodic	1	DFI read gate training request periodic
dfi_rdlvl_gate_en	1	DFI read gate training enable
dfi_rdlvl_gate_resp	1	DFI read gate training response
dfi_wrlvl_req	1	DFI write leveling training request
dfi_wrlvl_cs_n	MEMORY_CHIP_SELECTS	DFI write leveling training request target chip-select
dfi_wrlvl_periodic	1	DFI write leveling training request periodic
dfi_wrlvl_en	1	DFI write leveling training enable
dfi_wrlvl_strobe	1	DFI write leveling training strobe
dfi_wrlvl_resp	1	DFI write leveling training response
dfi_lvl_pattern	4	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_lvl_periodic	1	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_lvl_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.0, see JEDEC specification for details.
dfi_ref_en	1	DFI refresh during training enable
dfi_lp_ctrl_req	1	DFI command low power request
dfi_lp_data_req	1	DFI data low power request
dfi_lp_wakeup	4	DFI command low power PHY wakeup allowance
dfi_lp_ack	1	DFI command low power acknowledge

The following table shows the Q-Channel Interface for DMC bus list of the DMC.

Table A-12 DMC Q-Channel Interface for DMC list

Name	Width	Description
qreqn	1	Request from the external clock controller to prepare to stop the clock
qacceptn	1	Positive acknowledgement after receiving QREQn assertion indicating that the DMC has completed preparation to stop the clocks and that the external clock controller can stop the clock
qdeny	1	Negative acknowledgement after receiving QREQn assertion indicating that the DMC has refused the request from the external clock controller to prepare to stop the clock
qactive	1	Indication that the DMC is active

The following table shows the Q-Channel Interface for APB interface bus list of the DMC.

Table A-13 DMC Q-Channel Interface for APB interface list

Name	Width	Description
qreqn_apb	1	Request from the external clock controller to prepare to stop the clock
qacceptn_apb	1	Positive acknowledgement after receiving QREQn assertion indicating that the APB interface has completed preparation to stop the clocks and that the external clock controller can stop the clock
qdeny_apb	1	Negative acknowledgement after receiving QREQn assertion indicating that the APB interface has refused the request from the external clock controller to prepare to stop the clock
qactive_apb	1	Indication that the APB interface is active

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-14 DMC Clock Frequency Change Interface list

Name	Width	Description
cc_frequency	5	Used to indicate new frequency as part of frequency change protocol
cc_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
cc_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-15 DMC Clock Frequency Change Interface list

Name	Width	Description
dfi_frequency	5	Used to indicate new frequency as part of frequency change protocol
dfi_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
dfi_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Abort Interface bus list of the DMC.

Table A-16 DMC Abort Interface list

Name	Width	Description
abort_req	1	An input to abort retries in the face of DFI link errors.
abort_ack	1	An output to acknowledge that the DMC has completed outstanding transactions as a result of an abort.

The following table shows the Memory BIST interface bus list of the DMC.

Table A-17 DMC Memory BIST interface list

Name	Width	Description
mbistresetn	1	MBIST reset. Active low.
mbistreq	1	MBIST request
mbistack	1	MBIST acknowledge
mbistwriteen	1	MBIST write enable
mbistreaden	1	MBIST read enable
mbistaddr	7	MBIST address
mbistarray	5	MBIST array selection
mbistindata	154	MBIST write data
mbistoutdata	154	MBIST read data

The following table shows the Interrupt Interface bus list of the DMC.

Table A-18 DMC Interrupt Interface list

Name	Width	Description
ram_ecc_errc_int	1	The DMC has detected a correctable error in an internal RAM

The following table shows the Interrupt Interface bus list of the DMC.

Table A-19 DMC Interrupt Interface list

Name	Width	Description
ram_ecc_errd_int	1	The DMC has detected an un-correctable error in an internal RAM

The following table shows the Interrupt Interface bus list of the DMC.

Table A-20 DMC Interrupt Interface list

Name	Width	Description
dram_ecc_errc_int	1	The DMC has detected a correctable error in a DRAM burst

The following table shows the Interrupt Interface bus list of the DMC.

Table A-21 DMC Interrupt Interface list

Name	Width	Description
dram_ecc_errd_int	1	The DMC has detected a data failure that could not be corrected in a DRAM burst operation

The following table shows the Interrupt Interface bus list of the DMC.

Table A-22 DMC Interrupt Interface list

Name	Width	Description
failed_access_int	1	The DMC has detected a system request that has failed a permissions check

The following table shows the Interrupt Interface bus list of the DMC.

Table A-23 DMC Interrupt Interface list

Name	Width	Description
failed_prog_int	1	The DMC has detected a programming request that is not permitted

The following table shows the Interrupt Interface bus list of the DMC.

Table A-24 DMC Interrupt Interface list

Name	Width	Description
link_err_int	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun

The following table shows the Interrupt Interface bus list of the DMC.

Table A-25 DMC Interrupt Interface list

Name	Width	Description
temperature_event_int	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor

The following table shows the Interrupt Interface bus list of the DMC.

Table A-26 DMC Interrupt Interface list

Name	Width	Description
arch_fsm_int	1	The DMC has detected a change in the architectural state.

The following table shows the Interrupt Interface bus list of the DMC.

Table A-27 DMC Interrupt Interface list

Name	Width	Description
phy_request_int	1	The DMC has detected a PHY request.

The following table shows the Interrupt Interface bus list of the DMC.

Table A-28 DMC Interrupt Interface list

Name	Width	Description
combined_int	1	A combined interrupt that is the logical OR of the other interrupts.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-29 DMC Interrupt Overflow list

Name	Width	Description
ram_ecc_errc_oflow	1	The DMC has detected a correctable error in an internal RAM and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-30 DMC Interrupt Overflow list

Name	Width	Description
ram_ecc_errd_oflow	1	The DMC has detected a un-correctable error in an internal RAM and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-31 DMC Interrupt Overflow list

Name	Width	Description
dram_ecc_errc_oflow	1	The DMC has detected a correctable error in a DRAM burst and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-32 DMC Interrupt Overflow list

Name	Width	Description
dram_ecc_errd_oflow	1	The DMC has detected a data failure that could not be corrected in a DRAM burst operation and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-33 DMC Interrupt Overflow list

Name	Width	Description
failed_access_oflow	1	The DMC has detected a system request that has failed a permissions check and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-34 DMC Interrupt Overflow list

Name	Width	Description
failed_prog_oflow	1	The DMC has detected a programming request that is not permitted and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-35 DMC Interrupt Overflow list

Name	Width	Description
link_err_oflow	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-36 DMC Interrupt Overflow list

Name	Width	Description
temperature_event_oflow	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-37 DMC Interrupt Overflow list

Name	Width	Description
arch_fsm_oflow	1	The DMC has detected a change in the architectural state and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-38 DMC Interrupt Overflow list

Name	Width	Description
phy_request_oflow	1	The DMC has detected a PHY request and a previously detected assertion was not cleared.

The following table shows the Interrupt Overflow bus list of the DMC.

Table A-39 DMC Interrupt Overflow list

Name	Width	Description
combined_oflow	1	A combined interrupt that is the logical OR of the other interrupt overflows.

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following sections:

- *B.1 Revisions* on page Appx-B-160.

B.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue 0000-00

Change	Location	Affects
First release	-	-

Table B-2 Differences between issue 0000-00 and issue 0001-00

Change	Location	Affects
Updated the programmable registers	*3.2 Register summary* on page 3-32	All revisions
Updated the DIMM support list	*2.4 Constraints and limitations of use* on page 2-29	All revisions

Table B-3 Differences between issue 0001-00 and issue 0100-00

Change	Location	Affects
Added 32-bit memory width support to the memory interface	*1.3 Features* on page 1-14	r1p0
Added the format control register	*3.3.6 format_control* on page 3-45	r1p0

Table B-4 Differences between issue 0100-00 and issue 0200-00

Change	Location	Affects
Updated the Memory interface support	*1.3 Features* on page 1-14	r2p0
Updated configurable DFI options for clocks	• *1.5 Configurable options* on page 1-16 • *2.2 Clocking and resets* on page 2-24 • *2.3.3 PHY interface* on page 2-25	r2p0
Updated the System interface information	*2.1 About the functions* on page 2-22	r2p0
Added note about exclusive access	*2.3.1 System interface* on page 2-25	r2p0
Updated the DIMM support list	*2.4 Constraints and limitations of use* on page 2-29	r2p0

Table B-5 Differences between issue 0200-00 and issue 0200-01

Change	Location	Affects
There are no technical changes	-	-

Table B-6 Differences between issue 0200-01 and issue 0200-02

Change	Location	Affects
Clarified the RAS description	*2.1 About the functions* on page 2-22	r2p1
Clarified the Abort interface content	*2.3.6 Abort interface* on page 2-28	r2p1
Updated constraints and limitations of use	*2.4 Constraints and limitations of use* on page 2-29	r2p1

Table B-7 Differences between issue 0200-02 and issue 0202-00

Change	Location	Affects
There are no technical changes	-	-